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Research Article

Optimization of CNFET Parameters for High Performance Digital Circuits

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The Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising candidates to become successor of silicon CMOS in the near future because of its better electrostatics and higher mobility. The CNFET has many parameters such as operating voltage, number of tubes, pitch, nanotube diameter, dielectric constant, and contact materials which determine the digital circuit performance. This paper presents a study that investigates the effect of different CNFET parameters on performance and proposes a new CNFET design methodology to optimize performance characteristics such as current driving capability, delay, power consumption, and area for digital circuits. We investigate and conceptually explain the performance measures at 32 nm technologies for pure-CNFET, hybrid MOS-CNFET, and CMOS configurations. In our proposed design methodology, the power delay product (PDP) of the optimized CNFET is about 68%, 63%, and 79% less than that of the nonoptimized CNFET, hybrid MOS-CNFET, and CMOS circuits, respectively. Therefore, the proposed CNFET design is a strong candidate to implement high performance digital circuits.

1. Introduction

CMOS technology faces significant challenges at the nanoscale due to several factors like short-channel effects, a lack of control over static leakage current and source-to-drain tunneling [1, 2]. Now in order to sustain Moore's Law, it is necessary to look for alternatives like Carbon Nanotube Field Effect Transistors (CNFETs) that have received a lot of attention in the past few years as a promising extension to silicon CMOS for future digital logic integrated circuits. CNFETs show desirable characteristics such as high mobility of electrons movement near ballistic transport and the ability to carry large current and smaller device footprint as compared to conventional Si-MOSFETs [3]. Carbon nanotubes (CNTs) are a promising material for flexible electronics which offer a wide variety of applications such as flexible solar cells, skin-like pressure sensors, and conformable RFID tags [4].

CNFET has many applications in digital circuits such as arithmetic circuits, Full Adder-Subtractor [5–7], and 6T SRAM [8] and there is hybridization between MOS and CNFET to improve performance for digital [9] or analog design [10]. Efforts have been made in recent years on modeling and simulating CNT related devices such as CNFET [11, 12] to evaluate the potential performance at the device level. Various optimized schemes are suggested and demonstrated to minimize the effect of parasitic capacitances and thus improve the speed of CNT ICs [13].

There has been a previous work which investigates optimum design parameters to propose the suitability of pure and hybrid CMOS-CNFET in a wide range of high performance analog circuits [14]. In this paper, we discuss the design parameters of the CNFETs and show how to optimize these parameters for obtaining high performance CNFET for digital circuit implementation. The optimization is performed using HSPICE for extensive simulations. The results obtained are useful for understanding the design parameters of near ballistic CNFETs and for identifying important issues to further improve CNFET performance.

This paper is organized as follows: the structure and basic characteristics for CNFETs are discussed in Section 2. Section 3 describes the effect of all design parameters on

the performance of CNFETs. Section 4 gives the results and discussion. Finally, a concluding remark is given.

2. Carbon Nanotube Field Effect Transistors (CNFETs)

Both theory and experiments have demonstrated that a single walled carbon nanotube (SWCNT) can be either metallic or semiconducting, depending upon the arrangement of carbon atoms. This is decided by its chirality (Ch) whose magnitude is given by (1) and its relationship with CNT diameter (D_{CNT}) is given by (2), where "a" is the graphene lattice constant (0.249 nm) and n_1, n_2 are positive integers that specify the chirality of the tube

$$\mathrm{Ch} = a\sqrt{n_1^2 + n_2^2 + n_1 n_2}, \tag{1}$$

$$D_{\mathrm{CNT}} = \frac{\mathrm{Ch}}{\pi}. \tag{2}$$

CNFETs use a number of semiconducting SWCNTs as a transistor channel, as shown in Figure 1. The two ungated portions source and drain are heavily doped semiconducting CNTs with Palladium (Pd) as metal contacts while the CNT channel is undoped. The CNFET operates similar to that of a traditional MOSFET. The CNFET exhibits unipolar behavior and operates on the principle of barrier height modulation when applying a gate potential [14]. The CNFET offers many potential advantages with respect to silicon-based technology. This is due to its excellent electrical and structural characteristics such as quasi-1D ballistic transport of electrons, higher drive current, large transconductance, near ideal subthreshold slope, low intrinsic capacitance, and strong covalent bonding [15].

The CNT diameters, the channel width (W) of the CNFET transistor, the number of CNTs (N) in the channel of a CNFET, and internanotube spacing (S) are related by (3). The band gap energy (E_g) and the threshold voltage (V_{th}) of the intrinsic CNT channel are related by (4):

$$W = (N - 1)\, S + D_{\mathrm{CNT}}, \tag{3}$$

$$V_{\mathrm{th}} \approx \frac{E_g}{2 \cdot e}. \tag{4}$$

The high performance HSPICE model has been used for analyzing the performance of CNFET transistor and 32 nm Si-MOSFET. The CNFET model successfully accounts for its device parasitic and practical nonidealities. Apart from accurate predictions of dynamic and transient performances, the model gives more than 90% accuracy [11].

3. Optimization of Pure-CNFET Parameters

This section presents our simulation experiments to optimize the design parameters of the pure-CNFET. The pure-CNFET is designed in terms of optimum structural device parameters such as CNT diameter (D_{CNT}), number of perfectly aligned nanotubes (N) with uniform internanotube spacing (S), and

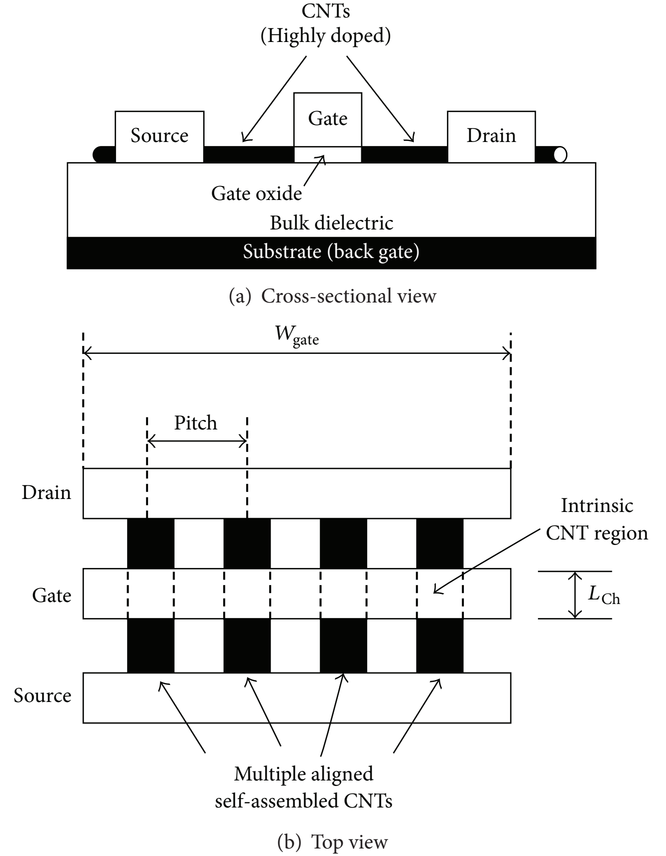


Figure 1: CNFET structure.

oxide thickness (T_{ox}) in addition to the selection of operating supply voltage. In these simulation experiments, the channel length of the CNFET is adjusted at 32 nm to be identical with that of Si-MOSFET for a fair comparison.

The optimization results presented in this section are obtained from several runs with different setups, where the original parameter values are listed in Table 3.

3.1. Optimum Supply Voltage. Both the static and dynamic powers will decrease with decreasing the supply voltage (V_{dd}); that is, an effective way to reduce the power dissipation is to scale down the supply voltage of the circuit [15]. Extensive simulation experiments using HSPICE are carried out to study the effect of V_{dd} on the delay and power consumption of CNFET, hybrid (NMOS-PCNFET), and CMOS inverters at 32 nm technology node. Figure 2 gives the simulation results of the average delay at different values for the supply voltage. It is observed from Figure 2 that hybrid inverter has shorter delay than the conventional MOS at all values of the supply voltage. But CNFET inverter has the shortest delay due to its higher current driving capability. The CNFET-based inverter does not offer minimum power consumption as shown in Figure 3. To obtain low PDP with acceptable supply voltage, the 0.6 V is chosen as a supply voltage.

3.2. Optimum CNT Diameter. Diameter is the main parameter that affects the on-current proportionally in a CNFET.

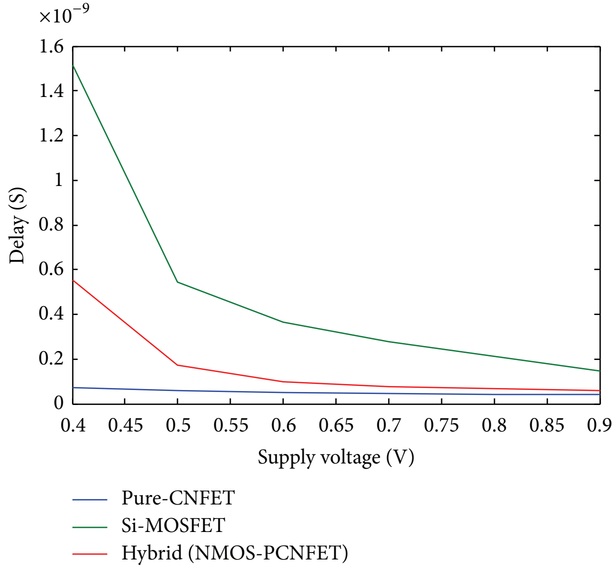


Figure 2: The propagation delay of pure-CNFET, hybrid and CMOS inverters for different supply voltages.

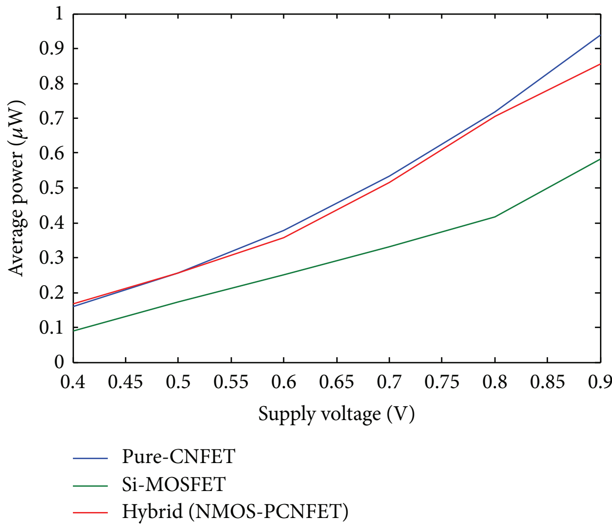


Figure 3: The average power consumption of pure-CNFET, hybrid, and CMOS inverter for different supply voltages.

Table 1: Showing different diameter values with V_{th} and I_{on}/I_{off} ratio.

Chirality	(13, 0)	(17, 0)	(19, 0)	(22, 0)	(26, 0)
Diameter (nm)	1	1.33	1.49	1.72	2
V_{th} (V)	0.422	0.32	0.3	0.24	0.2
I_{on}/I_{off} (xE04)	1192	55.5	22.8	6.95	2.016

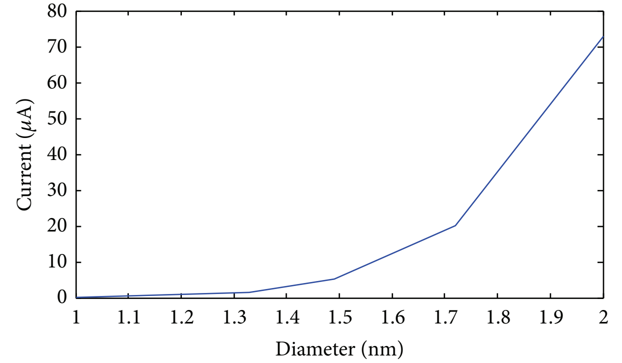


Figure 4: The current with variations of diameter of CNT for pure-CNFET.

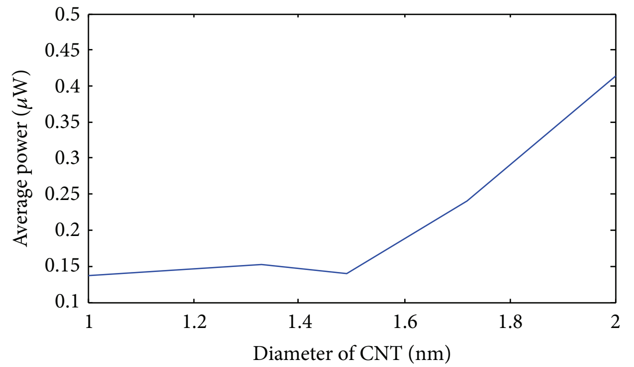


Figure 5: Effect of diameter variations on average power consumption for pure technology design.

Using a larger diameter reduces the band gap; therefore the on-current increases as shown in Figure 4. This is because the transconductance goes up with the increase in diameter of the nanotubes.

But at the same time, the leakage current is increased as well. The simulation results are illustrated in Table 1 showing degradation in I_{on} to I_{off} current ratio. This problem should be handled with care, because digital circuits require high on-currents, but also very low off-currents.

As shown in Figure 5 large diameter deteriorates the power handling capability as CNTs become more conducting. This is due to the inversely relation between the diameter and V_{th}. When V_{th} decreases for large diameter, the power consumption will increase. However, the switching speed increases and the device approach saturation faster. This is also observed in Figures 6 and 7 showing the large effect of diameter variations on delay and PDP for pure technology design.

Furthermore, the selection of the suitable diameter will depend on the value of PDP. The optimum diameter is 1.49 nm which is determined according to chiral vector (19, 0) of the nanotubes.

3.3. Optimum Number of CNTs. Single nanotube based transistor is not suitable to provide competitive performance over a traditional MOSFET. It is necessary to determine the number of CNTs to be used in an array in order to guarantee sufficient current supply.

In this section the problem associated with large number of tubes is investigated in addition to geometrical constraints. The on-current approximately is given by (5), where g_{CNT} is

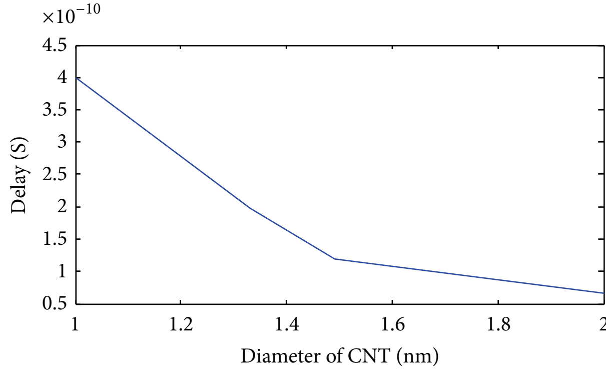


Figure 6: Effect of diameter variations on average delay for pure technology design.

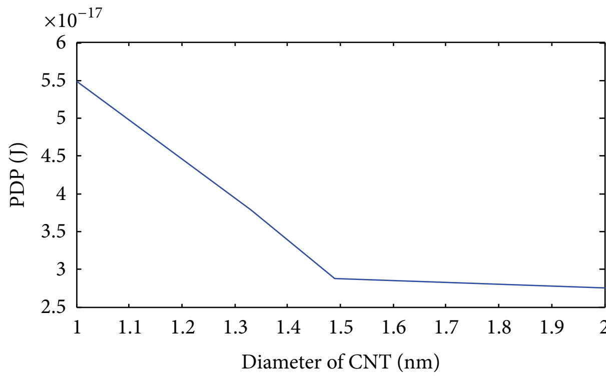


Figure 7: Effect of diameter variations on PDP for pure technology design.

the transconductance per CNT, L_s is the source length (doped CNT region), and ρ_s is the source resistance per unit length of doped CNT [11]:

$$I_{\text{CNFET}} \approx \frac{N g_{\text{CNT}} \left(V_{\text{dd}} - V_{\text{th}}\right)}{1 + g_{\text{CNT}} L_s \rho_s}. \quad (5)$$

It is worth noting that the total current drive in a CNFET depends on the number of CNTs per device ("N"). This explains the increase in current driving capability of the device with increasing the number of CNTs.

However, increase in number of CNT also incurs penalty in power dissipation which is clear in Figure 8.

The percentage of decreasing delay with N is larger than the increasing of average power consumption as shown in Figure 9. Thus, keeping all the design metrics such as power, delay, and PDP in mind, it is observed from Figure 10 that the PDP decreases with increase in number of CNT. This is due to the increase in the driving current and hence reduction in delay, which outweighs the increase in power dissipation.

We conclude that the upper limit on the number of CNTs used is determined by the power-performance trade-off but still looking at the overall performance merits. To maximize circuit performance at the 32 nm node, a minimum CNT density of 200 CNTs per μm gate width is desired [16]. Also in another research the optimum value of "N" comes out to

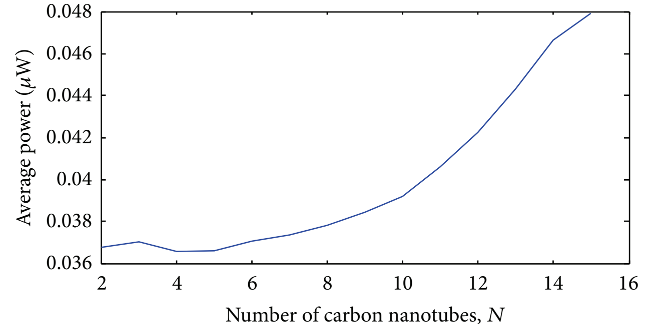


Figure 8: Average power versus number of carbon nanotubes for pure-CNFET inverter.

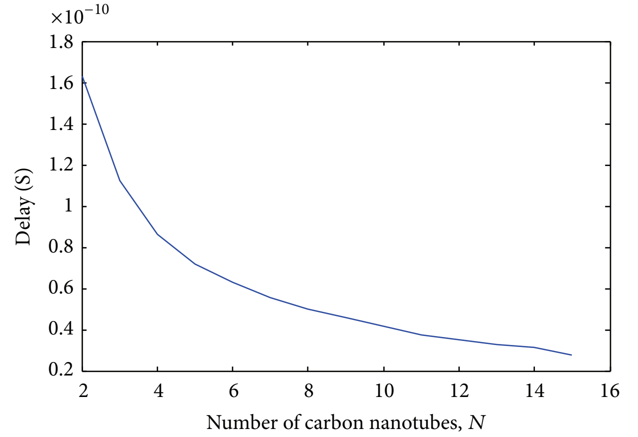


Figure 9: Delay versus number of carbon nanotubes for pure-CNFET inverter.

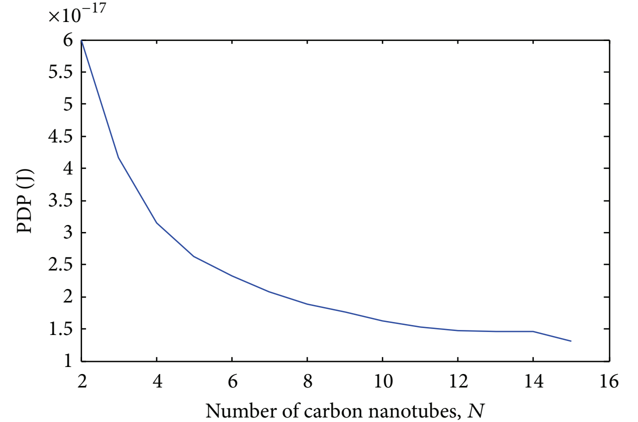


Figure 10: PDP versus number of carbon nanotubes for pure-CNFET inverter.

be 250/μm with equal spacing [10] which is nearly matched with our optimization. From previous results, the optimum number of CNT is 8.

3.4. Optimum Internanotube Spacing. The drain current of the CNFET is dependent on pitch value (internanotube spacing), which determines the amount of screening effect.

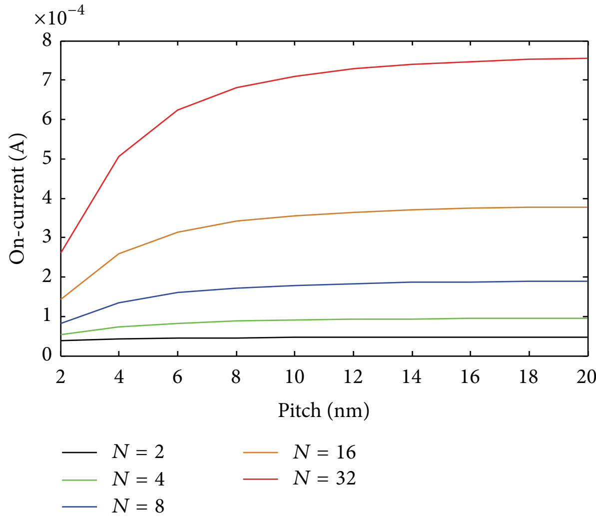
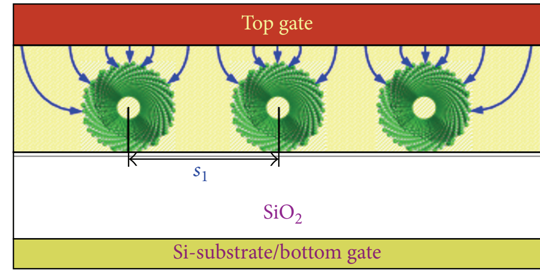
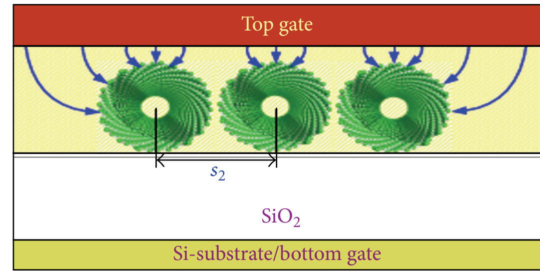


Figure 11: On-current versus pitch for different number of carbon nanotubes.



(a) The channel contains multiple tubes ($N = 3$) with large intertube pitch s_1



(b) The channel contains multiple tubes ($N = 3$) with a smaller intertube pitch s_2

Figure 12: Cross-sectional view of a multitube CNFET.

Figure 11 shows the drain current with different values of pitch and number of tubes.

I_{on}/I_{off} can be enhanced by increasing the pitch due to weakening the charge screening effect. However a larger pitch degrades the integration density. So, the trade-off between I_{on}/I_{off} and area efficiency must be considered.

With decreased intertube spacing (pitch), the gate-to-channel capacitance and the resulting current produced by a nanotube are reduced due to increasing screening effect which is shown in Figure 12. Charge screening reduces the effective width of the channel, thereby degrading the device current [11, 17]. But shorter pitches are desirable to enhance the integration density of a chip with CNFET technology.

It can be noted from Figure 13 that the minimum delay is achieved by placing the nanotubes far apart (to increase $I_{PER\ TUBE}$). Note that, for 1 nm of CNT diameter with 2 nm of HfO_2 dielectric thickness, the optimal spacing for high parasitic load is 1.6x the diameter. It is worthwhile to mention that the optimal S depends on the choice of diameter and the dielectric thickness [18]. After seeing results plotted in Figure 14, it can be noted that the PDP decreased slowly after pitch = 6 nm. So, we take the area trade-off into account. Thus we can say the best pitch value is 6 nm.

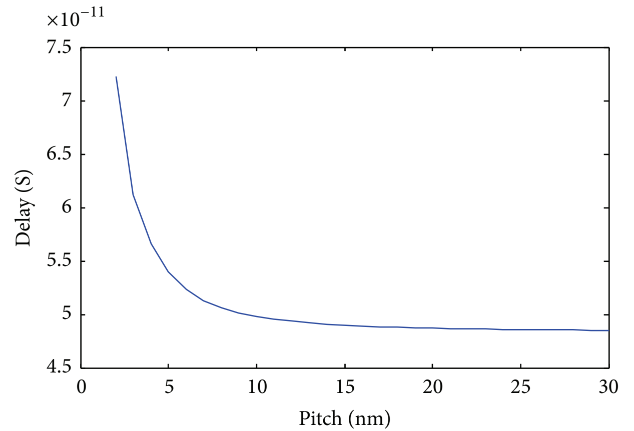


Figure 13: The effect of pitch on delay for pure-CNFET inverter.

3.5. Selection of Dielectric Material. The top-gated CNFETs have been fabricated using 15–20 nm thick SiO_2 as a gate insulator. To improve the device performance further, a thinner gate insulator with a higher dielectric constant can be used. Recently, high dielectric materials such as ZrO_2 and HfO_2 thin films have also been employed as the insulator in top-gated CNFETs [19]. The dielectric materials that are generally considered are listed in Table 2 along with their dielectric constants (K_{ox}).

The saturation current of CNFETs increases with increasing dielectric constant as shown in Figure 15 but the degree of this positive effect decreases as we go for higher dielectric material. This means that as we are going for higher and higher dielectric constant materials the increment in drain current with respect to K_{ox} reduces [20].

Zirconium oxide (ZrO_2) and hafnium oxide (HfO_2) are the forefront of materials science semiconductor electronics [19]. In our optimization, Zro_2 is used as a gate insulator with high K dielectric constant.

The speed advantage of CNFET over MOSFET technology is sensitive to the gate parasitic capacitance [16]. As the oxide thickness increases, the gate-to-channel capacitance deceases as shown in Figure 16 and therefore the device delay reduces. But by increasing the oxide thickness, the driving current decreases; therefore I_{on}/I_{off} ratio is decreased as shown in Figure 17. Thus, there is a trade-off between the current drive per device and speed. To improve the

Table 2: List of oxides considered for gate insulation with their dielectric constants.

Name of the oxide	Chemical formula	Dielectric constant (K_{ox})
Silicon dioxide	SiO_2	4
Hafnium dioxide	HfO_2	16
Zirconium dioxide	ZrO_2	25

Table 3: List of design parameters for nonoptimized and optimized CNFET.

Design parameter	Nonoptimized	Optimized
Supply voltage (V)	0.9	0.6
CNT diameter (nm)	1.5	1.5
Gate dielectric constant: K_{ox}	HfO_2 (16)	ZrO_2 (25)
Oxide thickness (nm)	4	1.5
CNT pitch (nm)	20	6
Number of CNTs	10	8
Work function contact (eV)	4.5	5.1

performance of the device, the oxide thickness of high K dielectric material must be chosen with care.

For inverters designed based on pure-CNFET, the dynamic power consumption and delay are plotted in Figures 18 and 19 for certain range of oxide thickness of ZrO_2. The power delay product is also computed to choose optimum oxide thickness. The less value of PDP is at T_{ox} = 2.5 nm. But there is no great difference between T_{ox} = 2.5 nm and 1.5 nm. So, we can say the optimum oxide thickness is 1.5 nm at K_{ox} = 25.

3.6. Selection of Contact Material. The contact between semiconducting CNT and metal is generally modeled as a Schottky barrier (SB), resulting from the Fermi level mismatch between semiconducting CNT and metal electrode [21, 22]. For a typical p-type CNT transistor, the metal with high work function forms small SB height contact, schematically, where the Fermi level of the metal aligns well with the valence band of the CNT. By eliminating the Schottky barrier between the source contact and source material, the transistor will be capable of delivering more on-current.

Palladium (Pd), which is a noble metal with high work function and good wetting interactions with CNT, has been found with good electrical contact to both semiconducting and metallic CNTs [23].

4. Results and Discussion

After selecting the best design parameters and ensuring by the simulation results that high performance is obtained for the CNFET device, we applied these parameters in basic logic gates (Inverter, NAND, and NOR) for optimized CNFET and compared them with nonoptimized CNFET, Si-MOSFET, and hybrid configuration. We summarize the nonoptimized and proposed optimized parameters of CNFET in Table 3.

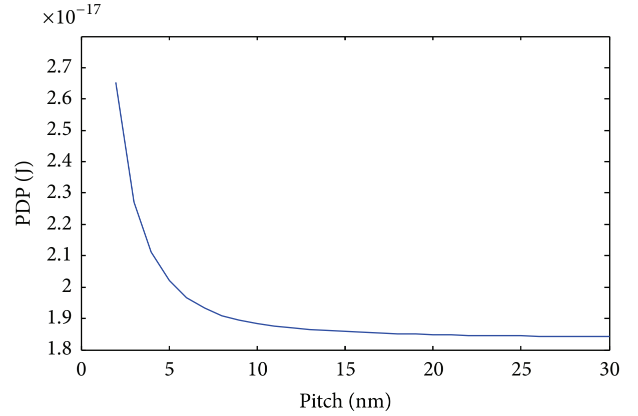


Figure 14: The effect of pitch on PDP for pure-CNFET inverter.

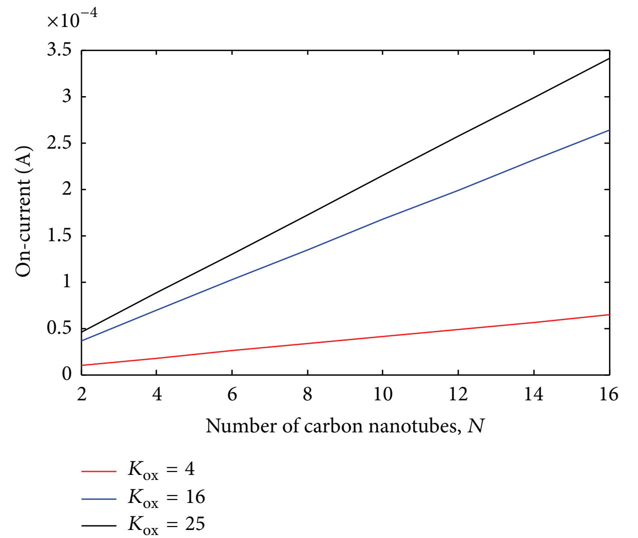


Figure 15: The on-current versus number of carbon nanotubes for different dielectric constants.

From the results shown in Table 4, nonoptimized CNFET has the smallest delay for the inverter and NOR design compared to optimized CNFET, hybrid (NMOS-PCNFET), and Si-MOSFET. But the optimized CNFET saves area by 75% rather than the nonoptimized CNFET.

For the average power consumed, the hybrid configuration is better than nonoptimized CNFET but optimized CNFET shows the best design for all logic gates compared to nonoptimized CNFET, hybrid, and Si-MOSFET according to the results listed in Table 5.

The percentage improvement in power consumption is greater than the percentage improvement in propagation delay. So, this good result reflects the PDP term.

From PDP results as listed in Table 6, hybrid configuration is better than nonoptimized CNFET for PDP term for NAND logic gate. But optimized CNFET is better than the hybrid configuration for all basic logic gates. The power delay product of the optimized CNFET is about 68%, 63%, and 79% times less than that of the nonoptimized CNFET circuits,

TABLE 4: The propagation delay of inverter, 2-input NAND, 2-input NOR gate for Si-MOS, pure-CNFET, and hybrid configuration.

	Delay (xE-11S)			
	Si-MOSFET 32 nm CMOS	Pure-CNFET Nonoptimized	Optimized	Hybrid NMOS-PCNFET
Inverter	14.6	3.80	9.51	5.94
2-input NAND	19.95	11.94	16.09	9.91
2-input NOR	20.50	7.54	9.95	10.17

TABLE 5: The power dissipation of inverter, 2-input NAND, and 2-input NOR gates for Si-MOS, pure-CNFET, and hybrid configuration.

	Power (xE-07W)			
	Si-MOSFET 32 nm CMOS	Pure-CNFET Nonoptimized	Optimized	Hybrid NMOS-PCNFET
Inverter	5.83	13.19	2.61	9.76
2-input NAND	13.98	17.26	3.53	12.35
2-input NOR	10.05	16.14	3.88	14.23

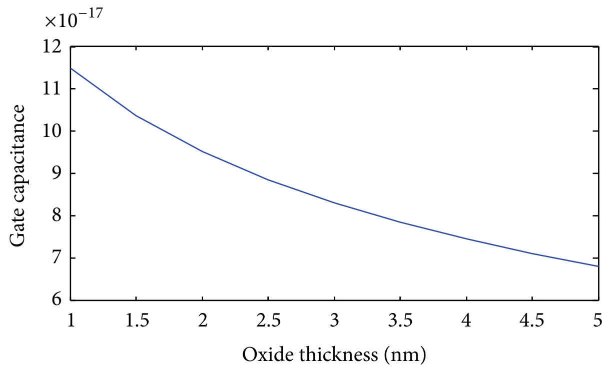


FIGURE 16: The gate parasitic capacitance with oxide thickness.

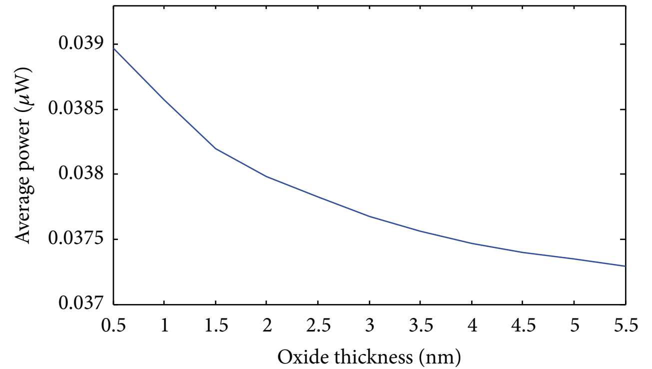


FIGURE 18: The average power for oxide thickness at $K_{ox} = 25$.

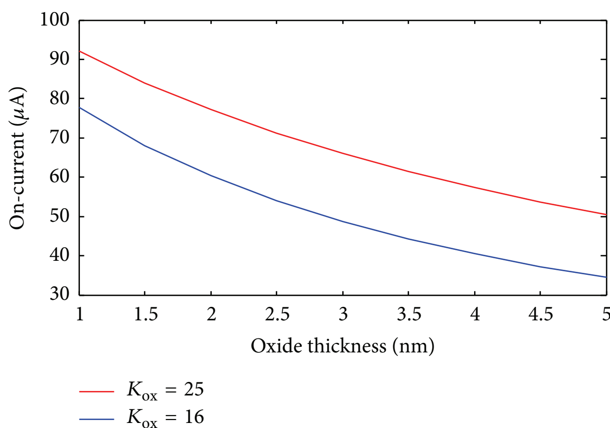


FIGURE 17: The on-current with different oxide thickness.

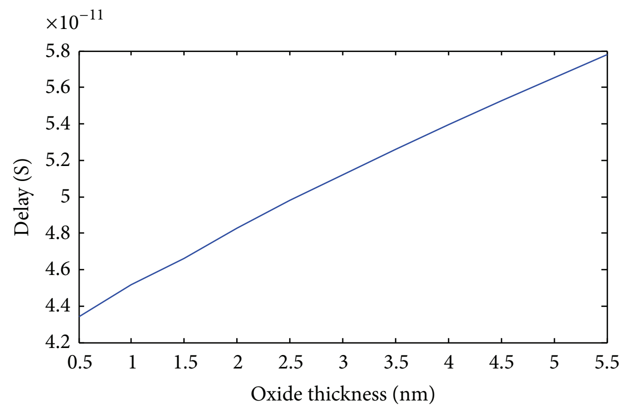


FIGURE 19: The delay for oxide thickness at $K_{ox} = 25$.

hybrid configuration, and Si-MOSFET, respectively. It can be summarized that optimized CNFET has the smallest PDP for all basic logic gates.

5. Conclusion

The influence of device design parameters of 32 nm pure-CNFET on the delay-power product and overall performance has been explored in this paper. First, we investigated the

Table 6: The power delay product of inverter, 2-input NAND, and 2-input NOR gate for Si-MOS, pure-CNFET, and hybrid configuration.

	PDP (xE-17J)			
	Si-MOSFET	Pure-CNFET		Hybrid
	32 nm CMOS	Nonoptimized	Optimized	NMOS-PCNFET
Inverter	8.51	5.01	2.48	5.79
2-input NAND	27.80	20.61	5.68	12.23
2-input NOR	20.60	12.16	3.86	14.47

influence of supply voltage on device performance and chose the optimum supply voltage. Then, we studied the effect of design parameters on speed, power, and area saving. The nanotube diameter, the number of nanotubes per device, and intertube pitch play the most important roles in determining both the area (physical gate width) and performance (I_{on}/I_{off}) of carbon nanotube transistors. Trade-off among area efficiency, Ion, and I_{on}/I_{off} of CNFETs are explored in this paper. Further performance improvement can be achieved by using a smaller diameter with upper range of number of CNTs with smaller pitch. We also reduced the thickness of dielectric with high-K material. Choosing Pd as a contact material is another factor to enhance the overall device performance. Finally, the results show that the design based optimal design parameters of CNFET have the smallest value of PDP compared to nonoptimized, hybrid, and Si-MOSFET designs for all basic logic gates.

Competing Interests

The authors declare that they have no competing interests.

References

[1] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. P. Wong, and F. Boeuf, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *IEEE Circuits and Devices Magazine*, vol. 21, no. 1, pp. 16–26, 2005.

[2] J. M. Rabaey and S. Malik, "Challenges and solutions for late- and post-silicon design," *IEEE Design and Test of Computers*, vol. 25, no. 4, pp. 296–302, 2008.

[3] Y. Sun and V. Kursun, "N-Type carbon-nanotube MOSFET device profile optimization for very large scale integration," *Transactions on Electrical and Electronic Materials*, vol. 12, no. 2, pp. 43–50, 2011.

[4] S. Park, M. Vosguerichian, and Z. Bao, "A review of fabrication and applications of carbon nanotube film-based flexible electronics," *Nanoscale*, vol. 5, no. 5, pp. 1727–1752, 2013.

[5] S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 217–225, 2011.

[6] F. Sharifi, A. Momei, and K. Navi, "CNFET based basic gates and a novel full adder cell," *International Journal of VLSI Design & Communication Systems*, vol. 3, no. 3, 2012.

[7] I. S. Shimaa and H. G. Salah El-Din, "A novel high-speed adder-subtractor design based on CNFET," *International Journal of Applied Information Systems*, vol. 10, no. 7, pp. 29–32, 2016.

[8] P. Dhilleswararao, R. Mahapatra, and P. S. T. N. Srinivas, "High SNM 32nm CNFET based 6T SRAM Cell design considering transistor ratio," in *Proceedings of the 2014 International Conference on Electronics and Communication Systems (ICECS '14)*, pp. 1–6, Coimbatore, India, February 2014.

[9] S. I. Sayed, M. M. Abutaleb, and Z. B. Nossair, "Performance optimization of logic circuits based on hybrid CMOS and CNFET design," *International Journal of Recent Technology and Engineering*, vol. 1, no. 6, pp. 1–4, 2013.

[10] D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close, and H.-S. P. Wong, "Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications," *IEEE Transactions on Nanotechnology*, vol. 7, no. 5, pp. 636–639, 2008.

[11] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—part I: model of the intrinsic channel region," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3186–3194, 2007.

[12] J. Luo, L. Wei, C.-S. Lee et al., "Compact model for carbon nanotube field-effect transistors including nonidealities and calibrated with experimental data down to 9-nm gate length," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1834–1843, 2013.

[13] P. Zhang, Y. Yang, T. Pei et al., "Transient response of carbon nanotube integrated circuits," *Nano Research*, vol. 8, no. 3, pp. 1005–1016, 2015.

[14] F. A. Usmani and M. Hasan, "Carbon nanotube field effect transistors for high performance analog applications: an optimum design approach," *Microelectronics Journal*, vol. 41, no. 7, pp. 395–402, 2010.

[15] L. Ding, S. Liang, T. Pei et al., "Carbon nanotube based ultra-low voltage integrated circuits: scaling down to 0.4 V," *Applied Physics Letters*, vol. 100, no. 26, Article ID 263116, 2012.

[16] J. Deng, N. Patil, K. Ryu et al., "Carbon nanotube transistor circuits: circuit-level performance benchmarking and design options for living with imperfections," in *Proceedings of the 54th IEEE International Solid-State Circuits Conference (ISSCC '07)*, pp. 70–588, San Francisco, Calif, USA, February 2007.

[17] C. Kshirsagar, H. Li, T. E. Kopley, and K. Banerjee, "Accurate intrinsic gate capacitance model for carbon nanotube-array based FETs considering screening effect," *IEEE Electron Device Letters*, vol. 29, no. 12, pp. 1408–1411, 2008.

[18] A. Raychowdhury, A. Keshavarzi, and J. Kurtin, "Optimal spacing of carbon nanotubes in a CNFET array for highest circuit performance," in *Proceedings of the 64th Device Research Conference*, State College, Pa, USA, June 2006.

[19] A. Javey, H. Kim, M. Brink et al., "High-κ dielectrics for advanced carbon-nanotube transistors and logic gates," *Nature Materials*, vol. 1, no. 4, pp. 241–246, 2002.

[20] R. Sahoo and R. R. Mishra, "Carbon nanotube field effect transistor: basic characterization and effect of high dielectric material," *International Journal of Recent Trends in Engineering*, vol. 2, no. 7, pp. 40–42, 2009.

[21] Z. Chen, J. Appenzeller, J. Knoch, Y.-M. Lin, and P. Avouris, "The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors," *Nano Letters*, vol. 5, no. 7, pp. 1497–1502, 2005.

[22] Y. Nosho, Y. Ohno, S. Kishimoto, and T. Mizutani, "Relation between conduction property and work function of contact metal in carbon nanotube field-effect transistors," *Nanotechnology*, vol. 17, no. 14, pp. 3412–3415, 2006.

[23] Y. Chai, A. Hazeghi, K. Takei et al., "Low-resistance electrical contact to carbon nanotubes with graphitic interfacial layer," *IEEE Transactions on Electron Devices*, vol. 59, no. 1, pp. 12–19, 2012.

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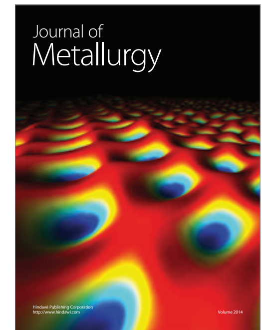
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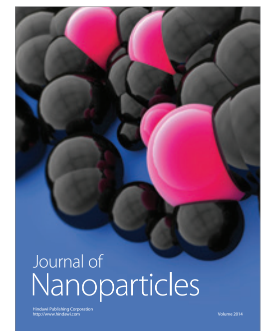
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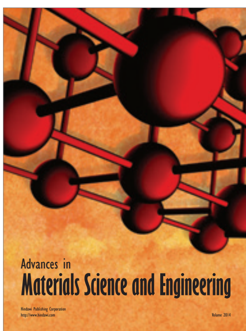
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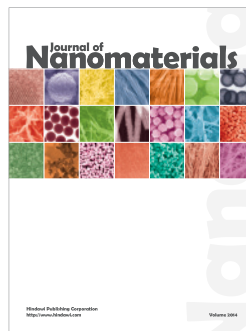
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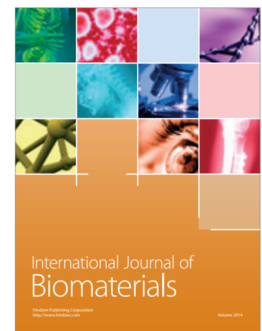
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