Hindawi
Journal of Sensors
Volume 2017, Article ID 7861025, 14 pages
https://doi.org/10.1155/2017/7861025

Research Article

Digital Closed-Loop Driving Technique Using the PFD-Based CORDIC Algorithm for a Biaxial Resonant Microaccelerometer

Bo Yang,[1,2] Lei Wu,[1,2] Binlong Wang,[1,2] and Qiuhua Wang[1,2]

[1]*School of Instrument Science and Engineering, Southeast University, Nanjing 210096, China*
[2]*Key Laboratory of Micro-Inertial Instrument and Advanced Navigation Technology, Ministry of Education, Nanjing 210096, China*

Correspondence should be addressed to Bo Yang; yangbo20022002@163.com

Received 19 June 2017; Revised 18 September 2017; Accepted 27 September 2017; Published 26 October 2017

Academic Editor: Francesco Dell'Olio

A digital closed-loop driving technique is presented in this paper that uses the PFD- (phase frequency detector-) based CORDIC (coordinate rotation digital computer) algorithm for a biaxial resonant microaccelerometer. A conventional digital closed-loop self-oscillation system based on the CORDIC algorithm is implemented and simulated using Simulink software to verify the system performance. The system performance simulations reveal that the incompatibility between the sampling frequency and effective bits of AD and DA convertors limits further performance improvements. Therefore, digital, closed-loop self-oscillation using the PFD-based CORDIC algorithm is designed to further optimize the system performance. The system experimental results illustrate that the optimized system using the PFD-based CORDIC improves the bias stability of the resonant microaccelerometer by more than 5.320 times compared to the conventional system. This demonstrates that the optimized digital closed-loop driving technique using the PFD-based CORDIC for the biaxial resonant microaccelerometer is effective.

1. Introduction

Increasing attention has been given to silicon resonant microaccelerometers due to their high sensitivity, large dynamic range, and frequency signal output. A successful excitation of resonant microaccelerometers is crucial to achieve high performance. Many methods to control these accelerometers have been published [1–5]. A nonlinear operator-theoretical approach based on the describing function technique was used to design the feedback parameters and characterize the analog loop performance [1, 2]. Previous studies [3, 4, 6, 7] proposed an analog control circuit based on automatic amplitude control (AGC) technology. Recently, a phase lock loop (PLL) combined with AGC was utilized to lock the natural frequency of the resonator and maintain a stable resonant amplitude [5, 8, 9]. However, most of the previous control technologies for microaccelerometers that adopted the analog circuitry were characterized by a large temperature drift, a complex adjustment in circuit parameters, difficulties in compensation, and other disadvantages. The silicon resonant microaccelerometer originally based on the frequency output may have more advantages than the digital control scheme. An all-digital MEMS tuning fork self-excited vibration control by phase-relation using time-A/D converter- (TAD-) based all-digital PLL (ADPLL), which uses no conventional analog method such as automatic gain control (AGC) or automatic level control (ALC), has been presented [10]. Preliminary experimental results confirmed its self-excited vibration, resulting in its resonance jitter level of 52.60 ns (standard deviation) at a 37.00 μs self-resonance period. In the digital closed-loop driving circuit of the resonant microaccelerometer, the numerically controlled oscillator (NCO) is usually applied to generate the sine and cosine signals for demodulation and drive. The ordinary look-up table (LUT) method based on read-only memory (ROM) is generally used to implement the NCO. The output signal of the LUT method was affected by the truncation error due to the limited data depth [11]. Unlike the normal applications of NCO with fixed or small changed frequency, such as fixed frequency source or the closed-loop control applications in the microgyroscope [12], the NCO in the driving applications of the resonant microaccelerometer

requires a large frequency lock range to track the natural frequency shift due to the acceleration input. The higher the mechanical sensitivity of the resonant microaccelerometer, the greater the frequency lock range of the NCO, which results in a greater consumption of memory if the LUT method is adopted. Therefore, the LUT method is not suitable for the driving application of resonant microaccelerometers since it will consume excessive memory resources to achieve high-precision control [13, 14]. The interpolation algorithm is another way to implement the NCO, which stores an amount of base point data and interpolates the other points of the trigonometric function to improve the accuracy [15]. Compared with the LTU, the interpolation algorithm greatly reduces the consumption of memory units but increased the consumption of logic units for the calculation demand. Simultaneously, the accuracy of the method is affected by the number of base points and the chosen interpolation method. The coordinate rotation digital computer (CORDIC) algorithm based on the iterative algorithm is mainly used to calculate trigonometric and hyperbolic functions [16]. The accuracy of the CORDIC depends on its iteration depth. Compared to the LTU method and interpolation algorithm, the CORDIC algorithm could achieve high precision without significant memory resources as the pipelining algorithm is adopted.

In this paper, we propose an optimized, digital, closed-loop self-oscillation technique using PFD-based CORDIC for a biaxial resonant microaccelerometer. The NCO, PFD, AGC, and PLL are realized in a single FPGA. In Section 2, a brief description of the structural principle of resonant microaccelerometers is given. In Sections 3 and 4, a conventional, digital, closed-loop self-oscillation system and an optimized self-oscillation system using the PFD-based CORDIC are presented. Then, the experimental results are illustrated in Section 5. Concluding remarks are finally given in the last section.

2. Structure Principle of the Biaxial Resonant Microaccelerometer

Figure 1 illustrates the structure of a biaxial resonant microaccelerometer [9]. Four identical sensing structures and a proof mass constitute the biaxial resonant microaccelerometer. Each sensing structure consists of a pair of lever mechanisms, a pair of decoupling beams, and a tuning fork resonator. Four tuning fork resonators are driven by control circuits to vibrate at their natural resonant frequencies. When the x-axis acceleration is input, the inertial force promotes the proof mass to move along the x-axis direction. Owing to the rigid stiffness of the x-axis decoupling beam, two x-axis lever mechanisms are spurred to move along x-axis along with the proof mass. The inertial forces are amplified and applied to two x-axis tuning fork resonators by lever mechanisms. Correspondingly, the resonant frequencies of the two tuning fork resonators deviate from their original natural resonant frequencies due to the input of acceleration. However, two lever mechanisms along the y-axis will remain stationary owing to soft stiffness of the y-axis decoupling beam.

Table 1: The structure parameters of the microaccelerometer.

Parameter	Value	Parameter	Value
h (μm)	70	L_x (μm)	1050
w (μm)	8	L_y (μm)	1130
m (μg)	37.56	f_x (Hz)	27000
$A_{x/y}$	25.6	f_y (Hz)	24000

The frequency change caused by two differential resonators in the input of acceleration is [9]

$$\Delta f_{x/y} \approx B_{x/y} m A_{x/y} D_{x/y} a_{x/y},$$
$$B_{x/y} = \frac{{L_{x/y}}^2 f_{x/y}}{Ehw^3}, \tag{1}$$

where $\Delta f_{x/y}$ are output frequency changes along the X/Y-axes, $a_{x/y}$ are the input acceleration along the X/Y-axes, m is the proof mass, $A_{x/y}$ are the amplification factors of the lever mechanism along the X/Y-axes, $B_{x/y}$ are the frequency conversion coefficients of the resonators in the X/Y-axes, $D_{x/y}$ represent decoupling coefficients along the X/Y-axes, $f_{x/y}$ are the natural frequencies of the resonator along the X/Y-axes, w is the width of the resonant beams, $L_{x/y}$ are the lengths of the resonant beams in the X/Y-axes, h is the thickness of resonant beams, and E is elastic modulus of silicon. The structure parameters are shown in Table 1.

A standard three-mask deep dry silicon on glass (DDSOG) process is used to fabricate the biaxial decoupled resonant microaccelerometer. The process flow consists of (1) laying photoresist on the silicon wafer and photoetching, (2) deep reactive ion etching (DRIE) aspect ratio to form the bonding area, (3) sputtering of a Cr/Ti/Au layer on 7740 Pyrex glass to fabricate the electrode wire, (4) Si/glass electrostatic bonding, (5) reducing the silicon wafer thickness by KOH wet etching and polishing, and (6) DRIE with 20 : 1 aspect ratio etching to release the structure. The structure of the biaxial resonant microaccelerometer has an overall size of 7500 μm (length) × 7500 μm (width) × 70.00 μm (thickness). To suppress the mutual interference between the x-axis and y-axis, two pairs of tuning fork resonators have a 3 kHz frequency difference. The vacuum encapsulation in the biaxial resonant microaccelerometer is implemented by parallel seam welding. Test results show that the relevant quality factors of the four resonators are 621.0, 648.0, 678.0, and 689.0, respectively.

3. Conventional Digital Closed-Loop Self-Oscillation System

3.1. Basic Scheme. The conventional digital closed-loop self-oscillation system based on the CORDIC algorithm for the tuning fork resonator is shown in Figure 2. The digital closed-loop self-oscillation system used to drive the tuning fork resonator and track the resonant frequency is implemented in the FPGA device. The FPGA chip is EP3C25E144I7 from the Altera corporation and has 2.462×10^4 programmable logic units, 6.083×10^5 RAM bits, 66 multipliers, and 4 PLL.

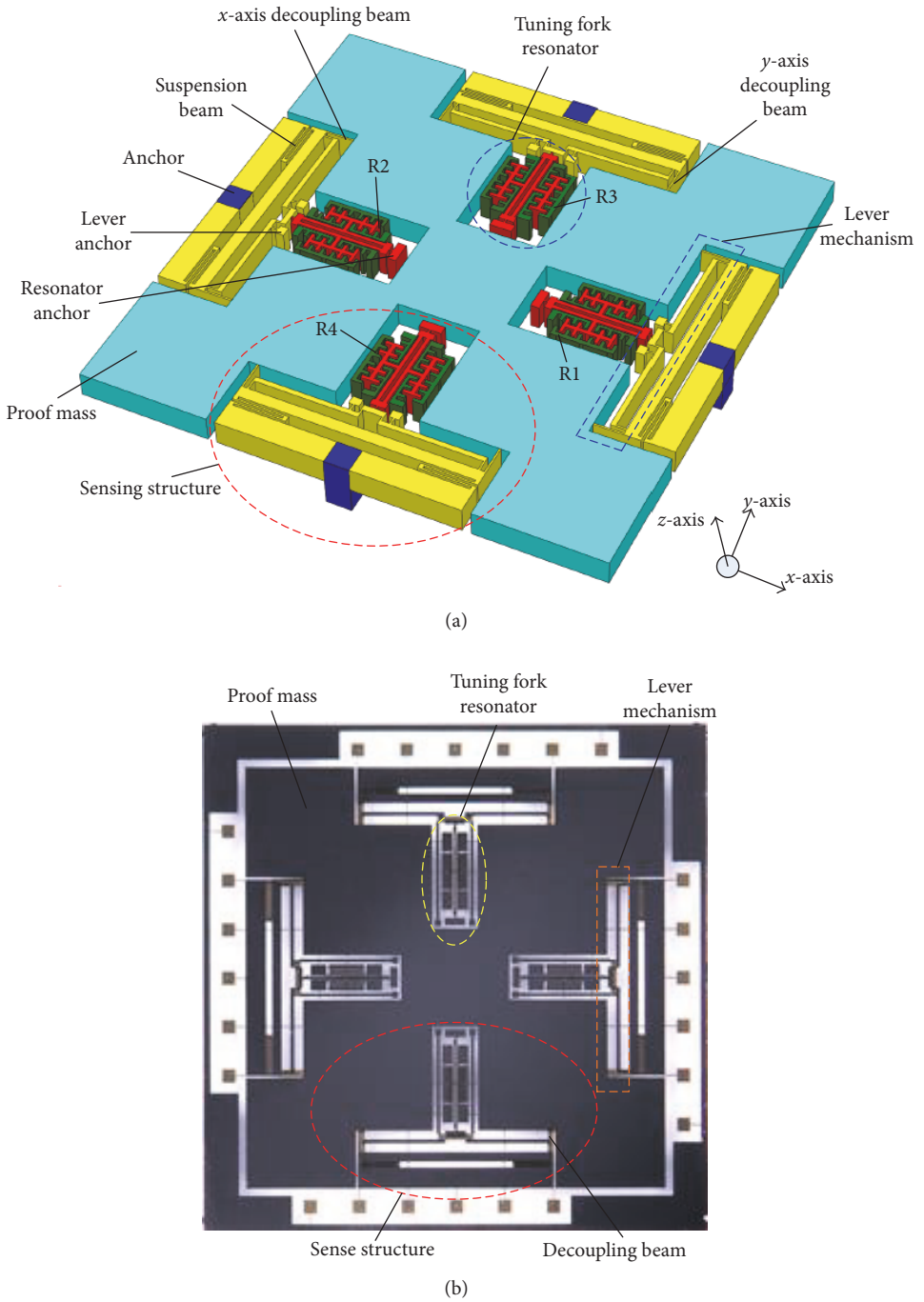


Figure 1: The biaxial resonant microaccelerometer: (a) the structure scheme; (b) a picture of the fabricated chip.

The entire hardware platform of the FPGA is based on fixed-point arithmetic processing with a main clock frequency of 12.29 MHz.

The NCO shown in Figure 3 is the key part of the digital PLL. The LUT and CORDIC algorithms are two main methods to implement the NCO. One cycle signal is divided into 2^N pieces and stored in different memory units in the LUT. The quantity of memory resources has an exponent relation with the data depth of the LUT. The LUT method will consume excessive memory resources to achieve high accuracy; otherwise, the output signal of the LUT will be affected by truncation errors due to the limited data depth. The CORDIC algorithm is a kind of iterative algorithm mainly used to calculate trigonometric and hyperbolic functions. The accuracy of the CORDIC depends on its iteration depth. Compared to the LUT method, the CORDIC algorithm could achieve high precision without significant memory resources since the pipelining algorithm is adopted.

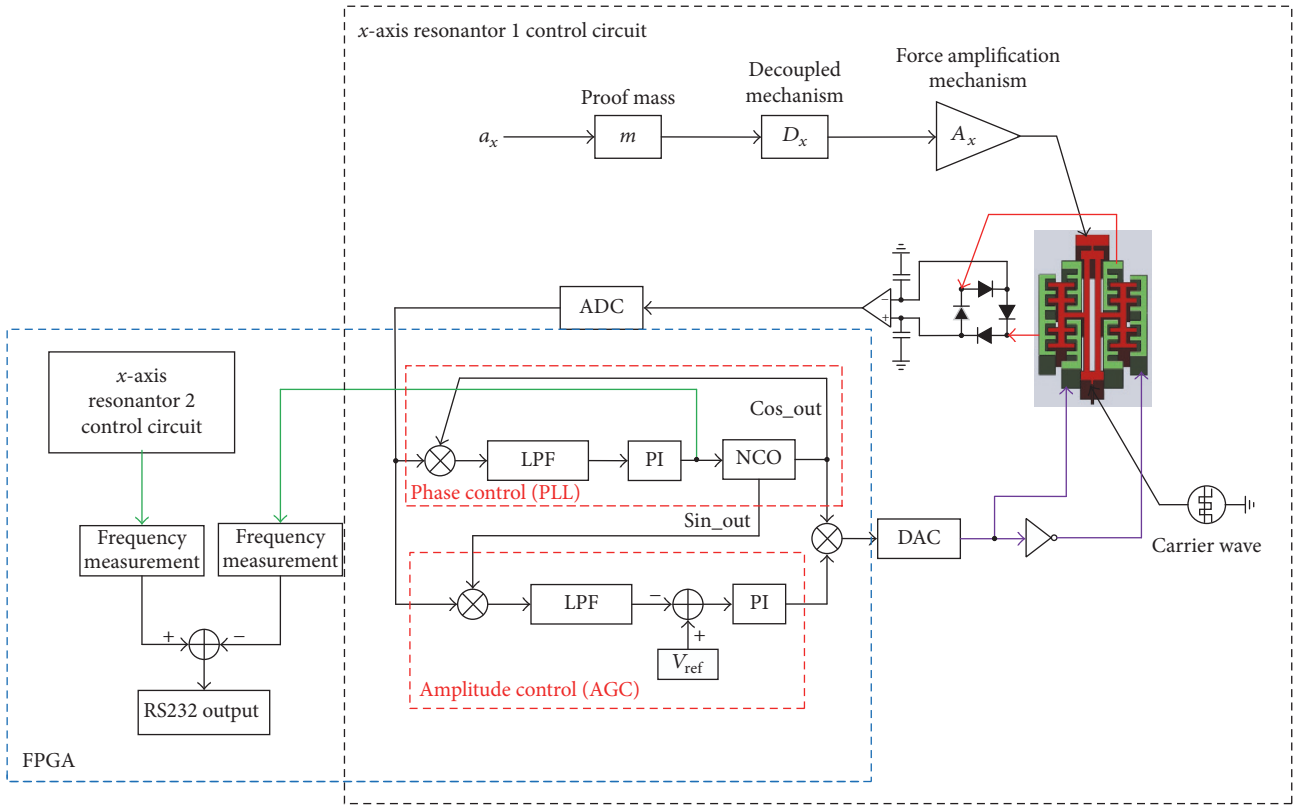


Figure 2: The scheme of digital closed-loop self-oscillation system for the tuning fork resonator.

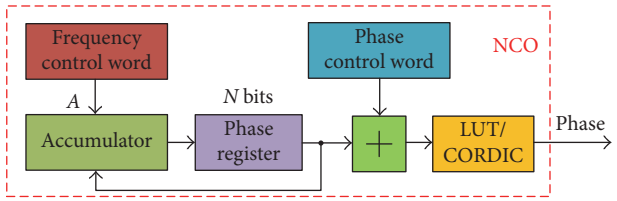


Figure 3: The block diagram of the NCO.

The AGC loop shown in Figure 2 is utilized to control the amplitude of the drive signal to a constant value. The PLL loop is designed to lock to the natural frequency of the resonator. The NCO is controlled by the output of the proportion-integral (PI) controller. As a result of the CORDIC algorithm, the implementation of the NCO does not require a multiplier resource but requires 3184 logic elements and 2347 registers. The low pass filter (LPF) based on the infinite impulse response (IIR) topology adopts 279 logic elements, 228 registers, and 7 embedded multipliers. The digital PI controller is implemented with 203 logic elements, 127 registers, and 7 embedded multipliers. The sine signal of the NCO is utilized to demodulate and determine the amplitude difference in the AGC loop, while the cosine signal of the NCO is used to demodulate and acquire the phase error in the PLL loop. The torquer exerts the drive signal on the drive electrodes to stimulate the tuning fork resonator in the harmonic frequency. The displacement of the resonator is converted and amplified by the interface circuit. Then, the output signal of the interface circuit is transferred to acquire the phase and amplitude control information with the PLL and AGC loop, respectively. Finally, the drive signal is fed into the tuning fork resonator and the self-oscillation is implemented. There are four identical control loops in the entire circuit to drive four resonators simultaneously, and the parameters of each loop are determined by the characteristics of each individual resonator. Due to the restriction on commercially available devices, the DA and AD only have the effective bits of 16 and 18, respectively, with a sampling frequency of 750.0 kHz. To approach the extreme accuracy of the simulation system, the entire hardware realization improves the signal processing accuracy by magnification or extending the digital width. Although the abovementioned processing method can well maintain the system accuracy, the whole system still shows some truncation error.

3.2. System Performance Simulation. The simulation model of the closed-loop self-oscillation system is constructed to analyze the system performance. The simulation models and parameters are similar to Figure 8 and Table 2, respectively. Figure 4 indicates the simulation results of the frequency control precision with different effective bits of AD and DA convertors in the sampling frequency of 750.0 kHz. The increase in the effective bits in the AD and DA convertors can significantly improve the control precision of the frequency. However, there is a significant inflection point where the effective bits of the AD and DA convertors are approximately

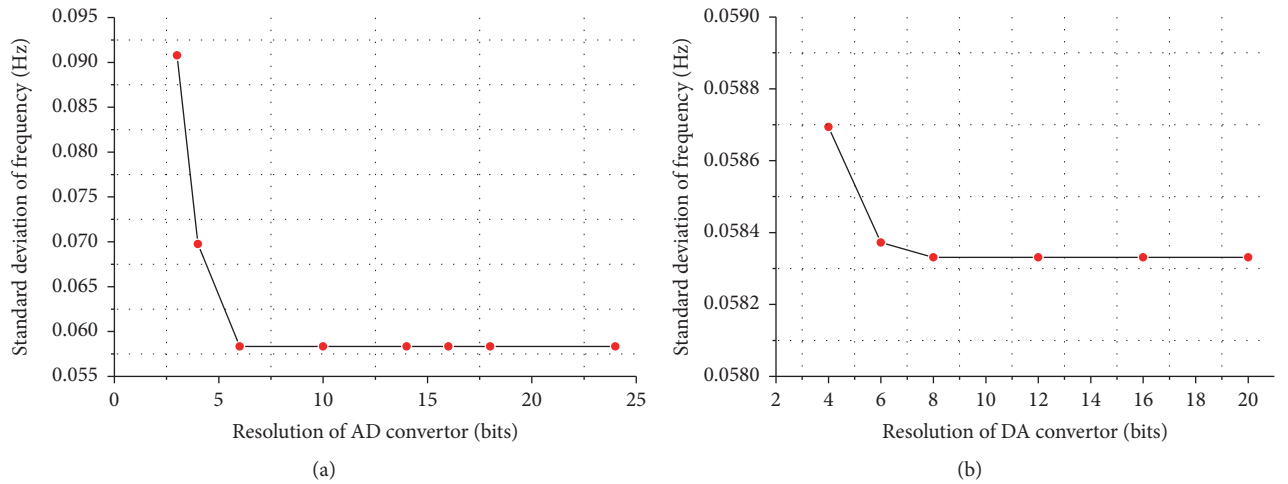


Figure 4: The control precision of the frequency with different effective bits of AD and DA convertors: (a) the resolution change of the AD converter with the effective bits of 16 in the DA convertor; (b) the resolution change of the DA converter with the effective bits of 18 in the AD convertor.

Table 2: The simulation parameters.

Parameter	Value	Parameter	Value
m (kg)	3.750×10^{-8}	K_p of PI_phase	0.1500
c (N·s/m)	9.830×8^{-8}	K_i of PI_phase	0.2000
k (N/m)	926.8	K_p of PI_amp	10.00
K	3.890×10^{6}	K_i of PI_amp	60.00
Fc of IIR1 or IIR2 (Hz)	60.00	$f(u)$ (Torquer)	$-5 * (u-1)^2/10$
Static frequency (NCO) (Hz)	2.510×10^{5}	Frequency sensitivity (NCO) (Hz/V)	1000

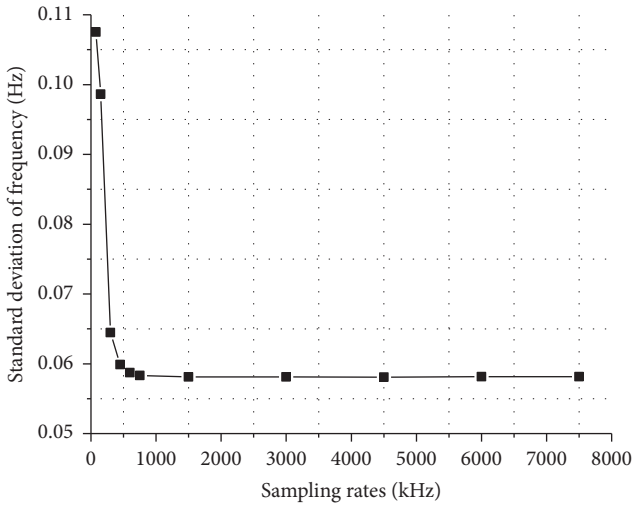


Figure 5: The control precision of the frequency for different sampling frequencies.

6 in Figures 4(a) and 4(b), which illustrates that the further increase of the effective bits of AD and DA convertors does not continuously improve the frequency control precision at a specific sampling frequency. Figure 5 shows the simulation results of the frequency control precision with different sample rates where the AD and DA convertors have the effective bits of 18 and 16, respectively. The higher sample rate results in a better frequency control precision. The main reason for this is that the higher sampling rate implements better signal integrity and demodulation accuracy, which increases the precision of the control system. However, the sampling rate is generally limited by the device hardware, such as the alternative AD and DA convertors. In the selectable commercial devices, the sampling rate can only reach 750.0 kHz in a high-precision 18-bit AD.

4. Optimized Digital Closed-Loop Self-Oscillation Using PFD-Based CORDIC

4.1. Basic Scheme. According to the simulation analysis, the conventional system performance shown in Figure 2 is affected by the sampling rate and effective bits of the AD and DA. However, the sampling frequency and effective bits of the control system are incompatible at the same time. In the actual hardware system, the AD and DA convertors with numerous effective bits are impossible to implement at the high sampling frequency simultaneously, which increases the difficulty in improving the system performance. A new digital closed-loop self-oscillation system using the PFD-based CORDIC shown in Figure 6 is proposed to further optimize the system performance. Unlike the foregoing scheme, the output signal of the interface circuit is divided

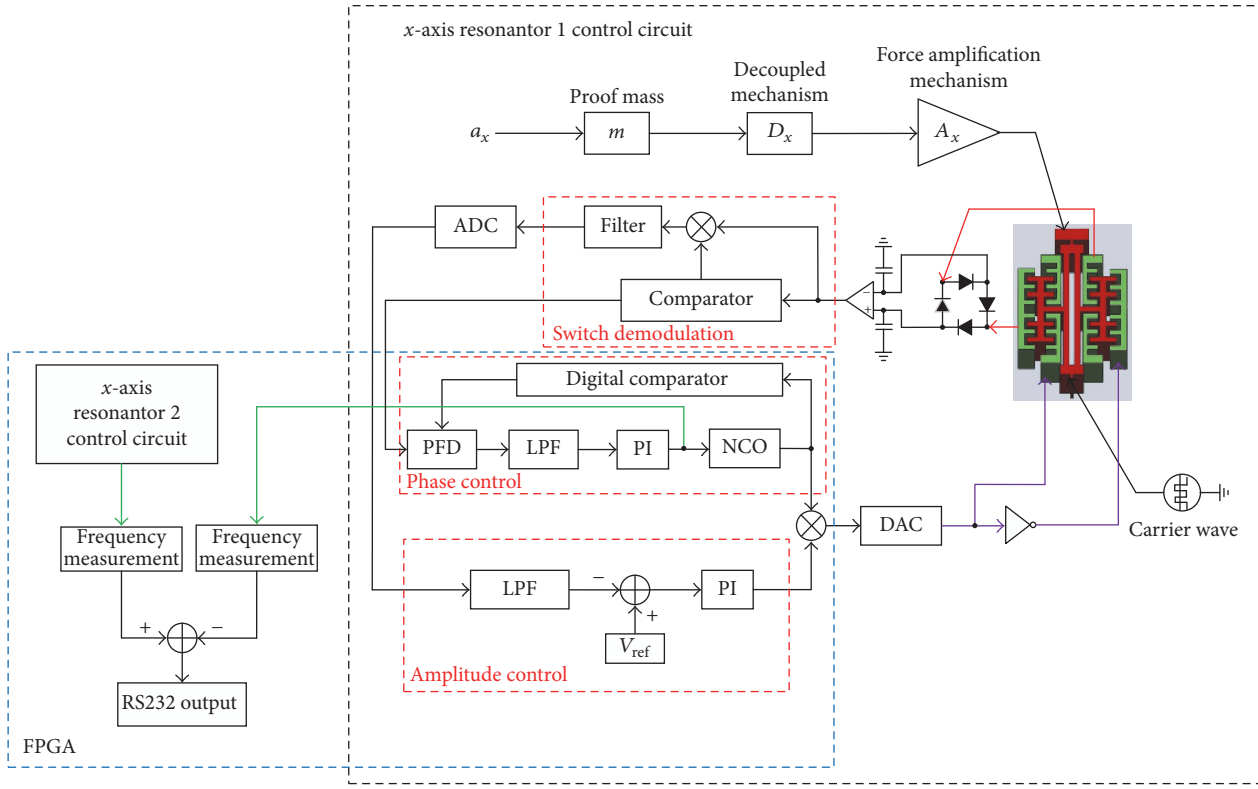


Figure 6: Optimized, digital, closed-loop self-oscillation system using the PFD-based CORDIC.

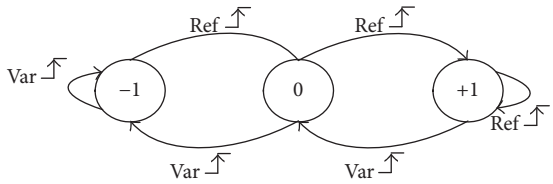


Figure 7: The state flow of the PFD.

into the amplitude signal and the phase signal before the AD sampling. The amplitude information is processed by the switch demodulation and filtering. Then, the output signal is quantized and sampled by the AD convertor. Since the bandwidth of the demodulated amplitude information is small, the digital signal with a high precision can be acquired by the accurate AD convertor with multiquantization bits and a low sampling frequency. The output phase signal after the comparator is extracted by the PFD. The PFD is implemented directly through the high-speed digital way and can acquire a high-precision phase signal, which avoids using the high-speed, multiquantization bits AD convertor. In the actual circuit, the sampling frequency of the PFD can be increased to the main clock frequency of 12.29 MHz. The DA and AD convertors of the optimized, closed-loop self-oscillation system have the same parameter settings as that of the conventional closed-loop self-oscillation system shown in Figure 2. Briefly, due to the incompatibility issues between the high sampling rate and numerous effective bits in the conventional control system shown in Figure 2, the proposed control circuit separately quantifies the amplitude information and the phase information. The amplitude information with approximate DC characteristics improves the quantization precision by increasing the number of effective bits and does not need a high sampling rate to achieve high-precision quantization. The phase information is sampled directly through the high-speed PFD to obtain a high-precision digital phase signal. The accuracy of the digital phase signal is only related to the sampling rate of the PDF and has no direct relationship with the effective bits due to the abandonment of the AD converter. Therefore, the separate quantification between the amplitude and phase significantly reduces the implementation difficulty of the hardware system, while improving the signal sampling accuracy.

Figure 7 shows the working state flow of the PFD adapted in the optimized, digital, closed-loop self-oscillation system. "Ref" in the figure refers to the input signal of the PFD from the output of the comparator and "Var" represents another input signal derived from the feedback signal of the NCO. State 0, state +1, and state −1 represent the fact that the phase difference between the Ref and Var is zero, positive, or negative, respectively. Suppose the initial state of the PFD is state 0; the state will change from state 0 to state +1 when the rising edge of Ref occurs before that of Var. Otherwise, the state will change from state 0 to state −1 when the rising edge of Var occurs before Ref. When the current state is state +1, the state will return to state 0 if the rising edge of Var is detected. However, the state will remain unchanged if the rising edge

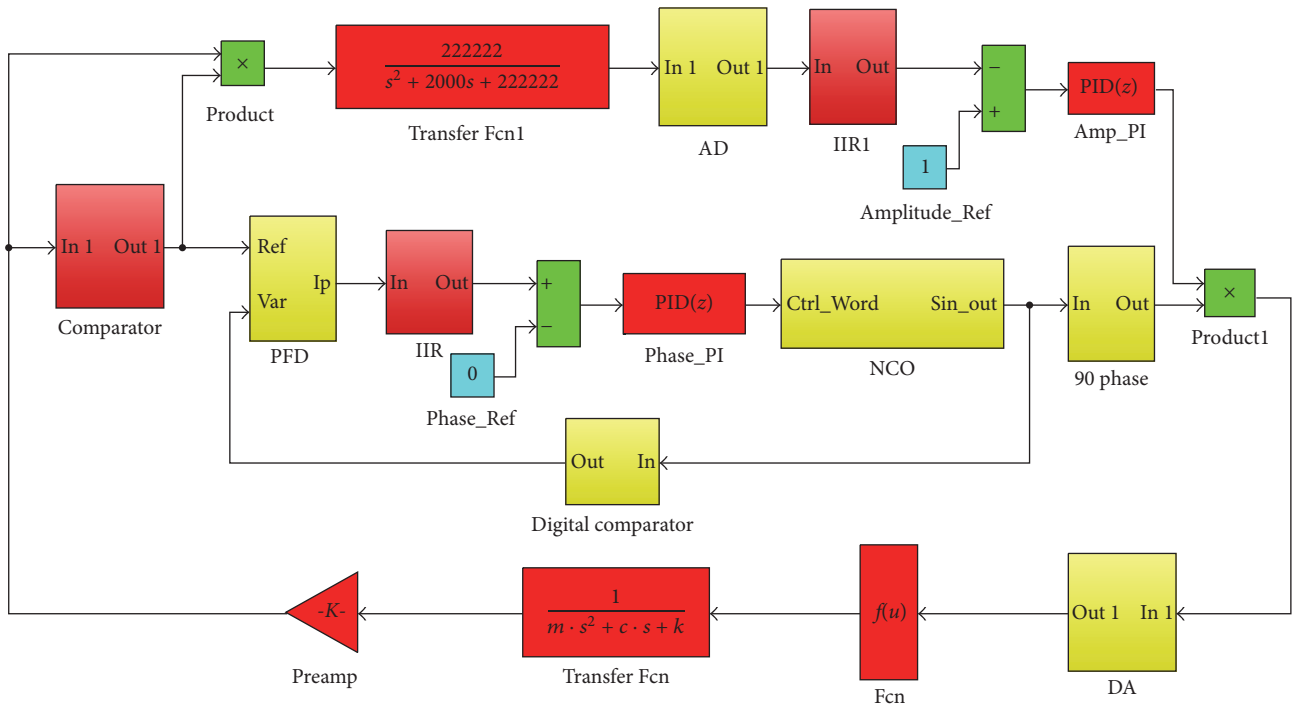


FIGURE 8: The simulation model of the optimized, digital, closed-loop self-oscillation based on PFD.

of Ref is detected. When the current state is state −1, the state will return to state 0 if the rising edge Ref is detected. Nevertheless, the state will maintain the current state if the rising edge of Var is detected.

Suppose Ref^n and Ref^{n+1} represent the current state and the next moment state of the signal Ref, and Var^n and Var^{n+1} represent the current state and next moment state of the signal Var. Therefore, $\overline{\text{Ref}^n}\text{Ref}^{n+1} = 1$ represents the rising edge of the signal Ref, and $\overline{\text{Var}^n}\text{Var}^{n+1} = 1$ represents the rising edge of the signal Var. The $\overline{\text{Ref}^{n+1}\text{Var}^{n+1}} = 0$ represents setting the state to zero when both Ref and Var are 1, which is restored to the initial state. The PFD_{out} represents the output of the PFD module. The relationship between state^{n+1} and state^n and Ref and Var can be expressed as

$$\begin{aligned}
\text{state}^{n+1} &= \text{state}^n \\
&\quad + \overline{\text{Ref}^{n+1}\text{Var}^{n+1}}\left(\overline{\text{Ref}^n}\text{Ref}^{n+1} - \overline{\text{Var}^n}\text{Var}^{n+1}\right) \\
&\qquad\qquad \text{state}^n = 0, \\
\text{state}^{n+1} &= \text{state}^n - \overline{\text{Var}^n}\text{Var}^{n+1} \quad \text{state}^n = 1, \\
\text{state}^{n+1} &= \text{state}^n + \overline{\text{Ref}^n}\text{Ref}^{n+1} \quad \text{state}^n = -1, \\
\text{PFD}_{\text{out}} &= \text{state}^{n+1}.
\end{aligned} \tag{2}$$

4.2. System Performance Simulation. The optimized, closed-loop control system using the PFD-based CORDIC and the conventional closed-loop control system are simulated to contrast the difference in their system performances. Figure 8 illustrates the simulation model of the optimized digital closed-loop self-oscillation system for the tuning fork resonator. The simulation model of the original closed-loop self-oscillation system can be constructed similarly. The PFD is implemented by flowchart integrated in Simulink. Since there is not a built-in CORDIC block in MATLAB's Simulink, the CORDIC algorithm is implemented by calling the S-function in the MATLAB platform. The S-function is a user-defined Simulink block implemented directly by programming according to the CORDIC algorithm. The output of the NCO alternates periodically the phase signal and the output precision of each phase relies on the iterative depth. The resonant frequency of the tuning fork resonator is set to 25.00 kHz. The effective bits of the DA and AD are set to 16 and 18, respectively, with the sampling frequency of 750.0 kHz.

According to the simulation parameters in Table 2, two control systems are simulated to compare the control performance. Figure 9 illustrates the waveforms of the interface circuit sensitive signal in the simulation model. Similar to the conventional system, the amplitude of the drive sensitive signal in the optimized system can quickly reach the reference value. Figure 10 compares the frequency control waveform between the optimized system and the conventional system. Due to the limit of the system memory, the simulation time is set to 5 seconds. The simulation results shown in Figures 10(a) and 10(b) indicate that the two systems implement an essentially stable tracking of the frequency in 40.00 ms. Compared to the optimized system, the conventional system has a small overshoot. The final control accuracy of the frequency between the optimized system and the conventional system is compared in Figures 10(c) and 10(d). The frequency control

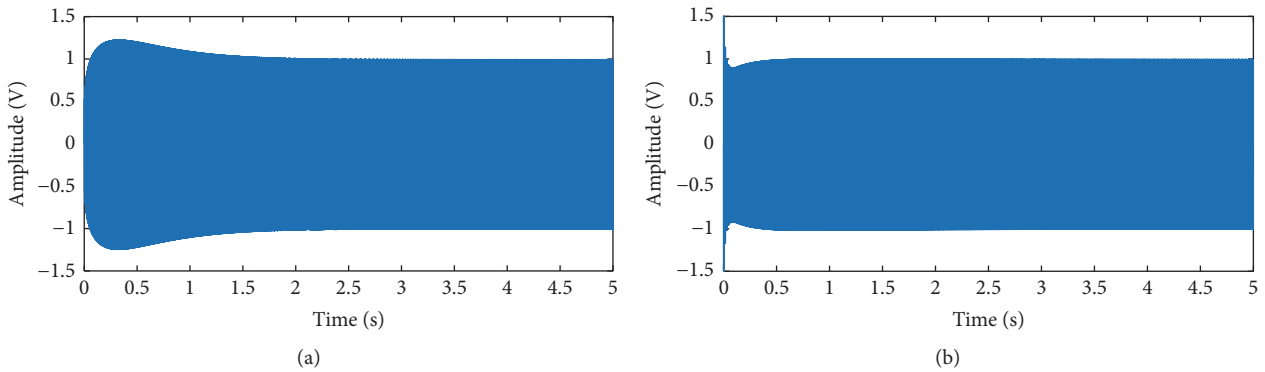


Figure 9: The sensitive signal of the interface circuit waveform: (a) the conventional system; (b) the optimized system.

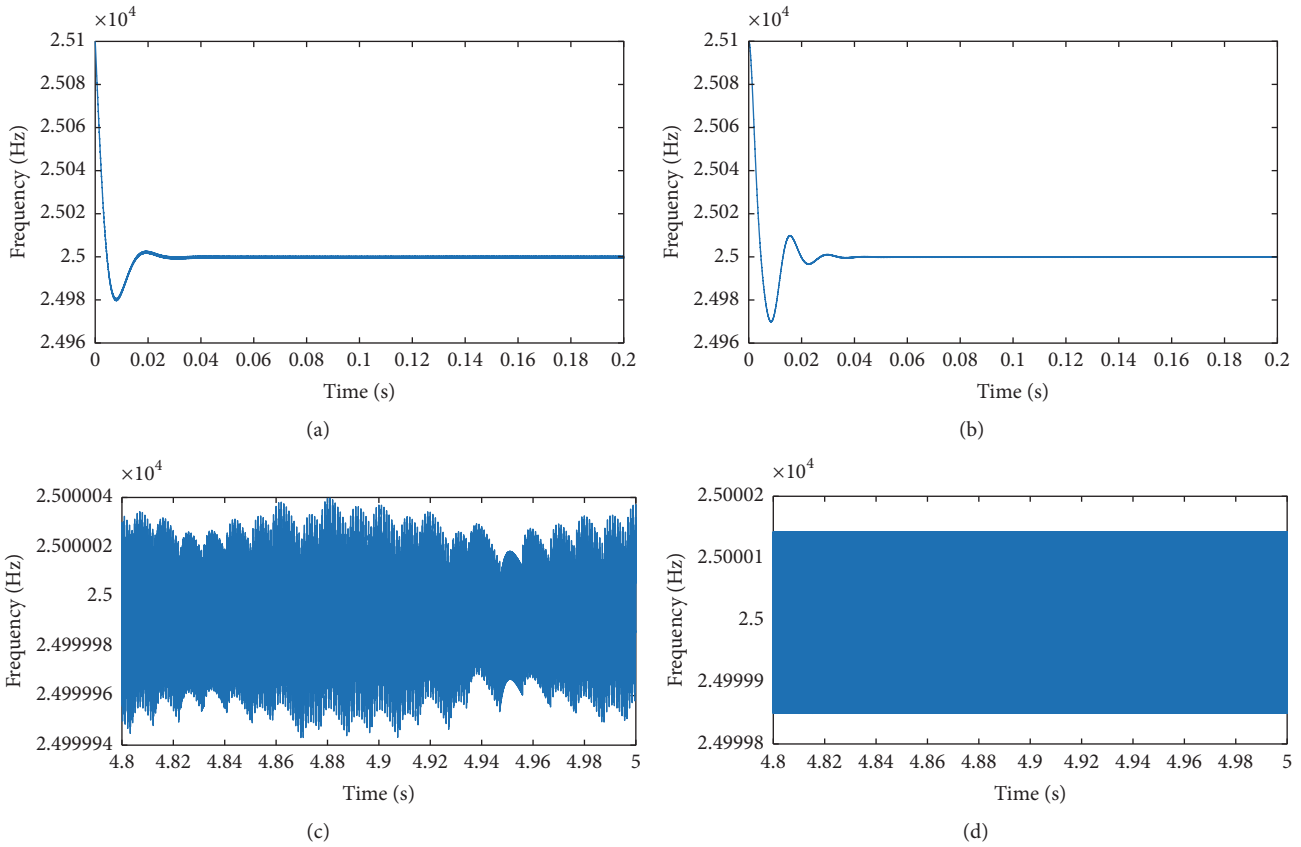


Figure 10: Comparison of the frequency control waveform between the optimized system and the conventional system: (a) the frequency control waveform of the optimized system in the first 200.0 ms, (b) the frequency control waveform of the conventional system in the first 200.0 ms, (c) the partial magnified frequency control waveform of the optimized system in the last 200.0 ms, and (d) the partial magnified frequency control waveform of conventional system in the last 200.0 ms.

accuracy of the improved system is significantly better than that of the conventional system.

Simultaneously, the control system at different sampling frequencies is simulated to verify the influence of the sampling frequency on the system performance. To make the simulation conditions consistent with the optional commercial devices, the sampling frequencies in the conventional system, including the AD/DA and the digital signal processing system in the FPGA, are changed at the same time. However, the optimized system only changes the sampling frequencies of the digital signal processing system in the FPGA and maintains the same sampling frequency of 750.0 kHz in the AD and DA convertors, which mainly reflects the system performance improvement by increasing the sampling frequency of the PFD. The frequency control precision of the optimized system for different sampling rates is shown in Figure 11. Apparently, the increase in the sampling frequency in both the conventional system, shown in Figure 5, and

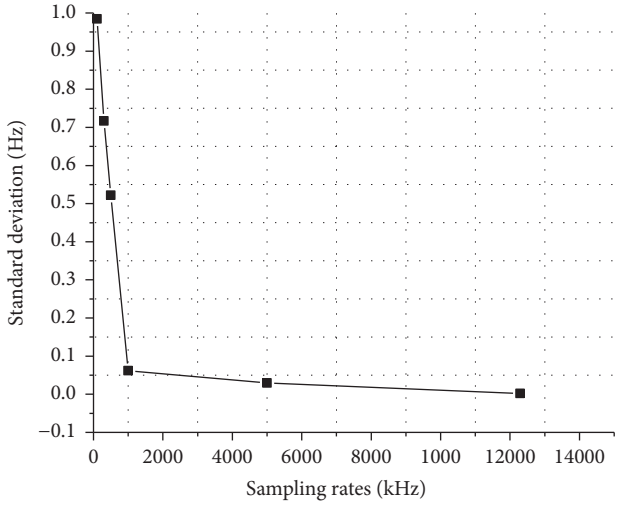
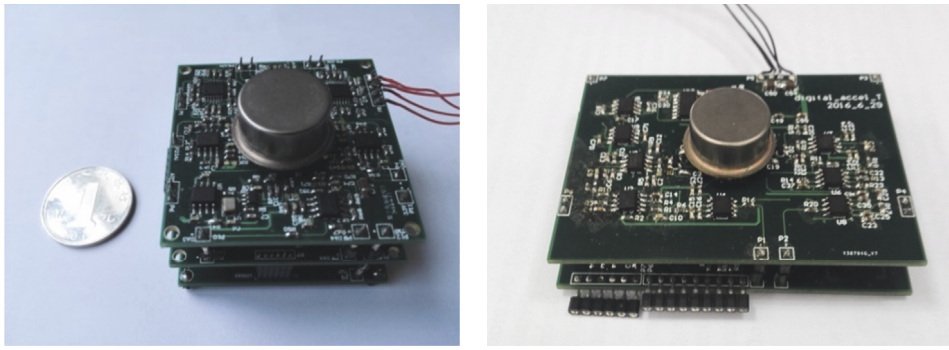


Figure 11: The frequency control precision of the optimized system with different sampling rates.



(a) (b)

Figure 12: Picture of test prototype with the digital closed-loop driving circuits: (a) the prototype with a conventional control system; (b) the prototype with the optimized control system.

the optimized system, shown in Figure 11, can significantly improve the frequency control accuracy. However, the actual sampling rate of the conventional system is significantly lower than that of the optimized system due to the restrictions of the hardware device, which is the main advantage of the optimized system. By comparing Figure 5 with Figure 11, we demonstrate that the frequency standard deviation of the conventional system with a sampling frequency of 750.0 kHz is 58.33 mHz, while the frequency standard deviation of the optimized system with sampling frequency of 12.29 MHz is 2.000 mHz, which increases theoretically by 29.20 times compared to the conventional system. In summary, the simulation results confirm that the optimized system can significantly improve the system performance.

5. Experiment

5.1. Structural Characteristics of Resonant Microaccelerometer. The experiments are implemented by interfacing the biaxial resonant microaccelerometer with the test circuits shown in Figure 12. The experiments of the amplitude-frequency characteristics are carried out under open-loop conditions by an Agilent 35670A dynamic signal analyzer. An excitation source from the dynamic signal analyzer generates a sweep signal to excite the resonators. Then, the output sensitive signals of the interface circuit are simultaneously analyzed with the dynamic signal analyzer.

Figure 13 illustrates the open-loop amplitude-frequency characteristics of the four tuning fork resonators with different acceleration inputs. By changing the deflection angle of the goniometer, different acceleration inputs are exerted on the proof mass and transferred to the tuning fork resonators. The test curves shown in Figure 13 indicate that the input acceleration results in an apparent shift in the natural frequency. However, it does not cause significant changes to the resonant amplitude, which demonstrates that the resonators have good mechanical properties. The experiment results indicate that the original resonant frequencies of the four resonators in the microaccelerometer are 25.00 kHz, 25.03 kHz, 28.23 kHz, and 28.33 kHz, respectively. Two pairs of resonators have an approximate frequency difference of 3.2 kHz, which is consistent with the theoretical design of the device. The frequency difference between two pairs of resonators is conducive to not only eliminating the mechanical coupling

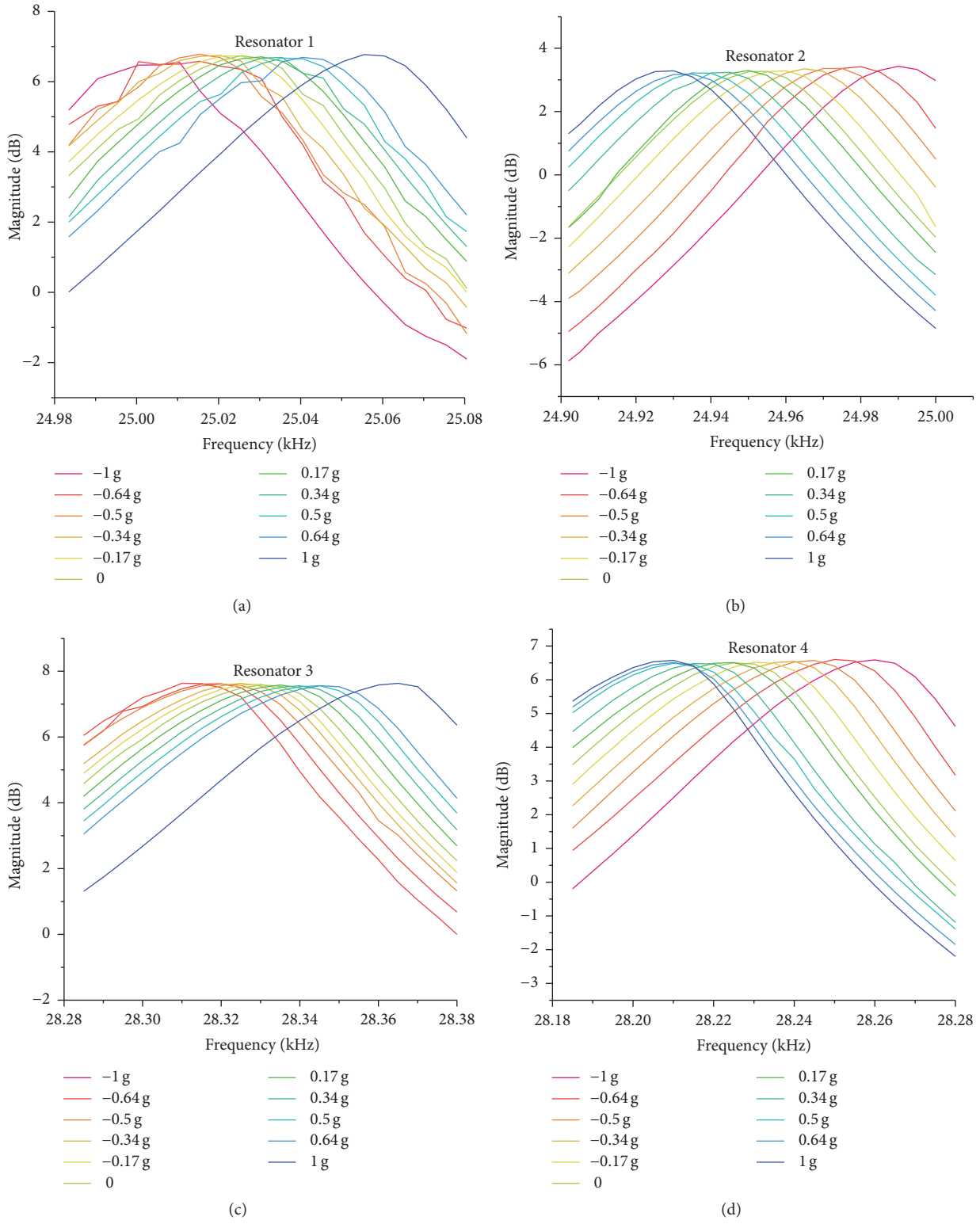


Figure 13: Amplitude-frequency characteristics for the four resonators labeled R1, R2, R3, and R4 in Figure 1 with different acceleration inputs: (a) the first resonator is labeled R1, (b) the second resonator is labeled R2, (c) the third resonator is labeled R3, and (d) the fourth resonator is labeled R4.

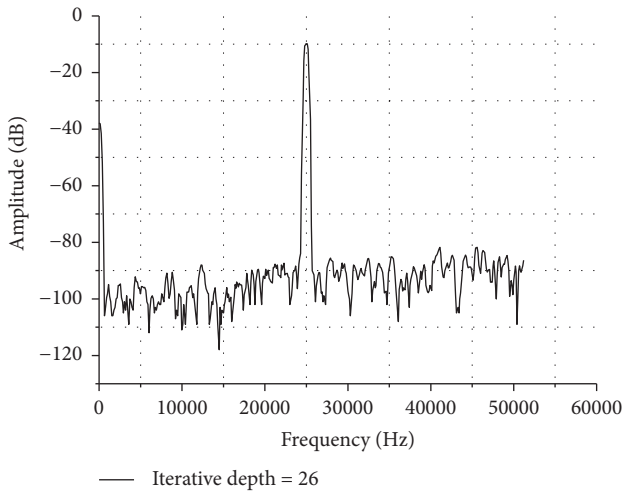


Figure 14: The frequency spectrum of the NCO output at the iterative depth of 26.

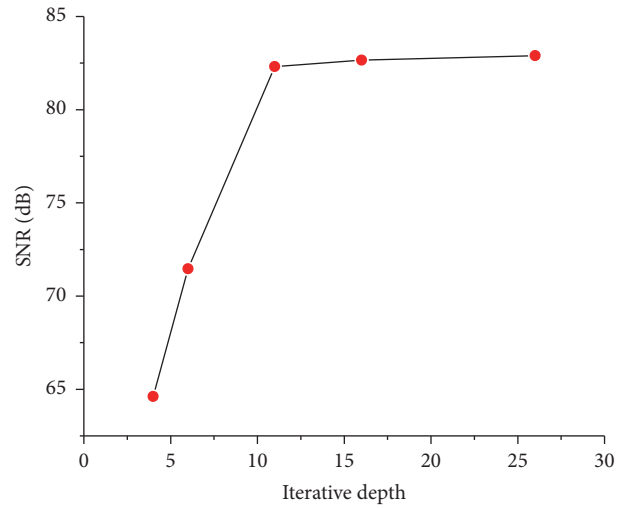


Figure 15: The SNR variation with the iterative depth.

between the two axes but also avoiding the same frequency interference between the resonant circuits. Since the digital closed-loop self-oscillation system can automatically lock the resonant frequencies of the resonators, the frequency difference between two pairs of resonators does not affect the structure and parameter design of the digital closed-loop self-oscillation circuit. However, the scale factors between the two axes will be slightly different due to the structural parameter differences between the two pairs of resonators, which can be corrected through subsequent circuits.

5.2. NCO Test. Figure 14 presents the spectrum of the NCO output at the iterative depth of 26. The center frequency of the NCO is set to 25.00 kHz with a sampling rate of 750.0 kHz. The bits of accumulator and the iteration depth of the CORDIC are set to 28 and 26, respectively. The output signal of the NCO is sent to the DA converter, and the spectrum is measured by the spectrum analyzer. The

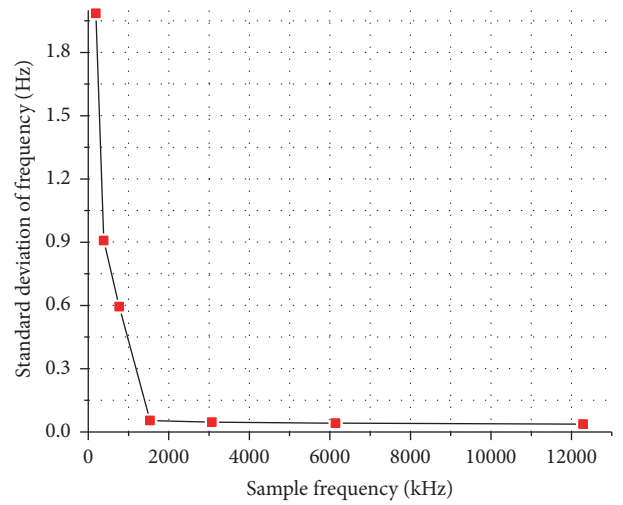


Figure 16: The frequency control precision of the optimized system for different sampling rates.

experiment results demonstrate that the SNR of the NCO is approximately 83.00 dB at the iterative depth of 26.

At the same time, the performance of the NCO at different iterative depths is shown in Figure 15. From the overall trend, the SNR is improved significantly with the increase of the iterative depth. However, the SNR remains essentially unchanged when the iteration depth is greater than 11. The calculated noise amplitude at the iterative depth of 26 is 22.90 μV, according to the experimental spectrum. The main reason for this is the ideal minimum resolution of the DA convertor being 15.26 μV in the reference voltage of 2 V. This analysis illustrates that the SNR is mainly limited by the quantization noise of the DA convertor.

Figure 16 shows the frequency control precision of the optimized system for different sampling rates. The center frequency is set to 25.00 kHz and the sampling rates are varied from 192.0 kHz to 12.29 MHz in the experiment. The standard deviation of the frequency is used to evaluate the control precision of the frequency in the optimized system. The experimental results indicate that the standard deviation of the frequency in the optimized system decreases exponentially with the increase of the sampling frequency. The best frequency variance in the optimized system is 37.80 mHz with a sampling rate of 12.29 MHz. In the conventional system, the sampling frequency of the AD that cannot be arbitrarily changed is determined by its chip clock. Therefore, the frequency control accuracy at the fixed sampling frequency of 750.0 kHz is used in the experiment, which gives a standard deviation of 136.7 mHz. The experimental results demonstrate that the best frequency control accuracy of the optimized system is improved by 3.620 times over that of the conventional system.

5.3. Influence of AD and DA Convertors in the Conventional Control System. Figure 17 gives the experimental results of zero bias stability with different effective bits of the AD and DA convertors. The experimental results illustrate that the

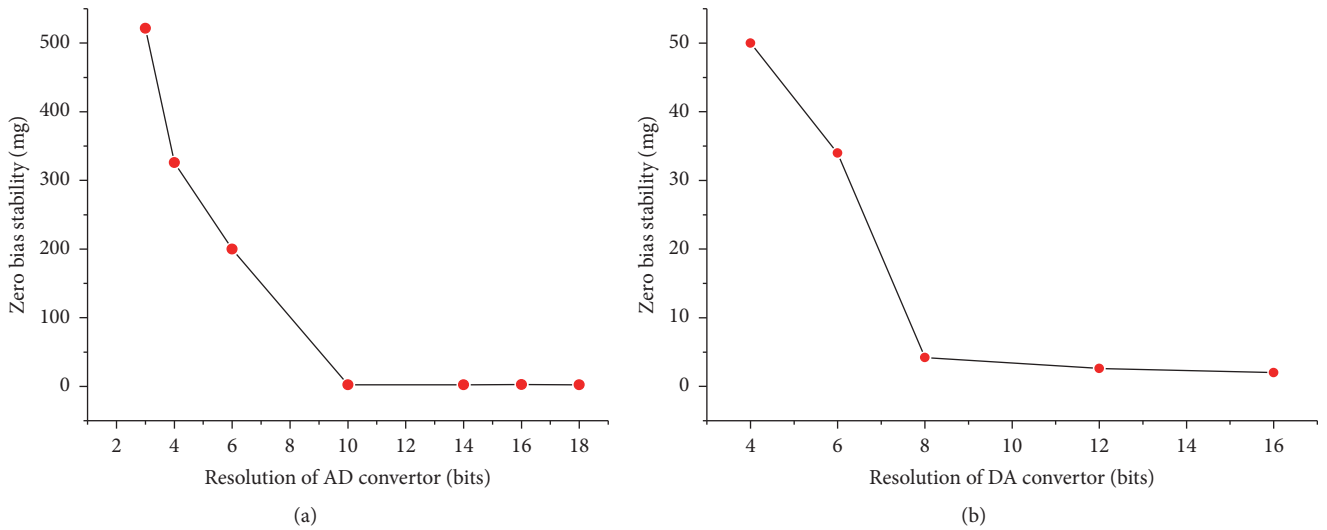


FIGURE 17: Test results of the zero bias stability with different effective bits of the AD and DA convertors: (a) the resolution change of the AD converter with the effective bits of 16 in the DA convertor; (b) the resolution change of the DA converter with the effective bits of 18 in the AD convertor.

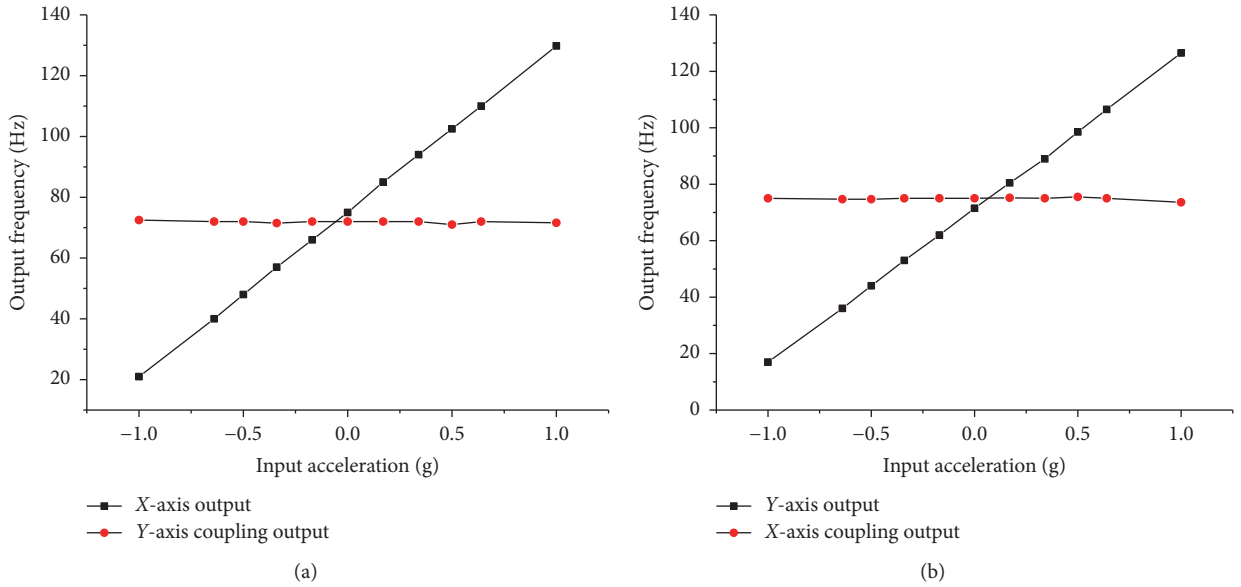


FIGURE 18: Measurement of scale factor: (a) differential frequency output along x-axis; (b) differential frequency output along y-axis.

general trend of the test data is consistent with the simulation. However, the experimental results with different effective bits of the AD and DA convertors shown in Figure 17 are significantly larger than the simulation results, especially in the low effective bits of the AD and DA convertors. Another difference between the experimental data and simulation results is the inflection point. However, this subtle distinction can be ignored as the simulation is implemented under ideal conditions. The differences between the experiment and simulation are mainly due to the bit limit of the multiplier and accumulator of the digital demodulator, quantization noise, the structure noise of the biaxial resonant microaccelerometer, and the interface coupling noise of circuits, which are difficult to simulate in the simulation system. The experiments for different sample rates shown in Figure 5 are not performed as the AD and DA convertors cannot achieve higher sample rates in the actual experimental system.

5.4. System Performance. The experiment for the system performance is performed to confirm the effectiveness of the digital closed-loop driving based on the CORDIC algorithm. The different acceleration rates are exerted on the proof mass by changing the goniometer deflection angle. Figure 18 illustrates that the measured scale factor along the x-axis is 57.55 Hz/g and the transverse sensitivity along the y-axis is 1.730%. Similarly, the scale factor along the y-axis is 53.88 Hz/g, and the transverse sensitivity along the x-axis is 2.960%, which demonstrates that the biaxial resonant

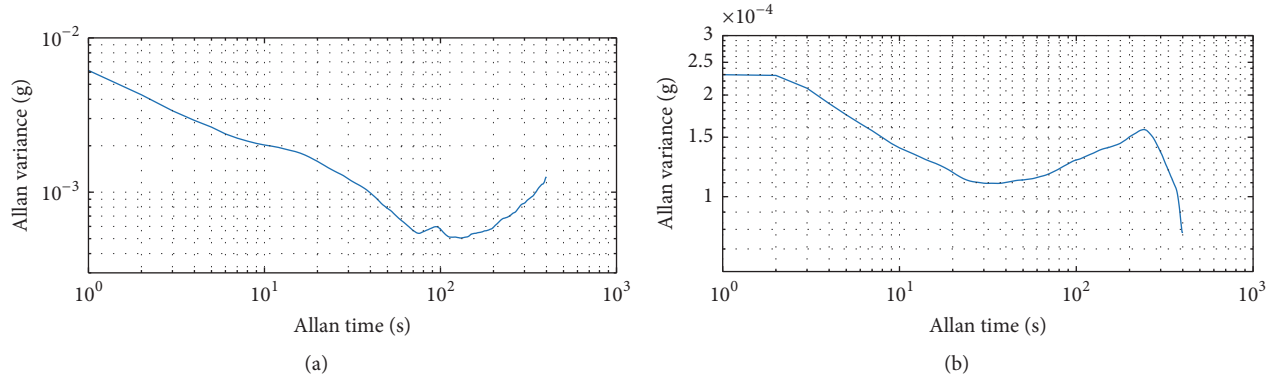


Figure 19: The Allan variance curve of y-axis: (a) the conventional system; (b) the optimized system.

Table 3: The system performance test results.

Test parameter (unit)	The conventional system (y-axis)	The optimized system (y-axis)
Dynamic range (g)	±10.00	±10.00
Scale factor (Hz/g)	53.88	52.21
Zero bias (mg)	−23.00	4.020
Zero bias stability (μg) (Allan variance)	532.7	100.1
Rate random walk ($\mu g/\sqrt{s}$)	91.90	26.80

microaccelerometer has good decoupling characteristics. Figure 19 presents the Allan variance curve along the y-axis. The zero bias stabilities of the Allan variance along the y-axis are 532.7 μg in the conventional system and 100.1 μg in the optimized system. The optimized system improves the bias stability of the resonant microaccelerometer by more than 5.320 times compared to the conventional system. The system performance results are summarized in Table 3. The experimental results demonstrate that the digital closed-loop driving based on the CORDIC algorithm with the PFD for the biaxial resonant microaccelerometer is effective.

6. Conclusions

Presented in this paper are the design, the simulation, and the experiment of a digital closed-loop driving technique using the PFD-based CORDIC algorithm for a biaxial resonant microaccelerometer. The conventional, digital, closed-loop self-oscillation system is implemented with the CORDIC algorithm in the FPGA device. The system simulation results demonstrate that the compromise between the sampling rate and the quantization accuracy of the AD and DA convertor increases the difficulty in further improvements of the system performance in the conventional, digital, closed-loop self-oscillation system. Accordingly, the digital closed-loop self-oscillation using the PFD-based CORDIC is designed to further optimize the system performance. The simulation results demonstrate that the frequency standard deviation of the optimized system with a sampling frequency of 12.29 MHz increases theoretically by 29.20 times compared to that of the conventional system with a sampling frequency of 750.0 kHz. The influences of the iteration depth of the CORDIC algorithm, sampling rate, and quantization accuracy of the AD and DA convertor on system performance are confirmed in the experiments, which is consistent with the simulation conclusions. Simultaneously, the comparison of the experimental results illustrates that the optimized system improves the bias stability of the resonant microaccelerometer by more than 5.320 times compared to that of the conventional system. This demonstrates that the optimized digital closed-loop driving technique using the PFD-based CORDIC for the biaxial resonant microaccelerometer is effective.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

The authors wish to acknowledge the support of the National Natural Science Foundation of China (Grant nos. 61571126 and 61104217), Equipment Pre-Research Field Foundation (Grant no. 6922001217), NSAF (Grant no. U1230114), the Aviation Science Foundation (Grant no. 20150869005), and the China Academy of Space Technology Innovation Foundation and the Eleventh Peak Talents Programme Foundation in the Six New Industry Areas.

References

[1] S. Sung, J. G. Lee, B. Lee, and T. Kang, "Design and performance test of an oscillation loop for a MEMS resonant accelerometer," *Journal of Micromechanics and Microengineering*, vol. 13, no. 2, pp. 246–253, 2003.

[2] S. Sung, J. G. Lee, and T. Kang, "Development and test of MEMS accelerometer with self-sustained oscillation loop," *Sensors and Actuators A: Physical*, vol. 109, no. 1-2, pp. 1–8, 2003.

[3] J. Zhao, G. Xia, Y. Zhao, A. Qiu, and Y. Su, "A Low Power MEMS-ASIC Silicon Resonant Accelerometor with Sub-ug Bias Instability and 30g Full-scale," in *IEEE International Symposium*

on Inertial Sensors and Systems, pp. 46–49, California, USA, 2016.

[4] D. H. Zhai, D. C. Liu, C. H. He et al., "A resonnat accelerometer based on ring-down measurement," in *Proceedings of the 18th International Conference on Solid-State Sensors, Actuators and Microsystems, TRANSDUCERS*, pp. 1125–1128, Alaska, USA, 2015.

[5] S. A. Zotov, B. R. Simon, A. A. Trusov, and A. M. Shkel, "High Quality Factor Resonant MEMS Accelerometer with Continuous Thermal Compensation," *IEEE Sensors Journal*, vol. 15, no. 9, pp. 5045–5052, 2015.

[6] C. Comi, A. Corigliano, G. Langfelder, A. Longoni, A. Tocchio, and B. Simoni, "A Resonant microaccelerometer with high sensitivity operating in an oscillating circuit," *Journal of Microelectromechanical Systems*, vol. 19, no. 5, pp. 1140–1152, 2010.

[7] U. Park, J. Rhim, J. U. Jeon, and J. Kim, "A micromachined differential resonant accelerometer based on robust structural design," *Microelectronic Engineering*, vol. 129, no. C, pp. 5–11, 2014.

[8] R.-E. Hopkins and J.-T. Borenstein, "The silicon oscillating accelerometer: A MEMS inertial instrument for strategic missile guidance," in *The Missile Sciences Conference*, pp. 45–51, 2000.

[9] B. Yang, H. Zhao, B. Dai, and X. Liu, "A new silicon biaxial decoupled resonant micro-accelerometer," *Microsystem Technologies*, vol. 21, no. 1, pp. 109–115, 2014.

[10] S. Yamauchi and T. Watanabe, "All-digital MEMS tuning-fork self-excited vibration control by phase-relation using TAD-based ADPLL," in *Proceedings of the 13th IEEE International NEW Circuits and Systems Conference, NEWCAS*, pp. 1–4, Grenoble, France, 2015.

[11] Y. Liu, C. He, D. Liu, Z. Yang, and G. Yan, "Digital closed-loop driver design of micromechanical gyroscopes based on coordinated rotation digital computer algorithm," in *Proceedings of the 8th Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems, IEEE NEMS*, pp. 1145–1148, Suzhou, China, 2013.

[12] D. Senkal, E.-J. Ng, V. Hong, and Y. Yang, "Parametric drive of a toroidal MEMS rate integrating gyroscope demonstrating < 20 PPM scale factor stability," in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, vol. 28, Estoril, Portugal, 2015.

[13] Z. Yang, X. Jin, H. Ma, and Z. Jin, "CORDIC algorithm based digital detection technique applied in resonator fiber optic gyroscope," *Optical Fiber Technology*, vol. 15, no. 3, pp. 328–331, 2009.

[14] C. Wu, B. Zhou, and J. Fang, "Research on improved CORDIC algorithm for high accuracy DDS signal source," in *Proceedings of the 4th International Conference on Computer Science and Network Technology, ICCSNT*, pp. 1351–1355, Harbin, China, 2015.

[15] H.-J. Hsu and S.-Y. Huang, "A low-jitter ADPLL via a suppressive digital filter and an interpolation-based locking scheme," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 1, pp. 165–170, 2011.

[16] X. Li, H. Li, and B. Yang, "The implementation of improved phase projection method in FPGA," in *Proceedings of the 2nd Annual Conference on Electrical and Control Engineering, ICECE*, pp. 4146–4149, Yichang, China, 2011.