Liu et al. Nanoscale Research Letters (2017) 12:120
DOI 10.1186/s11671-017-1913-3

Nanoscale Research Letters

NANO EXPRESS

Open Access

Strained Germanium Quantum Well PMOSFETs on SOI with Mobility Enhancement by External Uniaxial Stress

Yan Liu[1], Jiebin Niu[2], Hongjuan Wang[1], Genquan Han[1*], Chunfu Zhang[1], Qian Feng[1], Jincheng Zhang[1] and Yue Hao[1]

Abstract

Well-behaved Ge quantum well (QW) p-channel metal-oxide-semiconductor field-effect transistors (pMOSFETs) were fabricated on silicon-on-insulator (SOI) substrate. By optimizing the growth conditions, ultrathin fully strained Ge film was directly epitaxially grown on SOI at about 450 °C using ultra-high vacuum chemical vapor deposition. In situ Si_2H_6 passivation of Ge was utilized to form a high-quality SiO_2/Si interfacial layer between the high-κ dielectric and channels. Strained Ge QW pMOSFETs achieve the significantly improved effective hole mobility μ_{eff} as compared with the relaxed Si and Ge control devices. At an inversion charge density of Q_{inv} of 2×10^{12} cm^{-2}, Ge QW pMOSFETs on SOI exhibit a 104% μ_{eff} enhancement over relaxed Ge control transistors. It is also demonstrated that μ_{eff} of Ge pMOSFETs on SOI can be further boosted by applying an external uniaxial compressive strain.

Keywords: Germanium, MOSFET, Mobility, Quantum well

Background

Germanium (Ge) has been attracting tremendous research interests for future pMOSFET applications due to it possesses the higher hole mobility over Si. Theoretical and experimental results proved that in order for Ge channel transistors to have significantly improved mobility and driving current over their Si and SiGe channel competitors, compressive strain is essential [1–3]. A great deal of efforts were devoted to demonstrating biaxially strained Ge-based ultrathin quantum well (QW) pMOSFETs [2, 4, 5], which have exhibited the advantages of confining hole in the undoped quantum well, eliminating dopant impurity scattering, and accommodating very high strain in channel. Nonetheless, the development of defect-free SiGe buffer with smooth surface on Si raised a major challenge for Ge devices. It was reported that, by optimizing the growth condition and controlling the film thickness precisely, fully strained Ge channel could be pseudomorphically grown directly on Si and silicon-on-insulator (SOI) [6–8]. With the low thermal budget device fabrication process, the strain in channel region was maintained, which substantially boosted the transistor performance. Studies showed that the uniaxial compressive strain is also promising for improving the mobility of Ge pMOSFETs [9–11]. However, there is still lack of the study on the combination effects between uniaxial and biaxial strain on Ge pMOSFETs.

In this paper, ultrathin strained Ge QW pMOSFETs on SOI are realized and characterized. Devices achieve the superior hole mobility to the relaxed Si and Ge control transistors. Electrical performance of Ge QW transistors is further improved by applying the external uniaxial compressive strain being parallel to channel direction.

Methods

Material Growth

Ge channel was epitaxially grown on lightly doped p-type SOI wafer using ultra-high vacuum chemical vapor deposition tool. Before loading into the growth chamber, the top Si layer was thinned down to about 7 nm using dry oxidation followed by the dilute HF etching. It is well known that, as Ge is epitaxially grown on

* Correspondence: hangenquan@ieee.org; gqhan@xidian.edu.cn
[1]State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an 710071, China
Full list of author information is available at the end of the article

Springer Open

© The Author(s). 2017 **Open Access** This article is distributed under the terms of the Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made.

Si, Ge islands tend to form in Stranski-Krastanow mode due to the 4.2% lattice mismatch between Ge and Si. The formation of Ge islands could be prevented by decreasing the growth temperature; nevertheless, the misfit dislocations are preferred to appear in Ge layer to release the strain energy. To achieve the continuous and defect-free epitaxial Ge film, we carried out the growth of Ge (the growth of Ge) on ultrathin SOI with different substrate temperatures. During the growth, the flow rate of GeH_4 in a H_2 carrier gas is 20 sccm, the pressure in growth chamber is about 10^{-4} Pa, and the growth duration is 5 min. Figure 1 shows the atomic force microscope (AFM) images of Ge film on SOI samples grown at various temperatures. The formation of large numbers of Ge islands was observed on the sample grown at 500 °C. With the reduction of growth temperature to 400 °C, it was found that many nanopits were yielded in Ge layer with the self-assembled growth, which partially released the strain energy. A flat surface was achieved for the Ge layer grown at 450 °C without the observation of any nanostructure. Experiments demonstrated that, as 3~5 nm Ge channel was epitaxially grown on SOI, the transition from 2 to 3D growth mode can be effectively suppressed with the growth temperature ranging from 420 to 450 °C.

Device Fabrication

The key process steps for fabricating ultrathin fully strained Ge QW pMOSFETs are shown in Fig. 2a. After the epitaxial growth of strained Ge layer, Ge channel was treated using in situ Si_2H_6 passivation at 350 °C for 15 min. Gate stack comprising hafnium dioxide (HfO_2) by atomic layer deposition and metal gate by physical vapor deposition was formed. After the gate patterning and etching, BF_2^+ was implanted into drain and source regions at an energy of 10 keV and a dose of 1×10^{15} cm^{-2}. Self-aligned metallic source/drain (S/D) was formed by depositing 10 nm nickel followed by a thermal anneal (RTA) at ~450 °C for 30 s. During the Ni germanosilicide, the p-type dopants in S/D regions were partially activated by the dopant segregation. The residual Ni was removed by the concentrated H_2SO_4 cleaning. Using the similar process, Si and Ge control pMOSFETs on bulk substrates were also fabricated.

Figure 2b shows the cross-sectional schematic of a fabricated Ge pMOSFET. Figure 2c depicts the high-resolution transmission electron microscope (HRTEM) image of metal gate stack on strained Ge channel on SOI. The thicknesses of defect-free Ge channel and HfO_2 dielectric layer are 3.7 and 4.0 nm, respectively.

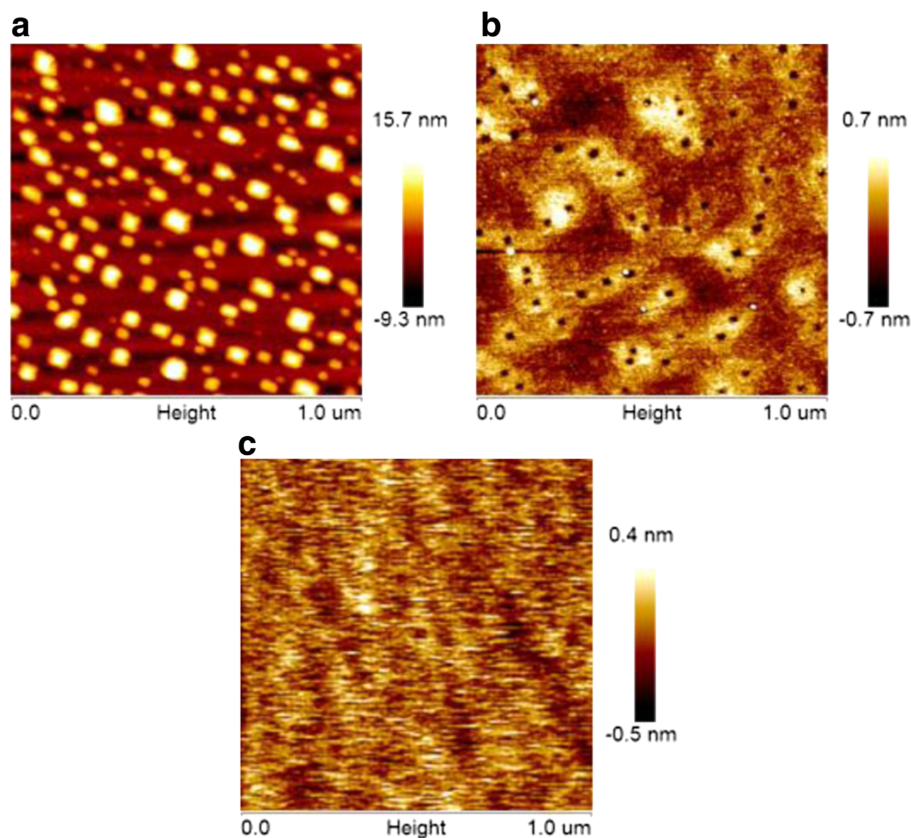

Fig. 1 AFM images of epitaxially grown Ge on ultrathin SOI at **a** 500, **b** 400, and **c** 450 °C

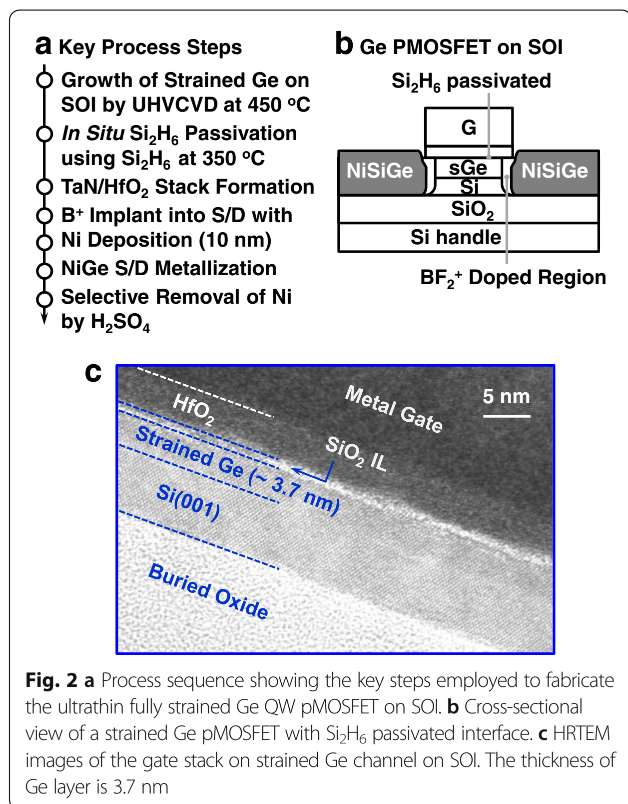

Fig. 2 **a** Process sequence showing the key steps employed to fabricate the ultrathin fully strained Ge QW pMOSFET on SOI. **b** Cross-sectional view of a strained Ge pMOSFET with Si_2H_6 passivated interface. **c** HRTEM images of the gate stack on strained Ge channel on SOI. The thickness of Ge layer is 3.7 nm

Excellent interface quality and a uniform SiO_2/Si interfacial layer (IL) are observed.

Flexure-Based Bending Setup

Uniaxial compressive strain was introduced into the Ge QW pMOSFETs on SOI through a mechanical flexure-based wafer bending apparatus. The apparatus is able to perform four-point bending upon chips positioned between loads and support, as shown in Fig. 3. The uniaxial strain was always applied parallel to the channel direction for the devices. The surface stress σ along the channel direction is calculated by $\sigma = E{\cdot}y{\cdot}t/[2a{\cdot}(L/2 - 2a/3)]$, where E is the Young's Modulus, y is the sample vertical displacement, t is the total thickness of the sample, L is the distance between the two supports, and a is the distance between the support and load [12]. The setup was calibrated with a load cell under the mounting platform and a strain gauge bonding on the sample.

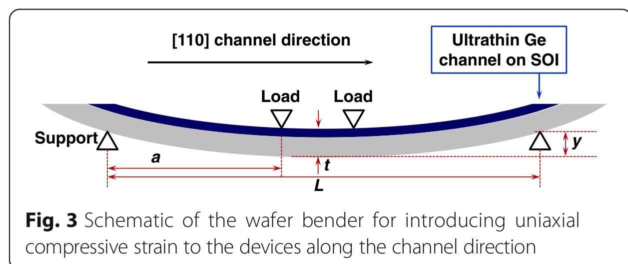

Fig. 3 Schematic of the wafer bender for introducing uniaxial compressive strain to the devices along the channel direction

Before measurement, the handle Si of SOI wafer was thinned down to about 300 μm by back side polishing to make sure it can accommodate the large strain. The values of Young's modulus for Ge along [110] direction is 138 GPa [13].

Results and Discussion

Figure 4a depicts the transfer characteristics of a typical Ge QW pMOSFET on SOI with and without external uniaxial compressive stress. The stress is along [110] and parallel to the channel direction. The gate length L_G of the device is 3.5 μm. Device has a subthreshold swing (SS) of ~90 mV/decade. The uniaxial stress has the negligible impact on the SS and the leakage floor characteristics of the Ge transistor. Here, V_{TH} is defined as the V_{GS} at a constant drive current of 10^{-7} A/μm and a V_{DS} of−0.1 V. V_{TH} is shown to be affected by the applied uniaxial compressive strain. As uniaxial stress is applied, devices exhibit a right shift of V_{TH}. I_{DS}–V_{DS} curves at different V_{GS}–V_{TH} for the devices are illustrated in Fig. 4b, which demonstrate the I_{DS} enhancement in devices under the uniaxial compressive stress. A −250 MPa uniaxial stress provides a 17% Ge I_{DS} enhancement in ultrathin Ge pMOSFET on SOI at V_{DD} of 1.5 V. Figure 4c shows the linear intrinsic transconductance G_M of the same pair of transistors in Fig. 4a. At V_{DS} of −0.1 V, a 24% peak G_M is achieved in devices under −250 MPa external uniaxial strain compared to the Ge QW transistor without uniaxial strain.

To evaluate the intrinsic channel piezoresistance characteristics for the Ge QW pMOSFETs, large amount of devices with and without external uniaxial compressive strain were measured with L_G ranging from 3.5 to 9.5 μm. The total resistance R_{total} as a function of L_G extracted at a gate overdrive of −1.5 V and V_{DS} of −0.1 V are plotted in Fig. 5. The intercept of the fitted lines with the y-axis yields the value of source/drain resistance R_{SD}. R_{SD} of Ge QW pMOSFETs on SOI is about 14 kΩ μm, and it is observed that the external uniaxial stress has little impact on R_{SD}. The slope of $\Delta R_{total}/\Delta L_G$ represents the channel resistance R_{ch}, which is related to the effective hole mobility μ_{eff} and inversion charge density. The uniaxially strained pMOSFETs achieve a 24% reduction in $\Delta R_{total}/\Delta L_G$ slope i.e. R_{ch}, compared to the devices without uniaxial compressive strain. Experiment demonstrates that the impact of external uniaxial strain on inversion capacitance of Ge QW pMOSFETs is negligibly small. Therefore, the decreasing of R_{ch} is attributed to the improvement in μ_{eff} for the transistors with the external uniaxial compressive stress.

μ_{eff} is a crucial factor, which affects the drive current and G_M of the devices. We extracted the μ_{eff} using the $\Delta R_{total}/\Delta L_G$ method. μ_{eff} was calculated by $\mu_{eff} = 1/[WQ_{inv}(\Delta R_{total}/\Delta L_G)]$, where W is the channel width,

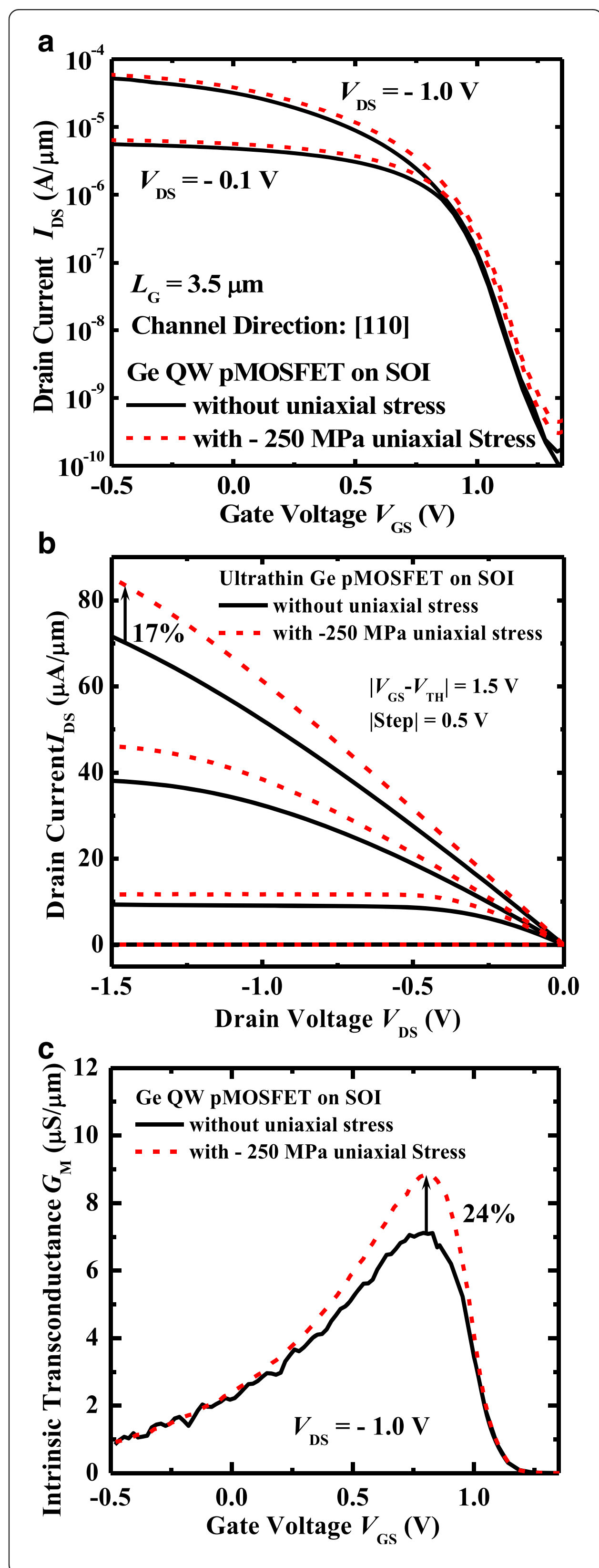

Fig. 4 **a** Transfer and **b** output characteristics of a typical Ge QW pMOSFET on SOI with and without a −250 MPa uniaxial stress, the latter shows the drive current enhancement. **c** Devices under −250 MPa external uniaxial strain is observed to enhance the peak intrinsic transconductance by 24% over the Ge QW transistor without uniaxial strain

Q_{inv} is the inversion charge density in Ge QW channel, and $\Delta R_{tot}/\Delta L_G$ is the slope of the R_{total} as a function of L_G plots as shown in Fig. 5. Q_{inv} in the channel was calculated by integrating the measured C_{inv} versus V_{GS} curves. Figure 6 illustrates the μ_{eff} as function of Q_{inv} characteristics of the Ge QW pMOSFETs on SOI with and without a −250 MPa uniaxial stress. Comparison of μ_{eff} for the Ge QW pMOSFETs with Si and Ge control on bulk wafers is also presented. Ge QW pMOSFETs under uniaxial compressive strain achieve a peak μ_{eff} of 897 $cm^2V^{-1}s^{-1}$. At the low Q_{inv}, Ge QW pMOSFETs under uniaxial compressive strain demonstrate an 18 times higher μ_{eff} as compared with Si control devices. At the Q_{inv} of 2×10^{12} cm^{-2}, Ge QW pMOSFETs without external uniaxial strain demonstrate a 104% μ_{eff} enhancement of over the relaxed Ge control device. This is attributed to the fact that the biaxial compressive strain in ultrathin Ge channel leads to the splitting of valence bands, and top valence band populated by carrier has a reduced effective mass than relaxed Ge [14, 15]. It is noted that, under the external uniaxial compressive strain, the Ge QW devices demonstrate a 24% μ_{eff} enhancement in comparison with the transistors without external strain. It is speculated that the external uniaxial

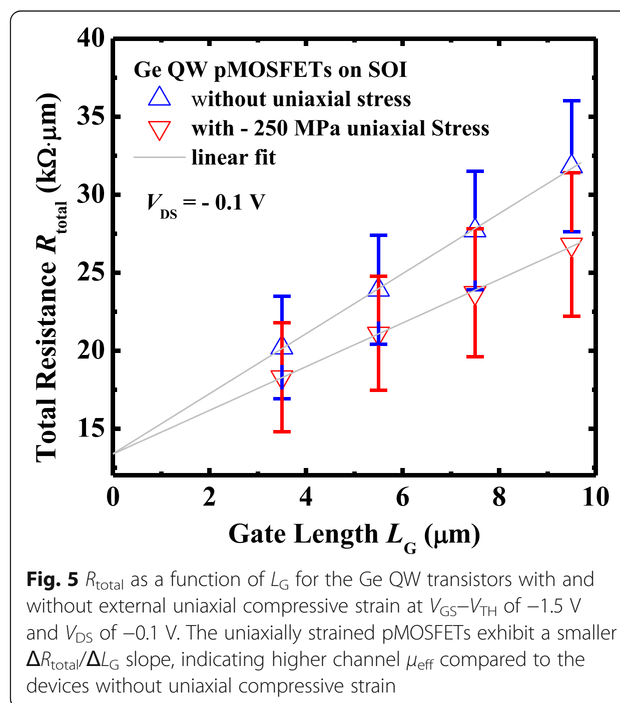

Fig. 5 R_{total} as a function of L_G for the Ge QW transistors with and without external uniaxial compressive strain at V_{GS}–V_{TH} of −1.5 V and V_{DS} of −0.1 V. The uniaxially strained pMOSFETs exhibit a smaller $\Delta R_{total}/\Delta L_G$ slope, indicating higher channel μ_{eff} compared to the devices without uniaxial compressive strain

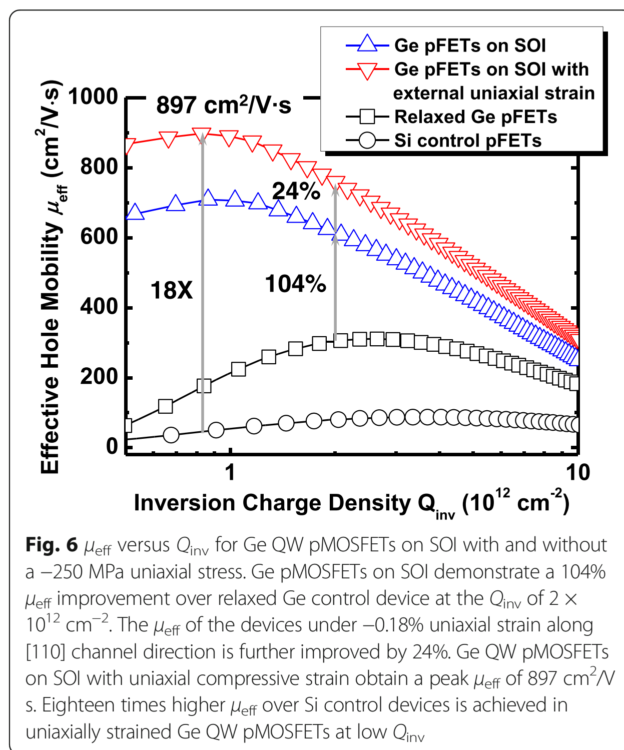

Fig. 6 μ_{eff} versus Q_{inv} for Ge QW pMOSFETs on SOI with and without a −250 MPa uniaxial stress. Ge pMOSFETs on SOI demonstrate a 104% μ_{eff} improvement over relaxed Ge control device at the Q_{inv} of 2 × 10^{12} cm^{-2}. The μ_{eff} of the devices under −0.18% uniaxial strain along [110] channel direction is further improved by 24%. Ge QW pMOSFETs on SOI with uniaxial compressive strain obtain a peak μ_{eff} of 897 cm^2/V s. Eighteen times higher μ_{eff} over Si control devices is achieved in uniaxially strained Ge QW pMOSFETs at low Q_{inv}

compressive strain further decreases the effective hole mobility, leading to the additional mobility enhancement, along transport direction in strained Ge channel.

Conclusions

High-mobility strained Ge QW pMOSFETs with high channel crystallinity on SOI platform are realized. Devices exhibit good transfer and output characteristics and a significantly improved μ_{eff} over Si and Ge control pMOSFETs. Ge QW pMOSFETs on SOI obtain a 104% improvement in μ_{eff} in comparison with the relaxed Ge control transistors at a fixed Q_{inv} of 4 × 10^{12} cm^{-2}. Ge QW pMOSFETs on SOI under an external uniaxial compressive stain achieve a further μ_{eff} enhancement, contributing to the reduced R_{ch} and the improved drive current over the transistors without external uniaxial compressive stain.

Acknowledgements

The authors acknowledge support from the National Natural Science Foundation of China (Grant No. 61534004, 61622405, and 61604112).

Authors' contributions

YL, HW, and GH carried out the experiments and drafted the manuscript. CZ, QF, JZ, and YH provided constructive advice in the drafting. JN gave kind suggestions about the experiment. GH and YL conceived the study and participated in the experiment design. All the authors read and approved the final manuscript.

Competing interests

The authors declare that they have no competing interests.

Author details

[1]State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an 710071, China. [2]Laboratory of Nano-Fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China.

Received: 21 December 2016 Accepted: 10 February 2017
Published online: 16 February 2017

References

1. Hashemi P, Chern W, Lee H–S, Teherani JT, Zhu Y, Gonsalvez J, Shahidi GG, Hoyt JL (2012) Ultrathin strained-Ge channel P-MOSFETs with high-/metal gate and sub-1-nm equivalent oxide thickness. IEEE Electron Device Lett 33(7):943–945
2. Pillarisetty R, Chu-Kung B, Corcoran S, Dewey G, Kavalieros J, Kennel H, Kotlyar R, Le V, Lionberger D, Metz M, Mukherjee N, Nah J, Rachmady W, Radosavljevic M, Shah U, Taft S, Then H, Zelick N, and Chau R (2010) High mobility strained germanium quantum well field effect transistor as the P-channel device option for low power (Vcc = 0.5 V) III–V CMOS architecture, Electron Devices Meeting (IEDM), IEEE International 6.7. 1–6.7. 4.
3. Ghosh B, Fan XF, Register LF, Banerjee SK (2006) Monte Carlo study of strained Germanium Nanoscale bulk pMOSFETs. IEEE Trans Electron Devices 53(3):533–537
4. Witters L, Mitard J, Loo R, Demuynck S, Chew SA, Schram T, Tao Z, Hikavyy A, Sun JW, Milenin AP, Mertens H, Vrancken C, Favia P, Schaekers M, Bender H, Horiguchi N, Langer R, Barla K, Mocuta D, Collaert N, Thean AV-Y (2015) Strained germanium quantum well p-FinFETs fabricated on 45 nm Fin pitch using replacement channel, replacement metal gate and germanide-free local interconnect. Symp VLSI Technol IEEE 2015:T56–T57
5. Han G, Wang Y, Liu Y, Zhang C, Feng Q, Liu M, Zhao S, Cheng B, Zhang J, Hao Y (2016) GeSn quantum well P-channel tunneling FETs fabricated on Si (001) and (111) with improved subthreshold swing. IEEE Electron Device Lett 37(6):943–945
6. Hsu C-C, Tsai Y-H, Chen C-W, Li J-H, Lin Y-H, Lee Y-J, Luo G-L, Chien C-H (2016) High-performance Schottky contact quantum-well germanium channel pMOSFET with low thermal budget process. IEEE Electron Device Lett 37(1):8–11
7. Krishnamohan T, Krivokapic Z, Uchida K, Nishi Y, Saraswat KC (2006) High-mobility ultrathin strained Ge MOSFETs on bulk and SOI with low band-to-band tunneling leakage: experiments, IEEE trans. IEEE Trans Electron Devices 53(5):990–999
8. Peng CY, Yuan F, Lee MH, Yu C-Y, Maikap S, Liao MH, Chang ST, Liu CW (2005) Novel schottky barrier strained germanium PMOS. Int Semiconductor Device Res Symp 2005:84–85
9. Weber O, Irisawa T, Numata T, Harada M, Taoka N, Yamashita Y, Yamamoto T, Sugiyama T, Takenaka M, Takagi S (2007) Examination of additive mobility enhancements for uniaxial stress combined with biaxially strained Si, biaxially strained SiGe and Ge channel MOSFETs. IEEE Int 2007:719–722, Electron Devices Meeting (IEDM)
10. Kim R, Avci UE, Young IA (2015) CMOS performance benchmarking of Si, InAs, GaAs, and Ge nanowire n- and pMOSFETs with Lg = 13 nm based on atomistic quantum transport simulation including strain effects. IEEE Int 2015:34.1.1–34.1.4, Electron Devices Meeting (IEDM)
11. Ikeda K, Moriyama Y, Kamimuta Y, Ono M, Irisawa T, Oda M, Kurosawa E, Tezuka T (2013) Advantage of (001)/<100 > oriented channels in biaxially- and uniaxially strained-Ge-on-insulator pMOSFETs with NiGe metal source/drain. IEEE Int 2013:26.2.1–26.2.4, Electron Devices Meeting (IEDM)
12. Suthram S, Ziegert JC, Nishida T, Thompson SE (2007) Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (~1.5 GPa) channel stress. IEEE Electron Device Lett 28(1):58–61
13. Adachi S (2009) Properties of semiconductor alloys: group-IV, III-V and II-VI semiconductors [M]. Wiley, Chichester
14. Liu M, Han G, Liu Y, Zhang C, Wang H, Li X, Zhang J, Cheng B, Hao Y (2014) Undoped Ge0.92Sn0.08 quantum well PMOSFETs on (001), (011) and (111) substrates with in situ Si2H6 passivation: high hole mobility and dependence of performance on orientation. Symp IEEE 2014:1–2, VLSI Technology
15. Fischetti MV, Laux SE (1996) Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys. J Appl Phys 80:2234