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Research Article

A 3.22–5.45 GHz and 199 dBc/Hz FoMT CMOS Complementary Class-C DCO

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This paper implements a complementary Class-C digitally controlled oscillator (DCO) with differential transistor pairs. The transistors are dynamically biased by feedback loops separately benefiting the robust oscillation start-up with low power consumption. By optimizing three switched capacitor arrays and employing fractional capacitor array with sigma-delta modulator (SDM), the presented DCO operates from 3.22 GHz to 5.45 GHz with a 51.5% frequency tuning range and 0.1 ppm frequency resolution. The design was implemented in a 65 nm CMOS process with power consumption of 2.8 mA at 1.2 V voltage supply. Measurement results show that the phase noise is about −126 dBc/Hz at 3 MHz offset from a 5.054 GHz carrier frequency with the $1/f^3$ corner frequency of 260 KHz. The resulting FoMT achieves 199.4 dBc/Hz and varies less than 2 dB across the frequency tuning range.

1. Introduction

Combining the high spectral purity, wide FTR, and low power consumption is still one of the most challenging targets in the design of frequency synthesizers, especially for the cellular GSM/WCDMA/LTE applications. In recent years, ADPLLs are deeply researched and widely used in cellular applications because of their downscaled area, low power consumption, and improved phase noise performance in advanced CMOS technology [1, 2]. DCO is one of the most challenging design blocks because good phase noise performance should be ensured with low power consumption and it needs to satisfy the wide FTR and high-frequency resolution simultaneously in ADPLL.

Compared with traditional *LC*-tank oscillators, the differential transistor pairs based Class-C oscillator delivers briefer and taller pulses and maximizes the output oscillation amplitude, which leads to a minimization of the phase noise [3]. It means that the phase noise can be improved theoretically with the same current consumption.

This paper implements a wide FTR and high FoMT Class-C DCO based on 65 nm 1P9M CMOS process. Two feedback loops ensure the robust oscillation start-up of DCO [4, 5], which is achieved by adjusting the DC biasing voltage

of the differential transistor pairs synchronously reducing power consumption. The FTR and frequency resolution of the presented DCO are improved and optimized by employing the three capacitor arrays and the fractional array with SDM.

The remaining paper is divided into three parts. Description of the presented complementary Class-C DCO is given in Section 2 and measurement results are shown in Section 3. Conclusion is described in Section 4.

2. Complementary Class-C DCO

2.1. Architecture Description. Figure 1 shows the complementary Class-C DCO architecture. Two cross-coupled pairs M_1/M_2 and M_3/M_4 provide negative resistance to recover the energy losses in the resonant load. The current mirror is made up of M_1/M_2 and M_{1bias}/M_{2bias} to provide the dc current bias, and it also has a high enough transconductance initially by using the negative feedback to ensure a robust start-up oscillation. Moreover, in steady state, the bias voltage V_{BN} falls from its start-up value which maximizes the output swing [4]. M_5 works as a level shifter to provide dc bias voltages V_{BP} and V_T through the common-mode negative feedback. *LC*-tank is composed of a tapped inductor and three capacitor arrays.
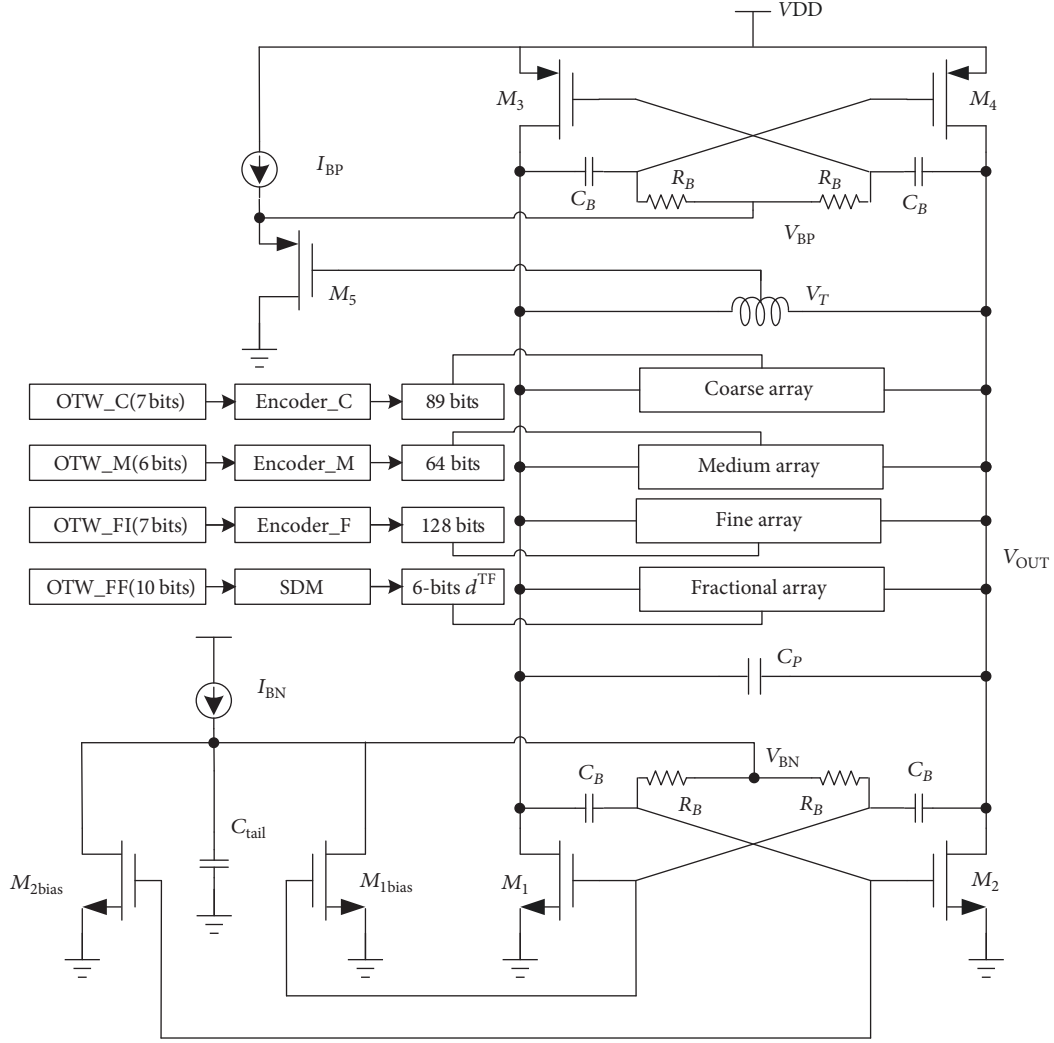
Figure 1: Schematic view of Class-C DCO.

2.2. Design of Capacitor Arrays. DCO's resonant frequency f_{CKV} can be tuned by switching the varactors between on-state and off-state as (1), in which $C_{0,k}$, d_k, and ΔC_k are the k_{th} varactor's off-state capacitance value, digitally controlled signal, and ΔC, separately. ΔC is the capacitance differential value between the on-state and off-state and C_p is the whole parasitic capacitance. Capacitor arrays include coarse array, medium array, and fine array and their corresponding FTS are K_{DCO_C}, K_{DCO_M}, and K_{DCO_F}, respectively. The capacitor arrays are constructed by PMOS varactor because of its high density capacitance.

$$f_{CKV} = \frac{1}{2\pi \sqrt{L \left\{ \sum_{k=0}^{N-1} \left(C_{0,k} + \overline{d_k} \Delta C_{k-1} \right) + C_p \right\}}}. \quad (1)$$

For coarse array, K_{DCO_C} is proportional to the inductor value L, ΔC, and the cube of f_{CKV} as shown in (2):

$$K_{DCO\_C} = \frac{\Delta f}{LSB} \approx \frac{\partial f}{\partial C} \cdot \frac{\Delta C}{LSB} = 2\pi^2 L f_{CKV}^3 \frac{\Delta C}{LSB} \quad (2)$$

$$H_{ol}(s) = \left(\alpha + \rho \cdot \frac{f_R}{s} \right) \cdot \frac{f_R}{s} \cdot \frac{K_{DCO\_C}}{\widehat{K}_{DCO}}. \quad (3)$$

Equation (3) gives the *s*-domain open loop transfer function of ADPLL [2], α and ρ are loop parameters, f_R is reference clock, and $\widehat{K}_{DCO}$ is the normalized gain of DCO. In coarse array, K_{DCO_C} changes 4.85 times ($\approx (5.45/3.22)^3$) across the entire FTR, and ADPLL's $H_{ol}(s)$ also changes with K_{DCO_C} as (3), which will result in instability of ADPLL loop. Therefore, varactors with different ΔC value are adopted at different frequency points realizing a constant K_{DCO_C} to ensure the loop stability.

$$K_{DCO\_C,i} = \frac{1}{2\pi \sqrt{LC}} - \frac{1}{2\pi \sqrt{L \left(C + \Delta C_{i-1} \right)}}$$

$$K_{DCO\_C,i+1} = \frac{1}{2\pi \sqrt{L \left(C - \Delta C_i \right)}} - \frac{1}{2\pi \sqrt{LC}}. \quad (4)$$

For *LC*-DCO, the i_{th} K_{DCO_C} and the $(i+1)_{th}$ K_{DCO_C} can be calculated by (4), where ΔC_{i-1}, ΔC_i, and C are the i_{th} ΔC, the $(i+1)_{th}$ ΔC, and all the capacitors of the coarse array, respectively. In order to get constant K_{DCO_C}, $K_{DCO,i}$ should
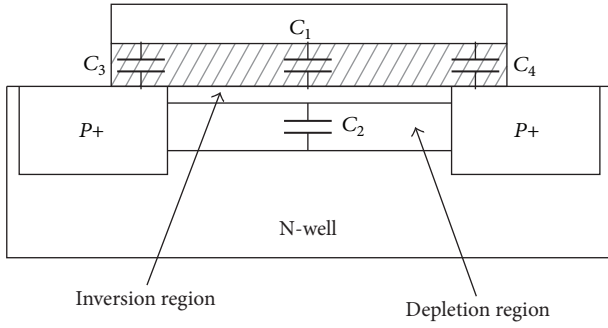
FIGURE 2: Parasitic capacitance model in PMOS varactor.

be equal to $K_{\mathrm{DCO},i+1}$, which means

$$1 - \frac{1}{\sqrt{1 + \Delta C_{i-1}/C}} = \frac{1}{\sqrt{1 - \Delta C_i/C}} - 1. \tag{5}$$

From (5), it can be concluded that the linearity of $K_{\mathrm{DCO\_C}}$ only depends on $\Delta C_i/C$. Finally, the coarse array is designed according to (2)~(5) with constant 24 MHz/LSB's $K_{\mathrm{DCO\_C}}$ which is equal to the reference clock 24 MHz. 89 varactors make up the coarse array to cover the wide FTR and they are decoded from 7 bits coarse oscillator tuning word (OTW), as shown in Figure 1; the postfixes _C, _M, _FI, and _FF are, respectively, the OTW of coarse array, medium array, integral fine array, and fractional fine array.

For the wide FTR application, the coarse array has the varactors with the biggest ΔC in the resonant tank. For PMOS varactor shown in Figure 2, the relevant parasitic capacitance can be classified into three parts as shown in Figure 2: (1) the oxide layer capacitance between gate and channel: $C_1 = WLC_{\mathrm{OX}}$, where C_{OX} is the capacitance of gate oxide layer per unit area and W and L are the gate width and gate length, respectively; (2) the depletion layer capacitance between substrate and channel: $C_2 = WL\sqrt{q\varepsilon_{\mathrm{si}}N_{\mathrm{nwell}}/(4\varphi_F)}$, where q is a charge constant, $\varepsilon_{\mathrm{si}}$ is the dielectric constant of silicon, N_{nwell} is the doping concentration of N-well, and φ_F is the built-in potential; (3) the overlapping capacitance among gate, source, and drain: C_3 and C_4 equal to WC_{OV}, where C_{OV} is the overlapping capacitance per unit width.

Therefore, when the PMOS varactor operates in inversion region, capacitance is maximized to C_{max}. When the PMOS varactor operates in depletion region, capacitance is minimized to C_{min}.

So the capacitance ratio is

$$C_R = \frac{C_{\mathrm{max}}}{C_{\mathrm{min}}} = \frac{LC_{\mathrm{OX}} + 2C_{\mathrm{OV}}}{L\sqrt{q\varepsilon_{\mathrm{si}}N_{\mathrm{nwell}}/(4\varphi_F)} + 2C_{\mathrm{OV}}}. \tag{6}$$

Because $C_{\mathrm{OV}} > \sqrt{q\varepsilon_{\mathrm{si}}N_{\mathrm{nwell}}/(4\varphi_F)}$, C_R increases when L is increased, and higher C_R means the wider FTR.

When PMOS varactor operates in depletion region, channel is not formed; the parasitic resistance only includes gate resistance R_g and metal contact parasitic resistance of source and drain R_a, so the Q value of PMOS varactor in depletion region is

$$Q_{\mathrm{dep}} = \frac{1}{\omega \left(R_g + R_a \right) C_{\mathrm{min}}}. \tag{7}$$

However, when the PMOS varactor lies in inversion region, the Q value can be inferred from [9] as the following equation shows:

$$Q_{\mathrm{inv}} = \frac{12k_p \left(V_{\mathrm{GS}} - V\mathrm{Tp} \right)}{\omega C_{\mathrm{OX}} L^2}. \tag{8}$$

In (8), k_p is the gain factor of PMOS transistor, V_{GS} is the voltage difference between gate and source, and $V\mathrm{Tp}$ is the threshold voltage for PMOS transistor. It can be concluded that Q_{inv} is inversely proportional to the square of L.

Therefore, the Q value, symmetry, and C_p are mainly determined by the coarse array. For the coarse array, it is difficult to trade off the Q value and the region of FTR. Finally, the channel length of the coarse array is set to 600 nm. As shown in the postsimulation in a 65 nm CMOS process, the Q value is higher than 25 and the C_R is about 7. Both of them satisfy the phase noise and the FTR requirements.

However, for the medium and fine array, frequency resolution is the most important design factor. 200 nm and 60 nm channel length are chosen, respectively, for high-frequency resolution and high Q value. Both of them are composed of unit cap array because their FTS varies a little with the change of frequency and these two arrays' FTS have little effect on the loop stability of ADPLL. The FTR of medium and fine arrays should respectively cover several LSBs of coarse and medium arrays so that the OTW of current array will not overflow due to the process, voltage, and temperature (PVT) variations. In the process of ADPLL locking, OTW overflow means that medium tuning or fine-tuning period cannot be finished and loss-of-lock may occur. According to the possible largest frequency error due to PVT variations and the required frequency resolution of the current locking period, 6-bit medium arrays and 7-bit fine arrays are designed to cover 4 LSBs of $K_{\mathrm{DCO\_C}}$ and 8 LSBs of $K_{\mathrm{DCO\_M}}$, respectively. Finally, the locking process of ADPLL can be divided into three frequency locking periods step by step without the possibility of loss-of-lock due to OTW overflow.

In order to improve the phase noise performance of the DCO, MOS varactor is controlled digitally. As shown in Figure 3, OTW (Oscillator Tuning Word) is decoded into the thermal code to control the on/off states of MOS varactor with an inverting driver. The voltage level of digital control signal d_k can be adjusted by V_{High} and V_{Low}. Figure 3 also shows the curve of a PMOS varactor capacitance versus V_{GS} (C-V curve). MOS varactors change linearly from V_1 to V_2 and A_0 is the output amplitude of DCO. During the whole oscillation period, the original C-V curve has to be transferred into the average C-V curve with red dashed dotted line as shown in Figure 3. Therefore, in order to stop the PMOS varactor from inducing the noise on the d_k, the varactor must be working in the on/off states region of the average C-V curve.
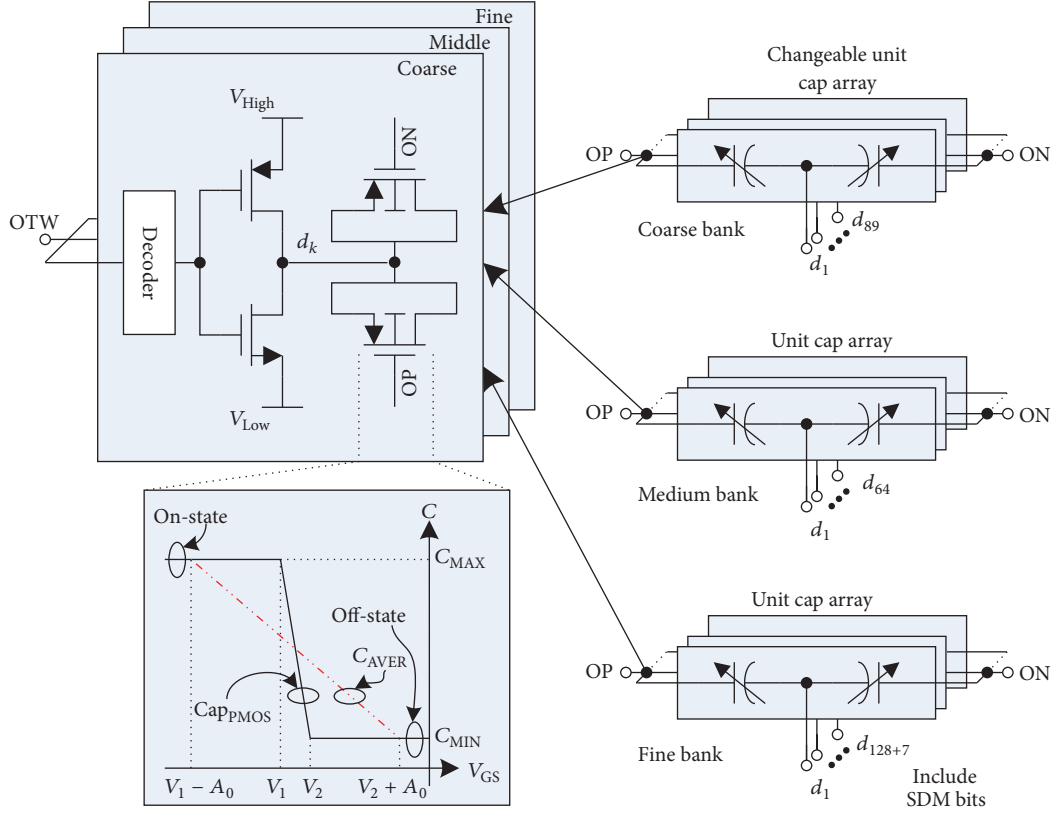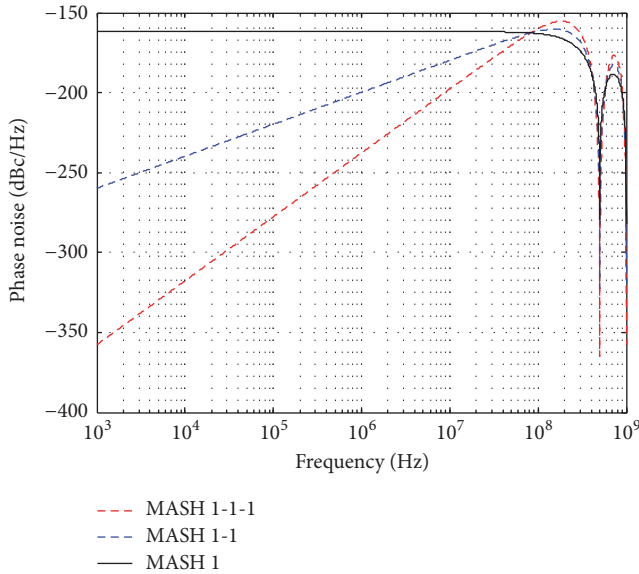
FIGURE 3: DCO capacitor array.

FIGURE 4: The comparison of phase noise contribution of SDM.

The finite frequency tuning resolution introduces the quantization noise and contributes the output phase noise of the ADPLL and hence a small tuning step is desired. The frequency resolution requirement is 0.1 ppm, but the smallest FTS is limited by the smallest ΔC in 65 nm process. Figure 4

compares the phase noise contribution among MASH 1, MASH 1-1, and MASH 1-1-1 SDM; it can be seen that MASH 1-1-1 SDM has the lowest in-band phase noise contribution and the best noise shaping character. Moreover, their out-band phase noise contributions are almost the same. Therefore, 10-bit OTW_FF is dithered with MASH 1-1-1 SDM to control 6-bit fractional capacitor arrays to improve the frequency resolution and decrease the noise contribution. The phase noise contribution of SDM to ADPLL is simulated with MATLAB as shown and it is below -150 dBc/Hz, which means it affects in a small way the whole phase noise performance. In Figure 5, $Eq_1(z)$, $Eq_2(z)$, and $Eq_3(z)$ are the quantization noise of each accumulator. Therefore, the output frequency of SDM can be deduced from

$$C_1 = OTW_{F\_F} + \left(1 - z^{-1}\right) * Eq_1(z)$$

$$C_2 = -Eq_1(z) * z^{-1} + \left(1 - z^{-1}\right) * Eq_2(z)$$

$$C_3 = -Eq_2(z) * z^{-1} + \left(1 - z^{-1}\right) * Eq_3(z)$$

$$\begin{aligned} f_{out} &= \left[C_1 z^{-3} + C_2 \left(z^{-2} - z^{-3}\right) + C_3 \left(z^{-1} - 2z^{-2} + z^{-3}\right) \right] \\ &\quad * K_{DCO\_F} \\ &= \left[OTW_{F\_F} * z^{-3} + z^{-1} \left(1 - z^{-1}\right)^3 * Eq_1(z) \right] \\ &\quad * K_{DCO\_F}. \end{aligned} \quad (9)$$
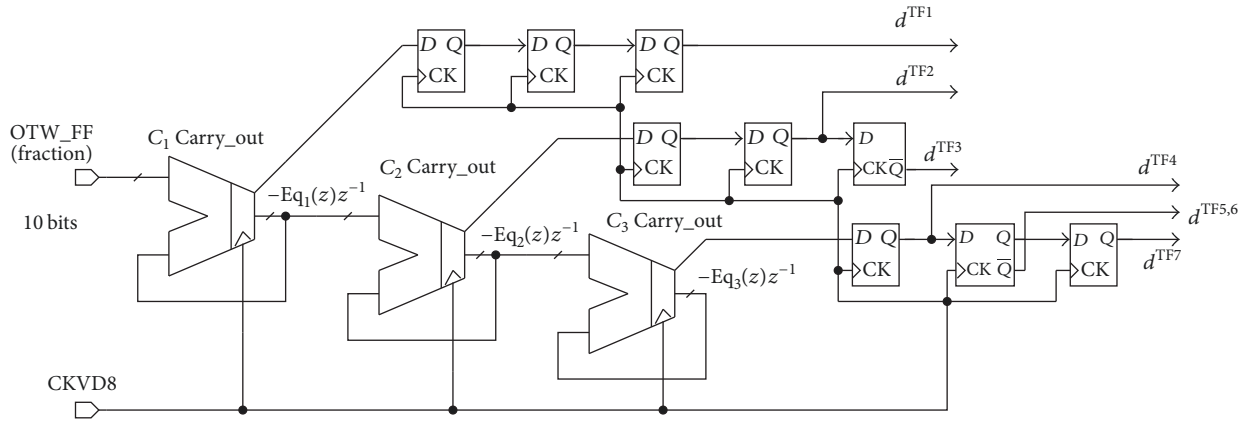
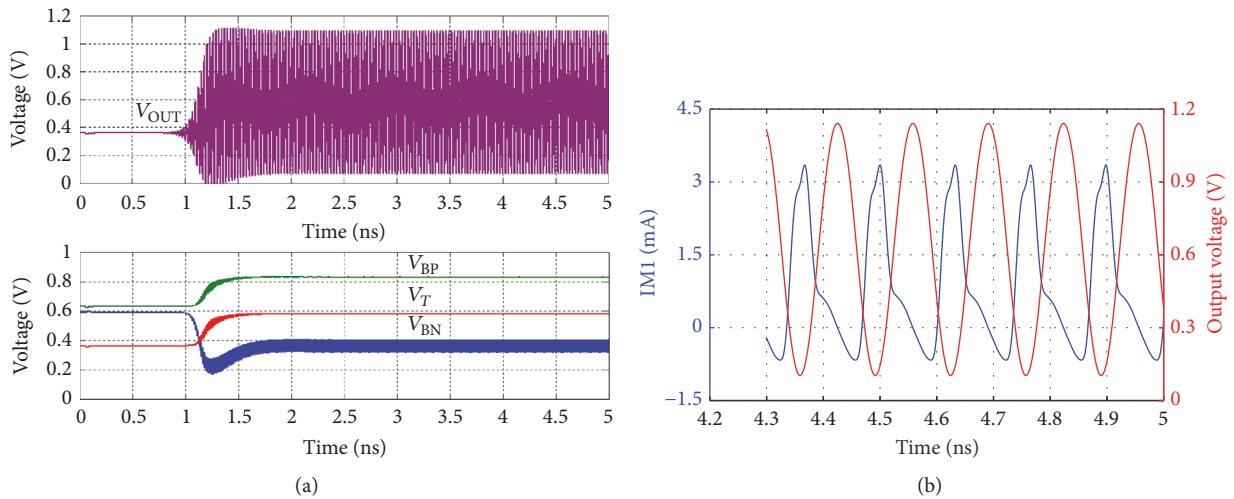FIGURE 5: MASH 1-1-1 sigma-delta modulator.

(a)

(b)

FIGURE 6: Transient voltage waveform of Class-C DCO (a) and $M1$ current transient simulation result (b).
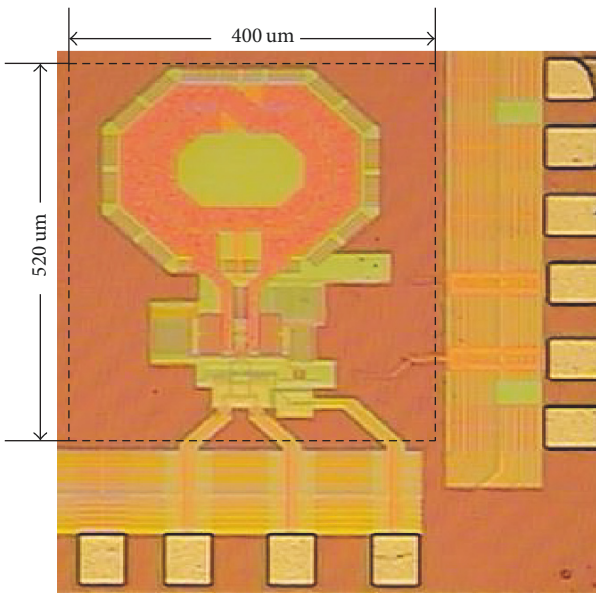

FIGURE 7: Die photo of Class-C DCO.

2.3. Class-C DCO's Negative Feedback Loops.

In Figure 1, current I_{BP} is chosen to bias M_5 providing a level shift voltage. A RC network is used to provide a dc bias voltage, and V_{BP} is higher than the tank common-mode voltage, which permits a larger resonator swing before the M_3/M_4 is pushed into the triode region. This is the same technique employed to bias the M_1/M_2. Moreover, a high RC constant of the RC biasing network is used to low-pass filter the noise introduced to V_{BN} and V_{BP}, optimizing the phase noise [5]. C_{tail} not only integrates the difference between I_{BN} and the current exhausted by the DCO but also filters the high-frequency noise contribution from M_{1bias}/M_{2bias}, improving the phase noise [4].

The simulated transient voltage of DCO is given in Figure 6(a); V_{out} is the oscillation output of DCO. Initially, the M_{1bias}/M_{2bias} are diode-connected (at DC) and I_{BN} is mirrored (multiplied by N) to the DCO core, which makes both PMOS and NMOS cross-coupled MOSFET work in saturation region and provide a high transconductance to guarantee a robust start-up. As the oscillator amplitude is increased, the average current I_{DC} depleted by M_{1bias}/M_{2bias}
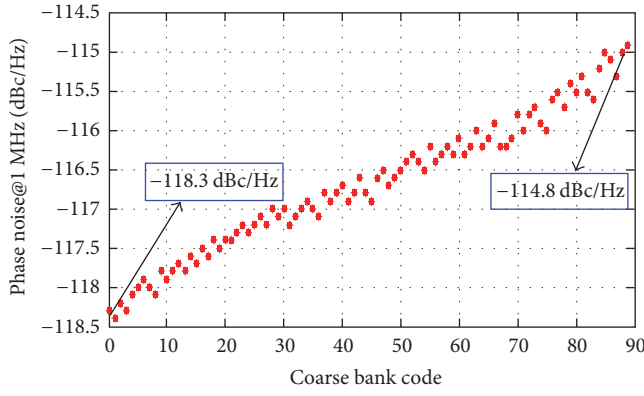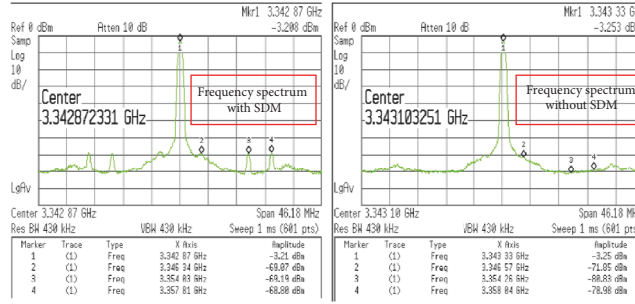
(a)
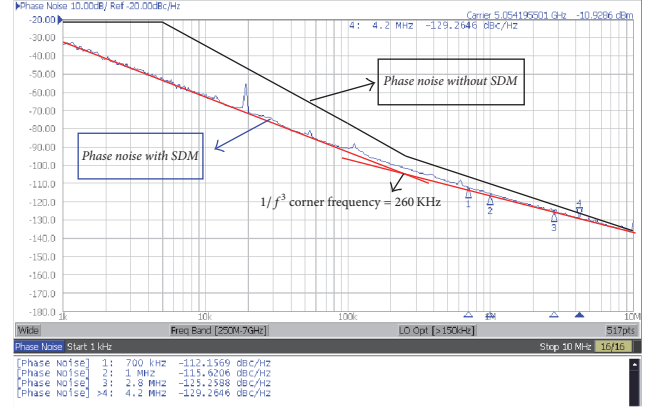
(b)

(c)

FIGURE 8: Measurement results of phase noise @ 1 MHz offset versus Coarse Code (a) phase noise of Class-C DCO at 5.054 GHz (b) and frequency spectrum with/without SDM (c).
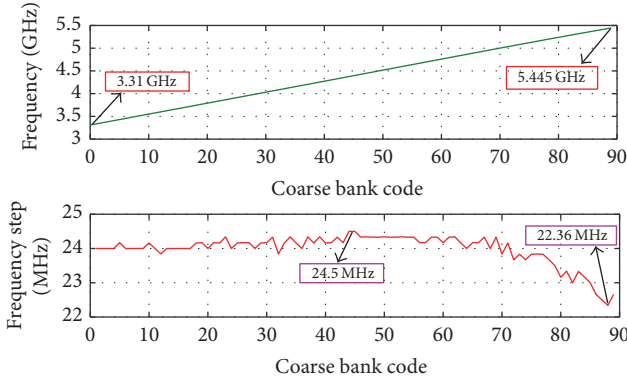

FIGURE 9: Measurement results of frequency range and frequency step of coarse array.

increases and then the superfluous current will be integrated into C_{tail} reducing V_{BN} and guiding the switching pair M_1/M_2 to work in Class-C mode. At the same time, V_{BP} increases and pushes PMOS working in Class-C mode. V_T is finally changed to the half value of the VDD to offer the common-mode voltage of DCO and the same overdrive of PMOS and NMOS pairs. Figure 6(b) shows the transient simulation result of M_1's current (blue line) when M_1 operates at Class-C mode; the tall and short pulses maximize the output oscillation

amplitude (red line), which minimizes the phase noise of DCO.

Referring to the noise analysis in [10], the proposed DCO's noise from feedback loop can be inferred in (10), where $\overline{v_{nR_B}^2}$, $\overline{v_{nr_0,M5}^2}$, and $\overline{v_{nI_B}^2}$ are, respectively, the white noise voltage power spectral density by bias resistor R_B, bias MOSFET M_5, and bias MOSFET $M_{1\text{bias}}/M_{2\text{bias}}$. ω_p is the single pole in the feedback loop. The $g_{\text{nl}}^2(\theta_c)\Gamma_{\text{osc}}^2(\theta_c)$ is the amplification and frequency translation that the feedback loop noise must undergo first.

$$
\begin{aligned}
N_{\text{FL}} \\
&= \frac{1}{T}\int_{-\theta_C/2}^{\theta_C/2}\frac{2\overline{v_{nR_B}^2}+\overline{v_{nr_{0,M5}}^2}+\overline{v_{nI_B}^2}}{1+\omega_p^2}g_{\text{nl}}^2\left(\theta_c\right)\Gamma_{\text{osc}}^2\left(\theta_c\right)d\theta_c \\
&= \frac{2\overline{v_{nR_B}^2}+\overline{v_{nr_{0,M5}}^2}+\overline{v_{nI_B}^2}}{1+\omega_p^2}g_0^2 f_{\text{fl}}\left(V_{\text{OSC}}\right).
\end{aligned}
\tag{10}
$$

Therefore, the total amount of phase noise can be deduced in (11) where K is Boltzmann constant, T_k is the absolute temperature in Kelvin, C is the capacitor in LC resonant bank, V_{OSC} is the oscillation amplitude of DCO, $2R$ is the parasitics losses, and γ is the technology coefficient. $f_{\text{cp}}(V_{\text{OSC}})$ and
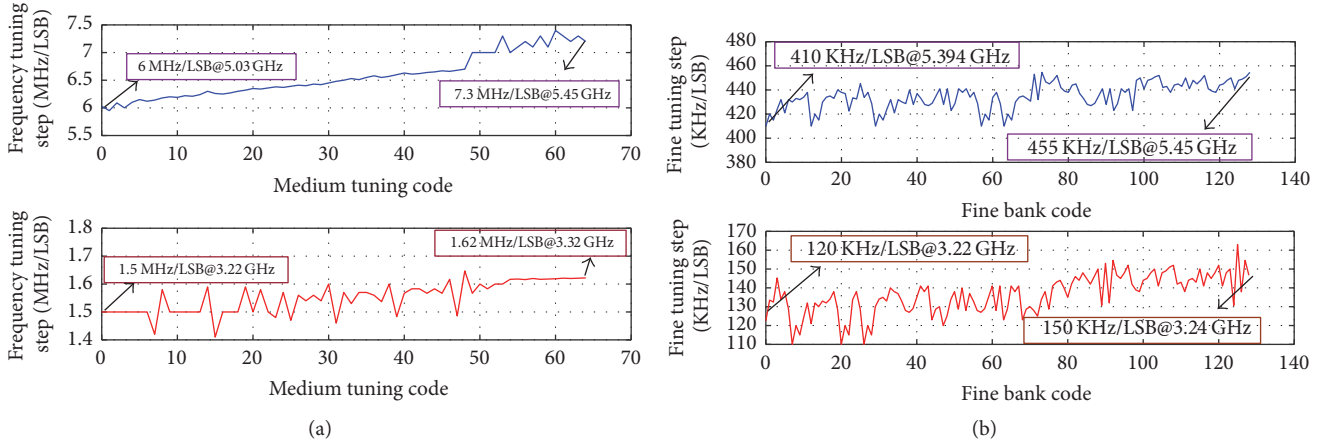
FIGURE 10: Measurement results of frequency range and frequency step of medium array (a) and fine array (b).

$f_{fl}(V_{OSC})$ are, respectively, weighing factors of cross-coupled MOSFETs and feedback loops.

$$\text{PN}(\Delta\omega) = \frac{KT_k}{\Delta\omega^2 C^2 V_{osc}^2} \left(\frac{1}{R} + \frac{\gamma}{\alpha} g_0 f_{cp}(V_{osc}) \right)$$
$$+ \frac{2\overline{v_{nR_B}^2} + \overline{v_{nr_{0,M5}}^2} + \overline{v_{nI_B}^2}}{\Delta\omega^2 C^2 V_{osc}^2 \left(1 + \omega_p^2 \right)} g_0^2 f_{fl}(V_{OSC}).$$

(11)

3. Measurement Results

The Class-C DCO was fabricated in a standard 65 nm CMOS process. Figure 7 offers the die photo of Class-C DCO; it occupies the area of $0.21\,\text{mm}^2$ without PADs. Figure 8(a) shows that the different phase noise measurement results in 1 MHz frequency offset at the different resonant frequency, which changes with coarse array code from −118.3 dBc/Hz to −114.8 dBc/Hz. The phase noise measurement results of Class-C DCO with SDM and without SDM at 5.054 GHz are shown in Figure 8(b); the $1/f^3$ corner frequency is about 260 KHz. Although SDM brings spurs, it can be seen that the phase noise performance with SDM is still better than the phase noise performance without SDM. With SDM, it is −116 dBc/Hz and −126 dBc/Hz at 1 MHz and 3 MHz frequency offset, respectively. Figure 8(c) shows the frequency spectrum of DCO at 3.34 GHz; it can be seen that SDM brings spurs about 10 dBc at point 3 and point 4 on the frequency spectrum of DCO, but it can be suppressed by the loop character of ADPLL. Figure 9 shows that the frequency and K_{DCO_C} change versus the coarse array code. The measured K_{DCO_C} is around 24 MHz/LSB with a maximum deviation of 1.64 MHz/LSB. Figure 10(a) displays the K_{DCO_M} at different frequency points, the red line and the blue line show the K_{DCO_M} at 3.32 GHz and 5.45 GHz, respectively, and K_{DCO_M} changes from 1.5 MHz/LSB to 7.4 MHz/LSB across the whole FTR because K_{DCO_M} is proportional to the cube of f_{CKV} as (2) shows. Figure 10(b) gives the K_{DCO_F} at different frequency points, and it changes from 120 KHz/LSB to 455 KHz/LSB through the whole FTR, with the same reason of K_{DCO_M}. After 10-bit SDM, fractional array's frequency resolution

K_{DCO_F} will be divided by 2^{10}, so the final frequency resolution varies from 117 Hz to 444 Hz, which is less than 0.1 ppm. When all the varactors change from on-state to off-state, the DCO will work from 3.22 GHz to 5.45 GHz, with the FTR of 51.5%.

Table 1 shows the comparison table of state-of-the-art LC-tank oscillators [2, 6–8]. Without the SDM, this DCO has achieved the frequency resolution of 120 KHz, which is close to other references, but it can be 117 Hz after SDM. Reference [8] is also a complementary Class-C DCO, but this work has better performance than it. Reference [6] is traditional LC-DCO; this work shows higher FoM than it due to its Class-C mode. This design works at close frequency with [6–8] while displaying wider FTR and better FoMT due to the design and optimization of capacitor arrays.

4. Conclusion

This paper presented a complementary Class-C digitally controlled oscillator (DCO) with differential transistor pairs. With three optimized capacitor arrays and a fractional array dithered by SDM, the DCO works from 3.22 GHz to 5.45 GHz with 51.5% FTR and less than 0.1 ppm frequency resolution. Through two feedback loops, the start-up oscillation is ensured and low power consumption is realized. The achieved phase noise is −126 dBc/Hz at 3 MHz offset from 5.054 GHz with the $1/f^3$ corner frequency of 260 KHz while consuming only 2.8 mA at 1.2 V voltage supply. The final FoM and FoMT are 185.2 dBc/Hz and 199.4 dBc/Hz, respectively.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

TABLE 1: Comparison with the state of the art.

	[2]	[6]	[7]	[8]	*This work*
Technology	40 nm	65 nm	16 nm	65 nm	*65 nm*
Freq. (GHz)	5.11	6.8	3.6	2.2	*5.054*
FTR (%)	64.6	20	22	9.1	*51.5*
Power (mW)	8	1	0.6	1.5	*3.4*
f_m (MHz)	1	3	10	3	*3*
PN@ f_m (dBc/Hz)	−130	−116	−134	−117	*−126*
Frequency resolution (Hz)	29 K	116 K	1.3 K	-	*120 K (wo SDM)/117 (wi SDM)*
FoM[1] (dBc/Hz)	187	183	188	173	*185.2*
FoMT[2] (dBc/Hz)	203	189	195	172	*199.4*

[1]$\text{FoM} = 10 \log_{10}((f_{\text{osc}}/f_m)^2 (1/P_{\text{DC}}(\text{mW}))) - \text{PN}$; [2]$\text{FoMT} = \text{FoM}^1 + 20 \log_{10}(\text{FTR}/10)$.

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