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Research Article

Modeling and Modulation of NNPC Four-Level Inverter for Solar Photovoltaic Power Plant

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Photovoltaic (PV) power plant is an attractive way of utilizing the solar energy. For high-power PV power plant, the multilevel inverter is of potential interest. In contrast to the neutral-point clamped (NPC) or flying capacitor (FC) multilevel inverter, the nested neutral point clamped (NNPC) four-level inverter has better features for solar photovoltaic power plant. In practical applications, the common mode voltage reduction of the NNPC four-level is one of the important issues. In order to solve the problem, a new modulation strategy is proposed to minimize the common mode voltage. Compared with the conventional solution, our proposal can reduce the common mode voltage to 1/18 of the DC bus voltage. Moreover, it has the capability to balance the capacitor voltages. Finally, we carried out time-domain simulations to test the performance of the NNPC four-level inverter.

1. Introduction

In recent years, the grid-connected wind and PV power systems have attracted considerable interests around the world [1–4]. Many industrialized nations have installed significant solar power capacity into their electrical grids, providing an alternative to conventional energy sources. While an increasing number of less developed nations have turned to solar to reduce dependence on expensive imported fuels. Different from most building-mounted and other domestic solar power applications which are mainly for the low-voltage local users [5, 6], the high voltage is necessary to integrate the solar photovoltaic power plant into utility. In this case, the multilevel inverters are of potential interest for PV plants [7–11]. In practice, however, there are leakage currents and EMC issues in high-power photovoltaic plants [12]. The leakage currents and electromagnetic interferences have potential safety problems [13, 14]. Therefore, it must be eliminated before connecting them into grid. For this aim, the solutions based on the interesting topologies and modulation strategies have been developed in recent years. Typically, there are three classical topologies of the multilevel inverters such as the flying capacitor (FC) topology, cascade H-bridge topology, and neutral point clamped (NPC) topology [15–18]. Compared with the conventional two-level inverter, the multilevel inverter has unique features such as reduced voltage stress, less dv/dt and high waveforms. In contrast to the existing topologies, a novel nested neutral point clamped (NNPC) inverter is proposed in [19], it is of great interest for medium-voltage power conversion, especially for solar PV plant applications. In practice, however, the common mode voltage may arise, resulting in the leakage current. In order to solve the problem, a new modulation strategy is proposed to minimize the common mode voltage. Compared with the conventional solution, our proposal can reduce the common mode voltage to 1/18 of the DC bus voltage. Meanwhile, it has the capacitor balancing capability. Finally, the time-domain performance tests are carried out. The results verify the effectiveness of the proposed solution.

2. Analysis of Four-Level NNPC Inverter

The schematic diagram of the novel four-level NNPC inverter is illustrated in Figure 1, where each phase includes 6 switches, 2 diodes, and 2 flying capacitors, which has fewer number of components and complexity than four-level NPC

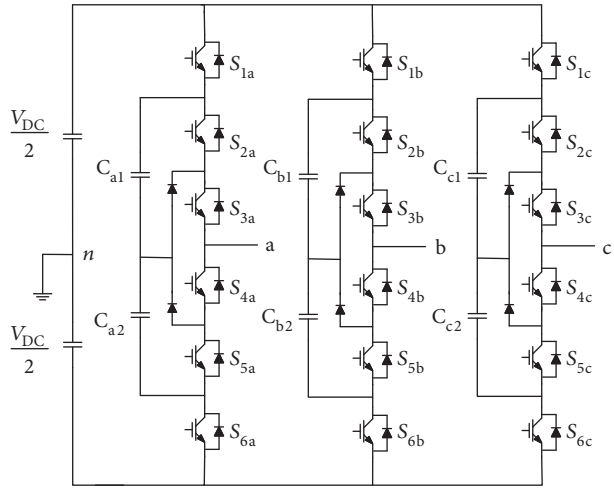


Figure 1: Schematic diagram of the four-level NNPC inverter.

Table 1: States, switching states, and flying capacitors voltage of four-level NNPC inverter.

Level		S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{5a}	S_{6a}	V_{Ca1}	V_{Ca2}	V_{an}
3		1	1	1	0	0	0	—	—	$V_{DC}/2$
2	2A	1	0	1	1	0	0	C ($i_a > 0$) D ($i_a < 0$)	—	$V_{DC}/6$
	2B	0	1	1	0	0	1	D ($i_a > 0$) C ($i_a < 0$)	D ($i_a > 0$) C ($i_a < 0$)	
1	1A	1	0	0	1	1	0	C ($i_a > 0$) D ($i_a < 0$)	C ($i_a > 0$) D ($i_a < 0$)	$-V_{DC}/6$
	1B	0	0	1	1	0	1	—	D ($i_a > 0$) C ($i_a < 0$)	
0		0	0	0	1	1	1	—	—	$-V_{DC}/2$

C: charging; D: discharging.

or FC inverter. Take phase A for example, there are six operation states of a phase, as shown in Table 1.

When the switch turns on, it corresponds to the state "1" in Table 1, while when the switch turns off, it corresponds to the state "0." The four levels of phase voltage are labeled as 3, 2, 1, and 0, which correspond to the topology of $V_{DC}/2$, $V_{DC}/6$, $-V_{DC}/6$, and $-V_{DC}/2$. Different from the conventional four-level NPC inverter, there are two kinds of redundant states on "1" and "2" levels of NNPC topology. "1" level corresponds to 1A and 1B, while "2" level corresponds to the 2A and 2B in Table 1. It should be noted that the flying capacitor is used in the NNPC inverter. So the capacitor voltage balancing should be considered. The impact of switching states on the capacitor voltage is shown in Table 1.

As shown in Figure 2, only the flying capacitor C_{a1} is charged or discharged during the state "2A," remaining the flying capacitor C_{a2} unaffected, while both the flying capacitors C_{a1} and C_{a2} will be charged or discharged during the state "2B." It is worth noting that if the current direction is different, the capacitor charging or discharging is also different. Take the state "2A" for example, when the current $i_a > 0$, the capacitor C_{a1} is charged, and while the current $i_a < 0$, the capacitor C_{a1} discharged. The details regarding the capacitor voltage balancing will be presented in the following section.

3. Common Mode Voltage of Four-Level NNPC Inverter

The common mode voltage is one of the important issues for power converters [20]. The common mode voltage of the NNCP inverter can be expressed as (1), where v_{cm} is the common voltage, and v_{an}, v_{bn}, and v_{cn} represent the three-phase voltages, respectively.

$$v_{cm} = \frac{v_{an} + v_{bn} + v_{cn}}{3}. \quad (1)$$

There are 4 switching states in each phase. So there are 64 switching states for NNPC inverter. The relationship between the common mode voltage and switching state is shown in Table 2. Taking "000" in Table 2 for example, it is indicated that the a phase output is 0 level, the b phase output is 0 level, and the c phase output is 0 level.

From Table 2, it can be observed that there are 10 kinds of values, including $\pm V_{DC}/2$, $\pm 7V_{DC}/18$, $\pm 5V_{DC}/18$, $\pm V_{DC}/6$,

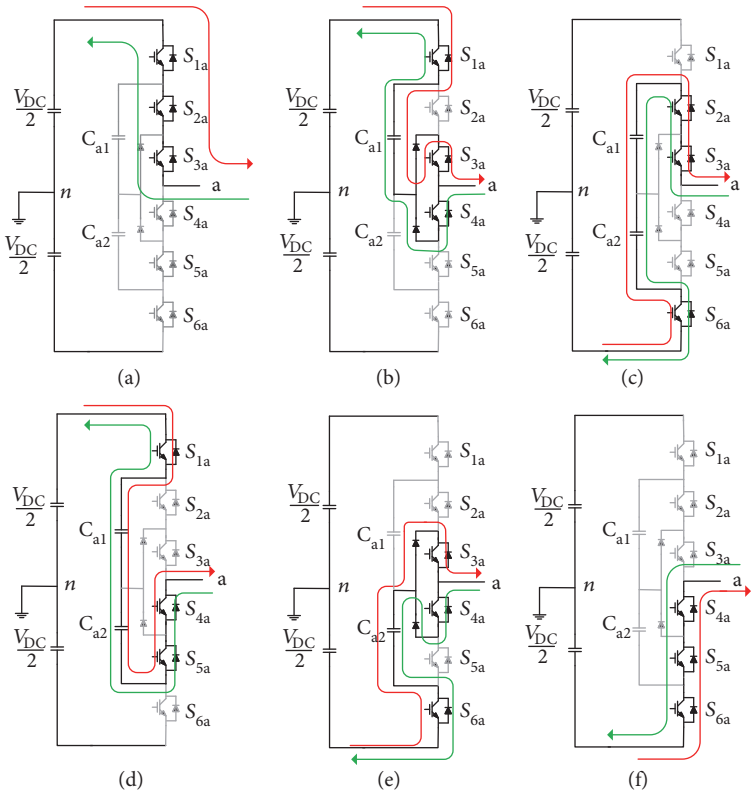


Figure 2: Six switching states of NNPC inverter: (a) switching state 3; (b) switching state 2A; (c) switching state 2B; (d) switching state 1A; (e) switching state 1B; and (f) switching state 0.

Table 2: Switching states and common mode voltage of four-level NNPC inverter.

Common mode voltage	Switch states
$-V_{DC}/2$	000
$-7\ V_{DC}/18$	001, 010, 100
$-5\ V_{DC}/18$	002, 011, 020, 101, 110, 200
$-V_{DC}/6$	003, 021, 012, 030, 102, 111, 120, 201, 210, 300
$-V_{DC}/18$	013, 022, 031, 103, 112, 121, 130, 202, 211, 220, 301, 310
$V_{DC}/18$	023, 032, 113, 122, 131, 203, 212, 221, 230, 302, 311, 320
$V_{DC}/6$	033, 123, 132, 213, 222, 231, 303, 312, 321, 330
$5\ V_{DC}\ 18$	133, 223, 232, 313, 322, 331,
$7\ V_{DC}/18$	233, 323, 332
$V_{DC}/2$	333

and $\pm V_{DC}/18$ regarding the common mode voltage of the NNPC inverter. Obviously, the common mode voltage would be very high if all switching states are involved. In order to reduce the common mode voltage, two groups of switching states can be utilized. In this way, the common mode voltage can be reduced to 1/18 of the DC bus voltage. The space vector diagram is as shown in Figure 3.

4. Proposed Modulation Strategy

As discussed above, the common mode voltage can be significantly reduced to $\pm V_{DC}/18$ by selecting the specified vectors and switching states. In order to achieve the objective, a new modulation strategy is proposed in this paper. Firstly, the desired level arrangement is generated by the modulation strategy. Secondly, select the redundant state to balance the flying capacitor voltage.

As shown in Figure 3, the vectors of the selected 24 switching states are similar to those of three-level vectors. If the outermost four-level vectors (e.g., 130 and 230) are not considered, the other four-level vectors are associated with the three-level vectors. Taking the sector of A1 as an example, the three-level vector of 000 in Figure 3(a) (redundant vectors 111 and 222) corresponds to the virtual vector (red cross presents the virtual vector) in Figure 3(b), while the three-level vector of 211 (redundant vectors 100) corresponds to the four-level vector of 211. Other relationship can also be derived, as shown in Table 3.

For the virtual vector, it can be achieved by vector synthesis. Taking the virtual vector of sector A1 for example, it can be synthesized through (1) vectors 221 and 310, (2) vectors 220 and 311, and (3) vectors 320 and 211. The vector synthesis diagram is shown in Figure 4.

Based on the above analysis, a novel modulation method is proposed in this paper. Firstly, comparing two triangle waves with sine wave, the three-level vectors can be

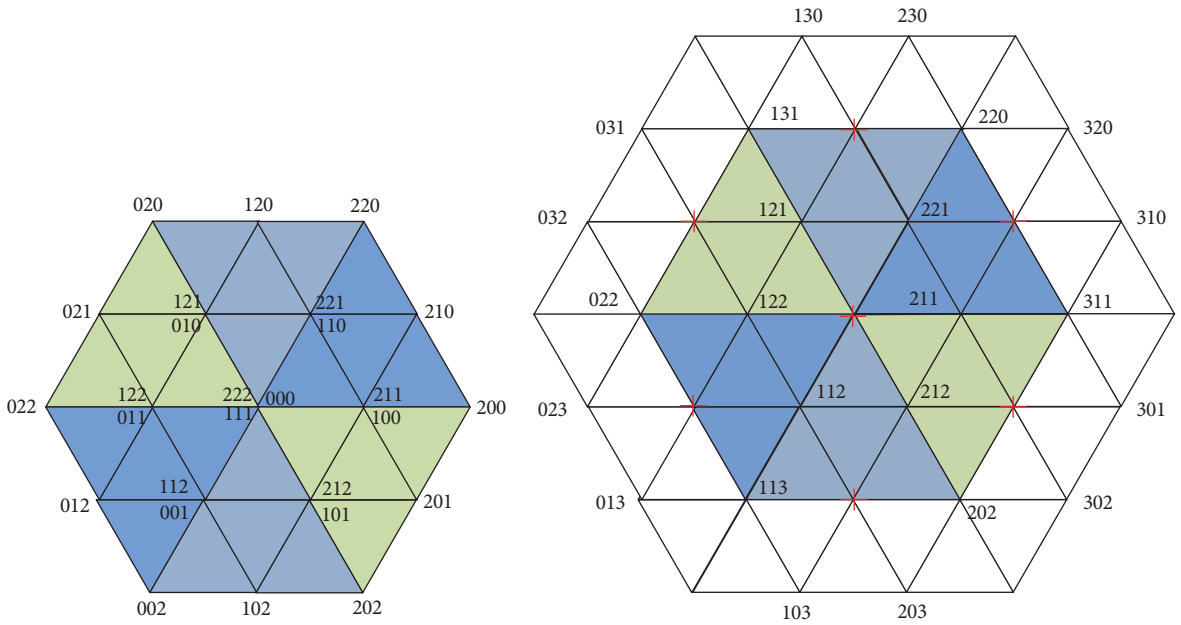


Figure 3: Space vector diagram (a) three-level inverter and (b) four-level inverter $v_{cm} = \pm V_{DC}/18$.

Table 3: Relationship between three-level inverter voltage vector and four-level inverter voltage vector.

Three-level vector	Four-level vector
211, 100	211
200	311
210	Virtual vector
221, 110	221
220	220
120	Virtual vector
121, 010	121
020	131
021	Virtual vector
122, 011	122
022	022
012	Virtual vector
112, 001	112
002	113
102	Virtual vector
212, 101	212
201	Virtual vector
202	202
000, 111, 222	Virtual vector

generated, as shown in Table 3. With the logical transformation, these vectors can be linked to the four-level vectors. The synthesis method is shown in Table 4.

For the selection of the carrier modulation, the in-phase disposition (IPD) modulation is used due to the following advantages.

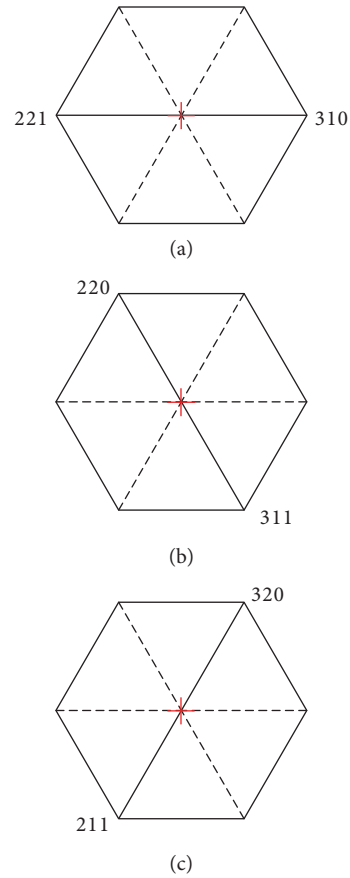


Figure 4: Virtual vector synthesis diagram.

Table 4: Relationship between virtual and synthesis vectors.

Virtual vector	Synthetic vector
210	Sector A1 ∩ B1 221 and 310
210	Sector A1 ∩ B2 211 and 320
120	Sector A2 ∩ B2 121 and 230
120	Sector A2 ∩ B3 221 and 130
021	Sector A3 ∩ B3 122 and 031
021	Sector A3 ∩ B4 121 and 032
012	Sector A4 ∩ B4 112 and 023
012	Sector A4 ∩ B5 122 and 013
102	Sector A5 ∩ B5 212 and 103
102	Sector A5 ∩ B6 112 and 203
201	Sector A6 ∩ B6 211 and 302
201	Sector A6 ∩ B1 212 and 301

(1) In IPD modulation, voltage vector complies with the "near three vector principle," that is, there no longer exists jumping of the two levels on the corresponding four-level vector.

(2) In the A1 sector, for example, in a switching period of IPD modulation, the vector 210 (i.e., three-level vector corresponding to the four-level virtual vector) has the same effect time in the first half and the second half switching periods. Therefore, it is easy to realize the vector synthesis in Table 4 (in the first Ts/2 with a synthetic vector, after Ts/2 with another synthetic vector).

As discussed above, the desired level can be generated by means of carrier modulation and logical transformation. Note that there are redundant states about "1" or "2" level (see Table 1) of the NNPC inverter. The capacitor voltage balance can be achieved with the redundant states. Taking one phase as an example, the variation of the flying capacitor voltage is defined as (2), where V_{ci} is the flying capacitor voltage, $i = 1, 2$. The capacitor voltage can be balanced if ΔV_{ci} is close to 0.

$$\Delta V_{ci} = V_{ci} - \frac{V_{DC}}{3} \tag{2}$$

The capacitor voltage balancing mechanism is shown in Table 5. The balance of the capacitor C_1 can be achieved only by selecting the redundancy state of "2" level, while the balance of the capacitor C_2 can be achieved by selecting the redundancy state of "1" level.

The control block diagram is shown in Figure 5. In this way, the output four-level voltage can be achieved. Meanwhile the common mode voltage can be significantly reduced to $\pm V_{DC}/18$. Aside from that, the capacitor voltage balancing can be achieved.

5. Simulation Results

In order to verify the effectiveness of the proposed solution, the time-domain simulations are carried out in MATLAB/Simulink. The type of simulation model we use is a real circuit with power switches, instead of a transfer function or mathematical description model. The simulation parameters are listed in Table 6.

Table 5: Mechanism of capacitor voltage balancing.

Level	ΔV_{Ci}	Phase current ia	Redundancy state
2	$\Delta V_{C1} < 0$	<0	2B
		≥ 0	2A
	$\Delta V_{C1} \geq 0$	<0	2A
		≥ 0	2B
1	$\Delta V_{C2} < 0$	<0	1B
		≥ 0	1A
	$\Delta V_{C2} \geq 0$	<0	1A
		≥ 0	1B

The simulation results are shown as follows. From Figures 6 and 7, it can be observed that the flying capacitor voltages can be well balanced around 2200 V ($V_{DC}/3$), and the ripple is less than 7.5% of the rated voltage. The output phase voltage is four-level waveform, while the line voltage is seven-level waveform. On the other hand, the common mode voltage of the conventional solution is as high as $\pm 5V_{DC}/18$, while the common mode voltage of the proposed solution is significantly reduced to $\pm V_{DC}/18$.

In order to verify the dynamic performance of the proposed solution, the simulations are carried out with a step change from half to full loads at 0.1 s. As shown in Figure 8, it can be seen that the current increases from half to full loads, and the waveform quality of current is kept well all the time. Note that the fluctuation of capacitor voltage after heavy loading increases, but it is still less than 7.5% of the rated voltage. So the system has a good dynamic performance. At the same time, the common mode voltage, before and after the load step, remains around $\pm V_{DC}/18$.

In order to further verify the effectiveness of the capacitor voltage balancing scheme, the balancing control is enabled, then disabled, and finally enabled, as shown in Figure 9.

From Figure 9, it can be observed that when the balancing control is disabled, the capacitor voltage tends to diverge. Meanwhile, the common mode voltage is negatively impacted with higher amplitude; that is, the capacitor voltage balancing has an impact on common mode voltage. After the balancing control is recovered at $t = 0.1$ s, common mode voltage and capacitor voltage can be quickly restored to normal operation state, which verifies the effectiveness of the proposed solution.

6. Conclusion

This paper has presented the modeling and analysis of a novel four-level NNPC inverter for PV power plant applications. It is concluded that the proposed solution can significantly reduce the common mode voltage to $V_{DC}/18$. Also, it can

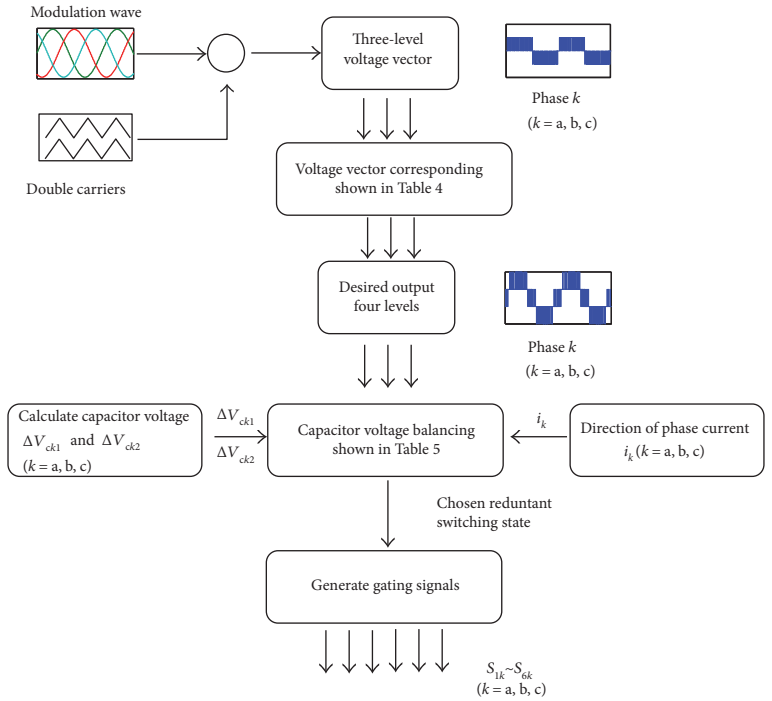
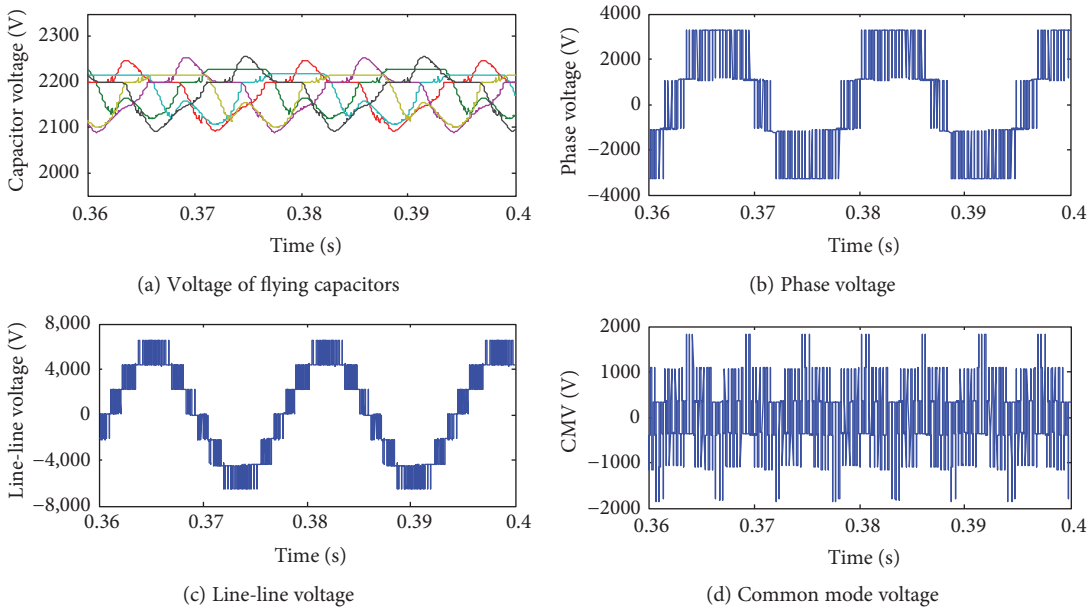


Figure 5: The controller diagram of the four-level NNPC inverter.

Table 6: Simulation parameters.

Parameters	Value
DC voltage	6.6 kV
Output frequency	60 Hz
Output inductor	5 mH
Output resistor	7.5 Ω
Flying capacitor	2200 μF
Modulation index	0.95



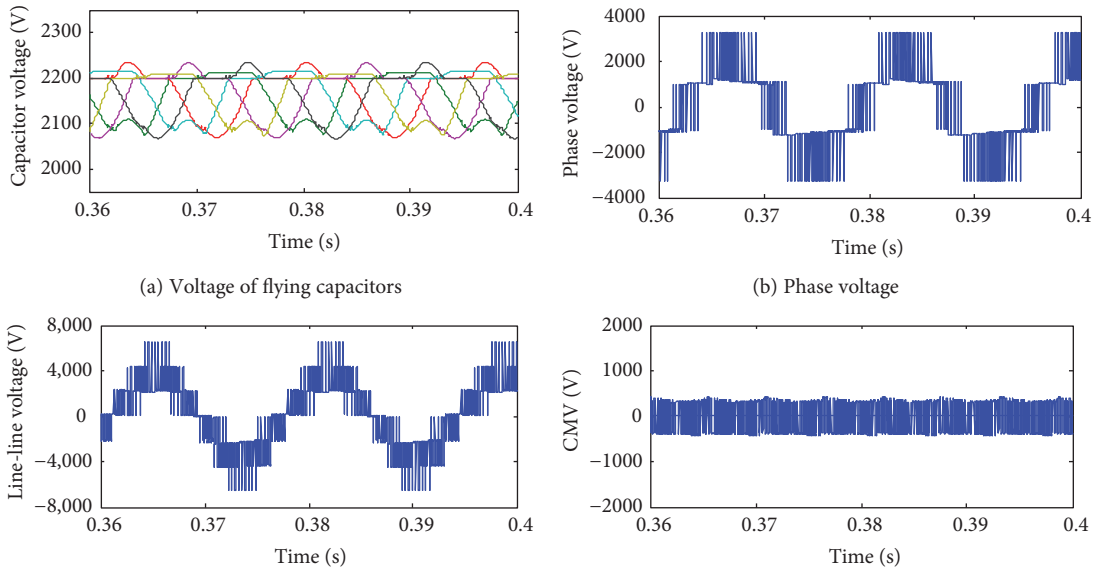
(a) Voltage of flying capacitors

(b) Phase voltage

(c) Line-line voltage

(d) Common mode voltage

Figure 6: Simulation results (conventional solution).



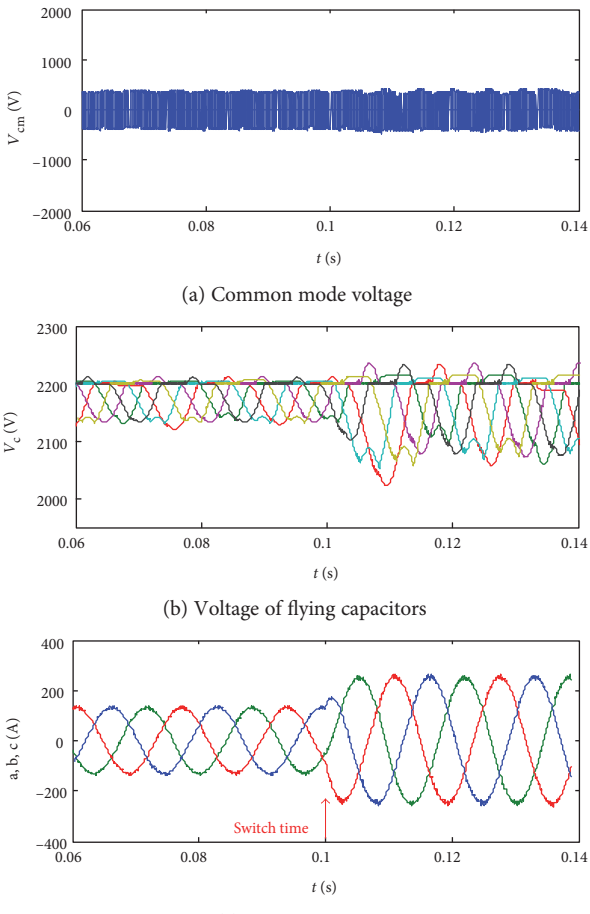
(a) Voltage of flying capacitors

(b) Phase voltage

(c) Line-line voltage

(d) Common mode voltage

Figure 7: Simulation results (proposed solution).

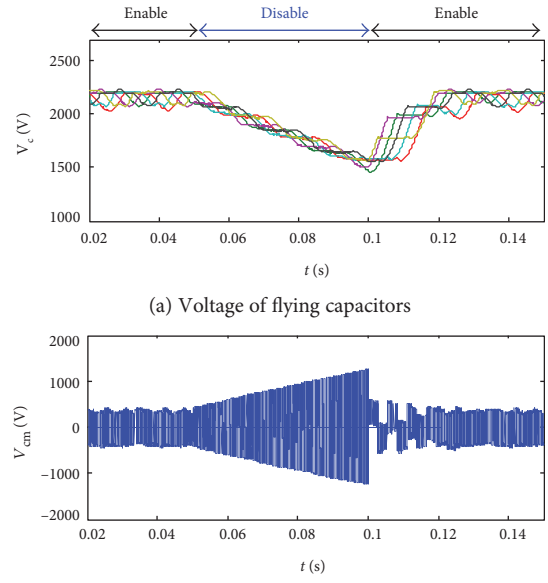


(a) Common mode voltage

(b) Voltage of flying capacitors

(c) Output current

Figure 8: Simulation results from half to full load.



(a) Voltage of flying capacitors

(b) Common mode voltage

Figure 9: Simulation results with and without capacitor balancing control.

achieve the capacitor voltage balancing. Different from the conventional solutions, the proposed one has advantages such as easy implementation with no need of complex space vector modulation. Therefore, it is of great potential interest for solar plant applications, where the common mode EMI is a major concern. It should be noted that the CMV and EMI reductions of the four-level NNPC inverter are focused for PV power plant. Other issues such as grid synchronization, control, and protection [21–26] are beyond the scope of the paper.

Conflicts of Interest

The authors declare that there is no conflict of interests regarding publication of this paper.

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