Hindawi Publishing Corporation
Journal of Sensors
Volume 2016, Article ID 5358963, 7 pages
http://dx.doi.org/10.1155/2016/5358963

Hindawi

Research Article

A Novel Differential Log-Companding Amplifier for Biosignal Sensing

Zigang Dong,[1,2] Xiaolin Zhou,[1,2] and Yuanting Zhang[1,2,3]

[1]*Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, 1068 Xueyuan Road, Xili, Nanshan, Shenzhen, Guangdong 518055, China*
[2]*Key Laboratory for Health Informatics of the Chinese Academy of Sciences (HICAS), 1068 Xueyuan Road, Xili, Nanshan, Shenzhen, Guangdong 518055, China*
[3]*Department of Electronic Engineering, The Chinese University of Hong Kong, Shatin, Hong Kong*

Correspondence should be addressed to Xiaolin Zhou; xl.zhou@siat.ac.cn

Received 23 May 2016; Accepted 31 July 2016

Academic Editor: Stephane Evoy

We proposed a new method for designing the CMOS differential log-companding amplifier which achieves significant improvements in linearity, common-mode rejection ratio (CMRR), and output range. With the new nonlinear function used in the log-companding technology, this proposed amplifier has a very small total harmonic distortion (THD) and simultaneously a wide output current range. Furthermore, a differential structure with conventionally symmetrical configuration has been adopted in this novel method in order to obtain a high CMRR. Because all transistors in this amplifier operate in the weak inversion, the supply voltage and the total power consumption are significantly reduced. The novel log-companding amplifier was designed using a 0.18 μm CMOS technology. Improvements in THD, output current range, noise, and CMRR are verified using simulation data. The proposed amplifier operates from a 0.8 V supply voltage, shows a 6.3 μA maximum output current range, and has a 6 μW power consumption. The THD is less than 0.03%, the CMRR of this circuit is 74 dB, and the input referred current noise density is 166.1 fA/$\sqrt{\text{Hz}}$. This new method is suitable for biomedical applications such as electrocardiogram (ECG) signal acquisition.

1. Introduction

In recent years, portable and wearable personal healthcare devices have become more and more popular in the world. For these kinds of devices, the biomedical signal acquisition is an important part. The analog amplifier is one of the key building blocks to the signal acquisition unit. Therefore, several requirements such as low power, low noise, low voltage, high total harmonic distortion (THD), and high common-mode rejection ratio (CMRR) are imposed on the amplifier in the biomedical applications. The log-companding technique [1, 2] is a new tool to reduce the amplifier's supply voltage, the internal voltage dynamic range (DR), and the power consumptions. It is also a good method to solve the trade-off between increasing the signal dynamic range and decreasing the supply voltage [3]. This technique, indeed, provides a practical solution for biomedical applications for its property of low power consumption, especially for the portable and wearable medical devices.

For the log-companding technique, the input signal firstly needs to be compressed from the current domain to the voltage domain by logarithmic (log) law. Then, a nonlinear signal processing can be done in the voltage domain. Finally, the processed signal is expanded back to the linear current domain from voltage domain to realize an external linear amplification. The log-companding technique is realized with MOS transistors biased in the subthreshold region for their exponential current versus voltage characteristics which consume very low power.

However, this technique has its limitations. For example, the output current range and the signal linearity are difficult to improve because of the property of MOS transistor operating in the weak inversion. To reduce the distortion, the transistors are biased with low currents which will limit

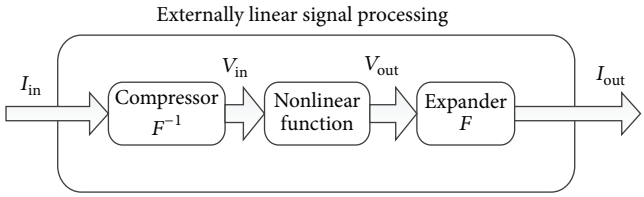

FIGURE 1: Diagram of log-companding technique.

the input and output current swings and reduce the signal-to-noise ratio (SNR). Although the biased currents can be improved by enhancing the widths of the transistors, it will increase the power consumption and induce a large parasitic capacitance. Because the differential operation of the conventional differential log-companding amplifier is operating in the current domain [4–7], it is not very effective in improving CMRR and THD for the log-companding technique.

In this paper, a novel method is proposed to improve the performance in linearity, CMRR, and low power of the log-companding amplifier by exploiting a nonlinear function and introducing a new differential stage. This method realizes the differential operation between the input signals in the log and linear domains, which is more effective in eliminating the common-mode input signal. A novel nonlinear function is employed to improve the system linearity and extend the output linear range. This paper is organized as follows: the log-companding design technique will be introduced in Section 2. In Section 3, the novel log-companding amplifier will be presented. The simulation results will be listed in Section 4, and Section 5 includes the conclusion.

2. Log-Companding Design Techniques

2.1. Basics of Log-Companding Techniques. For the expanding technique, the input signal in current domain is firstly compressed to voltage domain. Then, a nonlinear process is performed in the voltage domain. Finally, the processed signal is expanded back to the current domain to ensure an external linear function with the input signal. The block diagram of log-companding technique is shown in Figure 1 [8].

As shown in Figure 1, the log-companding technique includes three basic building blocks: I-V compressor F^{-1}, nonlinear function, and V-I expander F. Compressor F^{-1} and expander F are used to perform log-compression and log-expansion, respectively, by using a MOS transistor biased in weak inversion region which exactly gives the logarithmic function.

According to the EKV model [9], I-V function of a NMOS transistor can be expressed as follows:

$$I_D = I_S\left(\frac{W}{L}\right)\ln^2\left(1+e^{(V_{GB}-V_{TON}-nV_{SB})/2nU_t}\right) - I_S\left(\frac{W}{L}\right)\ln^2\left(1+e^{(V_{GB}-V_{TON}-nV_{DB})/2nU_t}\right) \quad (1)$$

$$I_S = 2n\beta U_t^2,$$

where I_S, n, β, V_{TON}, and U_t stand for the specific current, subthreshold slope, current factor, threshold voltage, and thermal potential, respectively. V_{GB}, V_{DB}, and V_{SB} are the gate-bulk, drain-bulk, and source-bulk voltage difference, respectively. MOS transistors can operate in three main operating regions which are called weak inversion, moderate inversion, and strong inversion, respectively. Each operating region can be further categorized into three saturation regions which can be called conduction, forward, and reverse saturation, respectively. Under these conditions, I-V (1) can be simplified as follows:

$$I_D = I_S\left(\frac{W}{L}\right)e^{(V_{GB}-V_{TON})/nU_t}e^{-V_{SB}/U_t} \quad (2)$$

(in weak inversion and forward saturation) and

$$I_D = I_S\left(\frac{W}{L}\right)e^{(V_{GB}-V_{TON})/nU_t}\left(e^{-V_{SB}/U_t}-e^{-V_{DB}/U_t}\right) \quad (3)$$

(in moderate inversion and conduction saturation).

In the conventional log-companding amplifier, all MOS transistors are biased in weak forward inversion such as in the blocks of compressor F^{-1} and expander F shown in Figure 1, since it exactly gives the logarithmic function. Moreover, the compressor and expander functions are two reciprocal functions to ensure external linear amplification.

For the PMOS operating in moderate conduction and weak forward inversion, I-V functions are depicted as follows:

$$I_D = I_S\left(\frac{W}{L}\right)e^{(-V_{GB}-V_{TOP})/nU_t}\left(e^{V_{SB}/U_t}-e^{V_{DB}/U_t}\right) \quad (4)$$

(in moderate inversion and conduction saturation) and

$$I_D = I_S\left(\frac{W}{L}\right)e^{(-V_{GB}-V_{TOP})/nU_t}e^{V_{SB}/U_t} \quad (5)$$

(in weak inversion and forward saturation).

2.2. Conventional Log-Companding Amplifiers. The main purpose of every amplifier is to obtain a linearly scaled copy of the input signal at the output port. In other words, the input signal is multiplied by a gain factor to yield the output signal. For the log-companding amplifier, however, this step is accomplished by adding a gain factor to the compression signal in the log region that is translated from the input signal by the log law, which corresponds to the part of nonlinear function in Figure 1. The general CMOS implementation of the log-companding amplifier topology is shown in Figure 2 [3].

3. Novel Log-Companding Amplifier

The proposed differential log-companding amplifier consists of four main parts including a compressor, a differentiator, a

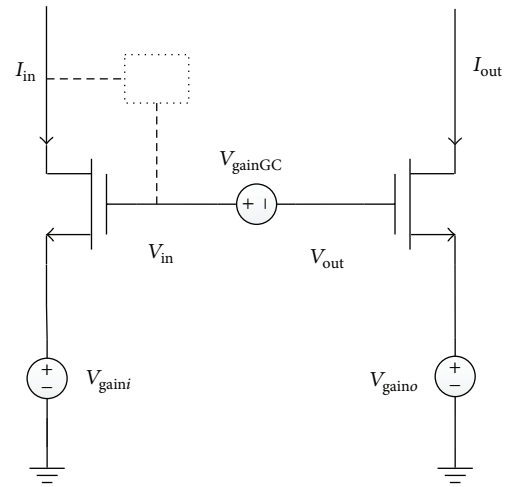

Figure 2: The general log-companding amplifier topology (auxiliary circuitry in dashed line).

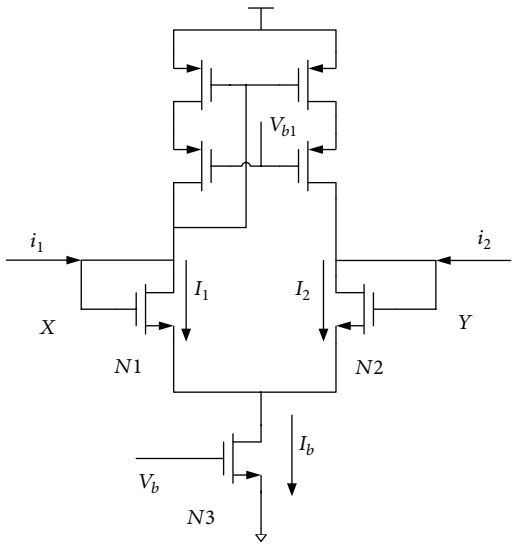

Figure 3: The diagram of compressor.

processor, and an expander [10]. The compressor is employed to logarithmically compress the input current signal into voltage signal. The differentiator is used to compare the difference between the two input current signals in voltage domain; the processer will process the nonlinear signal to improve the CMRR and THD. The expander will convert the voltage signal back to the current signal using log law to maintain external linear amplification.

3.1. Compressor. The compressor is shown in Figure 3, where i_1 and i_2 are the input current. All of the MOS transistors in this schematic are biased in weak forward saturation. From (2) and Figure 4, we can get the following:

$$I_1 - I_2 = i_1 - i_2$$

$$I_1 + I_2 = I_b = I_s \left(\frac{W}{L}\right)_{N3} e^{(V_b - V_{TON})/nU_t}$$

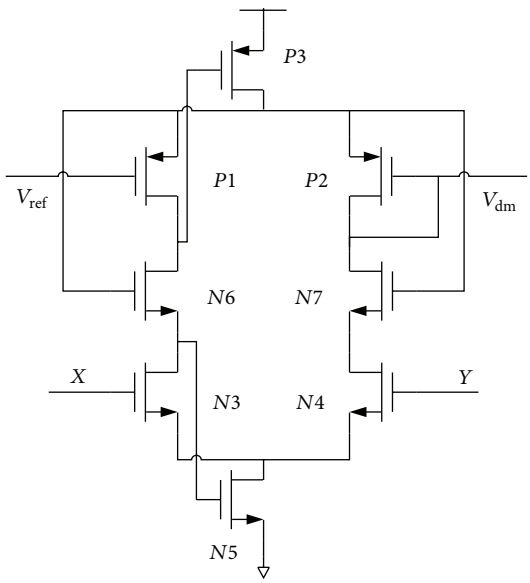

Figure 4: The diagram of differentiator.

$$I_1 = I_s \left(\frac{W}{L}\right)_{N1} e^{(V_{XB} - V_{TON})/nU_t} e^{-V_{SB}/nU_t}$$

$$I_2 = I_s \left(\frac{W}{L}\right)_{N2} e^{(V_{YB} - V_{TON})/nU_t} e^{-V_{SB}/nU_t}$$

$$\frac{I_1 - I_2}{I_1 + I_2} = \frac{i_1 - i_2}{I_b} = \frac{I_1/I_2 - 1}{I_1/I_2 + 1} = \frac{e^{V_{XY}/nU_t} - 1}{e^{V_{XY}/nU_t} + 1} = \tanh\left(\frac{V_{XY}}{2nU_t}\right). \tag{6}$$

Therefore,

$$i_1 - i_2 = I_b \tanh\left(\frac{V_{XY}}{2nU_t}\right), \tag{7}$$

where I_b is the quiescent operating current which will fix the input circuit operating point and control the amplifier's gain by tuning its value.

3.2. Differentiator. As shown in Figure 4, V_{ref} is a biased voltage that is provided by the biased circuit (it is not shown in this paper) to bias the MOS $P1$, $P7$ in weak forward inversion. V_{dm} is the output of differentiator.

Suppose that the MOS transistors are biased in weak forward inversion; recalling (2) and (5), we can get

$$V_{XY} = V_{dm} - V_{ref} \tag{8}$$

$$i_1 - i_2 = I_b \tanh\left(\frac{V_{dm} - V_{ref}}{2nU_t}\right). \tag{9}$$

The differentiator plays an important role in getting a high CMRR since the differential operation in the voltage domain.

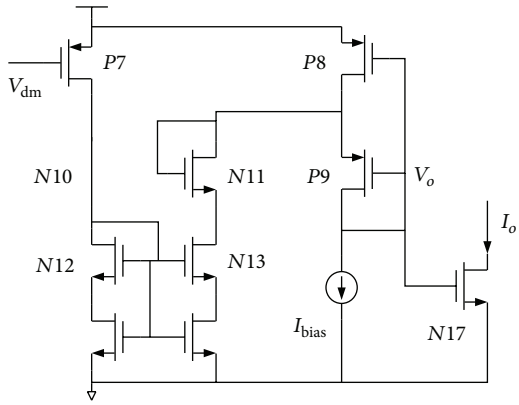

Figure 5: The diagram convertor and expander.

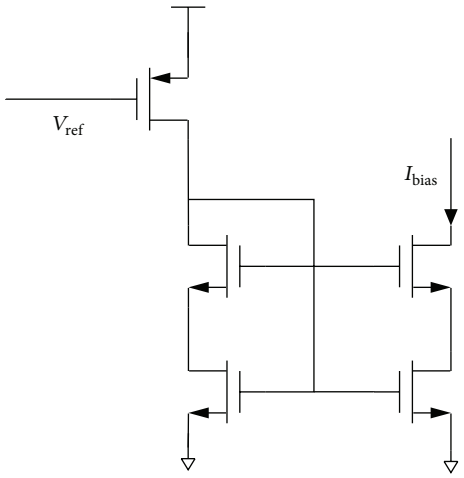

Figure 6: The current bias.

3.3. Nonlinear Convertor and Expander. The basic nonlinear processor is shown in Figure 6. The circuit converts the input signal V_{dm} from voltage domain to current domain by MOS $P7$ for conveniently tuning the signal. The current mirror involves two pairs of composite MOS transistors $N12$ and $N13$, respectively. MOS transistors $P8$, $P9$, and $N16$ expand the current signal back to voltage domain and complete signal V_{dm} nonlinear conversion to ensure linear amplification.

Suppose that $P8$ operates in weak forward saturation and the others in Figure 5 operate in weak inversion; according to (5), the drain current of $P7$ can be written as

$$I = I_s \left(\frac{W}{L}\right)_{P7} e^{(-V_{dB}+V_{TOP})/nU_t}, \tag{10}$$

where

$$V_B = V_{DD}. \tag{11}$$

According to (4) and (5) and assuming that the supply voltage is enough to saturate transistor $P9$, the current and voltage expressions of $P8$ and $P9$ can be given by

$$I_{bias} = I_s \left(\frac{W}{L}\right)_{P9} e^{(-V_{OB}+V_{TOP})/nU_t} e^{V_{SB}/nU_t} \tag{12}$$

$$I_{bias} + I = I_s \left(\frac{W}{L}\right)_{P8} e^{(-V_{OB}+V_{TOP})/nU_t} \left[1 - e^{V_{SB}/nU_t}\right]. \tag{13}$$

From (10)–(13), we can get

$$\left(1 + \frac{(W/L)_{P8}}{(W/L)_{P9}}\right) I_{bias} + I_s \left(\frac{W}{L}\right)_{P7} e^{(-V_{dB}+V_{TOP})/nU_t} = I_s \left(\frac{W}{L}\right)_{P8} e^{(-V_{OB}+V_{TOP})/nU_t}. \tag{14}$$

Multiply e^{V_{ref}/nU_t} by both sides of (14), rearranged to give

$$I_s \left(\frac{W}{L}\right)_{P8} e^{(V_{ref}-V_O)/nU_t} - I_s \left(\frac{W}{L}\right)_{P7} e^{(V_{ref}-V_{dm})/nU_t} = \left(1 + \frac{(W/L)_{P8}}{(W/L)_{P9}}\right) I_{bias} e^{-(V_{DD}+V_{TOP}-V_{ref})/nU_t}. \tag{15}$$

Let

$$M = \frac{\left(1 + (W/L)_{P8} / (W/L)_{P9}\right) I_{bias}}{I_s} e^{-(V_{DD}+V_{TOP}-V_{ref})/nU_t}. \tag{16}$$

Equation (15) can be written as

$$e^{(V_{dm}-V_{ref})/nU_t} = \frac{\left((W/L)_{P7} / (W/L)_{P8}\right) e^{(V_O-V_{ref})/nU_t}}{1 - \left(M / (W/L)_{P8}\right) e^{(V_O-V_{ref})/nU_t}}. \tag{17}$$

Then, let us take a look at the following function:

$$e^{2x} = \frac{f}{1-f}. \tag{18}$$

Solving (18) for f, this yields

$$f = \tanh(x) + \frac{1}{e^{2x}+1}. \tag{19}$$

In most practical cases, the second term of the right hand of (19) is much less than the first. For example, if $n = 1.2$, $U_t = 26$ mv, $V_{dm} = 0$, $V_{ref} = 400$ mv, calculated to give

$$\Delta = \frac{1}{e^{(V_{ref}-V_{dm})/nU_t}+1} \approx 2.7 \times 10^{-6}. \tag{20}$$

For this reason, assuming that

$$M = \left(\frac{W}{L}\right)_{P7} \tag{21}$$

and combining (9), (17), (18), and (19), we find

$$i_1 - i_2 = I_b \frac{(W/L)_{P7}}{(W/L)_{P8}} e^{(V_O-V_{ref})/nU_t}. \tag{22}$$

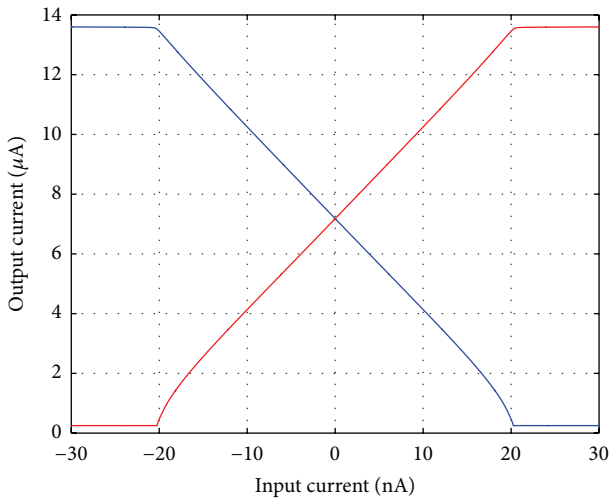

Figure 7: The output current curve with a varied input current.

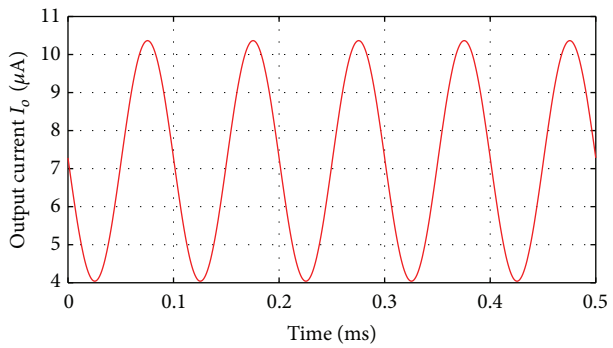

Figure 8: Transient response of output current of the amplifier.

From (2) and (22), the output current is given by

$$i_o = \frac{(W/L)_{P8}\,(W/L)_{N17}}{(W/L)_{P7}\,(W/L)_{N3}} e^{(V_{\text{ref}}-V_b)/nU_t}\,(i_1 - i_2)\,. \tag{23}$$

Recalling (16) and (21), the biasing current can be expressed as

$$I_{\text{bias}} = I_s \frac{(W/L)_{P7}\,(W/L)_{P9}}{(W/L)_{P8} + (W/L)_{P9}} e^{(V_{\text{DD}}+V_{\text{TOP}}-V_{\text{ref}})/nU_t}, \tag{24}$$

where I_{bias} is implemented as shown in Figure 6.

Although the derivation of (23) is based on the assumption that all MOS transistors operate in weak forward inversion, it can also keep the performance of the proposed amplifier when $P7$, $P8$, and $P9$ operate in moderate inversion.

4. Simulation Results

The differential log-companding amplifier is designed in a standard 0.18 μm CMOS technology. The supply voltage is 0.8 V and the bias voltage V_b is 320 mv. Note that the amplifier's gain can be controlled by voltage V_b. Because all the aforementioned deductions are based on the EKV model,

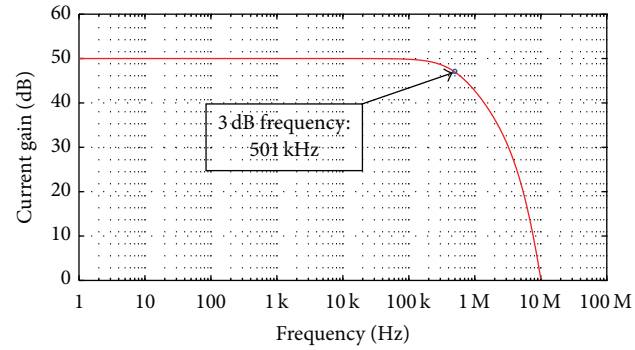

Figure 9: Frequency response of the amplifier.

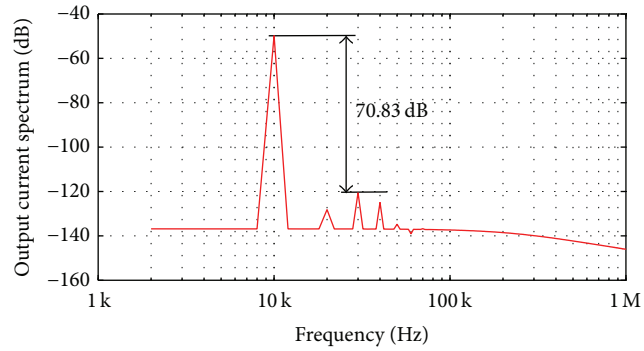

Figure 10: The distribution of THD with respect to the gain current.

Table 1: The corner simulation results.

	Typical	Worst case	Best case
MOS model	Typical	Fast	Slow
Temperature (°C)	27	0	80
Voltage supply (V)	0.8	0.8	0.8
Open loop gain (dB)	50	51.7	46.8
3 dB frequency (kHz)	510	340	850
Maximum input range (nApp)	20	10	46
Maximum output swing (μApp)	6.3	2.58	10
THD@maximum output swing (%)	0.028	0.056	0.03
CMRR (dB)	73	77.8	64.2

the design adopts the EKV model from the foundry in the following simulations to verify the analytical conclusions.

The output current changes from 0.23 μA to 13.6 μA when the input current varies from −20 nA to 20 nA as shown in Figure 7. The transient response of the output current is shown in Figure 8 with a sinusoidal input signal of 10 kHz frequency and 20 nApp peak-to-peak amplitude. Figure 9 shows the frequency response of the amplifier. The CMRR of log-companding amplifier is up to 73 dB using two stages of the differential structures shown in Figures 3 and 4. The THD of the proposed circuit is less than 0.03% at the maximum output as illustrated in Figure 10.

Considering that THD and CMRR are influenced by the device mismatch, the result of Monte Carlo simulation is provided as shown in Figure 11. THD is more than 80 dB and

Table 2: Performance comparison with other works.

	This work	[11]	[4]	[8]
Technology	0.18 μm CMOS	0.18 μm CMOS	0.25 μm CMOS	—
Topology	Current mode	Current mode	Current mode	Current mode
Supply voltage (V)	0.8	1	0.6	1
Open gain (dB)	50 dB	44.5/50/55.9	−40 to 38	−40 to +40
Bandwidth (Hz)	510 k	0.3~1 k~10 k	200 k	—
Input referred noise density (fA/sqrt (Hz))	166.1 fA (@10 kHz)	153 fA (@10 kHz)	—	—
Maximum input current (nApp)	20	20	—	—
Input dynamic range (dB)	92.9	53.29	—	—
Power consumption (μW)	6	13	3.16	25
CMRR (dB)	74	—	35.76	—
THD@maximum input (%)	0.0287@50 dB	1.03	0.55	0.6

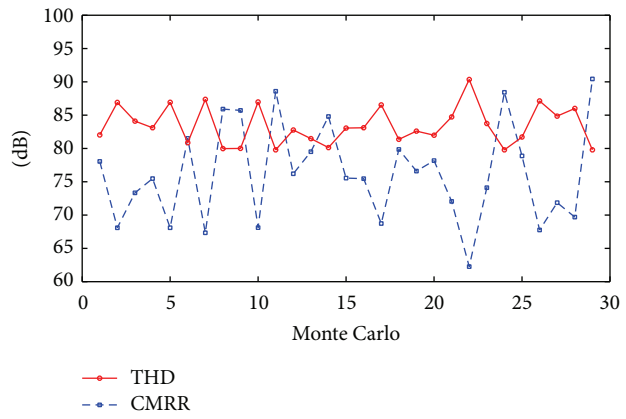

Figure 11: The Monte Carlo simulation.

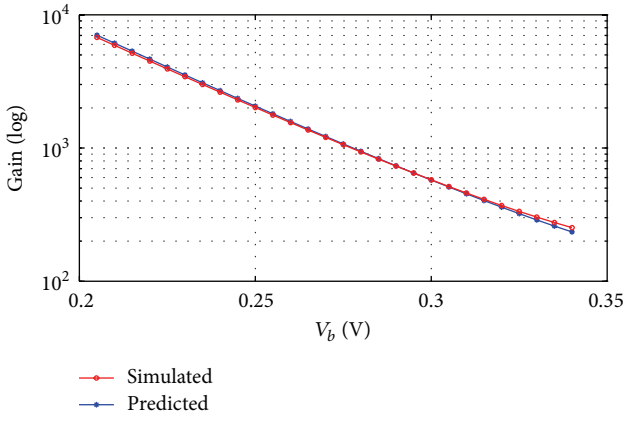

Figure 12: The amplifier gain curve with a varied V_b.

has a satisfactory result, CMRR is almost more than 72 dB and a very few points degrade. Figure 12 gives the comparison between the simulated gains and the predicted gain according to (24). The figure shows a good estimation.

The corner simulation results are shown in Table 1, which exhibit a good capability of operating in the real circumstance. Three corner simulations are different in temperature and same in voltage supply. Open loop gains vary only 5 dB in the range of different corners. 3 dB frequency has poor value in the worst case but it is acceptable for biosignal sensing application. They all have a good performance in THD and CMRR.

Table 2 displays the performance comparison with other design methods. They employed the same current-mode topology and work below the voltage supply 1 V. This work has the least power consumption only 6 μW and the best input dynamic range 92.9 dB. The proposed amplifier in this paper shows the lowest THD and the highest CMRR. Furthermore, it also shows excellent performance in low supply voltage and low power consumption.

5. Conclusions

A novel high linearity, low power, and high CMRR differential log-companding amplifier is introduced in this work. The amplifier is designed in a standard 0.18 μm CMOS technology with excellent linearity, high CMRR, and low power consumption. With the new nonlinear function used in the log-companding technology, the proposed amplifier has a very small THD and simultaneously a wide output current range. Furthermore, a differential structure with conventionally symmetrical configuration has been adopted in the novel method in order to obtain a high CMRR. The voltage supply is 0.8 V, the power consumption is 6 μW, and the THD is less than 0.03% at the maximum input. The CMRR of this circuit is 74 dB and the input referred current noise density is 166.1 fA/$\sqrt{\text{Hz}}$. It can be used in biomedical signal processing to decrease total power consumption, to ensure the signal linearity, and to eliminate common-mode noise. In conclusion, this technique can be used to design log-companding amplifier for many portable and wearable personal healthcare applications.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this article.

Acknowledgments

This study was funded by the National Basic Research Program 973 (no. 2010CB732606), National High-Tech R&D Program of China (863 Program, no. SS2015AA020109), the National Natural Science Foundation of China (no. 61401453), the STS Key Health Program of Chinese Academy of Sciences (nos. KFJEW-STS-097 and KFJ-EW-STS-095), the Guangdong Innovation Research Team Fund for Low-Cost Healthcare Technologies in China, the External Cooperation Program of Chinese Academy of Sciences (no. GJHZ1212), Guangdong Science and Technology Project for Application Research and Development (no. 2015B010129012), the Key Lab for Health Informatics of Chinese Academy of Sciences, the Peacock Program to Attract Overseas High-Caliber Talents to Shenzhen, and Shenzhen Municipal Government (nos. CXZZ20150504145109589, JCYJ20150630114942270, JCYJ20140417113430655, and JCYJ20140417113430619).

References

[1] Y. Tsividis, "Externally linear, time-invariant systems and their application to companding signal processors," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 2, pp. 65–85, 1997.

[2] R. W. Adams, "Filtering in the log domain," in *Proceedings of the 63rd AES Conference*, New York, NY, USA, May 1979.

[3] F. Serra-Graells and J. L. Huertas, "Low-voltage CMOS subthreshold log-domain filtering," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 10, pp. 2090–2100, 2005.

[4] K. Opasjumruskit and A. W. E. Leelarasamee, *A Design of CMOS Class-AB Differential Log-Companding Amplifier*, 2007.

[5] A. Gerosa, A. Maniero, and A. Neviani, "A fully integrated dual-channel log-domain programmable preamplifier and filter for an implantable cardiac pacemaker," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 10, pp. 1916–1925, 2004.

[6] M. A. Shaheen, A. A. Hamoui, and Y. Savaria, "A current-output DAC for low-power low-noise log-domain ΔΣ modulators," in *Proceedings of the IEEE 12th International New Circuits and Systems Conference (NEWCAS '14)*, pp. 281–284, Trois-Rivieres, Canada, June 2014.

[7] R. Groza and M. Cirlugea, "Current-mode log-domain programmable gain amplifier," in *Proceedings of the 2014 19th IEEE International Conference on Automation, Quality and Testing, Robotics (AQTR '14)*, pp. 1–4, Cluj-Napoca, Romania, May 2014.

[8] F. Serra-Graells, J. L. Huertas, and A. Rueda, *Low-Voltage CMOS Log Companding Analog Design*, Kluwer Academic, New York, NY, USA, 2003.

[9] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, 1995.

[10] G. Yang, R. F. Lyon, and E. M. Drakakis, "A 6 μ W per channel analog biomimetic cochlear implant processor filterbank architecture with across channels AGC," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 1, pp. 72–86, 2015.

[11] C.-Y. Wu, W.-M. Chen, and L.-T. Kuo, "A CMOS power-efficient low-noise current-mode front-end amplifier for neural signal recording," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 2, pp. 107–114, 2013.