Hindawi Publishing Corporation
Advances in Materials Science and Engineering
Volume 2014, Article ID 497274, 6 pages
http://dx.doi.org/10.1155/2014/497274

Hindawi

Research Article

Study of Interface Charge Densities for ZrO_2 and HfO_2 Based Metal-Oxide-Semiconductor Devices

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Received 25 March 2014; Revised 18 July 2014; Accepted 1 August 2014; Published 20 August 2014

Academic Editor: Maria A. Loi

A thickness-dependent interfacial distribution of oxide charges for thin metal oxide semiconductor (MOS) structures using high-k materials ZrO_2 and HfO_2 has been methodically investigated. The interface charge densities are analyzed using capacitance-voltage (C-V) method and also conductance (G-V) method. It indicates that, by reducing the effective oxide thickness (EOT), the interface charge densities (D_{it}) increases linearly. For the same EOT, D_{it} has been found for the materials to be of the order of 10^{12} cm^{-2} eV^{-1} and it is originated to be in good agreement with published fabrication results at p-type doping level of 1×10^{17} cm^{-3}. Numerical calculations and solutions are performed by MATLAB and device simulation is done by ATLAS.

1. Introduction

A MOS device is generally fabricated by oxidizing a Si substrate and depositing a conducting film on the resulting amorphous SiO_2 layer, forming the gate. The fabrication process always introduces defects at the SiO_2-Si boundary that critically affects the device characteristics of both the diode and the transistor. Increasing the size of wafer and decreasing the size of device, that is device scaling, are sensible approaches to reduce the cost. According to International Technology Roadmap for Semiconductor (ITRS), the next generation Si-based MOS device will require oxide with thickness ~1 nm. With the ever-increasing requirement for speed and density of silicon integrated circuits (ICs), MOS device scaling has become a primary concern of the semiconductor manufacturing industry. But there are some essential scaling limits with the ultrathin oxide. The leakage current (tunneling current) increases exponentially with the reduction of gate insulator thickness that in turn results in intolerable power consumption and device performance problems. As a result, the scaling limit of SiO_2 depends on both the elementary physics and accessible technology. It has been aimed towards achieving higher speed, lower power, lower cost, and higher density. Since the scaling of MOS devices utilizing SiO_2 as gate material has reached its limit, there is a prospect in thinning the electrical oxide thickness by using high-k dielectric material and/or metal gates to achieve a greater physical thickness and thus reducing the direct tunneling current while retaining a low oxide thickness [1–4]. Several insulator materials of gate in the lanthanum group exhibiting higher dielectric constant as shown in Table 1, in the range of 7–30, have been proposed as prospective candidates for gate dielectric and show outstanding results.

There are many requirements that need to be satisfied before a new material is acceptable to the semiconductor industry for its use as gate dielectric. Though high-k dielectric materials look very promising, there are certain challenges and issues that have to be met before successful transition from SiO_2 to high-k. The key guidelines for selecting an alternative dielectric are permittivity, band gap, band alignment to Si, thermal stability, film morphology, interface quality, compatibility with the current or expected materials to be used in processing for MOS devices, process compatibility, and reliability. In attempt to replace conventional SiO_2 with new high-k materials, HfO_2 and ZrO_2 have received

Table 1: Properties of high-k dielectric materials.

Material	k	Band gap, E_g (eV)	Band offset to Si (eV)	Crystal structure
SiO_2	3.9	9	3.5	Amorphous
Si_3N_4	7	5.3	2.4	Amorphous
Al_2O_3	9.3	8.8	2.8	Amorphous
$HfSiO_4$	15	6	1.5	Amorphous
Y_2O_3	15	6	2.3	Cubic
$ZrSiO_4$	15	6	1.5	Amorphous
HfO_2	22	6	1.5	Monoclinic, tetragonal
ZrO_2	22	5.8	1.4	Monoclinic, tetragonal
Ta_2O_5	26	4.4	0.3	Orthorhombic
La_2O_3	30	6	2.3	Hexagonal, cubic

tremendous attention and are quite promising materials [5–8] considering their permittivity and conduction band offsets values.

High-k materials often suffer from poor electrical quality of the oxide dielectric-semiconductor interface and are often associated with lower dielectric breakdown voltages and decreased lifetimes. Moreover, with the introduction of high-k materials there occurs formation of interface charges. Due to the scaling, it has become very significant to consider the effect of generated traps in Si-SiO_2 junction. The use of high-k gate dielectric generates a large number of interface traps at the surface channel and oxide trap charges in the gate dielectric bulk of MOS transistors, which would result in the degradation of device electrical characteristics. As the oxide thickness is reduced these interface trap charges become significant gradually. During the last three decades, gate oxide thickness was so large that this phenomenon was not noticeable, but nowadays it is a matter of importance to consider the interface states during MOS operation [9–12]. In this paper the interface charge densities have been measured and analyzed for thin MOS structure using ZrO_2 and HfO_2 high-k materials as gate dielectric.

2. Theoretical Analysis

Contributions are judged in terms of their extensive and debasing effect on the operational behavior of MOS devices; oxide-semiconductor interfacial traps must be considered as the most significant nonideality encountered in the MOS structure. Interface traps are allowed energy states in which electrons are localized in the vicinity of a material's surface. All of the bulk centers are found to add levels to the energy band diagram within the forbidden band gap. SiO_2 is often treated as an ideal insulator, where there are no traps or states at the interface of Si/SiO_2. But in real devices, the Si/SiO_2 interface and bulk SiO_2 are far from being electrically neutral. These may be caused by positive or negative charges at the Si/SiO_2 interface or by mobile ionic charges and fixed charges trapped within the oxide and itself, which are often created during the fabrication process. In reality, there are two types of charges that are associated with oxide layer, namely, interface trap charge and oxide charge. These charges play an important role affecting the physical and electrical properties of a MOS device. The features that distinguish interface trap charge from oxide charge are that interface charge varies with gate bias whereas oxide charge is independent of gate bias. The two thus have different effects on C-V characteristics. There are three types of oxide charges associated with the SiO_2-Si system. They are fixed oxide charge, mobile oxide charge, and oxide trapped charge. All of these charges are very much dependent on the device fabrication process. Already in the pioneering work for understanding the physical properties of MOS structures, the capacitance-voltage (C-V) method was used to establish the main qualities of oxide-silicon interfaces.

Three insulator related parameters typically determined with C-V measurement are (1) oxide charge density, ρ_{ox}, (2) interface trap density, Q_{it}, and (3) gate semiconductor work function difference, $\emptyset_{ms}$. They are determined from the flatband voltage:

$$V_{FB} = \emptyset_{ms} - \frac{1}{\varepsilon_{ox}\varepsilon_o} \int_0^{t_{ox}} x\rho(x)\,dx, \tag{1}$$

where ε_{ox} is the permittivity of the oxide, ε_o is the permittivity of the free space, and t_{ox} is the oxide thickness. The fixed charge density Q_f and interface trap density Q_{it} (function of surface potential, $\emptyset_s$) are assumed to be located at the SiO_2/Si interface and the remaining mobile ionic and oxide trap charge density, ρ_{ox} in the SiO_2, leading to the flatband voltage expression for uniform oxide charge density,

$$V_{FB} = \emptyset_{ms} - \frac{Q_f + Q_{it}(\emptyset_s)}{\varepsilon_{ox}\varepsilon_o} t_{ox} - \frac{\rho_{ox}}{2\varepsilon_{ox}\varepsilon_o} t_{ox}^2. \tag{2}$$

On assuming that only Q_{it} is present in the oxide layer, then the equation becomes

$$V_{FB} = \emptyset_{ms} - \frac{Q_{it}(\emptyset_s)}{\varepsilon_{ox}\varepsilon_o} t_{ox}. \tag{3}$$

But the most accurate and very sensitive method to extract the D_{it} is the conductance method. Recently, the conductance method has been investigated and adapted for rigorously proving the electrical passivation of novel semiconductor-dielectric interfaces. The equivalent circuits [12] for conductance measurement in MOS capacitor are

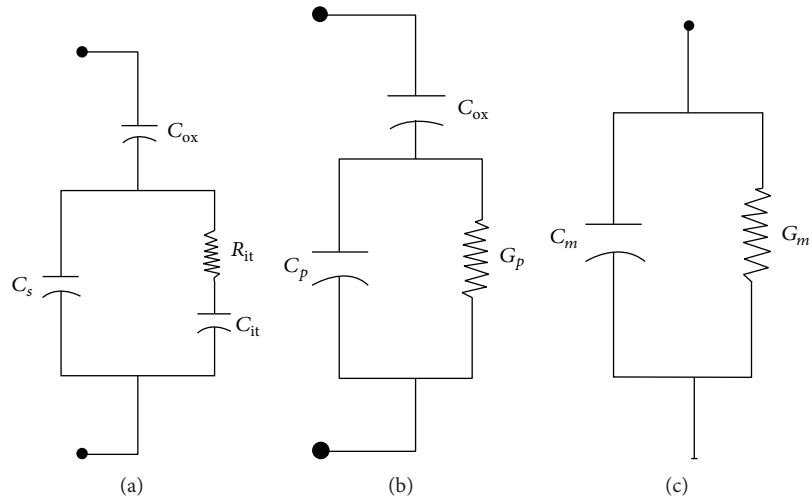

Figure 1: Equivalent circuits for conductance measurements; (a) MOS-C with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), and (c) measured circuit.

given in Figure 1. Figure 1(a) consists of the oxide (insulator) capacitance per unit area (C_{ox}), semiconductor capacitance per unit area (C_s), interface trap capacitance per unit area (C_{it}) and interface trap resistance per unit area (R_{it}). For the MOS interface charge analysis it is convenient to replace the circuit of Figure 1(a) with Figure 1(b): here C_p is the equivalent parallel capacitance and the G_p is the equivalent parallel conductance.

So the admittance of Figures 1(a) and 1(b) is given by

$$Y_a = j\omega C_s + \frac{j\omega q D_{it}}{1 + j\omega\tau_{it}} \frac{(1 - j\omega\tau_{it})}{(1 - j\omega\tau_{it})},$$

$$= j\omega C_s + \frac{j\omega q D_{it}(1 - j\omega\tau_{it})}{1 + (\omega\tau_{it})^2}, \quad (4)$$

$$Y_b = j\omega C_p + G_p,$$

where $\omega = 2\pi f$ (f = measured frequency), $C_{it} = qD_{it}$, and q is the magnitude of electronic charge.

If the real part and imaginary part are compared, respectively, we get

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2}. \quad (5)$$

Dividing G_p by ω makes it symmetrical in $\omega\tau_{it}$ and G_p/ω is directly related to D_{it}. It is more effective to calculate D_{it} [12], because it has only a parameter related to interface trap without including C_s. This equation considers the interface trap with single energy level in the band gap. For continuously distributed interface charge, we have to consider Figure 1(c), consisting of the measured equivalent parallel conductance (G_m) and measured capacitance (C_m). Using this circuit, G_p/ω value (assuming negligible series resistance and tunnel conductance) is given,

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2(C_{ox} - C_m)^2}. \quad (6)$$

D_{it} can be calculated from the obtained G_p/ω versus f graph from (5). At maximum G_p/ω, the ω is the inverse of τ_{it}; approximate expression of D_{it} can thus be given in terms of the measured maximum conductance as

$$D_{it} = \frac{2}{q}\left[\frac{G_p}{\omega}\right]_{max}. \quad (7)$$

3. Results and Discussion

Five groups of p-substrate MOS devices have been analyzed consisting of two high-k dielectric materials, ZrO_2 and HfO_2, having the dielectric constant of 22 for amorphous structure of the materials [13]. These materials were studied for different EOT at p-type doping level of 1×10^{17} cm^{-3}. If a high-k material can replace SiO_2, the dielectric thickness increases proportionally to keep the equal dielectric capacitance and EOT is the thickness of any dielectric material scaled by the ratio of its dielectric constant to the dielectric constant of SiO_2 ($k = 3.9$). Q_{it} can be extracted from the slope of plot between flatband voltages and oxide thickness. By considering presence of only interface charge at the oxide-semiconductor interface the value of Q_{it} has been calculated theoretically and through simulation. Figure 2 shows the plot of magnitude of the flatband voltage as function of EOT for the high-k materials.

The graphs shown in Figure 2 clearly demonstrate the validity of our assumption in (3). The flat-band voltage of all the samples indicated negative value due to the existence of deep donor type surface states and positive interface charges. This noticeably indicates the presence of some parasitic charges at the interface. The deviation of simulated result from the theoretical result was found due to the high dielectric value of the materials. The theoretical interface charge Q_{it} present in each of the MOS capacitor was 5×10^{10} C at the interface. The simulated result obtained is shown in Table 2. Using the simulated C-V and G-V characteristics curve the values of the C_m and G_m have been measured,

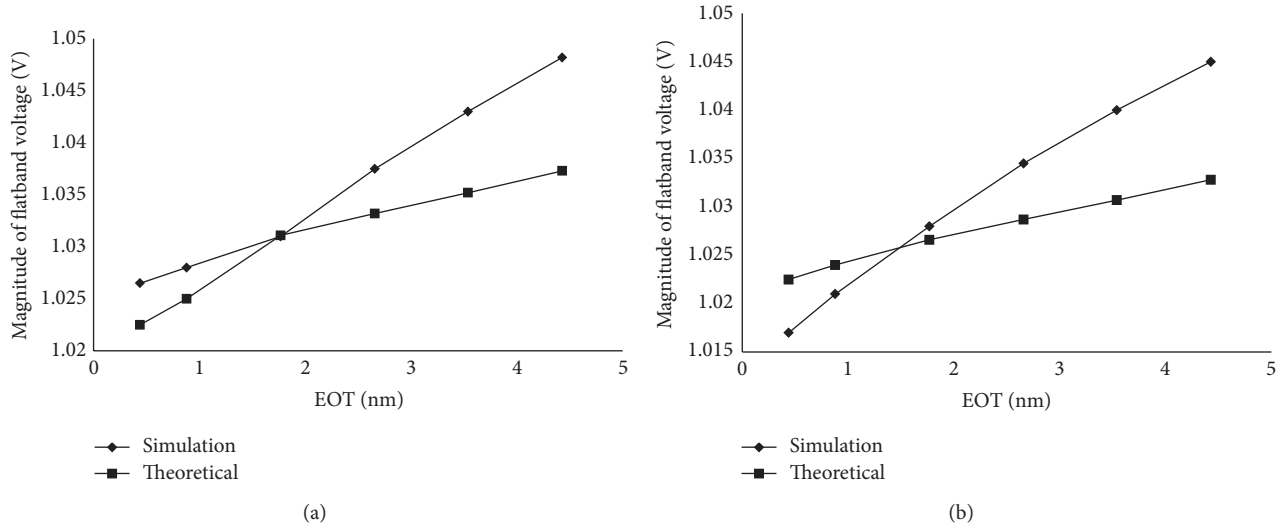

Figure 2: Variation of flatband voltage with oxide thickness for (a) ZrO_2 and (b) HfO_2.

Table 2: Interface charge Q_{it} in SiO_2 and different high-k material.

Material	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_{avg}
ZrO_2	1.355e11	1.400e11	1.436e11	1.314e11	1.266e11	1.363e11	1.356e11
HfO_2	1.379e11	1.400e11	1.582e11	1.278e11	1.339e11	1.217e11	1.366e11

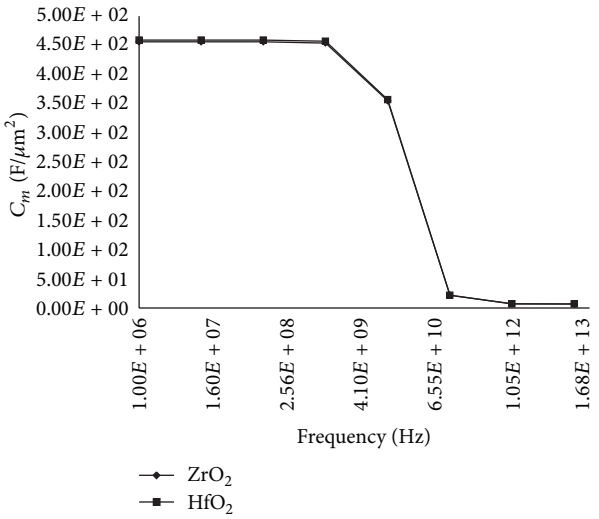

Figure 3: Variation of C_m with frequency.

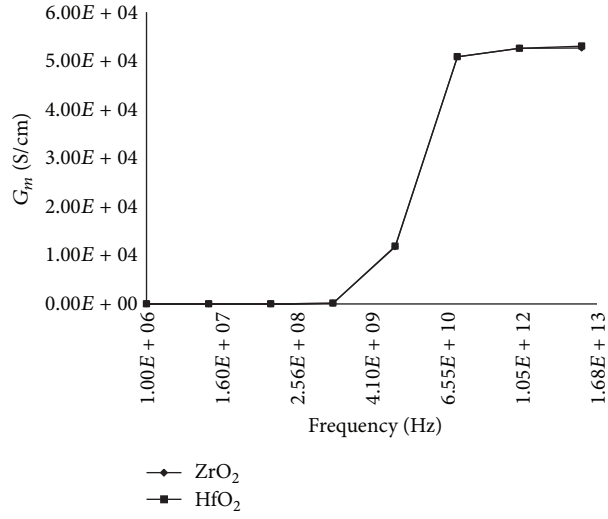

Figure 4: Variation of G_m with frequency.

respectively, and the variation with frequency for the high-k dielectric materials has been shown in Figures 3 and 4.

The value of D_{it} has been calculated using conductance method. It is a technique which replaces MOS capacitor with equivalent circuit model and calculates D_{it}. Using the G-V curve conductance of the MOS has been calculated in depletion region of −1 V.

Figures 5(a) and 5(b) show the relationship of G_p/ω versus f using ZrO_2 and HfO_2 high-k material of EOT at 1.77 nm, 2.65 nm, and 3.54 nm, respectively. This figure shows that the local maximum of each curve indicates the magnitude of D_{it}. The peaks of the curves used for the oxide materials mean that the interface state energy levels are measured. Both G_p/ω and G_p will peak as a function of bias voltage at gate terminal but only G_p/ω will peak as a function of frequency. G_p/ω will peak at a lower frequency when admittance is measured as a function of frequency with bias voltage at the gate as parameter or at the gate bias near to flatbands and when admittance is measured as a function of bias voltage at the gate with frequency as

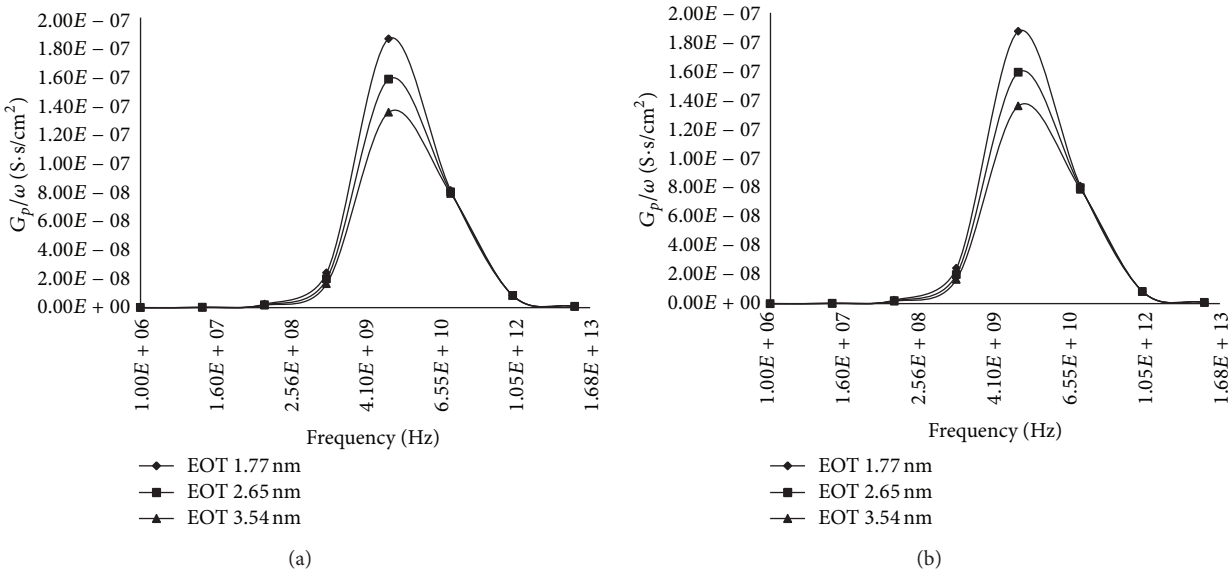

Figure 5: G_p/ω and frequency for (a) ZrO_2 and (b) HfO_2 at different EOT.

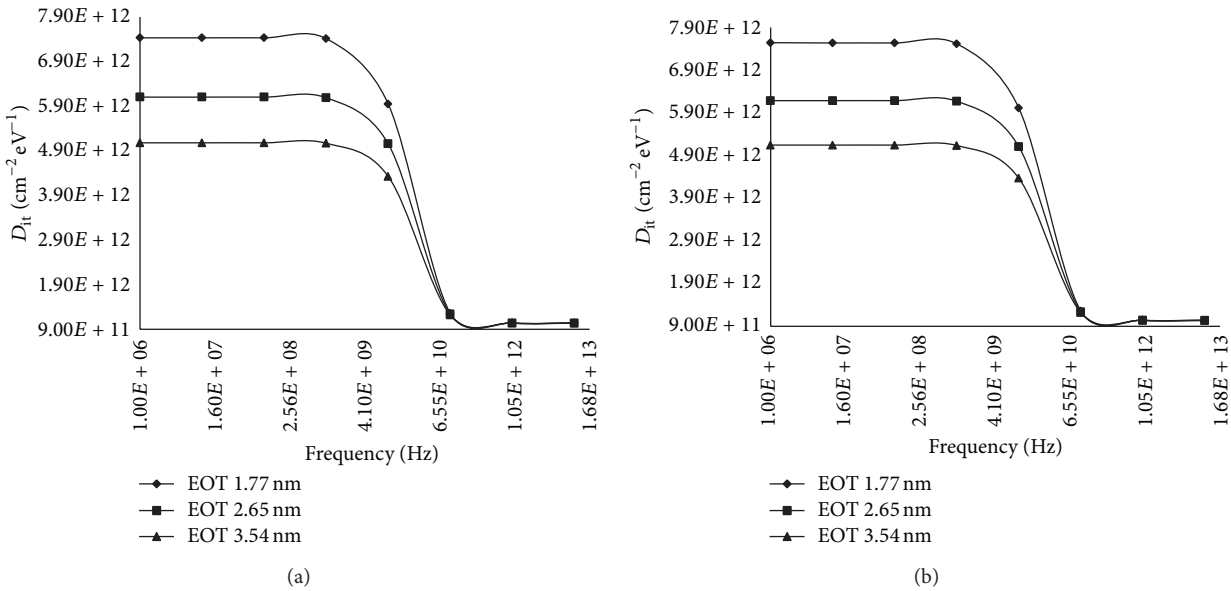

Figure 6: D_{it} and frequency for (a) $ZrO_2$and (b) HfO_2 at different EOT.

parameter. The characteristics of the graph are the same for these two materials and the G_p/ω is maximum at 10^{10} Hz. D_{it} was calculated for the different EOT for ZrO_2 and HfO_2. The increase in D_{it} is observed as the EOT is reduced as shown in Table 3 for a particular frequency of 1 MHz. This depicts that D_{it} increases as the EOT reduces because density of trap charges is concentrated at the interface.

Figures 6(a) and 6(b) show the relationship between D_{it} and f for ZrO_2 and HfO_2 high-k material, respectively. The value of D_{it} has been calculated at different frequencies using (5). At smaller frequencies the D_{it} has a constant and high value. As the frequency reaches the inverse of interface trap time constant, the D_{it} starts decreasing and at very high frequencies the value goes to a saturation region. The high value of D_{it} at lower frequencies and a low value at higher frequencies are because trap charges are able to follow low frequencies and as the frequency increases trap charges cannot follow it so it does not contribute to D_{it} at the large

Table 3: D_{it} value for ZrO_2 and HfO_2 at different EOT at 1 MHz.

EOT (nm)	ZrO_2 (cm^{-2} ev^{-1})	HfO_2 (cm^{-2} ev^{-1})
1.77	7.53E + 12	7.64E + 12
2.65	6.18E + 12	6.26E + 12
3.54	5.14E + 12	5.21E + 12

frequencies. The D_{it} is predicted by conductance method for HfO_2 with molecular beam deposition (MBD) process and for ZrO_2 with atomic layer deposition (ALD) technique which is in resemblance to the fabrication results [14] at p-type doping level of 1×10^{17} cm^{-3}.

4. Conclusions

The flatband voltage of all the samples indicated negative value due to the existence of deep donor type surface states and positive interface charges, and these effects are highly responsible for variation in D_{it} with EOT. The interface charge densities have been calculated using *C-V* method as well as conductance method and it has been found that as the thickness of the oxide is reduced, the interface trap density increases for both HfO_2 and ZrO_2. This increase in D_{it} by reducing the oxide thickness clearly demonstrates that the interface between oxide and silicon gets weaker.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

The authors are highly indebted to the Department of Science and Technology (DST), Ministry of Science and Technology, Government of India, for supporting this technical work.

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