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Research Article

Single VDTA Based Dual Mode Single Input Multioutput Biquad Filter

Rajeshwari Pandey, Neeta Pandey, and Navin Singhal

Department of Electronics and Communication Engineering, Delhi Technological University, Delhi 110042, India

Correspondence should be addressed to Rajeshwari Pandey; rajeshwaripandey@gmail.com

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This paper presents a dual mode, single input multioutput (SIMO) biquad filter configuration using single voltage differencing transconductance amplifier (VDTA), three capacitors, and a grounded resistor. The proposed topology can be used to synthesize low pass (LP), high pass (HP), and band pass (BP) filter functions. It can be configured as voltage mode (VM) or current mode (CM) structure with appropriate input excitation choice. The angular frequency (ω_0) of the proposed structure can be controlled independently of quality factor (Q_0). Workability of the proposed biquad configuration is demonstrated through PSPICE simulations using 0.18 μm TSMC CMOS process parameters.

1. Introduction

The ever shrinking feature size of devices on ICs and consequential reduction of power supply voltage poses serious challenges to analog design such as reduced input common mode range, output swing, and linearity. This can be handled by operating in the current domain, as current mode circuits are designed for lower voltage swings. Therefore, over the last few decades, current mode (CM) processing has evolved as an alternative design technique [1] and has resulted in emergence of numerous active building blocks (ABBs) [2] such as differential difference current conveyor transconductance amplifier (DDCCTA) [3], current difference transconductance amplifier (CDTA) [4], current feedback operational amplifier (CFOA) [5], operational transresistance amplifier (OTRA) [6], differential input buffered transconductance amplifier (DBTA) [7], current difference buffered amplifier (CDBA) [8], current conveyor transconductance amplifier (CCTA) [9], and voltage differencing transconductance amplifier [10] which are used for realization of various signal processing and generation circuits. Among these, the voltage differencing transconductance amplifier (VDTA) is a recently introduced active element [11]. The VDTA is a voltage input current output ABB with two transconductance gain stages. It provides electronic tuning ability through its transconductance gains. Thus, the VDTA is one of the most suitable ABBs for easy and compact CMOS implementation [12] of signal processing and generating circuits.

Electronic filters are essential building block of communication and instrumentation systems. A variety of VDTA based biquadratic filters are available in literature [10–18] which can be classified as single input multioutput (SIMO) [11–14, 18], multi-input single output (MISO) [15–17], and multi-input multioutput MIMO [10] filter configurations. These filters can further be classified as voltage mode [10, 13, 17], current mode [11, 12, 14–16], and dual mode [18] structures. A detailed comparison of these structures is given in Table 1.

It may be noted from Table 1 that only a single VDTA based dual mode SIMO structure is available in literature and it uses five passive components. In this paper, a new single VDTA based SIMO-type dual mode biquad filter using four passive components is proposed. The proposed structure provides either voltage or current outputs through proper selection of input excitation. The proposed structure realizes three standard filter functions, namely, LP, HP, and BP, with independent ω_0 and Q_0 tuning feature. Proposed circuit configuration also offers low passive sensitivities. The rest of the paper is organised as follows: In Section 2, detailed circuit description is presented. The circuit behaviour in

Table 1: Comparison of the proposed work with the previously reported work.

Ref.	Number of inputs	Simultaneous outputs	Standard filter functions	VM/CM	Active blocks used	Passive components	Orthogonal tunability of ω_0 and Q_0
[10]	Two	Two	LP, HP, BP	VM	Two	Two C	No
[11]	One	Three	LP, HP, BP	CM	Two	Two C	No
[12]	One	Three	LP, HP, BP	CM	One	Two C; One R	Yes
[13]	One	Five	LP, HP, BP, NF, AP	VM	Two	Two C; Two R	Yes
[14]	One	Three	LP, HP, BP	CM	One	Two C	No
[15]	Three	One	LP, HP, BP, NF, AP	CM	Two	Two C	Yes
[16]	Three	One	LP, HP, BP, NF, AP	CM	One	Two C	No
[17]	Three	One	LP, HP, BP, NF, AP	VM	one	Two C	Yes
[18]	One	Three	LP, HP, BP	VM and CM	One	Three C; two R	Yes
Proposed work	One	Three	LP, HP, BP	VM and CM	One	Three C; one R	Yes

presence of nonidealities of VDTA has been analysed in Section 3 and deviation in filter parameters is enumerated. The functionality of the proposed filter has been confirmed through SPICE simulations using 0.18 μm TSMC CMOS process parameters and the results are presented in Section 4. Section 5 concludes the paper.

2. Circuit Description

The circuit symbol of the VDTA is shown in Figure 1 where P and N are the input terminals and Z, X_+, and X_- are the output terminals. The CMOS realization of VDTA [10] is shown in Figure 2. It consists of two transconductance (TC) stages, namely, input and output stages. The input TC stage converts the differential input voltage (V_P -V_N,) into current I_Z through first TC gain (g_{m1}) and the voltage at Z terminal (V_Z) is converted to current (I_X) through second TC gain (g_{m2}). All VDTA terminals exhibit high impedance values [10]. The port relations are given in matrix form in

$$\begin{bmatrix} I_Z \\ I_{X_+} \\ I_{X_-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}. \quad (1)$$

The TC gains, g_{m1} and g_{m2}, respectively, can be expressed as [10]

$$g_{m1} = \frac{g_1 g_2}{g_1 + g_2} + \frac{g_3 g_4}{g_3 + g_4}$$
$$g_{m2} = \frac{g_5 g_6}{g_5 + g_6} + \frac{g_7 g_8}{g_7 + g_8}, \quad (2)$$

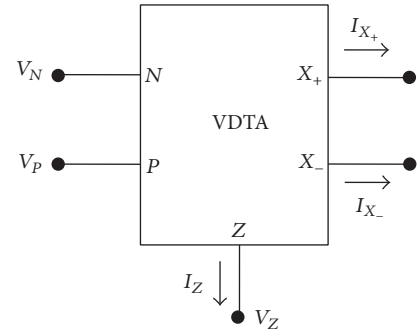

Figure 1: Circuit symbol of VDTA.

where g_i is the transconductance value of the ith transistor and is given by

$$g_i = \sqrt{\mu C_{ox} \left(\frac{W}{L}\right)_i I_{Bi}}. \quad (3)$$

In (3), μ is effective carrier mobility; C_{ox} is the gate oxide capacitance per unit area; I_{Bi} and $(W/L)_i$ represent the dc bias current and the aspect ratio of the ith MOS transistor, respectively.

The proposed dual mode SIMO filter is shown in Figure 3 which comprises of a single VDTA, three capacitors, and a resistor. With appropriate choice of input signal, it can be configured as either VM or CM structure.

2.1. The VM Configuration. The filter configuration of Figure 3 operates in VM if input current is removed ($I_{in} = 0$).

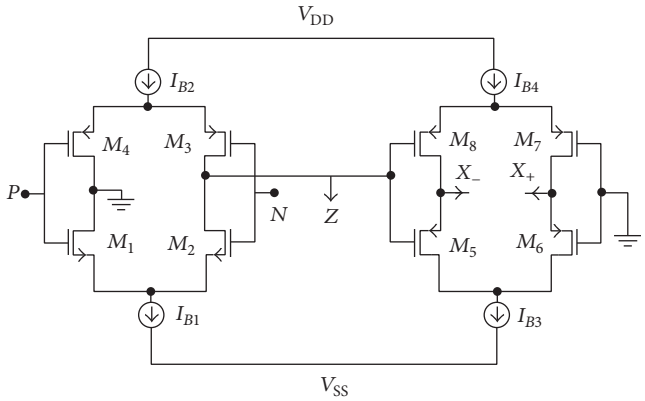

Figure 2: The CMOS realization of VDTA [10].

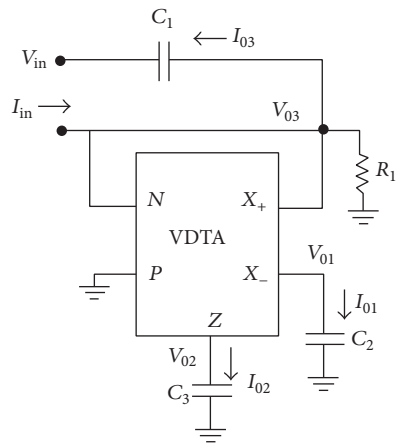

Figure 3: Proposed VM and CM mode SIMO filter.

Routine analysis of the circuit yields voltage mode transfer functions given by

$$\left.\frac{V_{01}}{V_{in}}\right|_{LP} = \frac{g_{m1}g_{m2}/C_2C_3}{\Delta}$$
$$\left.\frac{V_{02}}{V_{in}}\right|_{BP} = -\frac{(g_{m1}/C_3)\,s}{\Delta} \quad (4)$$
$$\left.\frac{V_{03}}{V_{in}}\right|_{HP} = \frac{s^2}{\Delta},$$

where

$$\Delta = s^2 + \frac{s}{R_1C_1} + \frac{g_{m1}g_{m2}}{C_1C_3}. \quad (5)$$

2.2. The CM Configuration. Removal of voltage source V_{in} ($V_{in} = 0$) in Figure 3 results in CM filter topology. Analysis of the resulting topology leads to the following transfer function:

$$\left.\frac{I_{01}}{I_{in}}\right|_{LP} = -\frac{g_{m1}g_{m2}/C_1C_3}{\Delta}$$
$$\left.\frac{I_{02}}{I_{in}}\right|_{BP} = \frac{(g_{m1}/C_1)\,s}{\Delta} \quad (6)$$
$$\left.\frac{I_{03}}{I_{in}}\right|_{HP} = -\frac{s^2}{\Delta}.$$

The angular frequency ω_0 and quality factor Q_0 for both the filter structures are given by

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_3}} \quad (7)$$

$$Q_0 = R_1\sqrt{\frac{g_{m1}g_{m2}C_1}{C_3}}. \quad (8)$$

It may be observed from (7) and (8) that the parameters ω_0 can be set to a desired value and Q_0 can be controlled through R_1 independently.

It is relevant to mention here that the voltage outputs of the proposed structure are available at high impedance, which is invariably true for all available VDTA based voltage mode structures [10, 13, 17, 18]. It is therefore suggested that either the voltage output structures should be used to drive the high input impedance circuits or the output should be taken through buffers. Further, in CM operation, current outputs are available through passive elements and would require additional ABBs for accessing current at high impedance. However, it is also applicable to all single ABB based SIMO structures [12, 14, 18]. It may also be noted that in proposed structure I_{02} can be accessed at high impedance by lifting the drain node of transistors M_1 and M_4.

The passive sensitivities of ω_0 and Q_0 of the proposed filter structures can be expressed as given by (9) and their absolute values do not exceed unity in magnitude.

$$S^{\omega_0}_{g_{m1},g_{m2}} = \frac{1}{2},$$
$$S^{\omega_0}_{C_1,C_3} = -\frac{1}{2},$$
$$S^{Q_0}_{g_{m1},g_{m2}} = \frac{1}{2},$$
$$S^{Q_0}_{C_1} = \frac{1}{2}, \quad (9)$$
$$S^{Q_0}_{C_3} = -\frac{1}{2},$$
$$S^{Q_0}_{R_1} = 1.$$

3. Nonideal Analysis

In this section, the effect of nonidealities of VDTA on the filter performance has been analysed. The nonidealities associated

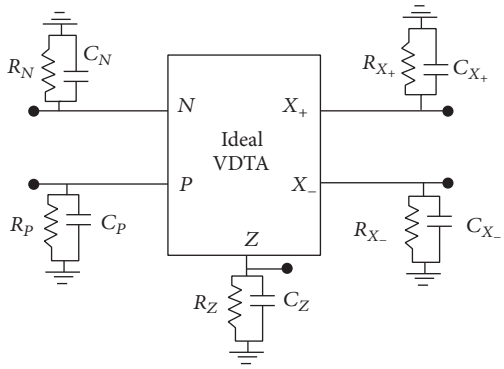

Figure 4: Nonideal model of VDTA.

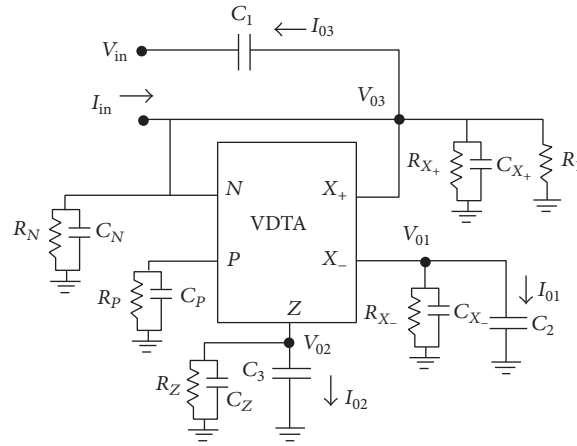

Figure 5: Nonideal filter structure.

with VDTA based circuits may be divided into two groups. The first group concerns the finite voltage tracking errors and the second results from the presence of parasitics at all the terminals of VDTA.

3.1. Nonideality due to Tracking Error. Taking the tracking errors of the VDTA into account, the port relations expressed by (1) get modified as

$$\begin{bmatrix} I_Z \\ I_{X_+} \\ I_{X_-} \end{bmatrix} = \begin{bmatrix} \beta_1 g_{m1} & -\beta_1 g_{m1} & 0 \\ 0 & 0 & \beta_2 g_{m2} \\ 0 & 0 & -\beta_2 g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}, \tag{10}$$

where β_1 and β_2 are, respectively, the tracking errors for the first and second stages of the VDTA. In presence of β_1 and β_2, the new expressions for ω_0 and Q_0 can be obtained as

$$\omega_0 = \sqrt{\frac{\beta_1\beta_2 g_{m1} g_{m2}}{C_1 C_3}}$$
$$Q_0 = R_1 \sqrt{\frac{\beta_1\beta_2 g_{m1} g_{m2} C_1}{C_3}}. \tag{11}$$

It is evident that the values of ω_0, and Q_0 deviate slightly from their ideal values. These changes may be accommodated by adjusting TC gains g_{m1} and g_{m2} through bias current of VDTA. However, the sensitivities of ω_0 and Q_0 with respect to β_1 and β_2 are quite low, as given by

$$S^{\omega_0}_{\beta_1,\beta_2} = S^{Q_0}_{\beta_1,\beta_2} = \frac{1}{2}. \tag{12}$$

3.2. Nonideality due to Parasitics. The nonideal model of VDTA is shown in Figure 4 wherein each terminal is characterized by finite parasitic impedance consisting of resistance in parallel with capacitance (R_P, C_P; R_N, C_N; R_Z, C_Z; R_{X_+}, C_{X_+}; R_{X_-}, C_{X_-} for V_P, V_N, Z, and X terminals, resp.) [12]. The filter performance might deviate from ideal behaviour due to parasitics of VDTA. Thus, the filter structure of Figure 3 is to be analysed in the presence of parasitics. Using the nonideal model of VDTA, the proposed filter structure can be redrawn as shown in Figure 5.

Using routine analysis, ω_0 and Q_0 of the filter configuration of Figure 5 may be obtained as

$$\omega_0 = \sqrt{\frac{A}{B}} \tag{13}$$

$$Q_0 = \sqrt{\frac{AB}{D}}, \tag{14}$$

where

$$A = g_{m1} g_{m2} + \frac{1}{R_1 R_Z} + \frac{1}{R_{X_+} R_Z} + \frac{1}{R_N R_Z} \tag{15}$$

$$B = C_1 C_3 + C_Z C_3 + C_{X_+} C_Z + C_N C_Z + C_2 C_{X_+} + C_2 C_N, \tag{16}$$

$$D = \left(\frac{C_3}{R_Z} + \frac{C_3}{R_1} + \frac{C_2}{R_{X_+}} + \frac{C_Z}{R_1} + \frac{C_Z}{R_{X_+}} + \frac{C_Z}{R_N} + \frac{C_{X_+}}{R_Z} + \frac{C_N}{R_Z} \right)^2. \tag{17}$$

The parasitic resistances associated with all terminals are practically too large making

$$\left(\frac{1}{R_1 R_Z} + \frac{1}{R_{X_+} R_Z} + \frac{1}{R_N R_Z} \right) \langle\langle g_{m1} g_{m2}. \tag{18}$$

Thus, (15) reduces to

$$A \approx g_{m1} g_{m2}. \tag{19}$$

By selecting external capacitances much larger than parasitic capacitances, (16) can be simplified as

$$B = C_3 C_1 + C_Z \left(C_3 + C_{X_+} \right) + C_{X_+} \left(C_2 + C_Z \right) + C_2 C_N = C_3 C_1 + C_Z C_3 + C_{X_+} C_2 + C_2 C_N \tag{20}$$
$$= C_3 \left(C_1 + C_Z \right) + C_2 \left(C_{X_+} + C_Z \right) \approx C_3 C_1.$$

Table 2: List of 0.18 μm CMOS process parameters used.

NMOS	LEVEL = 7+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9+XJ = 1E-7NCH = 2.3549E17 VTH0 = 0.3672292+K1 = 0.5893162 K2 = 3.053194E-3K3 = 1E-3+K3B = 1.8246765 W0 = 1E-7NLX = 1.771394E-7+DVTOW = 0 DVT1W= 0 DVT2W = 0+DVT0 = 1.2540673 DVT1 = 0.3671218DVT2 = 0.0374285+U0 = 2.3448599 UA = -1.473692E-9UB= 2.452512E-18+UC = 6.566514E-11 VSAT = 1.025312E5 A0 = 2+AGS = 0.4532362 B0= 3.222688E-7B1 = 5E-6+KETA = -0.0109204 A1= 0 A2 = 0.9744209+RDSW = 105 PRWG = 5PRWB = -0.2+WR = 1 WINT = 1.660932E-9 LINT = .520122E-8+XL = 0 XW = -1E-8DWG = -2.794177E-9+DWB = 7.839758E-9 VOFF = -0.091184 NFACTOR = 2.2684002+CIT = 0 CDSC = 2.4E-4 CDSCD = 0+CDSCB = 0 ETA0 = 3.031184E-3 ETAB = 9.427488E-6+DSUB = 0.0153239 PCLM = 0.704686 PDIBLC1 = 2435533 +PDIBLC2 = 2.76003E-3 PDIBLCB = -0.1 DROUT = 0.8035265+PSCBE1 = 4.372065E10 PSCBE2 = 2.518414E-9 PVAG = 0.0749313+DELTA = 0.01 RSH = 6.4 MOBMOD = 1+PRT = 0 UTE = -1.5 KT1 = -0.11+KT1L = 0 KT2 = 0.022 UA1= 4.31E-9+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 +WL = 0 WLN = 1 WW = 0+WWN = 1WWL = 0 LL = 0+LLN = 1 LW = 0 LWN = 1+LWL = 0 CAPMOD = 2 XPART = 0.5+CGDO = 8.79E-10 CGSO = 8.79E-10 CGBO = 1E-12+CJ = 9.605878E-4 PB = 0.8 MJ = 0.3831903+CJSW = .643918E-10 PBSW = 0.8 MJSW = 0.1407086+CJSWG = 3.3E-10 PBSWG = 0.8 MJSWG = 0.1407086+CF = 0 PVTH0 = -6.317463E-6 PRDSW = -.8440536+PK2 = 9.250773E-4 WKETA = 1.074587E-3 LKETA = -.453047E-3+PU0 = 4.3638022 PUA = -1.50117E-12 PUB = 0+PVSAT = 1.356677E3 PETA0 = 1.003159E-4 PKETA = -2.902589E-3
PMOS	LEVEL = 7+VERSION = 3.1 TNOM= 27 TOX = 4.1E-9+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.38888+K1 = 0.5636481 K2 = 0.0308017 K3 = 0+K3B= 7.400372 W0 =1E-6 NLX = 1.385693E-7+DVT0W = 0DVT1W = 0 DVT2W = 0+DVT0 = 0.5846878 DVT1 = 0.2165736 DVT2 = 0.1+U0 = 3.6325808 UA = 1.459877E-9 UB = 1.18636E-21+UC = -1E-10 VSAT = 2E5 A0 = 1.7849198+AGS = 0.3754547 B0 = 3.172437E-7 B1 = 7.280105E-7+KETA = 0.0156934 A1 = 0.3222966 A2 = 0.3+RDSW = 196.7345438 PRWG = 0.5 PRWB = -0.1589203+WR = 1 WINT = 0 LINT = 2.702835E-8+XL = 0 XW = -1E-8 DWG = -2.627805E-8+DWB = 1.03876E-9 VOFF = - 0.0927458 NFACTOR = 2+CIT = 0 CDSC = 2.4E-4 CDSCD = 0+CDSCB = 0 ETA0 = 0.145648 ETAB = -0.0543017+DSUB = 0.9610783 PCLM = 2.0812378 PDIBLC1 = 7.131255E-4+PDIBLC2 = 0.0185628 PDIBLCB = -9.170788E-4 DROUT = 0+PSCBE1 = 3.206374E9 PSCBE2 = 9.279285E-10 PVAG= 15+DELTA = 0.01 RSH = 7.3 MOBMOD = 1+PRT = 0 UTE = -1.5 KT1 = -0.11+KT1L = 0 KT2 = 0.022 UA1 = .31E-9+UB1 = -7.61E-18UC1 = -5.6E-11 AT = 3.3E4 +WL = 0 WLN = 1 WW= 0+WWN = 1 WWL= 0 LL = 0 +LLN= 1LW= 0 LWN = 1+LWL = 0 CAPMOD = 2 XPART = 0.5+CGDO = 6.41E-10CGSO = 6.41E-10 CGBO = 1E-12+CJ = 1.136354E-3 PB = 0.8459606 MJ = 0.4088875+CJSW = 2.255183E-10 PBSW = 0.832695 MJSW = 0.3342249+CJSWG = 4.22E-10 PBSWG = 0.832695 MJSWG = 0.3342249 +CF = 0 PVTH0 = 4.532819E-3 PRDSW = 7.6587079+PK2 = 3.513392E-3 WKETA = 0.0251295 LKETA = -2.32504E-3+PU0 = -.4738884 PUA = -8.40745E-11 PUB = 1E-21+PVSAT = -50 PETA0 = 1E-4 PKETA = -2.114056E-3

Similarly, (17) can be simplified as

$$D = \left(\frac{C_3}{R_Z} + \frac{C_3}{R_1} + \frac{C_2}{R_{X_+}} + \frac{C_Z}{R_1} + \frac{C_Z}{R_{X_+}} + \frac{C_Z}{R_N} + \frac{C_{X_+}}{R_Z} + \frac{C_N}{R_Z}\right)^2 = \left(\frac{C_3 + C_Z + C_N}{R_1} + \frac{C_3 + C_{X_+}}{R_Z} + \frac{C_Z + C_2}{R_{X_+}} + \frac{C_Z}{R_N}\right)^2 \approx \left(\frac{C_3}{R_1} + \frac{C_3}{R_Z} + \frac{C_2}{R_{X_+}} + \frac{C_Z}{R_N}\right)^2 \approx \left(\frac{C_3}{R_1} + \frac{C_3}{R_Z} + \frac{C_2}{R_{X_+}}\right)^2 \approx \left(\frac{C_3}{R_1}\right)^2. \tag{21}$$

Substituting (19) and (20), it may thus be noted that (13) can be approximated to (7) which represents the ideal value of ω_0.

Also putting (19), (20), and (21) in (14), Q_0 may be expressed by (22) which is equal to its ideal value.

$$Q_0 \approx \sqrt{\frac{g_{m1}g_{m2}C_3C_1}{(C_3/R_1)^2}} = R_1\sqrt{\frac{g_{m1}g_{m2}C_1}{C_3}}. \tag{22}$$

It may be concluded therefore that, by selecting external capacitances much larger than parasitic capacitances, the frequency response of the proposed structure would not be affected.

4. Simulation Results

The functionality of the proposed filter is validated through SPICE simulated using 0.18 μm TSMC process parameters which have been listed in Table 2 for ready reference. First, the DC transfer characteristic of the VDTA is validated which is followed by verification of both VM and CM filter responses.

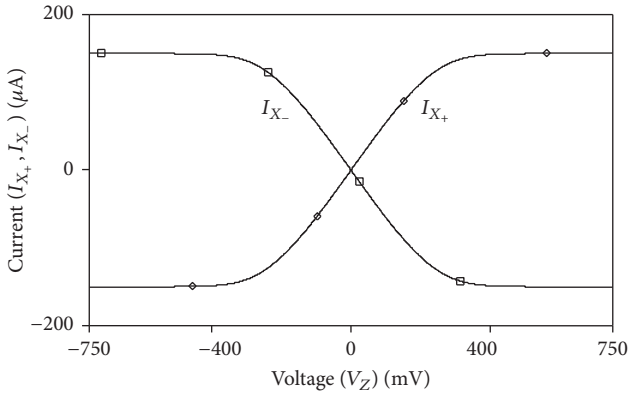

Figure 6: The DC transfer characteristics of the VDTA.

Table 3: The % frequency deviation for CM LP filter.

Capacitor value	Theoretical f_0	Simulated f_0	% frequency deviation
0.1 nF	1.01231 MHz	1.06 MHz	4.5
0.01 nF	10.1231 MHz	10.639 MHz	4.8
1 pF	101.231 MHz	108.854 MHz	7.0
0.1 pF	1.01231 GHz	886.833 MHz	12.3
0.01 pF	10.1231 GHz	2.269 GHz	77.0
1 fF	101.231 GHz	2.76 GHz	97.3

Subsequently, as a case study, the transient behaviour of BP filter (VM and CM) is studied and its total harmonic distortion (THD) variation is also observed.

4.1. The DC Transfer Characteristic. The VDTA structure shown in Figure 3 [10] with supply voltages of ±0.9 V is used for simulation. The same aspect ratios of the MOS transistors are used as given in [10]. The DC transfer characteristic of the VDTA, as shown in Figure 6, is plotted for $I_{B1} = I_{B2} = I_{B3} = I_{B4} \cong 150\,\mu$A, which resulted in $g_{m1} = g_{m2} = 636.3\,\mu$ A/V.

4.2. Frequency Response. The LP, HP, and BP filter responses for both VM and CM filter structures with $f_0 = 1$ MHz and $Q_0 = 1$ are shown in Figures 7(a) and 7(b), respectively. The passive components were chosen as $C_1 = C_2 = C_3 = 0.1$ nF and $R_1 = 1.57$ KΩ. The tuning of gain expression for low pass filter with respect to C_2 is shown in Figure 7(c).

It may be observed from (7) and (8) that f_0 can be tuned by changing either capacitance values (C_1, C_3) or the transconductances (g_{m1}, g_{m2}). The transconductance variation can be obtained through bias current adjustment. The Q_0 tuning can be accomplished through R_1 without affecting f_0. The orthogonal adjustment of f_0 and Q_0 is shown by plotting the BP responses for $f_0 = 100$ KHz, 1 MHz, and 10 MHz while keeping Q_0 fixed at 1. The responses for VM and CM structures are shown in Figures 8(a) and 8(b), respectively. Similarly, the simulation results for $Q_0 = 0.5$, 1, and 5 when f_0 remains constant at 1 MHz, for VM and CM topologies, are shown in Figures 9(a) and 9(b), respectively. It is evident from Figures 8 and 9 that f_0 and Q_0 are orthogonally tunable.

Another set of simulations have been carried out to examine frequency response limitations of the proposed structure. Low pass current mode response is used for illustration. The simulations conditions on bias currents are kept the same as reported in the beginning while the capacitor values are changed and corresponding theoretical and simulated pole frequencies are noted and listed in Table 3. It may be noted that there is a close match between theoretical and simulated pole frequencies when the values of external capacitors are chosen to be sufficiently greater than parasitic capacitances. However, a significant deviation is seen when external capacitances are selected close to parasitics (tens of fF order). Further, it is also observed that parasites limit frequency range because their pole frequencies are much lower than those for tracking errors.

4.3. Transient Response. The time domain behaviour of the VM BP filter is also studied by applying three sinusoidal frequency components: a low frequency signal of 1 MHz, a high frequency component of 100 MHz, and the third component of 10 MHz which is f_0 of the BP filter. The input signal is shown in Figure 10(a) and its frequency spectrum is depicted in Figure 10(b). The transient response of the filter and the associated frequency spectrum are shown in Figures 11(a) and 11(b), respectively. It may be noted that the frequency components other than f_0 are significantly attenuated.

To observe the transient response of CM BP filter, it is driven by an input current signal consisting of three frequency components: 1 KHz, 10 KHz, and 100 KHz. The BP filter is designed for an $f_0 = 10$ KHz. The related results are depicted in Figures 12 and 13 which clearly show that the signals outside the bandwidth of BP filter are significantly attenuated.

To check the quality of the output of BP filter, the percentage total harmonic distortion (%THD) with the sinusoidal input signal is obtained as shown in Figure 14. It is observed from Figure 14(a) that the %THD remains considerably low [19] for input signal values up to 500 mV for VM topology. Similarly, it may be noted from Figure 14(b) that the %THD is well below 7% for current signals up to 200 μA. The simulated value of power dissipation, in both VM and CM operations, is observed to be 0.54 mW.

5. Conclusion

A single VDTA based dual mode SIMO biquad which realizes LP, HP, and BP responses has been proposed in this paper. The proposed biquad is a SIMO structure and can be configured as voltage mode or current mode with appropriate input excitation selection. The angular frequency and the quality factor of the proposed configuration can be controlled in a noninteractive manner. The filter f_0 is electronically tunable. The filter structure functionality is verified through SPICE

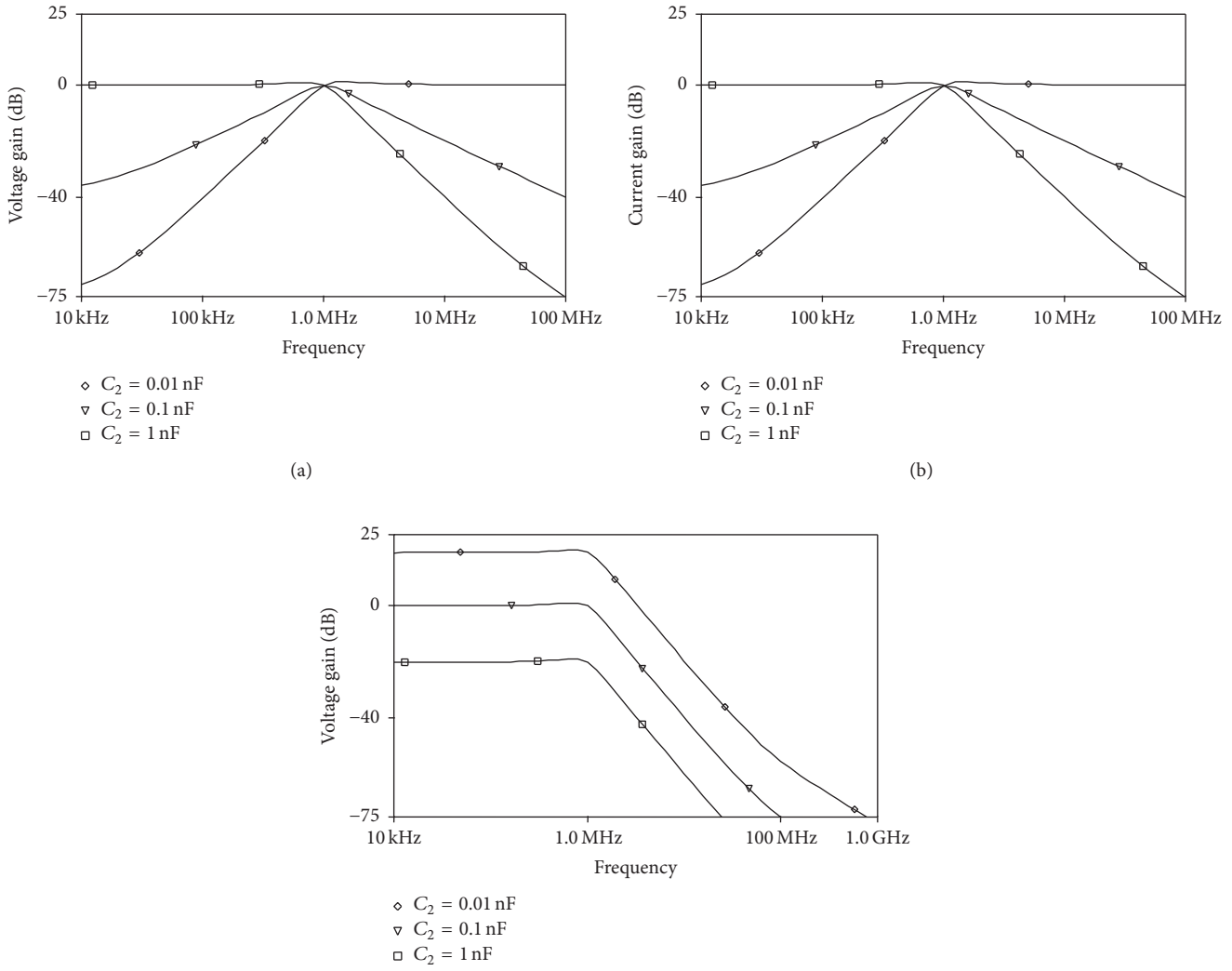

Figure 7: Frequency response at $f_0 = 1$ MHz and $Q_0 = 1$. (a) VM topology. (b) CM topology. (c) VM LP filter depicting gain tuning with C_2.

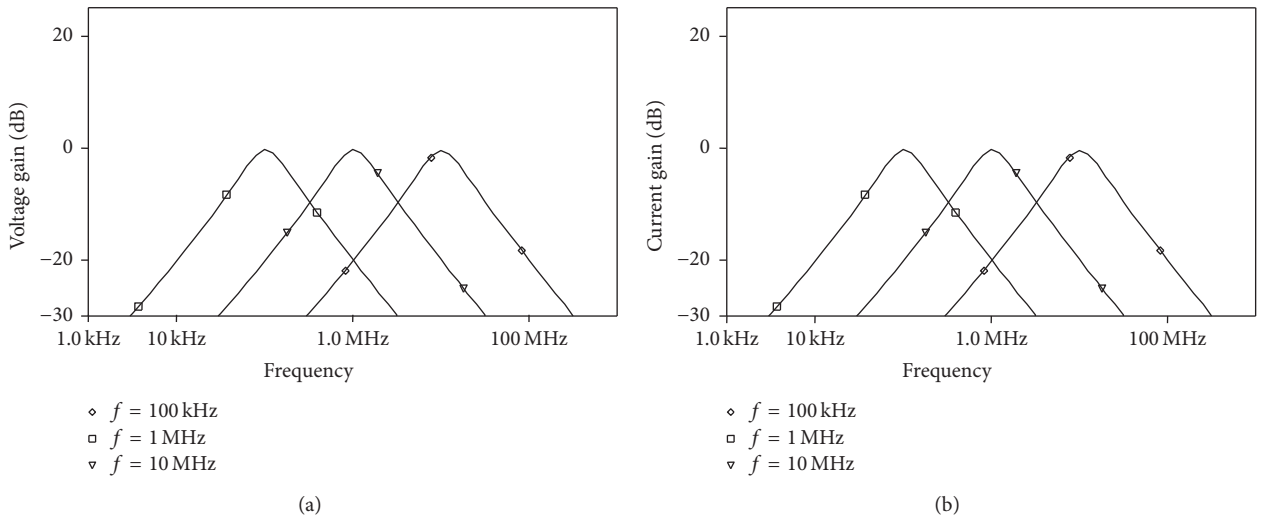

Figure 8: BP responses for $f_0 = 100$ KHz, 1 MHz, and 10 MHz keeping Q_0 fixed at 1 for (a) VM and (b) CM topology.

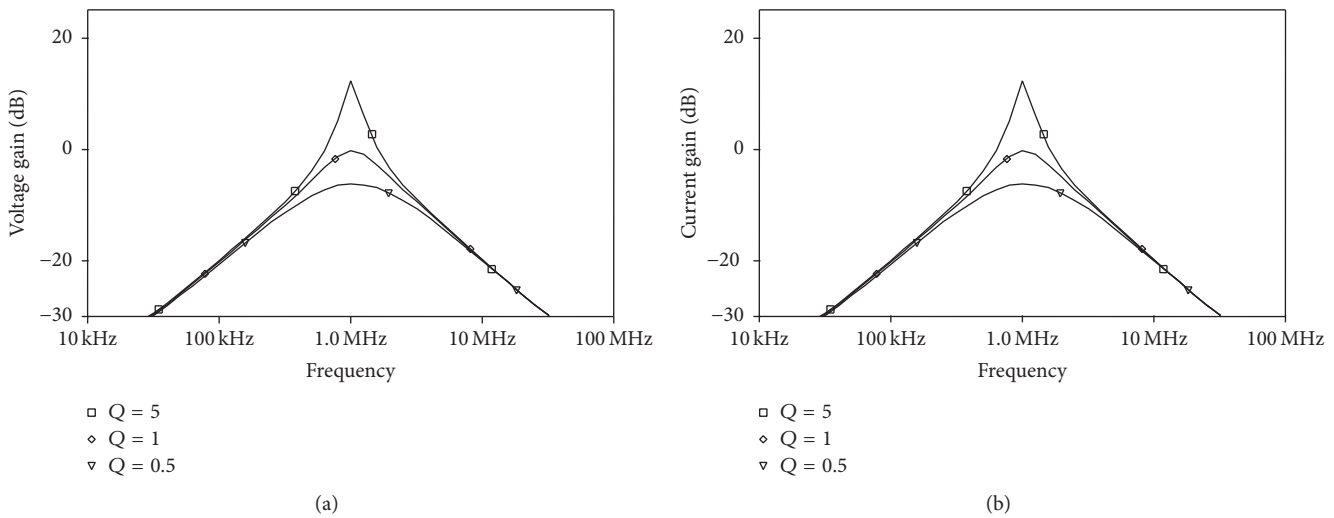

FIGURE 9: BP responses for $Q_0 = 0.5, 1$, and 5 with $f_0 = 1$ MHz for (a) VM and (b) CM topology.

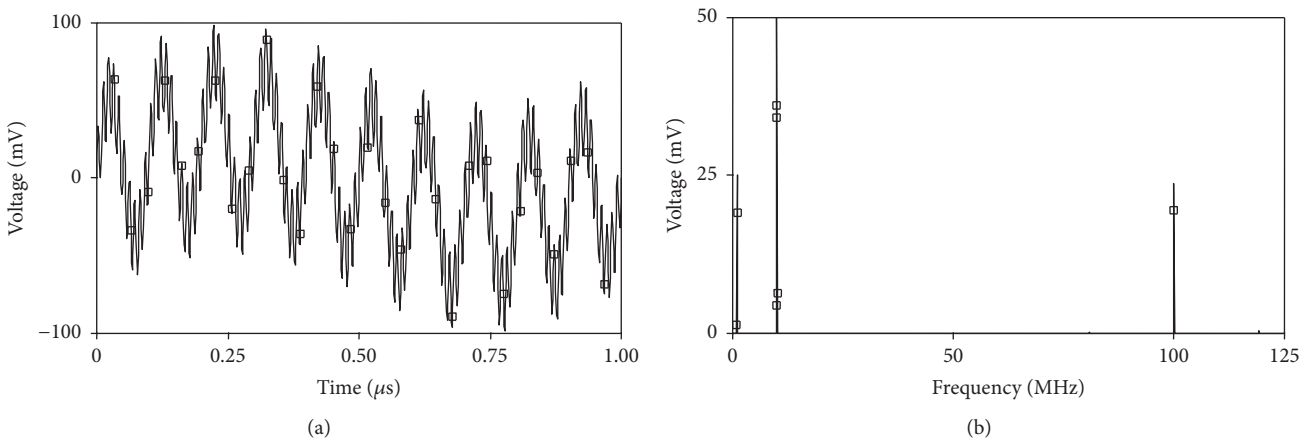

FIGURE 10: (a) The voltage input transient signal and (b) its frequency spectrum.

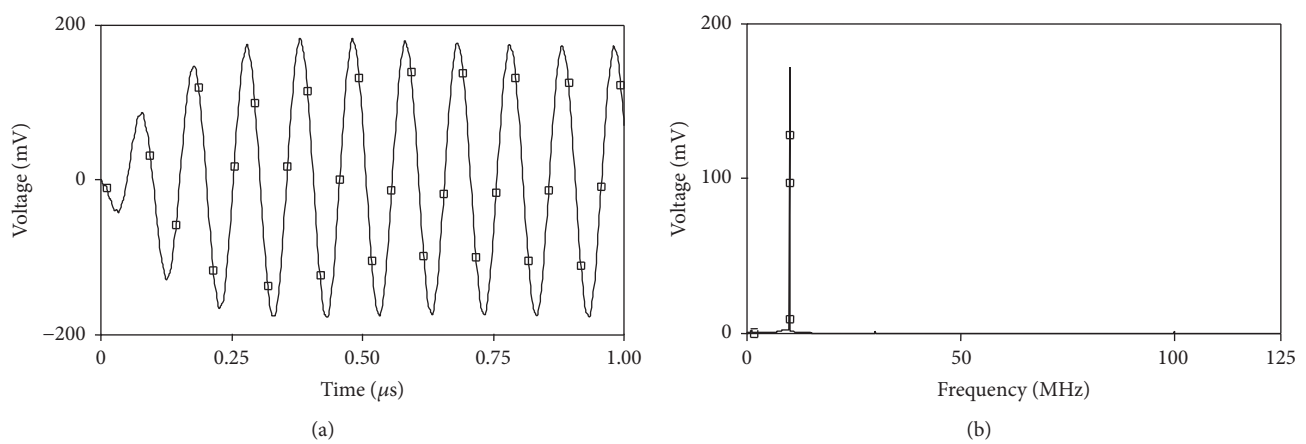

FIGURE 11: (a) The voltage output transient signal and (b) its frequency spectrum.

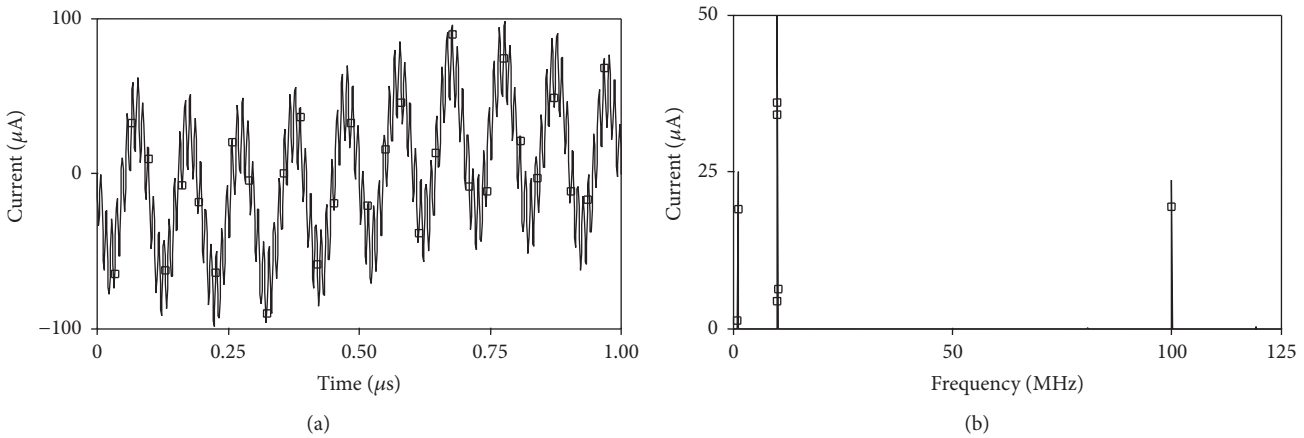

Figure 12: (a) The current input transient signal and (b) its frequency spectrum.

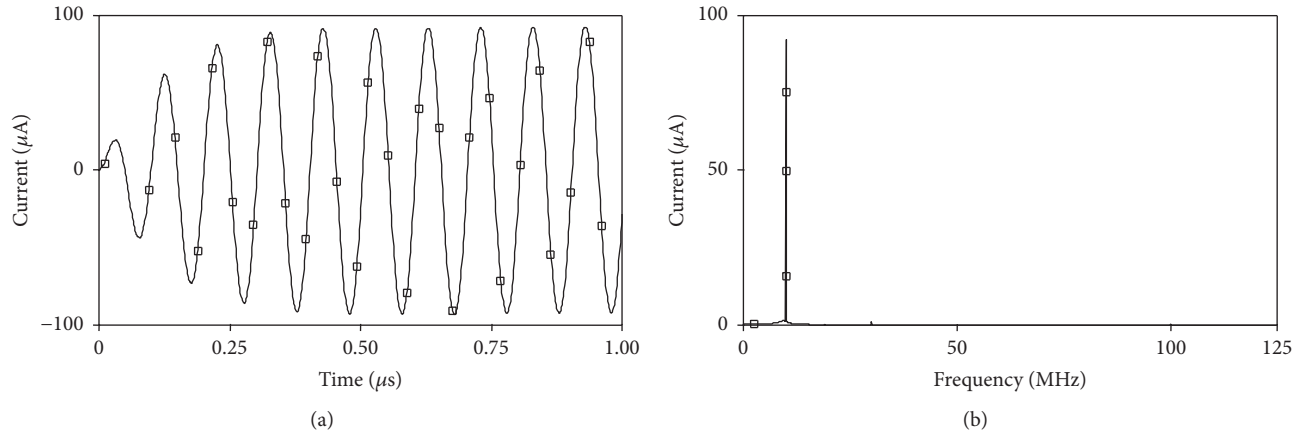

Figure 13: (a) The current output transient signal and (b) its frequency spectrum.

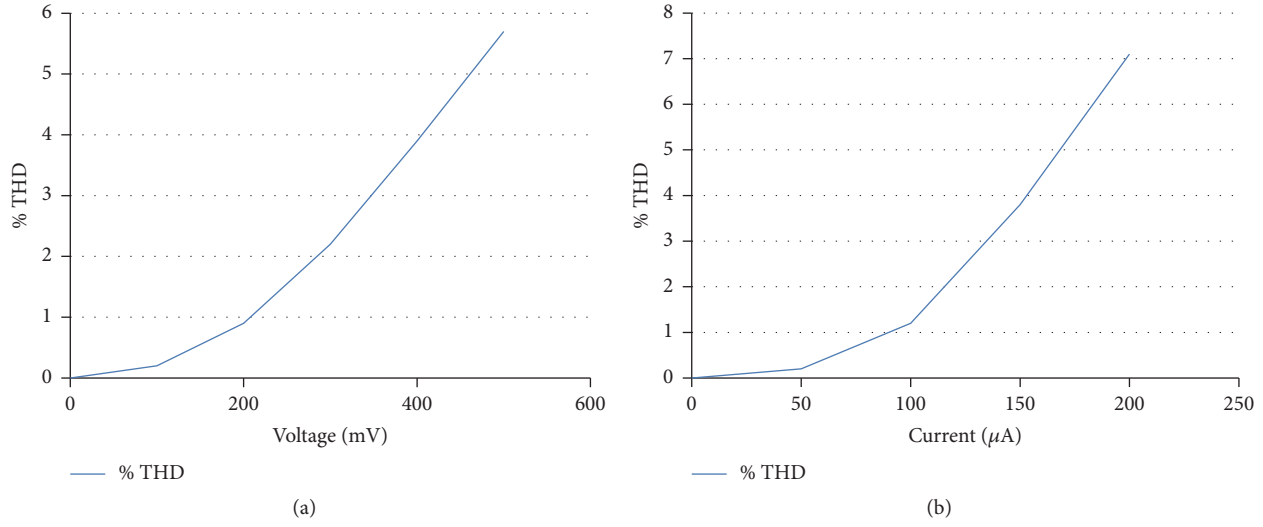

Figure 14: THD variation of BP filter against amplitude of the applied sinusoidal signal at 159 KHz (a) voltage mode and (b) current mode.

simulations and both frequency and transient responses are studied.

Competing Interests

The authors declare that they have no competing interests.

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