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Research Article

Improved Maximum Likelihood S-FSK Receiver for PLC Modem in AMR

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This paper deals with an optimized software implementation of a narrowband power line modem. The modem is a node in automatic meter reading (AMR) system compliant to IEC 61334-5-1 profile and operates in the CENELEC-A band. Because of the hostile communication environments of power line channel, a new design approach is carried out for an S-FSK demodulator capable of providing lower bit error rate (BER) than standard specifications. The best compromise between efficiency and architecture complexity is investigated in this paper. Some implementation results are presented to show that a communication throughput of 9.6 kbps is reachable with the designed S-FSK modem.

1. Introduction

International concerns about natural environment preservation have been increasingly serious during the last decades. In fact, one of the most ecologically influencing factors is energy. Besides, energy consumption rise was unexpectedly important and quick, neglecting efficiency and ecological considerations. These facts have pushed several countries to try to change their energy consumption policies.

The widest idea behind operating energy efficiently is called SmartGrid. This concept, as its name suggests, involves integrating intelligence into the whole power grid; generation, transmission, distribution, and management are concerned. The goal is to increase power generation, transmission, distribution, and usage efficiency by reducing power waste, favoring renewable energies, and sensitizing consumers about their actual consumption [1].

This big concept was only expressed lately after arise of more specific and actually applicable ideas. The first is automatic meter reading (AMR), enabling automated remote meter reading. Later were introduced automatic meter infrastructure (AMI) and automatic meter Management (AMM), which are two expansions providing more consumer- and management-oriented services.

Despite its obvious advantages, AMR have not been yet rolled out significantly. Actually, a major broad deployment inconvenient of smart meters was the lack of reliability on hostile communication environments of power line channel. In fact, early implementations of PLC modems were basic on ordinary amplitude shift keying (ASK) or frequency shift keying (FSK) techniques.

In this paper, we investigate the importance of spread frequency shift keying (S-FSK) modulation scheme to make transmissions robust against narrowband noise and attenuation in such hostile channel. Hence, an intelligent power line communication (PLC) modem solution for automatic meter reading using International Electrotechnical Commission (IEC) S-FSK profile is simulated and implemented using digital signal processor (DSP) [2].

The paper is organized as follows. In Section 2 we will start by presenting PLC-based automatic meter reading solution. The chosen S-FSK profile is briefly introduced. A description of the proposed S-FSK receiver is presented in Section 3. In Section 4 we focus on implementation of S-FSK modulation scheme using DSP architecture. The efficiency of the proposed design was illustrated by some implementation results that show the performances of the

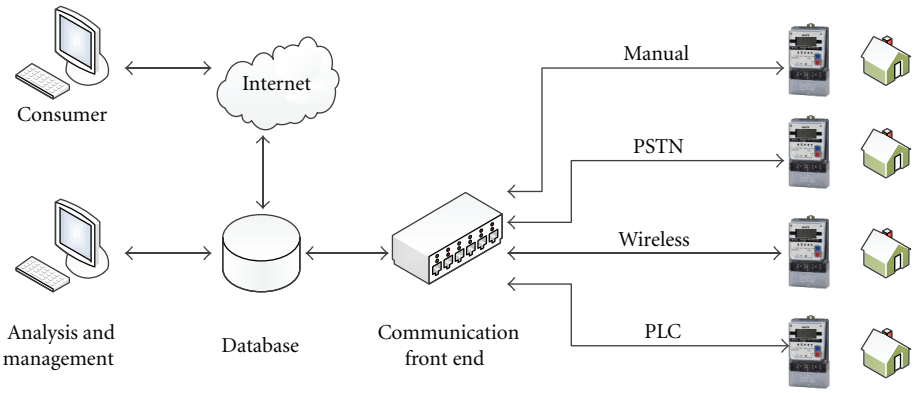

Figure 1: Different automatic meter reading techniques.

realized PLC Modem. Finally some conclusions are outlined in Section 5.

2. PLC Modems for AMR

The evolution of meter reading has been outstanding during the last decades. Several power suppliers, distributers jointly with their technological partners, have tried several novel approaches in order to automate meter reading.

The evolution from traditional manual meter reading to actual and future intelligent infrastructures passing through e-meters, semiautomatic meter reading, and fully automated meter reading gave these actors a great experience in this ever-evolving field.

Despite the abundance of the available technologies, power line communication has been agreed to be the best fit for last-mile meter reading and meter management communication. In fact, this technology has one of the lowest costs and is easily set up. Moreover, the technology is now considered as sufficiently ripe to be widely deployed.

PLC, as a technology, is very wide. A myriad of techniques are available using different modulation techniques and different protocols. From another side, the regulation is still under work. Nevertheless, some profiles have already been standardized and are being adopted by the market. The IEC S-FSK profile, for example, is actually one of the most used for AMR because it proved its simplicity and maturity.

In this section, we will briefly introduce automatic meter reading concepts, then present PLC from both technical and technological sides, and finally give a short survey on S-FSK PLC modems.

2.1. Automatic Meter Reading. Automatic meter reading is a technique used to collect data from electricity, gas, water, or other utility meters. Unlike manual meter reading, automatic meter reading relies on communication technologies to collect users' consumption. Meters send data automatically through a communication network to the management system. Collected data can be then transferred to a central database to be analyzed and used for billing. This means that billing can be based on actual consumption rather than on an estimate based on previous consumption statistics, giving customers better control of their usage of electric energy, gas, or water. From the other side, predicting energy usage remains a key advantage for energy distributors. With AMR, distributors can get accurate information of consumption profile of each consumer and monitor the network in order to prevent or capture defects.

The advantages of AMR are several and obvious:

(i) increasing meter reading and billing accuracy and security;

(ii) permitting a flexible tariff changing;

(iii) giving user the control over its consumption;

(iv) enabling a better grid monitoring and load management;

(v) remote power disconnection and reconnection.

Automatic meter reading system is summarized by Figure 1. Meters' data are collected using one of the available ways of communication into a database. This database is then accessible for analysis and management purposes in the information system center. A subset of these data can also be accessed by customers using dedicated services.

Several automatic meter reading technologies can be used depending on grid topology. Most important ones are as follows

(i) handheld, walk-by, and drive-by AMR;

(ii) public switched telephone network-based AMR;

(iii) wireless communication-based AMR;

(iv) power line communication-based AMR.

2.2. Power Line Communication-Based AMR. Power line communication consists of the use of the power lines as a physical communication medium. PLC has been used for data transfer for both indoor and outdoor networks. Anyhow, the profile of these applications is different.

Concerning PLC use for AMR and outdoor communication, PLC is the most approved technology by electricity distributors. In fact, electric network is already well expanded and offers a great coverage. Thus, no additional wireless

or wired communication medium needs to be used and deployment costs are then cut.

The main idea behind PLC is the use of the power line to carry radio frequency signals. Actually, a low power modulated signal containing information is added to the electric signal. Data then propagates over the electric network and is detected by remote stations.

Several modulation techniques can be used to transport data over power lines. But most of them are based on frequency modulation. Actually, data is converted to a higher frequency signal which is superimposed to the 50 Hz/60 Hz electrical signal. The signal is then repeatedly transmitted over the network until it reaches the destination node.

Several PLC communication profiles have been proposed and each profile is essentially based on the modulation scheme chosen.

Two different modulation scheme classes can be distinguished:

(i) single-carrier modulations;

(ii) multicarrier modulations.

The first technique is the simpler one. It uses a narrow frequency band for data transfer. Examples of these modulation schemes are FSK, S-FSK, and continuous phase frequency shift keying (CPFSK). These modulation schemes are often chosen for their maturity and implementation simplicity. Though, they do not offer great data transfer rates. Actually, data rates generally range from 300 bps to 2.4 kbps [3]. Narrowband PLC has been receiving widespread attention due to its applications in the SmartGrid.

The second uses multiple adjacent carriers in order to transfer data. Usually orthogonal frequency division multiplexing (OFDM) or a derived modulation scheme is used. These modulation schemes are applied in order to increase raw data throughput and/or to cope with harsh channel conditions. Broadband PLC is seen as an exciting and effective technology for multimedia distribution within homes.

In either case, AMR PLC technique must handle poor channel quality. In fact, outdoor power lines are exposed to several noise sources. Furthermore, power lines present highly varying impedance due to topology changes and high attenuation. Hence, power line channel quality is considered as time, space, and frequency dependent [4].

In order to overcome these impairments, high performance processing is unavoidable. This includes channel estimation and equalization, strong forward error correction algorithms, and signal repetition.

In addition to noise and channel quality difficulties, PLC-based AMR has two other main challenges. The first is that unlike usual communication techniques where transfer speed is the most significant criteria, cost and reliability are the most important factors in AMR. The second is the existence of a lot and very different protocols and standards, their specific underlying problems, and interoperability issues.

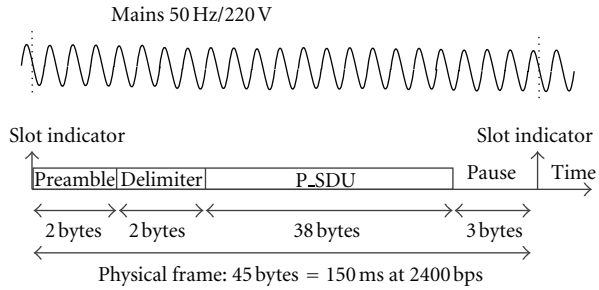

Figure 2: Physical frame structure.

2.3. PLC Modem Based on S-FSK Profile. The communication profile described by the IEC 61334-5-1 standard is based on the S-FSK modulation technique.

S-FSK is a modulation and demodulation technique which combines some of the advantages of a classical spread spectrum system (e.g., immunity against narrowband interferers) with the advantages of a classical FSK system (low-complexity, well-investigated implementations).

As the classical FSK, S-FSK uses two frequencies to transmit binary information at each bit time. By spreading the two used frequencies, S-FSK makes these two channels independent. This characteristic is then used by the demodulator and ensures a better reception quality than FSK. In fact, if signal qualities of the two channels are close, the demodulator makes the decision by comparing the signal on both channels. Otherwise, demodulation is based only on the channel having a better reception quality. Channel quality estimation is calculated using a predefined preamble preceding transmitted data.

Synchronization in this profile is based on zero crossing detection of electric signal. Therefore, the transmission and reception must start on the main zero cross. Due to the phase shift between 50 Hz and the carrier, the zero cross signal may provide incorrect timing of the bit-wise synchronization. To recover this delay the bit synchronization adjustment method is implemented in the modem software. This algorithm based on correlation method can move bit border during reception.

Time is divided into system wide synchronized time slots, and physical frames are only transmitted with the beginning of timeslots.

Timeslot synchronization is achieved using detection of any frame's preamble and delimiter as described in Figure 2. After physical synchronization, each station must keep track of slot indicator using an internal clock.

As described earlier, communication between meters and management system is done through a special node called access node usually placed at the medium/low voltage (MV/LV) transformer stations. Access nodes are specific nodes that manage the communication on a specific meter network.

This profile uses a master/slave communication paradigm based on polling mechanism. In fact, meters can only respond to queries made by master station. This method combined with slotted time simplifies considerably medium access control.

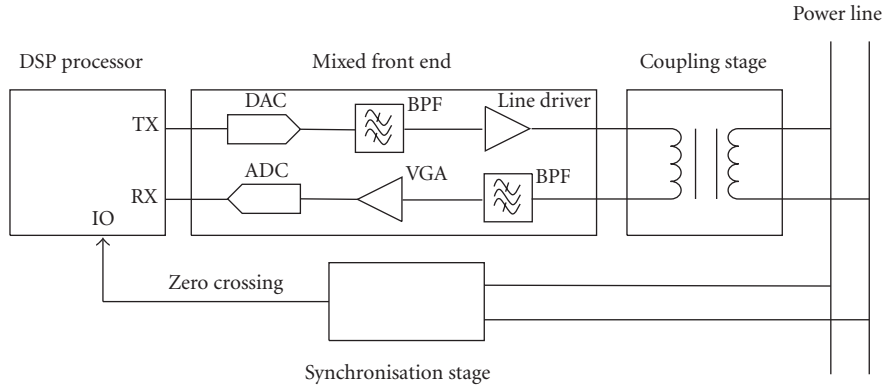

Figure 3: PLC modem functional block diagram.

The modem that we propose in this paper is an AMR PLC modem using IEC61334-5-1 compliant profile and operates in the CENELEC—A band [5]. It is based on three main stages as described in Figure 3; DSP processor, mixed front end, and a coupling interface:

(i) digital stage including DSP processor and external memories. DSP processor provides flexible software implementation and easily upgrade to new software version or merging standards;

(ii) mixed front end based on digital to analog converter (DAC) and line driver for transmitter section, analog to digital converter (ADC) and variable gain amplifier (VGA) for receiver section, and external band-pass filter (BPF);

(iii) coupling interface makes connection between the mixed front end and the power lines. It provides protection from high voltage and peak voltage/current, attenuation of 50/60 Hz signal, impedance matching to the mains for both transmitter and receiver paths, and nonisolated power supply.

The use of a DSP permits a greater control over the signal processing stage and a greater flexibility of the implemented S-FSK modem.

3. S-FSK Modulation Technique

This section details S-FSK modulation principle and gives theory and simulations of suboptimum receiver.

3.1. The S-FSK Principle. S-FSK modulation consists of a binary FSK modulation in which the frequency deviation Δf is large enough to generate a spectrum with two separate lobes. For this reason, the concept of dual channel is introduced: channel 0 refers to the signal placed around a frequency f_0 and channel 1 refers to the signal placed around a frequency f_1, with $\Delta f = |f_1 - f_0|/2$ [6, 7].

The symbols to be transmitted are generated with a rate $1/T$, where T is the symbol period, and belong to the alphabet $\{-1, +1\}$. Therefore, binary hypotheses H_0 and H_1 can be associated with 0 and 1 being transmitted, respectively.

A digital signal waveform with binary signaling consists of two kinds of signals $s_0(t)$ and $s_1(t)$ for $nT \le t \le (n+1)T$, n is a positive integer:

$$\begin{aligned} H_0 &: s_0(t) = A\sin(2\pi f_0 t), \\ H_1 &: s_1(t) = A\sin(2\pi f_1 t), \end{aligned} \tag{1}$$

where A is a real constant.

A frequency selective channel with an additive nonwhite Gaussian noise is considered; however, the channel gain G_i and the noise power spectral density N_i are assumed to be flat around the frequency f_i. Therefore, at the receiver input, the signal-to-noise ratio (SNR) for the channel i is

$$\mathrm{SNR}_i = \frac{A^2 G_i^2/2}{N_i/T}, \quad \text{with } i \in \{0, 1\}. \tag{2}$$

The SNR_i completely characterize the quality of the received signal. Moreover, another characterization of the quality of the received S-FSK signal may be made through the unbalancing factor x and the average signal-to-noise ratio $\mathrm{SNR}_{\mathrm{av}}$. This last term is defined as the ratio of the signal energy and the average noise power densities. These parameters are related to (2) as follows:

$$\mathrm{SNR}_{\mathrm{av}} = 2\frac{\mathrm{SNR}_0\ \mathrm{SNR}_1}{\mathrm{SNR}_0 + \mathrm{SNR}_1}, \qquad x = \frac{\mathrm{SNR}_1}{\mathrm{SNR}_0}. \tag{3}$$

3.2. The Maximum Likelihood S-FSK Receiver. In practical channels, the received signal phase is very difficult or even impossible to track. Thus, the detection process may have to disregard the phase information to avoid complex circuits, at some expense of performance degradation. This is called noncoherent detection [8, 9].

Using the channel model early presented the received signal under hypotheses H_0 and H_1 is

$$r(t) = \begin{cases} G_0 s_0(t, \theta) + n_0(t) & \text{under } H_0, \\ G_1 s_1(t, \theta) + n_1(t) & \text{under } H_1, \end{cases} \tag{4}$$

where $s_i(t, \theta)$ is the signal with an unknown phase θ and $n_i(t)$ is the white Gaussian noise with zero mean and a noise power spectral density $N_i/2$, with $i \in \{0, 1\}$.

The unknown phase is random with a power density function $p_\theta(\theta)$. We assume that θ is uniformly distributed on $[0, 2\pi]$, that is,

$$p_\theta(\theta) = \frac{1}{2\pi}, \quad 0 \le \theta \le 2\pi. \tag{5}$$

The correlation receiver correlates the input signal $r(t)$ with a stored replica of the signal $s_i(t)$. The outputs r_i are necessary to discriminate whether $+1$ or -1 has been transmitted.

The modulus of the envelop detectors' outputs may be modeled as follows for two orthogonal S-FSK signals:

$$r_0 = \begin{cases} |n_0| & \text{under } H_1 \\ |s_0 + n_0| & \text{under } H_0, \end{cases}$$
$$r_1 = \begin{cases} |n_1| & \text{under } H_0 \\ |s_1 + n_1| & \text{under } H_1, \end{cases} \tag{6}$$

where n_i is an additive circularly Gaussian noise with zero mean and variance σ_i^2, with $i \in \{0, 1\}$.

Under the assumption that the noise is Gaussian, the sampled outputs of the envelope detectors r_0 and r_1 are Rician or Rayleigh distributed depending on which of the two signals $s_0(t)$ and $s_1(t)$ is transmitted.

Under hypothesis H_0, the probability density function $p(r_i \mid H_0)$ of the amplitude of the signal r_i with $i \in \{0, 1\}$ is

$$p(r_0 \mid H_0) = \frac{2r_0}{\sigma_0^2}\, I_0\left(\frac{2r_0 a_0}{\sigma_0^2}\right) \exp\left(-\frac{r_0^2 + \mu_0^2}{\sigma_0^2}\right),$$
$$p(r_1 \mid H_0) = \frac{2r_1}{\sigma_1^2} \exp\left(-\frac{r_1^2}{\sigma_1^2}\right). \tag{7}$$

Under hypothesis H_1, the probability density function $p(r_i \mid H_1)$ of the amplitude of the signal r_i with $i \in \{0, 1\}$ is

$$p(r_0 \mid H_1) = \frac{2r_0}{\sigma_0^2} \exp\left(-\frac{r_0^2}{\sigma_0^2}\right),$$
$$p(r_0 \mid H_1) = \frac{2r_1}{\sigma_1^2}\, I_0\left(\frac{2r_1 a_1}{\sigma_1^2}\right) \exp\left(-\frac{r_1^2 + \mu_1^2}{\sigma_1^2}\right), \tag{8}$$

where $\mu_0 = \int_0^T s_0(t)^2 dt$ and $\mu_1 = \int_0^T s_1(t)^2 dt$. $I_0(\cdot)$ is the modified Bessel function of the first kind of order 0.

Assuming the symbols $\{+1, -1\}$ to be transmitted with the same probability and to deal with independent noises n_0 and n_1 (typical in the S-FSK modulation), the maximum likelihood (ML) decision turns out to be the optimum decision rule [10].

In particular, the decision rule uses the following decision values:

$$p(r \mid H_0) = p(r_0 \mid H_0) p(r_1 \mid H_0),$$
$$p(r \mid H_1) = p(r_0 \mid H_1) p(r_1 \mid H_1). \tag{9}$$

The decision rule is to compare likelihood functions and choose the largest:

$$\text{detect } 0 \; p(r \mid H_0) \gtrless p(r \mid H_1) \text{ detect } 1. \tag{10}$$

3.3. Improved ML S-FSK Receiver. Implementation of the ML receiver is difficult due to the complexity of formulae from (8) to (9). An improved method of estimating log-likelihood metric is proposed for a practical realization.

In order to describe the receiver, the log-likelihood ratio $l_i(r_i)$ of the signal r_i is introduced:

$$l_i(r_i) = \log\left(\frac{p(r_i \mid H_1)}{p(r_i \mid H_0)}\right). \tag{11}$$

Using the distributions (8)–(9), (11) can be simplified into the following equation:

$$l_i(r_i) = (2i - 1)\left(\log\left(I_0\left(\frac{2r_i\mu_i}{\sigma_i^2}\right)\right) - \frac{\mu_i^2}{\sigma_i^2}\right). \tag{12}$$

Logarithm and Bessel function are approached using approximating function. Let $g(\cdot)$ be a piecewise linear approximation of the composed function $\log(I_0(\cdot))$ defined as

$$g(X) = A_j X + B_j. \tag{13}$$

The approximation is defined over M intervals $I_1, I_2, \ldots, I_M$. A_j and B_j are calculated by imposing $g(\cdot)$ to be equal to $\log(I_0(\cdot))$ on the boundary of each interval that defines the piecewise approximation:

$$g(X) = \log(I_0(X)) \quad \text{with } X \in \{0, 2^1, 2^2, \ldots\}. \tag{14}$$

Using (14) in (12), an approximated estimation of the loglikelihood $l_i'(r_i)$ ratio is obtained with the equation:

$$l_i'(r_i) = (2i - 1)\left(g\left(\frac{2r_i\mu_i}{\sigma_i^2}\right) - \frac{\mu_i^2}{\sigma_i^2}\right). \tag{15}$$

The proposed receiver decides accordingly to (10) on the following decision values:

$$p(r \mid H_1) = l_1'(r_1), \qquad p(r \mid H_0) = l_0'(r_0). \tag{16}$$

Assuming to have knowledge of the first P symbols creating the Preamble (alternative 1 and 0 symbols), the channel and noise parameters may be estimated using the signals (6) as follows:

$$\widetilde{\sigma}_0^2 = \frac{2}{P} \sum_{k \in H_1} r_0(k)^2, \qquad \widetilde{\sigma}_1^2 = \frac{2}{P} \sum_{k \in H_0} r_1(k)^2,$$
$$\widetilde{\mu}_0^2 = \left| -\widetilde{\sigma}_0^2 + \frac{2}{P} \sum_{k \in H_0} r_0(k)^2 \right|,$$
$$\widetilde{\mu}_1^2 = \left| -\widetilde{\sigma}_1^2 + \frac{2}{P} \sum_{k \in H_1} r_1(k)^2 \right|. \tag{17}$$

3.4. Simulations' Results. The performance of different receiver is compared through communication schema implementation using Matlab. A packet-based transmission has been adopted, with preamble length P equal to 32 and

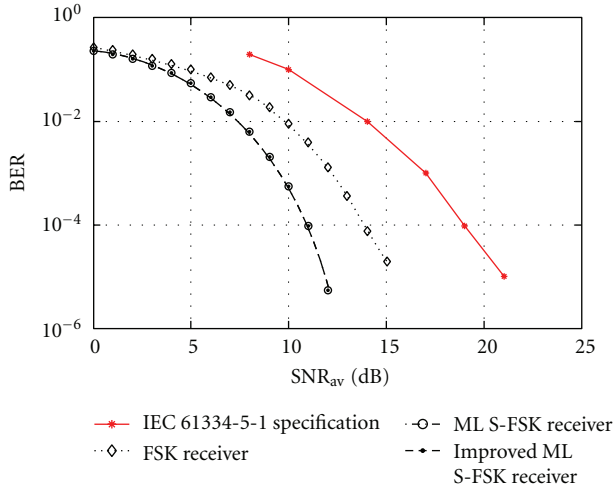

Figure 4: BER versus SNR$_{av}$ with $x = 5$ dB.

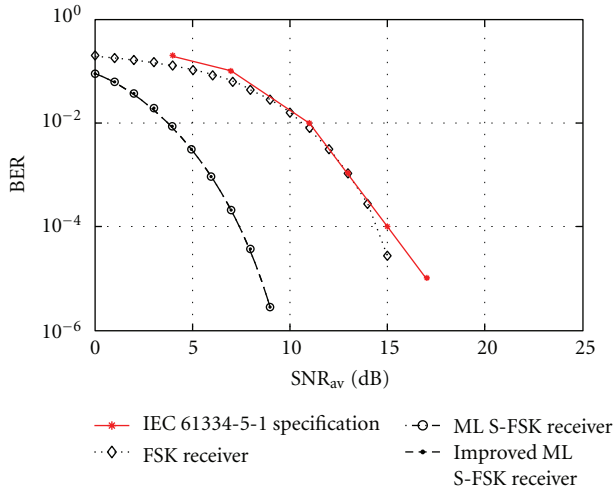

Figure 5: BER versus SNR$_{av}$ with $x = 10$ dB.

a payload of 304 random bits. The following curves are averaged over 1000 packets.

Figures 4, 5, and 6 show the bit error rate (BER) versus the average signal-to-noise ratio SNR$_{av}$ for three unbalancing factors $x \in \{+5, +10, +20\}$ dB.

From the previous figures, the FSK receiver loses in performance with the increasing of the unbalancing factor; however, the ML S-FSK receiver presents relevant improvement on balanced channels. For bit error rate equal to 10^{-4}, more than 6 dB gain at $x = 10$ dB.

For $X \in [0, 256]$ this approximation guarantees a mean square error lower than 10^{-3}, which is adequate to obtain negligible loss of performance between the ideal ML S-FSK receiver and the improved ML S-FSK receiver.

4. DSP Implementation Methodology

Priority in design was given to modularity, simplicity, low cost, and reliability. A 32-bit-fixed point general purpose DSP architecture is considered to optimize the software

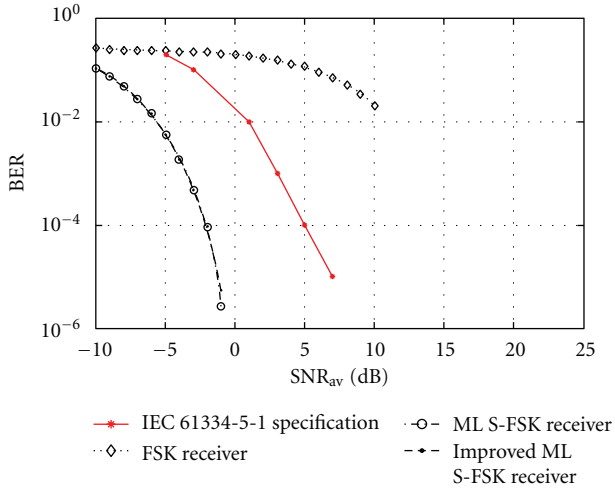

Figure 6: BER versus SNR$_{av}$ with $x = 20$ dB.

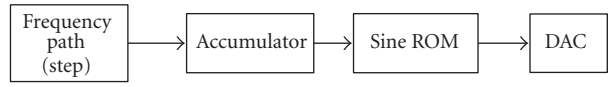

Figure 7: Modulator block diagram.

implementation of the S-FSK receiver. The DSP-based digital part communicates, through serial port in full duplex, with the host device. At the other end, DSP communicates, in half-duplex, through power line via a mixed front end coupling interface.

The DSP programming structure was defined to handle in real-time transmitting or receiving S-FSK signal.

The S-FSK base-band modem is obtained by the implementation of an S-FSK modulator at the transmitter side and an improved ML receiver at the receiver one.

4.1. Modulator Implementation. The transmitter is composed by three stages:

(i) a numeric stage involving a DSP that performs frequency synthesizing with a direct digital synthesizer (DDS);

(ii) a digital to analog convertor (DAC) capable to generate a linear signal up to its full scale output;

(iii) line driver delivering amplified signal.

As described in Figure 7, DDS is based on storing the samples of a sinusoidal signal in a look-up table (LUT) and to read it by a specified integer step index which determines the phase increment, in order to generate the desired frequency f_i which is related to the step index k, the sampling frequency f_s and the LUT length N by the following relation:

$$f_i = \frac{k f_s}{N}. \tag{18}$$

It is important to minimize the LUT size since the implementation will be done in an embedded processor where the resources especially the memory size are limited.

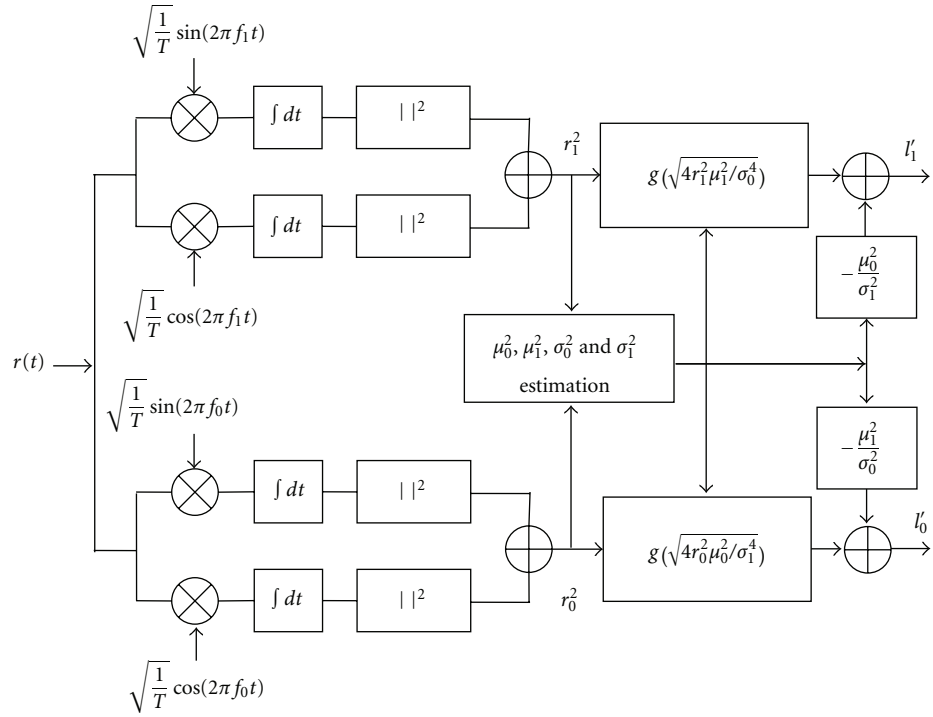

Figure 8: Implemented improved ML S-FSK receiver architecture.

The sampling frequency f_s is chosen as multiple of the data rate $1/T$, thus the number of samples in a bit period is an integer.

Once the appropriate sine samples are read they serve as input for the DAC. The generated signal by the DAC pin is amplified by the line driver.

The S-FSK modulator generates signal in the CENELEC band from 3 kHz to 95 kHz responding to the following specifications:

(i) frequency bandwidth $2\Delta f > 10$ kHz and multiple of bit rate D;

(ii) programmable bit rate D;

(iii) frequencies f_0 and f_1 are multiple of $D/2$.

The sampling frequency f_s is fixed at 3.125 MHz and the samples' number is set to 320 samples to optimize the error performance at the demodulator side. Therefore, the data rate is equal to 9.6 kbps.

The step index k is an integer; therefore, the resolution frequency is found by setting $k = 1$,

$$f_{\text{res}} = \frac{f_s}{N}. \tag{19}$$

Resolution frequency is set to 4.8 kHz to respect orthogonality constraint between two frequencies f_0 and f_1.

The minimum LUT lengths that satisfy the conditions already cited and the generation of the frequencies f_0 and f_1 with zero error are 656.

In Table 1, we present the possible choice of orthogonal frequency f_0 and f_1 in the case of S-FSK demodulator at baud rate 9.6 kbps.

Table 1: Orthogonality frequency choice for baud rate 9.6 kbps.

CENELEC band	Frequency (kHz)		Carrier frequency (kHz)
	f_0	f_1	
A band	91.2	72	81.6
	86.4	67.2	76.8
	81.6	62.4	72
	76.8	57.6	67.2
	72	52.8	62.4

4.2. Improved ML Receiver Implementation. Coherent FSK signals can be noncoherently demodulated to avoid the carrier recovery. The improved ML demodulator is a quadrature receiver capable of detecting signals with unknown phases.

It can be implemented with four correlators as shown in Figure 8, where the four reference signals are $\sin(2\pi f_0 t)$, $\cos(2\pi f_0 t)$, $\sin(2\pi f_1 t)$, and $\cos(2\pi f_1 t)$. We will use the same DDS module as the modulator one to generate those reference signals.

The signal consists of an in-phase component and a quadrature component. Thus, the signal is partially correlated with $\sin(2\pi f_i t)$ and partially correlated with $\cos(2\pi f_i t)$. Therefore, we use two correlators to collect the signal energy in these two parts.

The first P outputs are used to estimate channel parameters. Then, we apply probability function (15) to correlator output using estimated channel parameters and g function. The g function is a piecewise linear approximated and stored in data memory.

All samples of received bits are processed according to Figure 8. The main constraint in the receiver is to tune the sampling frequency of ADC f_{ADC} so as to have

$$\frac{f_s}{f_{ADC}} = M. \tag{20}$$

Different configurations are possible; we have to choose the one that maximizes f_{ADC}. In this case M is equal to 2 and the ADC sampling frequency f_{ADC} becomes equal to 1.565 MHz.

Thus, samples' count during bit time T is 160 samples. The number of samples per symbol period T must be multiple of 8 for direct memory access (DMA) use that offer transfer facility and rapidity.

4.3. Implementation Results. The DSP processor BF506F, sited to an evaluation board [11, 12], operates with frequency up to 400 MIPS with 32 Kbytes of L1 memory associated to instructions (L1_code), 32 Kbytes for data (L1_data) accessed at full processor speed, and 32 Mbytes of external flash memory.

To evaluate the complexity of the S-FSK modem software, it is important to determine the consumed cycles and the consumed data memory space [13].

We have used the data memory to store the LUT table that contains 656 samples encoded on 16 bits.

g function is stored also on data memory space. g function is defiened over 8 intervals and the affinity coefficients are encoded on 16 and 32 bits.

The cycles' consumption is limited by the available number of cycles per sample that is governed by the DSP speed which is 400 MIPS.

The DDS algorithm consumes only 2 cycles per sample, one cycle for memory access to read the sample from the LUT, and one cycle for incrementing the reading index. The transfer of DDS samples to DAC convertor requires 10 cycles per sample.

At the receiving site, the demodulator invokes 4 correlators. At each correlator, one sample is treated on 4 cycles to read, multiply, accumulate, and update index.

Finally, we apply g function on correlators' output at the end of symbol reception.

The cycle's consumptions per sample of these different modules are presented in Table 2. It is important to report that additional modules are implemented to ensure synchronization, build packets, and handling different events.

The cycle's consumption of the S-FSK modem software composed of the modulator, demodulator, and PHY layer functionalities according to IEC 61334-5-1 is lower than the available cycles per symbol period T.

By considering the DSP implementation, we measured an average cycles consumption of 9076 cycles during transmission (21.78% of available cycles) and 9232 cycles during reception (22.15% of available cycles).

Memory consumption is 10.25% for data memory and 45.17% for code memory.

Table 2: Memory and processing time analysis results for the PLC-modem DSP implementation.

Module	PM space (16-bit Word)	DM space (16-bit Word)	Number of cycles machine during T
Modulator module	1620	656	3840
ADC reception module	1066	160	1280
Correlation module	246	656	2560
S-FSK decision module	87	32	156
Initialization PHY module	513	10	2323
PHY layer FSM module	3869	822	5236

The physical layer is designed and implemented. The remaining available cycles and memory will be used to build upper layers: MAC layer and Application layer.

5. Conclusions

In this paper, we have described the design and optimized DSP implementation of an S-FSK profile for a PLC node in an AMR system. To overcome power line channel condition, an improved ML S-FSK receiver is used. Improved receiver presents close error performance to the ideal ML S-FSK receiver but has simplifier architecture.

Analysis of new receiver reveals excellent results in terms of memory occupations, required cycles, and BER performances.

Data rate of 9.6 kbps is easily provided with flexibility and programmability to change receiver parameters.

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