Graphene nanoribbons with zigzag and armchair edges prepared by scanning tunneling microscope lithography on gold substrates

P. Nemes – Incze[1,2,*], Levente Tapasztó[1,2] , G. Zs. Magda[1,2] , Z. Osváth[1,2], G. Dobrik[1,2] , X. Jin[2,3], C. Hwang[2,3], L.P. Biró[1,2]

1 Institute of Technical Physics and Materials Science, Centre for Natural Sciences, 1525 Budapest, PO Box 49, Hungary

2 Korean-Hungarian Joint Laboratory for Nanosciences (KHJLN), P.O. Box 49, 1525 Budapest, Hungary

3 Center for Nano-metrology Division of Industrial Metrology Korea Research Institute of Standards and Science, Yuseong, Daejeon 305-340, South Korea

Abstract

The properties of graphene nanoribbons are dependent on both the nanoribbon width and the crystallographic orientation of the edges. Scanning tunneling microscope lithography is a method which is able to create graphene nanoribbons with well defined edge orientation, having a width of a few nanometers. However, it has only been demonstrated on the top layer of graphite. In order to allow practical applications of this powerful lithography technique, it needs to be implemented on single layer graphene. We demonstrate the preparation of graphene nanoribbons with well defined crystallographic orientation on top of gold substrates. Our transfer and lithography approach brings one step closer the preparation of well defined graphene nanoribbons on arbitrary substrates for nanoelectronic applications.

1. Introduction

Graphene has been in the forefront of nanoscience research ever since the experimental observation that the charge carriers in this material are relativistic Dirac quasiparticles [1–3]. Research into the application of graphene has also been accelerated [4,5], with the goal of harnessing its electronic properties, particularly the high charge carrier mobility [6,7]. High frequency analog transistors have already been realized in graphene layers grown on top of SiC single crystals [8]. However, the application of graphene in nanoelectronic devices, particularly as active elements in digital – logic circuits still needs a lot of innovation on multiple fronts [5]. The most challenging aspects of this research can be addressed on two fronts. Firstly, we need to be able to prepare graphene on a large

* Corresponding author
email: nemes.incze.peter@ttk.mta.hu

scale, with good control over the quality of the graphene crystal, having low defect concentration and overall homogeneous properties [9,10]. Secondly, the properties of the graphene layer need to be modified most importantly to open a band gap [11,12], while keeping the good charge transport properties of the material. Tuning the properties of graphene and inducing a band gap can be achieved by confining the charge carriers along one direction in the graphene plane. However, due to Klein tunneling this can not be achieved as in the case of conventional two-dimensional electron gases by using electrostatic gating [13]. To achieve confinement we have to physically pattern graphene into stripes of a few nanometers in width, creating graphene nanoribbons (GNR) [14,15]. The properties of GNRs are sensitive to the width of the nanoribbon and the crystallographic orientation of the edges [14], with armchair type nanoribbons having a band gap that scales with the width of the ribbon and GNRs having zigzag edges predicted to have magnetically ordered edge states [16]. However, disorder at the edges of the GNR – unavoidably associated with current e-beam lithography methods – can suppress the edge specific properties of the nanoribbon [17–20]. Therefore we need good control over the nanoribbon width, crystallographic orientation and importantly the disorder at the ribbon edges has to be kept to a minimum. Various methods have been employed to prepare nanoribbons [21], from electron beam lithography, “unzipping” of carbon nanotubes, etching by metallic nanoparticles, carbothermal etching, etc. [20,22–25] The GNR preparation technique, which balances all the above requirements is scanning tunneling microscope lithography (STL) [12].

Due to its two-dimensional nature, graphene can be easily investigated by scanning probe methods, especially scanning tunneling microscopy (STM) [26]. In addition to giving us insight into the rich physics of graphene, such local probes can also be employed in the patterning of graphene layers [12,27]. Specifically, Tapasztó et al. have shown that graphene nanoribbons [12] and other graphene nanostructures [28] can be created on the surface of graphite (HOPG) by STL. STL relies on the oxidation of graphene, in a somewhat similar fashion as anodic oxidation by conductive AFM [21,27]. The great advantage of STL is that, whereas in the case of AFM the conductive channel where the oxidation takes place is comparable to the size of the water meniscus formed around the AFM tip, in the case of STL it scales with the width of the channel in which the majority of the tunneling current flows. The meniscus size in the case of AFM scales with the tip radius of curvature, which is 10 – 20 nm [21], while for STM most of the tunneling current is localized in a channel with lateral dimensions comparable to atomic distances [29]. As and additional advantage, the depth of the cut, can be fine tuned by the tunneling conditions [28].

Controlling the width and crystallographic orientation of the nanoribbons can be achieved, along with the possibility of creating hybrid structures, such as zigzag – armchair nanoribbon junctions. These nanoribbons show very low edge roughness resulting in Fabry – Perot-like electron interference patterns and armchair nanoribbons showing band gap opening, which scales with the ribbon width [12]. However, the top layer of graphene on graphite is not electronically decoupled from the bulk. For STL to be truly useful in creating crystallographically oriented graphene nanostructures it needs to be performed on a single layer of graphene, on a surface which does not perturb the Dirac fermion nature of the charge carriers. In this paper we present the next step in STM patterning of graphene layers by performing STL on chemical vapor deposition (CVD) grown graphene.

2. Experimental details

Graphene layers were prepared by CVD on polycrystalline copper foils, according to a procedure described elsewhere [30]. Briefly, copper foils were loaded inside a furnace under H_2 gas and annealed for 30 minutes at 1000^{o}C. After the annealing step, the growth of graphene was carried out in a mixture of H_2 and CH_4 gases. After the growth phase the sample was cooled to room temperature with a cooling rate of 50 K/min. The etching solution used for transferring the graphene layers from the copper surface was made up of 20% $CuCl_2$ in a water : HCl mixture, 4:1 volume ratio. STL was carried out under ambient conditions, using a Nanoscope III STM microscope from Bruker (formerly Veeco). During the STL step, the STM tip – sample bias was set to 2 – 2.6 V and the tip was moved in the desired pattern with a speed of 1 nm/s. Gold on mica substrates were purchased from SPI supplies. For imaging, the typical STM measurement parameters were 500 pA tunneling current and 100 mV bias voltage.

3. Results and discussion

Since both the patterning and initial characterization of the GNRs is done by STM, STL needs an electrically conductive support for the graphene. In the case of graphene layers supported on an insulator, such as SiO_2, if we cut away the graphene by STL we expose a region of insulating layer to the scanning STM tip, which can cause the imaging to be unstable and subsequently can damage the delicate GNRs prepared in the lithography step. For this reason STL has to be performed on graphene supported on an electrically conductive substrate. The most obvious candidate in for this is graphene prepared on a copper surface by CVD [9,30], which is a promising method to grow high quality graphene layers on a large scale. Furthermore, graphene can now be routinely transferred

from the initial copper surface to arbitrary substrates [31,32], raising the possibility of transferring the STL prepared nanostructures to insulating surfaces for further characterization.

After graphene growth by CVD, we have loaded the copper foil with the graphene layer on top into the sample bay of the STM. The surface of the sample shows a series of steps, which form on the surface of the copper crystallites (see Figure 1a). The atomic steps can be 100 nm or wider in certain regions and are atomically smooth, providing an ideal surface to perform STL. Applying the typical parameters used in the case of STL on graphite [12,28], we have been able to cut the graphene layer on top of the copper substrate. However, almost immediately after the lithography step, one can observe the deformation of the graphene layer next to the STL cut, with the graphene at the cut edges rising up to a few nanometers (see Figure 1b). This deformation gets bigger over time, growing in size and finally results in the STM image being unstable in the region. We attribute this topographic rise to the diffusion of oxygen and ambient water into the graphene copper interface through the STL cut in the graphene, leading to the oxidation of the copper surface [33]. It is clear from this experiment that the graphene on copper is not suitable for STL, because the oxidation of the surface would damage any GNR or graphene nanostructure that we prepare. In order to achieve our goal we need to transfer the graphene layer from the copper onto a different conductive substrate. A good candidate for this is gold.

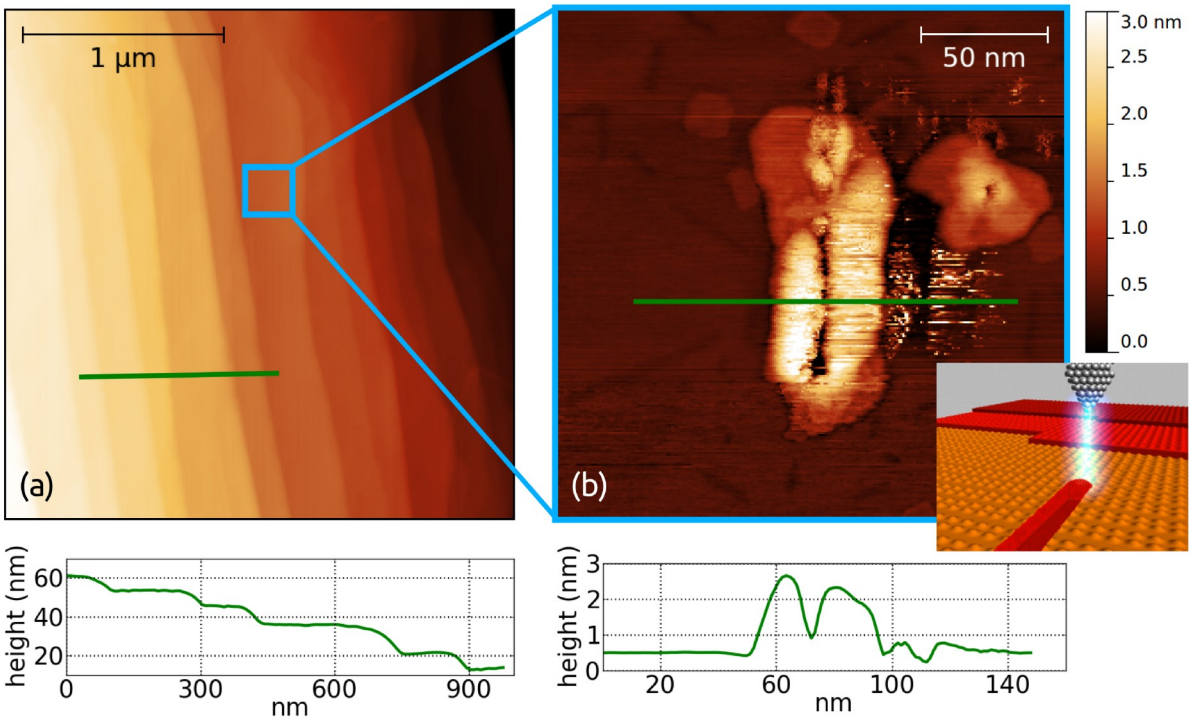

Figure 1. ***(a)*** *STM image of the stepped structure of the copper surface, with CVD graphene on top.* ***(b)*** *STM image of a cut in the surface of graphene. After the lithography step, the copper surface underneath almost immediately starts to oxidize, leading to a rise in the topographic height of the surface around the cut. Height profiles along the green lines can be seen below the STM images.*

Gold does not oxidize in the presence of oxygen and water, which are required for STL [12,27] and gold does not perturb the linear bands of graphene near the K points [34]. Furthermore, gold surfaces can be prepared to have large atomically flat terraces, making it a good candidate substrate. If it is thermally evaporated onto freshly cleaved mica, gold grows in an epitaxial manner and forms large atomic terraces [35]. In order to use this surface as a substrate for graphene, the gold has to be stripped off the mica surface. The sample preparation procedure can be seen in Figure 2. In the first step, a piece of silicon wafer is glued to the top of the gold by epoxy. After the epoxy has cured, the gold can be peeled off the mica surface by carefully lifting the edges of the silicon wafer with tweezers. The gold surface which was in contact with the mica can then be used as an atomically flat substrate to transfer graphene. In this way the sample will be smooth enough to allow STL. By contrast the surface of evaporated gold has a roughness on the nanometer scale.

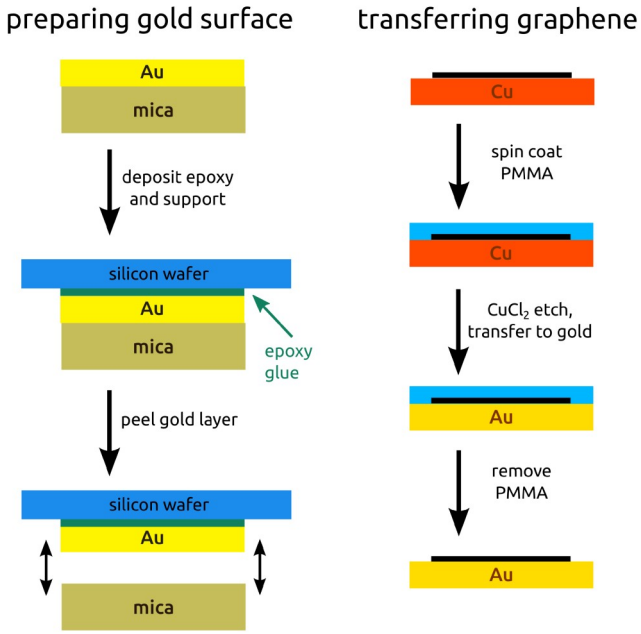

Figure 2. Preparing the gold surface and transfer of CVD graphene onto the gold.

For the transfer process, graphene was first capped by a PMMA layer and was placed on the surface of the etching solution. After the copper has been removed, the PMMA film was transferred onto DI water to remove the $CuCl_2$ residues. The PMMA with the graphene layer was then removed from the water surface by the previously prepared gold substrate. The PMMA was etched away by rinsing the sample in acetone.

The transferred graphene layer adheres to the gold surface, displaying wrinkles in certain regions (see Figure 3a), which is a result of the high temperature growth process and wet transfer [36]. The atomically flat terraces of the gold surface can be used to cut the graphene layer by STL. Figure 3 shows various GNRs prepared by STL. In a first step, the surface is imaged in atomic resolution, which is necessary to orient the STL cutting of the nanoribbon edges. After revealing the armchair and zigzag directions of the graphene surface, the STM tip is moved across the surface in the given direction, with a speed of 1 nm/s and a bias voltage of 2-2.6 V. The magnitude of the required bias voltage is dependent on the ambient humidity and it is carefully raised until the etching of the graphene under the tip is observed [21,27], this insures a smooth cut. Nanoribbons with both armchair and zigzag edges have been prepared, as can be seen in Figure 3, with the inset showing the atomic lattice of graphene and the crystallographic directions.

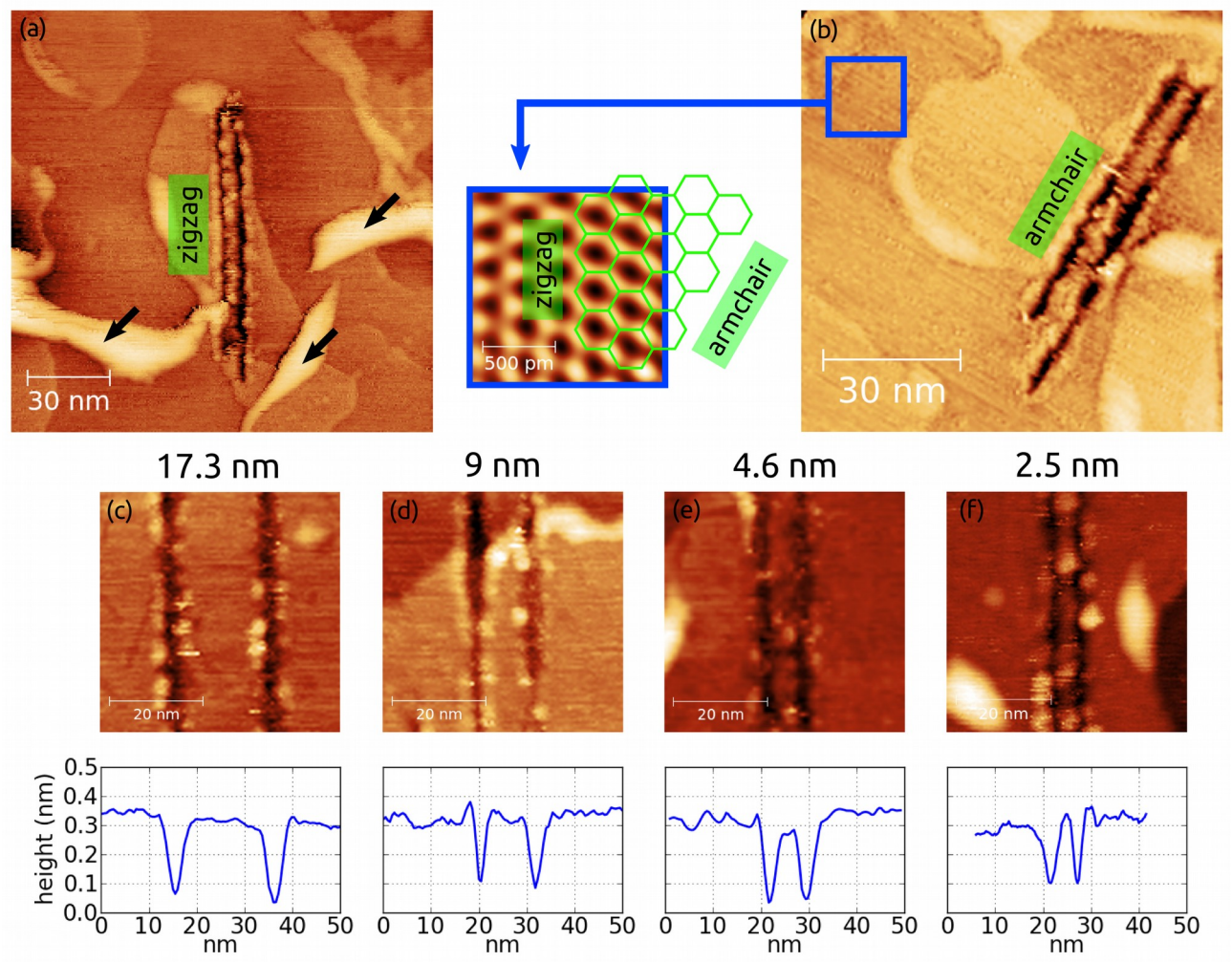

Figure 3. Various nanoribbons cut into the graphene layer on the gold surface. ***(a)*** *Zigzag edged nanoribbon and* ***(b)*** *armchair edged nanoribbon cut by STL. Black arrows show wrinkles in the graphene layer. Inset: atomic resolution image of the graphene surface, showing the zigzag and armchair directions.* ***(c-f)*** *Nanoribbons cut in the zigzag direction, with various widths. Height profiles can be seen beneath the STM topography images.*

A range of GNRs with differing widths can be seen in Figure 3c-f. Because of the high resolution of STL, we have been able to prepare GNRs with a lateral size down to 2.5 nm, which corresponds to roughly 10 benzene rings across. The width of this GNR is equal to the narrowest GNR that we have been able to prepare on top of graphite and it shows that STL can be implemented on single layer graphene just as well as on the top layer of graphite [12]. The roughness of the nanoribbon edges is comparable to the roughness of nanoribbons prepared by us on the top layer of HOPG [12]. The halfwidth of the cut prepared by the STM tip can be considered an upper bound for the edge roughness. Short sections of the nanoribbon can have even smoother edges in which case the roughness is comparable to atomic distances. As reported by us earlier, this low roughness enables the observation of the confinement induced band gap in armchair edged nanoribbons [12], in excellent agreement with theoretical predictions for perfectly smooth edges.

The fact that we have used CVD grown graphene to prepare GNRs, offers us some exciting new opportunities to prepare graphene nanostructures that have never been attempted before. It is well known that CVD grown graphene is not single crystalline and contains grain boundaries [10,37,38]. These structures can be identified by STM [39], thus we have the possibility of incorporating such defects, containing non hexagonal rings into GNRs. Such a nanostructure can be seen in Figure 4, where a nanoribbon was cut across a grain boundary, having a mismatch angle of 15.3°. Such hybrid GNRs have been considered in the literature and can be thought of as a junction of two GNRs with different crystallographic orientation of the edges and are predicted to have exotic properties, such as current rectification and ferromagnetism [40,41].

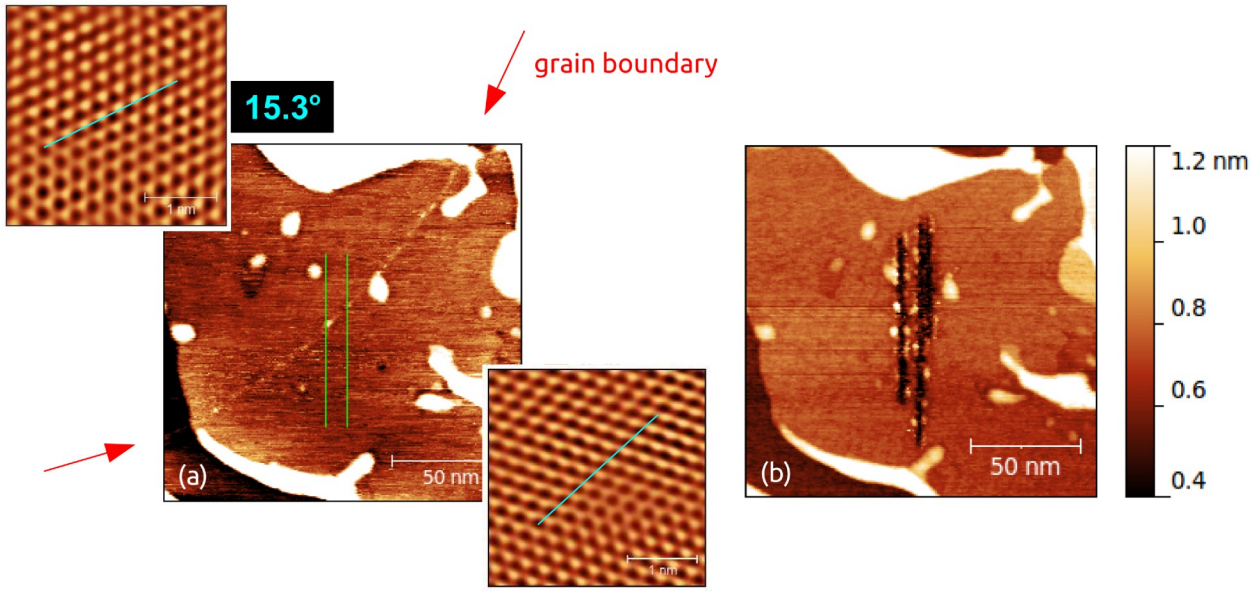

Figure 4. Cutting a GNR across a grain boundary in CVD graphene. The grain boundary was identified by atomic resolution STM measurements, having a mismatch angle of 15.3°. Green lines show the locations where the graphene layers was cut by STL.

4. Conclusions

We have demonstrated STL on single layer graphene transferred to a gold substrate. We have prepared GNRs, having well defined crystallographic orientation and lateral dimensions down to 2.5 nm. Using CVD grown graphene we have shown the possibility of creating graphene nanostructures, with functionality beyond armchair and zigzag nanoribbons. Furthermore, using transfer techniques these nanostructures prepared by STL could be transferred to insulating substrates [32] for further characterization by charge transport measurements.

Acknowledgement

The work in Hungary was supported in part by OTKA grants K101599 and PD 91160, the collaboration of Korean and Hungarian scientists was supported by the KRCF in the framework of the Korean-Hungarian Joint Laboratory for Nanosciences.

References

[1] K.S. Novoselov, A.K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V Dubonos, et al., Electric field effect in atomically thin carbon films, Science (80-.). 306 (2004) 666–9.

[2] K.S. Novoselov, A.K. Geim, S. V. Morozov, D. Jiang, M.I. Katsnelson, I. V. Grigorieva, et al., Two-dimensional gas of massless Dirac fermions in graphene, Nature. 438 (2005) 197–200.

[3] Y. Zhang, Y.-W. Tan, H.L. Stormer, P. Kim, Experimental observation of the quantum Hall effect and Berry's phase in graphene., Nature. 438 (2005) 201–4.

[4] F. Schwierz, Graphene transistors, Nat. Nanotechnol. 5 (2010) 487–496.

[5] K.S. Novoselov, V.I. Fal′ko, L. Colombo, P.R. Gellert, M.G. Schwab, K. Kim, A roadmap for graphene, Nature. 490 (2012) 192–200.

[6] S. Morozov, K. Novoselov, M. Katsnelson, F. Schedin, D. Elias, J. Jaszczak, et al., Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer, Phys. Rev. Lett. 100 (2008) 016602.

[7] A.S. Mayorov, R. V Gorbachev, S. V Morozov, L. Britnell, R. Jalil, L. a Ponomarenko, et al., Micrometer-Scale Ballistic Transport in Encapsulated Graphene at Room Temperature, Nano Lett. (2011).

[8] Y.-M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.-Y. Chiu, A. Grill, et al., 100-GHz Transistors from Wafer-Scale Epitaxial Graphene., Science (80-.). 327 (2010) 662.

[9] Y. Zhang, L. Zhang, C. Zhou, Review of Chemical Vapor Deposition of Graphene and Related Applications., Acc. Chem. Res. (2013).

[10] L.P. Biró, P. Lambin, Grain boundaries in graphene grown by chemical vapor deposition, New J. Phys. 15 (2013) 035024.

[11] L.P. Biró, P. Nemes-Incze, P. Lambin, Graphene: nanoscale processing and recent applications., Nanoscale. 4 (2012) 1824–39.

[12] L. Tapasztó, G. Dobrik, P. Lambin, L.P. Biró, Tailoring the atomic structure of graphene nanoribbons by scanning tunnelling microscope lithography., Nat. Nanotechnol. 3 (2008) 397–401.

[13] K.S. Novoselov, M.I. Katsnelson, A.K. Geim, A.K. Geim, Chiral tunnelling and the Klein paradox in graphene, Nat. Phys. 2 (2006) 620–625.

[14] Y.-W. Son, M.L. Cohen, S.G. Louie, Energy Gaps in Graphene Nanoribbons, Phys. Rev. Lett. 97 (2006) 216803.

[15] K. Nakada, M. Fujita, G. Dresselhaus, M.S. Dresselhaus, Edge state in graphene ribbons: Nanometer size effect and edge shape dependence, Phys. Rev. B. 54 (1996) 17954–61.

[16] Y.-W. Son, M.L. Cohen, S.G. Louie, Half-metallic graphene nanoribbons., Nature. 444 (2006) 347–9.

[17] M.Y. Han, J.C. Brant, P. Kim, Electron Transport in Disordered Graphene Nanoribbons, Phys. Rev. Lett. 104 (2010) 056801.

[18] P. Gallagher, K. Todd, D. Goldhaber-Gordon, Disorder-induced gap behavior in graphene nanoribbons, Phys. Rev. B. 81 (2010) 115409.

[19] B. Özyilmaz, P. Jarillo-Herrero, D. Efetov, P. Kim, Electronic transport in locally gated graphene nanoconstrictions, Appl. Phys. Lett. 91 (2007) 192107.

[20] M.Y. Han, B. Özyilmaz, Y. Zhang, P. Kim, Energy Band-Gap Engineering of Graphene Nanoribbons, Phys. Rev. Lett. 98 (2007) 206805.

[21] L.P. Biró, P. Lambin, Nanopatterning of graphene with crystallographic orientation control, Carbon N. Y. 48 (2010) 2677–2689.

[22] L. Jiao, X. Wang, G. Diankov, H. Wang, H. Dai, Facile synthesis of high-quality graphene nanoribbons., Nat. Nanotechnol. 5 (2010) 321–325.

[23] L.C. Campos, V.R. Manfrinato, J.D. Sanchez-Yamagishi, J. Kong, P. Jarillo-Herrero, Anisotropic etching and nanoribbon formation in single-layer graphene., Nano Lett. 9 (2009) 2600–4.

[24] J. Cai, P. Ruffieux, R. Jaafar, M. Bieri, T. Braun, S. Blankenburg, et al., Atomically precise bottom-up fabrication of graphene nanoribbons, Nature. 466 (2010) 470–473.

[25] P. Nemes-Incze, G. Magda, K. Kamarás, L.P. Biró, Crystallographically Selective Nanopatterning of Graphene on SiO2, Nano Res. 3 (2010) 110–116.

[26] A. Deshpande, B.J. LeRoy, Scanning probe microscopy of graphene, Phys. E. 44 (2012) 743–759.

[27] H. Hiura, Tailoring graphite layers by scanning tunneling microscopy, Appl. Surf. Sci. 222 (2004) 374–381.

[28] G. Dobrik, P. Nemes-Incze, L. Tapasztó, P. Lambin, L.P. Biró, Nanoscale lithography of graphene with crystallographic orientation control, Phys. E. 44 (2012) 971–975.

[29] C.J. Chen, Microscopic view of scanning tunneling microscopy, J. Vac. Sci. Technol. A. 9 (1991) 44.

[30] C. Hwang, K. Yoo, S.J. Kim, E.K. Seo, H. Yu, L.P. Biró, Initial Stage of Graphene Growth on a Cu Substrate, J. Phys. Chem. C. 115 (2011) 22369–22374.

[31] J. Kang, D. Shin, S. Bae, B.H. Hong, Graphene transfer: key for applications., Nanoscale. 4 (2012) 5527–37.

[32] B. Dlubak, P.R. Kidambi, R.S. Weatherup, S. Hofmann, J. Robertson, Substrate-assisted nucleation of ultra-thin dielectric layers on graphene by atomic layer deposition, Appl. Phys. Lett. 100 (2012) 173113.

[33] M. Schriver, W. Regan, W.J. Gannett, A.M. Zaniewski, M.F. Crommie, A. Zettl, Graphene as a Long-Term Metal Oxidation Barrier: Worse Than Nothing, ACS Nano. (2013).

[34] J.M. Wofford, E. Starodub, A.L. Walter, S. Nie, A. Bostwick, N.C. Bartelt, et al., Extraordinary epitaxial alignment of graphene islands on Au(111), New J. Phys. 14 (2012) 053008.

[35] M. Hegner, P. Wagner, G. Semenza, Ultralarge atomically flat template-stripped Au surfaces for scanning probe microscopy, Surf. Sci. 291 (1993) 39–46.

[36] G.-X. Ni, Y. Zheng, S. Bae, H.R. Kim, A. Pachoud, Y.S. Kim, et al., Quasi-periodic nanoripples in graphene grown by chemical vapor deposition and its impact on charge transport., ACS Nano. 6 (2012) 1158–64.

[37] P. Nemes-Incze, K.J. Yoo, L. Tapasztó, G. Dobrik, J. Lábár, Z.E. Horváth, et al., Revealing the grain structure of graphene grown by chemical vapor deposition, Appl. Phys. Lett. 99 (2011) 023104.

[38] P.Y. Huang, C.S. Ruiz-Vargas, A.M. van der Zande, W.S. Whitney, M.P. Levendorf, J.W. Kevek, et al., Grains and grain boundaries in single-layer graphene atomic patchwork quilts, Nature. 469 (2011) 389–392.

[39] L. Tapasztó, P. Nemes-Incze, G. Dobrik, K. Jae Yoo, C. Hwang, L.P. Biró, Mapping the electronic properties of individual graphene grain boundaries, Appl. Phys. Lett. 100 (2012) 053114.

[40] X.-F. Li, L.-L. Wang, K.-Q. Chen, Y. Luo, Design of Graphene-Nanoribbon Heterojunctions from First Principles, J. Phys. Chem. C. 115 (2011) 12616–12624.

[41] J. Zhou, T. Hu, J. Dong, Y. Kawazoe, Ferromagnetism in a graphene nanoribbon with grain boundary defects, Phys. Rev. B. 86 (2012) 035434.