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Monotonic transition based forward body bias for dual threshold voltage low power embedded processors

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Abstract. Dual threshold voltage and forward body bias techniques are effective ways to optimally balance the standby leakage power and performance. In this paper, we propose a novel fine-grained forward body biasing scheme for monotonic static logic circuits. In the proposed scheme, the forward body bias is applied to high threshold voltage of either the pull-up or the pull-down network based on the evaluation transition and the state of operation. This technique improves the low skew NAND and NOR circuit performance by 7% and 11%, high skew NAND and NOR by 8% and 13% respectively. It reduces both active and standby leakage power as compared to monotonic static CMOS with dual-V_T technique. The simulations are carried out using 130 nm mixed mode process technology to validate our proposed technique.

1 Introduction

In nanometer era, leakage power becomes gradually a major portion of the total power consumption in battery powered embedded systems. This increase in leakage power reduces the battery life time in such applications as wireless sensors with high standby to active time ratio (Jayapal et al., 2005a). To best utilize the battery source, both the active and standby leakage power has to be minimized while meeting the performance demands.

Modern CMOS process offers different types of threshold voltages and oxide thickness devices to meet the low power and high performance demands. The low and high threshold device provides high performance at the cost of high leakage and low leakage with low performance respectively. Depending on the application requirements, the designers can make optimal power performance trade-offs. For low standby power applications, dual threshold voltage with power gating reduces the standby leakage power at the cost of performance through traditional static CMOS logic circuits. On the other hand, in case of pass logic circuits an additional input gating is required at both ends of the customized pass logic blocks to reduce the standby leakage power (Jayapal et al., 2005b). To overcome this delay penalty and to reduce the transistor count, the high threshold voltage with forward body bias for improving the performance level has been introduced. The change in threshold voltage due to the bulk source potential is given by

$$\triangle V_t = \gamma\sqrt{2\Phi_F + V_{sb}} - \sqrt{2\Phi_F} \quad (1)$$

where $\gamma =$ body effect parameter, $\Phi_F =$ Fermi potential and $V_{sb} =$ SourceBulkpotential. Recent research reports indicate that the optimal forward body bias (FBB) value of 400–500 mV provides 13% and 37% performance improvement at 130 nm and 90 nm triple well process (Narenda etal., 2003; v. Arnim et al., 2004). This clearly suggests that the efficiency of body bias depends on process technology.

Monotonic Static CMOS circuits provide noise immunity low power and high performance (Solomatnikov et al., 2000), and differ from traditional static CMOS in the way transition are made. In order to have monotonic transitions at the gate outputs, the concept of pre-charge and evaluation mode resembles domino circuits. During the pre-charge mode, each gate output is either charged to V_{DD} or discharged to V_{SS}. In the evaluation mode, the output either stays at its present value or makes a transition depending on the inputs.

The rest of the paper will discuss the limitation of global body bias, the essentials of transition based fine grained FBB and simulation results using monotonic static low and high skewed gates.

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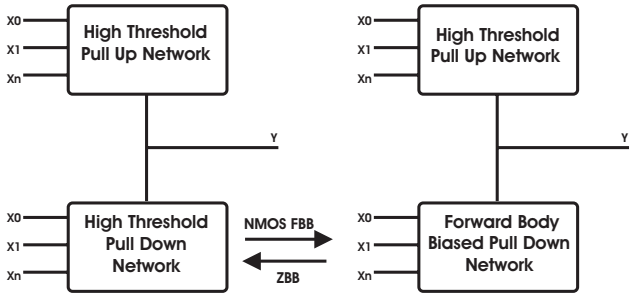

Fig. 1. Transition based fine grained forward body biasing with low skew NMOS body bias.

2 Fine-grained forward body bias

The application of global forward body bias using traditional static CMOS improves the performance at the expense of very high active leakage power. Applying forward body bias to high threshold device increases active leakage power from the non-evaluation transistors. On the other hand, it becomes challenging to place low and high threshold transistors in traditional static CMOS circuits depending on evaluation transitions. To overcome this, we chose monotonic static logic circuits in which placement of dual threshold devices based on evaluation transition becomes easier. However, this technique increases both active and standby leakage power because of static low threshold evaluation transistors. Similarly, applying FBB to the high threshold monotonic static CMOS logic causes more active leakage power similar to the monotonic static CMOS with dual-V_T technique (Thorp et al., 1999). As a result, the increase in active leakage power makes global body bias inadequate for low standby power applications.

We propose a transition based fine-grained forward body bias using monotonic static CMOS to avoid unwanted active leakage with performance improvement as shown in Fig. 1. In the proposed scheme, body bias is applied to high threshold transistors of either the pull-up or the pull-down network depending on the evaluation transitions. In monotonic static circuits, the applied forward body bias increases the transition rate without resizing the evaluation transistors. During active mode, a chosen body bias of 450 mV is applied to the evaluation transistors, which decreases the CV/I delay by increasing the I_{on}. The non-evaluation pre-charge high threshold transistor offers lower active leakage power and the body biased low threshold evaluation transistor contributes performance enhancement. During standby mode, the applied Zero Body Bias (ZBB) brings the body biased evaluation transistor into high threshold state to reduce standby leakage power. Thus, the selective forward and zero body biased evaluation transistor reduces both active and standby leakage power using monotonic property.

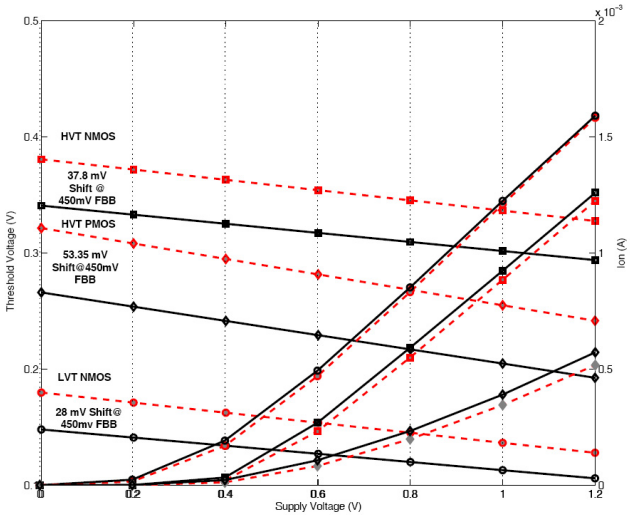

Fig. 2. The variation of threshold voltage and on-current of low and high threshold NMOS and PMOS devices.

Table 1. Threshold voltage variations and leakage currents for different supply voltages

Device under test	$\triangle V_T$ @1.2V VDD	$\triangle V_T$ @400 mV VDD	$\triangle V I_{\text{off}}$ @1.2V VDD	$\triangle V I_{\text{off}}$ @400 mV VDD
HVT NMOS	33.7 mV	37.8 mV	12.62 nA	41.4 nA
LVT NMOS	22 mV	28 mV	0.54 uA	0.268 uA

3 Transition based forward body bias - comparison of power and performance

Dual threshold 130 nm device measurement shows that applying 450 mV body bias to the high threshold NMOS and PMOS increases I_{on} by 3% and 11% at high drain source voltage. At the same time, the I_{on} of low threshold NMOS are virtually identical due to severe Drain Induced Barrier Lowering (DIBL) and V_T rolloff effects as shown in Fig. 2. Thus, the efficiency of body bias decreases with thinner oxide, shorter gate length and smaller V_T. Table 1 shows that the rate of change of threshold voltage with body bias at lower drain source voltage is greater due to reduced DIBL and V_T rolloff. Dual V_T high threshold PMOS measurement shows that the threshold voltage shift with 450 mV FBB is about 1.4x more than those of NMOS devices. As a result, the larger I_{on} from body bias increases robustness of leakage

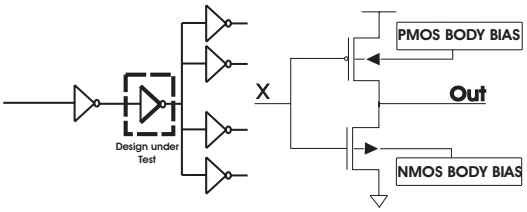

Fig. 3. Fan-out of 4 inverter delay with transition based forward body bias.

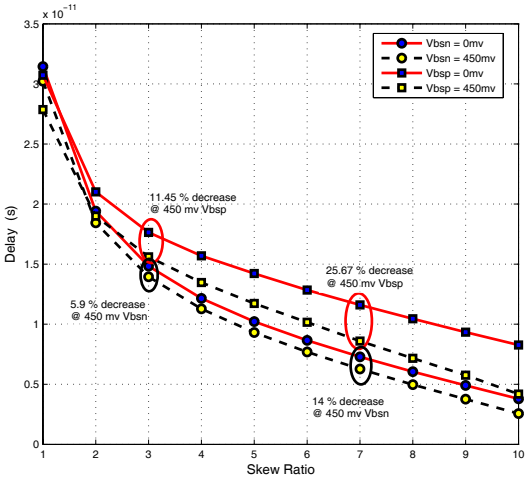

Fig. 4. FO4 Inverter delay variation with 450 mV FBB for various skew ratios.

sensitive circuits such as domino logic and highly skewed static logic gates.

Lower operating temperature improves performance, however the leakage current increase due to 450 mV FBB is about 3.2 x and 4 x at 1.2 V and 0.4 V V_{DS}. Higher temperature offers 2.6 x and 3.1 x increase in leakage current at 1.2 V and 0.4 V V_{DS}. Thus, the leakage current increase due to FBB at lower drain source voltage is slightly more than those of higher V_{DS}, irrespective of operating temperature.

To validate the proposed technique, the fan-out of 4 (FO4) inverter delay as shown in Fig. 3, is designed to compute the performance improvement for both evaluation transitions. Fig. 4 shows that the transition rate due to PMOS body bias has larger CV/I delay reduction compared to those of NMOS body bias. PMOS body bias provides the same CV/I delay with (1-2) x less skew ratio (the ratio between PMOS and NMOS transistor widths) compared to without body bias condition. On the other hand, the NMOS body bias offers the same transition rate with almost 1 x less skew ratio.

4 Monotonic static gates - design considerations

Figure 5 shows the monotonic static CMOS logic gates, each gate is biased to make faster Low to High (L-H) or High to

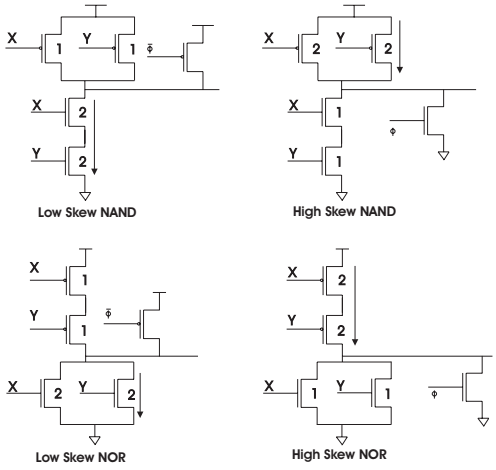

Fig. 5. Monotonic Static CMOS - Low and high skewed gates.

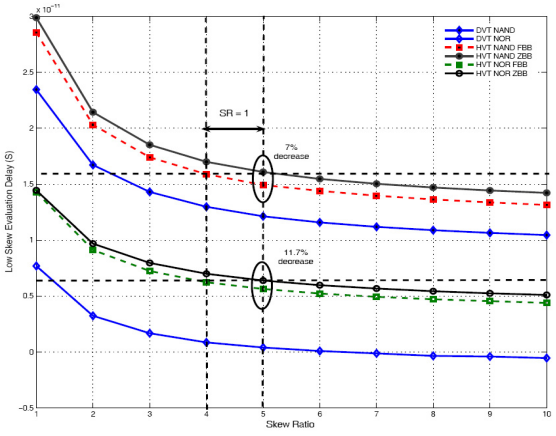

Fig. 6. Evaluation delay of low skewed gates for three different schemes.

Low (H-L) transitions. In general, there are two types of gates such as low skew (LS) gates which have faster H-L transitions and high skew (HS) gates with faster L-H transitions. Since monotonic logic is inherently non-inverting, it must be mapped to a network that does not contain intermediate inversions. This is in contrast to traditional static CMOS which can allow intermediate inverters. To utilize the monotonic property for fine-grained FBB, four different types of basic gates like LS-NAND, LS-NOR, HS-NAND and HS-NOR were chosen. Each skewed gate is analyzed for three different schemes like high threshold with transition based forward body bias, high threshold without body bias and MS-CMOS with dual V_T (low V_T in critical paths and high V_T in non-critical paths) (Thorp et al., 1999) techniques.

Figures 6 and 7 show the evaluation delay and average switching power for LS-NAND and LS-NOR in three different techniques. Like FO4 inverter, the LS-NAND and LS-NOR achieves the same CV/I delay with reduced skew ratio (SR = 1). The parallel connected high fan-in LS-NOR gains

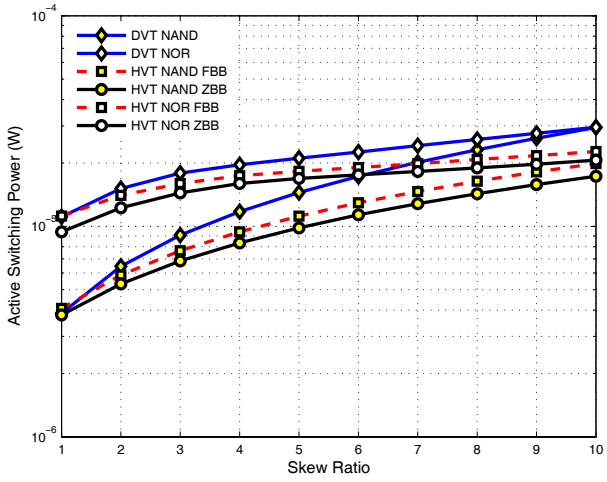

Fig. 7. Average switching power of low skewed gates for three different schemes.

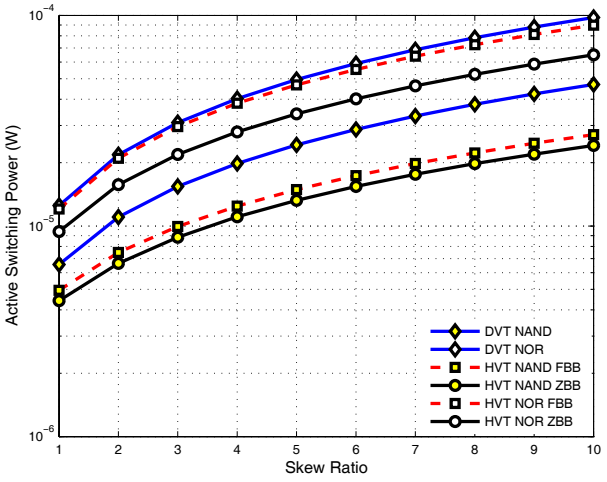

Fig. 9. Average switching power of high skewed gates for three different schemes.

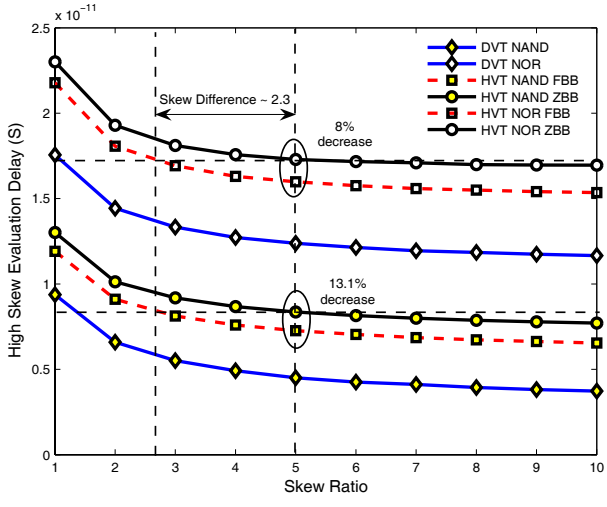

Fig. 8. Evaluation delay of high skewed gates for three different schemes.

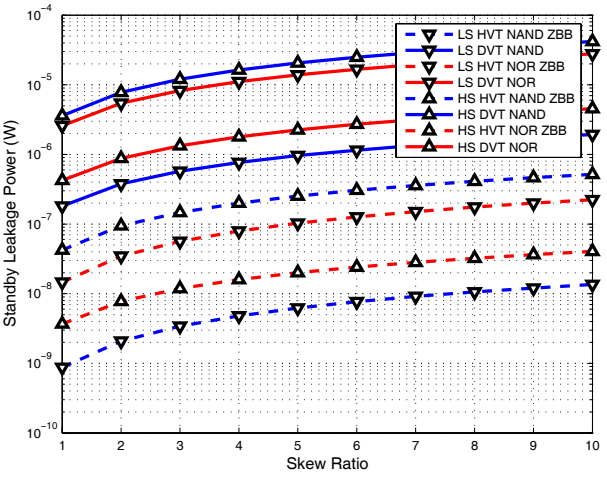

Fig. 10. The worst case standby leakage power of low and high skew gates.

0.67 times more delay reduction than the serial connected LS-NAND gate. The transition based body bias increases the switching power by 13.6% and 7.6% of LS-NAND and NOR gates, which is lower than that of MS-CMOS with dual V_T techniques. Thus, the LS-NOR attains substantial performance gain with marginal increase in switching power using transition based body bias. On the other hand, the switching power increase due to body bias in LS-NAND is greater than that of LS-NOR gate.

Like low skewed gates, the large fan-in HS-NAND PMOS body bias reduces the evaluation delay by 0.6 times than those of HS-NOR gate as shown in Fig. 8. High skewed gates with PMOS body bias achieve the same CV/I delay at reduced skew ratio (SR = 2.3). Thus, PMOS body bias gates achieve additional performance improvement with lower skew ratio than low skewed gates. From Fig. 9, the average switching power of HS-NOR is increased by a factor of 2 when compared to HS-NAND. Transition based forward body biased high skew gate consumes lower switching power than the MS-CMOS with dual V_T skewed gates.

The standby leakage power for both low and high skew gates are computed with worst case input patterns in Fig. 10. Applying Zero Body Bias (ZBB) during standby mode, brings the body biased skew gates to high V_T state. In MS-CMOS with dual V_T technique, the high dynamic and standby leakage power consumptions are mainly due to parallel connected low V_T evaluation transistors. Series connected LS-NAND and HS-NOR consumes lower standby leakage power than that of parallel connected LS-NOR and HS-NAND gates. Thus, the worst case standby leakage power for the proposed scheme is far below the MS-CMOS with dual V_T technique.

5 Conclusion

Transition based fine grained forward body bias using monotonic property has been proposed. The proposed fine-grained body bias scheme provides the same circuit performance with reduced skew ratio for both low and high skew gates. This method consumes lower dynamic and standby leakage power than MS-CMOS with dual V_T technique.

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