DESIGN-FOR-TEST OF MIXED-SIGNAL INTEGRATED CIRCUITS

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Outline

Introduction:

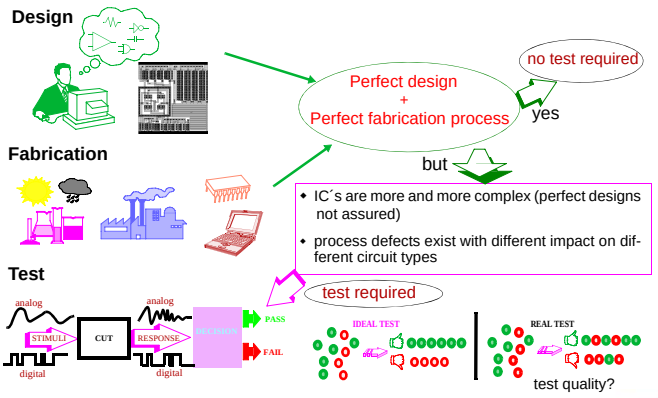
- Main test concepts
- Tecnology Trends
- Design-for-test: a must for present electronic systems?

Functional Test for Mixed-signal ICs:

- Circuit classes and metrics
- Test-on-Chip: signal generation & response acquisition
- TEST& BIST approaches

Structural Test for Mixed-signal ICs

Main steps in ICs realization



What does Test mean?

- **Testing (in general) is the process of verifying that an IC meets the specs for what it was designed**
- **Testing (alternative) is the process of verifying that the intended behavior of an IC is not affected by a defect**

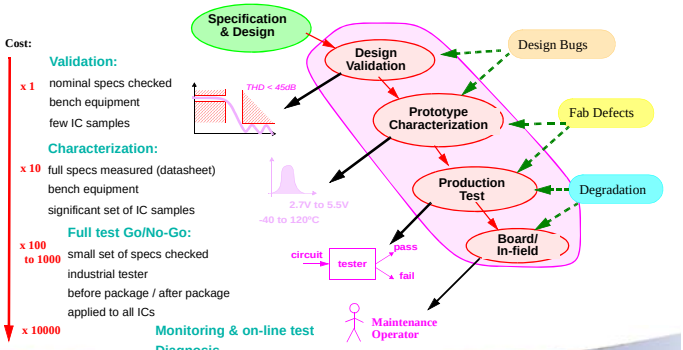
General causes for IC fail:

- Design Mistakes
  - Human Errors
  - Modelling Oversimplifications
  - Design Rules Violations
- Fabrication Flaws
  - Process fluctuations, mask misalignment
  - Spot defects
  - Handling & Finishing problems
- Operation Damages
  - Ageing
  - Mechanical Breaks
  - Thermal Stress
  - Electrical Influences
  - Environmental Changes

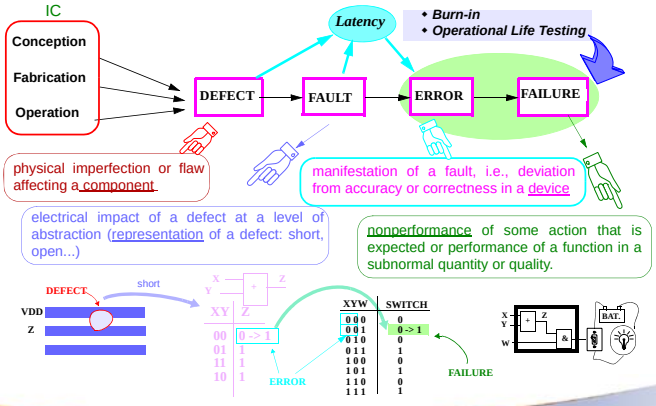
Conception
Fabrication
Operation

Test Types

❑ **Depending on the product lifetime testing procedures are different, and have different goals and costs**



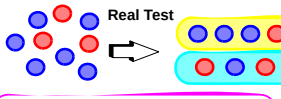
Defects and their effects



Yiel & IC Product Quality

Test Importance (in general):

- ICs are more and more complex (design not fully simulated)
- Time-to-Market is conditioned by Test Speed/Quality
- Test Cost (test time) is dominating in many Products
- Quality Enhancement is driven some Markets
- Present Quality Figures decreased (500 ppm ---> 1 ppm)



defect-free+escapes

$$Manufacturing\ Yield = \frac{number\ of\ defect-free}{total\ manufactured}$$

$$Defect-level = \frac{number\ of\ escapes}{total\ passed}$$

Test Quality: minimum test escapes

Product Quality: maximum Yield and minimum Defect-level

More on Yield & Product Quality

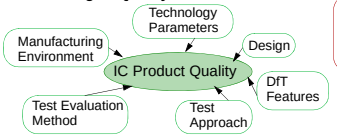
Process Yield:
Referred to the Number of Good Fabricated Circuits

$$Y_F = \frac{Fabricated - Good}{Fabricated}$$

Test Yield:
Referred to the Number of Correctly Tested Circuits

$$Y_T = \frac{Tested - Correct}{Tested}$$

Factors affecting IC Quality:



The quality level can vary greatly depending on the type of failures occurring and the type of failures targeted by the test approach

relation between faults modeled and yield is needed

Improving quality could mean more inprovements in test coverage than in manufacturing yield

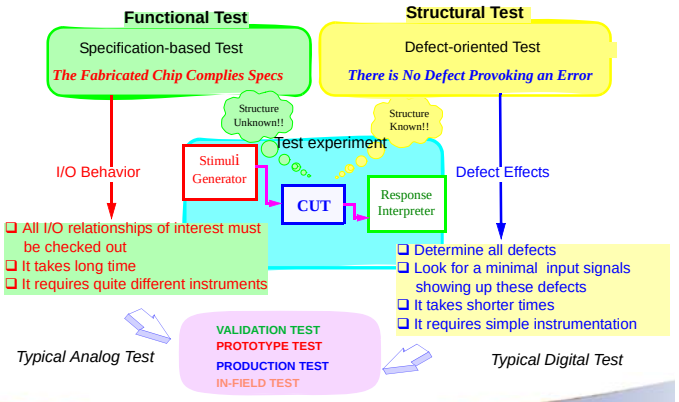
Some models for Quality Level:

$$QL = Y^{(1-T)}$$

$$QL = 1 - \frac{(1-T)(1-Y)e^{-(n-1)T}}{Y + (1-T)(1-Y)e^{-(n-1)T}}$$

T: Test Coverage=modeled faults detected/modeled faults
Y: Manufacturing Yield= defect-free parts tested/parts tested
n: average of faults per faulty part

Two Test Approaches



Yield & PQ for Structural Tests

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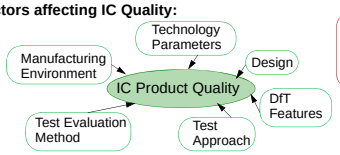

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Outline

Tecnology Trends

Technology Trends

Semiconductor industry is changing: fabless companies growth

- many agents to have care of IC yield, quality and reliability (IP providers, designers, fabs)

System-on-chip (SoC) designs are increasing

- emerging failure mechanisms
- different cores with different modelling, different test requirements and different tester lenguajes
- more to test, less test access (less pin/device): yield losses

New Failure and Yield analysis challenges

- increasing metals and circuit complexity lead to reduction of the traceability of signals: more complex monitor structures
- increasing wafer size and process variations across wafer

Technology Scaling and the Cost of Test

- manufacturing cost reduces for each technology generation but test cost remains almost constant: test cost will dominate product cost
- tester speeds not growing as chip speeds

Design-for-Test: a solution?

***Design-for-Test* (DfT): any method of improving the testability of a circuit by design**

Why to enhance Testability?

- **Decreasing Test Time/Cost**
- **At-Speed Testing**
- **Alleviating Tester Limitations**
- **Reducing External Interfaces**
- **Providing Periodic Re-Testing**
- **Helping Maintenance**
- **Increasing Long-term Quality**

How to enhance Testability?

- Reducing Defect Probability
- Optimizing/simplifying the Test Process
- Re-designing the Circuit (or some parts) to support easier measurements
- ProvidingTester Functions into Chips (BIST)
- Using Circuit Properties to Decrease Test Cost
- Re-configuring the Chip to Speed-up the Test or to test other parts

Mixed-signal DfT Challenges

Most difficulties for Mixed-signal DfT due to:

- **accuracy requirements for measuring analog signals**
- **lack of "accepted" analog fault models**
- **access issues for embedded components**
- **most class of circuits need specific testing methods**
- **current mixed-signal test requirements exceed available tools and ATEs**
- **lack of a structured test methodology**
- **advanced processes not stable: no good process characterization data**

DfT practical trade-offs:

- fault coverage
- performance impact
- extra area
- design impact
- yield loss
- availability of tools
- test time

como introducir BIST?

NICRON 2006
INAOE, Puebla, Mexico

NICRON 2006
INAOE, Puebla, Mexico

What to test? What to need?

Functional test : Parameters related to specs

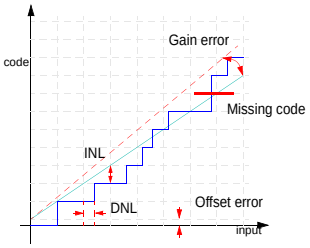
- standard metrics / standard measurements
- stimulus generation issues
- acquisition issues
- accessability issues

Structural test: Fault coverage and predict future yield problems

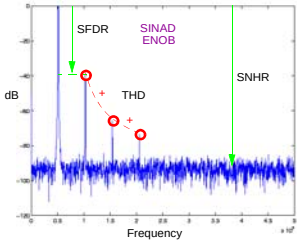
- defect-to-fault mapping
- fault models & fault simulations
- stimulus generation issues
- acquisition and response analysis issues
- accessability issues

Some of these issues: metrics

Static set of metrics



Dynamic set of metrics



Also: IM distortion, bandwidth, NPR, differential gain and phase, aperture effects,...

Some of these issues: methods

Code transition location → - servo-loop; - ramp histogram; - sinewave histogram

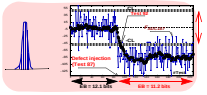
Sine-wave fit → - tree parameters; - four parameters

Discrete Fourier transform — IEEE Std 1241-2000

- huge number of samples, large records
- high-resolution input signal
- expensive test hardware

How Converter testing has evolved

- Better understanding of error sources
- New standard for parameter definitions and test methods
- Linking testing needs to applications
- Developing test schemes to manage different problems



Linearity, SINAD, IMD, Out-of-range, NPR, word error rate,...

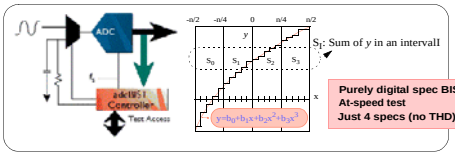
High performance
High reliability
Low cost

computer
telecon
automotive
consumer

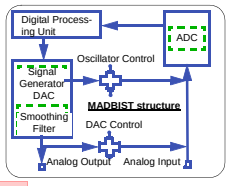
Scan chains, BIST, ad-doc, acces in SOC, BISTed cores, simplification, structural test, embedded test,...

Some Test Schemes

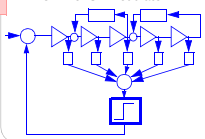
- HBIST (functional)
- MADBIST (functional)
- OBIST/BISTmaxx (functional & structural)
- adcBIST (functional)
- Ad-hoc BIST schemes (func.& struc.)



Purely digital spec BIST
At-speed test
Just 4 specs (no THD)



OBT for SD modulator



Histogram-based BIST

Offset
Gain
INL
DNL

Present situation

- Conventional test approaches inefficient to cope with current test requirements of ADCs (embedded in complex systems or alone)
- Yield loss getting worse as ICs performance reachs ATE performance

Solutions?

accurate simplified test

parallel test

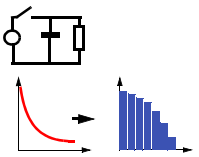
distributed test resources

defect-oriented test

Some emerging solutions-1

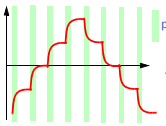
To relaxe source linearity requirement

Exponential waveform test signal



Proposed as a characterization test:
fitting algorithm → determines R, C and Vref
histogram → DNL(k)=$P_{act}(k)/P_{id}(k)$-1

Ramp equivalent signal:
digitally controlled on-chip
use external RC filter



processed samples

Applied to a 16 bit ΣΔ converter

Finite resolution ramps + new computational algorithm

Some emerging solutions-2

To reduce time

Model-based test

→ develop linear models with a reduced variable set

$$\begin{bmatrix} INL(i) \end{bmatrix} = \begin{bmatrix} \text{linear model} \end{bmatrix} \begin{bmatrix} var \end{bmatrix}$$

→ measure the parameters of interest only at some points and solve for the reduced variable set. (the number of points give the confidence interval)

→ extrapolate the non-measured (up to 2^n) values according the model

→ check if the specifications are respected

Short-codes + model-based test

Some emerging solutions-3

For high-resolution ΣΔ converters

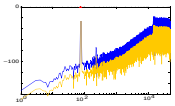
Precise on-chip generation of sine-waves is challenging:

- Use a DAC, in particular a ΣΔ DAC
- Use a recirculating bitstream of ΣΔ encoded sine-wave + a simple filter

Polar return-to-zero sequence
Coherent sampling
Register length => frequency limitations

- Use directly the scaled digital bitstream to test ΣΔ modulators

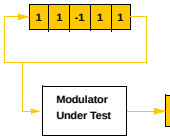
The scaling brings the stimulus noise below the modulator noise



Some emerging solutions-4

Design-spec based BIST

For integrator leakage in SD modulators



Digital Periodic Sequence:

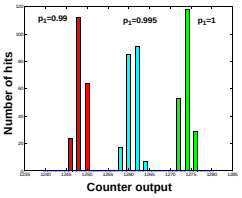
- Small recycling register
- Digital tester input

M.U.T.:

- Feedback DAC replica
- Modified switching scheme

Bitstream sum:

- Simple counter



Conclusions

Needs

more research for:

- accurate simplified test
- parallel test
- distributed test resources
- better structural test

IMSTW contributions to Converter Testing in 10 years:

1995 → 3 /45 ADC&DACpapers
2003 → 12/46 ADC&DACpapers

Structural Test for Mixed-signal ICs

Structural Test for Mixed-signal ICs

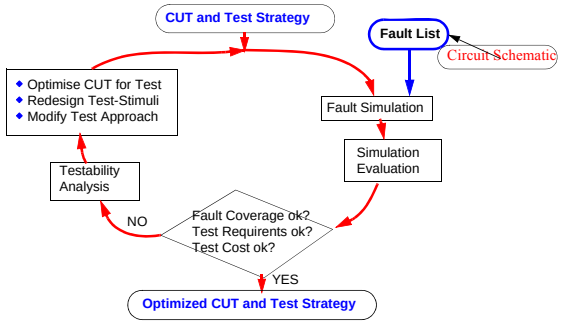
Functional test has been the unique "widely accepted" approach for mixed-signal ICs (embedded in complex systems or alone), but:

- Yield loss getting worse as ICs performance reaches ATE performance
- Functional test in SoCs is much more costly than for stand-alone parts
- Structural test may become the only viable method for current mixed-signal test requirements, because of
  - low-cost tester requirements
  - more compatible with IEEE 1149.4 test bus standard
  - easier for BIST implementation
- Structural test may be desirable for in-field test and diagnosis of Microsystems

Industry is now pushing innovations and improvements in mixed-signal structural test

Conventional Structural Test

Fault-based Test Flow: No Specs are, in general, measured



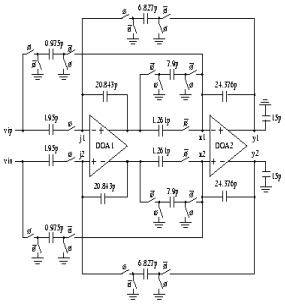
As good as fault models and fault simulations are

May be very costly in simulation time

An example

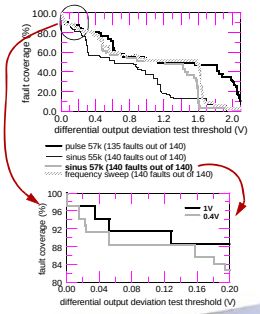
The CUT: **A second order SC Bandpass filter** (f_0 = 56.915kHz, Q= 19.233)

Test strategy: deviations of differential output from the fault-free circuit



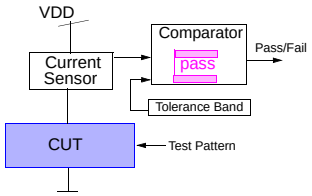
[Mir,...]

Fault coverage for different input test signals: Selection of test stimuli



I_{DDQ} Technique

- I_{DDQ} Testing is a well structured DfT methodology which is widely used by Semiconductor Industries (mainly for digital circuits)
- I_{DDQ} technique is based on the fact that defective circuits produce an abnormally high value of the quiescent power supply current



Basic areas to research

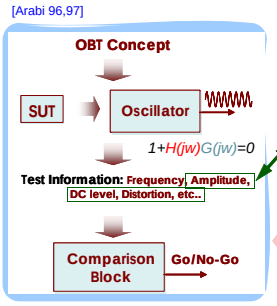
- Instrumentation for I_{DD} measurement
- Built-in current sensor (BICS)
- Fault models and metrics
- CAD tools
- Transient I_{DD}
- Signature-based techniques instead of pass/fail threshold
- Power supply partitioning at chip level

Up to now applied to simple analog blocks or as complement of other techniques

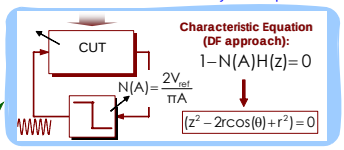
Oscillation-based Test (OBT)

Additional feedback added to the system or to some blocks to produce oscillations.
Faults are detected from: a) no oscillation, or,
b) deviation of the oscillating signal parameters

[Arabi 96,97]



[Huertas 99]
Nonlinear feedback for stability and amplitude control



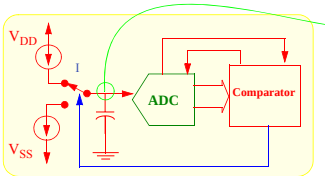
Structural Test Solution very appealing!!

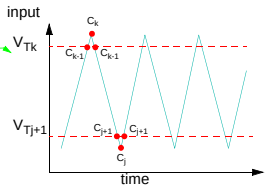
- Conceptually simple
- Vector-less method
- No important modifications of the SUT
- Easy to extend to BIST

BISTmaxx™

- Commercialised (Opmaxx) BIST structure for analog and mixed-signal ICs
- Convert block (filter, opamp, PLL, ADC, DAC, VCO, regulators) into circuit that oscillates at a predetermined frequency
- Frequency is treated as digital signature and is related to functional & structural parameters

Application to ADC:





The oscillation frequency of the two least significant bits may give information on the conversion time and DNL

$$\varepsilon_{DNL}^{k} = (V_k - V_{k+1}) = \frac{I}{2C(f_{osc} - 4t_C)} \rightarrow \varepsilon_{INL} = \sum_{k} \varepsilon_{DNL}^{k}$$

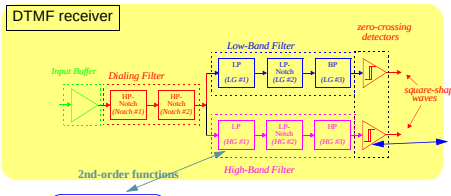
As the integration rate is constant, the frequency only depends on (VTk - VTj+1)

If k=j+2, it gives the width of step j+1

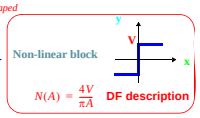
$$f_{osc} = \frac{1}{\frac{2(V_k - V_{j+1})C}{I} + 4t_C}$$

OBT in Filters: an example (1)

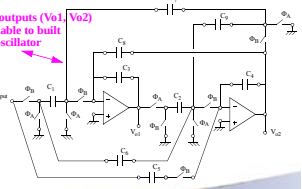
[Huertas 2002]



$$H(z) = \frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$$



Two outputs (Vo1, Vo2) available to built the oscillator



Analytical relationships for oscillation:

Oscillation conditions: $sign\{a_2 - a_0\} = sign\{b_0 a_2 - a_0\} \neq 0$

Amplitude of oscillations: $A_0 \approx \frac{4V}{\pi}\left|\frac{a_2 - a_0}{1 - b_0}\right|$

Frequency of oscillations: $f_{osc} \approx \frac{1}{2\pi}\arccos\left\{\frac{1}{2}\left[\frac{b_1 - a_1 N(A_0)}{1 - a_2 N(A_0)}\right]\right\}$

OBT in Filters: an example (2)

Validation Results:

BQ #	type	f_{osc}		A_0	
		theorical	simulated	theorical	simulated
1	LP	835.0	830.7	1.27	1.26
2	LP	1330.8	1331.7	1.27	1.26
3	Notch	791.4	717.1	0.72	0.79
4	Notch	968.6	967.7	1.84	1.79
5	Notch	1182.2	1177.5	1.55	1.54
6	Notch	603.9	592.9	1.64	1.81
7	BP	608.3	601.9	4.16	4.10
8	HP	1696.9	1694.9	1.47	1.46

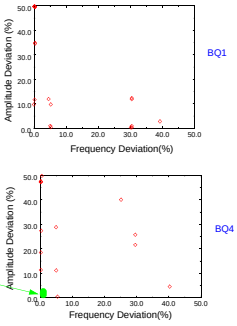
Table I: Oscillation frequencies and amplitudes for each biquad (V=1Volt)

MonteCarlo Analysis to define the minimum deviation that can be consider as faulty behavior

	1	2	3	4	5	6	7	8
ΔA_0 (%)	1.1	1.5	0.6	2.7	2.4	2.1	1.2	2.4
Δf_{osc} (%)	0.5	0.6	0.1	0.3	0.4	0.4	0.6	0.6

Table II: Parameter deviations for a 0.4% of mismatch in capacitor ratios.

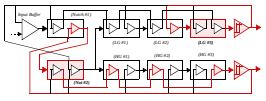
60/67 faults injected in each biquad



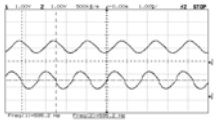
OBT in Filters: an example (3)

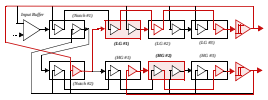
Application: Two biquads tested simultaneously

Making use of Sw-opamps

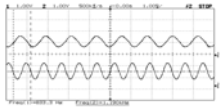


a) Group #1: Testing Not#2 and LG#3

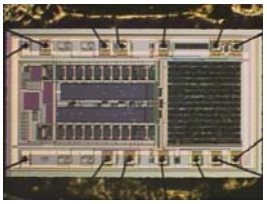




c) Group #3: Testing LG#1 and HG#2



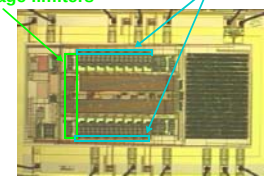
OBT in Filters: an example (4)



Design with no OBIST

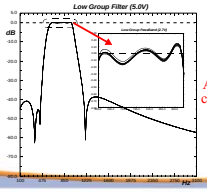
voltage limiters

(sw-opamps)

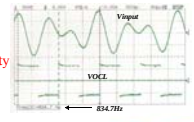


Design with OBIST & other test facilities

7% area overhead

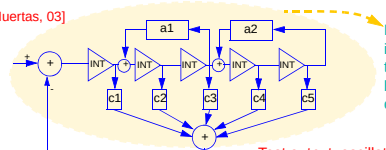


Acces capability



OBT in Σ-Δ Converters (1)

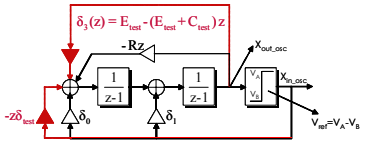
[Huertas, 03]



Disconnect the input and modify the structure to build a robust oscillator

Test output: oscillation waveform

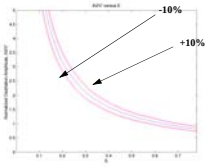
Regular output



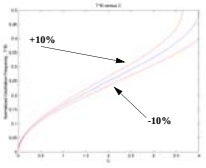
Oscillation Parameters	Oscillation Conditions
$f_{osc} = \frac{1}{2\pi T_s} a \cos\left(\frac{2+R\text{-}C_{test}}{2}\right)$	$-1 < \frac{2+R\text{-}C_{test}}{2} < 1$
$A_{osc} = \frac{2V_{ref}}{\pi}\left(\frac{\delta_1\text{-}\delta_0}{E_{test}}\right)$	$\text{sign}(V_{ref})=\text{sign}(\delta_1\text{-}\delta_0)$ $\delta_1\text{-}\delta_0 \neq 0$

OBT in Σ-Δ Converters (2)

Simulation results A_{os} and f_{os} as function of E_{test} and C_{test}



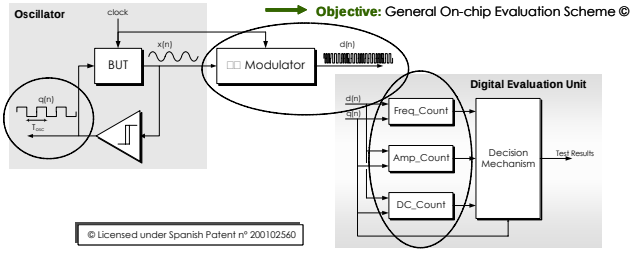
Changes in the Normalized Oscillation Amplitude for a 10% change in integrator gain



Changes in the Normalized Oscillation Frequency for a 10% change in integrator gain

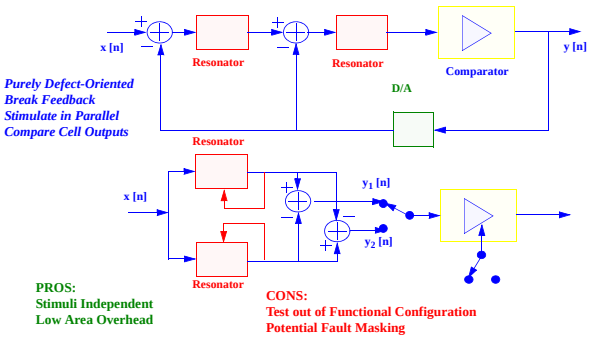
Extension to OBIST

[Vázquez, 02]



Reconfiguration-based BIST (1)

For Σ-Δ modulators [Mir, 97]



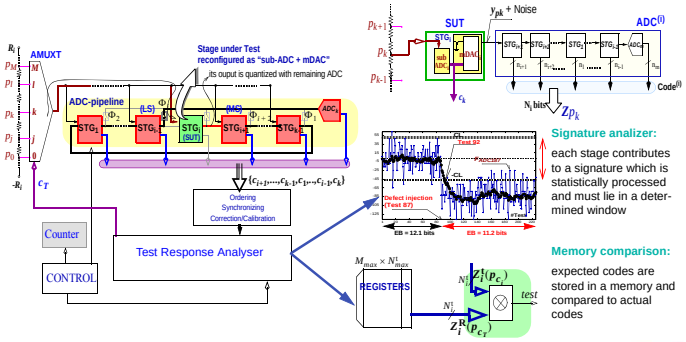
Purely Defect-Oriented
Break Feedback
Stimulate in Parallel
Compare Cell Outputs

PROS:
Stimuli Independent
Low Area Overhead

CONS:
Test out of Functional Configuration
Potential Fault Masking

Reconfiguration-based BIST (2)

For Pipeline ADCs [Peralías,00]



Signature analizer:
each stage contributes to a signature which is statistically processed and must lie in a determined window

Memory comparison:
expected codes are stored in a memory and compared to actual codes

Emerging solutions for ADC testing

Conventional Test Methods

Aimed to obtain performance parameters

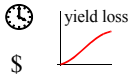
Code transition location → - servo-loop; - ramp histogram; - sinewave histogram

Sine-wave fit → - three parameters; - four parameters

Discrete Fourier transform

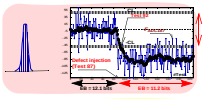
IEEE Std 1241-2000

- huge number of samples, large records
- high-resolution input signal
- diverse and expensive test hardware
- hard for BIST in embedded cores



How Converter testing has evolved

- Better understanding of error sources
- New standard for parameter definitions and test methods
- Linking testing needs to applications
- Developing test schemes to manage different problems



Linearity, SINAD, IMD, Out-of-range, NPR, word error rate,...

IEEE Std 1241-2000

High performance
High reliability
Low cost

computer
telecon
automotive
consumer

Scan chains, BIST, ad-doc, access in SOC, BISTed cores, simplification, structural test, embedded test,...

Some emerging solutions

What are the issues?:

Functional test
- easy interpretation
- precision limited: acquisition and generation
- very costly for high resolution ADCs

Structural test
- fast and low-cost
- confidence limited

Where are the improvements?:

Relaxing source linearity requirements:
- Finite resolution stimulus
- Other input signals: exponential, noise
- Alternate test

Reducing test time:
- Model-based methods
- Behavioral model-based Structural Test

More efficient BIST solutions

Relaxing input test signals (1)

Finite resolution stimulus + new computational algorithm [Jin,03 - Yu,04]

1) Histogram based approach

- Input: two "ramp-like" nonlinear signals
- Histogram-based algorithm
- Static performance: DNL, INL

Objective: separate the nonlinearity of the ADC from that in the input

Reported result: 8-bit linear inputs able to test a 16-bit ADC

2) Spectrally Related Excitation (SRE) approach

- Input: two imprecise sinewaves
- FFT-based algorithm
- Spectral performance: THD, SFDR

Idea: use of the spectral relationship between inputs to separate the distortion of the ADC

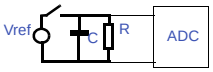
Reported result: 60dB sinewaves able to test 100dB SFDR ADC

Functional type: Reduce tester cost but not test time
Only good for partial BIST: generation part

Relaxing input test signals (2)

Exponential waveform test signal [Chen, 02 - Holcer, 03]

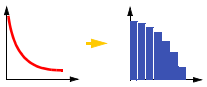
- based on capacitor discharge ---> well-known shape
- depend on R and C and Vref
- easily implemented



Proposed as a characterization test:

fitting algorithm → determines R, C and Vref

histogram → $DNL(k)=P_{act}(k)/P_{Id}(k)-1$



Staircase-like exponential waveform test signal [Roy,02]

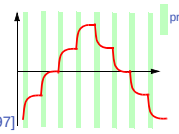
Ramp equivalent signal:

4 exponential steps: use of digital PWM

digitally controlled on-chip

use external RC filter

use polynomial fitting algorithm [Sunter97]



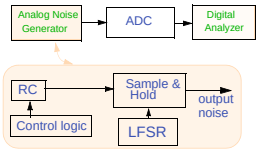
Purely digital spec BIST
At-speed test
Just 4 specs (no THD)

Validated for a 16-bit ΣΔ converter

Relaxing input test signals (3)

Noise input signal [Flores,05]

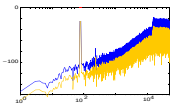
- based on multiple tone signal and spectral analysis
- valid for static and dynamic functional parameters
- needs less output samples than histogram-based



Specific input signal [Ong,02]

- for testing SD modulators
- test input is a scaled bitstream of the modulator
- extract only integrator leakage errors

Also developed with pseudorandom input

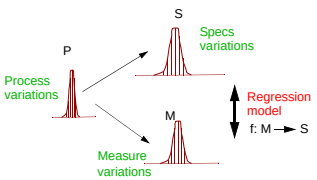


the scaling brings the stimulus noise below the modulator noise

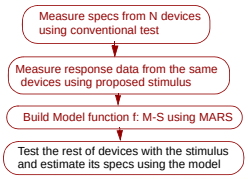
Relaxing input test signals (4)

Alternate Test [Variyam,98-02] [Bhattacharya,05]

- targeted to reduce tester resources requirements
- based on developing non-linear regression models
- uses the models to find the stimulus and to predict specs from responses
- valid for functional or structural techniques
- recently applied to high-resolution high-speed ADCs and to RF



Test Flow example



Reducing Test Time

Model-based Test [Wegener, 04-05]

- develop linear models with a reduced variable set

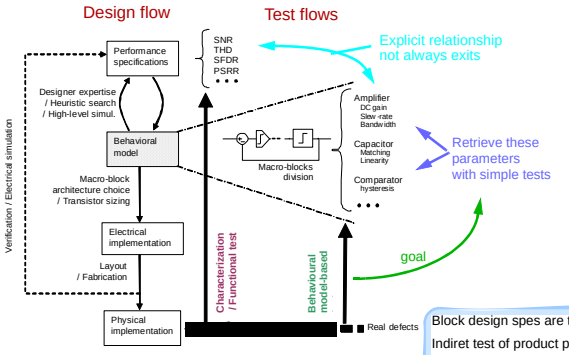
$$[\text{Specs}] = [\text{model}]\,[\text{var}]$$

- measure the parameters of interest only at some points and solve for the reduced variable set. (the number of points give the confidence interval)
- extrapolate the non-measured values according the model
- check if the specifications are respected

- Do not relax the tester req. but the number of specs to measure
- A good methodology exists

Behavioral model-based Test

Behavioral model-based Test

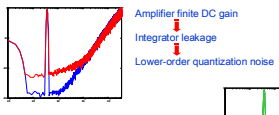


Block design spes are tested
Indiret test of product performance
Test generation linked to design flow

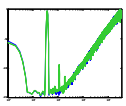
Like a defect-oriented test at the block level

Application to ΣΔ Converters

Block defect effects



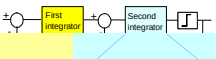
Amplifier finite DC gain
Integrator leakage
Lower-order quantization noise



Amplifier Slew-Rate and Gain-Bandwidth
Non-linear settling error
Harmonic distortion

Other parameters (DC gain non-linearity/Output swing, CMRR, ...)

Not equally significant for all the amplifier



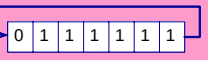
Demanding design:
Low thermal noise ➡ large capacitors
High and linear DC gain
Good settling

Relaxed design:
Small capacitors
High but not so linear
Relaxed settling

A Digital BIST for ΣΔ modulators (1)

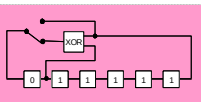
Fully digital BIST based on the behavioral test idea [Leger,04 - Leger, 06]

The test stimulus:
Digital sequences



Periodic input sequence: Q mean value

6-bit Pseudo-random input sequence



Seq → **ΣΔ Under Test** → Y → Up/down Counters

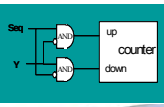
Clocking control

The signature analyser:
Simple up/down counters

Targeted to test:
- Integrator leakages
- Amplifier settling errors
- Non-linear amplifier gains

Added value of the BIST scheme:
- For production screening test
- For embedded circuits in SoC or SiP
- For in-field test
- For diagnosis

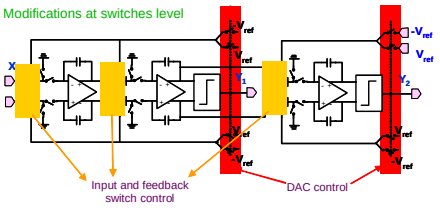
BIST Signature: realize the operation,



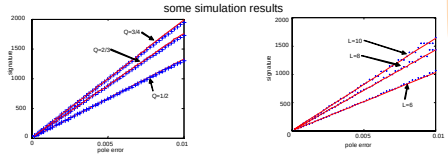
A Digital BIST for ΣΔ modulators (2)

Application to a 2-1 cascade modulator

Modifications at switches level



some simulation results



Some signatures

DC gain 1st integrator:

$$\sum_N (Y - X) = 2NQ(p_1 - 1)$$

N: number of adquired samples

Q: input seq mean value

p_1: integrator pole error (leakage

DC gain 2nd and 3rt integrators

$$\sum_N (Y - X) = \frac{-2N(1-p)}{\ln\left(\frac{5-3L}{5-L}\right)}$$

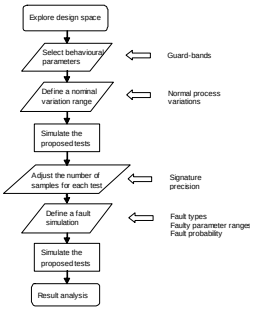
L: input seq period

Amplifier settling error:

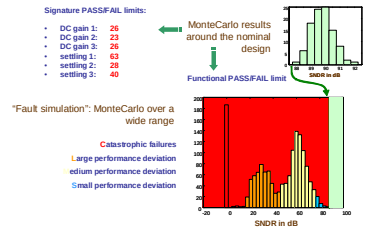
$$\sum_N (Y - X) = \frac{N}{4} \times er(-2)$$

A Digital BIST for ΣΔ modulators (3)

Tests set validation

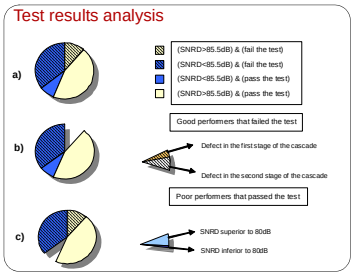


High-level simulation results

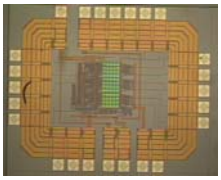


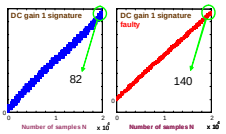
A Digital BIST for ΣΔ modulators (4)

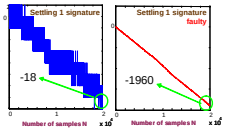
Test results analysis



Experimental results







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