Charge Recycling in MTCMOS Circuits: Concept and Analysis

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ABSTRACT

Designing an energy efficient power gating structure is an important and challenging task in Multi-Threshold CMOS (MTCMOS) circuit design. In order to achieve a very low power design, the large amount of energy consumed during mode transition in MTCMOS circuits should be avoided. In this paper, we propose an appropriate charge recycling technique to reduce energy consumption during the mode transition of MTCMOS circuits. The proposed method can save up to 46% of the mode transition energy while, in most cases, maintaining, or even improving, the wake up time of the original circuit. It also reduces the peak negative voltage value and the settling time of the ground bounce.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles-*Advanced Technologies*.

General Terms: Design

Keywords: MTCMOS, charge recycling, low power design.

1. INTRODUCTION

As CMOS technology scales down, the supply voltage is reduced so as to avoid device failure due to high electric fields in the gate oxide and the conducting channel under the gate. Voltage scaling reduces the circuit power consumption because of the quadratic relationship between dynamic power consumption and supply voltage, but it also increases the delay of logic gates. To compensate the resulting performance loss, transistor threshold voltages are decreased, which causes exponential increase in the sub-threshold leakage current [1].

MTCMOS technology provides low leakage and high performance operation by utilizing high speed, low Vt (LVT) transistors for logic cells and low leakage, high Vt (HVT) devices as sleep transistors. Sleep transistors disconnect logic cells from the supply and/or ground to reduce the leakage in the sleep mode. In this technology, also called power gating, the wake up latency and power plane integrity are key issues.

Assume a sleep/wake up signal is supplied by an on-chip power management module. A key question is how to minimize energy consumption while doing the mode transition, i.e., when switching from active to sleep mode or vice versa. Another important question is how to minimize the time required to turn on the circuit upon receiving the wake up signal since the length of the wake up time can affect the overall performance of the VLSI circuit. Furthermore, the large current flowing to ground when sleep transistors are turned on can become a major source of noise in the power distribution network, which can adversely impact the performance and/or functionality of the other parts of the circuit. Hence, there is a trade off between the generated noise due to the current flowing to ground and the transition time from the sleep mode to the active mode.

Sleep transistors cause logic cells to slow down during the active mode of the circuit operation. This is due to the voltage drop across the functionally-redundant sleep transistors and the increase in the threshold voltage of logic cell transistors as a result of the body effect. The performance penalty of a sleep transistor depends on its size and the amount of current that goes through it. Several researchers have proposed methods for optimal sizing of sleep transistors in a given circuit to meet a performance constraint [2]-[4]. In [5], the authors propose a power gating structure to support an intermediate power-saving mode and the traditional power cut-off mode. The idea is to add a PMOS transistor in parallel with each NMOS sleep transistor. By applying zero voltage to the gate of the PMOS transistor, the circuit can be put in the intermediate power saving mode whereby leakage reduction and data retention are both realized. Furthermore, by transitioning through this intermediate mode while changing between sleep and active modes, the magnitude of power supply voltage fluctuations during power-mode transitions is reduced. In the cut-off mode, the gate of the PMOS transistor is connected to V_{DD}.

None of these works attempt to minimize the power consumption during the sleep-to-active and active-to-sleep transitions, or reduce wake up time and the noise generated by the power gating structure. In contrast, we apply a charge recycling technique to minimize the power consumption during the mode transition in a power gating structure while maintaining, or sometimes even improving, the wake up time. We show that how the proposed technique also helps us reduce the ground bounce (GB) in the sleep to active transition.

The remainder of this paper is organized as follows. In section 2, we introduce the concept of using charge recycling technique in power gating MTCMOS circuits, and we find the optimal conditions to achieve the maximum Energy Saving Ratio (ESR). In section 3, we study the effect of the threshold voltages and sizing of the transistors used in the transmission gate (TG) on the saving ratio and wake up time of the circuit. In section 4 we analyze the influence of the proposed charge recycling technique on the wake up time, leakage and GB of the circuit. Section 5 represents the simulation results, and finally section 6 concludes the paper.

2. CHARGE RECYCLING TECHNIQUE

Consider the configuration shown in Figure 1. There are two different blocks in the circuit; one is power-gated by an NMOS sleep transistor which connects the virtual ground, i.e., node G in

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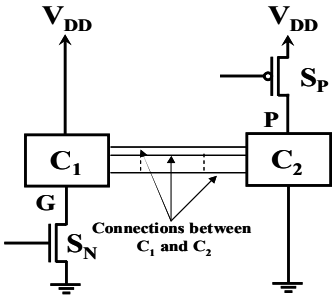

Figure 1. Conventional power gating structure using an NMOS or a PMOS sleep transistor for each circuit block.

the figure, to the ground, whereas the other is power-gated by a PMOS sleep transistor which connects the virtual supply, i.e., node P in the figure, to the supply. During the active period, sleep transistors S_N and S_P are in the linear region and the voltage values of the virtual ground and virtual supply are equal to 0 and V_{DD}, respectively. During the sleep time, sleep transistors S_N and S_P are turned off, and since they are chosen to be high threshold devices, they allow very little subthreshold leakage current to flow through them.

Now, if the duration of the sleep period is sufficiently long, all internal nodes of the gates in block C_1 and the virtual ground node, G, will be charged up to some voltage value very close to V_{DD} [6]. This is due to G being floated and leakage current causing its voltage level to rise toward V_{DD}. Similarly, if the duration of the sleep period is long enough, all the internal nodes of C_2 and virtual supply node, P, will be discharged to some voltage value very close to 0. When the sleep-to-active transition edge arrives at the gates of the sleep transistors to turn them on, G starts to fall toward 0, whereas *P* starts to rise toward V_{DD}. If we denote the total capacitance in the virtual ground and supply by C_G and C_P, respectively, we observe that during the active-to-sleep transition, C_G is charged up from 0 to V_{DD} while C_P is discharged from V_{DD} to 0. The situation is reversed for the sleep-to-active transition, that is, in this case C_G will be discharged from V_{DD} to 0, while C_P will be charged to V_{DD} from its initial value of 0. These charge and discharge events on the virtual ground and V_{DD} nodes are wasteful from a circuit energy dissipation point of view.

Our goal is to reduce the energy as we switch between active and sleep modes of the circuit. More precisely, we propose to use a charge recycling technique to reduce the switching power consumption during the active-to-sleep and sleep-to-active transitions by adding a TG between the virtual ground and supply nodes as shown in Figure 2. The proposed charge recycling strategy works as follows.

We turn on the TG (i) immediately before turning on the sleep transistors while going from sleep to active mode, and (ii) just after turning off the sleep transistors while going from active to sleep. By turning on the TG at the end of the sleep mode as the circuit is about to go from sleep to active mode, we allow charge sharing between the completely charged up capacitance C_G and the completely discharged capacitance C_P. After the charge recycling is completed, the common voltage of the virtual ground and virtual supply is αV_{DD}, where α is a positive real number less than 1. The value of α depends on the relative sizes of C_G and C_P. As a result of this step, power consumption due to switching on the sleep transistors is reduced. This is because in this case we have a

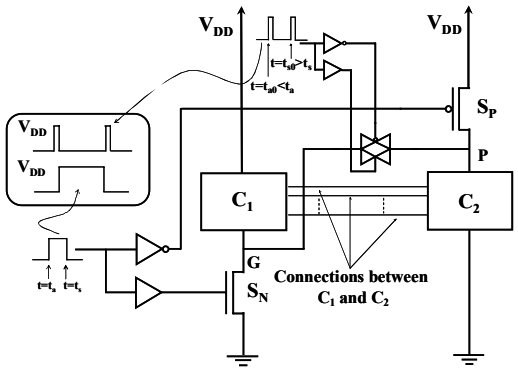

Figure 2. The proposed charge recycling configuration in power gating structures.

transition from αV_{DD} to 0 at the virtual ground, and from αV_{DD} to V_{DD} at the virtual supply; whereas in the conventional MTCMOS circuit without the charge recycling, the transition was from V_{DD} to 0 and from 0 to V_{DD} at the virtual ground and supply nodes, respectively. A similar analysis proves that the charge recycling technique helps reduce power consumption in the transition from active to sleep mode as well.

In the following, we calculate the maximum achievable power saving and the conditions we need to achieve this maximum saving. To do this, we consider two different transitions: sleep-to-active and active-to-sleep.

Case A: Wake-up Transition

In Figure 3, C_G and C_P represent the total capacitance in the virtual ground and supply nodes, respectively. We assume that the sleep period is long enough such that C_G has had time to charge up to some value close to V_{DD}, while C_P has had time to completely discharge to some small value close to 0. This is a good assumption in most circuits. Otherwise, the voltage of C_G and C_P will be a function of the length of the sleep period.

As stated earlier, to go from sleep mode to the active mode, instead of simply turning on sleep transistors, we first allow charge recycling between C_G and C_P. To do that, we close switch M at the time $t=t_{a0}$. Assuming ideal charge sharing between C_G and C_P, the common voltage value of nodes G and P after charge sharing is calculated by equating the total charge in both capacitances before and right after charge recycling:

$$V_{f\_sa} = \alpha V_{DD}$$
$$\alpha = \frac{C_G}{C_G + C_P} \quad (1)$$

The common voltage value of the virtual ground and virtual supply at the end of the charge sharing is αV_{DD}. After the charge sharing is complete, i.e., at time $t=t_{a1}$, we open switch M, and then turn on the SN and SP sleep transistors. As a result, there will be a path from the virtual ground to the (actual) ground going through SN which forces C_G to be discharged to 0. We will also have a path from the virtual supply to the (actual) supply going through S_P which causes C_P to be charged to V_{DD}. If we neglect the energy consumption in the switch itself, for now, the total energy drawn from the power supply is due to the process of charging capacitance C_P which can be obtained as follows:

$$E_{sleep-active} = C_P V_{DD} \times (\Delta V)$$
$$= C_P V_{DD} \times (V_{DD} - V_{f\_sa}) \quad (2)$$

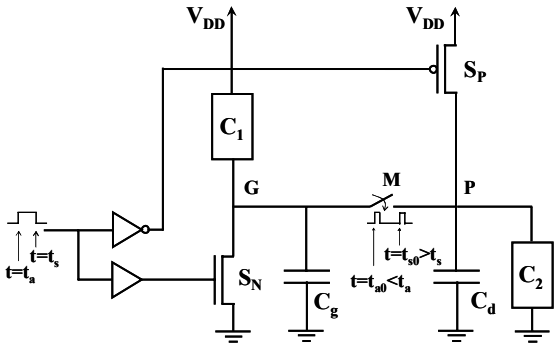

Figure 3. Charge recycling technique. TG is replaced by an ideal switch. C_G and C_P are total capacitance in virtual ground and virtual supply, respectively.

Substituting from (1) for V_{f_sa}, we obtain the energy consumption from the power supply in sleep-active transition:

$$E_{sleep-active} = C_P V_{DD} \times (V_{DD} - \alpha V_{DD}) = (1-\alpha) C_P V_{DD}^2 \quad (3)$$

Next we consider the transition from active to sleep.

Case B: Sleep Transition

Consider the circuit shown in Figure 3. As mentioned earlier, to go from active mode to the sleep mode, instead of simply turning off the sleep transistors, we do charge recycling between C_G and C_P as soon as the circuit enters the sleep mode. In particular, we close switch M at $t=t_{s0}$ which is the time when we turn off sleep transistors. The voltage values of the virtual ground and virtual supply nodes at this time are 0 and V_{DD}, respectively. Assuming ideal charge sharing between C_G and C_P, the common voltage value of nodes G and P after charge sharing is calculated by equating the total charge in both capacitances right before and after the charge sharing:

$$V_{f\_as} = \beta V_{DD}, \quad \beta = \frac{C_P}{C_G + C_P} \quad (4)$$

Based on the above equation, the common voltage value of the virtual ground and virtual supply at the end of the charge sharing is βV_{DD}. By the time the charge recycling is complete, $t=t_{s1}$, we open the switch. After opening the switch, there is a leakage path from the power supply to the virtual ground going through logic block C_1 which eventually causes C_G to be charged up to V_{DD}. We also have a leakage path from the virtual supply to the ground going through logic block C_2 which eventually causes C_P to be completely discharged into the ground. Again, if we neglect the power consumption in the switch, the total energy consumed from the power supply is due to the charging up the capacitance C_G in this case, and we can calculate this energy consumption as follows:

$$E_{active-sleep} = C_G V_{DD} \times (\Delta V) = C_G V_{DD} \times (V_{DD} - V_{f\_as}) \quad (5)$$

Substituting from (4) for V_{f_as}, we obtain:

$$E_{active-sleep} = C_G V_{DD} \times (V_{DD} - \beta V_{DD}) = (1-\beta) C_G V_{DD}^2 \quad (6)$$

Since $\alpha+\beta=1$, we can calculate the total energy consumption by adding $E_{active-sleep}$ and $E_{sleep-active}$ which results in:

$$E_{cr\_total} = E_{active-sleep} + E_{sleep-active} = \alpha C_G V_{DD}^2 + \beta C_P V_{DD}^2 \quad (7)$$

where $E_{cr-total}$ is energy consumption with charge recycling.

We can calculate the total energy consumption when we do not perform any charge recycling between P and G, yielding:

$$E_{total} = C_G V_{DD}^2 + C_P V_{DD}^2 \quad (8)$$

From (7) and (8), and after substituting for α and β from (1) and (4), we find the energy saving ratio (ESR) as follows:

$$ESR(X) = \frac{E_{total} - E_{cr\_total}}{E_{total}} = \frac{2X}{(1+X)^2} \quad (9)$$

where X is defined as the ratio of the virtual ground capacitance to the virtual supply capacitance, or $X=C_G/C_P$. The optimum value for X which maximizes $ESR(X)$ is obtained by equating the derivative of this ratio to zero which results in X=1, or $C_G=C_P$. In other words, in order to obtain the best energy saving, we need to have

equal capacitances in virtual ground and virtual supply. Then the maximum energy saving is:

$$ESR_{\max} = ESR(X)\ |_{X=1} = 0.5 \quad (10)$$

This means that we can obtain a maximum energy saving of 50% by using the charge recycling method. However, considering the power needed to turn on or off the TG, the total saving ratio is less than 50%. Figure 4 shows an example of the balanced (i.e., $C_G=C_P$) charge recycling operation when transitioning from sleep to active mode for an inverter chain in 70nm CMOS technology generated in HSPICE. In this figure we can see the virtual ground voltage, V_G, the virtual supply voltage, V_P, and the charge recycling signal, V_{CR}.

3. THRESHOLD VOLTAGES AND SIZES OF TRANSISTORS IN TG

All the equations we derived in the previous section were based on the assumption of having an ideal charge recycling process between C_G and C_P. Under this scenario, we assume that no energy is consumed to switch the TG on and off. We also assume that the TG is "ON" while the charge recycling is in process.

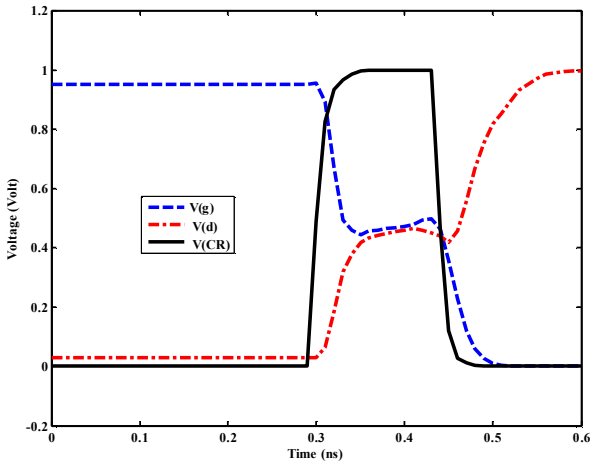

Figure 4. Charge recycling operation for an inverter chain in 70 nm CMOS technology.

However, because of the dynamic power consumption in the TG, and also the possibility of having incomplete charge sharing (cf. section 3.1), this is not a perfect replacement in practice. In this section we study the effects of the TG threshold voltage and sizing on the energy saving ratio and the wake up time of the charge recycling configuration.

3.1 Effect of Threshold Voltage

We consider a more realistic charge recycling scenario where we replace the ideal switch with a practical circuit model of a CMOS TG. Next, we discuss the effect of transistor threshold voltages on the power saving and the delay of the circuit.

Consider the charge sharing configuration shown in Figure 5. To have a complete charge sharing, the TG has to stay "ON" for the whole duration of the charge sharing process. In order to have this property, the absolute values of the threshold voltages of the N and P transistors of the TG have to be small enough. To guarantee this, the common final voltage value of virtual ground and virtual supply, i.e., V_f, has to satisfy at least one of the following two inequalities:

$$\begin{cases} V_{t,n} \le V_{DD} - V_f \\ \quad or \\ \left|V_{t,p}\right| \le V_f \end{cases} \tag{11}$$

where $V_{t,n}$ and $V_{t,p}$ denote threshold voltages of the NMOS and PMOS transistors in the TG accounting for the body effect. Notice that V_f can be obtained from (1) for the active to sleep case and from (4) for the sleep to active case. The inequalities guarantees that at least one of the transistors in the TG remains "ON" for the complete duration of charge sharing process.

In the case of equal capacitive loads in virtual ground and virtual supply, C_G=C_P, a complete charge sharing in both active-to-sleep and sleep-to-active cases results in a common final voltage value of V_f=V_{DD}/2, and (11) translates into $Min\{V_{t,n}, |V_{t,p}|\} \le V_{DD}/2$. If this condition is not satisfied, the charge recycling is not complete, and the energy saving ratio (ESR) will be less than what we have predicted. In this case, if V_{tn}=$|V_{tp}|$, we can simply use a pass transistor instead of a TG.

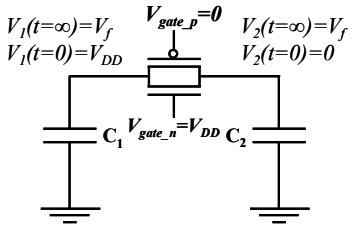

Figure 5. Charge sharing between C_1 and C_2 using a TG.

3.2 Transmission Gate Sizing Effect

Sizing of the TG is another factor that affects the ESR as well as the wake up time of the circuit. In case of the original configuration when there is not any charge recycling, the wake up time may be defined as the time between when we turn on the sleep transistors to when the voltage of the virtual ground reaches within 10% of its final value. However, in a circuit that uses charge recycling, the wake up time may be defined as the time between when we turn on the TG to when the virtual ground voltage goes below 10% of its final value. In the following discussion, we consider the effect of the dynamic power consumption of the TG on the energy saving ratio, ESR, which we previously calculated in section 2.

Figure 6 shows the TG along with its turn on circuit. Assume an input capacitance of C_{tg} for the NMOS transistor of the TG and the same input capacitance for the PMOS transistor of the TG. In

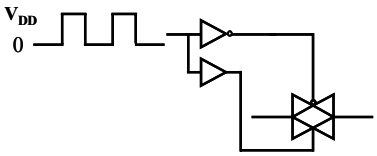

Figure 6. Drive circuitry for the charge recycling TG.

each active-sleep-active cycle, we need to switch on the TG twice, once before turning the sleep transistors on, and once after turning them off. Every time we turn the TG on, we are actually turning on both NMOS and PMOS transistors in the TG, i.e., the switched capacitance is $2C_{tg}$. Clearly, we turn off the TG after the charge sharing is complete. Therefore, we can calculate the dynamic energy consumption of the TG for one complete active-sleep cycle as follows:

$$E_{tg-total} = 4 \times \frac{1}{2} \times (2C_{tg}) V_{DD}^2 = 4C_{tg} V_{DD}^2 \tag{12}$$

Therefore, to calculate the actual energy saving ratio (ESR), we need to subtract the correction ratio $E_{tg\text{-}total}/E_{total}$ from the ideal ESR in (9). The correction ratio can be calculated as:

$$\frac{E_{tg-total}}{E_{total}} = \frac{4C_{tg} V_{DD}^2}{(C_G + C_P) V_{DD}^2} = \frac{4C_{tg}}{C_G + C_P} \tag{13}$$

This correction ratio is proportional to the size of the TG, since C_{tg} itself is proportional to the size of the TG. However, because there are usually too many gates connected to the virtual ground and virtual supply, C_G+C_P is usually much larger than C_{tg}, i.e., the correction ratio is usually in the order of few percents which makes the actual ESR to be less than the ideal ESR, 50%, by only a few percentage points.

By increasing the size of the TG, we can speed up the charge sharing process, and as a result, reduce the wake up time; however, this will also increase the correction ratio given in (13), hence, decreasing the energy saving ratio of the circuit. Therefore, there is a trade off between the wake up time and energy saving ratio.

4. WAKE UP TIME, LEAKAGE AND GROUND BOUNCE ANALYSIS

We analyze three important issues in power gating structures, namely the wake up time, leakage currents, and GB for our proposed charge recycling MTCMOS configuration.

4.1 Wake Up Time

In charge recycling MTCMOS, the larger the TG size is, the smaller the wake up time of the circuit is. The increased size, however, increases the dynamic power consumption of the TG. If we use a large enough TG, we can make the charge sharing time small enough such that we obtain a wake up time which is as small as, or sometimes even less than, that of the original circuit where we do not use any charge recycling. However, as seen from equation (12), by increasing the size of the TG, we are also increasing its energy consumption. Our experiments on a number of real circuits demonstrate that the size we need for the TG in order to maintain, or sometimes improve, the original wake up time is such that we will loose only a very small percentage of the ideal ESR.

4.2 Leakage

Consider Figure 7 a where r_1 and r_2 represent resistances of logic blocks C_1 and C_2, respectively, and R_N and R_P represent resistances of NMOS and PMOS sleep transistors, respectively. For conventional MTCMOS configuration, during the sleep period, there exist two different paths from V_{DD} to ground. Since C_1 and C_2 consist of LVT transistors, and sleep transistors are HVT transistors, we can assume that R_N, R_P >> r_1, r_2. Without loss of generality, and to simplify the discussion, we assume that R_N=R_P=R. The total resistance from the power supply to the ground is thus $R_{total\text{-}conv.}$=R/2, and the leakage power consumption is calculated as:

$$P_{leakage-conv.} = \frac{2V_{DD}^2}{R} \tag{14}$$

Next we calculate leakage power consumption for the charge recycling (CR) MTCMOS configuration. As seen in Figure 7 b, in this case, there is a new path from V_{DD} to the ground going through r_1, RTG and r_2. As we mentioned earlier, since C1 and C2 consist of LVT transistors, r_1 and r_2 are small resistances. In order to avoid having a high leakage path from the power supply to the ground, we have to make RTG as large as possible; this is possible by using HVT transistors in the TG. Let's assume that $R_{TG}=nR$ for some n. Knowing that R >> r_1, r_2, and by doing Δ-Y transformation for r1, RTG and RP, we arrive at the new resistive network shown in Figure 7 c where r_1^*, r_2^* and r_3^* are calculated as:

$$\begin{aligned} r_1^* &= \frac{r_1 R_P}{r_1 + R_{TG} + R_P} = \frac{1}{n+1} r_1 \\ r_2^* &= \frac{r_1 R_{TG}}{r_1 + R_{TG} + R_P} = \frac{n}{n+1} r_1 \\ r_3^* &= \frac{R_P R_{TG}}{r_1 + R_{TG} + R_P} = \frac{n}{n+1} R \end{aligned} \tag{15}$$

Total resistance from the supply to ground is calculated as:

$$R_{total-CR} = \frac{n}{2n+1} R \tag{16}$$

The leakage power in this case can be written as:

$$P_{leakage-CR} = \left(2 + \frac{1}{n}\right) \frac{V_{DD}^2}{R} \tag{17}$$

As seen from (17), the leakage power consumption has increased by a factor of (1+1/2n) compared to the conventional power gating method. If R_{TG}=2R, n is equal to 2, and we have a 25% increase in the leakage power. If the sleep period of the circuit is small, then this 25% increase in leakage energy consumption is negligible compared to the 50% switching energy saving that we achieve by using the charge recycling MTCMOS structure. On the other hand, if the sleep period is very long, we must use larger n by increasing resistance of the TG. This is possible by choosing transistors with smaller W/L ratios in the TG (which is also beneficial from the layout area point of view.) The potential disadvantage is that the charge cycling will take longer time to complete now since TG will have a larger "ON" resistance.

4.3 Ground Bounce

Ground and power line bounces are one of the most important design concerns with regard to power gating structures [6][7]. GB occurs in power gating structures at the sleep to active transition edge.

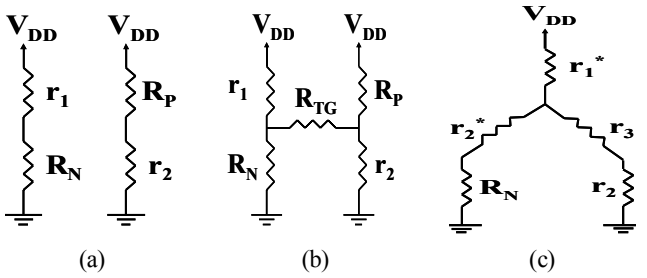

Figure 7. (a) Leakage paths for a conventional MTCMOS structure, (b) Leakage paths for CR MTCMOS structure (c) Δ-Y converted model of (b).

Consider Figure 8. After we turn on the sleep transistor at the end of the sleep period, a large amount of current flows into the ground. We adopt a simple RL model for the purpose of GB analysis. Because of the large di/dt at the turn-on time, there is a large voltage, Ldi/dt, appearing across the inductance. We next study the effect of the proposed charge recycling technique on the GB of the circuit.

Figure 8 shows the virtual ground capacitance, C_G, connected to the RL circuit (modeling the pin-package parasitics of the IC), via the sleep transistor, S_N.

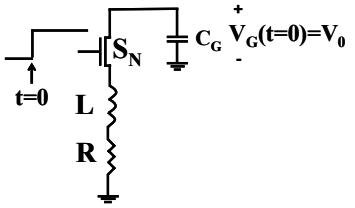

Figure 8. RL equivalent model of the ground used to analyze GB effect in MTCMOS.

We turn on the sleep transistor at t=0, and assume that the initial voltage of C_G at this time is V_0, i.e., $V_G(t=0)=V_0$. Based on the results of reference [8], the positive peak value of the GB occurs during the time when S_N operates in the saturation region. Although the peak value does not depend on voltage V_0, it depends on R, L, C_G, V_{Tn} and V_{DD} values. Therefore, we expect that the proposed charge recycling technique, which simply changes V_0 from V_{DD} to $V_{DD}/2$, does not change the positive peak value of the GB. However, the negative peak value of the GB, and the GB settling time both depend on V_0 [8]. Furthermore, both of these quantities decrease as V_0 is reduced. Therefore, both the negative peak value, and the settling time of the GB voltage are expected to decrease for the charge recycling MTCMOS. Degrees of improvement in the negative peak and settling time are dependent on the relative values of L, C_G, R, V_{DD}, and the sleep transistor parameters. Figure 9 compares GB waveforms resulting from conventional and charge recycling power gating structures for an inverter chain in 70nm CMOS technology. As expected, the positive peak value remains the same for both cases; however, the negative peak value and the settling time are smaller for the charge- recycling MTCMOS structure.

5. SIMULATION RESULTS

We used HSPICE to find the wake up time and energy consumption during mode transition for a number of circuits from ISCAS benchmark suite for a 90nm CMOS technology.

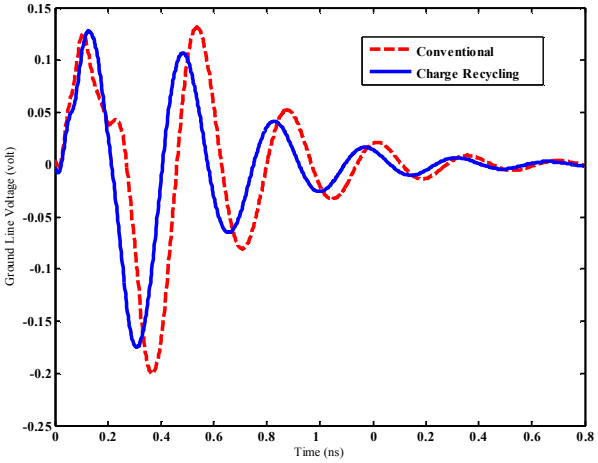

Figure 9. GB waveforms in conventional and CR structures for an inverter chain using 70nm CMOS technology.

Table 1 shows the experimental results in terms of the wake up time and energy consumption for a number of benchmarks when we use the conventional MTCMOS as well as the charge recycling MTCMOS. We observe from the table that energy saving during the mode transition is always more than 40% while the wake up time usually remains the same or improves slightly. However, for some cases e.g., C1908, we see that the energy saving ratio is 46% which is still more than 40%, but the wake up time has been increased by about 4%.

Table 1. Wake up time and energy consumption results.

Circuit	Wake up Time (pico second)		Mode Transition Energy Cons. (pico Jules)		Energy Saving	Wake up Time Reduction
	Conv.	CR	Conv.	CR		
9Sym	494	489.61	29	16	45%	0.9%
C432	240	232.73	10	5.7	43%	3%
C1355	132	125.42	12	7.2	40%	5%
C1908	267	275.63	38	20.5	46%	-3%
C2670	578	573	123	72.6	41%	0.9%
C3540	1500	1545	490	276.9	43%	-3%
C5315	1320	1307	638	357.3	44%	0.1%
C6288	2100	2047	1047	628.2	40%	2.5%
C7552	2310	2402	1532	842.6	45%	-4%

6. CONCLUSIONS

In this paper we introduced the concept of charge recycling (CR) in MTCMOS circuits. We showed that by applying the proposed CR technique to the MTCMOS circuits, we can save up to 50% of the mode transition energy while maintaining the wake up time of the original circuit. We also showed that by using the proposed technique, we can reduce the negative peak voltage value and the settling time of the ground bounce. Although leakage in the sleep mode of the circuit can go up as a result of the CR structure, the effect can be very well controlled by sizing down the TG, by judiciously selecting the HVT level to be used for both sleep transistors and charge recycling TG transistors in the first place, or even by using higher V_t values for the transistors in the TG compared to those for the sleep transistors. Since the subthreshold leakage current of a MOS transistor is exponentially dependent on the threshold voltage of the transistor, a slight increase in the threshold voltage value of the TG will result in a large difference in the resistance value of the gate, or in a large *n* value in equation (17), which makes the increase in the leakage power consumption negligible.

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