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Research Article

A Controllable Constant Power Generator in 0.35 μm CMOS Technology for Thermal-Based Sensor Applications

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A CMOS controllable constant power generator based on multiplier/divider circuit is presented. It generates constant power for a wide range of the resistive loads. For the generated power of 5 mW, and the resistance range from 0.5 kΩ to 1.5 kΩ, the relative error of dissipated power is less than 0.6%. For single supply voltage of 5 V, presented controllable constant power generator generates power from 0.5 mW to 7.8 mW, for the load resistance dynamic range from 3 up to 15, while the relative error of generated power is less than 2%. The frequency bandwidth of the proposed design is up to 5 MHz. Through the detailed analysis of the loop gain, it is shown that the circuit has no stability problems.

1. Introduction

The circuit which generates constant power for variable resistive loads finds application in various types of thermal-based sensors, such as mass flow meters, anemometers [1], AC power meters, gas monitoring [2, 3], plant water status monitoring [4], seepage meters [5], and other flowmeters intended for very slow fluids. Thermal-based flow sensors are very attractive because of their simple construction. They basically consist of constant power generator and sensing element. The surrounding fluid transfers heat to/from sensing element depending on its flow rate. As the temperature of the sensing element is changed, its resistance is changed, and the constant power generator changes the voltage drop across the sensing element to keep constant power. Measuring the voltage change across the sensing element, it is possible to extract the information about the fluid flow rate. So, the quality of the constant power generator as a part of the thermal-based sensor is very important. Controllable constant power generator is the circuit which generates constant power dissipation over a range of resistive loads. The control of the generated power is provided by control voltage or control current. The range of resistive loads has to be as large as possible for the particular generated power. In that sense, the quality of constant power generators is determined by the load resistance dynamic range, defined as the ratio of the largest load resistance to the smallest load resistance ($R_{L\max}/R_{L\min}$), for the particular value of dissipated power. The other important characteristic of the constant power generator is the value of generated power for a given load resistance, depending on specific application. The relative error of generated power over the range of load resistance is the key quality parameter of the constant power generator. Low-supply voltage of constant power generator is critical for many applications as a consequence of the general trend in electronics. The ratio of the largest voltage drop across the resistive load and supply voltage ($V_{L\max}/V_{DD}$) can be used as a quality indicator of constant power generators. One of the main problems in constant power generator design is its stability caused by feedback loops.

There are several designs of constant power generators, developed mostly in BiCMOS and bipolar technologies. A CMOS controllable constant power generator based on the resistive mirror [1] has the range of generated power from 0.48 mW to 10.8 mW, and the load resistance dynamic range up to 28, with the relative error of generated power less than 2.2% and the supply voltage of 10 V. The constant power generator presented in [1] uses four operational amplifiers OP97

which are designed in a complementary bipolar technology, while the rest of the circuit is realized using n-channel MOSFETs. Hence, the circuit [1] can be considered as a BiCMOS technology design. The controllable constant power generator [3], based on CMOS translinear loop, has a load resistance range from 470 Ω to 1.47 kΩ and is able to generate power up to 11 mW, with the supply voltage of ±5 V and the relative error of generated power up to 3%. The circuit presented in [3] uses off-chip operational amplifier LM301 designed in a complementary bipolar technology, while the rest of the circuit is realized in a CMOS technology. Hence, the circuit [3] can be considered as a BiCMOS technology design. Controllable constant power generator [4–6] can change the dissipated power by a factor of 1 : 1000, using the log-antilog circuit with bipolar junction transistors. This controllable constant power generator uses eight OPA4227 operational amplifiers designed in a complementary bipolar technology. Consequently, the circuit [4–6] can be considered as a bipolar technology design. The controllable constant power generator [7] in BiCMOS technology achieves load resistance range of 1 : 50, with generated power up to 100 mW. The microcontroller-based solution [9] can achieve large resistance dynamic range and large power dynamic range, but at the price of reduced frequency bandwidth. The CMOS design proposed in [10] for small variations of the resistive load has a large relative error of the generated power.

Taking into account that the existing designs of controllable constant power generators are designed mostly in BiCMOS and bipolar technologies and that CMOS technology is the most popular and the cheapest technology so far, the goal of this work is the design of fully integrated controllable constant power generator in a pure CMOS technology. This paper presents controllable constant power generator in 0.35 μm CMOS technology based on current-mode multiplier/divider circuit [8]. The generated power can be adjusted by two control currents which are the input currents of the multiplier/divider circuit. Through the detailed analysis and simulations, it is shown that proposed design is able to generate constant power over a large range of the load resistance. The mathematical model for the loop gain of the controllable constant power generator shows that circuit has no stability problems for a wide range of resistance for the particular generated power. The influence of the process parameter variations and the temperature variations to the proposed design is also analyzed.

2. Circuit Description

2.1. Basic Principle. The main purpose of the constant power generator is to maintain the constant power dissipation across the resistive load:

$$P_L = I_L V_L = \text{const}, \tag{1}$$

where P_L is the generated power across the resistive load, I_L is the current flowing through the resistive load, and V_L is the voltage across the resistive load. Generated power has to be independent of the load resistance. Also, it is desirable to have the possibility to control generated power easily.

The basic principle of the controllable constant power generator with a novel method for achieving a constant power dissipated on the resistive load is shown in Figure 1. It consists of multiplier/divider circuit, second generation current conveyor (CCII), load resistor R_L, reference resistor R_{REF}, and two DC current sources I_1 and I_2. The output current I_L of the multiplier/divider circuit is flowing through the resistive load R_L. The voltage V_L across the resistive load is transferred via CCII to the resistor R_{REF}. So, the output current I_3 of the CCII is given by

$$I_3 = \frac{V_L}{R_{\text{REF}}}. \tag{2}$$

On the other hand, the output current of the multiplier/divider circuit is given by

$$I_L = \frac{I_1 I_2}{I_3}. \tag{3}$$

So, the generated power P_L can be expressed as

$$P_L = I_L V_L = R_{\text{REF}} I_1 I_2 = \text{const}. \tag{4}$$

The generated power is independent of the load resistance R_L and can easily be adjusted by changing control currents I_1 and/or I_2.

2.2. Complete Circuit Schematic. The multiplier/divider circuit [8] is shown in Figure 2. It is based on the CMOS translinear principle. The circuit can be divided into two parts. The first part gives the current which is proportional to the square root of the product of two input currents (geometric mean) at its output. The second stage performs squarer/divider operation. The MOSFETs M_1, M_2, M_3, M_4, M_{1a}, M_{2a}, M_{3a}, and M_{4a} have long enough channels of 3 μm, so the channel length modulation effect can be neglected in the analysis. Assuming a good enough matching of MOSFETs forming the translinear loops ($V_{t1} = V_{t2} = V_{t3} = V_{t4}$, $V_{t1a} = V_{t2a} = V_{t3a} = V_{t4a}$, $\beta_1 = \beta_2 = \beta_3 = \beta_4$, and $\beta_{1a} = \beta_{2a} = \beta_{3a} = \beta_{4a}$) and a simple quadratic model for the drain current of the MOSFET operated in the saturated region, it can be shown [8] that the output current I_L of the multiplier/divider circuit is given by

$$I_L = \frac{I_1 I_2}{I_3}. \tag{5}$$

The second-order effects of the multiplier/divider circuits, such as channel length modulation effect and the threshold voltage mismatching effect, are analyzed in [8]. It is stated that the channel length modulation effect can be neglected for the long channel MOSFETs. On the other hand, the threshold voltage mismatching effect could affect the performances of the multiplier or divider circuit, assuming

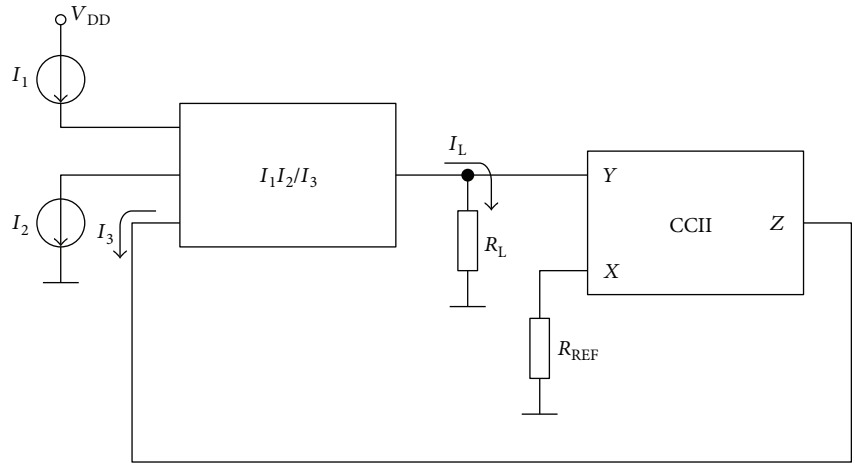

Figure 1: The principle of operation of the proposed controllable constant power generator.

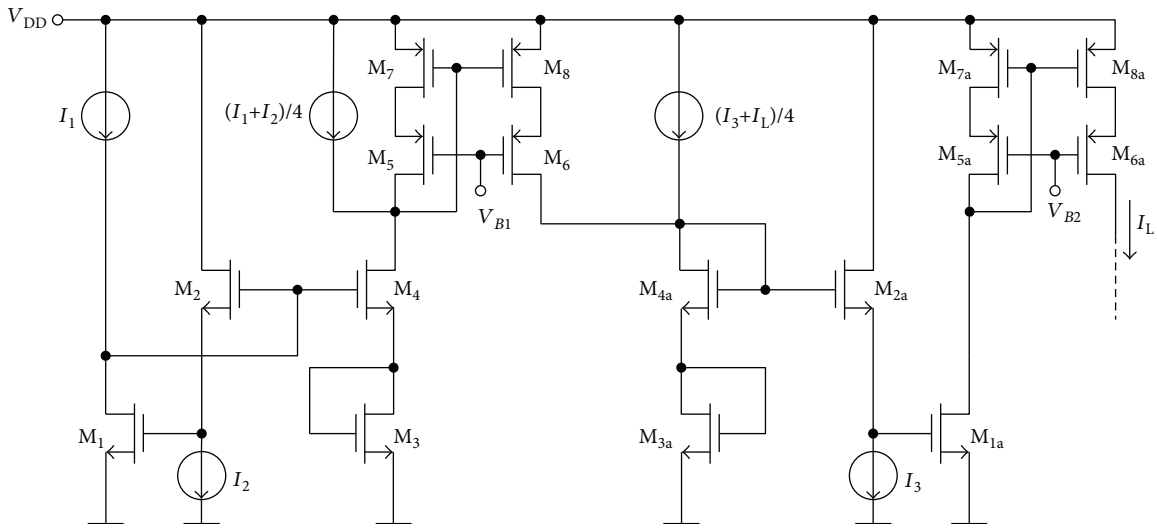

Figure 2: Multiplier/divider circuit schematic [8].

that the multiplier and divider are analyzed separately. On the other hand, if the multiplier and divider are used simultaneously within the multiplier/divider circuit, the threshold voltage mismatching effect is compensated [8]. The body effect of the n-channel MOSFETs in a real n-well CMOS implementation can be solved using n-channel MOSFETs with their own p-wells assuming a twin well technology.

The complete circuit schematic of the proposed controllable constant power generator with a novel method for achieving a constant power dissipated on the resistive load is shown in Figure 3. The output current of the multiplier/divider circuit is flowing through the resistive load R_L. The current I_3 is obtained as the output current of the CCII. The voltage V_L across the resistive load R_L is transferred via input stage of the CCII, so the current at terminal X of this CCII is V_L/R_{REF}. The differential input stage of the CCII is formed by the MOSFETs M_{12} and M_{13}, with the active cascoded load (MOSFETs M_{14}, M_{15}, M_{16}, and M_{17}). The differential input stage is biased by MOSFET M_{11} and biasing voltage V_{B3}. The output current is transferred by the two output cascoded current mirror (MOSFETs M_{18}, M_{19}, M_{20}, M_{21}, M_{22}, and M_{23}). So, the current at the output of the CCII is $I_3 = V_L/R_{REF}$. To change the direction of the current I_3, the wide-swing current mirror is used. This current mirror consists of MOSFETs M_{24}, M_{25}, M_{26}, and M_{27} and biasing voltage V_{B4}. The current I_L flowing through the resistive load R_L is mirrored by the current mirror formed by the MOSFETs M_{6a}, M_{8a}, M_9, and M_{10}. The current mirror formed by the MOSFETs M_{28}, M_{29}, M_{30}, and M_{31} is used to sum currents I_3 and I_L and to divide the sum of the currents by four. In that aim, the channel widths of the MOSFETs M_{28} and M_{30} are four times larger than the channel widths of the MOSFETs M_{29} and M_{31}. The direction of the resulting current is changed using the cascoded current mirror formed by MOSFETs M_{32}, M_{33}, M_{34}, and M_{35}.

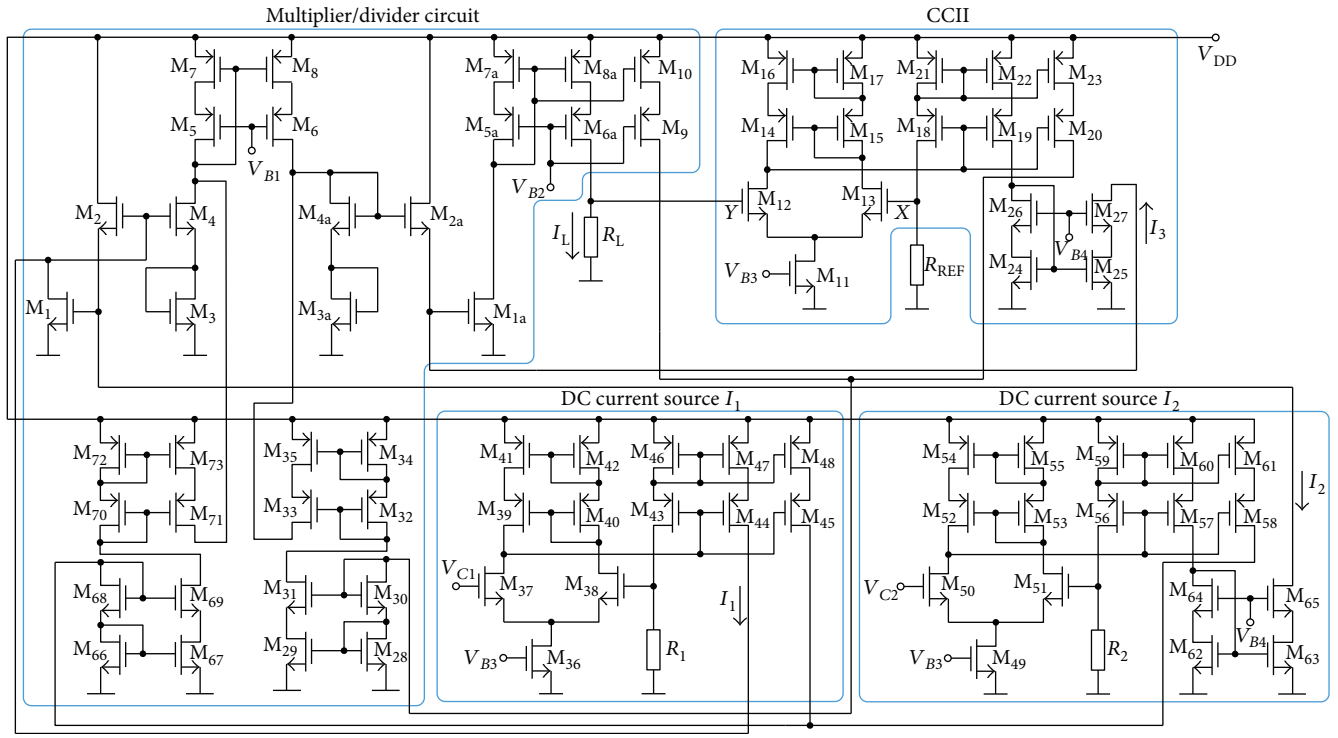

Figure 3: Complete circuit schematic of the proposed controllable constant power generator.

DC current source I_1 (I_2) is realized by using CCII. Its differential input stage is formed by the MOSFETs M_{37} and M_{38} (M_{50} and M_{51}), with the active cascoded load MOSFETs M_{39}, M_{40}, M_{41}, and M_{42} (M_{52}, M_{53}, M_{54}, and M_{55}). The differential input stage is biased by MOSFET M_{36} (M_{49}) and biasing voltage V_{B3}. The current at terminal X of this CCII is V_{C1}/R_1 (V_{C2}/R_2), and it is multiplied by the factor of eight by the two output cascoded current mirror MOSFETs M_{43}, M_{44}, M_{45}, M_{46}, M_{47}, and M_{48} (M_{56}, M_{57}, M_{58}, M_{59}, M_{60}, and M_{61}). So, the output current of this current source is $I_1 = 8V_{C1}/R_1$ ($I_2 = 8V_{C2}/R_2$). To change the direction of the current I_2, the wide-swing current mirror is used. This current mirror consists of MOSFETs M_{62}, M_{63}, M_{64}, and M_{65} and biasing voltage V_{B4}. The current mirror formed by MOSFETs M_{66}, M_{67}, M_{68}, and M_{69} is used to sum currents I_1 and I_2 and to divide the sum of the currents by four. In that aim, the channel widths of the MOSFETs M_{66} and M_{68} are four times larger than the channel widths of the MOSFETs M_{67} and M_{69}. The direction of the resulting current is changed using cascoded current mirror formed by MOSFETs M_{70}, M_{71}, M_{72}, and M_{73}.

The generated power of the proposed controllable constant power generator is given by

$$P_L = 64\frac{V_{C1}}{R_1}\frac{V_{C2}}{R_2}R_{\text{REF}}. \tag{6}$$

3. Stability Analysis

Controllable constant power generators usually suffer from stability problems [1, 3]. The range of resistive loads and the range of generated power are often reduced as a consequence of this problem [1, 3]. The stability analysis of the proposed controllable constant power generator is performed through the derivation of the loop gain $A\beta(s)$. In the small-signal analysis, the CCII, whose voltage input Y is connected to the active terminal of the resistive load (the output of the multiplier/divider circuit), is modelled as shown in Figure 4 [11, 12]. Capacitance C_X is the input capacitance at terminal X of the CCII, resistance R_X is the input resistance at terminal X of the CCII, capacitance C_Y is the input capacitance at terminal Y of the CCII, capacitance C_{Z1} is the output capacitance at terminal Z_1 of the CCII, resistance R_{Z1} is the output resistance at terminal Z_1 of the CCII, capacitance C_{Z2} is the output capacitance at terminal Z_2 of the CCII, and resistance R_{Z2} is the output resistance at terminal Z_2 of the CCII. The terminal X of the CCII is connected to the active terminal of the resistor R_{REF}. The terminal Y of the CCII is connected to the active terminal of the resistive load R_L. The terminal Z_1 of the CCII is connected to the source of the MOSFET M_{2a}, and the terminal Z_2 of the CCII is connected to the drain of the MOSFET M_9. Current mirrors within multiplier/divider circuit are modelled as simple ones.

The loop gain $A\beta(s)$ of the proposed controllable constant power generator is given by

$$A\beta(s) \approx \frac{g_{m1a}R_L}{g_{m2a}(R_X + R_{\text{REF}})}\frac{g_{m4a}g^2{}_{m28} + g_{m2a}g^2{}_{m34}}{g_{m4a}g^2{}_{m28} + g_{m1a}g^2{}_{m34}}\frac{\prod_{i=1}^{2}(1 + s/\omega_{Zi})}{\prod_{i=1}^{3}(1 + s/\omega_{pi})}, \tag{7}$$

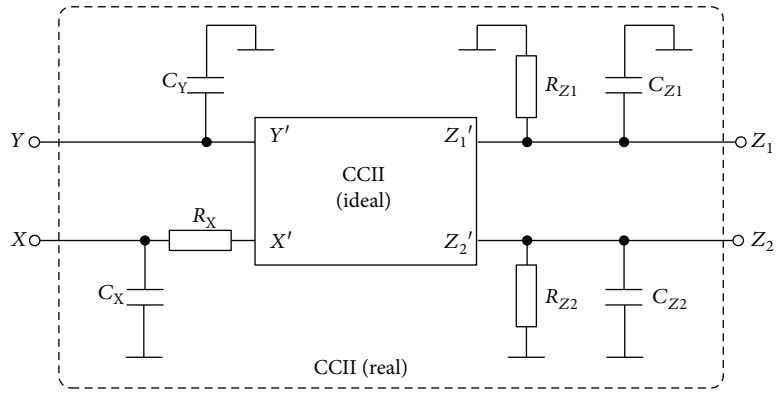

Figure 4: Small-signal model of the second generation current conveyor [11, 12].

where the zeroes ω_{zi} and the poles ω_{pi} are

$$\omega_{Z1} = \frac{1}{R_{\mathrm{REF}} C_X}, \tag{8}$$

$$\omega_{Z2} = \frac{g_{m4a}(C_{Z2} + C_4) + (g_{m28} + 1/R_{Z2})C_1}{C_1(C_{Z2} + C_4)}, \tag{9}$$

$$\omega_{p1} = \frac{1}{R_L(C_Y + C_3)}, \tag{10}$$

$$\omega_{p2} = \frac{1}{(R_X R_{\mathrm{REF}}/(R_X + R_{\mathrm{REF}}))C_X}, \tag{11}$$

$$\omega_{p3} = \frac{g_{m28}(g_{m28} + 1/R_{Z2})(g_{m2a} + 1/R_{Z1})C_1 + g_{m28}g_{m4a}(g_{m28} + 1/R_{Z2})(C_{Z1} + C_2) + g_{m28}g_{m4a}(g_{m2a} + 1/R_{Z1})(C_{Z2} + C_4)}{g_{m28}(g_{m28} + 1/R_{Z2})(C_{Z1} + C_2)C_1 + g_{m4a}g_{m28}(C_{Z1} + C_2)(C_{Z2} + C_4) + g_{m28}(g_{m2a} + 1/R_{Z1})(C_{Z2} + C_4)C_1}, \tag{12}$$

where g_{m1a}, g_{m2a}, g_{m3a}, g_{m4a}, g_{m28}, and g_{m34} are the transconductances of the saturated MOSFETs M_{1a}, M_{2a}, M_{3a}, M_{4a}, M_{28a}, and M_{34a}, respectively, C_1 is the parasitic capacitance at the drain of the MOSFET M_{4a}, C_2 is the parasitic capacitance at the gate of the MOSFET M_{1a}, C_3 is the parasitic capacitance at the drain of the MOSFET M_{6a}, and C_4 is the parasitic capacitance at the drain of the MOSFET M_9. It is calculated that the DC loop gain ranges from $|A\beta(s=0)| \approx 0.01$, for the lower limit of the resistive loads, to $|A\beta(s=0)| \approx 0.3$, for the upper limit of the resistive loads, for appropriate generated powers. The parasitic capacitances C_1, C_2, C_3, and C_4 are in the order of 1 pF, while the parasitic capacitances C_X, C_Y, C_{Z1}, and C_{Z2} are in the order of 100 fF. The transconductances of saturated MOSFETs are calculated as $g_{mi} = (2\beta_i I_{Di})^{1/2}$.

The absolute value of the loop gain frequency characteristic $|A\beta(j\omega)|$, for the lower limit of the resistive loads and for the appropriate generated powers, is shown in Figure 5. The frequency of the first zero ω_{z1} is about 150 MHz, the frequency of the next pole ω_{p2} is about 200 MHz, the frequency of the next pole ω_{p1} is between 300 MHz and 400 MHz, the frequency of the next pole ω_{p3} is in the order of 10 GHz, and the frequency of the last zero ω_{z2} is in the order of 100 GHz. The absolute value of the loop gain frequency characteristic $|A\beta(j\omega)|$, for the upper limit of the resistive loads and for the appropriate generated powers, is shown in Figure 6. The frequency of the first pole ω_{p1} is between 30 MHz and 130 MHz, the frequency of the next zero ω_{z1} is about 150 MHz, the frequency of the next pole ω_{p2} is about 250 MHz, the frequency of the next pole ω_{p3} is in the order of 10 GHz, and the frequency of the last zero ω_{z2} is in the order of 100 GHz. As the absolute value of the loop gain frequency characteristic $|A\beta(j\omega)|$ never reaches the value of 0 dB, the system is stable.

4. Simulated Results

The circuit is designed and simulated using PSpice with BSIM3 version 3.1 transistor model for TSMC 0.35 μm n-well CMOS process obtained by MOSIS. The circuit is single supplied by $V_{\mathrm{DD}} = 5$ V. Biasing voltages have the following values: $V_{B1} = 3$ V, $V_{B2} = 3.1$ V, $V_{B3} = 0.8$ V, and $V_{B4} = 1.9$ V. Resistances have the following values: $R_1 = 8$ kΩ, $R_2 = 8$ kΩ, and $R_{\mathrm{REF}} = 1.25$ kΩ.

The current I_L flowing through the resistive load as a function of the voltage V_L across the resistive load, for the

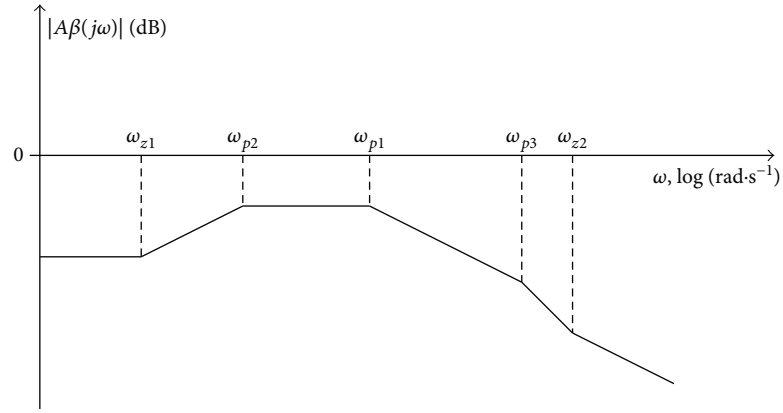

FIGURE 5: The absolute value of the loop gain frequency characteristic of the proposed controllable constant power generator, for the lower limit of the resistive loads and for the appropriate generated powers.

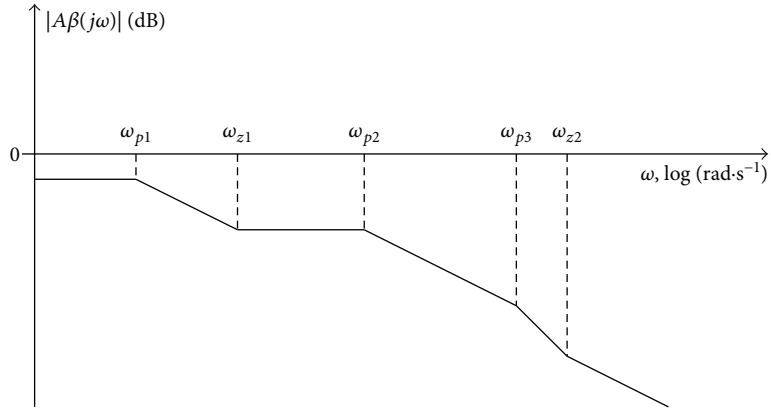

FIGURE 6: The absolute value of the loop gain frequency characteristic of the proposed controllable constant power generator, for the upper limit of the resistive loads and for the appropriate generated powers.

generated power $P_L = 5\,\text{mW}$, is shown in Figure 7. The resistance R_L is changed from $400\,\Omega$ to $2.2\,\text{k}\Omega$. Larger values of the voltage across the resistive load (corresponding to larger resistive load) are out of the input voltage range of the CCII, whose input is connected to the active terminal of the resistive load, for a given supply voltage. For larger values of the current flowing through the resistive load (corresponding to smaller resistive load), the multiplier/divider circuit shows larger errors caused by the channel length modulation of the MOSFET M_{1a}. The current I_L flowing through the resistive load increases rapidly with the decrease of the resistive load R_L due to square-hyperbolic dependence between them, $I_L = \sqrt{P_L}/\sqrt{R_L}$. The source-to-gate voltage V_{SG7a} of the MOSFET M_{7a} also increases rapidly, and the drain-to-source voltage V_{DS1a} of the MOSFET M_{1a} decreases rapidly.

Generated power P_L of 5 mW of the proposed controllable constant power generator for variable load resistances $500\,\Omega < R_L < 1.5\,\text{k}\Omega$ is shown in Figure 8. Relative error of generated power is $-0.6\% < E_L < 0.1\%$. The generated power is calculated (6), and the system is calibrated for the load resistance of $1\,\text{k}\Omega$.

Generated powers $P_L = \{0.5\,\text{mW}, 1\,\text{mW}\}$ of the proposed controllable constant power generator for variable load

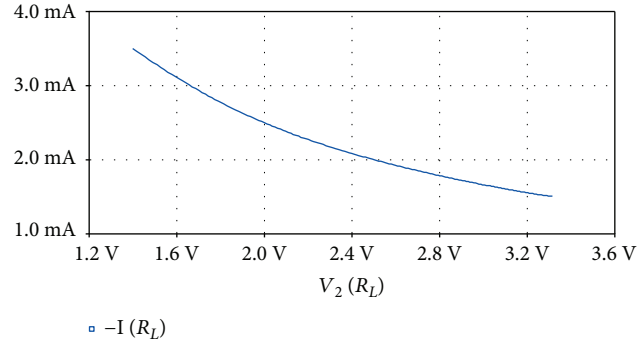

FIGURE 7: Current I_L flowing through the resistive load versus voltage V_L across the resistive load of the proposed controllable constant power generator, for generated power $P_L = 5\,\text{mW}$. The current $-\text{I}(R_L)$ is, in fact, the current I_L. The voltage $V_2(R_L)$ is the voltage V_L.

resistances $1\,\text{k}\Omega < R_L < 15\,\text{k}\Omega$ are shown in Figure 9. Generated powers $P_L = \{2\,\text{mW}, 3\,\text{mW}, 4\,\text{mW}, 5\,\text{mW}, 6\,\text{mW}, 7\,\text{mW}, 8\,\text{mW}, 9\,\text{mW}\}$ of the proposed controllable constant power generator for variable load resistances $400\,\Omega < R_L < 5.5\,\text{k}\Omega$ are shown in Figure 10. Table 1 shows summarized results

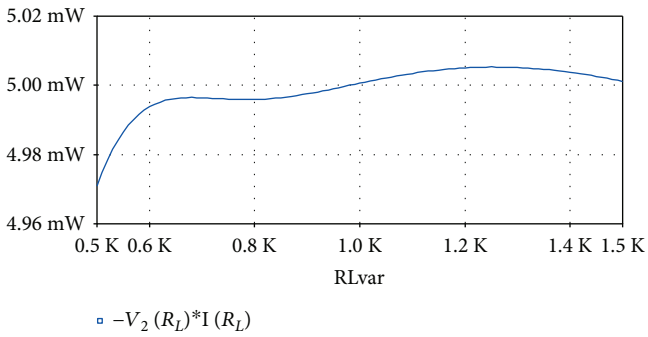

Figure 8: Generated power P_L versus load resistance R_L of the proposed controllable constant power generator, for control voltages $V_{C1} = 1.5$ V and $V_{C2} = 2.67$ V. The current $-I(R_L)$ is, in fact, the current I_L. The voltage $V_2(R_L)$ is the voltage V_L.

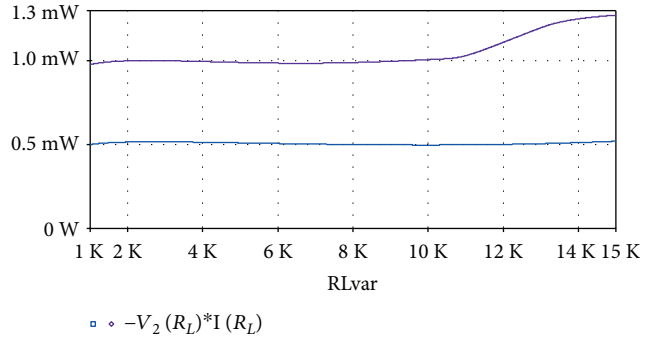

Figure 9: Generated powers $P_L = \{0.5\,\text{mW}, 1\,\text{mW}\}$ versus load resistance R_L of the proposed controllable constant power generator. The current $-I(R_L)$ is, in fact, the current I_L. The voltage $V_2(R_L)$ is the voltage V_L.

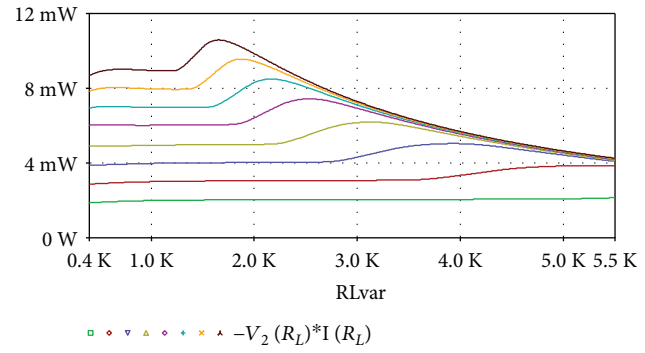

Figure 10: Generated powers $P_L = \{2\,\text{mW}, 3\,\text{mW}, 4\,\text{mW}, 5\,\text{mW}, 6\,\text{mW}, 7\,\text{mW}, 8\,\text{mW}, 9\,\text{mW}\}$ versus load resistance R_L of the proposed controllable constant power generator. The current $-I(R_L)$ is, in fact, the current I_L. The voltage $V_2(R_L)$ is the voltage V_L.

of the proposed controllable constant power generator. The range of resistive load R_L, for different values of dissipated power P_L, as well as the values of corresponding control voltages V_{C1} and V_{C2} is shown. The main demand was that the relative error of generated power is $|E_L| < 2\%$. For smaller generated power $0.5\,\text{mW} \le P_L \le 4\,\text{mW}$, the load resistance dynamic range is larger. It ranges from 15 ($1\,\text{k}\Omega \le R_L \le 15\,\text{k}\Omega$, for $P_L = 0.5\,\text{mW}$) to 7 ($0.4\,\text{k}\Omega \le R_L \le 2.8\,\text{k}\Omega$, for $P_L = 4\,\text{mW}$).

Table 1: Values of generated power P_L, resistive load R_L, control voltages V_{C1} and V_{C2}, for relative error of generated power $|E_R| < 2\%$.

P_L [mW]	R_L [kΩ]	V_{C1} [V]	V_{C2} [V]
0.5	$1 < R_L < 15$	0.67	0.6
1	$1 < R_L < 10$	1.33	0.6
2	$0.5 < R_L < 5.5$	0.6	2.67
3	$0.4 < R_L < 3.7$	0.9	2.67
4	$0.4 < R_L < 2.8$	1.2	2.67
5	$0.4 < R_L < 2.2$	1.5	2.67
6	$0.4 < R_L < 1.8$	1.8	2.67
7	$0.4 < R_L < 1.6$	2.1	2.67
8	$0.4 < R_L < 1.4$	2.4	2.67
9	$0.5 < R_L < 1.2$	2.7	2.67

For larger generated power $5\,\text{mW} \le P_L \le 9\,\text{mW}$, the load resistance dynamic range is smaller. It ranges from 5.5 ($0.4\,\text{k}\Omega \le R_L \le 2.2\,\text{k}\Omega$, for $P_L = 5\,\text{mW}$) to 2.4 ($0.5\,\text{k}\Omega \le R_L \le 1.2\,\text{k}\Omega$, for $P_L = 9\,\text{mW}$).

For smaller generated powers, the minimal value of the load resistance is limited by the input voltage offset of the CCII whose input is connected to the active terminal of the resistive load. That offset voltage is not constant over the all input voltage range of the current conveyor. Small absolute change of the offset voltage produces large enough relative change of the current I_3 that leads to the larger relative error of the generated power.

The main limitation for load resistance dynamic range, for all generated powers, is the supply voltage that directly affects the input voltage range of the CCII whose input is connected to the active terminal of the resistive load and the output current range of the multiplier/divider circuit. With larger supply voltage, it also would be possible to generate larger powers, as well as the larger range of generated powers.

In order to prove that the proposed controllable constant power generator is not particularly influenced by the process parameter variations, Monte Carlo simulations have been performed. The following process parameters have been changed within Monte Carlo simulations: carrier mobility, threshold voltage (for the source-to-bulk voltage $V_{SB} = 0$), body effect coefficient, and channel length modulation coefficient of all MOSFETs, as well as the resistances R_1, R_2, and R_{REF}. These values have been changed for 10% related to the nominal values for 100 runs. The nominal value of the generated power of $P_L = 5\,\text{mW}$ is changed with process parameter variations from 4.5 mW to 5.6 mW for the load resistance $500\,\Omega < R_L < 1.5\,\text{k}\Omega$. By analyzing the individual influence of a certain process parameter variations, it can be shown that the change of the generated power is dominantly caused by the variations of the resistances R_1, R_2, and R_{REF}. Although there is a change in the value of the generated power, it is important to stress that the relative error of the generated power is not affected by the process parameter variations. The absolute values of these relative errors range from 0.02% to 2.65% only. These relative errors are calculated

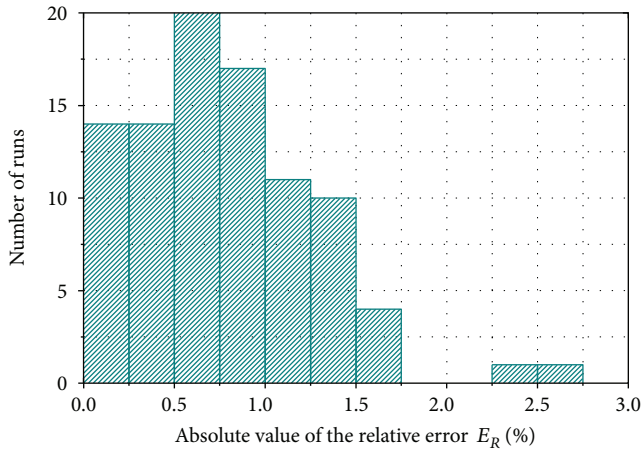

FIGURE 11: Distribution of the absolute value of the relative error E_R.

related to the power generated for the load resistance $R_L = 1\,\text{k}\Omega$ for each corresponding run. Distribution of these relative errors in the form of a histogram is shown in Figure 11. The absolute value of the relative error is less than 0.5% in 28% runs, less than 1% in 73% runs, and less than 1.5% in 95% runs.

In order to investigate the temperature influence to the proposed design, the generated power $P_L = 5\,\text{mW}$ of the controllable constant power generator for variable load resistance $0.5\,\text{k}\Omega < R_L < 1.5\,\text{k}\Omega$ with the temperature used as a parameter $T \in \{-20^\circ\text{C}, -10^\circ\text{C}, 0^\circ\text{C}, 10^\circ\text{C}, 20^\circ\text{C}, 30^\circ\text{C}, 40^\circ\text{C}, 50^\circ\text{C}, 60^\circ\text{C}, 70^\circ\text{C}, 80^\circ\text{C}\}$ has been simulated. Two types of the simulations have been performed. In the first one shown in Figure 12, the resistances R_1, R_2, and R_{REF} are constant, that is, temperature independent. In the second type shown in Figure 13, the temperature influence to the resistances R_1, R_2, and R_{REF} is modeled by using the linear temperature coefficient $\alpha = -3\times10^{-3}/\text{K}$. This is the typical value of the linear temperature coefficient of the resistor made by using a high resistivity poly in a standard 0.35 μm CMOS technology. The relative error is calculated related to the power generated for the load resistance $R_L = 1\,\text{k}\Omega$ at $T = 27^\circ\text{C}$. For the temperature-independent resistance R_1, R_2, and R_{REF} (Figure 12), the absolute value of the relative error is up to 8%. On the other hand, for the temperature-dependent resistances R_1, R_2, and R_{REF} (Figure 13), the absolute value of the relative error ranges is up to 12%. It is clear that the proposed controllable constant power generator is dominantly influenced by the temperature variations of the resistances R_1, R_2, and R_{REF} compared to the influence of the temperature variations of the active components. In order to reduce the temperature influence to the proposed design, according to the relation (6), either the resistors R_{REF} and R_1, or R_{REF} and R_2 have to be of the same type, while either the resistor R_2 or the resistor R_1 has to be designed with predetermined temperature coefficient (e.g., zero temperature coefficient). To that aim, either the resistor R_2 or the resistor R_1 can be designed as a composite one [13–15] with predetermined (zero) temperature coefficient. With this composite resistor, it can be expected that the overall temperature influence to the proposed controllable constant power generator will be similar to that shown in Figure 12 or even smaller. For the specific application of the proposed design in the plant tissue humidity measurements in the open arable field, the temperature range of interest is from 0°C to 50°C. In that case, the absolute value of the relative error is up to 3.5% for the temperature-independent resistances R_1, R_2, and R_{REF} and up to 8% for the temperature-dependent resistances R_1, R_2, and R_{REF}.

Simulations of the frequency response of the CCII M_{11}-M_{23} (Figure 3) are shown in Figures 14 and 15. The DC biasing voltage at the terminal Y of the CCII is used as a parameter and is changed from 0.7 V to 3.28 V with a step of 0.43 V. This DC biasing voltage corresponds to the DC voltage V_L across the resistive load R_L for the generated powers $0.5\,\text{mW} < P_L < 9\,\text{mW}$ and corresponding load resistance range. The load at the terminal Z is presented by the wide-swing current mirror M_{24}-M_{27}, with the drain of the MOSFET M_{27} connected to the supply voltage source V_{DD}. The CCII has been optimized to achieve the gain-peaking less than 3 dB in the frequency responses for all ranges of the DC biasing voltage at the terminal Y of the CCII. The frequency voltage transfer characteristic v_x/v_y is shown in Figure 14. The bandwidth ranges from 39 MHz ($V_Y = 0.7\,\text{V}$, $P_L = 0.5\,\text{mW}$) to 125 MHz ($V_Y = 3.28\,\text{V}$, $P_L = 9\,\text{mW}$). The frequency transconductance transfer characteristic i_z/v_y is shown in Figure 15. The bandwidth ranges from 39 MHz ($V_Y = 0.7\,\text{V}$, $P_L = 0.5\,\text{mW}$) to 137 MHz ($V_Y = 3.28\,\text{V}$, $P_L = 9\,\text{mW}$).

In order to prove that the proposed controllable constant power generator is stable, simulations of the transient response to a step change of the load resistance R_L have been performed. The voltage-controlled resistor [12, 16] is used as the resistive load R_L in order to simulate the step change of the resistance, Figure 16. The voltage follower within the voltage-controlled resistor is designed similar to that in [12], but with MOSFETs only. The resistors within the resistive voltage divider have the same resistances, $R_3 = R_4$. The load resistance is a step changed from $R_L = 0.707\,\text{k}\Omega$ to $R_L = 1.299\,\text{k}\Omega$, as the control voltage is a step changed from $V_C = 2.5\,\text{V}$ to $V_C = 1.6\,\text{V}$. The rise time and the fall time of the load resistance are 28 ns and 19 ns, respectively. The voltage V_L across the voltage-controlled resistor (resistive load R_L) is shown in Figure 17. The product of the voltage V_L and the current I_L of the voltage-controlled resistor is constant and equal to $P_L = V_L I_L = 5\,\text{mW}$. It can be seen that there is no overshoot in the transient responses which confirms the unconditional stability of the proposed design predicted by the mathematical model expressed by (7), (8), (9), (10), (11), and (12) and Figures 5 and 6. In addition, it can be estimated that the largest frequency bandwidth in the considered example is up to 5 MHz.

5. Discussion and Conclusions

Proposed controllable constant power generator based on multiplier/divider circuit is designed and simulated in 0.35 μm CMOS technology. It is possible to generate small power from 0.5 mW to 1 mW for load resistance from 2.5 kΩ to 10 kΩ (variation from −50% to 100%, for the load

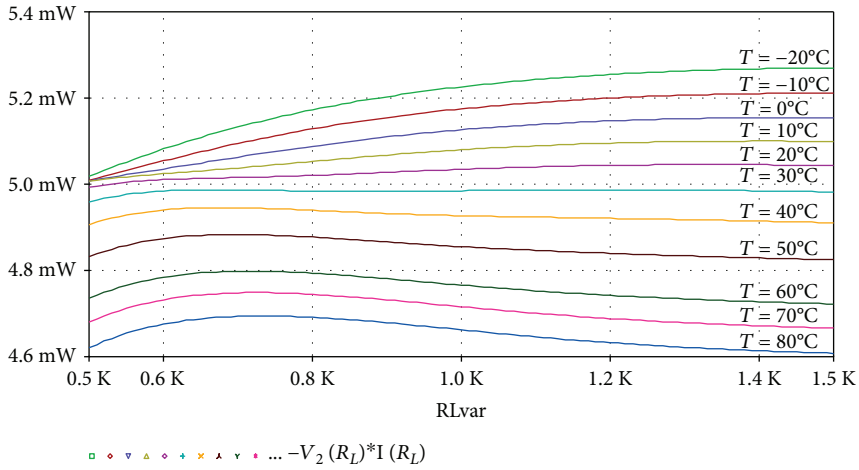

Figure 12: The generated power $P_L = 5$ mW of the proposed controllable constant power generator versus load resistance for temperatures $T \in \{-20^\circ C, -10^\circ C, 0^\circ C, 10^\circ C, 20^\circ C, 30^\circ C, 40^\circ C, 50^\circ C, 60^\circ C, 70^\circ C, 80^\circ C\}$, with temperature-independent resistors. The current $-I(R_L)$ is, in fact, the current I_L. The voltage $V_2(R_L)$ is the voltage V_L.

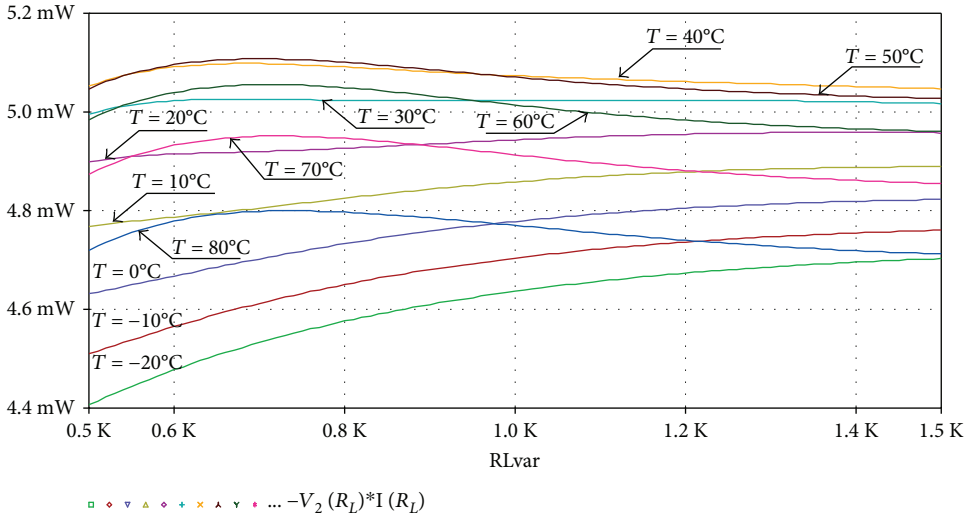

Figure 13: The generated power $P_L = 5$ mW of the proposed controllable constant power generator versus load resistance for temperatures $T \in \{-20^\circ C, -10^\circ C, 0^\circ C, 10^\circ C, 20^\circ C, 30^\circ C, 40^\circ C, 50^\circ C, 60^\circ C, 70^\circ C, 80^\circ C\}$, with temperature-dependent resistors. The current $-I(R_L)$ is, in fact, the current I_L. The voltage $V_2(R_L)$ is the voltage V_L.

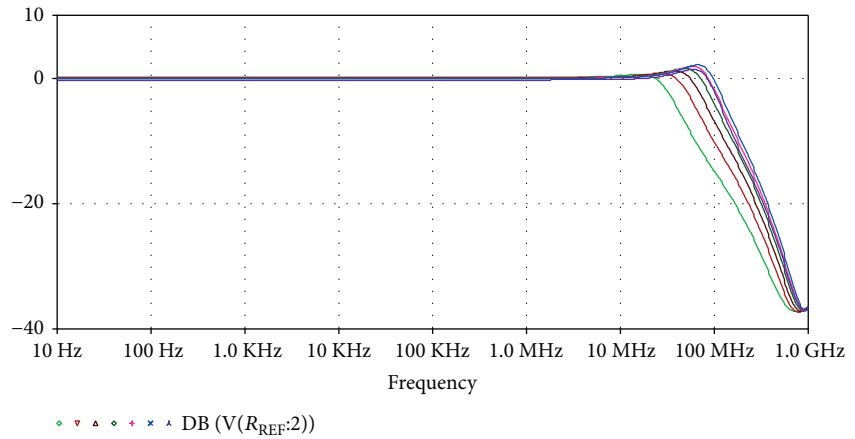

Figure 14: The frequency voltage transfer characteristic v_x/v_y. The voltage $V(R_{REF}:2)$ is, in fact, the voltage v_x.

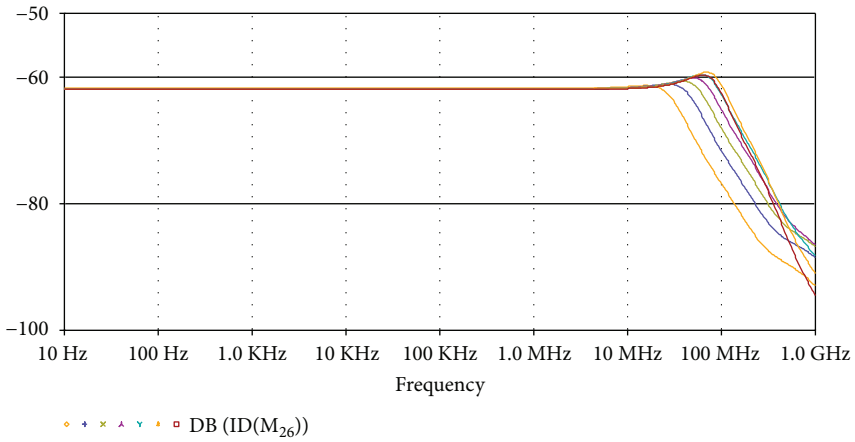

Figure 15: The frequency transconductance transfer characteristic i_z/v_y. The current ID(M_{26}) is, in fact, the current i_z.

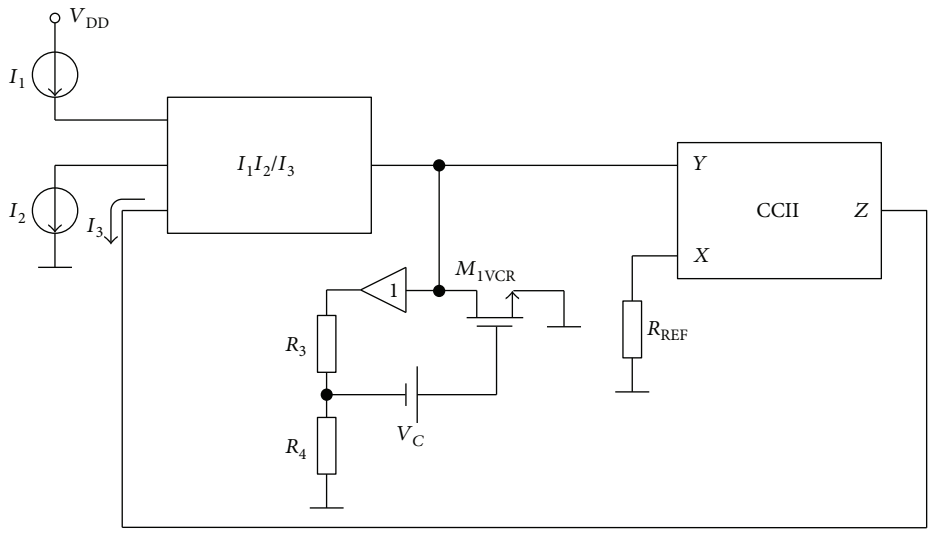

Figure 16: The circuit used for simulations of the transient response to a step change of the load resistance R_L using voltage-controlled resistor.

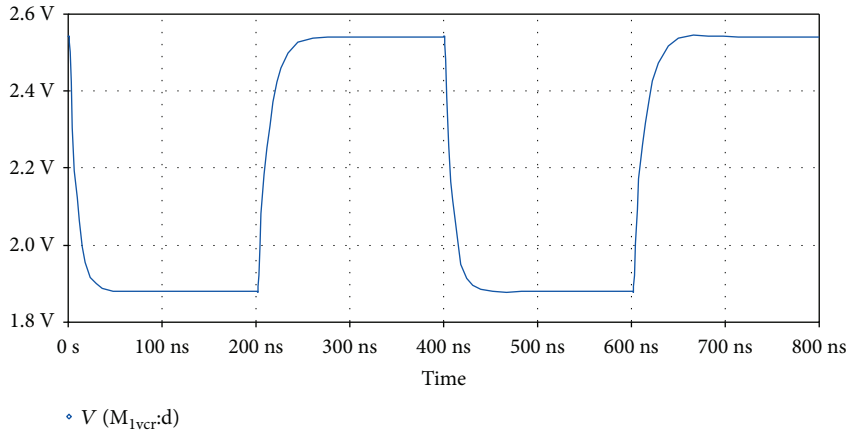

Figure 17: The output voltage of the controllable constant power generator for step change of the resistive load from $R_L = 0.707\,\text{k}\Omega$ to $R_L = 1.299\,\text{k}\Omega$. The voltage V($M_{1vcr}$:d) is, in fact, the output voltage of the controllable constant power generator in this analysis.

Table 2: Values of generated power P_L and corresponding relative error E_R, for resistive load $2.5\,\text{k}\Omega < R_L < 10\,\text{k}\Omega$.

P_L (mW)	E_R (%)
0.5	$-0.8 < R_L < 1.2$
1	$-0.9 < R_L < 0.5$

Table 3: Values of generated power P_L and corresponding relative error E_R, for resistive load $500\,\Omega < R_L < 1.5\,\text{k}\Omega$.

P_L (mW)	E_R (%)
2	$-2 < R_L < 1.5$
3	$-1.95 < R_L < 0.6$
4	$-1.9 < R_L < 0.35$
5	$-0.6 < R_L < 0.1$
6	$-0.1 < R_L < 0.3$
7	$-0.7 < R_L < 0.2$
7.8	$-1 < R_L < 2$

resistance $R_L = 5\,\text{k}\Omega$), with the relative error of generated power less than 1.2%. These results are shown in Table 2. Also, it is possible to generate larger power from 1 mW to 7.8 mW for load resistance from 0.5 kΩ to 1.5 kΩ (variation of ±50%, for the load resistance $R_L = 1\,\text{k}\Omega$), with the relative error of generated power less than 2%. These results are shown in Table 3. The circuit is optimized for 5 V single supply. The ratio of the largest voltage drop across the resistive load and the supply voltage ($V_{L\text{max}}/V_{\text{DD}}$) is 68%, which is a better result than 58% in [1], 40.6% in [3], and 44% in [4–6]. The supply voltage and power dissipation of the circuit are limiting factors in many applications, especially in the open field, powered by the solar cells. For different applications, where power consumption of the circuit is not critical, it would be possible to generate larger power, with wider load resistance dynamic range, with a higher value of the supply voltage.

Compared to the design presented in [1], proposed controllable constant power generator, for the load resistance range from 500 Ω to 1.5 kΩ, has the smaller range of generated power, with the same level of relative error, but with the 5 V single supply, compared to 7 V single supply. The design presented in [1] has larger load resistance dynamic range, but with 10 V single supply. Compared to the design presented in [3], proposed controllable constant power generator, for the load resistance range from 500 Ω to 1.5 kΩ, has the smaller range of generated power, but the smaller relative error with the 5 V single supply, compared to ±5 V supply voltage. The proposed controllable constant power generator also has larger load resistance dynamic range for the particular generated power, compared to the design presented in [3]. The largest relative error of the proposed design is 6 times smaller than in [10] for the same load resistance range, for the generated power $0.5\,\text{mW} < P_L < 12\,\text{mW}$. The frequency bandwidth of the proposed controllable constant power generator is approximately 500 times larger than in [1] and more than 6400 times larger than in [9]. The performance comparison between the proposed controllable constant power generator and controllable constant power generators presented in [1, 3], for resistive load $0.5\,\text{k}\Omega < R_L < 1.5\,\text{k}\Omega$ is given in Table 4. The proposed design has no stability problems for all generated powers over a wide range of the resistive loads. Based on achieved results, it can be concluded that the controllable constant power generator can be used in various thermal-based sensor applications.

Table 4: Performance comparison between the proposed controllable constant power generator and previous controllable constant power generators.

	[1]	[3]	This work*
$\lvert E_R\,(\%)\rvert_{\text{max}}$	2.2	3	2
$P_{L\text{min}}$ (mW)	0.48	—	2
$P_{L\text{max}}$ (mW)	10.8	11	7.8
$R_{L\text{min}}$ (kΩ)	0.5	0.5	0.5
$R_{L\text{max}}$ (kΩ)	1.5	1.5	1.5
Supply voltage (V)	7	±5	5
$V_{L\text{max}}/V_{\text{DD}}$ (%)	58	40.6	68
$f_{-3\,\text{dB}}$ (kHz)	10	—	5000

*Simulated.

Conflicts of Interest

The author declares that there is no conflict of interest regarding the publication of this paper.

Acknowledgments

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