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Research Article

A Three-Phase Interleaved Floating Output Boost Converter

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High step-up dc-dc converter is an essential part in several renewable energy systems. In this paper, a new topology of step-up dc-dc converter based on interleaved structure is proposed. The proposed converter uses three energy storing capacitors to achieve a high voltage gain. Besides the high voltage gain feature, the proposed converter also reduces the voltage stress across the semiconductor switches. This helps in using low rating switching devices which can reduce the overall size and cost of the converter. The operating principle of the proposed converter is discussed in detail and its principle waveforms are analyzed. An experiment is carried out on a 20 V input, 130 V output, and 21 W power prototype of the proposed converter in the laboratory to verify the performance of the proposed converter. An efficiency of 91.3% is achieved at the rated load.

1. Introduction

Several applications require high step-up dc-dc voltage conversion. One of the most common applications is the photovoltaic energy sources where the low input voltage should be stepped-up to high dc-link voltage. Other applications include fuel cell, hybrid electric vehicle (HEV), high-intensity discharge lamp ballasts, and uninterruptible power supplies. A high step-up dc-dc converter is essential for such kind of applications. For such type of high step-up dc-dc voltage conversion, a traditional boost converter shown in Figure 1 will operate at very high duty cycle (above 80%) as the voltage gain of a simple boost converter is $1/1 - D$. Such high duty cycle will cause severe reverse recovery problem of the output diode. Also the switches in the simple boost converter will experience a high voltage stress as their voltage stress is equal to the output voltage. Moreover, it needs large filter elements to minimize the ripples as it has only one inductor with no ripple cancellation. For this purpose, various high step-up topologies have been reported in the literature [1–3].

Two-stage/quadratic boost converter comprising two boost converters can be used to achieve high voltage gain as the voltage gain is equal to the product of the gains of two boost converters, that is, $1/(1-D)^2$. However, using two boost converters may degrade the overall efficiency as the overall efficiency is also equal to the product of the efficiencies of two boost converters [4–6]. Inductorless switched capacitor circuits can give high step-up voltage conversion ratio, but they use a large number of switches and gate drives. The efficiency of switched capacitor circuit also is poor [7, 8]. Interleaved or parallel structure is well known for reducing the ripples due to its well-known feature of ripple cancellation among the phases. Moreover, it can handle more power, but it does not help in increasing the step-up voltage gain or reducing the voltage stress on switches [9].

Tapping among the inductors and coupling of various inductors can achieve high step-up voltage conversion ratio by adjusting the turn ratio. However, it is very difficult to perfectly couple inductors and the existence of leakage inductance can create problems of large voltage overshoots [10–14]. Boost converter employing voltage multiplier and three-state switching cells can achieve high voltage gain and also reduces ripple in input current. But the voltage gain of one multiplier cell is not much high and for a very high step-up voltage conversion more numbers of multipliers cells will be needed [15, 16]. Isolated converters such as half-bridge, full-bridge, and flyback can achieve high step-up voltage conversion by adjusting the turn ratio of the transformer. But

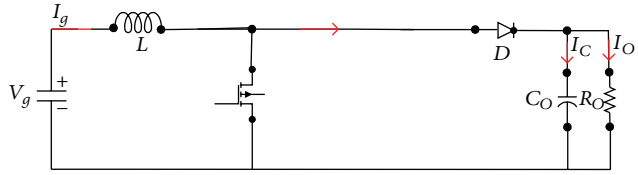

Figure 1: Circuit diagram of traditional boost converter.

they have their own problems related to transformers and are more expensive as compared to nonisolated types [17].

To achieve high voltage gain and lower switch stress, a new topology of dc-dc converter is presented in this paper. The circuit diagram is shown in Figure 2. The proposed converter is a three-phase interleaved boost converter with an intermediate capacitor and two output capacitors which forms the floating output. The proposed converter can achieve a very high voltage gain as well as reduce the voltage stress of switches.

2. Operating Principle of the Proposed Converter

Figure 2 shows the circuit diagram of the proposed converter. It consists of three phases with L_1 being the filtering inductor of phase #1, L_2 being the inductor of phase #2, and L_3 being the filtering inductor of phase #3. Transistors S_1, S_2, and S_3 are the main switches of phase #1, phase #2, and phase #3, respectively. Similarly, D_1, D_2, and D_3 are the rectifying diodes of three phases. V_S is the supply voltage, V_O is the output voltage, and R_L is load resistor. For the analysis of the proposed converter the following assumptions are made:

(i) $L_1 = L_2 = L_3 = L$ (where L is the inductance/phase),

(ii) $C_1 = C_2 = C$ (where C is the filter capacitor),

(iii) all capacitors and inductors are very large, so that their ripples are very small,

(iv) the converter always operates in continuous conduction mode (CCM).

The operation of the converter is done at a fixed switching frequency F_S and it has a fixed switching period of T_S. The operation is such that switches S_1, S_2, and S_3 are turned on and off by two PWM signals which is 180-degree phase shifted. One PWM signal is applied to the gate of S_2 and another PWM signal which is 180-degree phase shifted from the first one is applied to the gates of S_1 and S_3. There is no phase shift between phase #1 and phase #3 and both these phases are at 180-degree phase shift with phase #2. The converter is analyzed for a duty cycle D greater than 50%. There are total four switching states in one switching period. Figure 3 shows the circuit diagram of the proposed converter formed in each state and Figure 4 shows steady state waveforms for the proposed converter.

State-I ($t_O \le t \le t_1$). State-I starts at $t = t_O$ when all the transistors S_1–S_3 are turned on. During this state all the diodes D_1–D_3 remain off. Figure 3(a) shows the circuit topology of the proposed converter formed in this state. Inductors L_1, L_2, and L_3 get charged by the supply voltage V_S and the currents I_1, I_2, and I_3 through them increase with slopes of V_S/L. Capacitor C_{in} is disconnected from the supply as well as from the load; it neither charges nor discharges and its voltage $V_{C_{\text{in}}}$ is constant. Both the output capacitors C_1 and C_2 discharge to the load and their voltages V_{C_1} and V_{C_2} fall with slopes of $-V_O/(R_LC)$.

State-II ($t_1 \le t \le t_2$). State-II begins when switches S_1 and S_3 are turned off at $t = t_1$. The switch S_2 is still on. Diodes D_1 and D_3 start conducting, whereas diode D_2 is still off. Figure 3(b) shows the circuit topology formed in this state. Inductor L_2 is still in charging mode and its current I_2 rises with a slope of V_S/L. Inductors L_1 and L_3 are in discharge modes and their currents I_1 and I_3 fall with slopes of $(V_S - V_{C_{\text{in}}})/L$ and $(V_S - V_{C_2})/L$, respectively. Capacitor C_1 is still in discharge mode and its voltage V_{C_1} is still decreasing with same slope of $-V_O/(R_LC)$. Capacitors C_{in} and C_2 are charged up by the supply and their voltages $V_{C_{\text{in}}}$ and V_{C_2} rises with slopes of I_1/C_{in} and $I_3/C - V_O/(R_LC)$. This state ends at $t = t_2$.

State-III ($t_2 \le t \le t_3$). This state is similar to state-I. Again all the transistors are on and all the diodes are off. The circuit diagram is the same as in state-I (Figure 3(a)).

State-IV ($t_3 \le t \le t_4$). This state begins when switch S_2 is turned off at $t = t_3$. Switches S_1 and S_3 are still off. Diode D_2 starts conducting and diodes D_1 and D_3 remain off. Figure 3(c) shows the circuit topology formed in this state. Inductors L_1 and L_3 are charged by the supply and their currents I_1 and I_3 rise with slopes of V_S/L. Inductor L_2 discharges and its current I_2 decreases with a slope of $(V_S + V_{C_{\text{in}}} - V_{C_1})/L$. Capacitor C_{in} discharges to load and its voltage $V_{C_{\text{in}}}$ falls with a slope of $-I_2/C_{\text{in}}$. Capacitor C_1 gets charged and its voltage V_{C_1} rises with a slope of $I_2/C - V_O/(R_LC)$. Capacitor C_2 also discharges to load and its voltage falls with a slope of $-V_O/(R_LC)$. This state ends at $t = t_4$.

3. Steady State Analysis of the Proposed Converter

To simplify the analysis of the proposed converter, the time of each state is expressed in terms of duty cycle D and switching period T_S as

$$\begin{aligned} t_O &= 0 \text{ sec}, \\ t_1 &= \left(DT_S - \frac{T_S}{2}\right) \text{ sec}, \\ t_2 &= \frac{T_S}{2} \text{ sec}, \\ t_3 &= DT_S \text{ sec}, \\ t_4 &= T_S \text{ sec}. \end{aligned} \tag{1}$$

3.1. DC Conversion Ratio. For the voltage conversion ratio M of the proposed converter we will apply the principle of

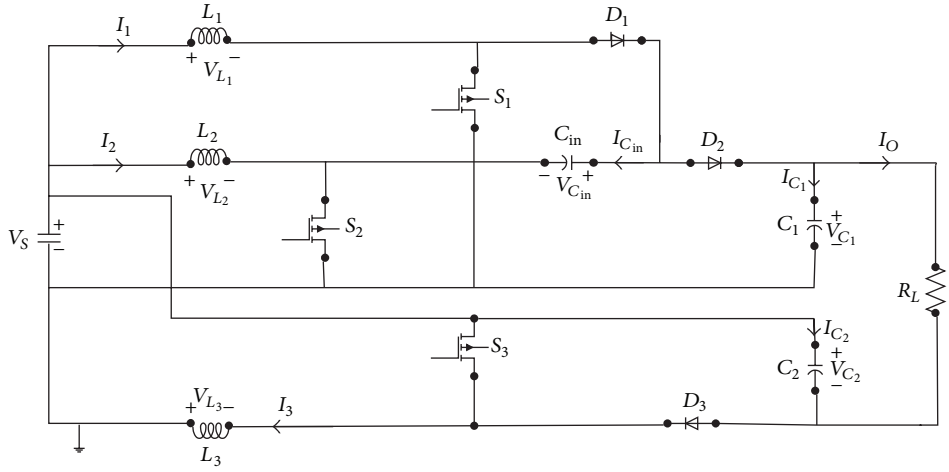

Figure 2: Circuit diagram of the proposed converter.

inductor volt second balance (VSB) on inductors L_1, L_2, and L_3. By VSB of inductor L_1 we get

$$V_S(t_1 - t_O) + \left(V_S - V_{C_{in}}\right)(t_2 - t_1) + V_S(t_3 - t_2) + V_S(t_4 - t_3) = 0. \tag{2}$$

The solution of (2) gives

$$V_{C_{in}} = \frac{V_S}{(1-D)}. \tag{3}$$

By VSB of inductor L_2 we get

$$V_S(t_1 - t_O) + V_S(t_2 - t_1) + V_S(t_3 - t_2) + \left(V_S + V_{C_{in}} - V_{C_1}\right)(t_4 - t_3) = 0. \tag{4}$$

The solution of (4) gives

$$V_{C_1} = \frac{V_S}{(1-D)} + V_{C_{in}}. \tag{5}$$

From (3) and (5) we get

$$V_{C_1} = \frac{2V_S}{(1-D)}. \tag{6}$$

By VSB of inductor L_3 we get

$$V_S(t_1 - t_O) + \left(V_S - V_{C_2}\right)(t_2 - t_1) + V_S(t_3 - t_2) + V_S(t_4 - t_3) = 0. \tag{7}$$

The solution of (7) gives

$$V_{C_2} = \frac{V_S}{(1-D)}. \tag{8}$$

The output capacitors C_1 and C_2 remain in series with the supply voltage V_S and therefore the output voltage V_O of the proposed converter is given by

$$V_O = V_{C_1} + V_{C_2} - V_S. \tag{9}$$

By (6), (8), and (7) we get

$$V_O = \left\{\frac{(2+D)}{(1-D)}\right\} V_S. \tag{10}$$

And the voltage conversion ratio M is

$$M = \frac{V_O}{V_S} = \frac{(2+D)}{(1-D)}. \tag{11}$$

3.2. Voltage Stress of Semiconductor Devices. Switches S_1 and S_3 are off in state-II and remain on in the rest of switching period. Referring to Figure 3(b), the off-state voltage (voltage stress) of switches S_1 and S_2 can be obtained as

$$V_{S_1} = V_{C_{in}} = \frac{V_S}{(1-D)}, \qquad V_{S_2} = V_{C_1} - V_{C_{in}} = \frac{V_S}{(1-D)}. \tag{12}$$

Switch S_2 is off only in state-IV. Referring to Figure 3(c) the voltage stress V_{S_3} of switch S_3 is given by

$$V_{S_3} = V_{C_2} = \frac{V_S}{(1-D)}. \tag{13}$$

In similar way the maximum voltage drop (voltage stress) of the diodes D_1, D_2, and D_3 can be found out and is given by

$$V_{D_1} = -V_{C_1} = -\frac{2V_S}{(1-D)}, \qquad V_{D_2} = -V_{C_2} + V_{C_{in}} = -\frac{V_S}{(1-D)}, \qquad V_{D_3} = V_{C_2} = \frac{V_S}{(1-D)}. \tag{14}$$

3.3. Ripple Current and Ripple Voltage. Referring to Figure 4, the peak to peak ripple Δi_1 in the current I_1, peak to peak

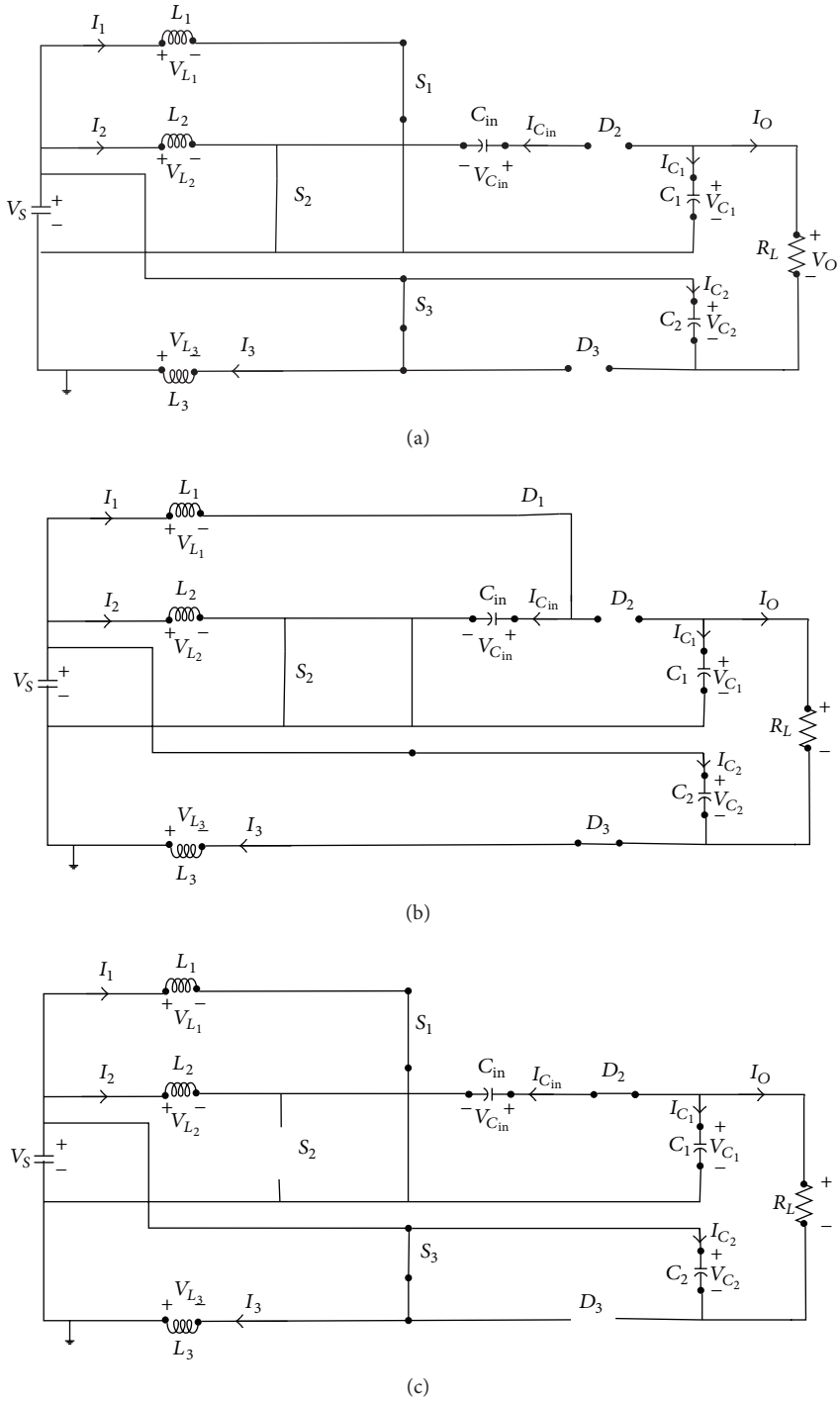

Figure 3: Operating circuits of the proposed converter. (a) State-I and state-III, (b) state-II, and (c) state-IV.

ripple Δi_2 in current I_2, and peak to peak ripple Δi_3 in current I_3 are expressed as

$$\Delta i_1 = \Delta i_2 = \Delta i_3 = \frac{(DV_S)}{(LF_S)}. \tag{15}$$

Similarly, the peak to peak ripple $\Delta V_{C_{in}}$ in voltage $V_{C_{in}}$ can be expressed as

$$\Delta V_{C_{in}} = \frac{V_O}{(R_L C_{in} F_S)}. \tag{16}$$

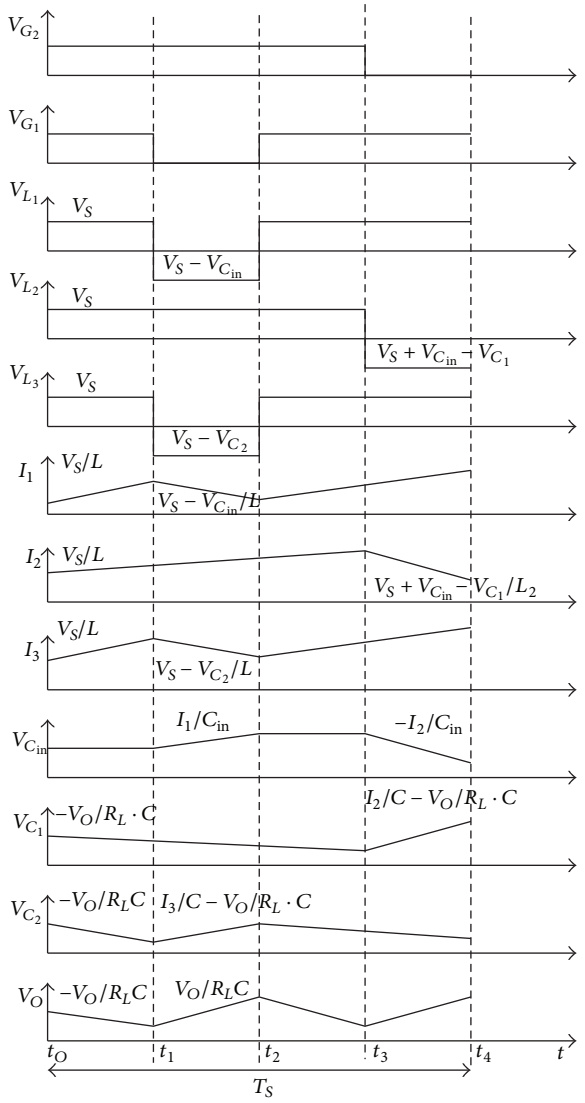

Figure 4: Steady state waveforms of the proposed converter.

The peak to peak ripple ΔV_{C_1} in voltage V_{C_1} and ΔV_{C_2} in voltage V_{C_2} are given by

$$\Delta V_{C_1} = \Delta V_{C_2} = \frac{(DV_O)}{(R_L C F_S)}. \tag{17}$$

The peak to peak ripple ΔV_O in the output voltage V_O is given by

$$\Delta V_O = \{(2D-1)\, V_O\}\, (R_L C F_S)\,. \tag{18}$$

4. Experimental Results

To verify the effectiveness of the proposed converter, the parameters listed in Table 1 are used to obtain the theoretical and experimental results of the proposed converter.

Table 1: Paramaters used for experiment.

Name of parameter	Symbol	Value
Output power	P_O	21 [W]
Input voltage	V_S	20 [V]
Output voltage	V_O	130 [V]
Load resistance	R_L	800 [Ω]
Frequency	F_S	100 [kHz]
Filter inductor/phase	L	200 [μH]
Intermediate capacitor	C_{in}	1 [μF]
Output smoothing capacitor	C	1 [μF]

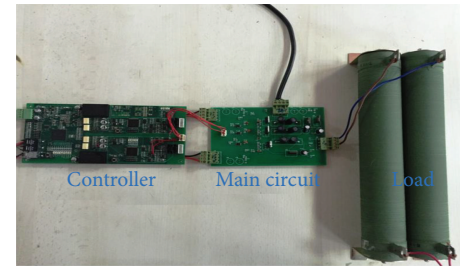

Figure 5: Photograph of prototype of the proposed converter.

Using (3), (6), (8), and (11) and using the parameters of Table 1, the following results are obtained:

$$\begin{aligned} D &= 0.6, \\ V_{C_{in}} &= 50\ \text{V}, \\ V_{C_1} &= 100\ \text{V}, \\ V_{C_2} &= 50\ \text{V}. \end{aligned} \tag{19}$$

Similarly using the parameters of Table 1 in (12), (13), and (14) gives the voltage stress of semiconductor devices:

$$\begin{aligned} V_{S_1} &= 50\ \text{V}, \\ V_{S_2} &= 50\ \text{V}, \\ V_{S_3} &= 50\ \text{V}, \\ V_{D_1} &= -100\ \text{V}, \\ V_{D_2} &= -50\ \text{V}, \\ V_{D_3} &= -50\ \text{V}. \end{aligned} \tag{20}$$

To verify the results and performance of the proposed converter an experiment has been carried out in the laboratory on a 21-watt prototype of the proposed converter using the parameters listed in Table 1. A photograph of the hardware of proposed converter is shown in Figure 5.

Figure 6 shows the experimental waveforms of the proposed converter for a duty cycle of 60%. The gate signals V_{G_1} and V_{G_2} are shown in Figure 6(a). It can be seen that these two signals are at 180-degree phase shift with each other both have 60% duty cycle. Figure 6(b) shows the waveforms of input

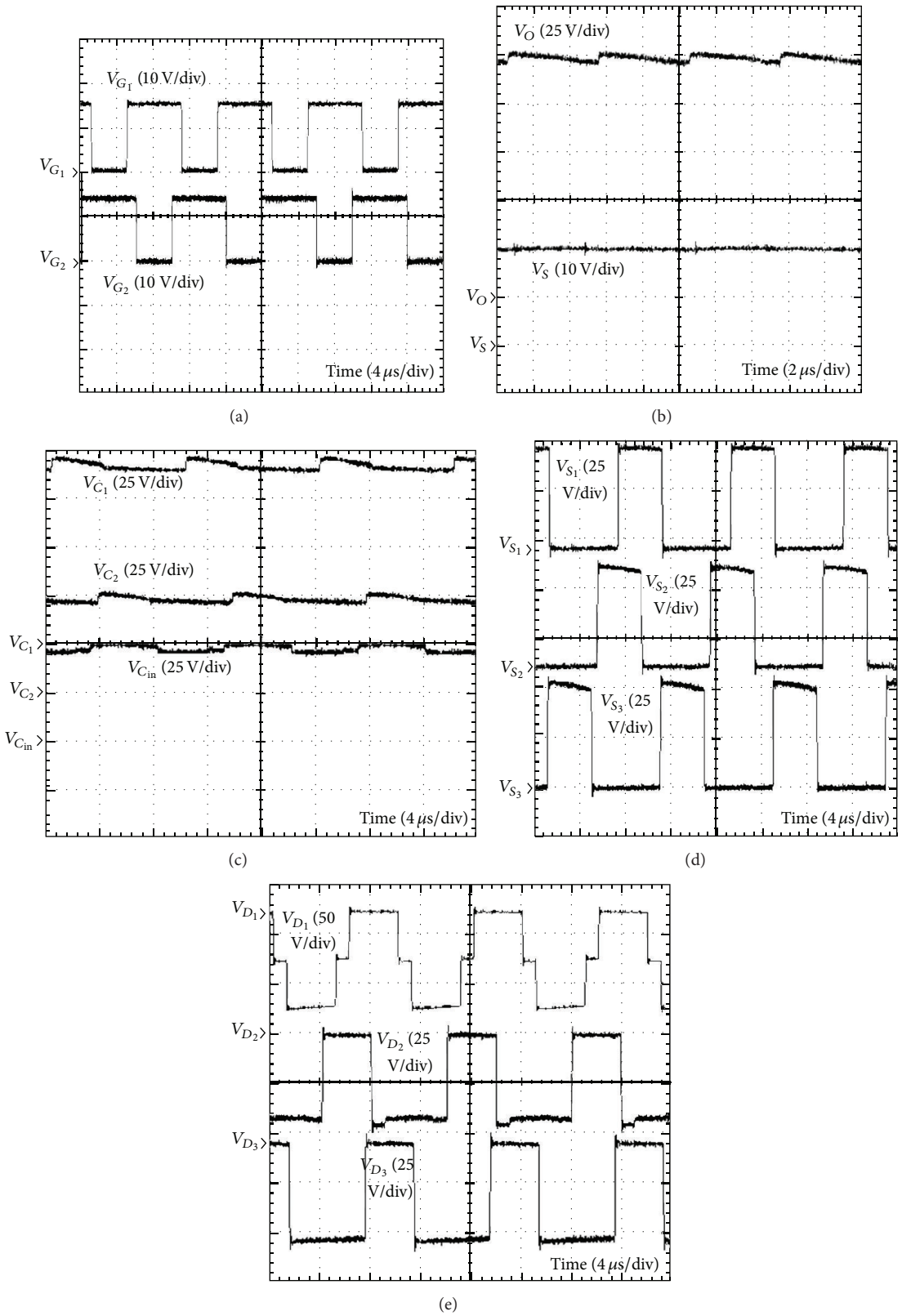

FIGURE 6: Experimental waveforms of the proposed converter. (a) Waveforms of PWM signals V_{G_1} and V_{G_2} with 60% duty cycle. (b) Waveforms of supply voltage V_S and output voltage V_O. (c) Waveforms of voltages V_{C_1}, V_{C_2}, and $V_{C_{in}}$ across capacitors C_1, C_2 &C_{in}. (d) Waveforms of voltage stresses V_{S_1}, V_{S_2} and V_{S_3} of MOSFETs S_1, S_2, and S_3. (e) Waveforms of voltage stresses V_{D_1}, V_{D_2}, and V_{D_3} of diodes D_1, D_2, and D_3.

and output voltages of the proposed converter. As clear from Figure 6(b) the supply voltage V_S to the proposed converter is 20 volts and the output voltage V_O is 121.5 volts which is close to the ideal value of 130 volts. Thus the proposed converter is able to produce 130 volts output from 20 volts input at 60% duty cycle and easily achieves a step-up voltage conversion ratio of 6.5. Figure 6(c) shows the waveforms of the voltages across the capacitors C_1, C_2, and C_{in}. The voltage V_{C_1} across capacitor C_1 is 93 volts and the voltage across each capacitor C_2 and C_{in} is 47 volts which are also close to ideal/theoretically calculated values. The waveforms of the voltage stresses V_{S_1}, V_{S_2}, and V_{S_3} across the MOSFETs S_1, S_2, and S_3 are shown in Figure 6(d). It can be seen that all the three voltages are equal to 50 volts. Thus the voltage stress across the MOSFETs is almost 2.6 times lower than the output voltage. Figure 6(e) shows the waveforms of the voltage stress across the diodes D_1, D_2, and D_3. As clear from Figure 6(e), the voltage stress V_{D_1} across diode D_1 is −98 volts, the voltage stress V_{D_2} across diode D_2 is −46 volts, and the voltage stress V_{D_3} across diode D_3 is −48 volts. Thus the voltage stress across the diodes is also reduced considerably.

Traditional interleaved boost converters whether of two phases or three phases have step-up voltage conversion ratio of $1/(1 - D)$ and the voltage stress across their switches (transistors and diodes) is equal to the output voltage [18, 19]. Thus, for producing an output voltage of 130 volts from an input voltage of 20 volts, the traditional interleaved boost converter must operate at a duty cycle of 84.6% which is very high as compared to the proposed interleaved boost converter. Also for 130-volt output voltage, the voltage stress across the transistors and diodes of traditional interleaved boost converter will be 130 volts which is also very high as compared to the switch stresses of the proposed converter.

From experimental results, it is clear that the proposed converter has very good performance as compared to the traditional interleaved boost converter. It nearly produces 130-volt output voltage from an input voltage of 16 volts with a duty cycle of 60% whereas the conventional interleaved boost converter will produce the same output at a duty cycle of 84.6% which is very high and can result in severe reverse recovery problems. Thus the proposed converter has considerably higher step-up voltage conversion ratio as compared to traditional interleaved boost converter and it easily overcomes the extreme high duty cycle operation and reverse recovery problem of the output diodes which appear in traditional interleaved boost converter. The voltage stress on the semiconductor devices of the proposed converter is also reduced considerably. Except the voltage stress of diode D_1 which is 100 volts, the voltage stress of all other switches in the proposed converter is 50 volts; thus low rating devices can be used which results in reducing the overall cost and size of the converter whereas the voltage stress of the switches of traditional interleaved boost converter is equal to the output voltage, that is, 130 volts. Thus the voltage stress across the switches of the proposed converter is 2.6 times lower than that across the switches of traditional interleaved boost converter.

Figure 7 shows a plot of experimentally measured efficiency of the proposed converter against the load. The load resistor is varied to change the power and efficiency is measured at different loads. An efficiency of 91.3% is achieved at the rated power of 21 watts and a maximum efficiency of 92.5% is achieved at 16-watt output power. At 38-watt output power, the efficiency is lowered to 87.7% due to increased conduction losses.

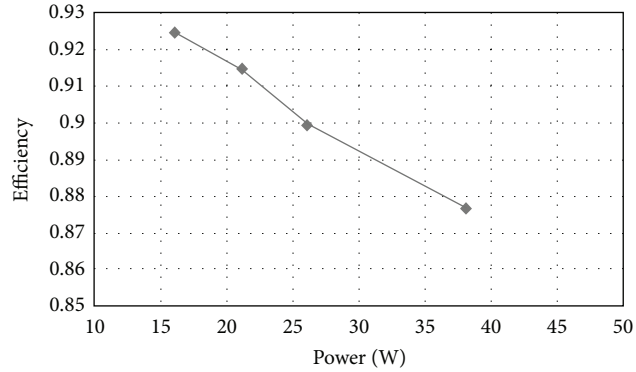

Figure 7: Experimentally measured efficiency of the proposed converter.

5. Conclusion

A new topology of interleaved boost converter is presented in this study. Besides the well-known feature of ripple reduction/cancellation of the interleaved converters, the proposed topology has several additional advantages over the traditional interleaved boost converter. The analysis shows that traditional interleaved boost converter will undergo high duty cycle operation and reverse recovery problem, whereas the proposed converter can achieve the same voltage gain at appropriate duty cycle. The voltage stress on switches of the proposed converter is 260% less than that of traditional interleaved boost converter. An efficiency of above 90% is achieved which is considered good. These features make the proposed converter a more suitable candidate for renewable energy generating system where high step-up dc-dc voltage conversion is required.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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