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Research Article

Analysis of CNT Bundle and Its Comparison with Copper Interconnect for CMOS and CNFET Drivers

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In nanoscale regime as the CMOS process technology continues to scale, the standard copper (Cu) interconnect will become a major hurdle for onchip communication due to high resistivity and electromigration. This paper presents the comprehensive evaluation of mixed CNT bundle interconnects and investigates their prospects as a low power high-speed interconnect for future nanoscale-integrated circuits. The performance of mixed CNT bundle interconnect is examined with carbon nanotube field effect transistor (CNFET) as a driver and compared with the traditional interconnect, that is, CMOS driver on Cu interconnect. All HSPICE simulations are carried out at operating frequency of 1 GHz and it is found that mixed CNT bundle interconnects with CNFET as the driver can potentially provide a substantial delay reduction over traditional interconnects implemented at 32 nm process technology. Similarly, the CNFET driver with mixed CNT bundle as interconnect is more energy efficient than the traditional interconnect at all supply voltages (VDD) from 0.9 V to 0.3 V.

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1. Introduction

As the process technology scales into the nanoscale regime, the impact of onchip communication on performance and reliability continues to increase. Each new technology node brings smaller transistors and wires. Although this makes transistors faster (more leakage), wires get slower [1]. Further, the traditional copper interconnects will suffer from significant increase in resistivity due to surface roughness, grain boundary scattering and from electromigration problems due to lower current densities supported by the copper conductor [2, 3]. As the interconnect performance depends on both wire and driver transistor characteristics, alternative interconnect and device technologies must be simultaneously investigated for onchip communication in future nanoscale integrated circuits.

Carbon nanotubes (CNTs) have been proposed as possible replacements for copper interconnect due to their large conductivity and current carrying capabilities [4–7]. CNTs can be thought of being made by rolling up a single atomic layer of graphite to form a seamless cylinder. The resulting structure is called single-walled carbon nanotube (SWCNT) [8] as shown in Figure 1(a). If several SWCNTs with varying diameter are nested concentrically inside one another, then the resulting structure is called as multiwalled carbon nanotube (MWCNT) [9], as shown in Figure 1(b). The SWCNT consists of one grapheme shell, whereas the MWCNT has multishells [10]. However, the individual SWCNTs suffer from a high ballistic resistance of 6.5 kΩ. To reduce the impact of individual tube, bundles of SWCNTs in parallel are required to provide high conductance. Almost all experimental results have demonstrated that a realistic nanotube bundle contains a mixed bundle of SWCNTs and MWCNTs. Depending on the process controls and conditions during CNT synthesis, the diameters of the CNTs inside a bundle follow normal distributions [11–13].

This paper analyses the various design aspects of mixed CNT bundle and investigates the prospects of mixed bundle of CNTs on carbon nanotube field effect transistor technology (CNFET_CNT) as a low power high-speed interconnects for future nanoscale integrated circuits. To the best of our knowledge, this is the first effort to analyze the detail performance of CNFET_CNT and its comparison with traditional interconnects. All simulations are carried out at

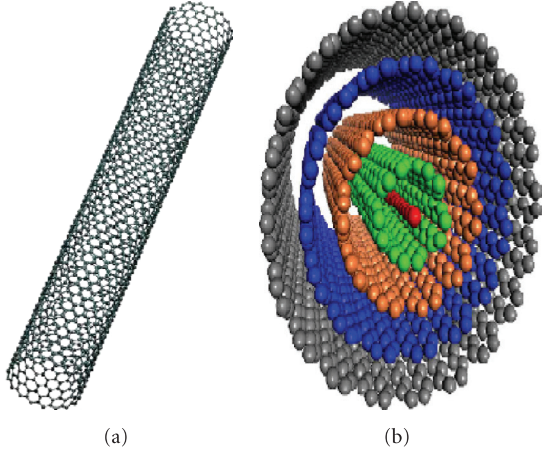

Figure 1: (a) Single-walled CNT. (b) Multi-walled CNT.

32 nm technology node at operating frequency of 1 GHz. The paper is organized as follows. Section 2 describes the conductance of CNT bundle. Section 3 describes the inductance and capacitance of CNT bundle. Section 4 compares the conductance of CNT and Cu interconnects. Section 5 explains the basic structure of CNFET. Section 6 compares the performance of CNFET driver with CNT interconnects and traditional (CMOS driver with Cu interconnects) and Section 7 concludes this paper.

2. Conductance of CNT Bundle

The conduction of an SWCNT or MWCNT is determined by two parameters: the conducting channel per shell and the number of shells. An SWCNT has one shell, whereas the number of shells (N_{sh}) in MWCNT depends on diameter [10]:

$$N_{sh} = 1 + \frac{(D_{out} - D_{in})}{2\delta}, \quad (1)$$

where D_{out} and D_{in} are the maximum and minimum shell diameter and δ is the van der Waals distance between graphene layers in graphite (which is 0.34 nm). Figure 2 shows the simulation results of different process parameters such as tube density (D), the ratio D_{in}/D_{out} (R), and probability of metallic CNTs (r) in a bundle. For the same aspect ratio of a CNT bundle if the D varies from $1E + 12$ to $5E + 12$ tubes/cm^2 the numbers of tubes in the bundle increases from 21 to 90. Similarly the variation of r from 1/3 to 2/3 increases the number of conduction channels from 256 to 312. The variation of R ratio impacts the number of the shells of MWCNTs. A smaller R ratio leads to more shells and a higher conductance. Simulation results show that compared to $D = 1E + 12$, $r = 0.33$, and $R = 0.5$ the process parameters ($D = 5E + 12$, $r = 0.667$, and $R = 0.3$) improve the bundle conductance by 10X. Hence the proper selection of above parameters decides the improvement in bundle conduction.

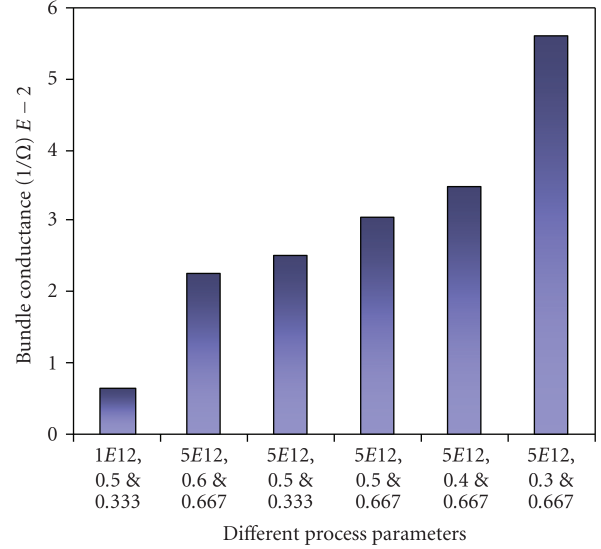

Figure 2: Bundle conductance versus process parameters (D, R, and r).

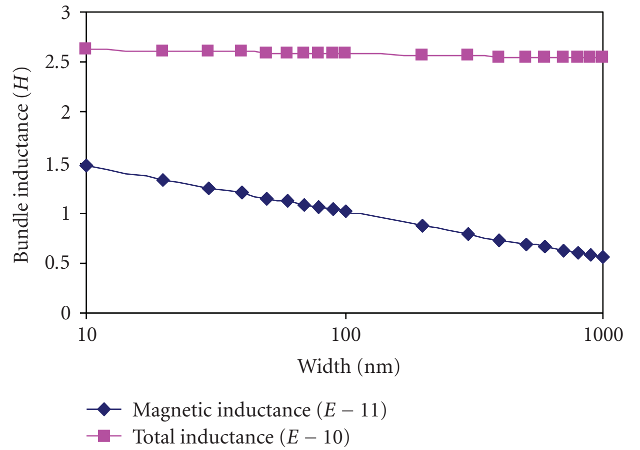

Figure 3: Inductance versus bundle width (W).

3. Inductance and Capacitance of CNT Bundle

3.1. Inductance. The CNT has two types of inductances, magnetic inductance and kinetic inductance. The magnetic inductance depends on the magnetic field inside and between the tubes. Whereas kinetic inductance is the kinetic energy of electrons, which is per unit length for each conduction channel in a CNT shell.

To analyze the contribution of both inductance types a simulation has carried out for a bundle geometry of [width (W) = height (H) for interconnect length (L) = 10 um) with other process parameter constant, it is found that as W increases the magnetic inductance starts to fall, whereas due to constant number of conduction channel (as R fixed) the kinetic inductance remains constant. Hence the total inductance (kinetic + magnetic) falls gradually with W as shown in Figure 3. Hence for a significant reduction into

total inductance, it's required to see the reduced contribution of magnetic inductance also.

The kinetic inductance (LK) per conduction channel is given by [14]

$$LK = \frac{hL}{4e^2 vfNc}, \quad (2)$$

where h is planks constant, e is the charge of single electron, vf is the Fermi velocity in graphite, Nc is the number of conduction channels, and L is the length of CNTs. This shows that the kinetic inductance of a bundle is inversely proportional to number of conduction channels. As per discussion in Section 1 by lowering the R, we can create more conduction channels, and hence can lower the kinetic inductance. Simulation results of Figure 4 for bundle geometry ($W = H = 50$ nm and $L = 10$ um) shows that compared to $D = 5E + 12$, $r = 0.33$, and $R = 0.6$ the process parameters ($D = 5E + 12$, $r = 0.667$, and $R = 0.3$) reduces the kinetic inductance by 67%.

Similarly Figure 5 shows the simulation results of the above geometry bundle with respective to average diameter of tubes. As the average diameter increases from 2.5 to 4 nm the bundle has around 120 tubes and the number of conduction channels (Nc) increases from 271 to 421. This decreases the kinetic inductance from $2.96E - 10$ to $1.91E - 10$ Henry (which 35% less), respectively. Now as the average diameter reaches to 4.5 nm, the numbers of tubes accompanied by the said bundle reduces from 120 to 105, therefore, Nc falls from 421 to 312. This results in the increase of kinetic inductance from $1.91E - 10$ to $2.57E - 10$ Henry. Beyond the average diameter of 4.5 nm the density of tubes cross the limit of $5E + 12$ tubes/cm^2 therefore the simulations are restricted up to an average diameter of 4.5 nm only. Hence it is important to choose the average diameter carefully so as to reduce the kinetic inductance of a given mixed CNT bundle for the selected tube density.

3.2. Capacitance. The capacitance of a CNT arises from two sources. The electrostatic capacitance (Ce) is calculated by treating the CNT a thin wire, with diameter "d" which is placed a distance "y" away from the ground plane and given by

$$Ce = \frac{2\prod \varepsilon}{\ln(y/d)}, \quad (3)$$

whereas the quantum capacitance (Cq) arises from the quantum electrostatic energy stored in the nanotube, when it carries the current. The Cq of each shell is given by [14]

$$Cq = \frac{4e^2 NcL}{hvf}. \quad (4)$$

This shows that Cq is directly proportional to Nc subjected to L constant. When CNT carries the current, then these two capacitance appears in series. Figure 6 shows the simulation results of ($W = H = 50$ nm and $L = 10$ um) bundle geometry, as the average diameter increases from 2.5 to 4 nm. The number of the tubes remains 120

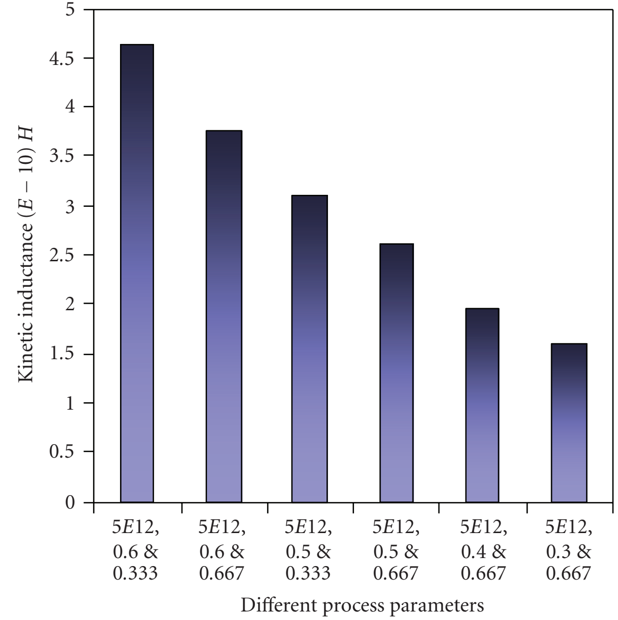

Figure 4: Kinetic inductance versus process parameters (D, R, and r).

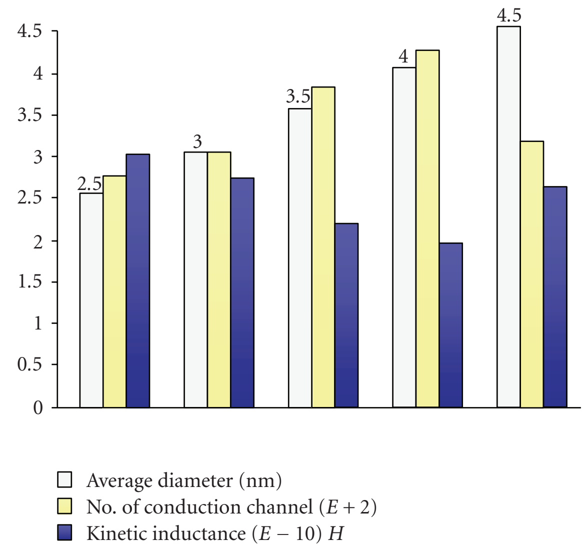

Figure 5: Kinetic inductance versus Average diameters.

and due to increasing number of subbands, Nc increases from 236 to 372, therefore, Cq increases by 37%. As the average diameter approaches to 4.5 nm, then the said bundle geometry accommodate only 105 tubes and Nc reduces to 256 from 372 which decreases the Cq by 31%. Hence the proper selection of average diameter is important because it decides the magnitude of Cq.

4. Conductance of CNT and Copper Interconnect

As the process technology scales down in order to provide sufficient current and to minimize the electromigration,

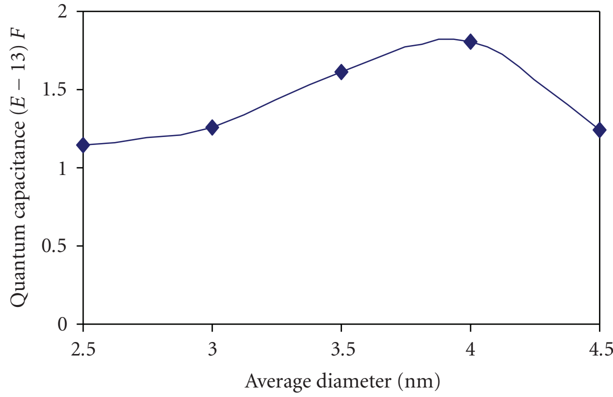

Figure 6: Quantum capacitance (Cq) of bundle.

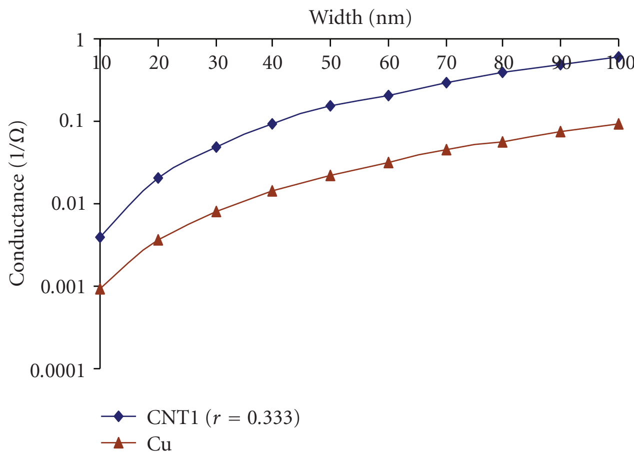

Figure 7: Conductance comparison of CNT bundle versus Cu.

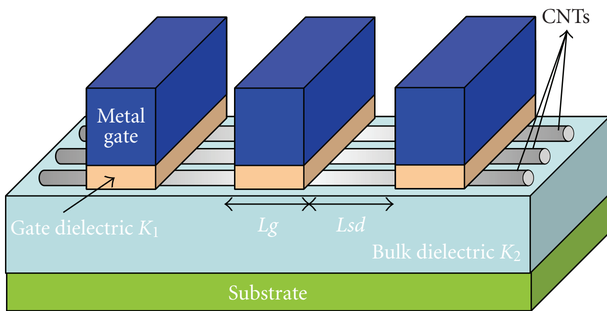

Figure 8: 3D CNFET structure.

the conductor height-to-width aspect ratio of traditional copper interconnect continues to increase [15]. Since the CNTs can reliably handle three orders of magnitude larger current densities than copper conductor [16], CNTs-based interconnects potentially provide larger benefits in area. A mixed bundle of CNTs and Cu interconnects are modeled as equivalent transmission line and the equivalent circuit parameters (R, L, C) were extracted, using the Carbon Nanotubes Interconnect Analyzer (CNIA) [17] and BPTM

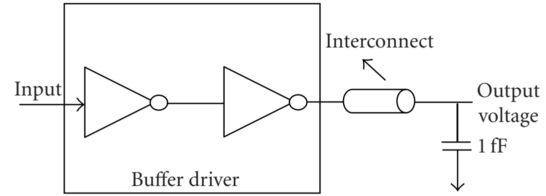

Figure 9: Test setup for simulation.

tools [18], with the interconnects geometry suggested in [19, 20]. Figure 7 shows the comparison of conductance between the mixed CNT bundle and Cu for the same geometry. At lower bundle width (<20 nm) the number of tubes accompanied by the bundle are less and hence the conductance dropped, but still it is 5.7X the conductance of Cu.

5. Basic Structure of CNFET

As shown in Figure 8, the CNTs are placed on the bulk substrate (k_2), a high (k_1) dielectric separates the CNTs from metal gate electrode by an insulator thickness "Tox," with dielectric constant of 16. Depending on the direction in which the CNTs are rolled up (Chirality), they demonstrate either metallic or semiconducting properties. The chiral vector of value (n, m) decides the diameter "d" of CNT which is given as

$$d = a\sqrt{\frac{(n^2 + m^2 + nm)}{\pi}}. \quad (5)$$

Substituting $n = 26$ and $m = 0$ in (5) results in "d" = 2 nm. Using lattice constant "a" = 2.49 e^{-10}m, Width of the CNFET transistor is define as $W = N * S$ [21], where "N" is the number of tubes and "S" is the pitch. In this paper we have used MOSFET like CNFET model from [22] with following specification: $d = 2$ nm, $S = 2d = 2 * 2$ nm = 4 nm, Tox = 2 nm, Channel length $Lg = 32$ nm, and Source/Drain under-lapped LSS = LSD = 32 nm.

6. Compaison of CNFET and CMOS Driver with CNT and Copper Interconnect

Figure 9 shows HSPICE test setup used for performance evaluation of CNFET and CMOS driver with mixed CNT bundle and Cu as interconnect, respectively. The length of the interconnect considered for simulation is 100 um. The measured ratio between parallel nanotubes in a CNFET-based inverter is 3 : 2 (i.e., parallel 3 and 2 CNTs each for N and P type CNFET, resp.) to effectively balance the on-current of inverter. Whereas for CMOS inverter it is 1 : 2 (i.e., W/L of PMOS is 2X of W/L of NMOS). For performance comparison with CNFET, a high performance (HP) predictive model of MOSFET [23] is used.

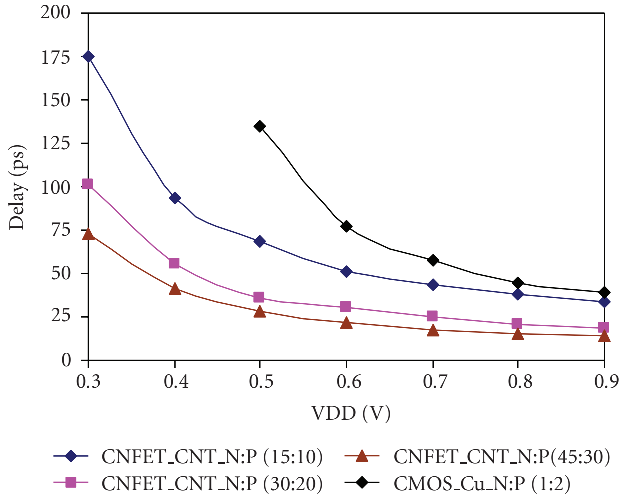

Figure 10: Delay of driver-interconnect system.

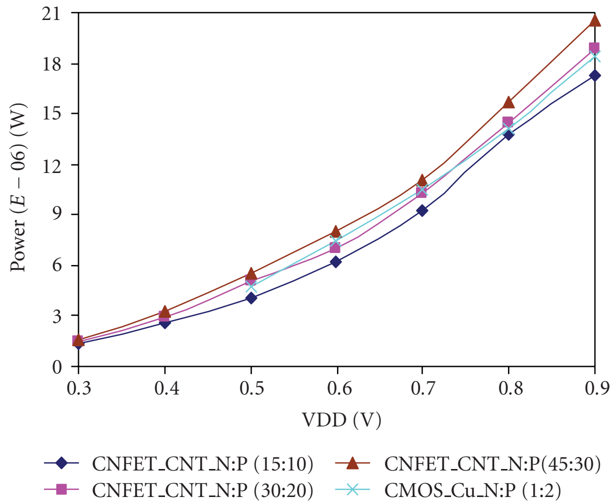

Figure 11: Power of driver-interconnect system.

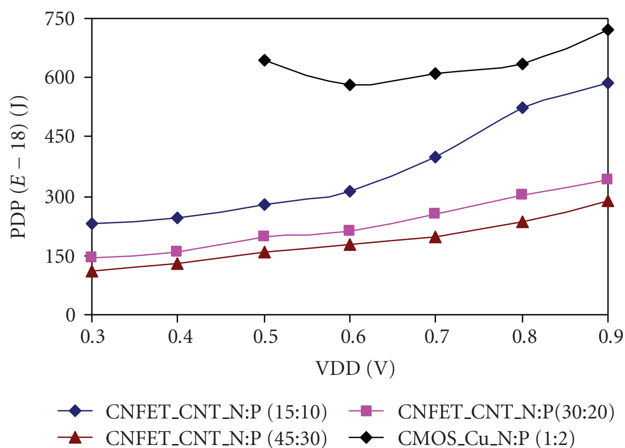

Figure 12: Power delay product of driver-interconnect system.

To observe the effect of numbers of CNTs used in a CNFET three drivers of different CNT ratio such as (15 : 10), (30 : 20), and (45 : 30) are used and it is found that as the number of CNTs in a buffer increases they are able to more effectively drive the load capacitance, which results in shorter delay. As shown in Figure 10 and as discussed in Section 4, the delay of CMOS driver with copper, that is, (traditional interconnect) is 2.8X and 4.78X more than that of the CNFET (45 : 30) driver with CNT interconnect at supply voltage (VDD) of 0.9 V and 0.5 V, respectively, Whereas for CMOS buffer the delay increases as VDD is decreased since the operating voltage approaches the threshold voltage of MOSFETs. Further, as the channel length of CNT used in the CNFET buffer is less than the mean free path of acoustic phonon, the CNFETs buffer operates in the ballistic mode and, therefore, provides higher on-current at relatively lowers bias voltages [24–26]. As the number of CNTs in a CNFET driver increases the gate parasitic capacitance increases but it is comparable to traditional interconnect as shown in Figure 11. Therefore, for performance evaluation here, we have considered the power delay product (PDP). Because of ballistic conduction of CNFETs and due to higher conductance of CNT interconnects the resultant delay of CNFET driver with CNT interconnect is very small, therefore, the said combination of (45 : 30) is 60% and 76% more energy efficient than the traditional interconnect at VDD of 0.9 V and 0.5 V, respectively, as shown in Figure 12.

7. Conclusions

This paper presents an analysis of mixed CNT bundle interconnects and compares it with Copper interconnects. Our investigation of CNFET driver with CNT interconnects compared to traditional interconnects shows very good potential as low power high speed interconnects. All simulations are carried out at 32 nm technology node at operating frequency of 1 GHz. The supply voltage used for 32 nm technology node is 0.9 V. The power dissipation analysis of the CNT interconnects on CNFET technology have been performed and compared with traditional interconnect for the first time and it is observed that for interconnect length of 100 um, the CNTs with CNFET consume comparable power as that of Cu with CMOS counterpart. Similarly the CNT interconnect has very low resistance and due to ballistic mode of operation and high mobility of CNFET, the said driver provides higher on-current at relatively lower bias voltages. Therefore, the CNFET driver with CNT interconnects are more energy efficient than the traditional interconnect.

Our analysis results also point out that the tube density, tube distribution, metallic tube ratio, the ratio of D_{in}/D_{out} and bundle dimension are crucial factors in determining the inductance capacitance and conductance performance of the mixed CNT bundle. The discussion on the selection of these CNT parameters can provide an important guideline for the design of mixed CNT bundles for future VLSI interconnects.

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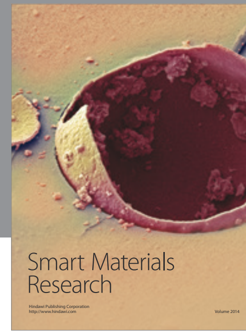
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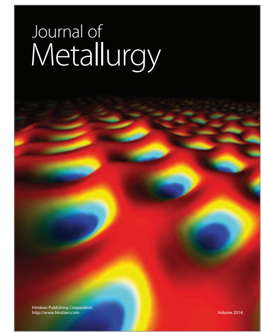
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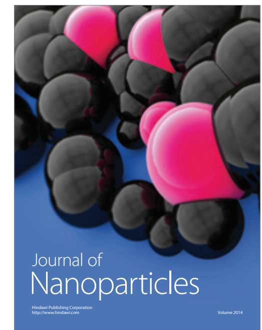
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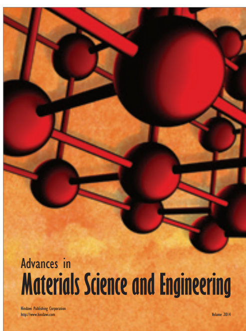
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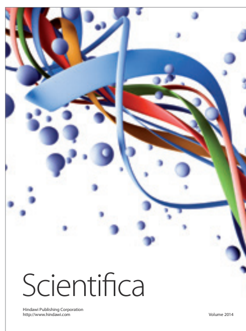
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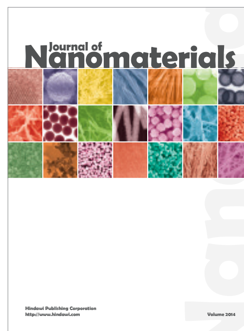
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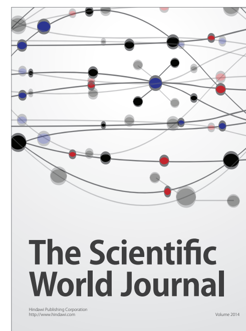
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