Hindawi Publishing Corporation
International Journal of Photoenergy
Volume 2016, Article ID 4063167, 8 pages
http://dx.doi.org/10.1155/2016/4063167

Hindawi

Research Article

Modeling and Analysis of New Multilevel Inverter for Solar Photovoltaic Power Plant

Xiaoqiang Guo,[1] Ran He,[1] and Mehdi Narimani[2]

[1]*Department of Electrical Engineering, Yanshan University, Qinhuangdao, China*
[2]*Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada*

Correspondence should be addressed to Xiaoqiang Guo; yeduming@163.com

Received 22 June 2016; Revised 18 August 2016; Accepted 28 August 2016

Academic Editor: Md. Rabiul Islam

Solar photovoltaic (PV) power plant is an effective way to utilize the renewable energy sources. EMI is one of the major concerns in PV power plant. Typically, the multilevel inverters are used in high voltage PV power plant. However, the conventional multilevel inverters require more semiconductors, which complicate the circuit structure and control algorithm. In this paper, a novel five-level inverter is introduced for the high voltage PV power plant applications. The model of the inverter is analyzed. With the redundant switching states, a new modulation strategy is proposed to reduce the common-mode voltage and EMI. The proposed approach is able to eliminate the common-mode voltage; meanwhile it has the capability of balancing the capacitor voltages. The cosimulation tests with the Matlab/Simulink and S-function are carried out. The results verify the effectiveness of the proposed method.

1. Introduction

The solar photovoltaic power plant is recently attracting much attention throughout the world. Typically, the multilevel inverters are applied in high voltage PV power plant [1–4], mainly due to the high voltage capability, low switching frequency, and low power losses [5, 6]. The classic multilevel topologies include the diode clamped, flying capacitor, and cascaded H-bridge converters [7–12]. However, these kinds of converters give rise to common-mode voltage (CMV), which could induce the ground leakage currents, as well as electromagnetic interference (EMI). And the EMI is one of the major concerns in PV power plant applications [13–16]. To reduce the EMI, many interesting methods have been reported in literature. For example, the CMV reduction for cascaded converters has been discussed in [17–19]. The CMV reduction strategies for neutral point clamped topologies have been reported in [20–22]. As for other types of multilevel converters, the space vector modulation (SVM) for CMV reduction of a four-level inverter is presented in [23] and for a five-level inverter is presented in [24]. Unfortunately, the balance of the capacitor voltage is not considered in the abovementioned modulation strategies. Actually, the balance of the capacitor voltage is one of the key issues in multilevel converters [7, 25]. Therefore, the modulation strategy which is able to eliminate the CMV and balance the capacitor voltage needs further investigation.

The objective of this paper is to present the modeling and analysis of a novel five-level inverter for PV power plant applications. The rest of the paper is organized as follows. Section 2 presents the analysis of the system operation principle. The proposed strategy is discussed in Section 3. The simulation interface and results are shown in Section 4. Finally, the conclusion is presented in Section 5.

2. Analysis of the New Five-Level Inverter

2.1. Operation of the Novel Five-Level Inverter. The novel five-level inverter, as shown in Figure 1, is a combination of a flying capacitor inverter and a neutral point clamped inverter presented in [26]. To ensure the equally spaced steps in the output voltages, the capacitors C_{x1} and C_{x2} $(x = a, b, c)$ are charged to $1/4V_{dc}$ and C_{x3} is charged to $3/4V_{dc}$. V_{dc} is the dc-link voltage. As shown in Table 1, the phase voltages are $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$, with respect to the midpoint n of the dc-link, corresponding to the phase switching states S_k $(k = a, b, c) = 2, 1, 0, -1, -2$.

Table 1: Switching states of the five-level inverter.

S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}	S_{7x}	S_{8x}	$V_{C_{x1}}$		$V_{C_{x2}}$		$V_{C_{x3}}$		V_{xn}	
								$i_x > 0$	$i_x < 0$	$i_x > 0$	$i_x < 0$	$i_x > 0$	$i_x < 0$		
1	1	1	1	0	0	0	0	—	—	—	—	—	—	$V_{dc}/2$	(*a*)
1	1	0	1	1	0	0	0	C	D	—	—	—	—		(*b*)
0	1	1	1	0	0	0	1	—	—	—	—	D	C	$V_{dc}/4$	(*c*)
1	0	1	1	0	0	1	0	D	C	D	C	C	D		(*d*)
1	1	0	0	1	1	0	0	C	D	C	D	—	—		(*e*)
1	0	0	1	1	0	1	0	—	—	D	C	C	D	0	(*f*)
0	1	0	1	1	0	0	1	C	D	—	—	D	C		(*g*)
0	0	1	1	0	0	1	1	D	C	D	C	—	—		(*h*)
0	0	0	1	1	0	1	1	—	—	D	C	—	—		(*i*)
1	0	0	0	1	1	1	0	—	—	—	—	C	D	$-V_{dc}/4$	(*j*)
0	1	0	0	1	1	0	1	C	D	C	D	D	C		(*k*)
0	0	0	0	1	1	1	1	—	—	—	—	—	—	$-V_{dc}/2$	(*l*)

C: charging; D: discharging.

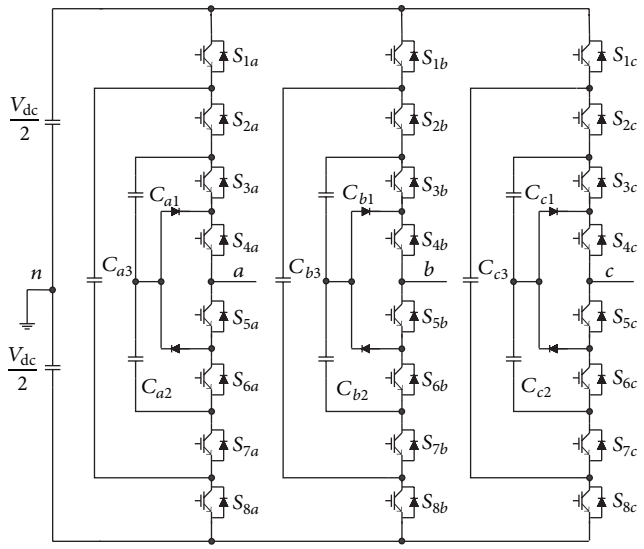


Figure 1: Schematic of the novel five-level inverter.

2.2. Common-Mode Voltage in the Novel Five-Level Inverter. The relationship between phase voltages and switching states can be expressed as follows:

$$V_{xn} = \begin{cases} \dfrac{V_{dc}}{2} & S_x = 2 \\ \dfrac{V_{dc}}{4} & S_x = 1 \\ 0 & S_x = 0 \\ -\dfrac{V_{dc}}{4} & S_x = -1 \\ -\dfrac{V_{dc}}{2} & S_x = -2 \end{cases} \quad x = a, b, c,$$

$$V_{an} = \frac{V_{dc}}{4} \times S_a,$$

$$V_{bn} = \frac{V_{dc}}{4} \times S_b,$$

$$V_{cn} = \frac{V_{dc}}{4} \times S_c. \tag{1}$$

The CMV is

$$V_{CM} = \frac{(V_{an} + V_{bn} + V_{cn})}{3}. \tag{2}$$

S_{sum} can be defined as

$$S_{sum} = S_a + S_b + S_c. \tag{3}$$

And the CMV generated by switching states can be expressed as

$$V_{CM}(S_{sum}) = \frac{V_{dc}}{12} \times S_{sum}. \tag{4}$$

According to (4), the CMV of all the switching states can be calculated. Table 2 demonstrates the number of switching states corresponding to each CMV; for instance, 19 switching states make CMV zero. The switching states that make zero CMV are shown in Table 3, where

$$S_a + S_b + S_c = 0. \tag{5}$$

Figure 2 shows the 19 switching states that generate zero CMV where the switching states are symmetric in the space vector diagram. The switching states in the different sectors can be transformed into region I. For example, switching states (01-1), (-110), (-101), (0-11), and (1-10) can be converted to (10-1) in region I using the corresponding angle. Therefore, without considering the voltage balancing of the capacitors, the inverter can properly operate by employing the switching states and selecting the appropriate switching sequence.

Table 2: CMV and switching states.

CMV	The number of switching states
$V_{dc}/2$	1
$5V_{dc}/12$	3
$V_{dc}/3$	6
$V_{dc}/4$	10
$V_{dc}/6$	15
$V_{dc}/12$	18
0	19
$-V_{dc}/12$	18
$-V_{dc}/6$	15
$-V_{dc}/4$	10
$-V_{dc}/3$	6
$-5V_{dc}/12$	3
$-V_{dc}/2$	1

Table 3: Switching states with zero CMV.

CMV	Switching states
0	2-1-1, 20-2, 10-1, 11-2, 02-2, 01-1, -12-1, -220, -110, -211, -202, -101, -1-12, 0-22, 0-11, 1-21, 2-20, 1-10, 000

3. Proposed Strategy

3.1. Modulation Strategy. The CMV can not be eliminated in the conventional carrier-based modulation presented in [6] and this is because the different switching states generate different CMVs. For example, when the given reference falls into the shaded triangle in Figure 2, only one of the three switching states, namely, (10-1), is with zero CMV; however with the conventional modulation the CMV cannot be kept zero.

Figure 3(a) shows the three-level space vector diagram and Figure 3(b) is the same as Figure 2 rotated by 30 degrees. There are 27 switching states and 7 redundant switching states in Figure 3(a) where the redundant switching states operate similar to synthesize reference vectors. Therefore, regardless of redundant switching states, the number of actually working switching states is 19, which is the same as five-level switching states with zero CMV. In other words, there is corresponding relationship between three-level switching states and five-level switching states with zero CMV as shown in Table 4. For example, switching state (20-2) in a five-level space vector diagram with zero CMV is corresponding to a (200) switching state in a three-level diagram, and similarly switching state (10-1) in a five-level diagram is corresponding to switching states (211) or (100) in a three-level diagram.

Table 4 shows the relationship between the three-level switching states and five-level switching states with zero CMV. This feature results in the three-level modulation strategy employing Table 4 being used for a five-level inverter while achieving zero CMV.

To achieve the three-level modulation strategy, there are space vector modulation and carrier-based modulation. Due to the complex calculation and implementation of space vector modulation, the carrier-based modulation is used in this paper.

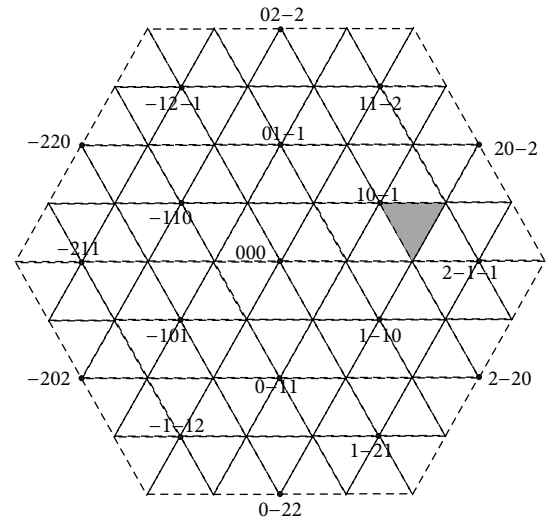


Figure 2: Space vector diagram in a five-level inverter.

Table 4: Relationship between three-level switching states and five-level switching states.

Three-level switching states	Five-level switching states
200	20-2
211, 100	10-1
210	11-2
211, 110	01-1
220	02-2
120	-12-1
020	-220
121, 010	-110
021	-211
022	-202
122, 011	-101
012	-1-12
112, 001	0-11
002	0-22
102	1-21
202	2-20
101, 212	1-10
201	2-1-1
222, 111, 000	000

It should be noted that the zero CMV is achieved where the capacitor voltages are balanced. The following section will present a strategy to balance the capacitor voltages in each phase.

3.2. Capacitor Voltage Balancing Strategy. The capacitor voltages $V_{C_{x1}}$ and $V_{C_{x2}}$ should be kept at 1/4 of the dc bus voltage ($V_{dc}/4$) and $V_{C_{x3}}$ should be maintained at 3/4 of the dc bus voltage ($3V_{dc}/4$) to ensure the proper operation of the five-level inverter. The voltage deviation of flying capacitor is

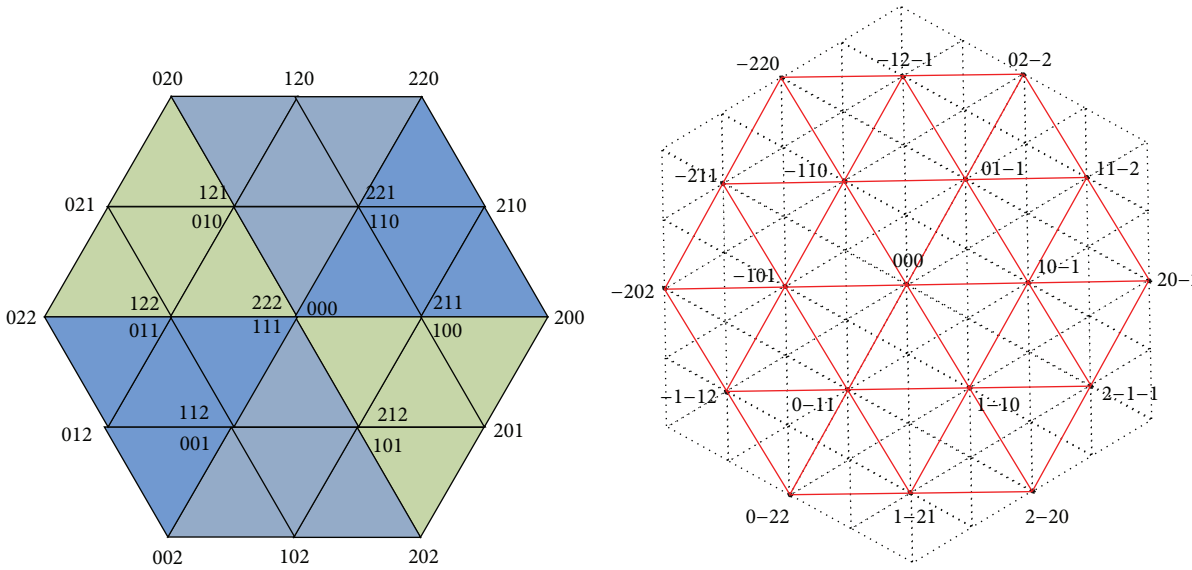


Figure 3: Space vector diagram: (a) three levels and (b) five levels (CMV = 0).

defined as the difference between flying capacitor voltage and the given value, which can be expressed as

$$\Delta V_{C_{x1}} = V_{C_{x1}} - \frac{V_{dc}}{4},$$
$$\Delta V_{C_{x2}} = V_{C_{x2}} - \frac{V_{dc}}{4}, \quad (6)$$
$$\Delta V_{C_{x3}} = V_{C_{x3}} - \frac{3V_{dc}}{4},$$

where $V_{C_{x1}}$, $V_{C_{x2}}$, and $V_{C_{x3}}$ are capacitor voltages and $\Delta V_{C_{x1}}$, $\Delta V_{C_{x2}}$, and $\Delta V_{C_{x3}}$ are the deviation of capacitor voltages. The capacitor voltage can be balanced by controlling the absolute value of the deviation voltages close to zero.

The switching states (a)~(k) can affect the current flowing into the flying capacitors and can change the capacitor voltages by either charging or discharging. Taking switching state (b) as an example, when $i_k > 0$, the capacitor C_{x1} is charged, and when $i_k < 0$, the capacitor C_{x1} is discharged.

The capacitor voltage balancing strategy can be defined as follows:

(i) Switching state $S_k = 1$ is employed to control capacitor voltages $V_{C_{x1}}$ and $V_{C_{x3}}$.

(ii) Switching state $S_k = -1$ is employed to control capacitor voltages $V_{C_{x2}}$ and $V_{C_{x3}}$.

(iii) Switching state $S_k = 0$ is employed to control capacitor voltages $V_{C_{x1}}$ and $V_{C_{x2}}$.

Details of the control method are shown in Tables 5, 6, and 7.

Table 5: Control table for capacitor voltage: $S_x = 1$.

Input conditions			Output results
S_x	ΔV_{C1}	ΔV_{C3}	The chosen switching states
1	>0	>0	(c)
	>0	<0	(d)
	<0	>0	(c)
	<0	<0	(b)

Table 6: Control table for capacitor voltage: $S_x = -1$.

Input conditions			Output results
S_x	ΔV_{C2}	ΔV_{C3}	The chosen switching states
−1	>0	>0	(j)
	>0	<0	(k)
	<0	>0	(j)
	<0	<0	(i)

Table 7: Control table for capacitor voltage: $S_x = 0$.

Input conditions				Output results
S_x	i_x	ΔV_{C1}	ΔV_{C2}	The chosen switching states
0	>0	>0	>0	(h)
		>0	<0	(e)
		<0	>0	(g)
		<0	<0	(e)
0	<0	>0	>0	(e)
		>0	<0	(f)
		<0	>0	(h)
		<0	<0	(h)

3.3. Integration Capacitor Voltage Balancing with PWM Schemes. The abovementioned capacitor voltage balancing method can be easily integrated with the proposed zero CMV modulation strategy. The schematic diagram of the

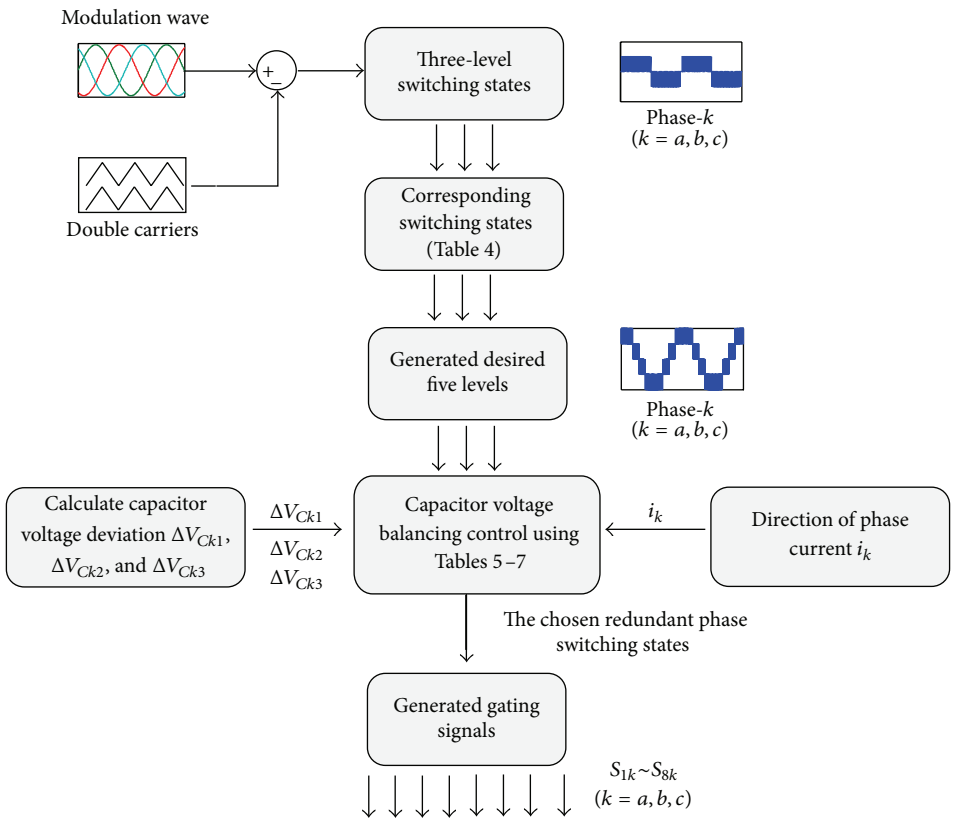


Figure 4: The control diagram of the novel five-level inverter.

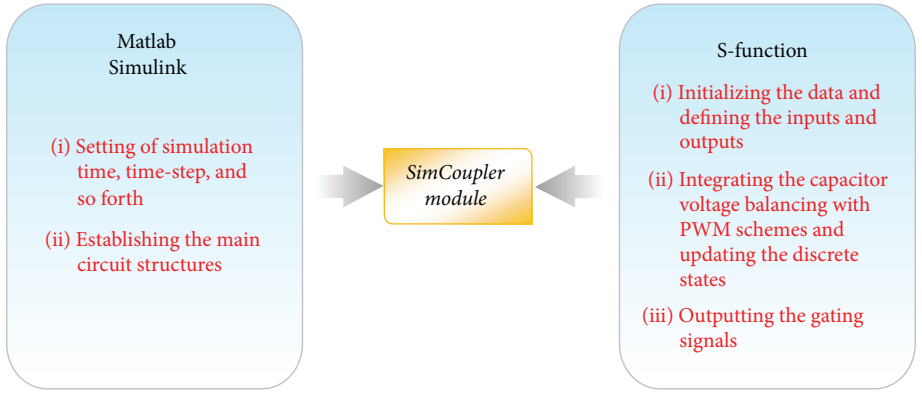


Figure 5: Matlab/Simulink and S-function cosimulation.

integration is shown in Figure 4. The procedure consists of the following steps:

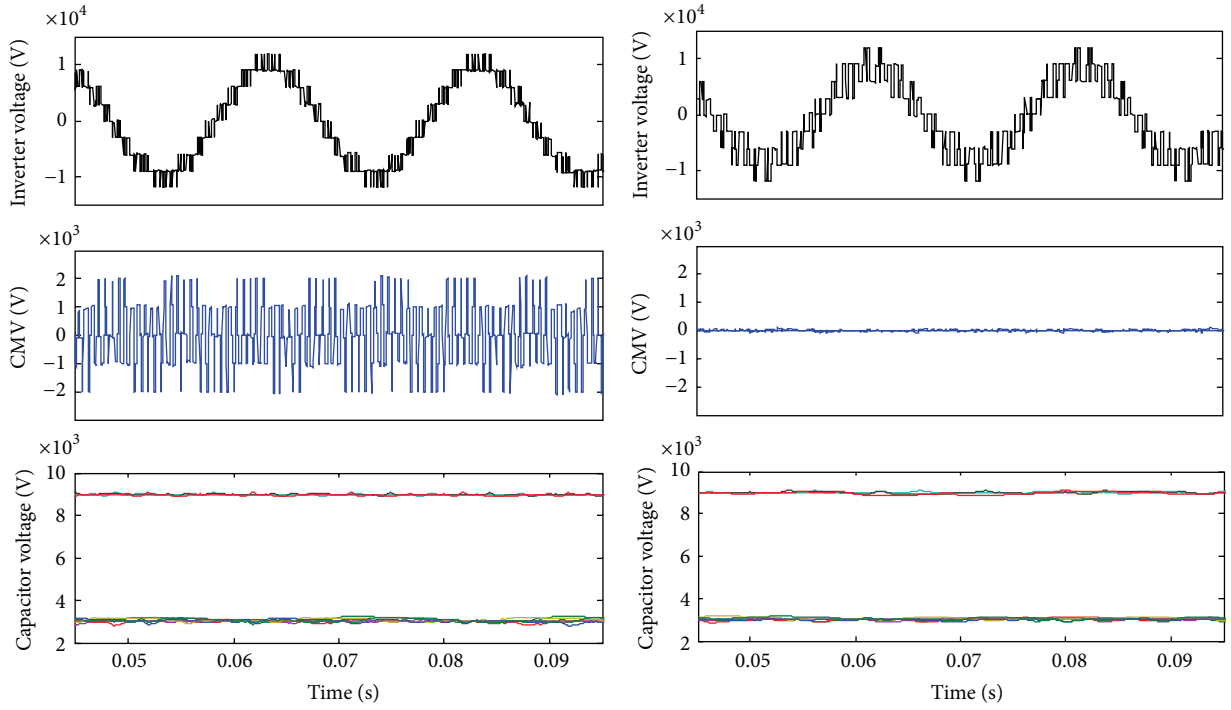
(1) First, the three-level switching states are generated by a dual-carrier-based PWM scheme.

(2) According to Table 4, the five-level switching states corresponding to three-level switching states can be determined to keep the novel five-level inverter with zero CMV.

(3) Finally, the capacitor voltage balancing can be achieved by using control tables of Table 5, 6, and 7 and considering the direction of phase current i_k.

4. Simulation Interface and Results

The cosimulation between Matlab/Simulink and S-function is realized to verify the effectiveness of the proposed method, as shown in Figure 5. The simulation parameters are listed in Table 8. In Simulink environment, the model of each system component is expressed by block diagram, and the lines among the block diagram indicate the direction of the signal flow. From the perspective of the whole system, *Simulink* is fast and convenient. However, for some complex and lengthy program code, it is not suitable with modularity. That is the reason why S-function is used for the simulation interface.



(a) Conventional modulation method

(b) Proposed modulation method

Figure 6: Simulation results of different modulations.

Table 8: Simulation parameters.

Inverter parameters	Values
Input dc voltage	12 kV
Capacitor	1000 μF
Inverter rating	3 MVA
Output frequency	50 Hz
Output inductance	5 mH
Power factor	0.9
Modulation index	0.95
Switching frequency	700 Hz

The cosimulation system is very useful to tackle the demand of the simulation and implementation of complex multilevel inverter systems.

Figure 6 shows the performance of the five-level inverter with conventional and proposed modulations. The total harmonic distortion of the line-line voltage with conventional modulation is 17.32% and the CMV cannot be eliminated, varying within the range of $V_{dc}/6$ and $-V_{dc}/6$. Whereas the total harmonic distortion of the line-line voltage with proposed modulation is 37.41%, however, the CMV can be effectively eliminated. It should be noted that, like other modulation strategy regarding the common-mode voltage reduction, the voltage THD will be higher. However, it mainly consists of high frequency components. So the THD can be reduced with the output filter, as shown in Figure 7.

To evaluate the dynamic performance of the proposed modulation, a step change from half load to full load has been studied at $t = 0.1$ s, as shown in Figure 7. The voltage of the flying capacitors can be maintained at the nominal values and the CMV can be kept constant at zero before and after the step change.

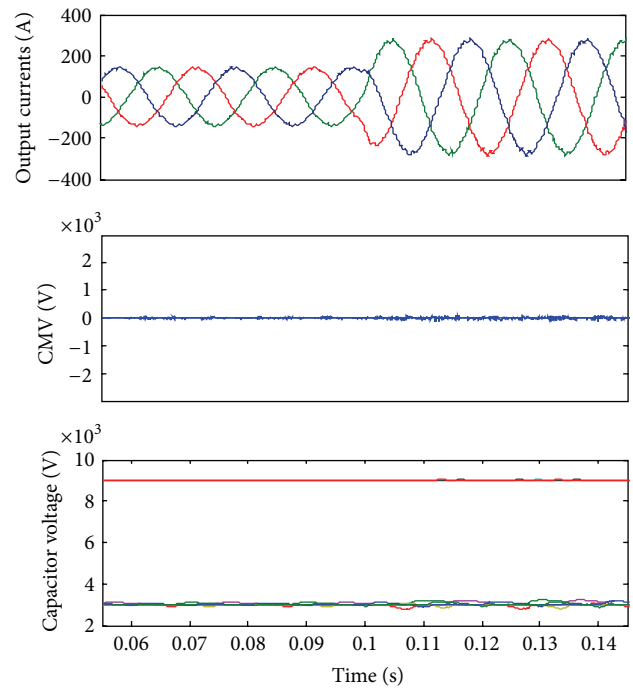


Figure 7: Simulation results from half to full loads.

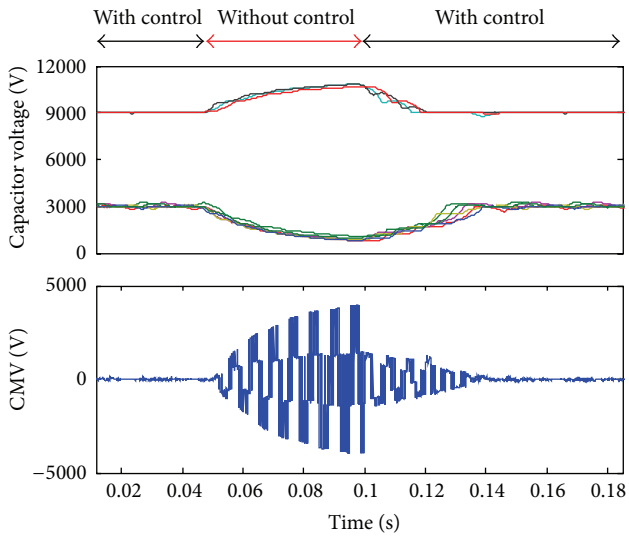


FIGURE 8: Simulation results with and without proposed controller.

In order to verify the performance of the proposed control strategy with and without the proposed control, the simulation test is carried out and shown in Figure 8. In this case, the proposed controller is enabled and, at $t = 0.05$ s, the controller is disabled; then the controller is reactivated at $t = 0.1$ s. As can be seen from Figure 8, when the controller is deactivated, the capacitor voltages diverge and the CMV gets bigger. However, when the controller is reactivated, the capacitor voltage starts converging and the CMV approaches zero rapidly, which verifies the effectiveness of the proposed control strategy.

5. Conclusion

The modeling and analysis of a novel five-level inverter for PV power plant applications has been presented in this paper. The common-mode voltage can be eliminated by selecting the specific switching states. Also, the balancing of flying capacitor voltages can be achieved with a simple control strategy. In contrast to the conventional solutions, our proposal reduces the number of calculations which simplifies the implementation, and thus it is very attractive for PV power plant applications, where the EMI is a major concern. It should be noted that this paper mainly focuses on the CMV and EMI reduction of the five-level inverter for PV power plant. The MPPT and other issues of PV power plant are the subject of the future research.

Competing Interests

The authors declare that there is no conflict of interests regarding publication of this paper.

Acknowledgments

This work was supported by Science Foundation for Distinguished Young Scholars of Hebei Province (E2016203133) and China Postdoctoral Science Foundation (2015T80230).

References

[1] H. Nademi, A. Das, R. Burgos, and L. E. Norum, "A new circuit performance of modular multilevel inverter suitable for photovoltaic conversion plants," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 393–404, 2016.

[2] S. Essakiappan, H. S. Krishnamoorthy, P. Enjeti, R. S. Balog, and S. Ahmed, "Multilevel medium-frequency link inverter for utility scale photovoltaic integration," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3674–3684, 2015.

[3] M. Hamzeh, A. Ghazanfari, H. Mokhtari, and H. Karimi, "Integrating hybrid power source into an Islanded MV microgrid using CHB multilevel inverter under unbalanced and nonlinear load conditions," *IEEE Transactions on Energy Conversion*, vol. 28, no. 3, pp. 643–651, 2013.

[4] L. Liu, H. Li, Y. Xue, and W. Liu, "Decoupled active and reactive power control for large-scale grid-connected photovoltaic systems using cascaded modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 176–187, 2015.

[5] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930–2945, 2007.

[6] S. Kouro, M. Malinowski, K. Gopakumar et al., "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010.

[7] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1907–1918, 2013.

[8] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalán, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 305–314, 2009.

[9] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 642–651, 2012.

[10] J. I. Leon, S. Kouro, S. Vazquez et al., "Multidimensional modulation technique for cascaded multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 412–420, 2011.

[11] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: high-power adjustable speed drive topologies," *IEEE Industry Applications Magazine*, vol. 18, no. 4, pp. 26–39, 2012.

[12] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2688–2701, 2016.

[13] R. Araneo, S. Lammens, M. Grossi, and S. Bertone, "EMC issues in high-power grid-connected photovoltaic plants," *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 3, pp. 639–648, 2009.

[14] Z. Wang, S. Fan, Y. Zheng, and M. Cheng, "Design and analysis of a CHB converter based PV-battery hybrid system

for better electromagnetic compatibility," *IEEE Transactions on Magnetics*, vol. 48, no. 11, pp. 4530–4533, 2012.

[15] W. Chen, Y. Duan, L. Guo, Y. Xuan, and X. Yang, "Modeling and prediction of radiated emission from solar cell in a photovoltaic generation system," *IEEE Journal of Photovoltaics*, vol. 6, no. 2, pp. 540–545, 2016.

[16] Y. Bae and R.-Y. Kim, "Suppression of common-mode voltage using a multicentral photovoltaic inverter topology with synchronized PWM," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4722–4733, 2014.

[17] P. C. Loh, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1386–1395, 2003.

[18] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1672–1681, 2007.

[19] J. Rodríguez, J. Pontt, P. Correa, P. Cortés, and C. Silva, "A new modulation method to reduce common-mode voltages in multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 4, pp. 834–839, 2004.

[20] H. Zhang, A. Von Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Transactions on Industry Applications*, vol. 36, no. 6, pp. 1645–1653, 2000.

[21] H.-J. Kim, H.-D. Lee, and S.-K. Sul, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed ac motor drives," *IEEE Transactions on Industry Applications*, vol. 37, no. 6, pp. 1840–1845, 2001.

[22] A. Von Jouanne, S. Dai, and H. Zhang, "A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common-mode voltage elimination," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 739–745, 2002.

[23] N. Rashidi-Rad, A. Rahmati, A. Abrishamifar et al., "Reduction of common-mode voltage in an even level inverter by a new SVM method," *International Journal of Advanced Computer Science*, vol. 2, no. 9, pp. 343–347, 2012.

[24] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1598–1607, 2008.

[25] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2262–2271, 2010.

[26] M. Narimani, B. Wu, G. Cheng, and N. Zargari, "Improved multilevel voltage source converters and systems," United States US Patent 20,140,376,287 A1.