NANO EXPRESS

Open Access

CrossMark

The Study of Electrical Properties for Multilayer La_2O_3/Al_2O_3 Dielectric Stacks and $LaAlO_3$ Dielectric Film Deposited by ALD

Xing-Yao Feng, Hong-Xia Liu[*], Xing Wang, Lu Zhao, Chen-Xi Fei and He-Lei Liu

Abstract

The capacitance and leakage current properties of multilayer La_2O_3/Al_2O_3 dielectric stacks and $LaAlO_3$ dielectric film are investigated in this paper. A clear promotion of capacitance properties is observed for multilayer La_2O_3/Al_2O_3 stacks after post-deposition annealing (PDA) at 800 °C compared with PDA at 600 °C, which indicated the recombination of defects and dangling bonds performs better at the high-*k*/Si substrate interface for a higher annealing temperature. For $LaAlO_3$ dielectric film, compared with multilayer La_2O_3/Al_2O_3 dielectric stacks, a clear promotion of trapped charges density (N_{ot}) and a degradation of interface trap density (D_{it}) can be obtained simultaneously. In addition, a significant improvement about leakage current property is observed for $LaAlO_3$ dielectric film compared with multilayer La_2O_3/Al_2O_3 stacks at the same annealing condition. We also noticed that a better breakdown behavior for multilayer La_2O_3/Al_2O_3 stack is achieved after annealing at a higher temperature for its less defects.

Background

With the continuous development of integrated circuit, high-*k* materials have been extensively studied to substitute traditional SiO_2 gate dielectrics in CMOS devices as a solution for the saturation of the leakage current and power consumption [1–3]. Lanthanum oxide (La_2O_3), aluminum oxide (Al_2O_3), yttrium oxide (Y_2O_3), hafnium oxide (HfO_2), and zirconium oxides (ZrO_2) have been tried to use as alternative gate dielectric materials [4–7]. Among them, La_2O_3 is regarded as a promising candidate due to the high dielectric constant ($k \sim 27$) and large band gap. Simultaneously, the accompanying problems also draw great attentions [8, 9].

The electrical properties of La_2O_3 and Al_2O_3 dielectric stacks have been studied by many researchers. Srikant Jayanti pointed out that significant improvement about charge trapping and leakage characteristics was obtained by using a La_2O_3 interface scavenging layer for Al_2O_3 interpoly dielectric [10]. Lee found that the hydration of La_2O_3 can be blocked by the Al_2O_3 in Al_2O_3/La_2O_3/Si (ALO structure) after the annealing treatment at 700 °C

[11]. Researchers also revealed that the ultra-thin 0.5-nm Al_2O_3 inserted layer under the 4 nm $LaAlO_3$ can reduce the EOT to 1.2 nm with optimized interface trap density. And compared with La_2O_3 and Al_2O_3 dielectric stacks (ALO or LAO structure), the lanthanum aluminate ($LaAlO_3$) meets the thermal processing requirement better, since the added Al_2O_3 greatly improves the chemical stability and crystallization temperature [12, 13]. However, the electrical property difference between the La_2O_3/Al_2O_3 dielectric stacks and $LaAlO_3$ have not been fully studied. In this paper, multilayer La_2O_3/Al_2O_3 stacks and $LaAlO_3$ dielectric film were prepared by ALD reactor, and then, post-deposition annealing (PDA) was carried out at different temperatures. After the deposition of metal gate, the interfacial issues and electrical properties of the fabricated MIS structures were studied.

Methods

P-type Si (100) wafers with resistivity of 3–8 Ω cm were dipped in deionized water and diluted HF for 3 min, respectively, to remove the native oxide before deposition. Then La_2O_3/Al_2O_3 high-*k* stacks were deposited on Si wafers by ALD reactor (Picosun R-150, Espoo, Finland) in 300 °C. La(i-PrCp)$_3$ and trinethyluminium

* Correspondence: hxliu@mail.xidian.edu.cn
Key Laboratory for Wide-Band Gap Semiconductor Materials and Devices of Education, School of Microelectronics, Xidian University, Xi'an 710071, China

Feng et al. Nanoscale Research Letters (2017) 12:230

Page 2 of 4

(TMA) were used as precursors of La and Al, and O_3 was used as oxidant. Besides, ultra-high purity nitrogen (N_2, 99.999%) was employed as purge gas and carrier. The rapid thermal annealing (RTA) process was carried out at 600 and 800 °C in N_2 ambient for 1 min after the deposition. A metal electrode with a diameter of 300 μm was fabricated by depositing 150 nm Al by the electron-beam evaporation through a shadow mask. In the end, the electrical properties including capacitance-voltage (C-V), conductance-voltage (G-V), and leakage current-voltage (I-V) characteristics were evaluated using an Agilent B1500A semiconductor parameter analyzer at the frequency of 100 kHz. X-ray photoelectron spectroscopy (XPS) was used to examine the bonding structures and chemical quantitative composition of the films. C1s peak from adventitious carbon at 284.6 eV [14] was used as an internal energy reference during the analysis.

Results and Discussion

The schematic structures and annealing temperatures are shown in Fig. 1 and Table 1. In Table 1, one-cycle La_2O_3 or Al_2O_3 came out from the reaction of a pulse of La or Al precursor and a pulse of oxidant O_3. The samples S1 and S2 are multilayer La_2O_3/Al_2O_3 stacks with the same film structure and with 600 and 800 °C annealing temperatures, respectively, while the sample S3 is the $LaAlO_3$ dielectric film annealed at 600 °C.

Figures 2 and 3 show the C-V and G-V curves of samples S1, S2, and S3. The capacitors were swept forward (bias from negative to positive) and backward (bias from positive to negative) to check the C-V hysteresis at the frequency of 100 kHz. G-V curves were obtained simultaneously with the C-V curves. The ΔV_{FB} is the flat band voltage difference of the C-V curve and its

hysteresis. A clear decreasing of ΔV_{FB} was observed with a higher annealing temperature with the same multilayer La_2O_3/Al_2O_3 stack structure. More apparently, sample S3 has a very small ΔV_{FB} compared with S1 and S2.

As we know, the trapped charges are responsible for the ΔV_{FB} (hysteresis width) [15], and we assume that the two-dimensional distribution of traps near the interface contributes to the film capacitance. Then, the trapped charges density (N_{ot}) can be expressed as in the following equation [16, 17]:

$$N_{ot} = \frac{\Delta V_{FB} C_{ox}}{qA} \tag{1}$$

$$C_{ox} = C_{ac} \left[1 + \left(\frac{G_{ac}}{\omega C_{ac}} \right)^2 \right] \tag{2}$$

Where C_{ox} is the insulator capacitance, q is the electron charge (1.602×10^{-19} C), A is the electrode area, C_{ac} is the measured accumulation capacitance, ω is the angular frequency, and G_{ac} is the conductance in accumulation region. By this model, the N_{ot} is estimated to be 2.46×10^{12} cm^{-2}, 1.54×10^{12} cm^{-2}, and 6.20×10^{11} cm^{-2} for samples S1, S2, and S3 respectively.

The interface trap density (D_{it}) value is another characteristic to evaluate the interface property of fabricated MIS capacitors. By Hill-Coleman single-frequency approximation, the D_{it} can be expressed as [18]:

$$D_{it} = \frac{2}{qA} \cdot \frac{\frac{G_{ac}}{\omega}}{\left[\left(\frac{G_{max}}{\omega C_{ox}} \right)^2 + \left(1 - \frac{C_c}{C_{ox}} \right)^2 \right]} \tag{3}$$

Where G_{max} is the maximum value of conductance, and C_c is the corresponding capacitance of the gate
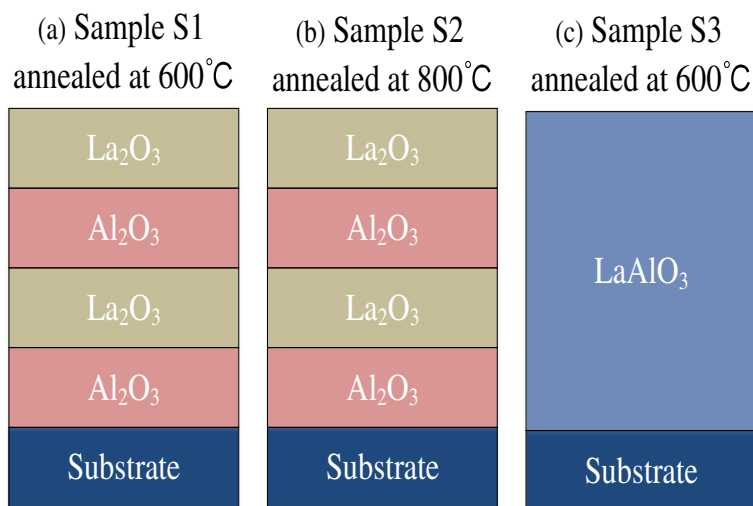
**Fig. 1** Schematic structures of multilayer La_2O_3/Al_2O_3 stack samples S1 and S2 and $LaAlO_3$ sample S3

Feng *et al. Nanoscale Research Letters* (2017) 12:230

Page 3 of 4

Table 1 The structures and annealing temperatures of samples S1–S3

Sample	Film structures	Annealing temperature
S1	$2 \times (20\text{-cycle } Al_2O_3 + 20\text{-cycle } La_2O_3)$	600 °C
S2	$2 \times (20\text{-cycle } Al_2O_3 + 20\text{-cycle } La_2O_3)$	800 °C
S3	$40 \times (1\text{-cycle } Al_2O_3 + 1\text{-cycle } La_2O_3)$	600 °C

voltage at which the G_{max} is obtained. The D_{it} of samples S1, S2, and S3 can be figured out as 1.24×10^{12} $eV^{-1}cm^{-2}$, 6.05×10^{11} $eV^{-1}cm^{-2}$, and 1.98×10^{12} $eV^{-1}cm^{-2}$ respectively. A higher D_{it} of sample S1 than S2 can be attributed to the more recombination of dangling bonds at the high-k/Si interface for a higher annealing temperature. Compared with S1, sample S3 contains more La_2O_3/Al_2O_3 interfaces (we can regard the $LaAlO_3$ dielectric film as a multilayer La_2O_3/Al_2O_3 stack which contains a very large number of plies), which means more interface trap.
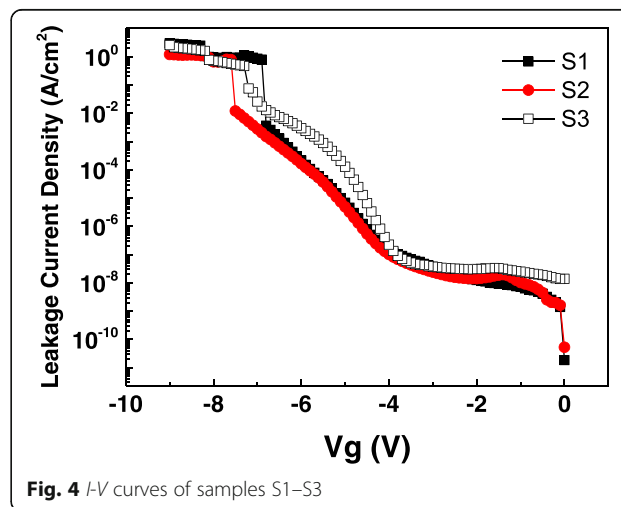
So, a significant promotion in these two electrical properties can be obtained for a multilayer La_2O_3/Al_2O_3 stack at 800 °C annealing temperature compared with 600 °C. However, for $LaAlO_3$ dielectric film, a promotion of N_{ot} and a degradation of D_{it} are obtained simultaneously. In a more comprehensive perspective, a better capacitance property are obtained from the $LaAlO_3$ dielectric film, since the lower flat band voltage and less ΔV_{FB}. And it is worth noting that a flat band voltage modulation can be carried out by manipulating the annealing temperature and the number of plies in multilayer La_2O_3/Al_2O_3 stack [19].
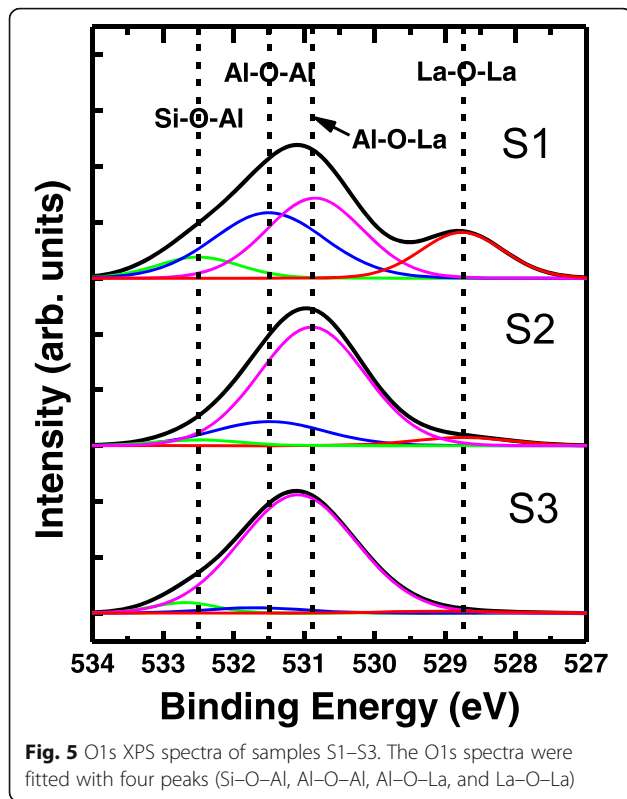
Figure 4 shows the leakage current density as a function of the applied gate voltage. S1 and S2 show a very similar leakage current, while S3 shows a $1 \sim 2$ orders of magnitude larger leakage current with the same applied gate voltage. Then, XPS was employed to seek the

Fig. 3 *G-V* curves of samples S1–S3
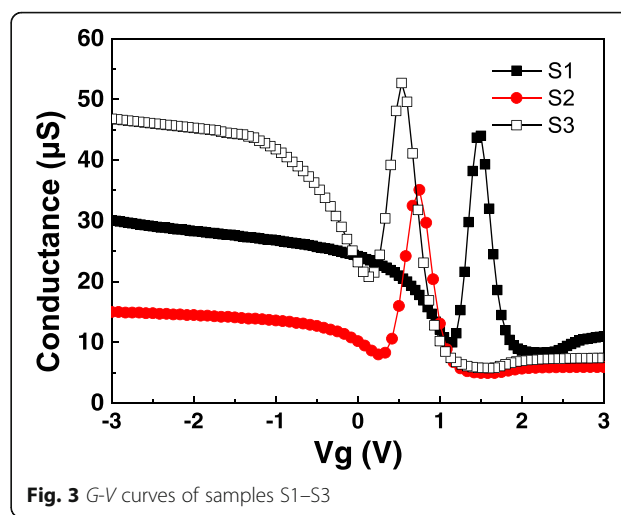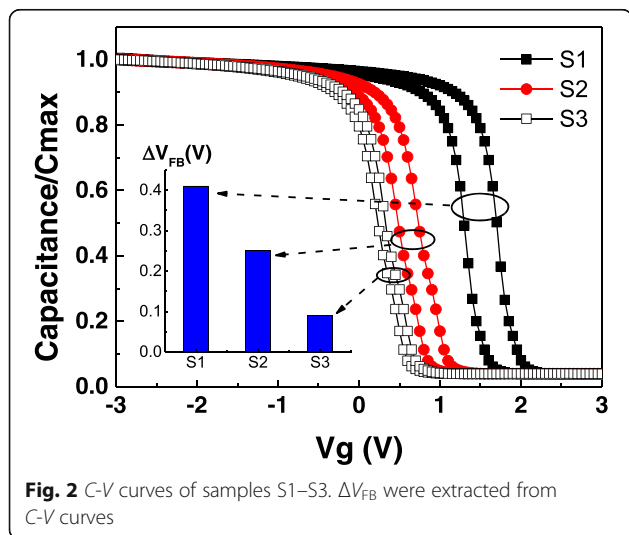
explanation. Figure 5 shows the O1s XPS spectra of samples S1–S3, which was fitted with four peaks Si–O–Al (532.5 eV), Al–O–Al (531.5 eV), Al–O–La (530.9 eV), and La–O–La (528.75 eV). It is obvious that La–O–Al peaks become larger, while La–O–La, Al–O–Al, and Si–O–Al peaks become smaller from S1 to S3. Therefore, compared with S1 and S2, more La_2O_3 will appear at the interface of high-k/Si in sample S3. La_2O_3 has lower conduction band offset (CBO) and valence band offset (VBO) with respect to p-type Si substrate compared with Al_2O_3 (the CBO and VBO are about 2.3 and 2.6 eV for La_2O_3 and are about 2.8 and 4.9 eV for Al_2O_3) [20]. So, the increase of La_2O_3 in the high-k/Si interface will lead to the decrease of band offset as well as the increase of leakage current.

In addition, we notice that the sample S2 has a higher breakdown voltage than S1. It can be attributed to the lower trapped charges density, since structural defects lead to the possibility to generate a conduction path in gate dielectric [15].

Fig. 2 *C-V* curves of samples S1–S3. ΔV_{FB} were extracted from *C-V* curves

Fig. 4 *I-V* curves of samples S1–S3

Feng *et al. Nanoscale Research Letters* (2017) 12:230

Page 4 of 4

Fig. 5 O1s XPS spectra of samples S1–S3. The O1s spectra were fitted with four peaks (Si–O–Al, Al–O–Al, Al–O–La, and La–O–La)

Conclusions

In summary, the capacitance and leakage current properties for multilayer La_2O_3/Al_2O_3 stacks and $LaAlO_3$ dielectric film have been studied systematically. A clear promotion of capacitance properties is observed for multilayer La_2O_3/Al_2O_3 stacks after PDA at 800 °C compared with that at 600 °C. As for $LaAlO_3$ dielectric film, compared with multilayer La_2O_3/Al_2O_3 dielectric stacks, a promotion of N_{ot} and a degradation of D_{it} can be obtained at the same time. On the other hand, the $LaAlO_3$ dielectric film presents a better leakage property which attributes to its higher CBO and VBO with respect to p-type Si substrate. And the breakdown behavior showed a clear improvement for the film with a higher annealing temperature for its less defects.

Abbreviations

ALD: Atomic layer deposition; CBO: Conduction band offset; CMOS: Complementary metal oxide semiconductor; *C-V*: Capacitance-voltage; D_{it}: Interface trap density; *G-V*: Conductance-voltage; *I-V*: Leakage current-voltage; N_{ot}: Trapped charges density; PAD: Post-deposition annealing; RTA: Rapid thermal annealing; TMA: Trinethyluminium; VBO: Valence band offset; XPS: X-ray photoelectron spectroscopy

Authors' Contributions

The research idea is from XyF; the work of the data analysis and the paper writing are also from XyF. XyF and XW carried out the experiments and the measurements. XW, LZ, CxF, and HlL participated in the discussions. HxL has given final approval of the version to be published. All authors read and approved the final manuscript.

Authors' Information

XyF and HlL are master students in the Xidian University. HxL is a professor in the Xidian University. XW, LZ, and CxF are PhD students in the Xidian University.

Competing Interests

The authors declare that they have no competing interests.

Publisher's Note

Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

References

1. Ye C, Wang Y, Zhang J et al (2011) Evidence of interface conversion and electrical characteristics improvement of ultra-thin HfTiO films upon rapid thermal annealing. Appl Phys Lett 99(18):182904
2. Liu J, Liao M, Imura M et al (2014) Low on-resistance diamond field effect transistor with high-*k* ZrO_2 as dielectric. Scientific Reports 4(7416):6395–6395
3. Liu JW, Liao MY, Imura M et al (2014) Diamond field effect transistors with a high-dielectric constant Ta_2O_5 as gate material. J Phys D Appl Phys 47(24):113–116
4. He G, Chen X, Sun Z (2013) Interface engineering and chemistry of Hf-based high-k dielectrics on III–V substrates. Surf Sci 68(1):68–107
5. He G, Deng B, Chen H et al (2013) Effect of dimethylaluminumhydride-derived aluminum oxynitride passivation layer on the interface chemistry and band alignment of HfTiO-InGaAs gate stacks. APL Materials 1(1):091002
6. He G, Liu J, Chen H et al (2014) Interface control and modification of band alignment and electrical properties of HfTiO/GaAs gate stacks by nitrogen incorporation. J Mater Chem C 2(27):5299–5308
7. He G, Gao J, Chen H et al (2014) Modulating the interface quality and electrical properties of HfTiO/InGaAs gate stack by atomic-layer-deposition-derived Al2O3 passivation layer. ACS Appl Mater Interfaces 6(24):22013–25
8. Zhao Y, Kita K, Kyuno K et al (2009) Band gap enhancement and electrical properties of La_2O_3 films doped with Y_2O_3 as high-k gate insulators. Appl Phys Lett 94:042901
9. Cao D, Cheng X, Yu Y et al (2013) Competitive Si and La effect in HfO_2 phase stabilization in multilayer $(La_2O_3)0.08(HfO_2)$ films. Appl Phys Lett 103:081607
10. Jayanti S, Yang X, Lichtenwalner DJ et al (2010) Technique to improve performance of Al_2O_3 interpoly dielectric using a La_2O_3 interface scavenging layer for floating gate memory structures. Appl Phys Lett 96(9):092905
11. Lee WJ, Ma JW, Bae JM et al (2013) The diffusion of silicon atoms in stack structures of La_2O_3 and Al_2O_3. Curr Appl Phys 13(4):633–639
12. Fujitsuka R, Sakashita M, Sakai A et al (2005) Thermal stability and electrical properties of $(La_2O_3)_{1−x}(Al_2O_3)_x$ composite films. Jpn J Appl Phys 44:2428–2432
13. Sivasubramani P, Kim MJ, Gnade BE et al (2005) Outdiffusion of La and Al from amorphous $LaAlO_3$ in direct contact with Si (001). Appl Phys Lett 86(20):201901
14. Pelloquin S, Saint-Girons G, Baboux N et al (2013) LaAlO3/Si capacitors: comparison of different molecular beam deposition conditions and their impact on electrical properties. J Appl Phys 113:034106
15. Wang X, Liu H, Fei C et al (2016) Electrical properties and interfacial issues of high-k/Si MIS capacitors characterized by the thickness of Al_2O_3 interlayer. AIP Adv 6(6):034106–236
16. Sze SM, Ng Kwok K (2006) Physics of semiconductor devices, 3rd edn. John Wiley & Sons Inc, New Jersey
17. Nicollian EH, Brews JR (1982) MOS physics and technology. John Wiley & Sons Inc, New York
18. Hill WA, Coleman CC (1980) A single-frequency approximation for interface-state density determination. Solid State Electron 23(9):987–993
19. Feng X-Y, Liu H-X, Wang X et al (2016) Impacts of annealing conditions on the flat band voltage of alternate La_2O_3/Al_2O_3 multilayer stack structures. Nanoscale Res Lett 11:1
20. Robertson J (2005) Interfaces and defects of high-K oxides on silicon. Solid State Electron 49(3):283–293