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Research Article

Realization of DVCCTA Based Versatile Modulator

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A Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) based versatile modulator is proposed which can work as an amplitude modulator, frequency modulator, delta modulator, and sigma delta modulator. The modulator operational scheme uses pulse generator as a core and its output is used as carrier signal. A DVCCTA based pulse generator is proposed first and subsequently configured as different modulators. Compact realization is the key feature of the proposed circuit as it uses two DVCCTA; a grounded resistor and a grounded capacitor hence are appropriate for IC realization. The functionality of the proposed circuit is verified through SPICE simulations using TSMC 0.25 μm CMOS process model parameters. The performance parameters such as power dissipation and noise for various modulator schemes are also obtained.

1. Introduction

Modulation is a process of modifying some characteristic of a carrier signal according to the instantaneous value of modulating signal and is a fundamental requirement of any communication system. Analog and digital modulations are two representative classes of modulation techniques. Amplitude and frequency modulation fall under analog modulation schemes wherein amplitude and frequency of the carrier signal, respectively, are varied according to the instantaneous value of the modulating signal while keeping other parameters constant. Delta and sigma delta modulation belong to digital modulation and are widely used in digital communication and digital signal processing and analog to digital converters.

Mobile communication systems and portable electronic equipment demand low-power circuitry to enable longer battery operation. The current-mode (CM) processing has emerged as a promising solution for such circuits as CM circuits are designed for lower voltage swings. Exploiting this virtue of CM processing the researchers have reported a large number of modulator circuits using different CM active building blocks (ABB) such as current conveyor II (CCII) [1], operational transconductance amplifier (OTA) [2–4], current controlled current difference transconductance amplifier (CCCDTA) [5], multiple output current controlled current difference transconductance amplifier (MOCCCDTA) [6], and operational transresistance amplifier (OTRA) [7]. The pulse width of the carrier signal is modulated in accordance with input modulating signal in circuits proposed in [1–7]. Sigma delta modulators are the other class of modulators available in literature [4, 8–15]. These modulators can be classified as designs based on (i) switched capacitor technique [8–11], (ii) switched current technique [12], (iii) Loop filter and quantizer method [13–15], and (iv) ABB [4]. A detailed comparison of these structures is given in Table 1. It is evident from Table 1 that a large number of modulator circuits are available in literature but only the modulator structure of [4] can provide amplitude, frequency, delta, and sigma delta modulated outputs. In this paper, a DVCCTA based versatile modulator is presented which employs two ABBs and two grounded passive elements only as against the three ABBs and three passive elements used in [4].

The paper is organized as follows. Section 2 describes the port relation of DVCCTA and its CMOS based implementation. Operational scheme of the proposed modulator

Table 1: Comparison of exiting modulator topologies.

Ref. number	Implementation scheme	Active element used	Modulation type
[1]	Schmitt trigger followed by integrator	CCII, Opamps	PWM
[2, 3]	Schmitt trigger followed by integrator	OTAs	PWM
[4]	Schmitt trigger followed by integrator	OTAs	AM, FM, delta, and sigma delta
[5]	Schmitt trigger followed by integrator	CCCDTA	PWM
[6]	Schmitt trigger followed by integrator	MOCCCDTA	PWM
[7]	Schmitt trigger followed by integrator	OTRA	PWM
[8]	Switched capacitor	Opamps	Sigma delta
[9]	Comparator based switched capacitors	Dynamic Comparator OTA	Sigma delta
[10]	Class-C inverter switched capacitor	Class-C inverter	Sigma delta
[11]	Comparator based switched capacitors	Opamps	Sigma delta
[12]	Switched current CMOS	None	Sigma delta
[13–15]	Loop filter + quantizer	Opamps	Sigma delta
Proposed	Schmitt trigger followed by integrator	DVCCTA	AM, FM, delta, and sigma delta

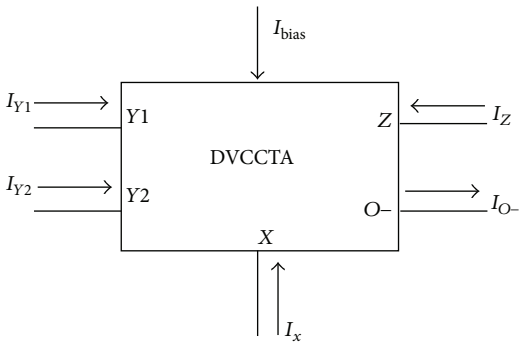

Figure 1: Symbol of proposed DVCCTA.

is elaborated in Section 3 wherein a DVCCTA based pulse generator core is described first followed by its applications as amplitude, frequency, delta, and sigma delta modulators. The proposed work is concluded in Section 6.

2. DVCCTA

The DVCCTA [16], a relatively new ABB, employs DVCC [17] as input block which is followed by a TA. The circuit symbol of DVCCTA is shown in Figure 1 and its terminal characteristics in matrix form are given by

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -g & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \\ V_{O-} \end{bmatrix}, \quad (1)$$

where g is transconductance of the DVCCTA. The CMOS implementation of DVCCTA [16] is given in Figure 2. It comprises of a DVCC block (Md1–Md12) [16] which is followed by transconductance amplifier (Md13–Md20). The value of transconductance (g) is expressed by (2) which can be adjusted by varying current I_{Bias}, thereby making it electronically tunable:

$$g = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_{15,16} I_{\text{Bias}}}. \quad (2)$$

3. Modulator Operational Scheme

The modulator operational scheme uses pulse generator as a core and its output is used as carrier signal. The pulse generator can be constructed using the well-known scheme of placing an integrator in a feedback loop with Schmitt trigger [18] as shown in Figure 3 and has been implemented using DVCCTA in this work. The DVCCTA based realization of pulse generator is depicted in Figure 4. The first DVCCTA with capacitor C forms an integrator, whereas the second DVCCTA works as Schmitt trigger with resistor R.

The operation of the circuit is as follows. Both DVCCTAs operate in saturation mode irrespective of the bias currents and voltages at the input terminals as their Z ports are left open. The voltage of Z port would approach to V_{DD} or V_{SS} depending upon the current flowing into X (I_{in}) terminal:

$$V_Z = \begin{cases} V_{\text{DD}} & \text{for } I_{\text{in}} \geq 0 \\ V_{\text{SS}} & \text{for } I_{\text{in}} < 0. \end{cases} \quad (3)$$

It may be noted that the amplitude of current would be positive if voltage of $Y1$ terminal is larger than $Y2$ terminal voltage. The amplitude of current flowing through $O-$ port would remain constant and equal to bias current (I_{Bias}) and the exact values would be given by

$$I_{O-} = \begin{cases} -I_{\text{Bias}} & \text{for } I_{\text{in}} \geq 0 \\ I_{\text{Bias}} & \text{for } I_{\text{in}} < 0. \end{cases} \quad (4)$$

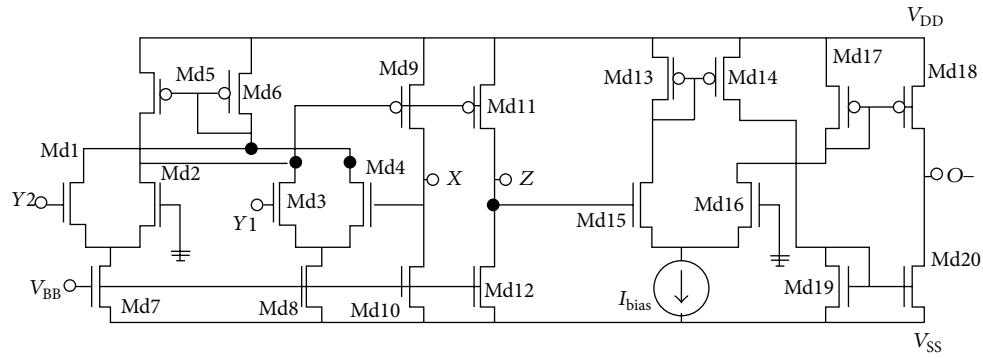

Figure 2: CMOS implementation of DVCCTA [16].

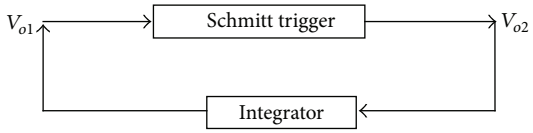

Figure 3: Pulse generator scheme [18].

The maximum and minimmum output voltages of the schmitt trigger are given by the following:

$$V_{\max} = I_{\text{Bias2}} R, \tag{5a}$$

$$V_{\min} = -I_{\text{Bias2}} R. \tag{5b}$$

The upper and lower threshold values for the schmitt trigger are given by

$$V_{\text{TH}} = V_{\max} = I_{\text{Bias2}} R, \tag{6a}$$

$$V_{\text{TL}} = V_{\min} = -I_{\text{Bias2}} R. \tag{6b}$$

The frequency of the output signal can be obtained by calculating the charging (to V_{TH}) and discharging (to V_{TL}) time of the capacitor. The time taken by the capacitor to charge to V_{TL} from level V_{TH} is given by

$$t_1 = \frac{C\left(V_{\text{TH}} - V_{\text{TL}}\right)}{I_{\text{Bias1}}}. \tag{7}$$

The time taken by the capacitor to discharge from V_{TH} to V_{TL} is given by

$$t_2 = \frac{C\left(V_{\text{TL}} - V_{\text{TH}}\right)}{-I_{\text{Bias1}}}. \tag{8}$$

The frequency of the output signal is expressed as

$$f = \frac{1}{t_1 + t_2}. \tag{9}$$

As V_{TL} and V_{TH} are equal in magnitude, using (6a) and (6b) to (9), the frequency is computed by (10) which can be adjusted electronically via bias currents of DVCCTAs:

$$f = \frac{I_{\text{Bias1}}}{4RCI_{\text{Bias2}}}. \tag{10}$$

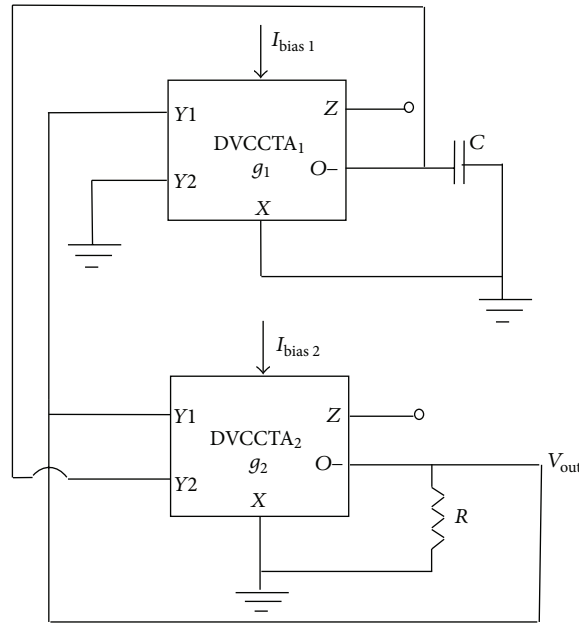

Figure 4: Proposed DVCCTA based pulse generator.

In the following subsections, analog (AM and FM) and digital (delta and sigma delta modulation) modulator circuits based on pulse generator circuit of Figure 4 are presented.

3.1. Amplitude Modulator. In amplitude modulation, the amplitude of the carrier signal varied according to the instantaneous value of the modulating signal. According to (5a) and (5b), the output amplitude of the pulse generator circuit of Figure 4 depends on bias current I_{Bias2}. Therefore, the pulse generator circuit can work as amplitude modulator if the bias currents I_{Bias1} and I_{Bias2} are taken as sinusoidal modulating signal ($I_m(t)$) superposed on the dc offset signal (I_{offset}). The condition on the amplitude of modulating signal and offset current is given by

$$I_{\text{Bias2}} = I_{\text{offset}} + I_m(t) \quad \forall t. \tag{11}$$

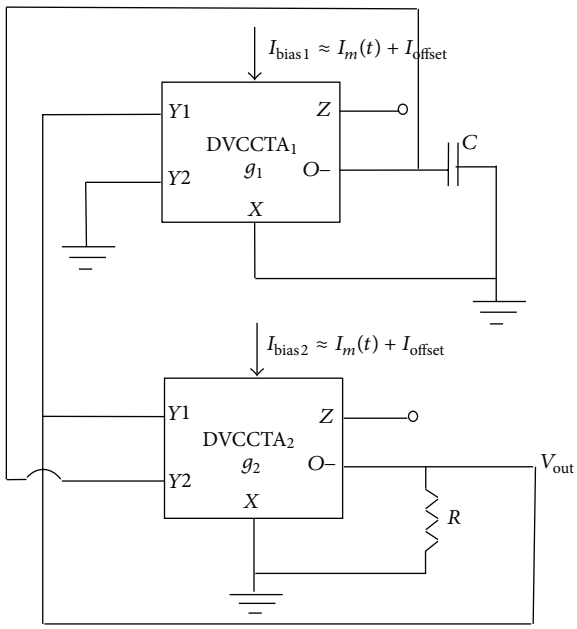

Figure 5: Proposed AM modulator.

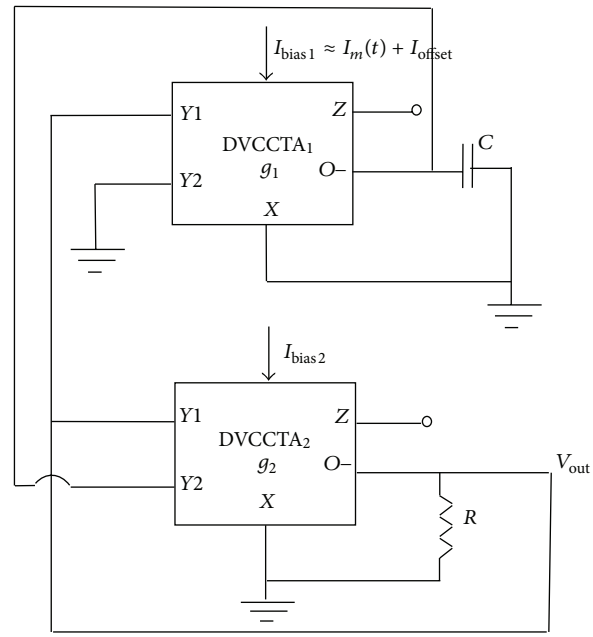

Figure 6: Proposed FM modulator.

Using (5a) and (5b), the maximum and minimum output voltages are expressed by

$$V_{\max} = \left(I_{\text{offset}} + I_m(t)\right) R, \tag{12a}$$

$$V_{\min} = -\left(I_{\text{offset}} + I_m(t)\right) R. \tag{12b}$$

Thus peak to peak output voltage is given by

$$V_{\text{out}} = 2\left(I_{\text{offset}} + I_m(t)\right) R. \tag{13}$$

The output voltage amplitude is proportional to modulating signal if a sufficiently large offset current is chosen. Since the output frequency is function of ratio of bias currents $I_{\text{Bias1}}/I_{\text{Bias2}}$ as shown by (10), the output frequency remains unaltered if the ratio of bias currents I_{Bias1} and I_{Bias2} are kept equal. Thus the circuit of Figure 5 works as an amplitude modulator.

3.2. Frequency Modulator. In frequency modulation, the frequency of the carrier signal varied according to the instantaneous value of the modulating signal. According to (10), the frequency of pulse generator is function of ratio of bias currents $I_{\text{Bias1}}/I_{\text{Bias2}}$ whereas the output amplitude depends solely on bias current I_{Bias2}. Therefore, the pulse generator circuit can work as frequency modulator if a sinusoidal modulating signal ($I_m(t)$) superimposed on the dc offset signal (I_{offset}) is applied as bias currents I_{Bias1} while keeping bias current I_{Bias2} constant. This selection of bias currents causes the output to toggle between $I_{\text{Bias2}}R$ and $-I_{\text{Bias2}}R$ whose frequency varies with the instantaneous value of the modulating current. Figure 6 shows the DVCCTA based frequency modulator.

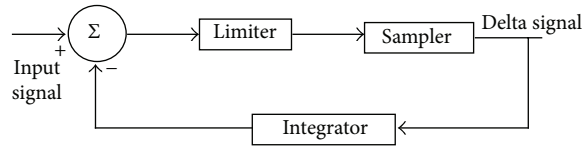

Figure 7: Delta modulator scheme.

3.3. Delta Modulator. The pulse code modulation (PCM) is fundamental technique for digital modulation. It, however, has drawback of data redundancy in digitally encoded data. The differential pulse code modulation (DPCM) eliminates this problem by encoding difference between successive samples. Delta modulation is a special case of DPCM where the output is one bit encoded. The schematic of delta modulation is shown in Figure 7 wherein the difference of the input and integrated output signal is applied to limiter and sampler. The 1st DVCCTA of Figure 4 gives integrated output as capacitor voltage. The 2nd DVCCTA provides functionality of both limiter and sampler as it generates output voltage $I_{\text{Bias2}}R$ or $-I_{\text{Bias2}}R$ by comparing the output voltage with the capacitor voltage. If the modulating input signal is connected to $Y1$ terminal of 2nd DVCCTA as shown in Figure 8, then the comparison is performed between modulating and integrated output signals which is desired in delta modulator.

3.4. Sigma Delta Modulator. Sigma delta modulation is another scheme, as shown in Figure 9, which can be considered as smoothed version of delta modulation [19]. The name sigma delta modulator comes from the fact that a sigma

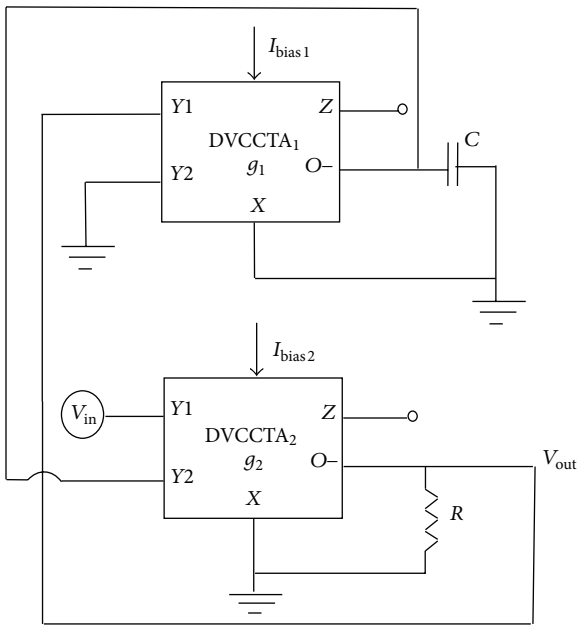

Figure 8: Proposed delta modulator.

Table 2: Aspect ratio of transistors.

DVCCTA	
MOSFETs	W (μm)/L (μm)
Md5, Md6, Md13, Md14, Md17–Md20	5/0.5
Md9, Md11	8.5/0.5
Md1, Md2, Md3, Md4	10/0.5
Md15, Md16	27/0.5
Md7, Md8	27.25/0.5
Md10, Md12	44/0.5

which means integrator is put in front of delta modulator. A close observation of the schematic of Figures 7 and 9 indicates that the only difference in the implementation scheme of the delta and sigma delta modulator lies in the way input is fed to a limiter and a sampler blocks. The limiter and sampler blocks as shown in Figures 7 and 9 can be realized with DVCCTA based pulse generator circuit implemented in Figure 4. For sigma delta modulation, the difference between output and modulating signal need to be integrated. This can be easily achieved by the voltage differencing property of the DVCCTA (building block employed in pulse generator circuit), that is by simply connecting modulating signal to $Y2$ terminal of first DVCCTA block in Figure 4. The resulting DVCCTA based schematic of sigma delta modulator is shown in Figure 10.

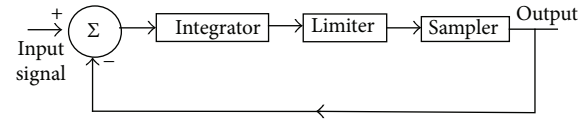

Figure 9: Sigma delta modulator scheme.

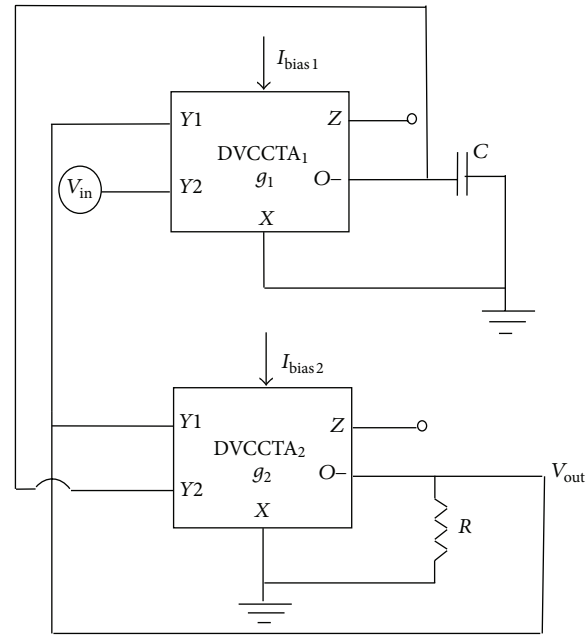

Figure 10: Proposed sigma delta modulator.

4. Simulation Results

The theoretical propositions have been verified through SPICE simulations using TSMC 0.25 μm CMOS process model parameters. The CMOS schematic of Figure 2 is used for DVCCTA implementation. Aspect ratio used for various transistors is given in Table 2. Supply voltages of $V_{DD} = -V_{SS} = 1.25$ V and $V_{BB} = -0.8$ V are used and the passive components are chosen as $C = 100$ pF and $R = 4$ KΩ. The voltage V_Z and current I_{O-} responses of proposed pulse generator are plotted in Figures 11 and 12, respectively, for $I_{Bias1} = I_{Bias2} = 20\,\mu$A. It may be noted that V_Z and I_{O-} saturate to supply voltages and bias current, respectively, thus verifying the theoretical propositions of (3) and (4). The pulse generator output and the voltage across the capacitor are depicted in Figure 13. The transient responses of the pulse generator by simultaneous variation of I_{Bias1} and I_{Bias2} from 20 μA to 50 μA in step of 10 μA are shown in Figures 14(a)–14(d), respectively. The analytical and simulated pulse generator output amplitude curves with respect to bias currents, for different capacitance values (50 pF, 100 pF, and 200 pF) are plotted in Figure 15. It is observed from Figure 15 that the output amplitude is dependent on bias currents irrespective of capacitance value

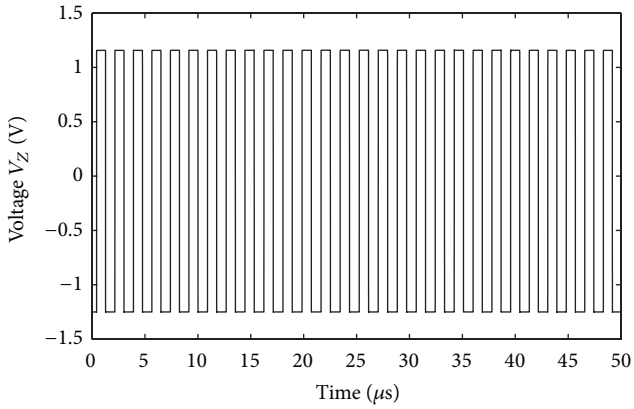

Figure 11: Voltage V_Z of pulse generator.

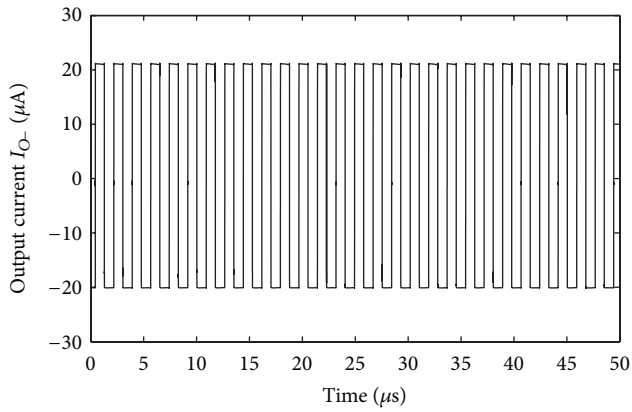

Figure 12: Current I_{O-} of pulse generator.

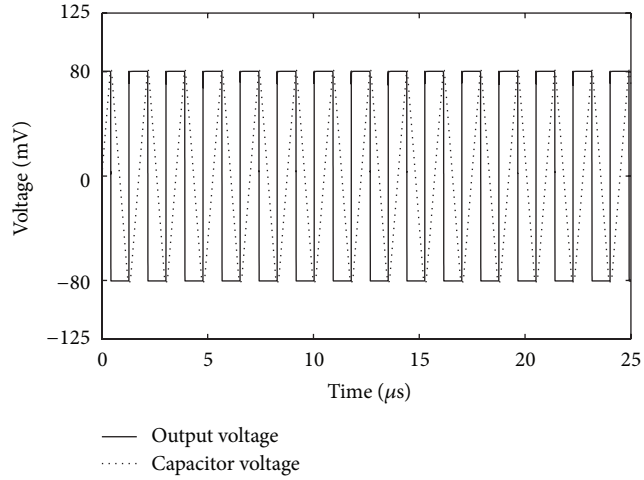

Figure 13: Output and capacitor's voltage waveform of pulse generator.

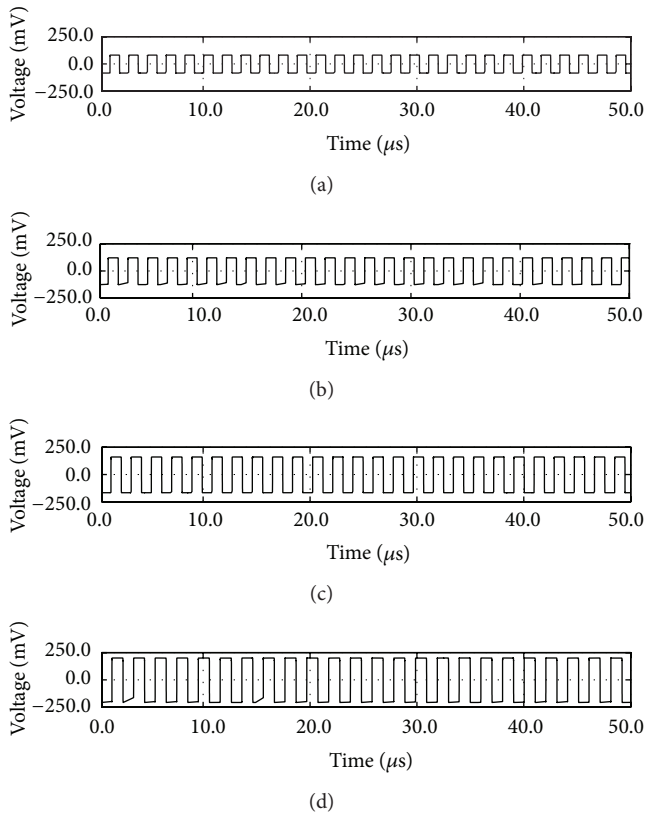

Figure 14: Output voltage with (a) $I_{Bias1} = I_{Bias2} = 20\,\mu$A, (b) $I_{Bias1} = I_{Bias2} = 30\,\mu$A, (c) $I_{Bias1} = I_{Bias2} = 40\,\mu$A, and (d) $I_{Bias1} = I_{Bias2} = 50\,\mu$A.

which is in tune with the proposed theory. It may also be noted that the analytical and simulated responses are in close agreement. The transient responses of the pulse generator, showing frequency variation with I_{Bias1}, have been depicted in Figures 16(a)–16(d) wherein I_{Bias1} is varied from 10 μA to 50 μA in step of 10 μA keeping I_{Bias2} fixed at 20 μA. Figure 17 shows the analytical and simulated frequency versus I_{Bias1} curves, for different capacitor values, depicting the frequency controllability through I_{Bias1}. Both analytical and simulated frequency curves are found to be in synchronization.

In order to obtain amplitude modulated output, a 10 μA, sinusoidal modulating signal of 10 KHz is superimposed on the bias currents I_{Bias1} and I_{Bias2} keeping DC offset to be 20 μA. The modulating current signal and amplitude modulated output voltage are shown in Figures 18(a) and 18(b), respectively. The workability of pulse generator as frequency modulator is verified by applying $I_{Bias1}(t)$ as a 20 μA, 10 KHz sinusoidal modulating signal with a DC offset of 30 μA, and keeping I_{Bias2} constant at 20 μA. The modulating and the modulated output signals are shown in Figures 19(a) and 19(b), respectively. The performance of the delta and sigma delta modulators is verified for two different modulating signals: a triangular and a sinusoidal, each one represented as 50 KHz, 150 mV signal. The bias currents I_{Bias1} and I_{Bias2} are, respectively, set as 20 μA and 40 μA. The outputs of delta modulator for triangular and sinusoidal modulating signals are shown in Figures 20 and 21, respectively, and those

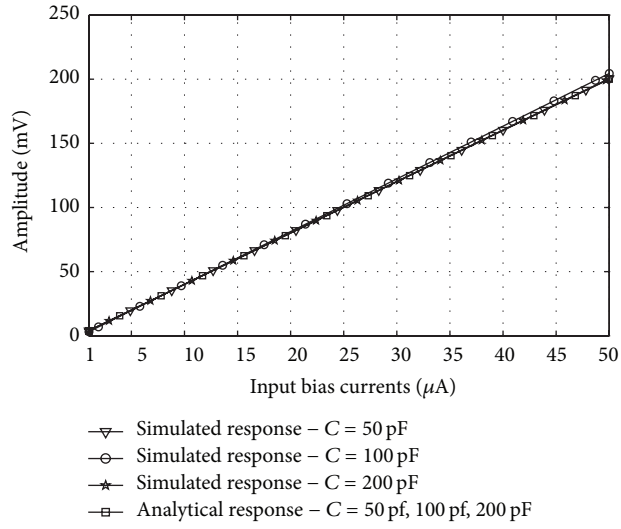

Figure 15: Amplitude versus bias current of pulse generator.

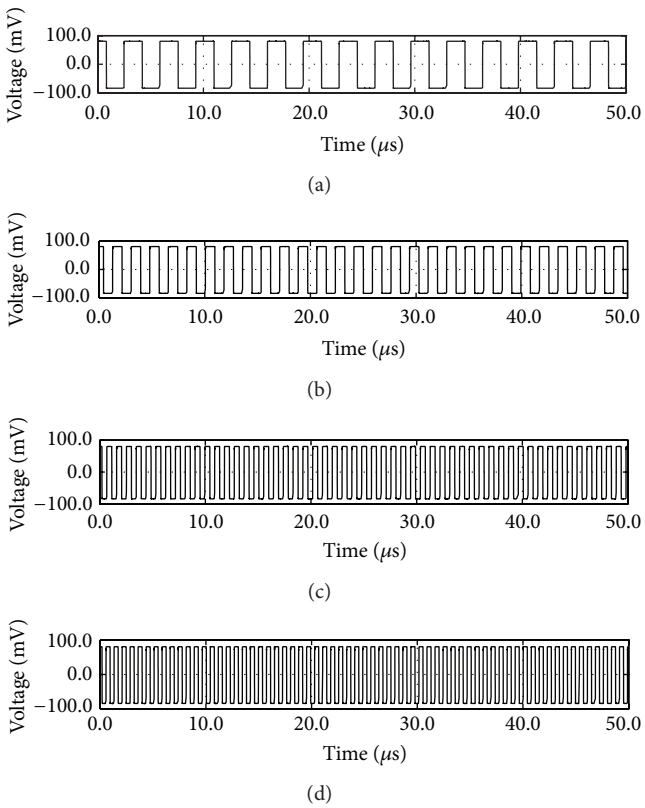

Figure 16: Output voltage with I_{Bias2} = 20 μA and I_{Bias1} = (a) 10 μA, (b) 20 μA, (c) 40 μA, and (d) 50 μA.

for sigma delta modulators are given in Figures 22 and 23, respectively.

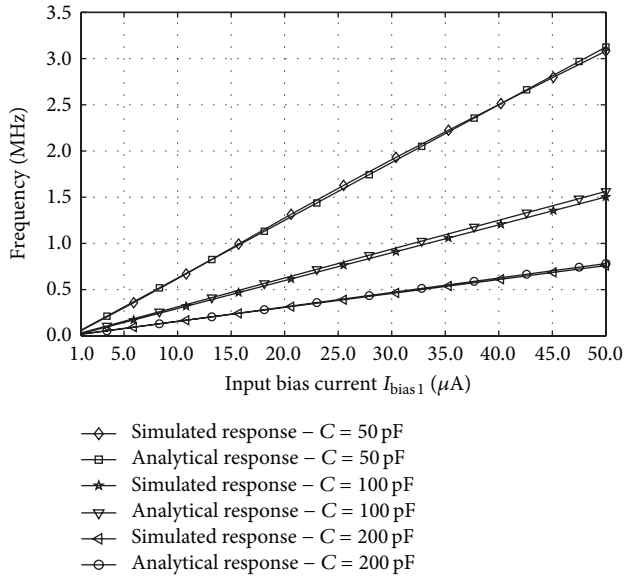

Figure 17: Frequency control of pulse generator.

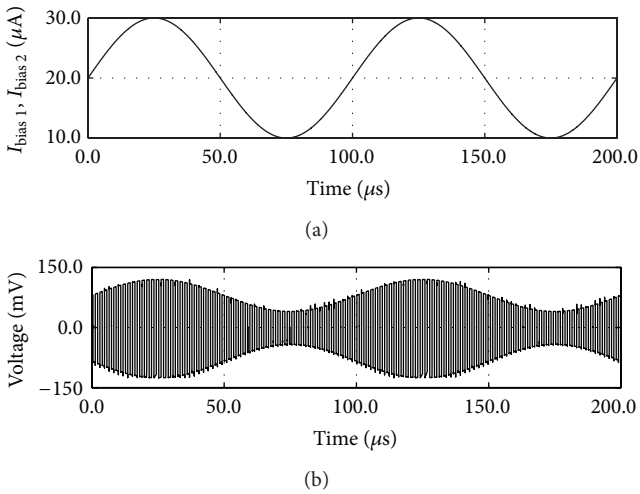

Figure 18: (a) Modulating signal and (b) amplitude modulated signal.

Table 3: Performance characteristics of DVCCTA based modulators.

Modulator type	Power dissipation (mW)	Output noise voltage (nV)
AM modulator	0.55 mW	15.64 nV
FM modulator	0.36 mW	4.50 nV
Delta modulator	1.69 mW	5.79 nV
Sigma delta modulator	0.63 mW	15.64 nV

5. Performance Evaluation

The performance of proposed DVCCTA based modulator circuits is studied in terms of power dissipation. The overall

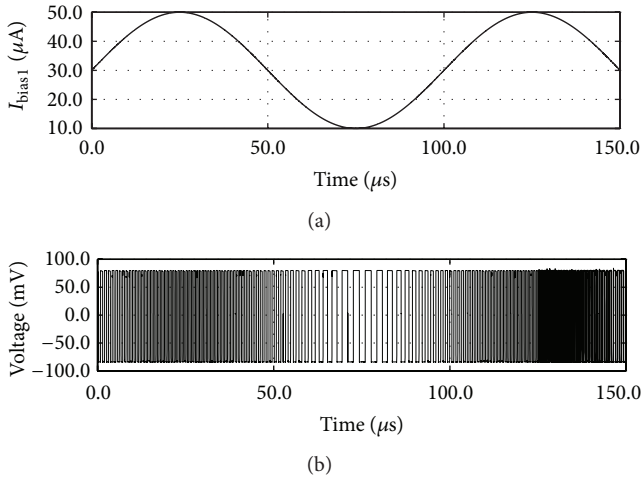

Figure 19: (a) Modulating signal and (b) frequency modulated signal.

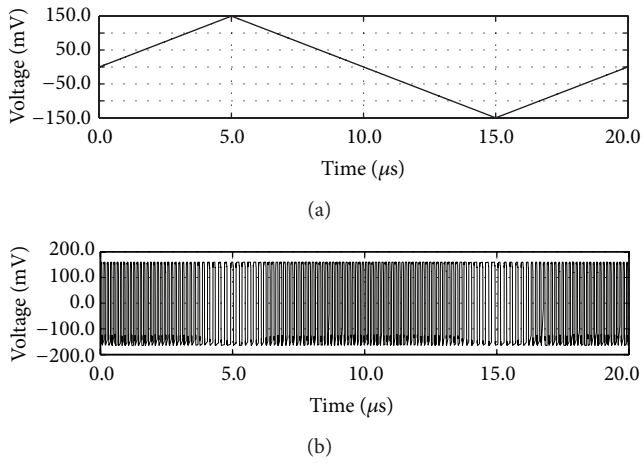

Figure 20: (a) Triangular modulating signal and (b) delta modulated signal.

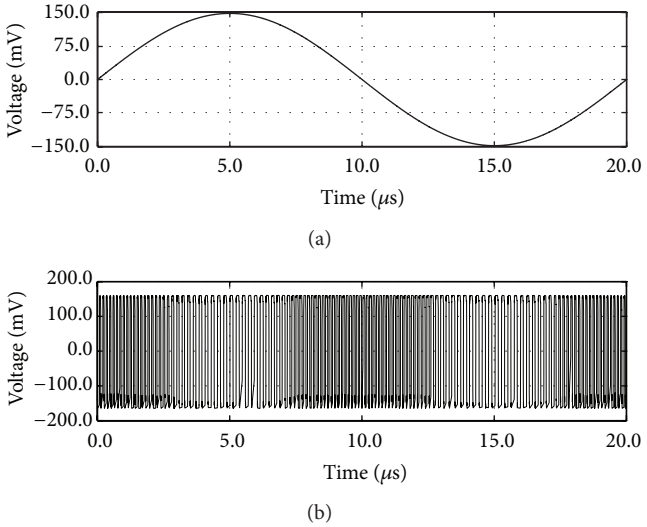

Figure 21: (a) Sinusoidal modulating signal and (b) delta modulated signal.

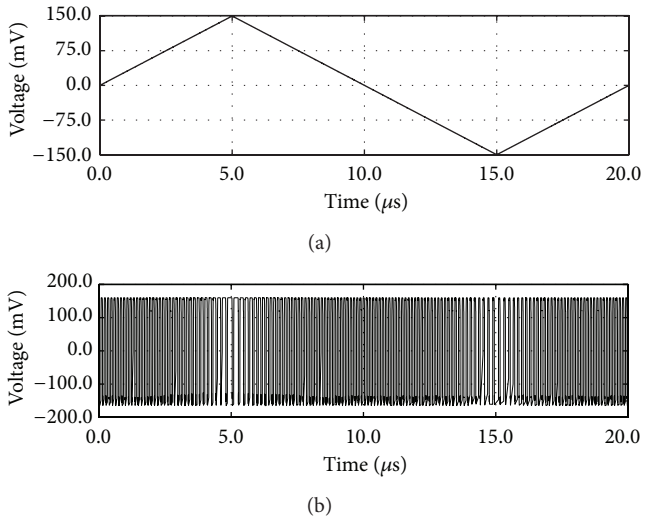

Figure 22: (a) Triangular modulating signal and (b) sigma delta modulated signal.

performance characteristics of DVCCTA based modulators are summarized in Table 3. The performance of proposed DVCCTA based modulator circuits is studied in terms of power dissipation and output noise voltage. The power dissipation of the versatile modulator circuit when I_{Bias1} and I_{Bias2} are set to 1 μA each is 0.418 mW. The minimum cut-off value of the input bias current, I_{Bias2} for proper functioning of circuit as an amplitude modulator, is 0.5 μA. The modulating signal with maximum frequency of 3.84 MHz can be applied to FM Modulator when I_{Bias1} is set to 0.01 μA. On increasing the magnitude of I_{Bias1}, the frequency of modulating signal can be increased to maximum value of carrier signal frequency.

6. Conclusion

A differential voltage current conveyor transconductance amplifier (DVCCTA) based modulator configuration is presented in this paper. A pulse generator based on DVCCTA has been is proposed and later configured as AM, FM, delta, and sigma delta modulator. The topology uses grounded capacitor and is suitable from integration viewpoint. The simulation results are included to demonstrate the workability of the pulse generator scheme and different modulation schemes. The performance of modulation schemes is studied in terms of power dissipation and noise.

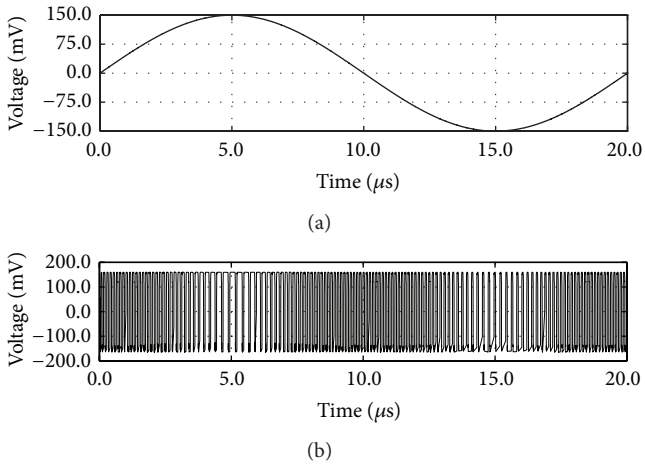

Figure 23: Sinusoidal modulating signal and (b) sigma delta modulated signal.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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