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Research Article

Leakage Immune Modified Pass Transistor Based 8T SRAM Cell in Subthreshold Region

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The paper presents a novel 8T SRAM cell with access pass gates replaced with modified PMOS pass transistor logic. In comparison to 6T SRAM cell, the proposed cell achieves 3.5x higher read SNM and 2.4x higher write SNM with 16.6% improved SINM (static current noise margin) distribution at the expense of 7x lower WTI (write trip current) at 0.4 V power supply voltage, while maintaining similar stability in hold mode. The proposed 8T SRAM cell shows improvements in terms of 7.735x narrower spread in average standby power, 2.61x less in average T_{WA} (write access time), and 1.07x less in average T_{RA} (read access time) at supply voltage varying from 0.3 V to 0.5 V as compared to 6T SRAM equivalent at 45 nm technology node. Thus, comparative analysis shows that the proposed design has a significant improvement, thereby achieving high cell stability at 45 nm technology node.

1. Introduction

During the last decade, extensive consideration has been given to the use of low power static random access memory (SRAM) cell design which is a crucial component in the memory hierarchy of modern computing systems. Owing to these facts, SRAMs are expected to occupy more than 70% of the final system-on-chip (SoC) area [1]. Thus, SRAM's area, power, performance, and leakage became significant deciding factors in overall budgeting of SoC. To satisfy the low power requirement of the SRAM cells, subthreshold design technique is being introduced which involves scaling voltage below the device threshold [2]. As a result of reduced voltage, all the leakage components in an SRAM cell are effectively minimized.

However, nanoscaled SRAM bit-cells in subthreshold regime having minimum supply voltage and minimum sized transistors are vulnerable to sensitivity of the device parameters (e.g., length, width, oxide thickness, subwavelength lithography, etching, and annealing) and circuit parameters (e.g., delay and leakage power, leading to loss in parametric yield). The resultant effects of sensitivity increase the interdie as well as intradie process variations which limits the circuit operation in the subthreshold region. Intradie process variations include random dopant fluctuation (RDF) due to threshold voltage (V_{th}) mismatch between the adjacent transistors in a memory cell, line edge roughness (LER), and so forth. In SRAM cell read, write access and hold failures, both parametric and functional, can occur due to fluctuation in V_{th}, caused by process variations, which consequently deteriorates the yield. Accordingly, variation in threshold voltage directly influences current, noise, power dissipation, and the speed of the cell and is not able to perform expected functions in subthreshold regime at 45 nm technology [3, 4].

Numerous prominent publications have appeared over the recent years targeted at low power SRAM cells design to improve cell stability in subthreshold regime. In [5], static noise margin (SNM) evaluation of 6T SRAM bit-cell operating in subthreshold has been done. The detailed analysis of the statistical distribution of SNM with process variation provides a model for the tail of the probability density failure (PDF) that dominates SNM failures. Conventional low power 6T SRAM cell (6T) fails to achieve reliable subthreshold operation [6]. Single-ended low power conventional 6T suffers from stability during read/write analysis [7]. In [8], a new differential 10T bit-cell for the reliable subthreshold operation has been designed which effectively separates read and write operations, thereby achieving high cell stability.

In [9], a novel Schmitt trigger (ST) based fully differential 10T SRAM bit-cell has been presented which is suitable for subthreshold operation. The Schmitt trigger based bit-cell achieves 1.56x higher read SNM (V_{DD} = 0.4 V) compared to 6T. In [10], a novel scheme has been presented which uses dynamic mechanism cutting the feedback to improve the write SNM and lowering the write access time. The new 9T-cell SRAM design is similar to the 6T (some reduction exists due to the stacked transistors) structure which shows robust stability and 80% and 50% improvement in read and write SNM, respectively, in comparison to the 6T.

Subthreshold operating voltages leave less room for large SNM and provide inaccurate logic cells characterization, sensitive performance, instable functionality due to process, voltage, and temperature (PVT) variations, and read/write stability problems. This paper proposes a modified PMOS pass transistor logic- (PTL-) based eight-transistor SRAM cell (hereafter called MPT8T) and its thorough evaluation performance which are compared with 6T in subthreshold regime at 45 nm technology. The MPT8T achieves better read and write stability, improved process variation tolerance, lower read failure probability, low-voltage/low power operation, and improved data retention capability at 0.4 V. The results are observed to be better than alternative SRAM cell design as discussed later in Section 4.

The rest of the paper is organized as follows. Section 2 presents the detailed analysis of the proposed MPT8T and their read/write current analysis. Sections 3 and 4 describe the simulation methodology and overall post-layout simulation results of the proposed design and alternative designs. Section 5 presents a summary of the paper and the concluding remarks.

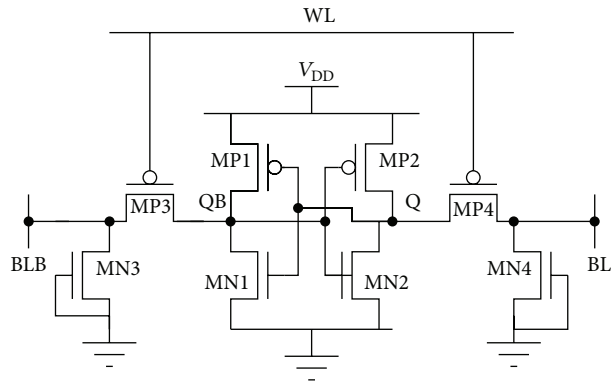

Figure 1: Design of MPT8T.

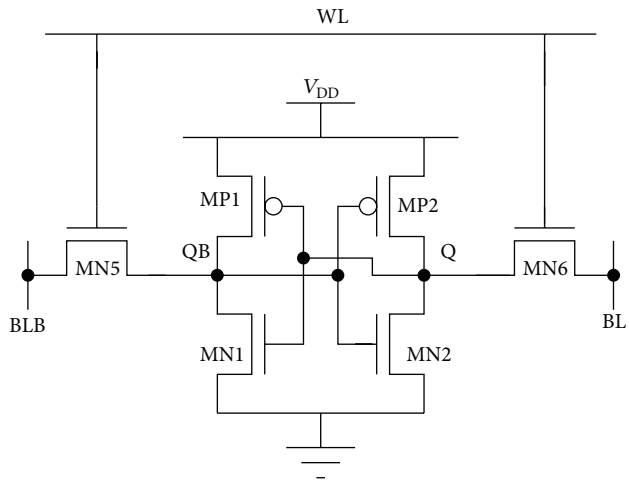

Figure 2: Design of 6T.

2. Design and Analysis of the Proposed MPT8T

2.1. Architecture Exploration and Operation. The proposed MPT8T SRAM cell comprises eight transistors as shown in Figure 1. The internal architecture of the proposed 8T SRAM cell consists of a cross-coupled inverter pair (MP1/MN1 and MP2/MN2) working as the storage cell to maintain 1-bit information. MPT8T utilizes differential operation and does not require much architectural change compared to the conventional 6T SRAM cell architecture as shown in Figure 2, except that the access transistors (MN5, MN6) of 6T are replaced by MP3-MN3 pair and MP4-MN4 pair, respectively, thereby making it an 8T SRAM cell. The additional NMOS transistors are connected in such a way that no additional control lines would be needed to switch the data of the cell; they remain in cutoff region for both read/write operations but help to overcome the voltage degradation and balance the leakage currents observed at 45 nm technology for PMOS (MP3/MP4) transistors.

The MPT8T SRAM cell operates as follows. *(a) For a read operation*, assume that "logic 0" is stored in the cell. The transistors MP2 and MN1 are turned off, while the transistors MP1 and MN2 operate in linear mode. Thus, internal node voltages are Q = "0" and QB = "1" before the access transistors (MP3 and MP4) are turned on. During read operation, the bit-lines (BL/BLB) are precharged to a high level (V_{DD}) and word-line (WL) is enabled (pulsed to a low level) which turns on the PMOS transistors of the corresponding access transistor pairs. After the pass transistors MP3 and MP4 are switched on, the voltage at BLB will not have a significant variation as no current flows through MP3. On the other hand, MP4 and MN2 will conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are sensed by sense amplifier. The read operation would be stable provided the node voltage Q does not exceed the threshold voltage of MN1. *(b) For a write operation*, consider a write "0" operation, assuming logic "1" is stored in the SRAM cell initially. The transistors MP1 and MN2 are turned off, while the transistors MN1 and MP2 operate in linear mode. Thus, internal node voltages are Q = "1" and QB = "0" before the access transistors (MP3 and MP4) are turned on. During write operation, the bit-lines BLB is precharged to a high level (V_{DD}) and BL is precharged to low level (logic "0") and WL is enabled (pulsed to a low level) which turns on the PMOS transistors of the corresponding access transistor pairs. After the pass transistors MP3 and MP4 are switched on, the voltage at node QB should not rise above the threshold voltage of MN2 to

Table 1: Results of conventional and modified access transistors logic at 0.4 V supply in 45 nm technology.

Access transistor type	Enable [EN = 1 for NMOS = 0 for PMOS] (ON condition)		Enable [EN = 0 for NMOS = 1 for PMOS] (OFF condition)		Operation	
	Input given at node X (V)	Output at node Y (V)	Input at node X (V)	Output at node Y (V)	Turn-on	Turn-off
N (MN5/MN6)	0.4	0.247	0.4	0.097	Proper	Degraded
P	0.4	0.400	0.4	0.350	Proper	Degraded
NP	0.4	0.400	0.4	0.400	Proper	Degraded
PP	0.4	0.400	0.4	0.361	Proper	Degraded
PN	0.4	0.400	0.4	0.000	Proper	Proper
NN	0.4	0.038	0.4	0.000	Degraded	Proper

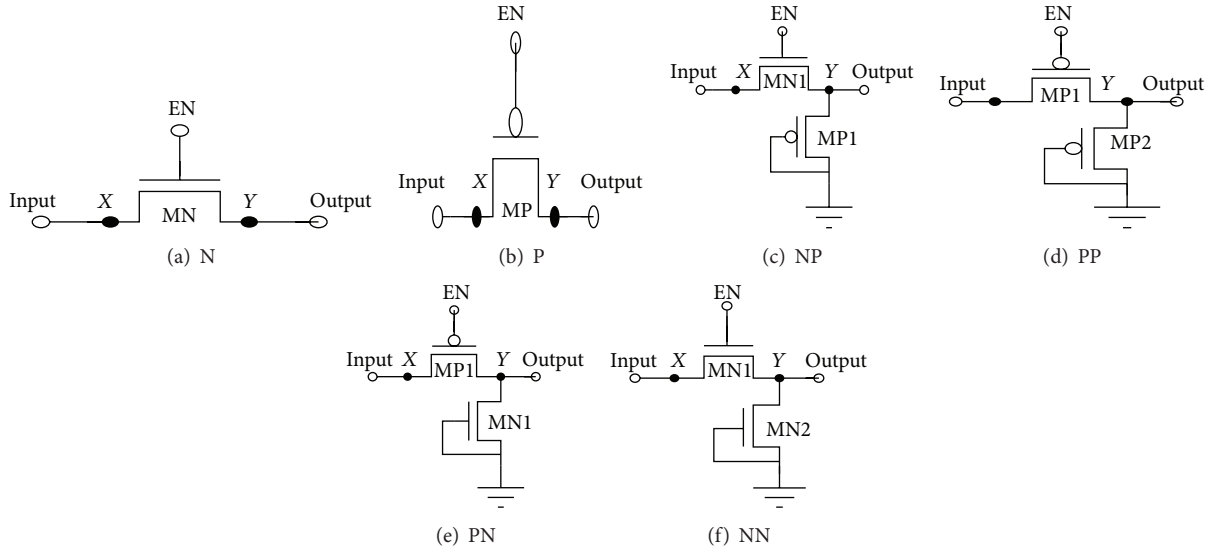

Figure 3: Schematics of access transistor.

change the stored information, that is, forcing node Q = "0" and QB = "1." For successful write operation, the node voltage Q should be reduced below the threshold voltage of MN1. For stable write and read operation, the aspect ratios of the transistors (MP4, MN2 and MP3, MN1) have to be computed accurately. The detailed analyses of read/write operation of MPT8T are given in the further section.

Due to high leakage current in OFF state at 45 nm technology node, NMOS/PMOS pass transistors do not turn off completely. Therefore, modification is required in Figure 2 for its proper operation. Figure 3 shows five different transistor/transistor combinations P, NP, PP, PN, and NN that can replace NMOS access transistor, that is, MN5/MN6, in Figure 2. Simulation results of these five combinations are given in Table 1.

Various combinations of N and P transistors have been explored. The simulation results given in Table 1 indicates that the NMOS (N) transistor does not turn off completely with a voltage of 0.111 V at its output which is high compared to 0 V. This is due to high subthreshold leakage current. This causes degradation in stability. The function of PMOS (P) transistor also has a turn-off problem and does not have 0 V at its output. So N has been modified by adding a transistor at its output which remains always off. The purpose of adding this additional transistor is to discharge the output node (Y) to 0 V.

NN combination has shown a turn-on problem as output remains in discharged stage always. In PN, transistors are carefully sized so that they are strong enough to allow data to be changed at the storage nodes during writing but weak enough not to flip the state of the cell during reading. The sizing of transistor is set as $(W/L)_{\mathrm{N}} = 10(W/L)_{\mathrm{P}}$ in PN combination with $L_{\mathrm{P,N}} = 50$ nm. The graph shown in Figure 4 shows the ON/OFF state analysis of access transistors. The plotted graph shows that PN combination performs perfect operation for both turn-on and turn-off state.

2.2. Current Analysis for Read and Write Operation. Figure 5 shows direction of the read and write current flow through the proposed MPT8T. At the start of a read operation, the bit-line pair (BL/BLB) is precharged to high voltage (V_{DD}) and then word-line (WL) is asserted, which enables MP3 and MP4. As a result, cell current or read current (I_{read}) begins to flow from BLB which goes in through MP3 to MP1 and flows out through MN2 to GND.

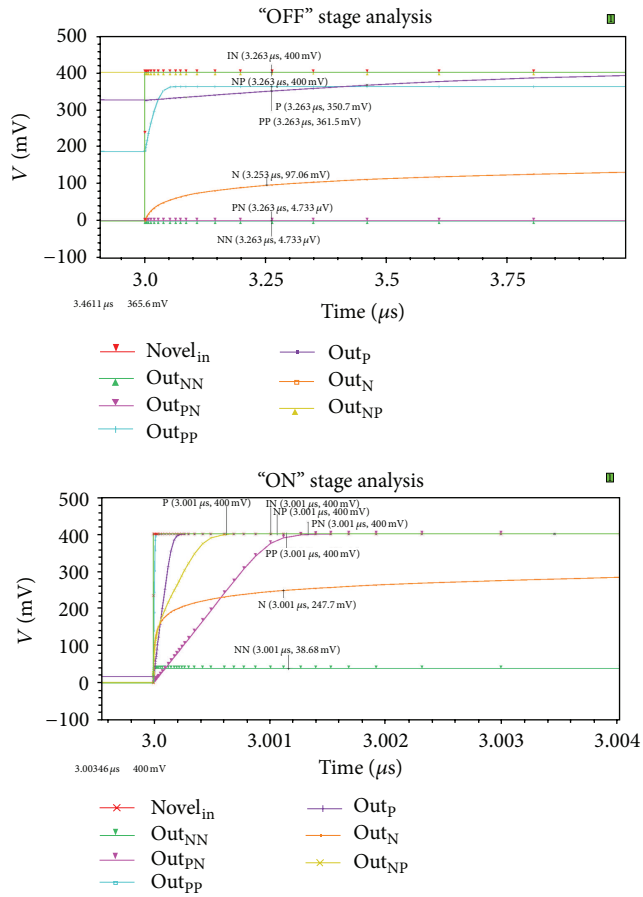

FIGURE 4: ON/OFF state analysis of access transistors.

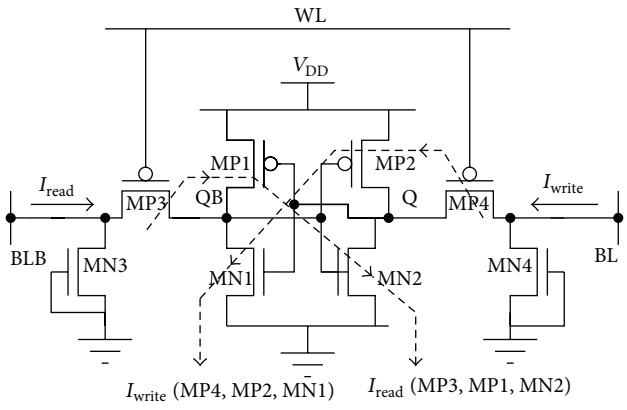

FIGURE 5: Read and write current flow through MPT8T.

I_{read} can be expressed analytically by solving Kirchhoff's current law at internal node "QB" storing "0":

$$I_{read} = \text{FUNCTION}\left(I_{MP3}, I_{MP1}, I_{MN2}\right), \quad (1)$$

where BLB and BL = "1" (ON state because of PMOS), WL = "0" (ON), QB = "0" (V_L), and Q = "1" (V_H),

$$\begin{aligned} I_{read} &= I_{MP3}\left(V_{GS} = V_{WL} - V_L,\ V_{DS} = V_{BLB} - V_L\right) \\ &\quad + I_{MP1}\left(V_{GS} = V_H - V_{DD},\ V_{DS} = V_L - V_{DD}\right) \\ &\quad - I_{MN2}\left(V_{GS} = V_L,\ V_{DS} = V_H\right). \end{aligned} \quad (2)$$

I_{read} is the sum of the currents through MP1 and MN1 while discharging precharged BLB (bit-line bar). The amount of read current flowing through the cell directly determines how fast the bit-lines can be discharged. The magnitude of the read current therefore significantly influences the maximum speed of the memory.

During write operation, one of the bit-lines is precharged to high voltage (V_{DD}) and the other is precharged to low voltage (GND). Thereafter, WL is asserted, which enables MP3 and MP4. As a result, write current (I_{write}) begins to flow from BL (V_{DD}) which goes in through MP4 to MP2 and flows out through MN1 to GND.

I_{write} can also be expressed analytically by solving Kirchhoff's current law at internal node "Q" storing "1":

$$I_{write} = \text{FUNCTION}\left(I_{MP4}, I_{MP2}, I_{MN1}\right), \quad (3)$$

Table 2: V_{DS} and V_{GS} values of each transistor at the end of read operation at voltage difference of 70 mV between BL and BLB.

Device	V_{DS}	V_{GS}
MP1	$V_L - V_{DD} = -339$ mV	$V_H - V_{DD} = 0$ mV
MP2	$V_H - V_{DD} = 0$ mV	$V_L - V_{DD} = -339$ mV
MP3	$V_{BLB} - V_L = V_{DD} - 70$ mV $- V_L = 269$ mV	$V_{WL} - V_L = 339$ mV
MP4	$V_{BL} - V_H = 0$ mV	$V_{WL} - V_H = 0$ mV
MN1	$V_L = 61$ mV	$V_H = 400$ mV
MN2	$V_H = 400$ mV	$V_L = 61$ mV
MN3	$V_{BLB} - V_{GND} = 330$ mV	$V_{GND} = 0$ mV
MN4	$V_{BL} - V_{GND} = 400$ mV	$V_{GND} = 0$ mV

where BLB = "0", BL = "1", WL = "0" (ON), QB = "0" (V_L), and Q = "1" (V_H),

$$I_{write} = I_{MP4}\left(V_{GS} = V_{WL} - V_H,\ V_{DS} = V_{BL} - V_H\right) + I_{MP2}\left(V_{GS} = V_L - V_{DD},\ V_{DS} = V_H - V_{DD}\right) - I_{MN1}\left(V_{GS} = V_H,\ V_{DS} = V_L\right). \quad (4)$$

I_{write} is the difference of current through MP2 and MP1 discharging the node "Q." Stronger pass gates and slightly weaker pull-up transistors are normally employed to ensure a robust write operation in the worst case process corner.

Read metrics such as read delay and I_{read} are estimated with the development of 70 mV difference between BL and BLB. For MPT8T, the operating mode, gate drives (VGS), and drain to source drives (VDS) are reported in Table 2.

3. Simulation Results and Discussion

This section presents comparative analysis of various design metrics like read stability, write-ability, hold stability, SINM, WTI, read and write access time, and leakage power dissipation of the proposed MPT8T and 6T cells. These design metrics are estimated with Monte Carlo simulation using 45 nm technology in subthreshold regime.

3.1. SRAM Standby Stability Analysis (Hold Stability). The primary concern metric in nanoscale SRAM design is stability which is analyzed by computing SNM in hold mode. This hold SNM metric, first defined by Seevinck et al. [19], measures the maximum serial dc voltage that can be applied to the internal nodes of the cell without flipping the state of the cell or minimum dc noise voltage required to flip the state of the cell. A higher SNM indicates better stability of the cell. Conceptual test circuits for measuring the hold SNM of MPT8T and conventional 6T are shown in Figures 6 and 7, respectively.

Under hold state, BL/BLB is precharged to high voltage (V_{DD}) and WL of the cell is biased at logic "0" (for 6T)/logic "1" (for MPT8T). This disconnects the cell nodes QB and Q from both bit-lines. Two equal dc voltage sources, VN1 and VN2, are placed between inverters indicating the dc noise sources. These two voltage sources are swept alternatively from 0 to V_{DD} to measure (low voltage) V_L and (high voltage) V_H, respectively. Then, voltage transfer curve (VTC)

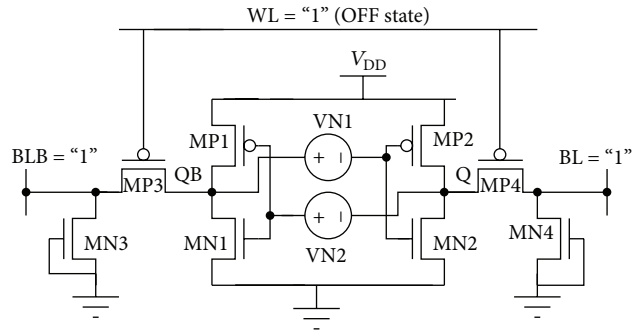

Figure 6: Test circuit for measurement of hold SNM of MPT8T.

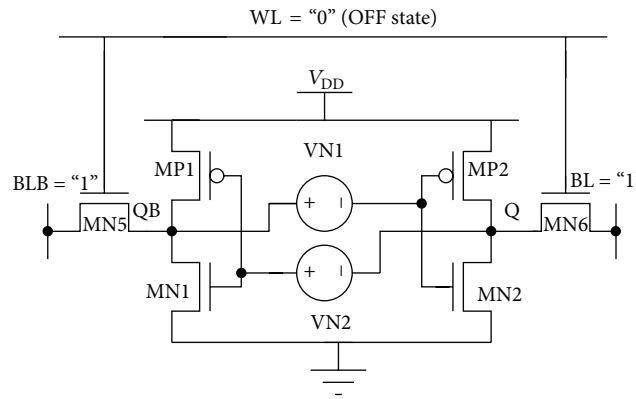

Figure 7: Test circuit for measurement of hold SNM of 6T.

of inverter (MP1/MN1) and the mirrored voltage transfer curve (VTC^{-1}) of inverter (MP2/MN2) are plotted on the same axis. The resultant curve is referred to as "butterfly curve." The side length of the largest square that can be embedded inside the lobes of the butterfly curve represents the hold SNM of the cell. Figure 8 shows "butterfly curve" of both 6T and MPT8T during hold operation. The two curves are merged into each other as expected since cross-coupled inverter pair designs are similar for both.

SNM of both designs is 160 mV at nominal supply voltage of $V_{DD} = 0.4$ V in 45 nm technology. It is observed that there are three intersection points of the hold state VTC (V_Q, V_{QB}) = (0.4, 0) V, (0, 0.4) V, and (0.23, 0.23) V. The stable states are corresponding to intersection points (0.4, 0) V and (0, 0.4) V, whereas the cell's state corresponding to (0.23, 0.23) V is

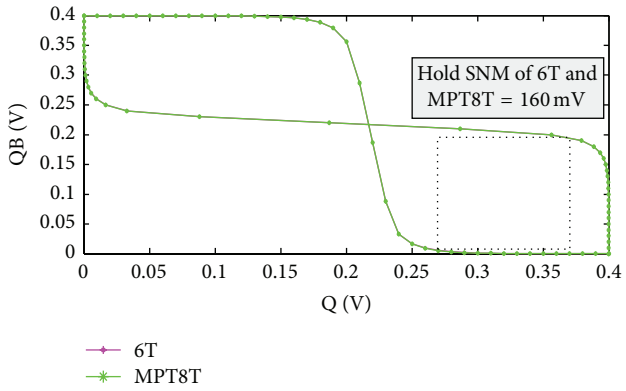

Figure 8: Hold SNM of MPT8T and 6T.

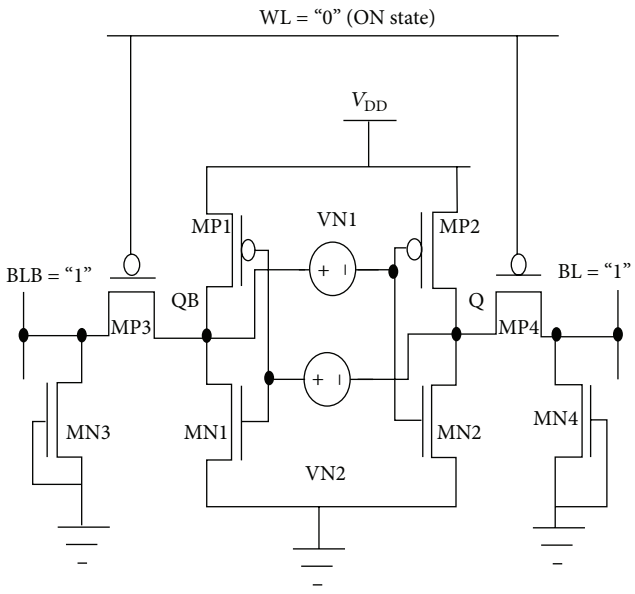

Figure 9: Test circuit for measurement of read SNM (RSNM) of MPT8T.

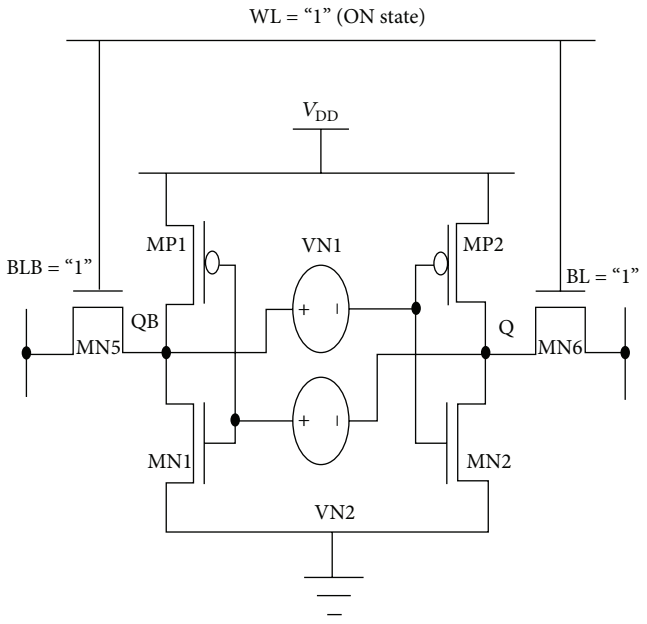

Figure 10: Test circuit for measurement of read SNM (RSNM) of 6T.

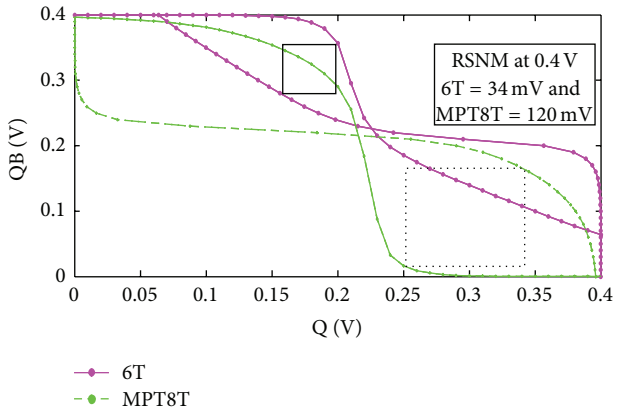

Figure 11: RSNM "butterfly curve" of MPT8T and 6T.

unstable. The SNM of both cells are equivalent (160 mV) indicating that both are equally stable in hold mode. Thus, the hold stability of the proposed cell remains untouched.

3.2. SRAM Read Stability Analysis. Read stability, analyzed by read SNM (RSNM), is an important design metric of SRAM cell. Measurements of RSNM are carried out in a similar fashion as done for hold SNM with BL/BLB precharged to V_{DD} and WL is biased in ON state with logic "1" (for 6T) and at logic "0" (for MPT8T) as shown in Figures 9 and 10.

From Figure 10, the size of MN2 and MN6 is represented as the cell ratio (CR) defined as CR = $\beta_{driver}/\beta_{access}$. For 6T, β_{driver} is $[W_{n2}/L_{n2}]$ of MN2 and $\beta_{access} = [W_{n6}/L_{n6}]$ of MN6, respectively, whereas from Figure 9 of MPT8T CR is defined as $[W_{n2}/L_{n2}/W_{p4}/L_{p4}]$. During read access, CR is critical for value of logic "0" at Q. Lower value of CR requires smaller noise voltage at Q to trip the cell, thereby compromising on speed and read stability. Higher values of CR provide higher I_{read} and improved stability at the cost of increased cell area. Figure 11 represents RSNM "butterfly curve" for both in subthreshold regime.

The MPT8T has 3.5x improvement in RSNM compared to the conventional 6T for CR = 1.5, (at V_{DD} = 0.4 V). Since the MPT8T consumes more area compared to the 6T, it is worthwhile to compare these cells under "isoarea" condition. For isoarea condition, the CR in the conventional 6T is increased so as to have the same area as that of the MPT8T. However, in subthreshold region, any CR increment will result in marginal change in the drain current due to exponential relation between drain current and gate voltage. Thus, RSNM of 6T with increased area show marginal change [20] as given in Figure 12.

Figure 13 shows the process variation impact on RSNM of MPT8T with ±10% variation in temperature and voltage at slow-slow (SS), fast-fast (FF), and typical-typical (TT) corners.

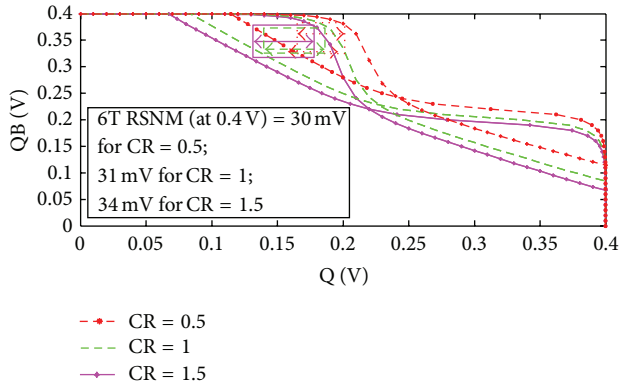

Figure 12: RSNM of 6T with varying CR.

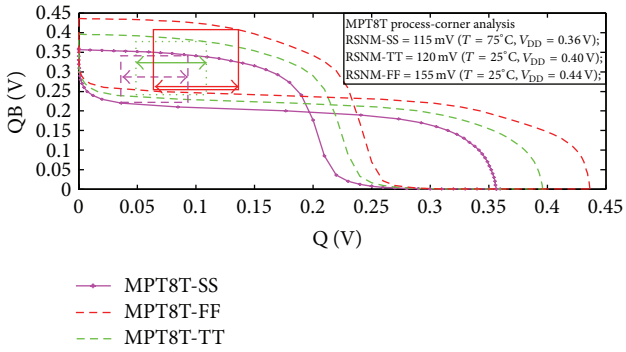

Figure 13: Process variations impact on RSNM of MPT8T.

3.3. SRAM Write Stability Analysis. Write stability, analyzed by write SNM (WSNM), is the minimum voltage necessary to drive the bit-cell into a monostable state during a write operation. Measurements of WSNM are carried out when one of the BL/BLB lines is precharged to high voltage (V_{DD}) and WL of the cell is biased at active mode, logic "1" (for 6T) and logic "0" (for MPT8T), as shown in Figures 14 and 15.

During write operation, the bit-line pair directly connects to the nodes Q and QB and forces the nodes Q and QB (the stored information) to obtain required voltage levels. On completion of change in state, WL signal is asserted low, and cross-coupled inverter pair stores the written 1-bit information. The write-ability of the cell depends on size of MN5 and MP1 and is represented as the pull-up ratio (PR) defined as PR = $\beta_{pullup}/\beta_{access}$. For 6T, β_{pullup} is $[W_{p1}/L_{p1}]$ of MP1 and $\beta_{access} = [W_{n5}/L_{n5}]$ of MN5, respectively, whereas, for MPT8T, PR is defined as $[W_{n1}/L_{n1}/W_{p3}/L_{p3}]$. A high value of PR is critical for storing logic "1" at Q to ensure a robust write operation in the worst case process corner. The write margin is the minimum bit-line voltage at which the cell flips its state [21]. Figure 16 represents combined read and write VTC curve for WSNM of MPT8T and 6T in 45 nm technology node in subthreshold regime.

As observed from Figure 16, there is only one intersection point of both the read VTC and write VTC curve. This indicates the single stable point which signifies the successful write operation and functionality of the cross-coupled inverters of the cell as monostable circuit. The MPT8T and 6T show 218 mV and 90 mV WSNM, respectively, giving 2.4x improvements. Figure 17 shows comparative SNM graph of MPT8T and 6T showing the superior hold, read, and write SNM of the MPT8T.

3.4. Alternative Noise Margins. An alternative noise margins method based on N-curve metrics (NCM) of the cell [22] is used for the evaluation of robustness of the SRAM cell. Figure 18 shows the test circuit for extracting NCM of MPT8T during read mode. Bit-line pair is precharged to V_{DD} and WL is precharged at logic "0" (ON state) for the NCM analysis [23]. An external voltage source (V_{in}) is applied at the input storage node "QB." V_{in} is swept from 0 V to V_{DD} and corresponding input current (I_{in}) produces the NCM characteristics as shown in Figure 19.

Basically, three common metrics known as static voltage noise margin (SVNM), SINM, and WTI are found in the NCM of the cell. The curve is analyzed at the three points (A, B, and C), where it crosses zero. Points A and C are the two stable points, while B is a metastable point. The voltage difference between A and B gives SVNM which indicates the maximum tolerable dc noise voltage at the internal node "QB." The analyzed results of NCM give 220 mV SVNM for both MPT8T and 6T.

The positive peak current between A and B indicates the stability of the cell, characterized as SINM which indicates the maximum injected dc current in the SRAM cell required to flip the content. The analyzed results of NCM give 12 μA and 10 μA of SINM for MPT8T and 6T, respectively.

The third metrics WTI is the amount of current needed to write the cell when both bit-lines are kept at V_{DD}. The negative current peak between points B and C gives WTI. Figure 19 shows −28 μA and −4 μA WTI for MPT8T and 6T, respectively. For better read and write stability of the design, it is preferable to have smaller value of WTI and larger value for SINM. The MPT8T bit-cell gives significant improvement in terms of SVNM, WTI, SINM, and WTV.

3.5. Read/Write Access Time and Leakage Power Dissipation. Write delay is the estimated time required to flip the cell contents at WL = "ON" during write operation. It is measured as the time required for writing "0" or "1" at Q/QB nodes, when WL reaches 50% of supply voltage (from its initial low level) to the point when Q/QB falls or rises to 10% or 90% of its maximum value. The write access time (T_{WA}) and read access time (T_{RA}) of 4 KB array of MPT8T are compared to similar array of 6T at power supply voltage varying from 0.3 V to 0.5 V and results are shown in Figures 20 and 21. The results show lower write and read delays of the MPT8T than 6T at all supply voltages.

The MPT8T offers 2.61x improvements in average T_{WA} at supply voltage ranging from 0.3 V to 0.5 V. Similarly, T_{RA} is measured from the point when WL reaches its 50% point from its initial low level to the point when 70 mV differential voltage is developed between BL and BLB from their initial precharged level.

The sense amplifier can easily detect the voltage differential of 70 mV between BL and BLB without generating any read error.

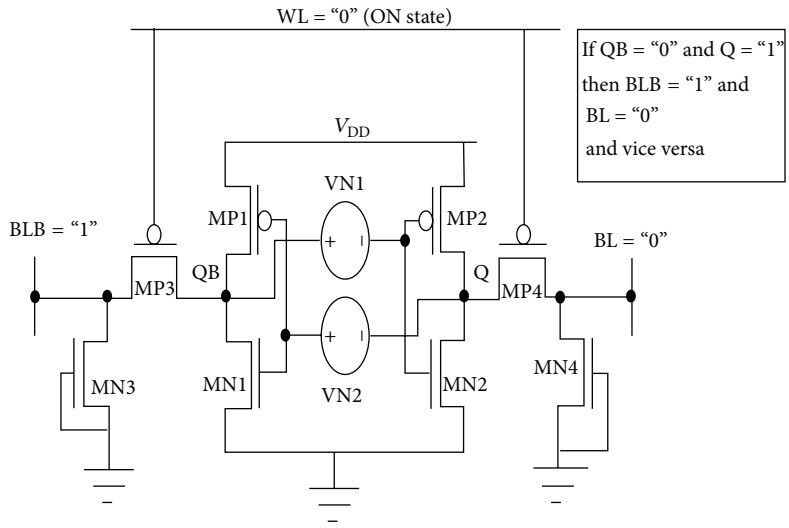

Figure 14: Test circuit for measurement of WSNM of MPT8T.

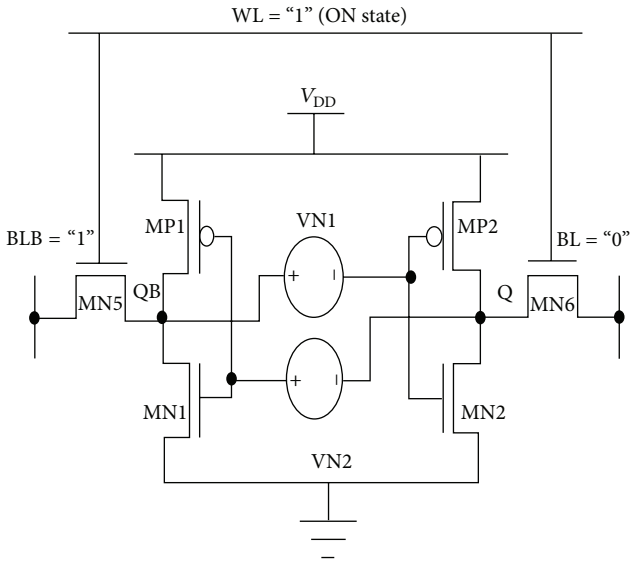

Figure 15: Test circuit for measurement of WSNM of 6T.

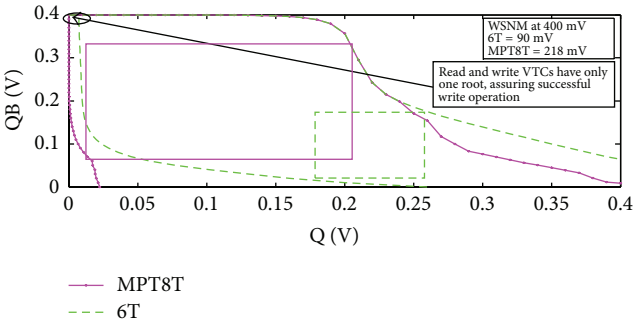

Figure 16: The combined read and write VTC curve for WSNM of MPT8T and 6T.

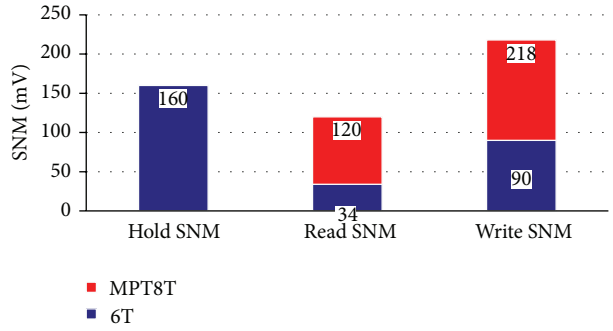

Figure 17: Comparative SNM graph of MPT8T and 6T.

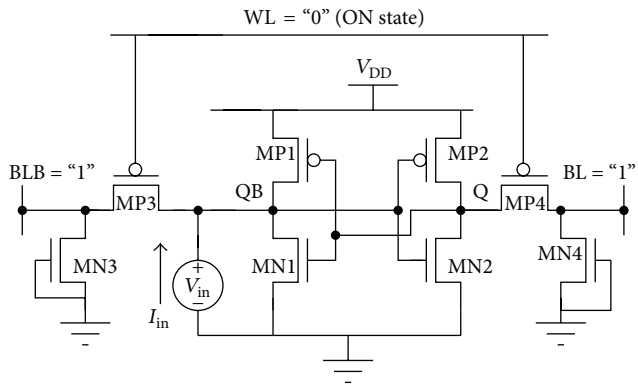

Figure 18: Test circuit for extracting N-curve of MPT8T during read mode.

Figure 21 shows that MPT8T offers marginal improvements in average T_{RA} at varying supply voltage from 0.3 V to 0.5 V. A comparison of average standby power at supply voltage varying from 0.3 V to 0.5 V is shown in Figure 22; the MPT8T achieves 7.735x narrower spread in average standby power as compared to 6T.

Table 3: Comparison of various SRAM cells at 45 nm technology.

References	Types of cell	SINM (μA)	WTI (μA)	SVNM (mV)	RSNM (mV)	WSNM (mV)	Standby power (nW)	Area (μm^2)	Comments
[11]	4T	—	—	—	—	—	7510.0	1.987	Not working
[12]	5T	—	—	—	—	—	1360.0	2.960	Not working
[13]	5T (2)	7	−28	200	80	129	2.04	3.011	Poor RSNM
[14]	6T (2)	6	−32	150	50	150	2.04	4.186	Poor SINM
[15]	6T	10	−4	210	34	90	5.77	3.824	Poor WTI
[16]	7T	11	−26	200	—	—	2.99	4.977	RSNM/WSNM not found
[17]	8T	6	−3	250	40	53	3770.0	6.279	Poor WTI
[18]	10T	6	−5.5	230	80	50	1682.0	7.989	Poor results
MPT8T	8T	12	−28	210	120	218	2.01	5.986	Best results among all expect area

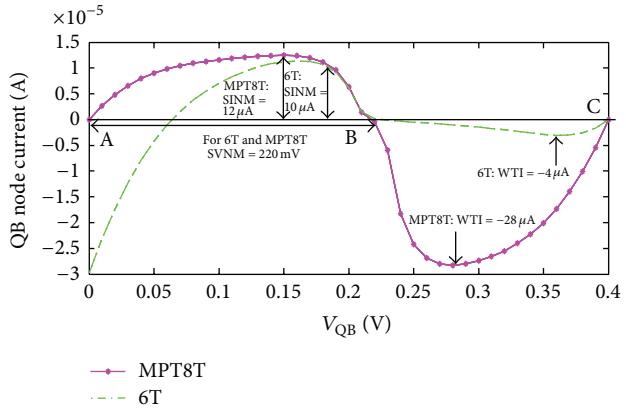

Figure 19: SINM, SVNM, and WTI versus internal node voltage.

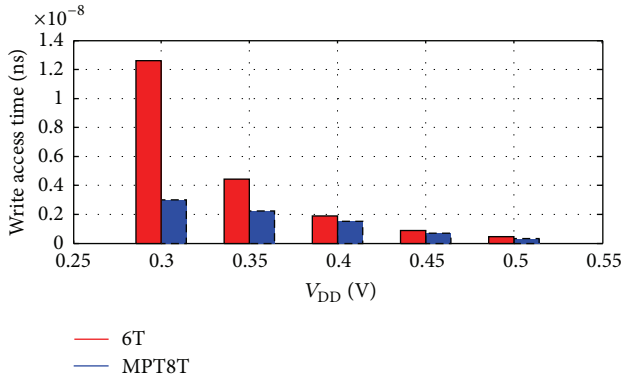

Figure 20: Write access time versus V_{DD}.

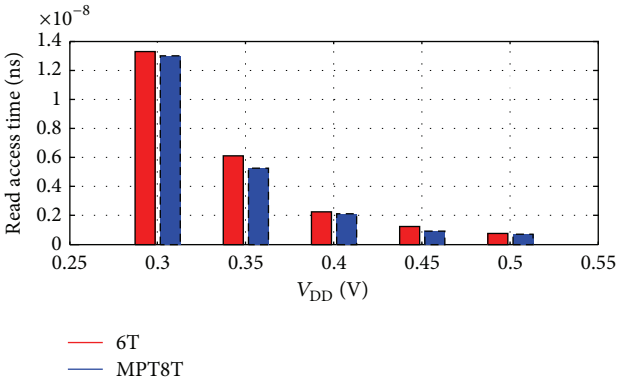

Figure 21: Read access time versus V_{DD}.

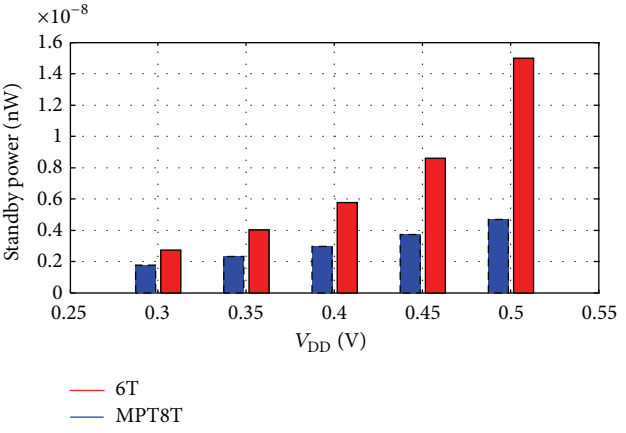

Figure 22: Leakage power versus V_{DD}.

4. Result Comparison of MPT8T and Referenced SRAM Cells

Table 3 gives comparison of stability parameters of MPT8T with the referenced SRAM cell. The schematics of the referenced cells are kept the same as given in original references. But the cells are redesigned at 45 nm CMOS technology for 0.4 V supply voltage to obtain their results for subthreshold operation in the same simulation setup as MPT8T. The comparative results show that the MPT8T cell has the best results among all.

5. Conclusions

Acute problem of variability is found in standard CMOS technology due to technology scaling driven by benefit of integration density, lower power dissipation, and overall power delay product. This work proposes functional MPT8T

SRAM cell at 45 nm technology with improved stability for subthreshold operation. The thorough analyses of stability, standby power, write access time, and read access time have been done. The MPT8T exhibits 3.5x *higher read SNM and* 2.4x *higher write SNM* indicating robustness of operation at 0.4 V power supply voltage with 7.735x lower standby power consumption over 6T. This is achieved without inserting an additional control line to switch the data into the MPT8T. The proposed design is an attractive choice for low power based application in scaled technology.

Conflict of Interests

The authors have no conflict of interests regarding the publication of this paper.

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