Hindawi Publishing Corporation
Journal of Nanotechnology
Volume 2013, Article ID 797964, 4 pages
http://dx.doi.org/10.1155/2013/797964

Research Article

Room-Temperature Hysteresis in a Hole-Based Quantum Dot Memory Structure

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Received 26 June 2013; Accepted 23 July 2013

Academic Editor: John A. Capobianco

We demonstrate a memory effect in self-assembled InAs/$Al_{0.9}Ga_{0.1}As$ quantum dots (QDs) near room temperature. The QD layer is embedded into a modulation-doped field-effect transistor (MODFET) which allows to charge and discharge the QDs and read out the logic state of the QDs. The hole storage times in the QDs decrease from seconds at 200 K down to milliseconds at room temperature.

1. Introduction

Today's semiconductor memory market is divided mainly between two memories: the dynamic random access memory (DRAM) and the flash, both having their advantages and disadvantages [1]. The DRAM is fast but volatile, while the flash is nonvolatile but suffers from a slow write time. The semiconductor memory community hence looks for alternatives to combine the advantages of both memories in what is termed the ultimate memory [2]. A promising option which could facilitate nonvolatility with fast write times is a memory based on self-organized quantum dots (QDs) [3]. The concept uses the confining properties of QDs to store data and a modulation-doped field-effect transistor (MODFET) to perform the necessary memory operations (write, erase, and read) [4, 5]. One key advantage is a wide variety of different materials when using III-V compound semiconductors, hence allowing to specifically tailor the band structure and tune the storage time according to the needs. The other key advantage is a very fast carrier capture time in QDs, which is in the range of some picoseconds at room temperature [6, 7]. Write times of a few nanoseconds in QDs have already been demonstrated, yet limited by the parasitics of the device [8]. Full memory operation has been demonstrated by various groups, yet the memory operation was either limited to low temperatures [9–11] or the storage of charges in the QDs was questioned and attributed to defects [12].

In this paper, we present a QD memory based on InAs QDs embedded into a MODFET ($GaAs/Al_{0.9}Ga_{0.1}As$) which can operate at much higher temperatures than hitherto. Hysteresis measurements prove a memory effect up to room temperature.

2. Sample

The sample investigated here has been grown by molecular beam epitaxy (MBE). A schematic of the structure is shown in Figure 1. On top of a semi-insulating substrate, a 1000-nm-wide buffer layer of nominally undoped $Al_{0.9}Ga_{0.1}As$ is grown. Then, a p-doped $Al_{0.9}Ga_{0.1}As$ layer with $p = 1 \cdot 10^{18}\ cm^{-3}$ and 30 nm width is deposited, which serves as a doping layer to provide holes for the channel. After a 7-nm-wide $Al_{0.9}Ga_{0.1}As$ spacer layer, an 8-nm-wide GaAs layer is grown to form the channel, in which a two-dimensional hole gas (2DHG) forms. Another 28 nm of undoped $Al_{0.9}Ga_{0.1}As$ forms a tunneling barrier, on top of which the layer of InAs QDs is grown, sandwiched between GaAs (to smooth the surface after the $Al_{0.9}Ga_{0.1}As$ growth and to cap the QDs). From uncapped samples with similar

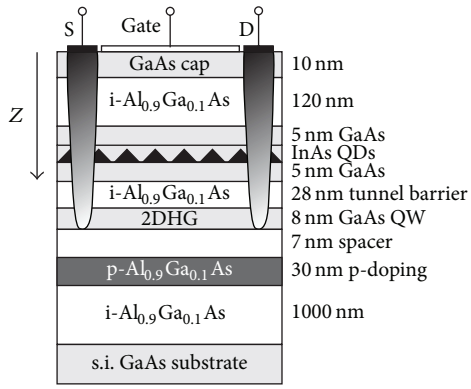

Figure 1: Schematic of the QD-based memory structure: A layer of QDs is embedded into a MODFET structure. The QDs and the 2DHG are separated by a 28-nm-wide tunnel barrier (consisting of 15 nm $Al_{0.9}Ga_{0.1}As$ and 8 nm GaAs).

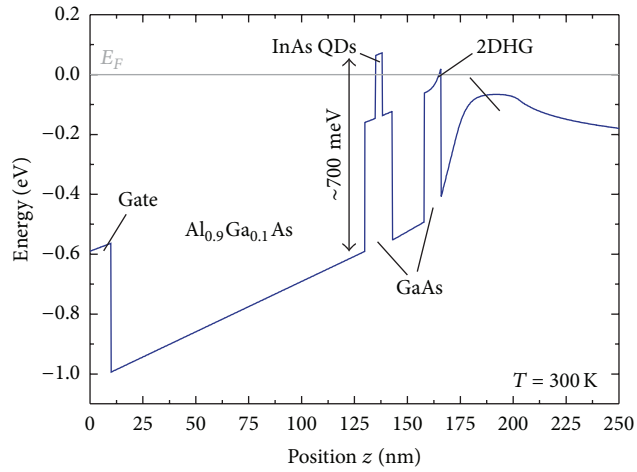

Figure 2: Valence band structure of the device. The InAs QDs inside the GaAs QW have a total localization energy of about 700 meV, which can be estimated from a previous work [13] and from the valence band offset between GaAs and $Al_{0.9}Ga_{0.1}As$ (500 meV) [14].

growth conditions, the QD area density is estimated to be $3 \cdot 10^{10}\,\mathrm{cm}^{-2}$. The structure is then completed with 120 nm undoped $Al_{0.9}Ga_{0.1}As$ and a 10-nm-wide GaAs capping layer in order to avoid surface oxidation of the AlGaAs.

The structure is processed into a device by using standard optical lithography and chemical wet etching techniques. The source and drain contacts are formed by Ni/Zn/Au and subsequent annealing for 3 min at 400°C, which lets the Zn diffuse into the AlGaAs layer down to the 2DHG. The gate contact ($740 \times 310\,\mu\mathrm{m}^2$) is a Schottky contact formed by using Ni/Au.

Figure 2 shows the valence band structure of the device at 300 K. The total localization energy of the QDs is estimated from a previous work [13] and the valence band offset between GaAs and $Al_{0.9}Ga_{0.1}As$ [14] to be ~700 meV. In equilibrium, the holes partly reside in the 2DHG channel and partly in the QDs. By applying a gate bias, the holes can be transferred from the channel to the QDs and vice versa.

Similar devices have already been successfully used in order to study many-particle ground states, being able to resolve the individual charging spectrum of the QD ensemble [15]. However, these devices had much narrower tunneling barriers, making operation possible at low temperatures only.

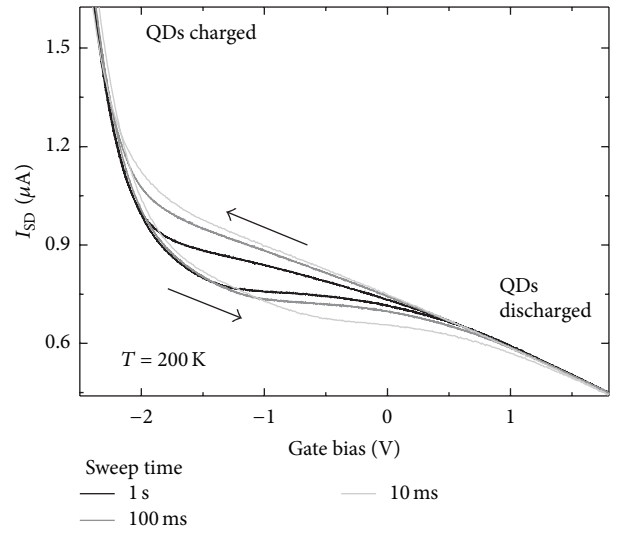

Figure 3: Source-drain current measurements for gate voltage sweeps with different sweep times at a temperature of 200 K. The curves show a clear hysteresis opening due to the memory effect of the QDs.

3. Results

Holes stored in the QDs (nonequilibrium situation) are reemitted with a certain probability. Neglecting optical effects, there are three mechanisms by which the holes can be reemitted: thermal emission, tunneling emission, and thermally-assisted tunneling emission [16–18]. The storage time in the QDs depends on the height and width of the barrier. For a specific device design, it can be altered either by changing the temperature or the gate bias (altering the band structure and hence the tunneling barrier). If the storage time in the QDs is larger than the operation that is performed on the gate, the memory effect in the QDs can be directly observed.

According to the simple Drude model, the conductance of a 2DHG depends on the mobility of the carriers and the charge density in the gas [19, 20]. If holes are present in the dots, both values change as the scattering probability is increased and the holes transferred to the dots are now missing in the 2DHG. Hence, the occupation of the QDs can be directly measured by a measurement of the current flowing through the 2DHG.

Figure 3 shows a measurement of the source-drain current I_{SD} (at $V_{SD} = 20\,\mathrm{mV}$) while simultaneously sweeping the gate bias between voltages of −2.5 V and 1.75 V with

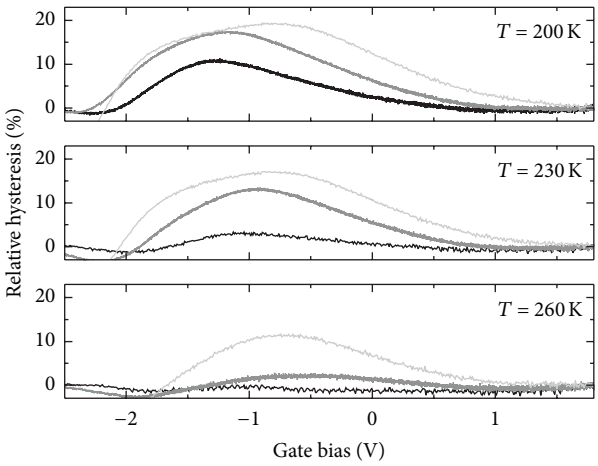

Figure 4: Relative hysteresis opening (with respect to the upper curve in Figure 3) for the three sweep times at different temperatures.

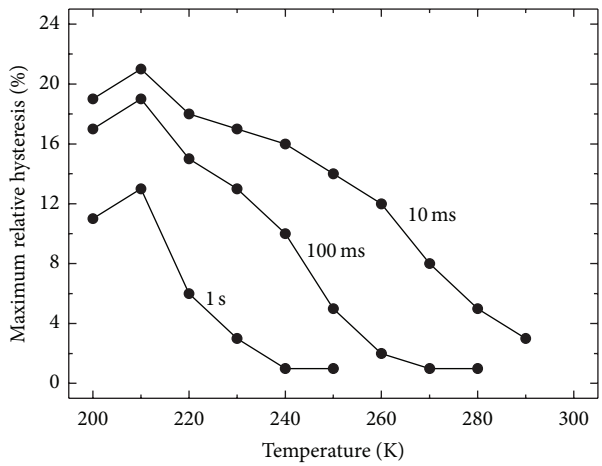

Figure 5: Relative hysteresis opening (with respect to the upper curve in Figure 3) as a function of temperature. A clear hysteresis can be seen up to a temperature of 290 K. The room temperature storage time of holes in the QDs can be estimated to be in the range of milliseconds.

sweep times between 10 ms and 1 s at a temperature of 200 K. Depending on the direction of the voltage change, the occupation in the QDs is changed, and a different current is measured. Coming from −2.5 V, the QDs are charged with holes, and the 2DHG is partly depleted, resulting in a lower current. In contrast, when coming from 1.8 V, the QDs are completely empty, the holes are now in the 2DHG, and hence a larger current is measured. The hysteresis opening is a measure for the number of holes that is present in the dots. Increasing the sweep time results in the partial emission of the holes, which decreases the number of holes stored in the dots and causes the hysteresis opening to close. From the sweep times used here, the storage time of holes in the QDs at 200 K can be estimated to be larger than 1 s.

When the temperature is increased, the available thermal energy increases, resulting in an increased thermal and thermally-assisted tunneling emission rate. This can be seen in Figure 4 where the hysteresis opening relative to the upper path of the hysteresis curve is shown versus the gate bias at three different temperatures. When the temperature is increased, the hysteresis opening decreases. Also, the maximum of the curve shifts with respect to the gate bias. This shift is due to a shift of the time constants of the emission processes for the individual hole levels of the QD ensemble. The maximum value appears at that position where the sweep time is comparable to the inverse emission rate. Hence, if the hole level with such a value changes, the bias voltage position is also changed.

The maximum values extracted from Figure 4 and larger temperatures are shown in Figure 5. An almost linear decrease of the relative hysteresis opening with temperature can be seen. At a temperature of 290 K, a hysteresis opening of ~3% can still be observed for a sweep time of 10 ms. Consequently, the storage time at 300 K can be estimated to be in the millisecond range. The storage time hence decreases from seconds at 200 K by about three orders of magnitude to milliseconds at room temperature.

4. Discussion

The results demonstrate a memory operation in QDs near room temperature with storage times in the millisecond range. However, storage times of 1.6 s in QDs have already been demonstrated in the same material system in simplified pn diode structures [13]. Assuming the same barrier height for the QDs in both samples, the deviation of about three orders of magnitude in storage time can be explained if the barrier width is taken into account. The storage time of 1.6 s was the result of an emission process limited by pure thermal emission, as thermally-assisted tunnel emission was not involved. In the work presented here, the storage time is not only limited by thermal emission, but suffers from thermally-assisted tunneling, as the tunnel barrier is about 5 nm narrower (15 nm $Al_{0.9}Ga_{0.1}As$ as compared to 20 nm in [13]). Hence, if thermal emission is to be the limiting emission process, the barrier width has to be at least 20 nm.

A further increase in the storage time of self-organized QDs can also be expected for other material systems, such as GaSb/GaP [21, 22].

5. Summary

We have demonstrated a memory effect in self-organized $InAs/Al_{0.9}Ga_{0.1}As$ QDs at temperatures near room temperature. The storage time decreases from seconds at 200 K down to milliseconds at room temperature. The storage of the holes in the QD ensemble is limited by a thermally-assisted tunneling process. A further increase of storage time can be expected for other material systems, such as GaSb/GaP.

Acknowledgments

The authors gratefully acknowledge financial support by the EC NanoSci-E+ Project QD2D (BI284/30-1), DFG Contract

No. BI284/29-1, and the BMBF Project HOFUS. The work of part of the authors was funded by the Deanship of Scientific Research (DSR), King Abdulaziz University, under Grant No. 2-4-1432/HiCi. These authors, therefore, acknowledge with thanks the DSR technical and financial support.

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