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Research Article

Fault Tolerant Ancillary Function of Power Converters in Distributed Generation Power System within a Microgrid Structure

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Distributed generation (DG) is deeply changing the existing distribution networks which become very sophisticated and complex incorporating both active and passive equipment. The simplification of their management can be obtained assuming a structure with small networks, namely, microgrids, reproducing, in a smaller scale, the structure of large networks including production, transmission, and distribution of the electrical energy. Power converters in distributed generation systems carry on some different ancillary functions as, for example, grid synchronization, islanding detection, fault ride through, and so on. In view of an optimal utilization of the generated electrical power, fault tolerant operation is to be considered as a suitable ancillary function for the next future. This paper presents a complete modeling of fault tolerant inverters able to simulate the main fault type occurrence and a control algorithm for fault tolerant converters suitable for microgrids. After the model description, formulated in terms of healthy device and leg binary variables, and the illustration of the fault tolerant control strategy, the paper shows how the control preserves power quality when the converter works in the linear range. The effectiveness of the proposed approach and control is shown through computer simulations and experimental results.

1. Introduction

The exponential penetration of distributed generation (DG) is leading to enormous changes in the conception of the electrical system management. Involved networks are no longer to be regarded as passive components but integrate a growing number of functions such as load management, demand side management, and generation curtailment.

Both standalone and grid connected microgrids, locally reproducing the structure of the whole generation and distribution system, may be a viable solution to enhance DG benefits, reducing at the same time the drawbacks of DG itself.

All the future hypothetical scenarios will lead to great transformations in the design of power systems, with interesting implications in different fields of research [1–5].

Some problems which arise immediately are the presence of bidirectional power flow, the need for a different design of the power lines and transformers, the unwanted islanding conditions, a different protection philosophy, and the possibility of a fault tolerant operation to increase the level of continuity.

This paper considers fault tolerant operation as a possible ancillary function. This additional function may be important in autonomous microgrid that cannot benefit from back up interventions of the traditional distribution network [6].

Since about a decade, the fault tolerant converters are the subject of research and development and their concept has now been extended to multilevel converters too because of their large number of devices and their redundancy making them suitable candidates for such an operation.

The present technical literature on the topic is abundant even not still exhaustive because the research fields are still up and many open questions are still waiting for significant answers [7, 8].

Among the various aspects, the most frequently discussed are control problems [8–13], fault diagnosis and protection [6, 7, 9, 14, 15], topologies, reconfiguration of circuits and

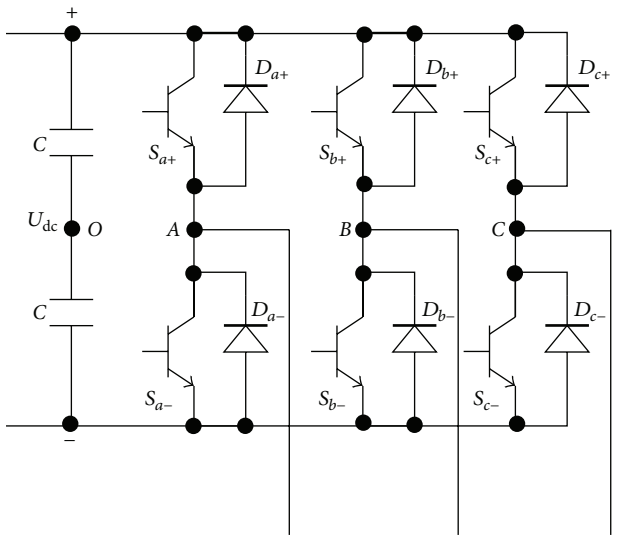

Figure 1: The VSI topology.

controls [4, 8, 13, 16, 17], and effect of fault tolerant operations on the main network [14, 18] and on the loads, with a special reference to evaluation of performance of AC electrical drives [7, 9–11].

This paper presents first a mathematical model able to represent both the behavior of a faulted converter and the fault tolerant operating mode. Subsequently a control strategy that can generate a substantially symmetrical three-phase output and the related implementation algorithm are examined. The fault tolerant operation is therefore considered in the context of a grid converter operation analyzing the system behavior and the operating limits of the same one in order to guarantee an acceptable level of power quality. In this scenario, some immediate indications on levels of transmitted power and performance deviations with respect to a classical grid converter are given. The validation of the control strategy and of the used algorithm is verified through simulations and experimental tests of a prototype built within the SDESLAB at the University of Palermo.

The next sections are organized as follows.

Section 2 deals with the general model of the inverter. Section 3 shows the simulation of the open-circuit fault. Section 4 illustrates the fault tolerant mode and the corresponding control algorithm and displays the simulation results. Section 5 deals with the specific case of a grid converter within a microgrid and outlines some considerations about the transmitted power and the current distortion and the need for a higher level of the DC Link voltage. Section 6 shows the experimental results obtained by tests on the realized prototype. Finally, Section 7 summarizes the conclusions.

2. The General Inverter Model

2.1. The General Model for Healthy Mode. For the general model of the Voltage Source Inverter in faulty and unfaulty, let us consider the circuit of Figure 1 presenting the general topology of a VSI.

The current circulation on free-wheeling diodes is also considered as also illustrated in the references [19–21].

For each controllable device, a switching function is defined in terms of gate pulse. For the jth upper device, it is, for example,

$$S_{j+} = \begin{cases} 1 & \text{if driving pulse is given,} \\ 0 & \text{otherwise } (\text{with } j = \{A, B, C\}). \end{cases} \tag{1}$$

A complementary switching function is defined for the lower device S_{j-}. The effective turning on of the device is conditioned by the current sign. In fact, an upper controllable device can effectively be turned on only if the load current is positive; conversely a lower device can be turned on only if the same current is negative. In general, current not being conducted by controlled devices is conducted by the free-wheeling diodes. Even if diodes are not controllable devices, switching functions may be defined for them also by taking into account the current sign. For example, an upper diode conducting the negative current is turned on only if the lower controllable device is off. In this way, the switching function for the upper diode is

$$D_{j+} = \overline{S_{j-}} \otimes \left(i_j < 0\right). \tag{2}$$

In a similar manner for the lower diode, it is

$$D_{j-} = \overline{S_{j+}} \otimes \left(i_j > 0\right). \tag{3}$$

By summarizing all the previous considerations, two generalized switching functions may be defined

$$\begin{aligned} \widehat{S}_{j+} &= \left[S_{j+} \otimes \left(i_j > 0\right)\right] \oplus \left[\overline{S_{j-}} \otimes \left(i_j < 0\right)\right], \\ \widehat{S}_{j-} &= \left[S_{j-} \otimes \left(i_j < 0\right)\right] \oplus \left[\overline{S_{j+}} \otimes \left(i_j > 0\right)\right]. \end{aligned} \tag{4}$$

Considering now the converter topology, output voltage with respect to the O point, as sketched in Figure 1, may be written as

$$v_{jO} = \left(\widehat{S}_{j+} - \widehat{S}_{j-}\right) \frac{u_{DC}}{2}; \quad j = \{A, B, C\}. \tag{5}$$

If the load impedances are balanced, the phase to neutral voltages have the well-known expressions

$$v_{jN} = v_{jO} - \frac{\sum_{k=j} v_{kO}}{3}; \quad j = \{A, B, C\}. \tag{6}$$

The load currents can be found from the equations

$$v_{jN} = Ri_j + L\frac{di_j}{dt} + e_{jN}. \tag{7}$$

For a complete inverter model, the equations describing the DC link circuit transient must be considered. In particular the expression of the DC link voltage is

$$C\frac{du_{DC}}{dt} = i_0 - \sum_{k=j} i_k \widehat{S}_{k^+} \tag{8}$$

and i_0 is given by

$$u - u_{\mathrm{DC}} = R_0 i_0 + L_0 \frac{di_0}{dt}. \tag{9}$$

Equations (4)–(9) constitute the model of a VSI in the healthy mode.

The Section 2.2 considers the modified converter model at faulty mode.

2.2. The General Model for the Faulty Mode. Recent studies have shown as up than the 80% of converter faults are due to single or multiple device failures [22].

Every power structure designer strives to remain well within the operating limits of the power device as specified by the IGBT manufacturer. However, there are component failures either of the power switching device or of supporting components that result in one or more IGBT power device failures. When the IGBT power devices fail, under certain circumstances, the failure can result in the rupture of the power module and extensive damage to the surrounding power components [23].

Typically failures are manifest as counterblow destruction, as in the case of short circuit of silicon packed devices, or by losing driver pulse occurring if driver circuit or its power supply are invalid so that no trigger pulse is sent to the gate [8]. Open-circuit faults generally do not cause shutdown of the system but degrade its performance [10, 21].

Some of the gate drive failure can result from breaking of passive components (resistors and capacity) or from a drift of their values for which the behavior of the driver does not meet the original specifications. With regard to short circuits or defects caused by overcurrent, a crucial parameter is the passing through energy I^2t that, during time, causes a degradation of the materials employed in the construction of the components.

Short circuit faults have a very fast evolution and, in general, no software algorithm is able to detect them in the short time required to interrupt and insulate the faulted zone from the rest of the system. For this reason, they are generally managed directly with hardware additional device or circuits and interrupted with ultrafast fuses, taking care that these last ones should not introduce any additional inductances in the main circuit.

Short circuits and ruptures that do not imply any further damage to the remaining part of the power circuit evolve to an open circuit condition. For this reason only open circuit faults are considered here.

Multiple device faults are less frequent but may be also significant if the inverter leg is an integrated packaged one. However, the presented model will also consider the case of multiple devices damage. Furthermore, thanks to the followed approach, in all the examined cases, an inverter reconfiguration for the fault tolerant mode can be simulated.

In this section, the single device faults for drive failure and also for diode breakdown are considered.

If a controllable upper device goes to a drive failure condition, in this case, the S_{j+} switching function is always zero. A positive current cannot be conducted by any device of the faulted phase. The negative current may instead circulate in the upper diode and in the lower controlled device. Starting from diode conduction if the lower device is turned off, a commutation phenomenon appears, then the diode current turns to zero while the transistor current rises up. In this case, the general switching function becomes

$$\begin{aligned} \widehat{S}_{j+} &= \left[\overline{S_{j-}} \otimes \left(i_j < 0\right)\right], \\ \widehat{S}_{j-} &= \left[S_{j-} \otimes \left(i_j < 0\right)\right]. \end{aligned} \tag{10}$$

In particular $\widehat{S}_{j+}$ considers only the upper diode conduction while $\widehat{S}_{j-}$ denotes the lower transistor conduction. Similar consideration applies when the faulted device is the lower. In fact, in this case, the general switching functions become

$$\begin{aligned} \widehat{S}_{j+} &= \left[S_{j+} \otimes \left(i_j > 0\right)\right], \\ \widehat{S}_{j-} &= \left[\overline{S_{j+}} \otimes \left(i_j > 0\right)\right]. \end{aligned} \tag{11}$$

For the general case, the introduction of a *healthy device binary variable (HDBV)* is useful. It is defined as follows:

$$h_{j\pm} = \begin{cases} 1 & \text{if the upper } (+) \text{ /lower } (-) \text{ device is healthy,} \\ 0 & \text{otherwise.} \end{cases} \tag{12}$$

The introduction HDBVs makes the definition of the generalized (i.e., in faulty and unfaulty mode) switching function very simple. In fact

$$\begin{aligned} \widehat{S}_{j+} &= \left[h_{j+} S_{j+} \otimes \left(i_j > 0\right)\right] \oplus \left[h_{j-} \overline{S_{j-}} \otimes \left(i_j < 0\right)\right], \\ \widehat{S}_{j-} &= \left[h_{j-} S_{j-} \otimes \left(i_j < 0\right)\right] \oplus \left[h_{j+} \overline{S_{j+}} \otimes \left(i_j > 0\right)\right], \end{aligned} \tag{13}$$

that is, in a general simulation scheme, the fault behavior is modeled simply with the product of $S_{j\pm}$ by $h_{j\pm}$.

The same principle applies when both the transistor and the diode are broken, but the first expression of (10) now contains two incompatible conditions. However, to get a correct simulation result, the signal of (10) may be used to reset the integrators of (7). In other words, when the lower power device is turned off, the load current is forced to zero.

The loss of entire converter leg does not introduce any difference because the approach with healthy device binary variable also allows an easy and affordable modeling in inverter reconfiguration for the management of the converter in fault-tolerant mode. With this aim, the healthy leg binary variables (HLBV) are then introduced as follows:

$$h_j = h_{j+} \oplus h_{j-}. \tag{14}$$

In reconfiguration, after the fault diagnosis, the faulted leg is disabled and the load terminal of the faulted phase is connected to the middle point of the DC link allowing the current circulation by means of bidirectional switches. The reconfigured inverter assumes the topology of a B4 circuit (see Figure 2).

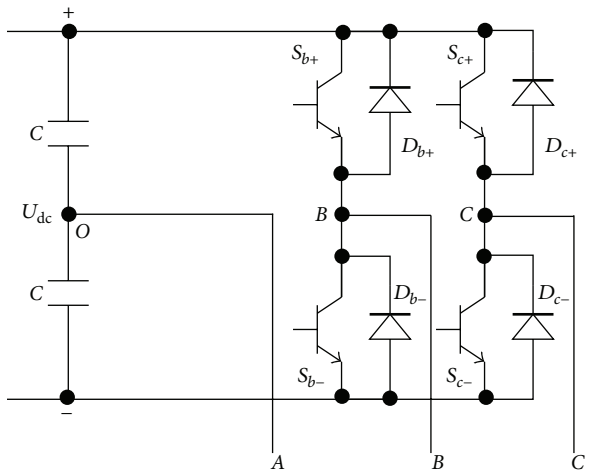

FIGURE 2: The reconfigured inverter after the fault (B4 topology).

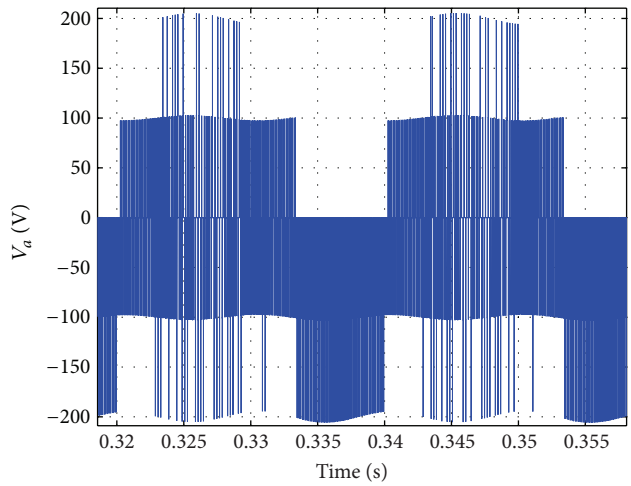

FIGURE 3: Voltage on load faulted phase for upper device drive failure.

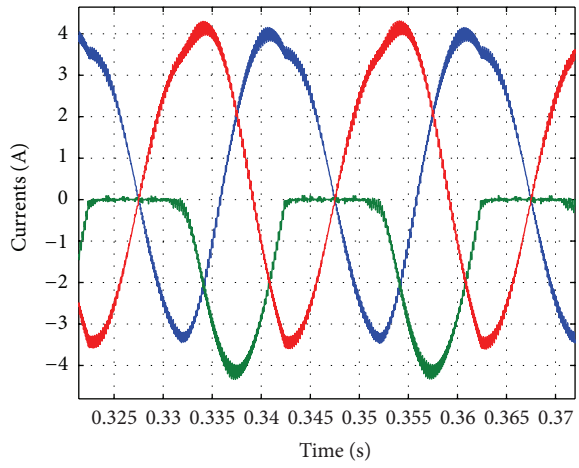

FIGURE 4: Currents on the load after fault.

In previous papers of the authors [14, 18, 21, 24–27], this reconfiguration has been extensively investigated and the general model of the reconfigured inverter has been also presented. This model will consist of the following equations:

$$U_1 = \frac{1}{C}\int_0^t \left(i_0 - \widehat{\mathbf{S}}_{\mathbf{k}}^{\mathbf{t}}\mathbf{H}_{\mathbf{k}}\mathbf{i}_{\mathbf{k}}\right) dt,$$
$$U_2 = \frac{1}{C}\int_0^t \left(i_0 - \left[\widehat{\mathbf{S}}_k^t\mathbf{H}_k - \mathbf{1}^t\mathbf{H}_k\right]\mathbf{i}_{\mathbf{k}}\right) dt, \quad (15)$$

for the partial DC link voltages with

$$\mathbf{H}_k = \begin{pmatrix} h_A & 0 & 0 \\ 0 & h_B & 0 \\ 0 & 0 & h_C \end{pmatrix}, \quad (16)$$

$$\mathbf{v}_{kN} = U_{\mathrm{DC}}\mathbf{T}\mathbf{H}_k\widehat{\mathbf{S}}_k - \mathbf{T}\mathbf{H}_k\mathbf{1}U_2,$$

for the inverter output voltages with

$$\mathbf{T} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}. \quad (17)$$

The load (grid) equations remain unchanged.

3. Simulation of the Faults

Simulations of faults are made with the help of the previous model whose equations are implemented thanks to the Matlab-Simulink software package. In the simulation, a VSI with a 300 V DC link voltage is hypothesized. Simulation results are illustrated in the figures below.

Figure 3 shows the output voltage on the faulted phase when a driver failure for an upper device appears, while Figure 4 shows the currents on the load after fault.

Simulations show clearly the positive current interruption and the negative current which flows through the diode.

During the current interruption, the average value of the phase voltage is zero (the instantaneous value is only made up of a series of voltage spikes). Other currents on unfaulty phases become phase opposite while the applied voltages on it are half of the line to line voltage with a different sign.

Figure 5 shows, instead, the voltage on an unfaulted phase.

Figures 6 and 7 show, respectively, the same simulation results when the fault regards both the device and the free-wheeling diode.

Voltage is very similar to that of the previous analyzed case except for a higher number of spikes. Currents are instead quite different being composed of a series of negative pulse due to commutation of the lower transistor. The unfaulted phase voltages are very similar to the previous ones and, for this reason, are not reported here.

4. The Control Strategy for the Fault Tolerant Operation

4.1. The Fault Tolerant Control Arrangement. In the case of loss of an entire leg, the only reconnection of the faulted

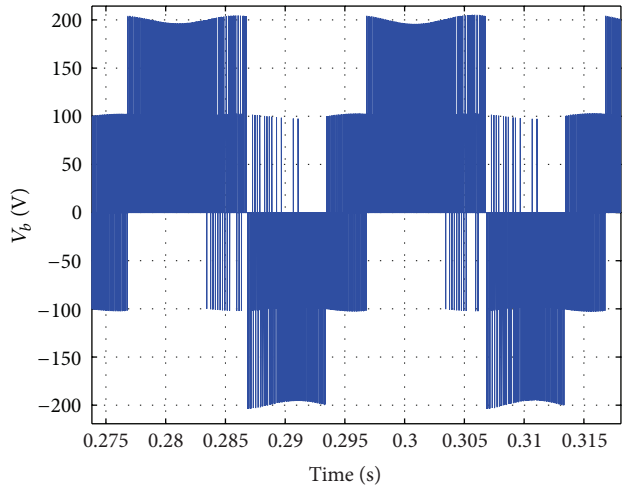

FIGURE 5: Voltage on an unfaulted phase.

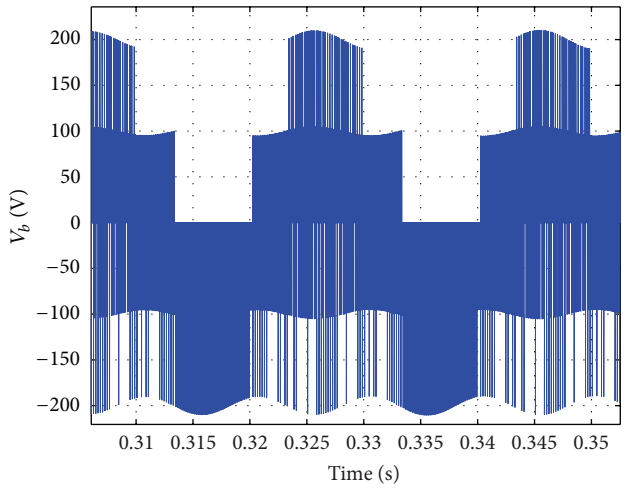

FIGURE 6: Faulty phase voltage after transistor and diode have broken.

TABLE 1: Synthesis of the postfault reference voltages.

Healthy U_{ref}	Phase A fault	Phase B fault	Phase C fault
u_A	0	$-u_C$	u_B
u_B	u_C	0	$-u_A$
u_C	$-u_B$	u_A	0

phase to DC link middle point does not ensure a correct operation. In particular, the current peak amplitude of the faulted phase results lowers by a factor $\sqrt{3}$. In order to obtain a balanced currents system, the voltage references used in the modulation process must be changed.

In the case of a grid converter, its capability to maintain a set of symmetrical voltages is very important for the power quality in view to limit as possible disturbances propagation into the grid avoiding oversized apparatuses to their mitigation.

The new modified set of reference voltages in the fault-tolerant mode should then present a minimal inverse component.

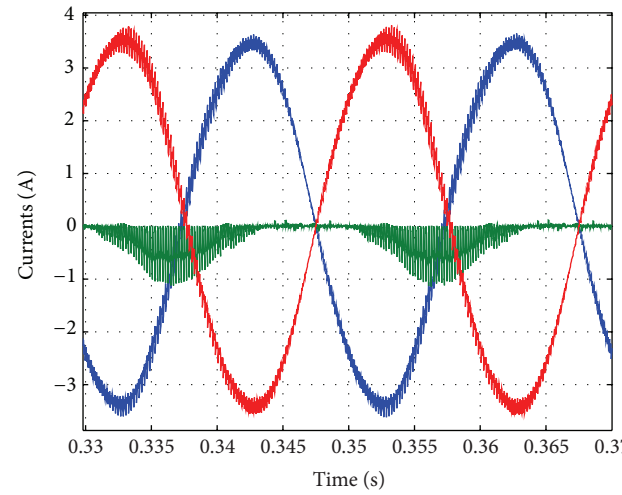

FIGURE 7: Load currents after broken transistor and diode.

The new reference voltages consist of a set of two sinusoidal signals controlling the healthy legs.

Suppose now that the signals corresponding phasors are

$$U_{\text{ref1}} = U_x \exp(j0),$$
$$U_{\text{ref2}} = U_x \exp(-j\varphi). \tag{18}$$

For the fault cases, on phases A, B, and C, respectively, the inverse component of this reference system is

$$U_{\text{inv}A} = 0 + \alpha U_{\text{ref1}} + \alpha^2 U_{\text{ref2}},$$
$$U_{\text{inv}B} = U_{\text{ref1}} + \alpha 0 + \alpha^2 U_{\text{ref2}}, \tag{19}$$
$$U_{\text{inv}C} = U_{\text{ref1}} + \alpha U_{\text{ref2}} + \alpha^2 0.$$

By calculating the module of the inverse components, it follows that

$$|U_{\text{inv}}| = \sqrt{2} U_x \sqrt{1 + \cos\left(\varphi \pm \frac{2\pi}{3}\right)}, \tag{20}$$

in which the sign "+" is for a fault on phase A and C while the sign "−" is for a fault on phase B. In both cases, the minimum inverse factor is reached for $\varphi \pm 2\pi/3 = \pi$, that is, for $\varphi = \pm\pi/3$ and it results just $|U_{\text{inv}}| = 0$.

Hence, in a fault tolerant converter, the new references have equal amplitude and a 60-degree phase displacement.

Furthermore, the new references can be built following the suggestion of Table 1.

Therefore, the general expression of the reference voltages (u_k^* with $k = A, B, C$) for healthy and faulted conditions is

$$u_A^* = u_A h_A h_B h_C + \sqrt{3}\left(\underline{h_C} u_B - \underline{h_B} u_C\right),$$
$$u_B^* = u_B h_A h_B h_C + \sqrt{3}\left(\underline{h_A} u_C - \underline{h_C} u_A\right), \tag{21}$$
$$u_C^* = u_C h_A h_B h_C + \sqrt{3}\left(\underline{h_B} u_A - \underline{h_A} u_B\right),$$

where u_j is the set of normal symmetrical three-phase reference voltages.

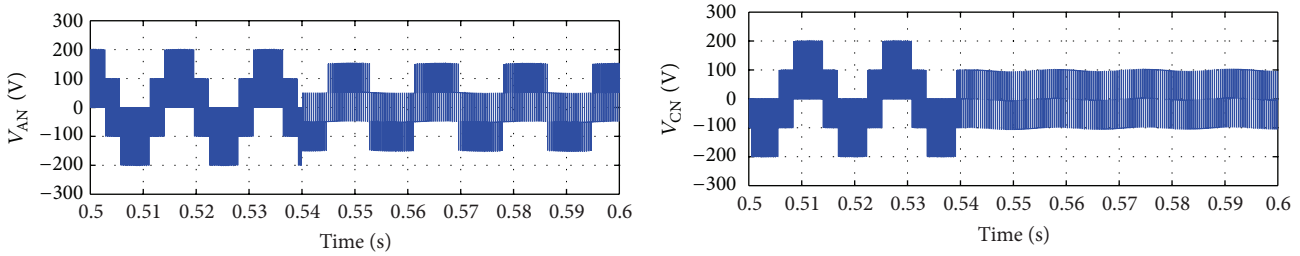

Figure 8: Phase voltages at unfaulted and faulted converter leg.

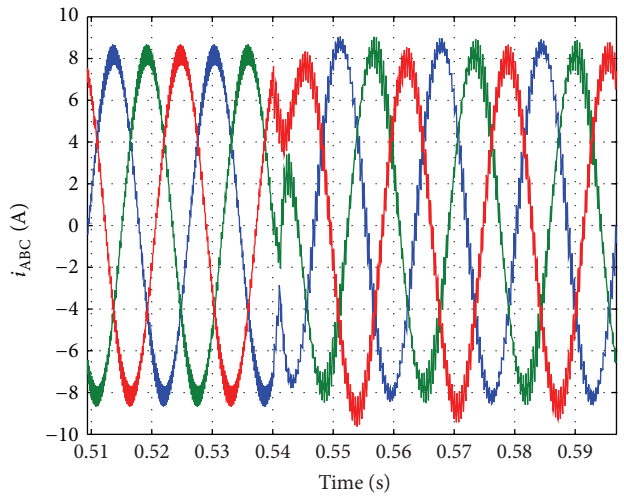

Figure 9: Load current before and after faults.

Equation (21) may be also written in vector notation

$$\mathbf{u}^* = \lambda \mathbf{u} + \sqrt{3}\mathbf{u} \times \underline{\mathbf{h}}, \tag{22}$$

where $\lambda = h_A h_B h_C = \det(\mathbf{H}_k)$.

The modified reference voltage are very simple to be implemented on microprocessors and diagnostic signals on the converters can be used to synthesize the new postfault reference voltages.

In (21), the general term $\lambda\mathbf{u}$ is the reference for the healthy case while the vectors cross product $\sqrt{3}(\mathbf{u} \times \underline{\mathbf{h}})$ is the new reference in the faulted case. The factor $\sqrt{3}$ guarantees the identity of the voltage and current amplitude, even after the fault has occurred.

Note that the cross product term $\sqrt{3}(\mathbf{u} \times \underline{\mathbf{h}})$ should be $\pi/2$ clockwise rotated if the converter is a grid connected, thus maintaining the synchronization between converter and grid voltages. In this case, the reference voltages system, expressed in vector form, results

$$\mathbf{u}^* = \lambda \mathbf{u} + \sqrt{3}\left(\mathbf{u} \times \underline{\mathbf{h}}\right) e^{-j(\pi/2)}. \tag{23}$$

The first advantage of (23) is a close integration of the diagnostic signals directly in the control for the inverter reconfiguration, another advantage is to make the fault and reconfiguration transparent to the main control system. In fact, any regulating action of external variables can provide a three-phase voltage reference that will be then manipulated according to (23) in order to generate the correct reference. In other words, the only reason for which the control system can be affected by the fault is the unavoidable DC link voltage ripple (as discussed later) and its effect on the current.

4.2. The Control Simulation. Control simulation results are illustrated in the following figures showing how the fault condition is managed by the model with the modified control strategy in order to guarantee the minimal derating in power quality.

Figure 8 shows the converter phase voltage measured at unfaulted (a) and faulted leg (b) after the faults occurred, resulting their first harmonics a symmetrical system even after the fault.

The voltage waveforms are quite different from those with unfaulted converter condition and the faulted leg voltage exhibits the greatest difference.

Figure 9 shows converter currents before and after fault occurrence with the instantaneous modification of the converter references. The residual current imbalance after fault is due to the alternating components in the DC-link voltage depending on the current amplitude and on the output frequency. In general, the voltage oscillation in single DC capacitors does not affect significantly the entire value of the DC link voltage and the general converter performance.

Postfault currents exhibit a phase jump due to reconfiguration unless this is compensated. Figure 10 shows instead the effect on load currents with the phase jump correction introduced in (23).

The linear region of the converter during the fault is, in each case, restricted. Linear range is quite important in order to achieve minimal currents asymmetry.

Figure 11 shows a higher load current distortion and unbalance during overmodulation (i.e., with an amplitude modulation index higher than 0.5, in the faulted case).

Figure 12 shows the voltage imbalance on the two DC link capacitors.

5. Simulation of a Grid Converter with Fault Tolerant Operation

The illustrated simulation was made for a standalone converter. In the case of a grid converter fed by a DG source,

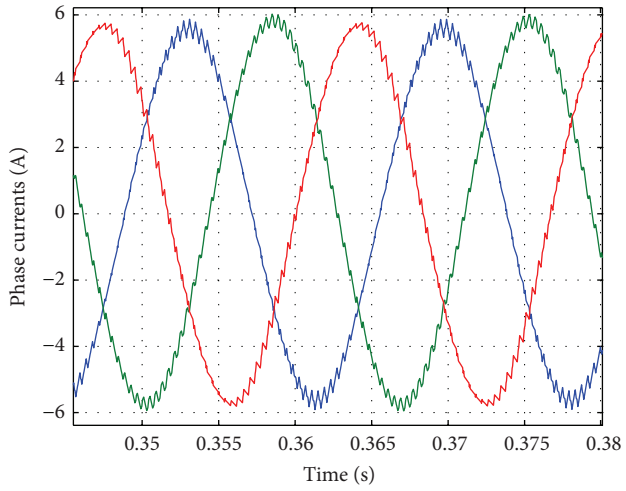

Figure 10: Load currents before and after fault with phase jump correction.

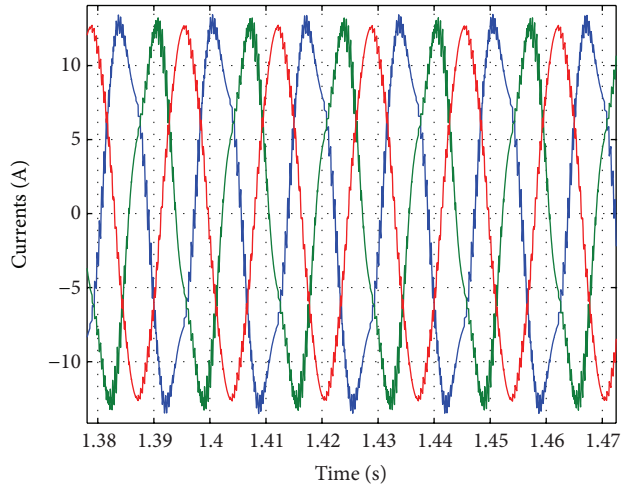

Figure 11: Distorted and unbalanced load currents with higher distortion during faulted condition in overmodulation mode.

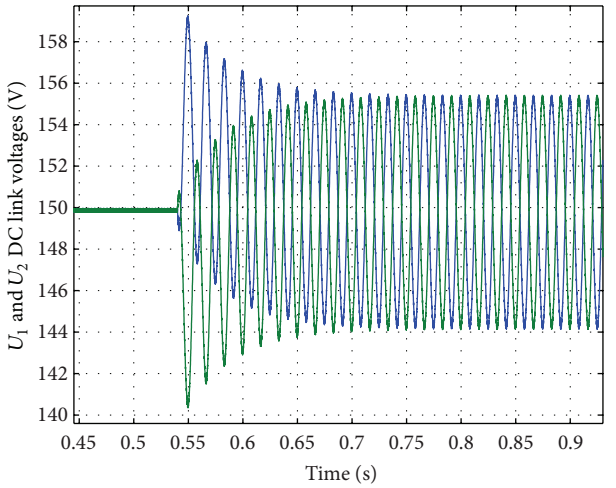

Figure 12: Voltage unbalance through DC link ca pacitors.

the system and the control are more complicated. However, no modification of the classical control structure of a grid converter is needed. Figure 13 shows the simplified scheme of the control structure for a grid converter control in which active and reactive power are managed via current control loop and DC link voltage loop. A complete description of the grid converter control system and of some other different solutions is given in [28, 29].

The control scheme allows active P and reactive power Q to be managed separately by decoupling DQ channels for the current control, so that P depends on i_D and Q depends on i_Q via previous proper grid synchronization via PLL. The DC link voltage control is also performed.

In the example of this section, the grid filter is not optimally designed with the aim to put better in evidence some aspect of the fault tolerant grid converter behavior.

The simulation assumes the occurrence of a fault, the fast reconfiguration of the converter, and the decrease of the active power injected into the grid. Subsequently the reactive power transferred to the grid is vanished. It is evident that despite the active power decrease, there is a greater distortion of the output current, as it is seen in Figures 14 and 15 (also with reference to the i_D and i_Q components) due to the increased voltage ripple on the DC link. This oscillation is natural and the control system can only fix its mean value forced by the set point. The simulation shows well as vanishing the delivered reactive power, the DC link voltage oscillation decreases with benefit for both the input and the grid current that exhibit a lower distortion as evident from Figures 16, 17, 18, 19, and 20.

It is worthwhile to remark that for avoiding overmodulation, the fault tolerant converter has a DC link voltage 25–30% greater than that of a traditional grid converter.

6. Experimental Results

Experimental results were made available in the case of the fault tolerant mode where the reconfiguration makes the converter operation more safe for a normal laboratory test. It was not possible to test the converter as a grid-converter one, so the tests on the fault tolerant operation have been made by feeding an induction motor and registering output voltages and currents.

For the experimental test, a customary benchmark based on an INFRANOR power converter and a dSPACE control board has been built and set up.

The converter used in the test bench is a commercial frequency converter whose control board has been replaced by a customary one designed to be driven by the dSPACE control board and converting the TTL gating pulses to the "line drive" type of the INFRANOR converter (see Figure 21).

In the practical realization of a fault tolerant converter, some issues are mandatory to be taken into account: Triacs for the current path closure may suffer for a dv/dt not sufficient immunity, having, therefore, unwanted switchings. A solution to this problem can be the choice of a different bidirectional controllable switch. In particular, the combination of power diodes in a bridge configuration with an auxiliary

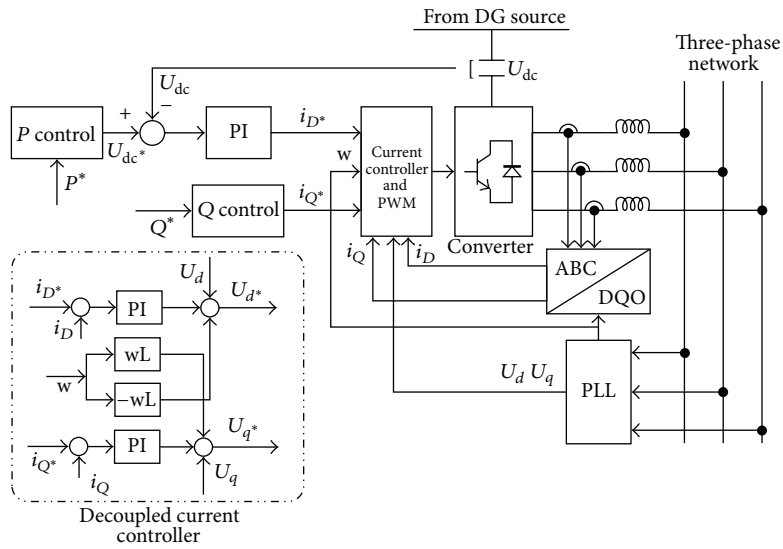

Figure 13: The control structure of a grid converter.

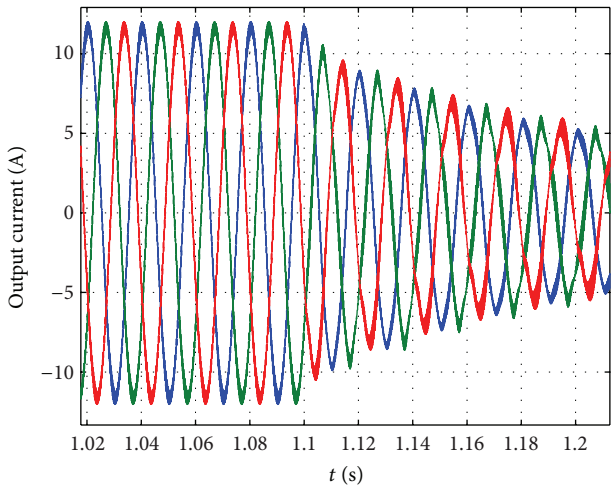

Figure 14: Current decrease after fault and reconfiguration.

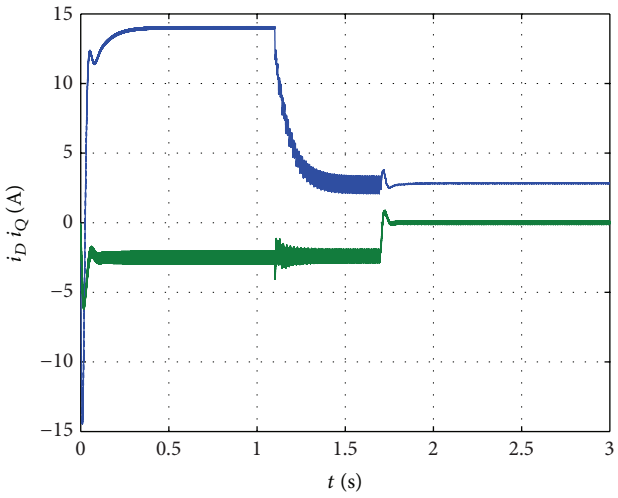

Figure 15: i_D (blue) and i_Q (green) current components.

IGBT is able to reach bidirectional current circulation (see Figure 22 for topology details). A fault detection algorithm based on the elaboration of load current signal has also been implemented. An extensive technical literature (see e.g., [4, 5]) exists on fault detection, but its discussion here is out of the scopes of this paper.

The fed induction motor is a two-pole three-phase squirrel cage whose nameplate is reported in Table 2.

A digital oscilloscope with two differential probes (up to a 25-MHz bandwidth) and 3% accuracy has been used to register voltage and current waveforms. Measurements data were stored in the computer hosting the dSPACE board with the help of "Octave" software.

Fault emulation have been realized with the help of solid state relays and connectors being driven from the dSPACE board and software interface. In this way, it was possible to test the behavior of the fault-tolerant converter in all possible condition without a real disruption of the power devices.

Figures 23, 24, and 25 shows, respectively, the measurements of voltage on faulty and unfaulty phases and the measurement of the currents, before and after fault and reconfiguration.

This final comparison validates the proposed general model of VSI in healthy and faulty mode implemented algorithm.

7. Conclusions

The use of fault-tolerant systems is essential for the optimal development of electrical power production by renewable sources as well as for the achievement of high reliability

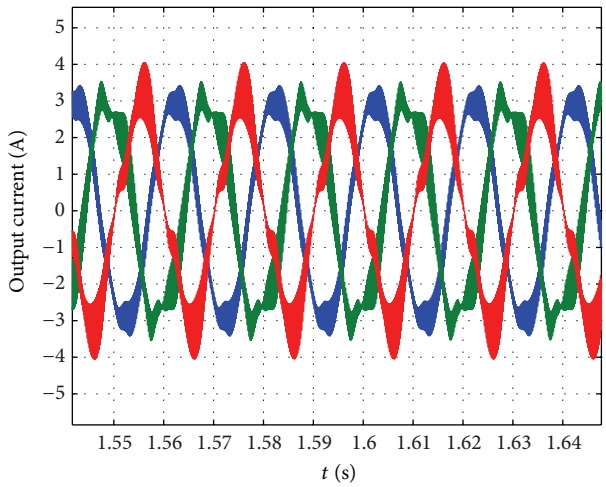

Figure 16: After fault current zoom.

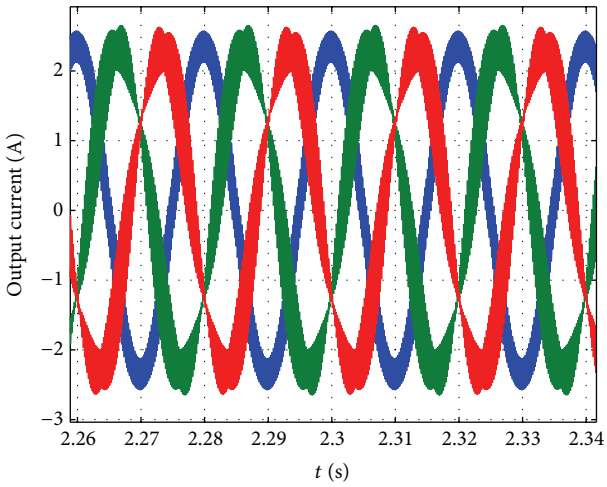

Figure 17: After fault current with no reactive power.

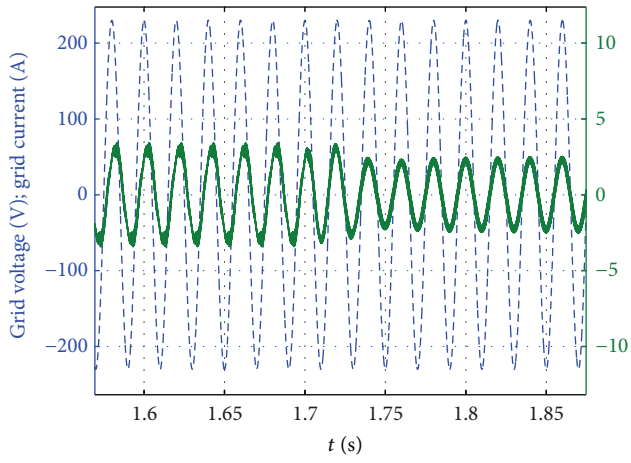

Figure 18: Phase voltage (blue dashed) and current (green continuous) with and without Q transmission.

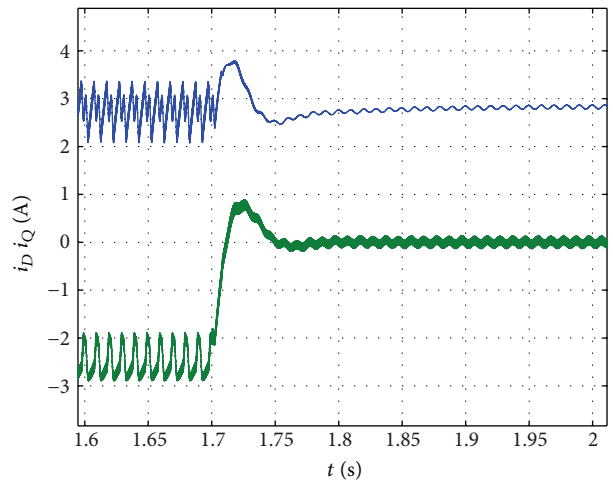

Figure 19: i_D and i_Q transient after vanishing Q.

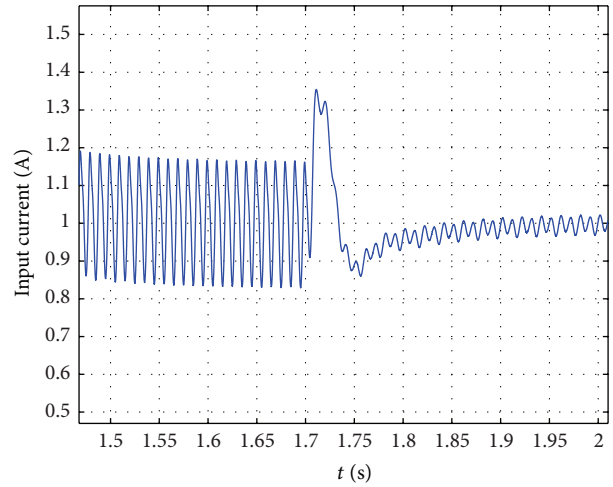

Figure 20: Transient on i_0 after vanishing Q.

Table 2: Test bench induction motor nameplates.

Ratings	Value
Power	5.5 kW
Speed	2870 r.p.m
Frequency	50–60 Hz
Torque	18.3 Nm
Voltage	400 V
Current	13 A
Poles	2

and power quality fundamental for both end users and grid manager.

Fault tolerant converters require intelligent real-time detection algorithms of incoming failures easy to implement even on low cost hardware, such as microcontrollers or Pegasus.

In this paper, the authors have considered the fault tolerant operation of an inverter for distributed generation

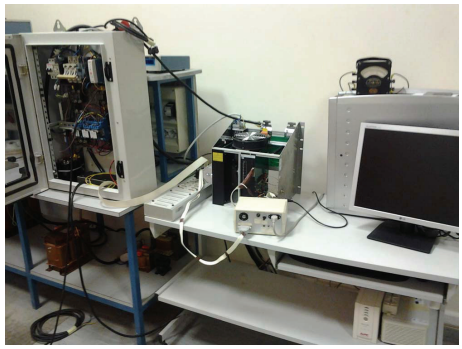

Figure 21: Picture of the realized test bench.

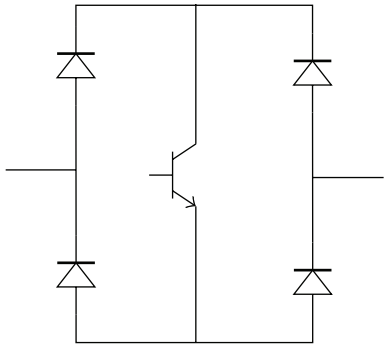

Figure 22: A bidirectional switch realized with diode and IGBT.

system seen as an ancillary complementary function in addiction to the classical ones already developed. The general inverter model here presented in the paper is suitable and useful for the simulation of faults and fault-tolerant operation of a VSI. The presented model is very helpful to predict transient phenomena due to faults occurrence. Switching function definition has been extended in order to cover the condition of diode turning on and open fault occurrence. The introduction of HDBVs and HLBVs allows for the construction of a unified model suitable for simulations with equation solver tools. This makes the simulations affordable and at the same time fast in their operation.

The implementation algorithm is very suitable in large context as grid connected converter for DG because it is transparent to the action of the main power control and synchronization.

Numerical simulations presented in the paper have considered both a standalone and a grid converter. In order to guarantee minimal power quality degradation, the following considerations apply in the converter control:

(i) over modulation must be avoided;

(ii) for this reason both a reduction of the transmitted active power and vanishing the reactive power are mandatory;

(iii) a 25–30% greater DC link voltage with respect to traditional value must be chosen.

The control has been also verified with experimental results in the case of reconfigurable operation. Comparison of

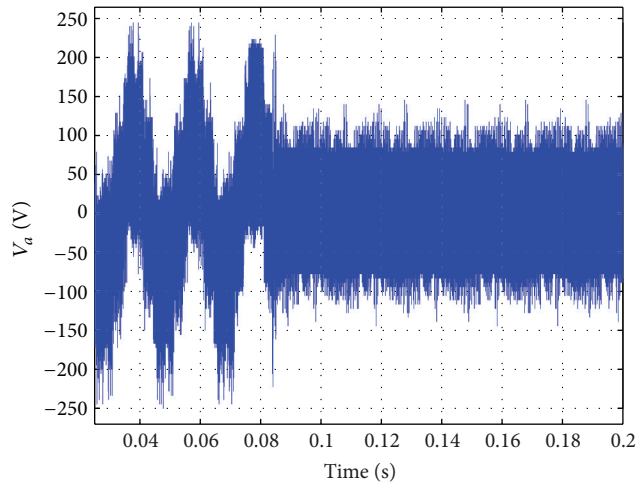

Figure 23: Measurement of faulty phase voltage before and after the fault.

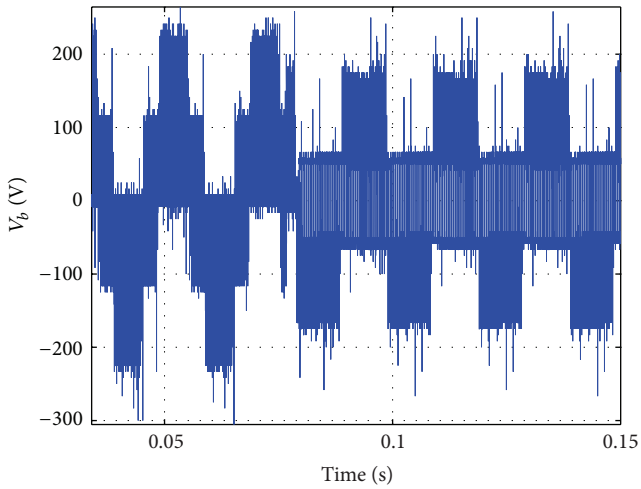

Figure 24: Measurement of unfaulty phase voltage before and after the fault.

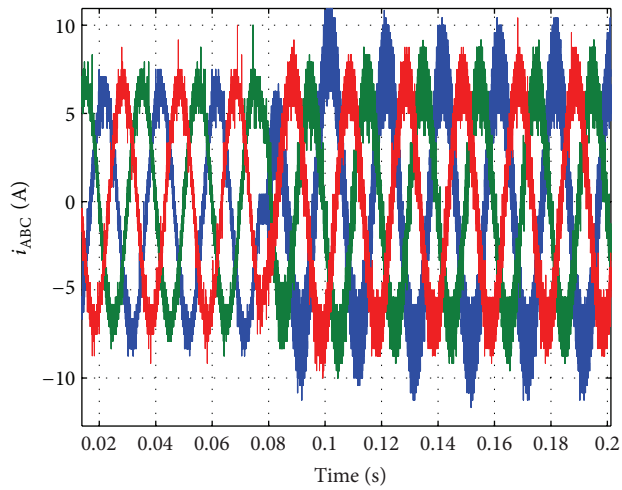

Figure 25: Measurement of phase currents before and after the fault.

simulations and experimental results, with the clear good accordance between them, confirms the validity of the proposed model and encourages the proposed implementation algorithm to include fault tolerance as an additional ancillary function in the next generation of grid converters.

Abbreviations

$j = \{A, B, C\}$: Phase index
$v_{jO(N)}$; i_j: Phase voltages and currents on the AC side
e_{jN}: Back e.m.f. of the load (or grid voltages)
$h_{j\pm}$: Upper(+)/lower(−) healthy device binary variables
h_j: Healthy leg binary variables
$S_{j\pm}$: Upper(+)/lower(−) side transistor switching function for phase j
$\widehat{S}_{j\pm}$: Upper(+)/lower(−) side transistor generalized switching function for phase j
$D_{j\pm}$: Upper(+)/lower(−) side diode switching function for phase j
$\otimes$: Logical AND operator
$\oplus$: Logical OR operator
U_{DC}: Whole inverter capacitor bank voltage
U_1, U_2: Partial capacitor bank voltage
i_0: DC side inverter input current
R_0, L_0: DC side wires parasitic circuital parameters
C: Value of the single DC link capacitor
R, L: Load circuital parameter (or grid filter resistance and inductance)
$[\cdots]^t$: Transposition of a matrix (a vector)
$\mathbf{1} = [111]^t$: Unitary three-dimensional vector
$\mathbf{u}_{\mathrm{ref}}$: Vector of the reference voltage in PWM control
$\mathbf{u}^*_{\mathrm{ref}}$: Vector of the reference voltage in PWM control after a fault
$\mathbf{v_k}$: Vector of the converter output voltages
$\mathbf{h}$: Vector of the healthy leg binary variables
$\underline{\mathbf{h}}$: NOT($\mathbf{h}$) vector
$\mathbf{i_k}$: Vector of the load currents
$\widehat{\mathbf{S}}_\mathbf{k}$: Vector of the switching functions $[\widehat{S}_A, \widehat{S}_B, \widehat{S}_C]^t$
φ: Angle displacement
U_x: Phasor voltage peak
$\alpha = \exp(j(2\pi/3))$: Fortescue operator for symmetrical Components
$\mathbf{v}_1 \times \mathbf{v}_2$: Cross product between generic vectors $\mathbf{v}_1$ and $\mathbf{v}_2$

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