

## Editorial

# Advanced RF and Analog Integrated Circuits for Fourth Generation Wireless Communications and Beyond

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Fourth generation wireless communications are approaching to market, and recent innovations are at peak to come up with RF and analog circuit solutions to provide low power and high speed tiny chips at very low cost. This special issue presents the researches and technical know-how suitable for critical advanced researches in ICs development. After rigorous review of numerous research and review articles, this special issue finalizes one review article and three research articles which address the recent developments in IC design and are suitable for publication in this peer journal.

Oscillators are one of the most critical components of transceiver, and designing low phase noise oscillators operating at several GHz is a challenging task. To help researchers understand the design implementation and its performance with different topologies and architectures, the recent advances in CMOS VCOs are discussed. Recently, innovations in CMOS oscillators have extended to higher end of millimeter-wave region maintaining their performance comparable to microwave oscillators.

Present and future communication systems demand that electronic devices be suitable for a range of applications with different bandwidth, speed, and accuracy. This necessitates the need for reconfigurable devices, and to cover this flavor, innovation in reconfigurable LNA for UWB receivers has been addressed. This LNA exploits the programmable circuit to control the mode of operation and with current reuse

improves the gain and flatness. The designed LNA operates in two subbands of MB-OFDM UWB, UWB mode-1 and mode-3, as a single or concurrent mode.

Miniaturization is the key for CMOS technology and bulky inductors are the main hindrance. Therefore, circuit topology without a bulky inductor is highly desired and promoted. Inductorless PLL with subharmonic pulse injection locking has been introduced. A half-integral subharmonic locking technique helped to improve phase noise characteristics.

Although, recent developments and scaling of CMOS technology are pushing the signal processing into digital domain, the hard truth is that the real world is analog, and, therefore, analog-to-digital converter is an integral part of chip design. Delta-sigma modulator is gaining more and more attention and popularity because of its potential to achieve high resolution and high speed. Continuous-time delta-sigma modulator helps to design low power modulator, and hence a systematic design methodology to design such modulator is presented.

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*Ramesh Pokharel*  
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