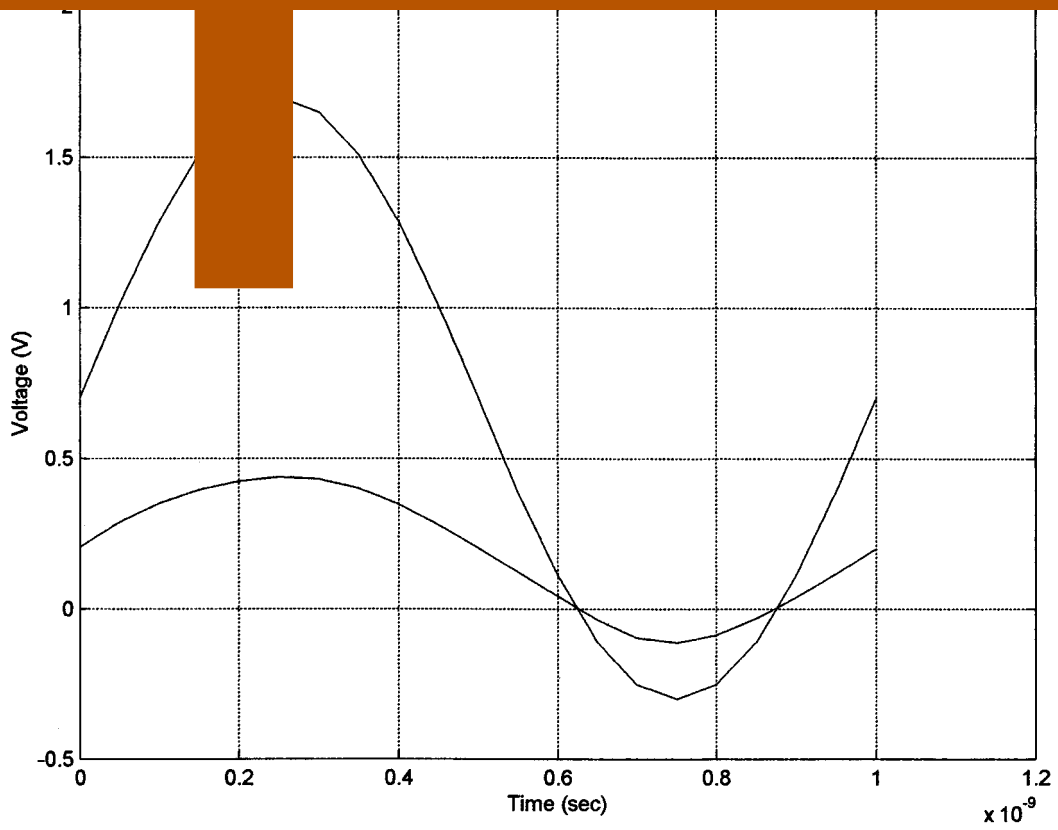

Figure 3 Voltage waveform over one period of fittest individual from final generation

not require auxiliary information such as a Jacobian matrix, which represents a major advantage over existing implementations of harmonic balance.

REFERENCES

1. P.J.C. Rodrigues, Computer-aided analysis of nonlinear microwave circuits, Artech House, Norwood, MA, 1998.
2. R.J. Gilmore and M.B. Steer, Nonlinear circuit analysis using the method of harmonic-balance—A review of the art. 1. Introductory concepts, Int J Microwave Millimeter-Wave Computer-Aided Eng 1 (1991), 22–37.
3. P.J.C. Rodrigues, M.J. Howes, and J.R. Richardson, Efficient computation of the steady-state response of periodic nonlinear microwave circuits using a convolution-based sample-balance technique, IEEE Trans Microwave Theory Tech 39 (1991), 732–737.
4. S. Iezekiel and A. Feresidis, Application of genetic algorithm to sample balance analysis of nonlinear circuits, Electron Lett 34 (1998), 2080–2082.
5. Z. Michalewicz, Genetic algorithms + data structures = evolution programs, Springer-Verlag, Berlin, Germany, 1994.
6. A.J. Chipperfield, P.J. Fleming, H. Pohlheim, and C.M. Fonseca, Genetic algorithm toolbox user's guide, Department of Automat Contr Syst Eng, University of Sheffield, England, Res Rep 512, 1994.

INTEGRATED SSFIP-HORN ANTENNA AT 75 GHz

Tomasz M. Grzegorczyk,[1] Alejandro A. Melcón,[2] Jean-François Zürcher,[1] Anja K. Skrivervik,[1] Philipe Renaud,[3] and Juan R. Mosig[1]
[1] Electromagnetics and Acoustics Laboratory (LEMA)
Ecole Polytechnique Fédérale de Lausanne (EPFL)
CH-1015 Lausanne, Switzerland
[2] Electromagnetics and Telecommunications Group
Polytechnic University of Carthagena
30201 Cartagena (Murcia), Spain
[3] Institute of Microsystems (IMS)
Ecole Polytechnique Fédérale de Lausanne (EPFL)
CH-1015 Lausanne, Switzerland

Received 20 March 2000

ABSTRACT: *We present in this paper an integrated cavity-backed patch antenna operating at 75 GHz. The design was optimized using a full-wave software based on the integral-equation method. The antenna was realized using micromachining technologies on two wafers: a silicon one supporting a membrane and a radiating patch, and a Pyrex one constituting the feeding element. The measurements are in good agreement with the theoretical predictions.* © 2000 John Wiley & Sons, Inc. Microwave Opt Technol Lett 26: 298–302, 2000.

Key words: *horn antenna; integrated device; micromachining technology; V-band measurements*

1. INTRODUCTION

Various applications, from communication to biomedical systems, are calling for increasingly reduced-size components. In

the world of antennas, microstrip technology proves to be very flexible in that direction, mainly because of its simplicity, conformability, and low fabrication costs. Thus, the use of micromachining techniques for the elaboration of ever smaller devices is nowadays in full expansion, ranging from packaging technology [1], to power meters [2], filters [3], diplexers [4], and, of course, microstrip antennas [5, 6].

However, a limiting factor as the operating frequency increases is represented by the losses in the dielectric substrate, mainly due to the undesirable surface waves excited. The latter can drastically alter the behavior of an antenna by reducing its bandwidth, deteriorating its radiation pattern, or lowering its efficiency [7]. Possible solutions to reduce the surface-wave excitation are the use of low-index dielectrics [8] exciting mainly space waves, of circular patches with appropriate radii [9], or of membranes supporting rectangular patches over an air cavity or a low-index material [6].

Driven by the purpose of surface-wave elimination, the overall concept of the antenna presented in this paper is based on the already well-known SSFIP antennas (strip–slot–foam–inverted–patch) [10, 11], which are easy to manufacture using classical technologies in the *C*-band, and exhibit good electromagnetic characteristics (easy to match, large bandwidth, good gain). Based on well-established results, our purpose is to reach a tenfold increase in the operation frequency of the antenna, thus entering into the *V*-band. As a consequence, the dimensions of the device are reduced by a similar factor, leading to a complete change of the associated technological challenges and procedures. The general layout of the antenna and the materials used are presented in Figure 1. The proposed structure can be used for high radiation efficiency antennas in the millimeter-wave band since surface waves are inherently suppressed with the use of a metallic horn cavity configuration. All of the dimensions have been optimized by a full-wave analysis of an equivalent design (see Section 2), and the technological steps are presented in Section 3.

2. ELECTROMAGNETIC PART

2.1. Insight into the Theory. A reasonable way to analyze the antenna of Figure 1 is to consider it as being a succession of connected metallizations embedded in a multilayered medium. Thus, our problem falls into the category of microstrip antennas with vertical connections, embedded in stratified media. This subject has been in the scope of research for many years now, so that it is already well known in the literature for either horizontal sources [12–14] or, more recently, for vertical sources [15, 16].

The purely theoretical kernel of the treatment being beyond the scope of this paper, we will not enter into extensive details, and the reader is once again referred to [16]. However, for the sake of clarity, we should nevertheless mention that the integral equation has been proved to be an efficient technique to deal with such problems. Based on the accurate determination of all of the Green's functions for the fields in multilayered media, it has been widely used in the literature for the study of more classical microstrip antennas. A variation of this method is the mixed-potential integral equation (MPIE) which uses the Green's functions for the potentials instead of those for the fields, leading to more stable numerical algorithms (the Green's functions for potentials being less divergent than those for the fields). This is the one we have used, combined with a Galerkin implementation of the method of moments [17], to obtain the simulated results presented in Figure 2.

2.2. Optimized Design. As can be seen in Figure 1, the antenna is composed of two parts having complementary roles: the first one (Pyrex wafer, $\varepsilon_r \simeq 4.4$ determined by an annular

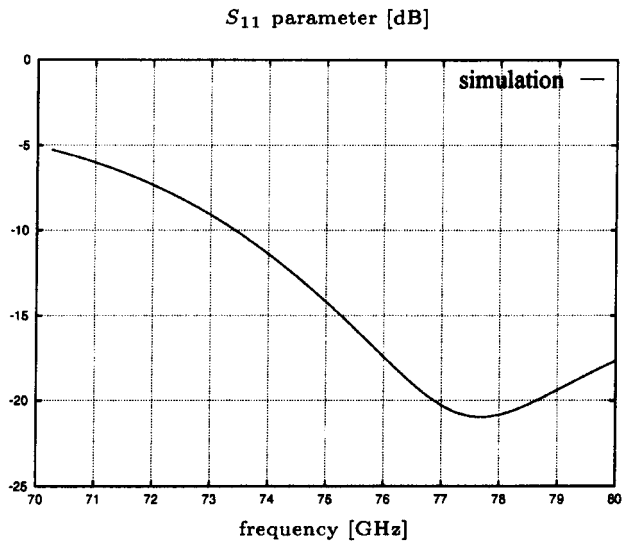

Figure 2 Simulated results of an SSFIP antenna equivalent to the one depicted in Figure 1, where the horn has been replaced by a cavity with vertical walls

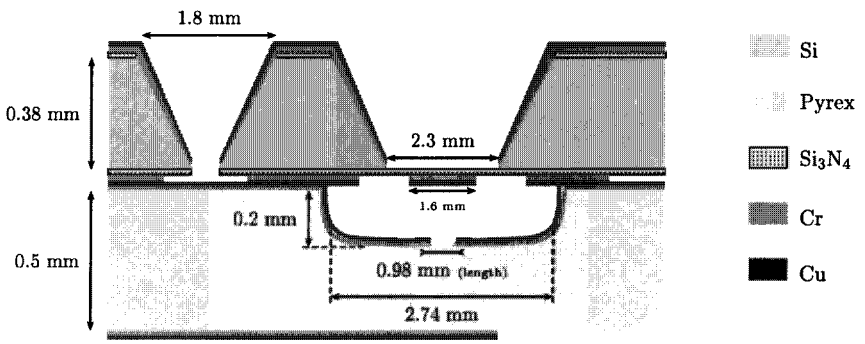

Figure 1 Design of the integrated horn antenna at 75 GHz. The antenna is composed of two wafers: a silicon wafer (with a horn, a membrane supporting a patch, and an auxiliary hole for the electric contact with the second wafer) and a Pyrex wafer (with a cavity, a slot, and a feeding line)

line resonance) supports the excitation of the antenna, whereas the second one (silicon wafer) represents the radiating part. Previous analysis of SSFIP antennas [18] has shown that special attention should be paid to the parameters (*line–slot–patch*) since they are of primary importance for the adaptation of the device. The large number of simulations run has shown that the size of the cavity, once adjusted, has a second-order influence on the frequency of operation. For the sake of clarity, the important parameters for the optimization are defined in Figure 3 and are developed hereafter.

- *Feeding Line*: Due to the change in the height of the substrate below the cavity, the line needs to have two different widths in order to keep a 50 Ω characteristic impedance. At $f = 75$ GHz, the widths are $W_1 = 1290$ μm and $W_2 = 672$ μm. The transition between W_1 and W_2 has been accomplished by tapering the line over a length of λ_g (λ_g being the guided wavelength). The length of the line beyond the slot has been set to $\lambda_g/4$ in order to have a maximum current right below the slot.
- *Slot*: The optimal slot dimensions were found to be $L_{\text{slot}} = 980$ μm, $W_{\text{slot}} = 80$ μm. However, the adaptation of the antenna is not too sensitive to the width of the slot, which can be chosen larger than the optimum in order to render the technological realization easier.
- *Cavity*: The depth and the dimensions of the cavity, once optimized, were found to be: depth = 200 μm (see Fig. 1), $L_{\text{cavity}} = W_{\text{cavity}} = 3200$ μm.
- *Patch and Membrane*: The optimum results were obtained for a square patch of dimensions $L_{\text{patch}} = W_{\text{patch}} = 1600$ μm printed on a square membrane with parameters $L_{\text{mem}} = W_{\text{mem}} = 2300$ μm.
- *Horn*: Since the thickness of the silicon wafer (approximately 380 μm) as well as the etching plane ($\langle 100 \rangle$, giving an apex angle of 70.6°) are fixed in our case, the aperture of the horn is already determined by the size of the membrane (because of the anisotropic nature of the chemical etching). However, for the analysis, we have considered a cavity model with vertical planes, allowing the direct use of the cavity Green's functions [19] instead of a recursive algorithm [20]. This assumption is not a hindrance in our case since it has been clearly shown [21] that, in a horn antenna, the entire part above the patch has a negligible influence on the input impedance of the device, but affects mainly the radiation pattern (and, conversely, the part below the patch affects mainly the input impedance, and almost not the radiation pattern). Therefore, the approximation of a square cavity is a reasonable choice in our case.

3. TECHNOLOGICAL DETAILS

3.1. Silicon Wafer. A 380 μm $\langle 100 \rangle$ low-doped ($< 10^{19}$) silicon wafer has been used for the realization of the upper part of the antenna. An Si_3N_4 low-stress 1 μm thick layer has been chemically evaporated on both sides, and, in the future, will constitute the membrane supporting the radiating patch.

The technological steps applied to the wafer are the following.

Step A.1: Wafer preparation.
Step A.2: Back-side metallization.
Step A.3: Front-side Si_3N_4 patterning.
Step A.4: Back-side patterning.
Step A.5: Si etching.
Step A.6: Front-side metallization.

A precise cleaning of the wafer in a HNO_3 solution at room temperature for 5 min followed by a BHF cleaning for 30 s has been applied first (Step A.1) in order to obtain a good adherence of the metals further evaporated on the Si_3N_4 layer. This step is of the foremost importance in our case since a defect in the metallizations of the final device can drastically alter its electromagnetic behavior.

The conducting metal used for the antenna is copper, which is widely used at lower frequencies (e.g., for microstrip

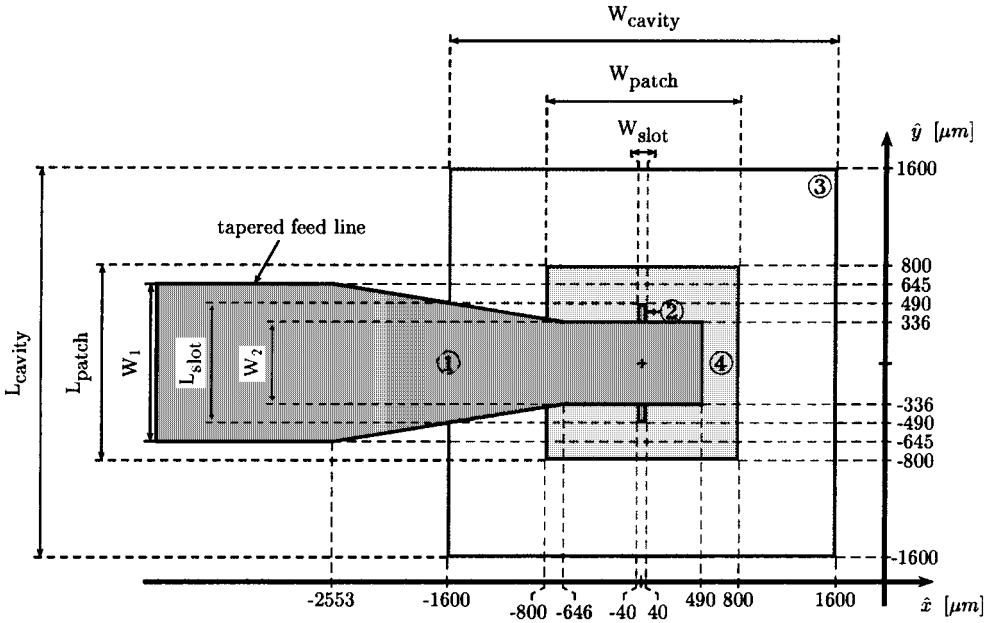

Figure 3 2-D layout of the SSFIP antenna operating at 75 GHz. From the bottom of the antenna to the top, the successive elements are: (1) line, (2) slot, (3) cavity, (4) patch

antennas). In order to obtain a good adherence on the Si_3N_4 layer, a chrome layer (thickness 30 nm) has been evaporated before the copper one (thickness 200 nm). The thickness of the chrome layer should be kept as small as possible because of its low conductivity which can degradate the electromagnetic performances of the whole device. Then, in order to reach a 5 μm thickness of copper, which is large enough in comparison with the skin depth at these frequencies, a galvanization at a rate of 0.75 μm/h has been performed (Step A.2). The front-side patterning (Step A.3) enters into a classical photolithographic process (with a positive S1813 photoresist), and is followed by a plasma etching of the Si_3N_4. The back-side galvanization (Step A.4) is very similar to Steps A.2 and A.3 so we will not give further details here. Notice, however, that for the patterning, we need to etch the chrome layer without removing the copper one. This can be done in two ways: either by using a solution that attacks both metals at the same rate, and considering that the copper layer will not be too affected due to the large difference in thicknesses between the two metals, or by using a selective solution (Cr etch, selective to Cu). This last possibility is more reliable, but also highly dangerous because of the chemicals involved.

The silicon etching (Step A.5) represents a limit in the process beyond which all manipulations should be performed extremely carefully. As a matter of fact, a 24 h KOH bath at 60°C completely etches the silicon wafer, thus revealing the 1 μm thick membranes with the patches printed on their back sides (the measured etching rate was about 16 μm/h). Finally, the front-side metallization (Step A.6) has been performed following an already described processes (Cr + Cu evaporation, Cu galvanization, photolithography), and a view of the top of the final chip is proposed in Figure 4.

3.2. Pyrex Wafer. From a technological point of view, the processing of the Pyrex wafer (thickness = 500 μm $\pm$ 50 μm) demands less attention than that for the silicon one, mainly because no real fragile steps have to be dealt with. The overall process can be divided into the following steps.

Step B.1: Wafer preparation (similar to Step A.1).
Step B.2: Mask elaboration.
Step B.3: Pyrex etching.
Step B.4: Slot (front) and feed line (back) design.

In view of a quite severe chemical attack to etch the cavity in the Pyrex, we have doubled the mask on both sides of the wafer (Step B.2). First, a layer of sputtered chrome (cold reaction) has been deposited, and second, a negative SC450 photoresist (needing a 85°C postbake for about 1 h, a development in a WNRD solution, and a raise in an N butyl acetate solution). Once the photolithographic process was finished and the chrome was removed at the corresponding locations, the attack was done in a 50% HF solution heated at 30°C (in order to homogenize the attack and avoid a porous cavity bottom), etching at a rate of about 10 μm/min (Step B.3). Although dangerous, this step is not delicate, provided that a regular control of the etching depth is performed. The negative photoresist is then removed by a 5 min bath in a Piranah solution, and the remaining chrome by a classical Cr-etch solution. The design of the slot on the front and of the line on the back sides follows a now classical process (Step B.4): a thin chrome layer is evaporated for better adherence of the copper, which is then evaporated and galvanized. The photolithography is done on both sides simultaneously since the line and the slot need to be perfectly aligned. It is interesting to note at this point that a classical spinning of a positive S1813 photoresist is very efficient, despite the nonplanar structure of the wafer.

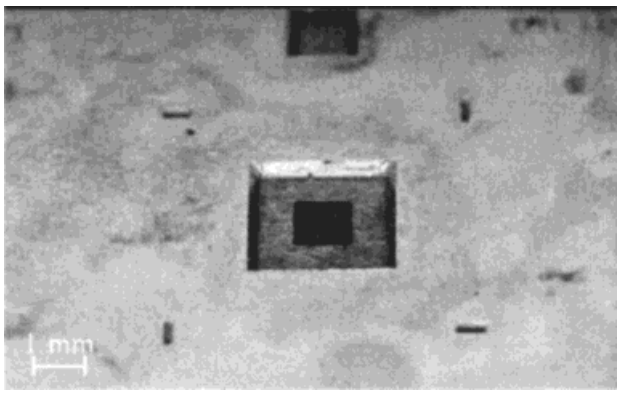

Figure 4 Above perspective of the silicon wafer at the end of the process. The different elements are clearly visible: the horn, the patch, and the different alignment marks

The final chip obtained is presented in Figure 5, where an additional canal for the air evaluation has been etched. The latter will be needed in the future in order to maintain a constant pressure inside the cavity (when the two wafers will be stacked together), and thus lowering the risk of breaking the membrane.

4. RESULTS AND CONCLUSION

The integrated horn antenna was designed to work at 75 GHz, and its input impedance was measured in the 50–100 GHz range on an HP 8510 XF network analyzer (able to measure from 1 up to 110 GHz). The results are presented in Figure 6. It must be pointed out that the antenna has been realized and measured at the final frequency of 75 GHz with no room for scale models. Despite the expected high losses at these frequencies (the simulations were performed with dielectric losses measured in the *C*-band) that are probably responsible for the -3 dB shift in the lower part of the frequency range (50–60 GHz), and the general ripples probably due to multiple-wave reflections difficult to control in the *V*-band, the results show a good similarity with the

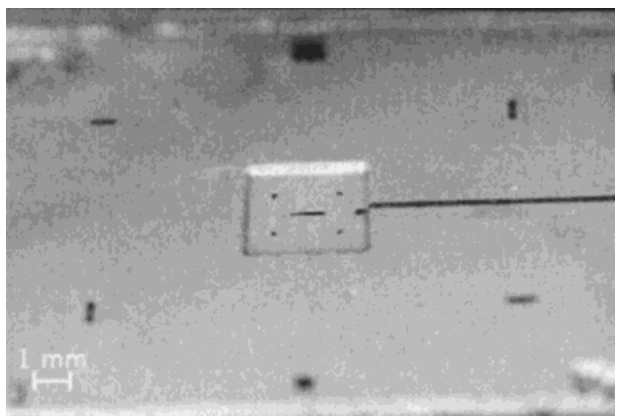

Figure 5 Above perspective of the Pyrex wafer at the end of the process. The different elements are clearly visible: the cavity, the slot, the different alignment marks, and the evacuation canal

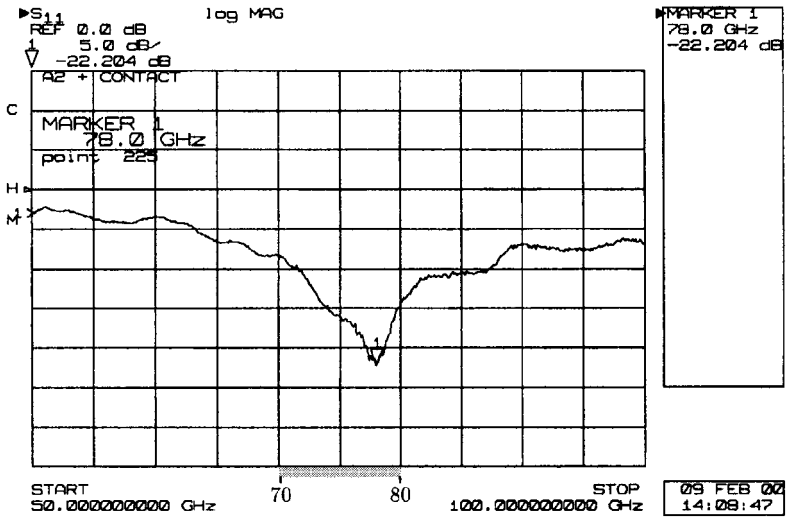

Figure 6 Measurements of the integrated antenna in the 50–100 GHz range. The shaded region corresponds to the simulated frequency range of Figure 2

theoretical predictions (see Fig. 2), in both the resonant frequency and the matching level.

Thus, we have shown that the technology for the fabrication of these types of antennas is now mature, and combined with accurate electromagnetic analysis software, can lead to reliable designs and small development times, including optimization and final fabrication.

REFERENCES

1. R.M. Henderson and L.P. Katechi, Silicon-based micromachined packages for high-frequency applications, IEEE Trans Microwave Theory Tech 47 (1999), 1563–1569.
2. C.C. Ling and G.M. Rebeiz, A wide-band monolithic quasi-optical power meter for millimeter- and submillimeter-wave applications, IEEE Trans Microwave Theory Tech 39 (1991), 1257–1261.
3. C.-Y. Chi and G.M. Rebeiz, Planar microwave and millimeter-wave lumped elements and coupled-line filters using micromachining techniques, IEEE Trans Microwave Theory Tech 43 (1995), 730–738.
4. A.R. Brown and G.M. Rebeiz, A high-performance integrated *K*-band diplexer, IEEE Trans Microwave Theory Tech 47 (1999), 1477–1481.
5. M.J. Vaughan, K.Y. Hur, and R.C. Compton, Improvement of microstrip patch antenna radiation patterns, IEEE Trans Antennas Propagat 42 (1994), 882–885.
6. I. Papapolymerou, R.F. Drayton, and L.P. Katehi, Micromachined patch antennas, IEEE Trans Antennas Propagat 46 (1998), 275–283.
7. D.H. Schaubert and K.S. Yngvesson, Experimental study of a microstrip array on high pervittivity substrate, IEEE Trans Antennas Propagat AP-34 (1986), 92–97.
8. N.G. Alexopoulos and D.R. Jackson, Fundamental superstrate (cover) effects on printed circuit antennas, IEEE Trans Antennas Propagat AP-32 (1984), 807–816.
9. D. Jackson, J. Williams, A. Bhattacharyya, R. Smith, S. Buchheit, and S. Long, Microstrip patch designs that do not excite surface waves, IEEE Trans Antennas Propagat 41 (1993), 1026–1037.
10. J.-F. Zücher and F.E. Gardiol, SSFIP—A global concept for high performance broadband planar antennas, Electron Lett 24 (1988), 1433–1435.
11. J.-F. Zürcher and F.E. Gardiol, Broadband patch antennas, Artech House, Norwood, MA, 1995.
12. J.R. Mosig and F. Gardiol, General integral equation formulation for microstrip antennas and scatterers, Proc Inst Elect Eng 132 (1985), 424–432.
13. J.R. Mosig, Arbitrarily shaped microstrip structures and their analysis with a mixed potential integral equation, IEEE Trans Microwave Theory Tech 36 (1988), 314–323.
14. Y.L. Chow, N. Hojjat, S. Safavi-Naeini, and R. Faraji-Dana, Spectral Green's functions for multilayer media in a convenient computational form, Proc Inst Elec Eng 145 (1998), 85–91.
15. N. Kinayman and M.I. Aksun, Efficient use of closed-form Green's functions for the analysis of planar geometries with vertical connections, IEEE Trans Microwave Theory Tech 45 (1997), 593–603.
16. T.M. Grzegorczyk and J.R. Mosig, Full-wave analysis of antennas containing horizontal and vertical metalizations embedded in multilayered media, IEEE Trans Antennas Propagat (submitted).
17. R.F. Harrington, Field computation by moment method, IEEE Press, New York, 1993.
18. Y. Brand, Antennes imprimées SSFIP: de l'élément isolé au réseau planaire, Ph.D. dissertation, Ecole Polytechnique Fédérale de Lausanne, Switzerland, 1996.
19. A.A. Melcón and J.R. Mosig, Strip, slot, air, inverted patch (ssaip): A cavity backed alternative to broadband communication antennas, Radio Sci 33 (1998), 1525–1542.
20. T.M. Grzegorczyk, J.-F. Zücher, and A.K. Skrivervik, Analysis of a horn antenna by the integral equation method, JINA Conf, Nov. 1998, pp. 92–95.
21. G.V. Eleftheriades, Analysis and design of integrated-circuit horn antennas for millimeter and submillimeter-wave applications, Ph.D. dissertation, Radiation Lab, University of Michigan, 1993.