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PASSIVE ON-CHIP COMPONENTS FOR FULLY INTEGRATED SILICON RF VCOs

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In this work integrated passive devices used in RF VCOs are presented. The operation of on-chip inductors and variable capacitors is outlined along with simple electrical equivalent circuits suitable for hand calculations. Design examples of passive devices operating at 5 and 6 GHz in a commercial HBT BiCMOS process are also presented. The parallel resonator quality factor is computed as a function of inductor L capacitor C and their respective losses R_{SL} and R_{SC}.

1 INTRODUCTION

The deployment of modern wireless communication systems demands low power portable devices with small form factors that operate at high frequencies. Recent standardization activities have allocated frequencies up to 5 GHz for personal communications and wireless data transmission. One of the key issues that need to be addressed in order to successfully implement low power portable devices is the integration level of RF circuits. In current implementations a significant amount of external passive and active components accompanies the RF circuitry. External inductors and capacitors are used for matching networks and resonators. External filtering is performed with SAW filters, increasing both the PCB area and power consumption, leading to large and power-hungry portable devices. Having most of the RF circuitry into the same IC can significantly reduce current consumption, since there is no need to interface with external 50-ohm systems. By integrating passive components the reliability of the RF circuitry is increased and the printed circuit board is more compact and cost-effective to manufacture.

Recent research activities have demonstrated the potential for increasing the level of integration of various RF subsystems into the same IC [1–7].

One of the major building blocks in an RF transceiver is the Local Oscillator (LO) signal generator. A voltage-controlled oscillator (VCO) is used in a phase locked loop (PLL) to generate the LO signal and drive the up- and down-conversion mixers. VCO circuits can be divided into three major categories: relaxation, ring and harmonic oscillators. For high frequency LO generation, harmonic oscillators are almost exclusively used. Their superior

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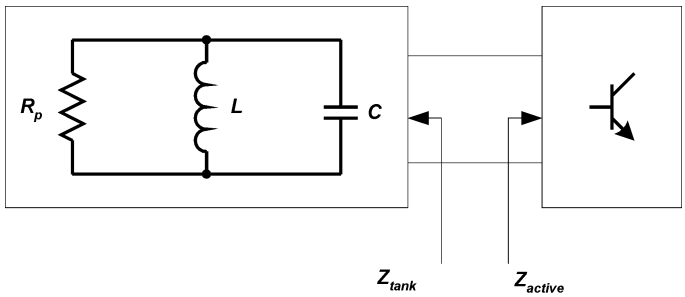

FIGURE 1 General harmonic oscillator topology.

performance in terms of phase noise, harmonic content and current consumption compared to relaxation and ring oscillators makes them an excellent choice. A general topology is shown in Figure 1. Harmonic oscillators are formed by the parallel connection of a passive resonator circuit and an active part that compensates for the resonator losses. The passive resonator is formed by the parallel or series connection of an inductor and a capacitor.

One of the most important parameters for a VCO circuit is phase noise, which determines the spectral purity of the output signal. Phase noise in a harmonic VCO depends heavily on resonator quality factor that is a measure of resonator non-ideality and frequency selectivity. For low phase noise the resonator should have high quality factor. High-Q resonators have very sharp frequency selectivity and the resulting oscillator has high spectral purity.

The integration of high-Q resonators can be problematic, since on-chip passive components have significantly lower quality factors compared to their discrete equivalents. This can place a limit to the lowest phase noise integrated VCOs can achieve. However, advances in process technologies provide on-chip components with improved quality factors. It is believed that in the near future integrated VCOs will be capable of meeting phase noise specifications of modern wireless communication systems.

The subject of VCO design has been treated extensively in the literature. In recent research works the feasibility of integrating VCOs onto silicon has been treated, demonstrating the various problems towards VCO integration [8–22]. In this paper the passive components used in integrated VCOs are presented from the circuit designer's perspective. The characteristics of on-chip passive components are presented along with simple equivalent circuits that can be used for hand calculations. Performance limits are presented along with implementation examples in a commercial silicon process. The quality factor of the resonator is calculated as a function of its elements. The effect of the biasing resistor in three different resonator topologies is also examined.

2 PASSIVE COMPONENTS FOR INTEGRATED VCOs

2.1 Integrated Inductors

Integrated inductors are implemented as planar spiral structures in one or more metal layers. The most common structures are square and octagonal spirals, as shown in Figure 2, although circular implementations can be used provided they are allowed from the technology.

The main design parameters for a spiral inductor are its inductance L, quality factor Q and self-resonance frequency f_{SR}, which depend on the geometry of the spiral structure. In an ideal inductor the inductance is constant at all frequencies. The integrated inductor however, exhibits a non-constant inductance with respect to frequency, as shown in Figure 3. Three distinct

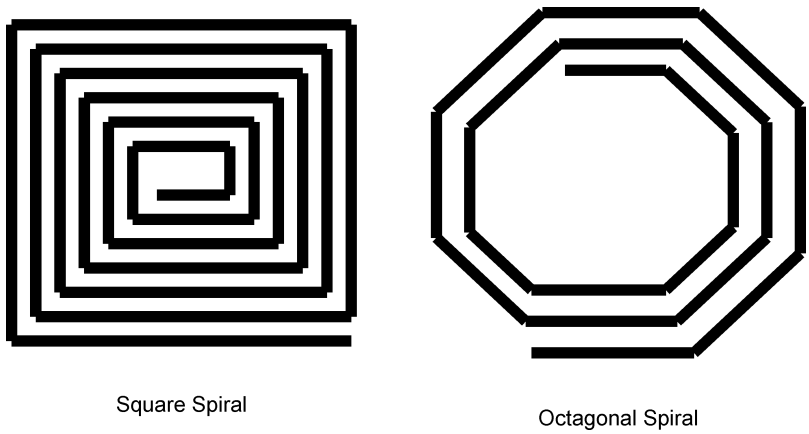

FIGURE 2 Common planar spiral structures.

areas of operation exist [23]. At low frequencies the inductance is relatively constant and insensitive to process spreads. This frequency region is the useful region where the spiral can be used as an inductor. At mid frequencies there is a transition from inductive to capacitive behaviour, where inductance changes with respect to frequency. Although the spiral structure behaves like an inductor, its inductance changes significantly from its low frequency value and is sensitive to process spreads. The frequency where the inductance equals to zero is the first self-resonance frequency. At this frequency the spiral structure behaves as a tuned LC tank. The self-resonance frequency depends mainly on the parasitic capacitance of spiral metal tracks to the substrate and capacitive coupling between the spiral segments. It is sensitive to process spreads. At higher frequencies the spiral structure behaves as a capacitor and cannot be used.

The quality factor of the inductor is a measure of the power dissipated as heat in the spiral structure. The main loss mechanisms of integrated inductors are substrate and metal track resistances.

When the spiral inductor operates at high frequencies, the substrate underneath behaves like a lossy dielectric and contributes to inductor losses. The magnetic field of the inductor induces currents to the substrate. By decreasing substrate resistivity, the induced currents increase, increasing also inductor losses. In deep submicron digital CMOS processes the substrate is heavily doped for proper operation of the transistors. The integration of spiral

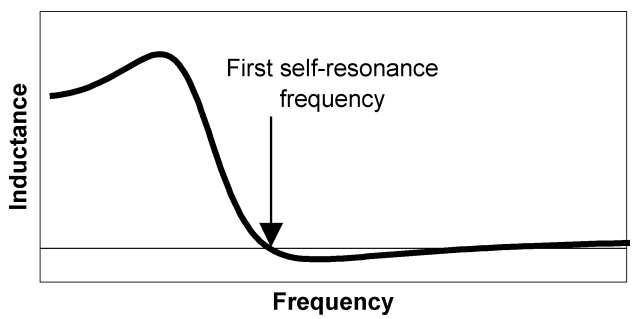

FIGURE 3 Typical integrated inductor performance.

inductors in these processes can be problematic, since higher substrate conductivity causes higher substrate and overall inductor losses.

The distance of the spiral structure from the substrate influences substrate currents. By designing the spiral to higher metal layers, its distance from the substrate increases, decreasing substrate currents. Deep submicron technologies provide several metal layers, 4,5 or even 6. If the highest metal layer is used to design the inductor the effect of higher substrate conductivity can be partly overcome.

The metal tracks that comprise the inductor are not ideal conductors. Their ohmic resistance contributes to inductor losses as series resistance. For a certain spiral structure the designer should use wide metal tracks to reduce series ohmic resistance. However, at the same time the parasitic capacitance to ground as well as the layout area increase. Since the self-resonance frequency f_{SR} of the inductor depends on the parasitic capacitance, as we increase the width of the metal tracks, f_{SR} decreases and can become as low as the frequency of operation thus making the inductor unusable.

Another way to increase inductor Q comes from a technology perspective. In modern submicron processes copper and gold alloys are used for the upper metalization layers along with increased metal track thickness. Since both Cu and Au have smaller characteristic ohmic resistance than the aluminium alloys already used, the total ohmic resistance of the spiral structure can be reduced.

From the above simple description it is evident that the design of integrated inductors is a challenging task. Several design trade-offs exist that make essential the accurate modelling of the spiral structure. The CAD tool presented in [24, 25] can be used to simulate the spiral structure. It can be used to evaluate the inductance and quality factor from the spiral's geometrical characteristics and optimise its performance for both quality factor and self-resonance frequency, helping the designer obtain the best possible integrated inductor in a particular technology.

After the design of the spiral structure we can use the simulated inductance L and quality factor Q to compute the electrical parameters of the simplified equivalent circuit of Figure 4. The equivalent circuit models the behaviour of the inductor in a narrow band of interest and not over the entire frequency band. Assuming the inductor has self-resonance frequency

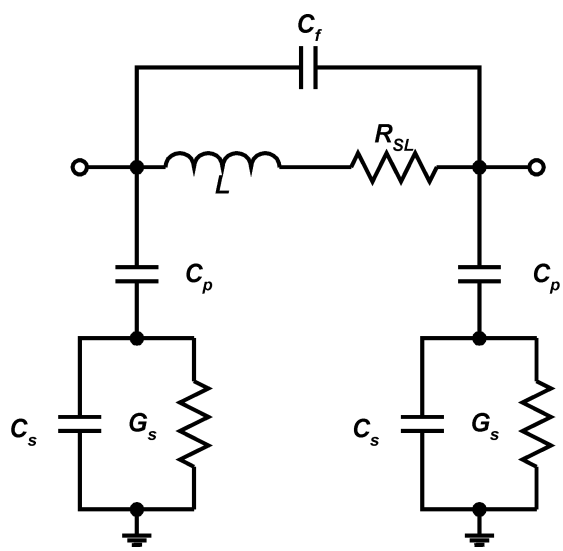

FIGURE 4 Simplified inductor model.

much higher than the frequency band of operation, we can neglect the effect of parasitic capacitances C_p, C_f and C_s, and compute the series resistance as $R_{\mathrm{SL}} = 2\pi fL/Q$. The simplified equivalent circuit can be used to perform hand calculations for the resonator characteristics, as will be presented later.

The design of inductors that operate at high frequencies, *e.g.* at 5 GHz, is even more challenging. This is because small inductances are needed, *e.g.* in the order of 1 nH. To achieve such a small inductance the spiral structure should have small geometrical characteristics. Interconnections between the inductor and the rest of the circuitry are comparable to inductor size and play a significant role to the total inductance of the spiral structure. Their influence should be carefully considered during the design phase.

Figure 5 illustrates an example of a small integrated inductor design. It shows a microphotograph of the inductor along with a sketch of its geometrical characteristics. The structure is a square spiral of $190 \times 190\,\mu\mathrm{m}^2$ with 7 segments. The interconnections are done with

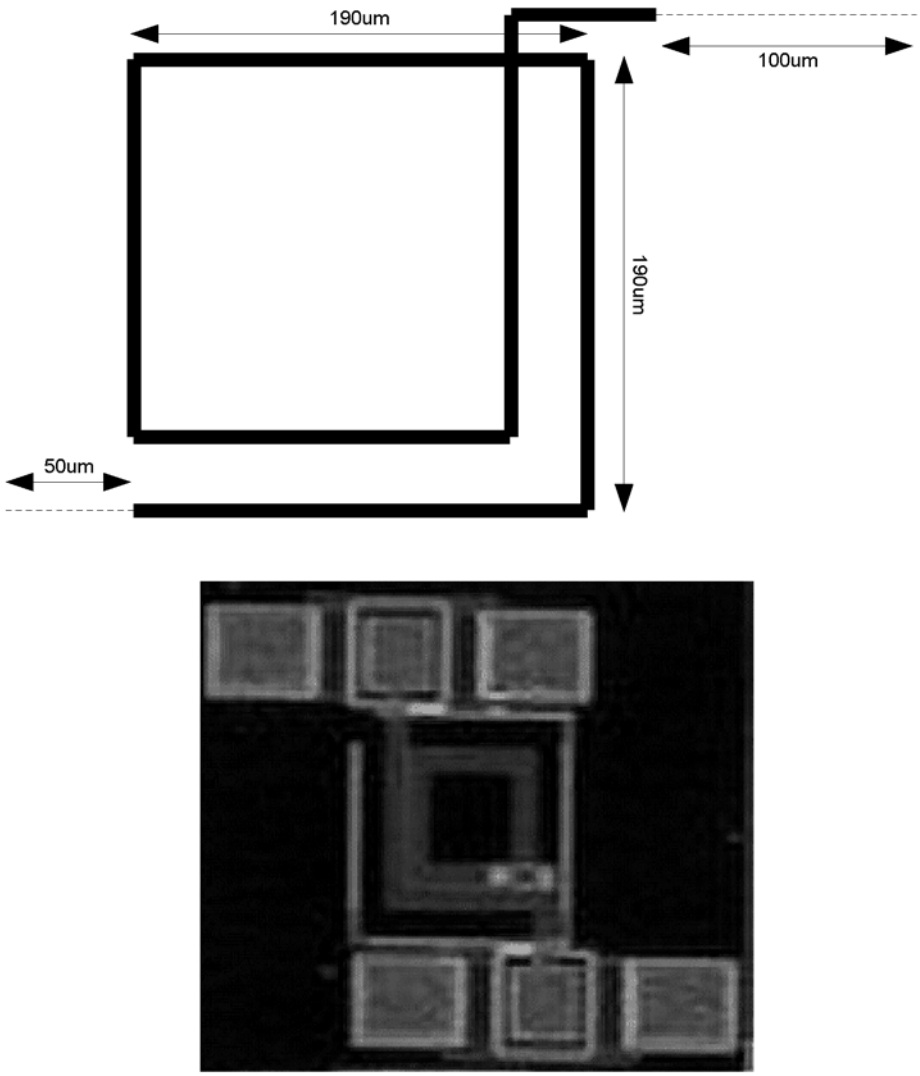

FIGURE 5 Inductor with small geometrical characteristics and its interconnections.

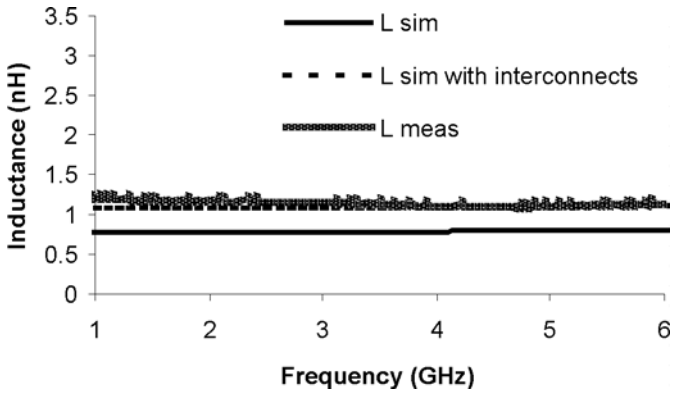

FIGURE 6 Small inductance performance.

two stabs of 50 μm and 100 μm at each end of the spiral, as shown in the sketch. The spiral is designed in AMS's 0.8 μm HBT BiCMOS process. The process provides two metal layers and the inductor is designed to the top metal layer in order to have the highest possible Q. The inductor is simulated to have an inductance of approximately 0.8 nH with a quality factor of 6 at 5 GHz.

Figure 6 shows the simulated inductance of the spiral itself and with the interconnections taken into account, along with measurement results. It is evident that interconnections influence overall inductance and should be taken into account. The variation due to the interconnections is approximately 42% from the nominal inductance value of 0.8 nH. Figure 7 shows simulation and measurement results for the inductor quality factor.

2.2 Variable Capacitors

Variable capacitors are used in LC tanks to tune the resonance frequency. The most common implementation in silicon technologies is the reverse biased p/n junction. In bipolar and BiCMOS processes the base–emitter and base–collector junctions of a bipolar transistor can be used. The base–emitter junction has the advantage of low emitter resistance and thus low losses. However, its low breakdown voltage, in the order of 2 V for a 0.8 μm BiCMOS process, does not permit high reverse bias voltages to be applied, reducing the oscillation tuning range.

The base–collector junction can withstand higher reverse bias voltages, as its breakdown voltage is in the order of 15 V for a 0.8 μm BiCMOS process, and can thus provide increased tuning range. However, the collector ohmic resistance is high increasing diode losses.

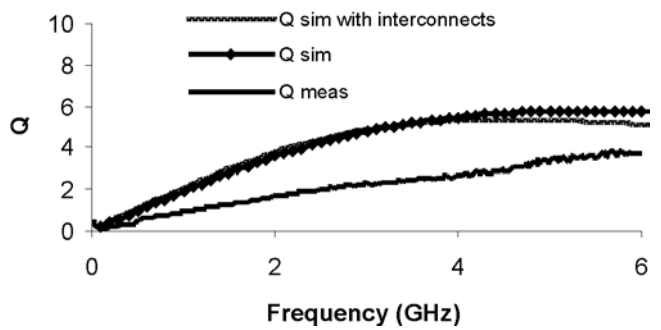

FIGURE 7 Small inductance quality factor.

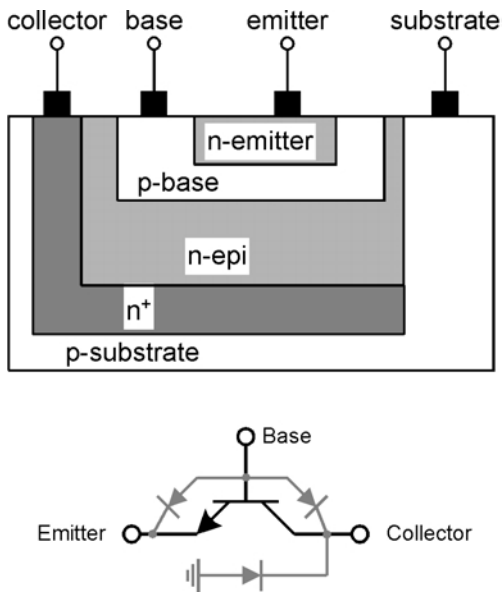

FIGURE 8 Bipolar transistor structure.

The parasitic diode between collector and substrate has an impact to the overall tuning capacitance and should be considered during design phase.

In a CMOS process the p/n junction can be implemented as the junction between the p-substrate and n+ implantation for a grounded diode, or between n-well and p+ implantation for a floating diode, as shown in Figure 9.

In the case of the floating CMOS diode, the parasitic diode between n-well and p-substrate should be taken into account as it is a low-Q diode and forms a parasitic capacitance from cathode to ground.

Figure 10 shows a simplified electrical equivalent for the variable capacitor, where C_j is the junction capacitance, R_p the equivalent resistance of the recombination and surface current, R_s the series parasitic resistance and L the series parasitic inductance of interconnections. C_j is given as $C_j = C_{j0}/(1 - V_R/\phi)^m$ where V_R is the reverse bias voltage, C_{j0} the capacitance at zero bias, and ϕ, m constants that depend on technology and diode structure [26, 27].

At high frequencies considered here, the effect of resistance R_p is not taken into account, since it is shunted by the junction capacitance C_j. The effect of R_s dominates and the quality factor of the reverse biased diode is computed as $Q \approx 1/\omega R_s C_j$. The simplified variable capacitor model of Figure 10 can be used for hand calculations during resonator design. For a given frequency and geometry of the diode, the quality factor depends on the reverse

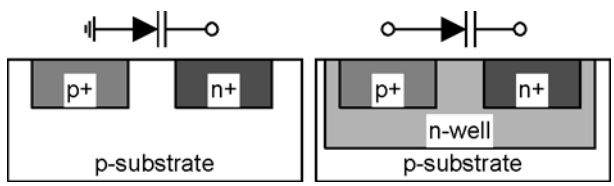

FIGURE 9 CMOS varactor implementations.

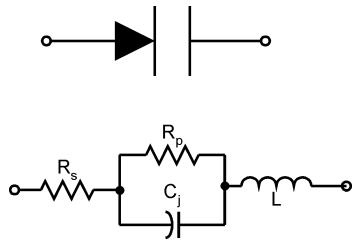

FIGURE 10 Varactor simplified electrical model.

bias voltage. As the reverse bias voltage increases, both the junction capacitance C_j and series resistance R_s decrease and quality factor increases.

The basic loss mechanism is the ohmic resistance of the p- and n-silicon areas that form the diode. Changing the geometrical dimensions can reduce the resistance of the silicon areas. Figure 11 shows the top and cross-section of a floating p/n junction. If we design the diode to be short, *e.g.* with x as the minimum dimension allowed by the technology, then the horizontal resistance between anode and cathode is minimized. The vertical dimension can be larger than the minimum allowed by the technology, but not very large because the resistance of metal interconnections increases the diode series resistance. The structure in Figure 11 can be used as a unit variable capacitor. To further reduce overall diode resistance many unit structures can be connected in parallel. However, as more structures are connected the parasitic capacitance to ground increases, altering overall tuning capacitance and oscillation frequency.

Figure 13 shows measurement results for a floating CMOS varactor. The structure is laid out in interdigitized form of p^+ and n^+ regions, as shown in Figure 12. The diode structure is designed in AMS's 0.8 μm HBT BiCMOS process. The capacitance is computed from S_{11} and S_{22} parameters as the imaginary part of the input impedance evaluated at 6 GHz. Port1 is connected to the anode and Port2 to the cathode of the diode. The difference in capacitance between Port1 and Port2 demonstrates the influence the parasitic diode has to the overall tuning capacitance.

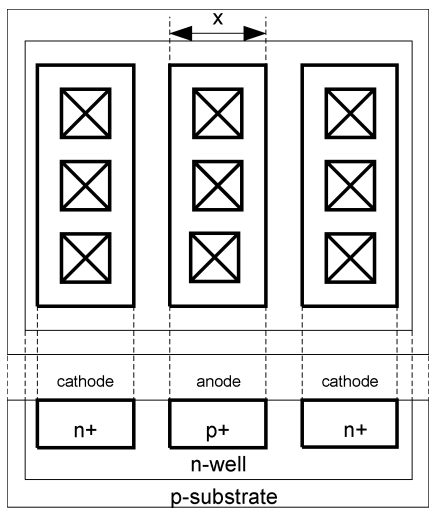

FIGURE 11 p/n junction cross-section.

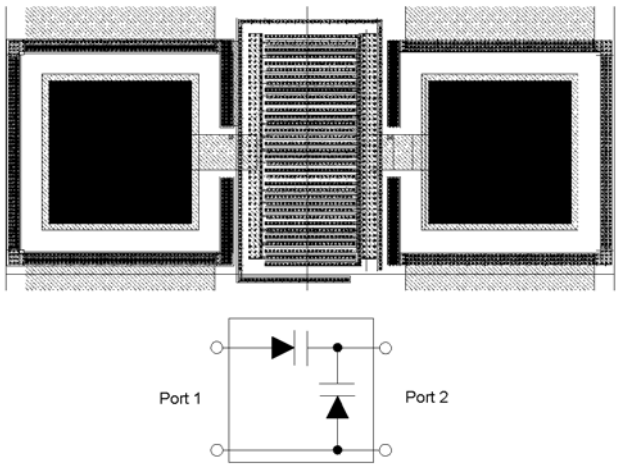

FIGURE 12 Floating varactor design example.

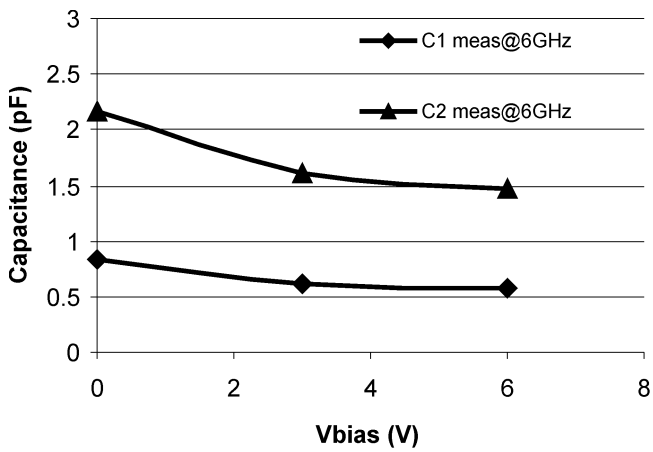

FIGURE 13 Varactor measurement results.

3 RESONATOR DESIGN

The resonator is the passive circuit that determines the oscillation frequency. It is formed by the series or parallel connection of an inductor and a variable capacitor. In this paper we will consider the parallel connection, as it is the appropriate configuration for differential pair VCO circuits. In the following we will extract expressions that relate the tank quality factor with the inductance L, capacitance C and their respective series ohmic losses R_{SL} and R_{SC}. We will use the equivalent circuits from Figure 4 and Figure 10. To facilitate calculations we can transform each passive component, L and C, along with their series ohmic losses to their equivalent parallels as shown in Figure 14.

For the inductor we have:

$$R_{PL} = R_{SL}\left[1 + \left(\frac{\omega L}{R_{SL}}\right)^2\right],\ L' = \frac{R_{SL}^2 + (\omega L)^2}{\omega^2 L} \tag{1}$$

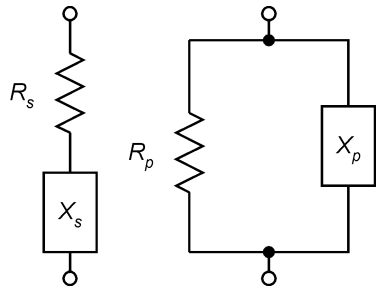

FIGURE 14 Series to parallel impedance conversion.

For the capacitor we have:

$$R_{\mathrm{PC}} = R_{\mathrm{SC}}\left[1 + \left(\frac{1}{\omega R_{\mathrm{SC}} C}\right)^2\right], \quad C' = \frac{C}{1 + (\omega R_{\mathrm{SC}} C)^2} \tag{2}$$

where $L(C)$ and $L'(C')$ are the inductance (capacitance) of the series and parallel equivalent impedances respectively. We can compute the resonance frequency and equivalent parallel resistance of the resonator as:

$$\omega_0 = \frac{\sqrt{CL(L - CR_{\mathrm{sC}}^2)(L - CR_{\mathrm{sL}}^2)}}{CL^2 - LC^2R_{\mathrm{SC}}^2}, \quad R_p = \frac{L + R_{\mathrm{SC}}R_{\mathrm{SL}}C}{C[R_{\mathrm{SC}} + R_{\mathrm{SL}}]} \tag{3}$$

R_p is a measure of the resonator quality factor. The ideal resonator has no losses and the quality factor and R_p have an infinite value. However, real resonators are lossy and thus have finite R_p. The lower the R_p the lossier the resonator.

The tank impedance as a function of frequency is calculated as:

$$Z_{\mathrm{tank}}(s) = \frac{s/C'}{s^2 + (s/C'R_p) + (1/L'C')} \tag{4}$$

It has the band-pass form of

$$\frac{As}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{5}$$

Where

$$\omega_0 = \frac{1}{\sqrt{L'C'}} \quad \text{and} \quad Q = \omega_0 C' R_p = \sqrt{\frac{C'}{L'}}R_p \tag{6}$$

Substituting C', L' and R_p with their equivalents from Eqs. (1) and (2) we get

$$Q_{\mathrm{tank}} \approx \sqrt{\frac{L}{C}}\frac{1}{R_{\mathrm{SL}} + R_{\mathrm{SC}}} \tag{7}$$

To increase resonator quality factor passive devices with high quality factors should be used so as to reduce R_{SL} and R_{SC} as much as possible. However, fabrication technology poses a limitation to the maximum quality factor. A high inductance should also be used in order to increase the nominator of Eq. (7). To keep the resonance frequency constant the tuning capacitance should be decreased. As the tuning range of the resonator depends on the capacitance value range, by decreasing the tuning capacitance the tuning range also decreases. There is a trade-off between the required tuning range and the maximum resonator quality factor we can achieve by increasing the inductance.

Although the above hand calculations are simple, they provide a rough estimate on the performance of the VCO. Accurate results will be obtained through simulations with SPICE-like simulators, like SpectreRF, where more complex models are available for the junction diode and the active devices of the oscillator.

For the parallel resonator considered in this work, there are three basic different configurations, as shown in Figure 15.

In Figure 15(a, b) the tuning voltage is applied to the varactor through the bias resistor R_B and inductor L. The series capacitor C_s isolates the varactor from the inductor and the negative terminal of the tuning voltage. Usually it is implemented as a low-loss MIM capacitor. The parallel capacitance C_P is always present and represents the wiring and inductor parasitic capacitance. For high frequency signals the biasing resistor of Figure 15(a) is transformed into the resonant circuit as an additional equivalent shunt resistance R_c. The value of R_c is given from Eq. (8):

$$R_c = R_B\left(1 + \frac{C_s}{C_{\text{var}}}\right)^2 \tag{8}$$

In the case of Figure 15(b) the equivalent resistance R_c becomes:

$$R_c = R_B\left(1 + \frac{C_{\text{var}}}{C_s}\right)^2 \tag{9}$$

By comparing the above two equations, the influence of bias resistor R_B in Figure 15(b) is larger than that in Figure 15(a), provided that $C_s C_{\text{var}}$. The disadvantage of the configurations in Figure 15(a, b) is that the influence of the biasing resistor R_B depends on C_{var} and is a function of the tuning voltage.

In Figure 15(c) the resonant circuit is tuned using two varactor diodes. For tuning purposes the two varactors are connected in parallel and have the same capacitance value. For high frequency signals they are connected in series. This topology has the advantage that the

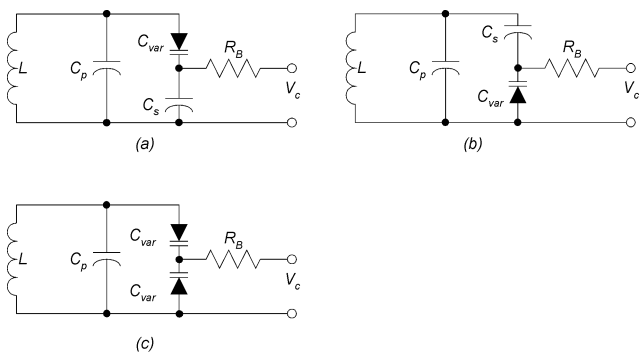

FIGURE 15 Parallel resonator topologies.

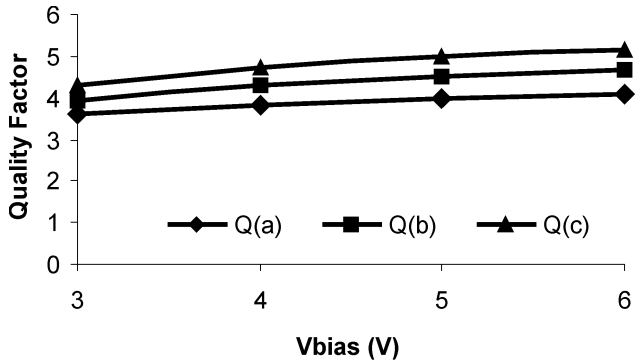

FIGURE 16 Different resonator configurations: quality factor.

capacitance shift caused by the oscillator signal takes effect in opposite directions for the two diodes and therefore cancels itself. The capacitance shift cancellation provides a resonance frequency that is more stable with respect to the oscillator signal. The bias resistor is transformed into the circuit as a constant resistance throughout the whole tuning range with value $R_c = 4R_B$.

Figure 16 shows the simulated quality factor for the three resonator configurations of Figure 15. The inductor is the one presented in Figure 6. The varactors are the ones presented in Figure 13 and the fixed capacitor is 5 pF with no losses. The biasing resistor is 1K. The Q for each resonator is calculated as $Q = \pi f_0 \tau_d$ where τ_d is the group delay of the resonator and f_0 the frequency where group delay is maximized. Q is simulated as follows.

The resonator impedance can be rewritten in the form of

$$\frac{1}{1 + jQ(\omega/\omega_0 - \omega_0/\omega)} \tag{10}$$

Its phase is

$$\phi(\omega) = a\tan(Q\omega_0/\omega - Q\omega/\omega_0) \tag{11}$$

The group delay is computed as

$$\tau_d(\omega) = -\frac{\partial\phi(\omega)}{\partial\omega} = \frac{Q/\omega_0 + Q\omega_0/\omega^2}{1 + (Q(\omega_0/\omega) - Q(\omega/\omega_0))^2} \tag{12}$$

At the resonance frequency the group delay and the quality factor are calculated as $\tau_d = 2Q/\omega_0 \Rightarrow Q = f_0\tau_d$.

From the simulation results is evident that the configuration of Figure 15(c) exhibits higher quality factor than the other two, as it was expected from the previous analysis. The inductor Q dominates the resonator Q and that explains the small differences between the three resonator configurations.

4 SUMMARY

In this paper the issue of on-chip passive device design has been addressed. High quality inductor implementation is a challenge and at high frequencies interconnections should be carefully considered as they significantly influence the overall inductance. Although p/n

junctions used as variable capacitors have superior quality factors compared to inductors, as we move to higher frequencies of operation their Qs decrease and can become comparable to inductor Qs. For high performance VCOs passive components with low losses are required. Advances in silicon technologies are believed to be able to provide the necessary passive devices for high performance fully integrated VCO designs.

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