EPJ Web of Conferences **79**, 01004 (2014)
DOI: 10.1051/epjconf/20147901004

Silicon heterojunction metal wrap through solar cells – a 3D TCAD simulation study

I. Dirnstorfer[1,a], D.K. Simon[1], B. Leszczynska[2] and T. Mikolajick[1,2]

[1] NaMLab gGmbH, Nöthnitzer Str. 64, 01187 Dresden, Germany
[2] Institute for Semiconductor and Microsystems Technology, TU Dresden, 01062 Dresden, Germany

Abstract. Silicon heterojunction metal wrap through solar cells have the potential for high efficiencies in a simple process flow. However, the non-conformal deposition of the hydrogenated amorphous silicon emitter causes specific loss mechanisms of this cell concept. The emitter does not fully cover the inner via surface. As a consequence, the via surface is not passivated and the via metallization is in electrical contact with the silicon base. The resulting loss processes are determined in 3D TCAD simulations. While via related recombination losses are negligible even for highest surface recombination velocities, the resistive losses are found to be critical. The limit for the contact resistance between via metallization and silicon is in the range of 1 $\Omega\,cm^2$, depending on substrate doping and via diameter. Below this value, the cell performance significantly degrades. Finally, three different approaches for novel SHJ-MWT solar cells are discussed.

1. Introduction

Silicon heterojunction (SHJ) solar cells based on hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si) achieve excellent efficiencies of up to 24.7% in a simple low-temperature process scheme [1]. However, optical losses due to front side metallization are still limiting the cell performance. One concept to reduce the shaded area is the connection of the front contact through vias to the wafer back side. In this metal wrap through (MWT) concept, both electrical contacts are at the rear side of the cell [2]. The combination of both concepts to a SHJ-MWT solar cell seems very attractive; however, the realization of this combined concept has not been reported so far.

The MWT concept has been intensively investigated for silicon homojunction cells. The reduced front side shading is the main advantage of MWT solar cells resulting in an additional photocurrent of about 3% and a slight increase of the open circuit voltage. However, these advantages are partly compensated by resistive losses, which lead to a reduced fill factor (FF) in MWT cells. These losses are caused by the arrangement of the vias and metal base contacts (Fig. 1a). Due to the spacing between the base contacts, photo-generated majority carriers move laterally towards the base contacts. This induces an additional contribution to the series resistance. Furthermore, the position and the surface recombination velocity of the rear contact insulation (RCI) have a negative influence on the FF. In the conventional MWT concept, the via metallisation and the silicon base are insulated by a

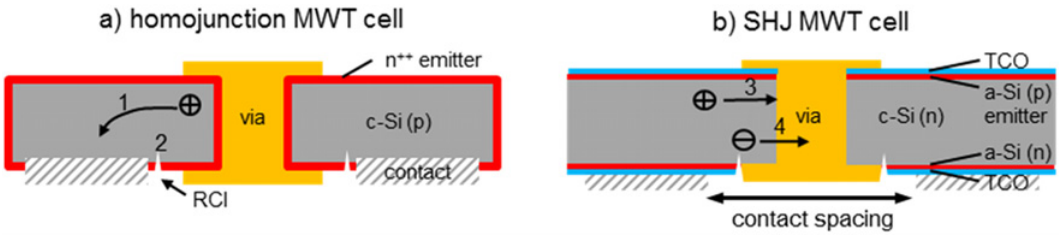

Figure 1. Loss mechanisms in MWT cells: In homojunction MWT cells (a) the lateral current towards the base contacts (1) and losses at the RCI (2) are critical. In SHJ-MWT cells (b) additional loss mechanisms are caused by via surface recombination (3) and via-base leakage (4).

Table 1. Input parameters used for TCAD simulations. Defect state distributions in a-Si:H denote for acceptor- (A) and donor- (D) like states.

	c-Si base	**a-Si:H emitter**
Thickness [μm]	150	0.015
Band gap [eV]	1.17	1.72
Electron affinity [eV]	4.05	3.9
Doping concentration [cm^{-3}] / type	10^{16} / n	10^{20} / p
Mid gap defects: density [$cm^{-3}eV^{-3}$], position [eV], width [eV]	–	10^{19}/1.2/0.21 (A) 10^{19}/1.1/0.21 (D)
Bandtails: density [cm^{-3}], Urbach energy [eV]	–	10^{21}/0.08 (A) 10^{21}/0.12 (D)

conformal emitter layer, which is typically formed in a $POCl_3$ diffusion process. Therefore, resistive and recombination losses within the via are negligible [3–5].

SHJ solar cells base on a a-Si:H emitter, which is grown in a plasma enhanced chemical vapour deposition (PECVD) process. In contrast to diffused emitters, a-Si:H is deposited non-conformal, i.e. it does not cover the via surface (Fig. 1b). As a consequence, the via metallization directly contacts the silicon base in the SHJ-MWT cell. This induces additional loss mechanisms, which are specific for MWT concepts without emitter in the vias. The electrical contact between via metallization and silicon causes an electron shunt current in the cell, which is termed via-gate leakage for simplicity. Additionally, the unpassivated via surface acts as recombination sink for minority carriers and causes a hole diffusion current towards the via [6]. The purpose of this work is to model these additional loss processes using 3D simulations and to define material specifications for SHJ-MWT solar cells.

2. Simulation methodology

Numerical simulations in 3D were done with the TCAD device simulator from Synopsys. The *pn*-junction based on a *n*-type crystalline silicon wafer with a *p*-type a-Si:H emitter (Table 1). The material parameters of a-Si:H, such as band gap, energy distribution of the exponential band tails and Gaussian distribution of mid-gap trap states, were chosen in accordance to other simulation studies [7, 8]. The values were fine tuned to fit the band alignment and the electrical characteristics of SHJ solar cells (Table 2).

A continuous bus bar cell architecture [2, 4] with a front grid line spacing of 3 mm and 3 rear bus bars was assumed. The simulated cell geometry is shown in Fig. 2. The distance between the base contacts (contact spacing) was 2 mm throughout this work. Each grid line is contacted through vias to each rear bus bar. Assuming a total cell size of $156 \cdot 156\,mm^2$, the total number of vias was 156. Since the via

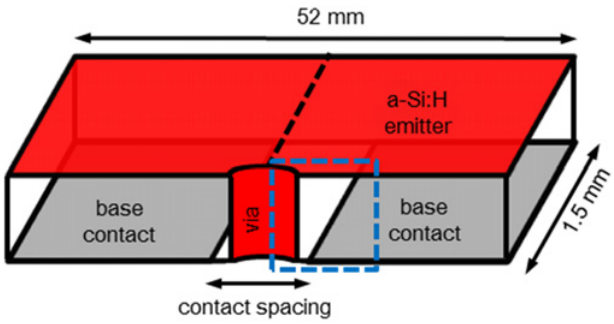

Figure 2. Cell geometry for 3D-simulation. The results are presented as 2D slices through the via (dashed area).

related losses scale with the via density, this study is very conservative. The alternative point bus bar concept [9] requires only 16 vias. In the point bus bar concept the via-related losses are smaller.

Three electrical contacts were defined. Emitter and the via contacts were on same potential. The via contact resistance was varied in the range of 0.01 to 10 $\Omega\,cm^2$ to simulate the via-base leakage. The via surface recombination velocity was varied in the range of zero to 10^7 cm/s to simulate via related recombination. By setting the via surface as an electrode, the via bulk resistance was zero by definition. This is in good agreement with the experimental results, which show that the via resistance is negligible for good via pastes [10]. The base contact was kept at zero potential during simulation. The rear bus bar metallization was not considered in this study.

For simplicity, only the surface recombination at the via was modelled; all other surfaces were considered to be perfectly passivated. However, the model considered Auger and doping dependent Shockley-Read-Hall (SRH) recombination with a maximum minority carrier lifetime of 1 ms in the c-Si bulk. The calculation based on the conventional diffusion-drift model with thermionic emission to correctly model the transport mechanism at the abrupt heterointerfaces. The device characteristic was calculated in a quasistationary ramp from zero to open circuit voltage.

3. Results and discussion

This study assumes a non-conformal growth of the a-Si:H emitter, which does not electrically insulate the via surface in SHJ-MWT solar cells. To confirm this assumption, a 550 nm thick layer of a-Si:H was deposited on a silicon wafer with laser drilled vias. After deposition the cross-section of the via was inspected with scanning electron microscopy (SEM). Fig. 3 shows that the a-Si:H thickness already decreased to 50% at the via top. At mid position of the via the thickness reduced to 20% and at via bottom the thickness was below detection limit. Since a typical emitter thickness is 15 nm only, it can be expected that the deposition in the via is not sufficient to suppress the via-base leakage.

Figure 4 shows the electrical current distributions for different via-base contact resistances. The current density close to the base contact was about 35 mA/cm^2, which was the average cell current density at the point of operation. In the area between via and base contact, the current density increased due to the lateral flow of photogenerated majority carriers either towards the base contact or the via surface.

For infinite via-base resistance, all photogenerated electrons were collected at the base contact. The lateral current density mainly depended on the contact spacing and wafer resistivity. An analytical expression for the additional cell serial resistance is given in reference [5]. However, for contact resistance values below 10 $\Omega\,cm^2$, an additional electron current from the silicon base to the via metallization appeared, which was in competition to the electron collection at the base contact. The

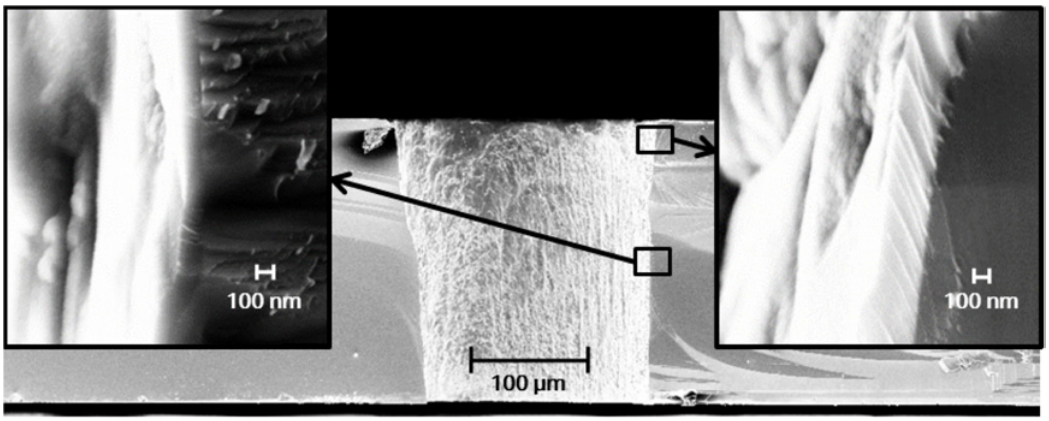

Figure 3. SEM cross-section through a via after deposition of 550 nm a-Si:H in a PECVD process. The a-Si:H thickness is 300 nm at via top (right) and below 100 nm at the via mid-position (left), respectively.

simulation showed separated collection areas of the via and the base contact, respectively. At the border line, the current density became minimum. The electron collection length of the via was 300, 850 and 1400 μm, for contact resistance values of 3, 1 and 0.1 $\Omega\,cm^2$, respectively.

The plotted current density is the sum of electron and hole currents. However, light absorption and generation of electron hole pairs mainly occur in the front part of the cell. Photogenerated holes only travel a short distance towards the emitter. Electrons travel to the rear side of the wafer and in lateral direction towards the base contacts. As a consequence, the total current density in the wafer bulk is mainly caused by electrons and the vectors essentially indicate the electron current in Fig. 4 (conventional current direction).

Figure 5 shows that the cell efficiency deteriorates for smaller via-base resistances and higher via diameters. The via-base leakage mainly impacts the fill factor; open circuit voltage and short circuit current hardly changed. Using this simulation, limits for the required via insulation were defined. Assuming a tolerable fill factor loss of 0.3% and a via with 100 μm diameter, the minimum via-base resistance is 1 $\Omega\,cm^2$. This corresponds to an absolute shunt resistance of 2 kΩ per via or a total cell shunt resistance of 3 k$\Omega\,cm^2$ assuming the cell layout defined in the methodology chapter.

The influence of the via-base leakage also depended on the doping of the silicon substrate (Fig. 6). The simulated values correspond to wafer resistivities between 0.3 and 10 Ω cm. For high via-base contact resistances, a high substrate doping of $>10^{16}\,cm^{-3}$ was beneficial for the MWT-SHJ solar cell. However, for via-base contact resistances below 0.1 $\Omega\,cm^2$, a lower substrate doping became beneficial. The lower doping effectively suppressed the lateral electron shunt current towards the via.

Another loss mechanism is the recombination at the via surface. Figure 7 shows the hole current density at vias with different surface recombination velocities. In the case of negligible recombination (S_{eff}: 0 cm/s), the photogenerated holes travel straight towards the emitter. However, with increasing recombination velocity the carriers also laterally diffuse towards the via. The electrical field of the space charge region and the via recombination centres compete for minority carriers. The simulation showed a diagonal separation line between collection areas of emitter and via, respectively. Though the collection area of the via was not small, the total recombination current was very low. The carrier generation occurred close to the wafer surface and the minorities were mainly collected by the emitter. As a consequence, the efficiency loss due to via recombination was negligible. The simulation showed that vias with 100 μm diameter and a recombination velocity of 10^7 cm/s only reduced the efficiency by 0.02%.

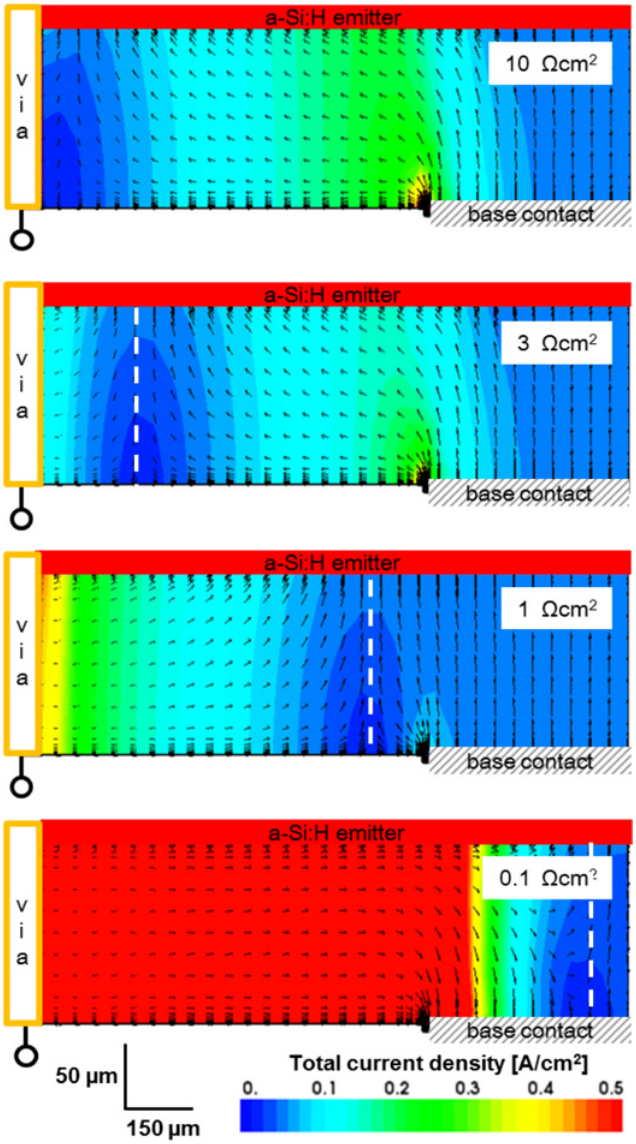

Figure 4. Current densities and vectors for different via-base contact resistances for a 100 μm via at the operation point of the cell (simulated area as indicated in Fig. 2). The vectors point in the direction of the conventional current flow.

4. Discussion

According to simulation, the via-base leakage becomes the limiting factor of the cell efficiency if the contact resistance comes below a limit of 1 $\Omega\,\mathrm{cm}^2$. Since the resistance of "good" metal-semiconductor contact is in the order of 0.001 $\Omega\,\mathrm{cm}^2$, the via-base leakage has to be considered in the cell design. Wu et al. suggested to electrically insulate the via by a local deposition of a-Si:H or SiN_x [11] . However, this insulation involves additional process steps for masking and back etching and a low-cost implementation seems challenging. Another possibility is the application of selective via pastes, as

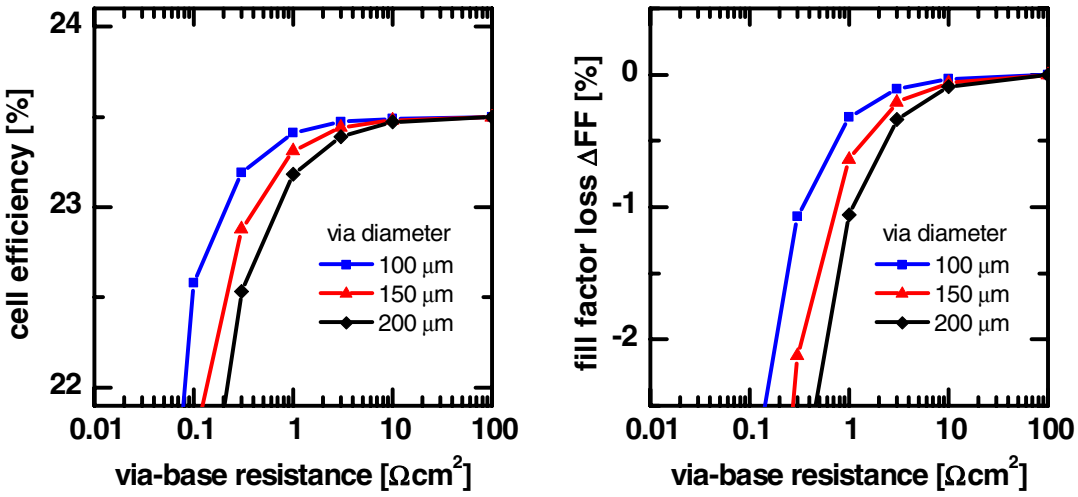

Figure 5. Simulated solar cell efficiencies and FF for different via-base resistances and different via diameters. Below 1 $\Omega\,cm^2$, the cell performance drastically decreases.

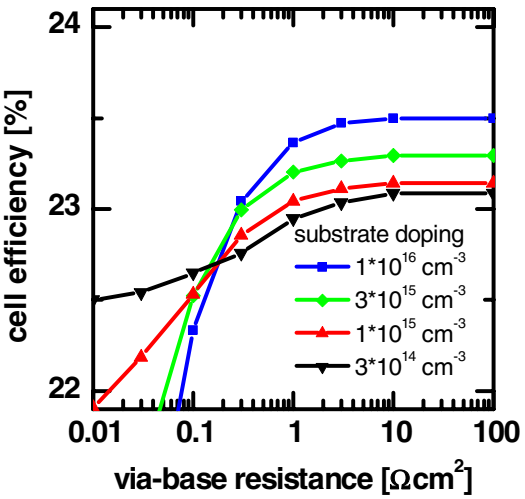

Figure 6. Simulated solar cell efficiencies for different via-base resistances and different substrate doping levels. The influence of the via-base leakage decreased for lower substrate doping.

it was suggested for the MWT-HIP+ solar cell concept [12]. The applied pastes showed low contact resistance on the highly doped emitter and sufficient insulation to high ohmic silicon base. The SHJ-MWT concept requires a novel paste, which selectively contacts TCO and insulates the silicon base. Furthermore, this novel paste has to comply with the SHJ low temperature process scheme. Another option to realize SHJ-MWT solar cells is to change the conventional front junction design to a back junction design, where the emitter is located at the wafer back side [6]. In this cell design, the via metallization contacts the silicon base at the wafer front side and in the via. Via-base leakage does not occur. The electrical contact between via metallization and rear contact through the rear emitter could be insulated with conventional RCI [6].

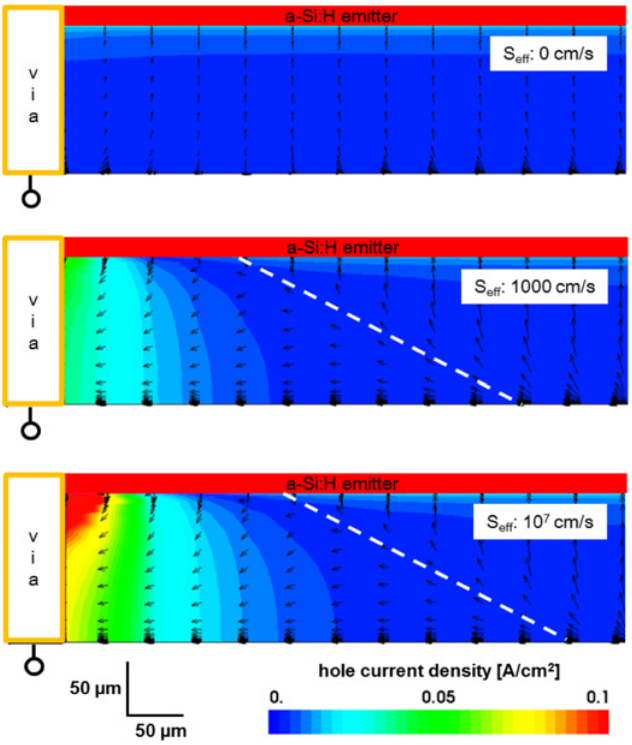

Figure 7. Hole current densities and vectors for different via surface recombination velocities for a 100 μm via at the operation point of the cell. The vectors point in the direction of the conventional current flow.

5. Summary

The combination of SHJ solar cells with MWT metallization is a very promising strategy to exceed today's efficiency values. However, the SHJ-MWT cells have additional loss mechanisms compared to the standard homojunction MWT cells. These loss mechanisms are related to the non-conformal a-Si:H deposition during the PECVD process. As a consequence, the via is neither insulated nor passivated, which causes resistive and recombination losses. While recombination losses were negligible even for highest surface recombination velocities, the resistive losses were found to be critical. A limit of 1 $\Omega\,\mathrm{cm}^2$ was defined for the via-base contact resistance. A lower contact resistance caused a significant degradation of the FF and the cell efficiency. Finally, three different approaches for novel SHJ-MWT solar cells were discussed: a concept with local via insulation, a concept involving selective via metallization and a back junction concept with rear emitter and RCI insulation.

C. Richter is acknowledged for processing the laser vias. This work was supported by the Federal Ministry of Education and Research BMBF (FKZ 03SF0420A).

References

[1] M. Taguchi, A. Vano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, *Proc. PVSC 39th IEEE*, p. 827, 2013

[2] F. Clement, M. Menkoe, R. Hoenig, J. Haunschild, D. Biro, R. Preu, D. Lahmer, J. Lossen, and H.-J. Krokoszinski, *Proc. PVSC 34th IEEE*, p. 223, 2009

[3] T. Fellmeth, K. Meyer, J. Greulich, F. Clement, B. Biro, R. Preu, M. Menkoe, D. Lahmer, and H.-J. Krokoszinski, *Proc 25th PVSEC*, p. 2201, 2010
[4] P. Magnone, D. Tonini, R. De Rose, M. Frei, F. Crupi, E. Sangiorgi, and C. Fiegna, *IEEE J. Photovoltaics*, p. 1, 2013
[5] B. Thaidigsmann, J. Greulich, E. Lohmüller, S. Schmeißer, F. Clement, A. Wolf, D. Biro, and R. Preu, *Sol. Energy Mater. Sol. Cells*, **106**, p. 89, 2012
[6] I. Dirnstorfer, F. Benner, D. K. Simon, T. Mikolajick, N. Schilling, and U. Klotzbach, *Proc. 28th PVSEC*, p. 1108, 2013
[7] R. Stangl, C. Leendertz, and J. Haschke, "Numerical Simulation of Solar Cells and Solar Cell Characterization Methods: the Open-Source on Demand Program AFORS-HET", in *InTech e-book: "SolarEnergy"*, p. 432, 2010
[8] M. Lu, U. Das, S. Bowden, S. Hegedus, and R. Birkmir, *Proc. PVSC 34th IEEE*, p. 001475, 2009
[9] M. W. P. E. Lamers, C. Tjengdrawira, M. Koppes, I. J. Bennett, E. E. Bende, T. P. Visser, E. Kossen, B. Brockholz, A. A. Mewe, I. G. Romijn, E. Sauar, L. Carnel, S. Julsrud, T. Naas, P. C. de Jong and A. W. Weeber, Prog. Photovolt: Res. Appl. **20**, p. 62, 2012
[10] E. Lohmüller, B. Thaidigsmann, S. Werner, F. Clement, A. Wolf, D. Biro, and R. Preu, *Proc 27th PVSEC*, p. 590, 2012
[11] D.-C. Wu, J.-C. Shiao, C.-H. Chen, C.-C. Lin, C.-H. Lin, W.-H. Lu, and C.-L. Chen, 2011, *Proc. PVSC 37th IEEE*, p. 1515, 2011
[12] B. Thaidigsmann, M. Hendrichs, S. Nold, E. Lohmüller, A. Wolf, F. Clement, D. Biro, and R. Preu, *Proc. 28th PVSEC*, p. 1099, 2013