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Spot Defect Diagnosis in Analog Nonlinear Circuits with Possible Multiple Operating Points

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Abstract The paper is focused on local spot defect diagnosis in nonlinear analog integrated circuits. The defects are simulated by finite resistors, high in the case of open and low in the case of short. A diagnostic method that allows detecting, locating, and estimating the value of the defect is developed. The method employs the simulation before test approach leading to a fault dictionary and brings a procedure for locating the defect and estimating its value, on the basis of some quantities measured during the diagnostic test. Because the nonlinear circuit under test may have multiple operating points, even if the fault-free circuit has a unique solution, building the fault dictionary requires a special approach. It is based on some families of characteristics, expressing the resistances that simulate the defects in terms of several voltages, taking into account the deviations of the fault-free parameters within their tolerance ranges. To illustrate the proposed approach two numerical examples are given.

Keywords Analog circuits · Fault diagnosis · Nonlinear circuits · Spot defects

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1 Introduction

Fault diagnosis of electronic circuits is an essential area of scientific research. Although the question has been of considerable interest during the past decades [1, 2, 5, 6, 8–16, 18–20, 22, 23, 25–28] there is no all-purpose procedure for fault diagnosis of analog circuits. The problem is difficult because in modern fabrication process only a limited number of nodes is accessible for measurement and excitation, the values of fault-free elements are scattered within their tolerance ranges and some circuit elements may form ambiguity groups. Much works in this area exploit heuristic methods, artificial neural networks, evolutionary techniques, support vector machines, and elements of fuzzy logic [1, 2, 6, 8, 12, 15]. Some researches concentrate on self-testing of analog circuitry of mixed-signal systems using built-in self test blocks, e.g., [5].

Most physical failures (80–90)% in ICs are local spot defects, opens and shorts [11, 12, 28]. They are caused by major structural deformation and can result in unexpected failures in further processing or during customer usage. In BJT and MOS transistors shorts dominate opens, (70–80)% of failures are shorts and (10–20)% are opens. Opens and shorts called hard faults are extreme cases of large increase or decrease of the nominal values which occur in actual ICs. The real open fault can be simulated by a high resistance (e.g., 100 kΩ–10 MΩ) connected in series with the component or the path. The real short fault can be simulated by a low resistance (e.g., 10 Ω–10 kΩ) connected between a pair of nodes. Such soft spot defects are considered in this paper. The main purpose of the work is to develop a method that allows detecting and locating these defects as well as evaluating their values.

The diagnostic method is classified as the simulation-after test (SAT) approach if most of circuit simulations take place after any testing. Otherwise, the method is classified as the simulation-before test (SBT) approach. In the last case the

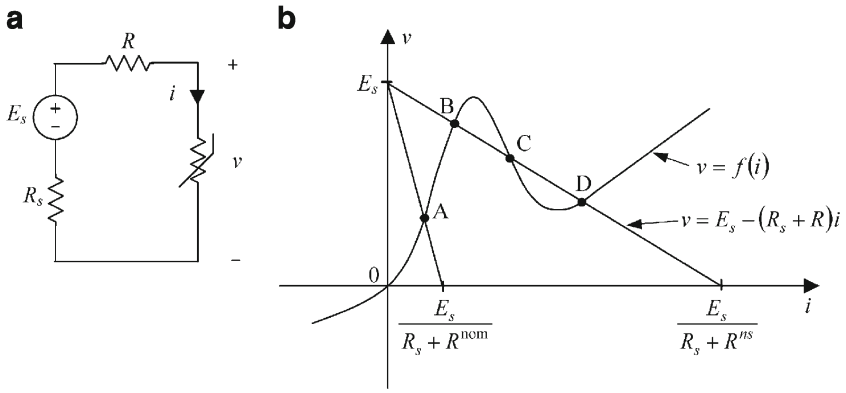

Fig. 1 An exemplary nonlinear circuit (**a**) and graphical analysis of this circuit (**b**)

results of circuit simulations are stored as patterns in a fault dictionary, e.g., [10, 14, 19, 27]. By comparing some quantities, obtained on the basis of measurement, with the patterns contained in the dictionary the fault can be located and identified. During the last decades many tools have been used to build and exploit fault dictionary, e.g., sensitivity analysis [14], neural networks [1, 2], and the Householder formula in matrix theory [22].

If the circuit under test has multiple DC operating points the tested output voltage or current may assume different values for a fixed value of the input voltage. The question which of the possible values actually occurs depends on the transient state which precedes the DC steady state. Since it is unknown, all the operating points should be considered during fault diagnosis. Reference [27] is the only work in the area of the fault diagnosis of the analog circuits having multiple DC operating points. The problem is essential because even if the fault-free circuit has a unique DC operating point, the faulty circuit may have multiple operating points [27]. Therefore, the diagnostic method should take this fact into account.

This paper is devoted to soft spot defects and offers a SBT method for their diagnosis in nonlinear DC circuits, with the special attention paid to bipolar and CMOS circuits, which may have multiple DC operating points. It allows detecting and locating a fault, simulated by a resistor, as well as evaluating its value. The fault dictionary is proposed, built on the basis of families of parametric characteristics that express resistances of the resistors in terms of some output voltages. In addition, a procedure that locates the defect and estimates its value is developed.

2 The Main Idea

The crucial point of the fault diagnosis method developed in this paper is tracing a parametric characteristic that expresses the tested defect, simulated by a resistance, in terms of an output voltage between a pair of nodes or a current flowing through a branch, accessible for measurement. This is a difficult problem because the characteristic can be very complex, due to the fact that the nonlinear circuit may have multiple operating points (DC solutions), even if the fault-free circuit has a unique solution. The problem is explained in Fig. 1.

Let us consider the nonlinear circuit shown in Fig. 1a, where the nonlinear resistor is specified by the function

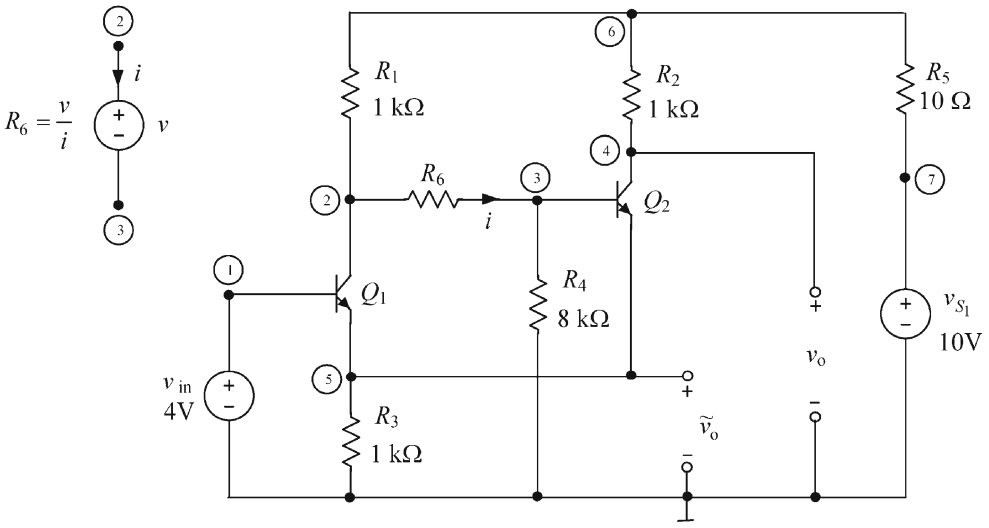

Fig. 2 An exemplary circuit

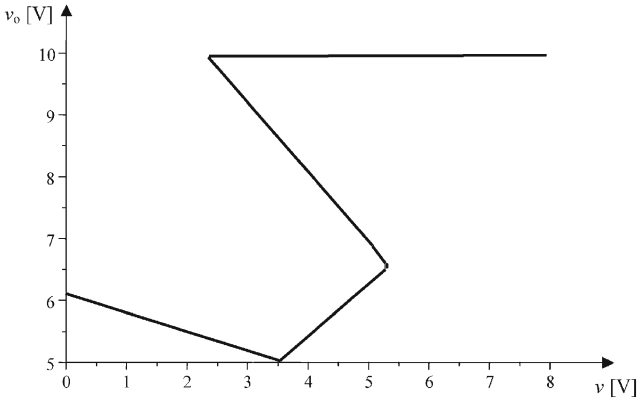

Fig. 3 Transfer characteristic $v-v_o$

$v=f(i)$ having graphical representation shown in Fig. 1b. The circuit can be described by the set of equations

$$\begin{aligned} v &= f(i) \ , \\ v &= E_s - (R_s + R)i. \end{aligned} \tag{1}$$

To solve this system of equations the load-line method is used as depicted in Fig. 1b. If R is nominal, $R=R^{\text{nom}}$, there exists one point of intersection of the straight line $v=E_s-(R_s+R)i$ and the curve $v=f(i)$, which means that the circuit has a unique DC solution (point A). However, if the resistor is near-short $R=R^{ns} \ll R^{\text{nom}}$, three points of intersection exist and the circuit has three DC solutions (points B, C, and D).

If the circuit has multiple DC solutions the input and transfer characteristics may be multivalued, in consequence, the parametric characteristics can be very complex and difficult to trace. For example in the circuit shown in Fig. 2 where the transistor parameters are as described in Example 1 (Section 5), the characteristics $v-v_o$, $v-i$ are depicted in Figs. 3 and 4. They are traced by replacing resistor R_6 with the voltage source v (see Fig. 2).

The parametric characteristic v_o-R_6, shown in Fig. 5, can be traced using the brute-force approach. For each chosen value of the resistance R_6 a very sophisticated method is used to find the corresponding values of v_o. In consequence, the computation process is very time consuming and the approach is efficient in the case of simple circuits only. On the other hand the SPICE simulator applied to trace a parametric characteristic usually loses some of its fragments and gives incorrect characteristic. This is illustrated in Fig. 6, that shows a deformed characteristic v_o-R_6 provided by SPICE.

In this paper we propose to trace the parametric characteristic $R=f(v_o)$ using the following approach. We extract from the circuit the tested resistor R and the pair of nodes with the output voltage v_o. Next the resistor is replaced by a voltage source v (see Fig. 7). In this circuit we calculate the transfer and input characteristics $v-v_o$ and $v-i$ using a very fast and effective method based on the theory named a linear complementarity problem [4, 7, 24, 27]. During this process v is automatically increased or decreased and for each achieved value of v the attached values v_o and i are found and resistance $R=v/i$ is computed.

As a result a point $(v_o,\ R)$ on the parametric characteristic is obtained. If the characteristic is single-valued, it can be directly used to find resistance R for the measured voltage v_o. Otherwise, if the characteristic is multivalued, several values of the resistor may exist for the measured voltage v_o (see $v_o = \overline{v}$ in Fig. 5). In such a case another voltage $\tilde{v}_o$ is chosen and the characteristic $R=p(v_o,\tilde{v}_o)$ is traced in three-dimension space, which allows finding a unique resistance for the measured voltages v_o and $\tilde{v}_o$. Figure 8 shows the characteristic in the circuit depicted in Fig. 2

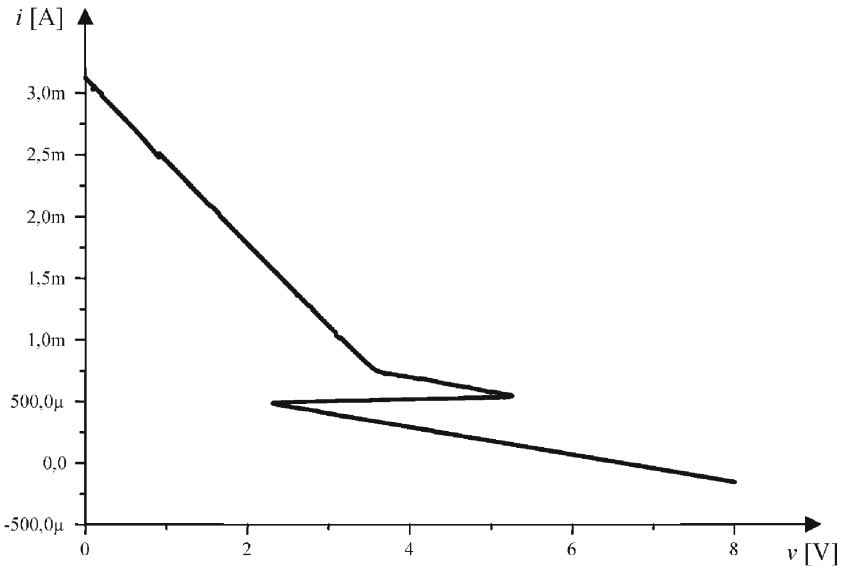

Fig. 4 Input characteristic $v-i$

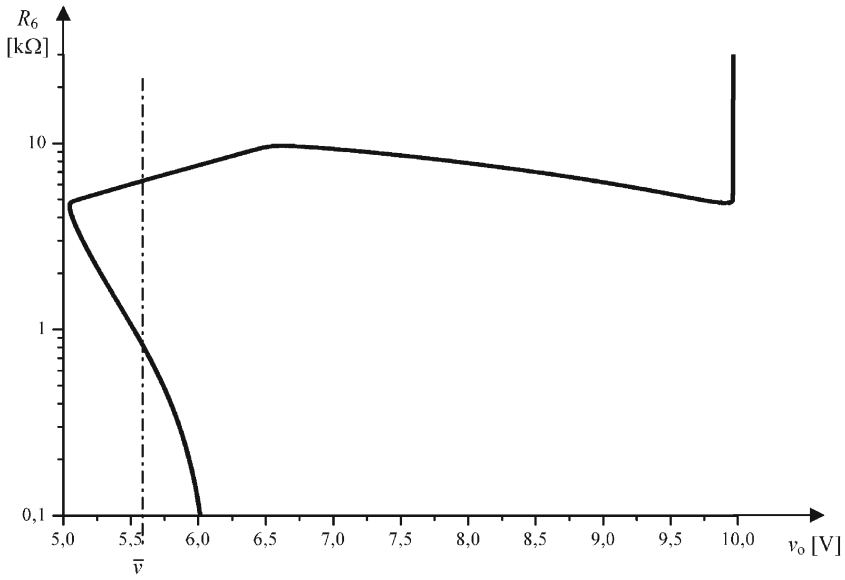

Fig. 5 Parametric characteristic $v_o - R_6$

that allows finding the resistance $R=R_6$ of the faulty resistor. Another characteristic in three-dimension space can be traced using a current flowing through a branch, instead of the voltage $\tilde{v}_o$.

3 Building Fault Dictionary

In this section we consider bipolar and MOS transistor circuits driven by voltage sources. The bipolar transistors will be characterized by the Ebers-Moll model including a pair of diode-controlled source combinations. The voltage–current characteristics of emitter and collector diodes will be approximated by piecewise-linear functions. In such a case each of the diodes can be synthesized using ideal diodes, resistors and voltage sources (see [24, 27]). We introduce this representation into the Ebers-Moll model as shown in Fig. 9. The MOS transistors will be represented by the Shichman-Hodges model built up in Level 1 of SPICE [17]. It can be shown [21, 24, 27] that this model is equivalent to the circuit having similar form as the Ebers-Moll model of bipolar transistors, where α_R and α_F are replaced with $\alpha=1$ and the diodes are described by rather polynomial than exponential functions (see Fig. 15 in reference [24]). The model also includes resistors R_S and R_D. Using the piecewise-linear representation of the diodes, we obtain an MOS transistor model very similar to the circuit shown in Fig. 9.

Let us consider a bipolar or MOS transistor circuit. After replacing all the transistors by the above-described models we obtain the circuit comprising ideal diodes, resistors, current-

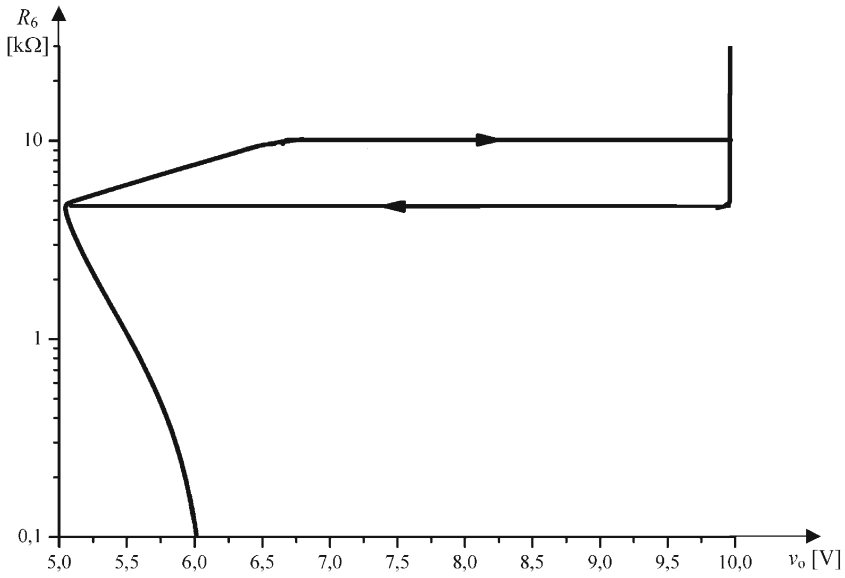

Fig. 6 Deformed parametric characteristic $v_o - R_6$ given by SPICE

Fig. 7 Circuit for tracing the characteristics

controlled current sources and voltage sources. In this circuit we wish to diagnose soft spot defect (soft short or soft open), that is simulated by resistance of the resistor R connected to the circuit.

For this purpose we extract from the circuit all the ideal diodes, the resistor R, the open-circuit branches $(n+2)$, $(n+2)'$ and $(n+3)$, $(n+3)'$ corresponding to voltages v_o and $\tilde{v}_o$. In this way the circuit shown in Fig. 10 is obtained, where the reverse reference direction of the voltages across the ideal diodes is used. Under such convention each ideal diode has the following description

$$i \geq 0, v \geq 0, vi = 0. \tag{2}$$

To describe the circuit shown in Fig. 10 we replace the ideal diodes and the resistor R by voltage sources and connect to terminals $(n+2)$, $(n+2)'$ and $(n+3)$, $(n+3)'$ zero current sources as depicted in Fig. 11.

Let us describe this circuit using the hybrid representation [3]

$$\begin{bmatrix} i_1 \\ \vdots \\ i_n \\ i_{n+1} \\ \hline\hline v_{n+2} \\ \hline\hline v_{n+3} \end{bmatrix} = \boldsymbol{H} \begin{bmatrix} -v_1 \\ \vdots \\ -v_n \\ v_{n+1} \\ \hline\hline i_{n+2} \\ \hline\hline i_{n+3} \end{bmatrix} + \boldsymbol{s}, \tag{3}$$

where $\boldsymbol{H}=[h_{ij}]_{(n+3)\times(n+3)}$ is a hybrid matrix, $\boldsymbol{s}=[s_1 \cdots s_{n+3}]^{\mathrm{T}}$ is a source vector. Equation (3) will be rearranged as follows. Since

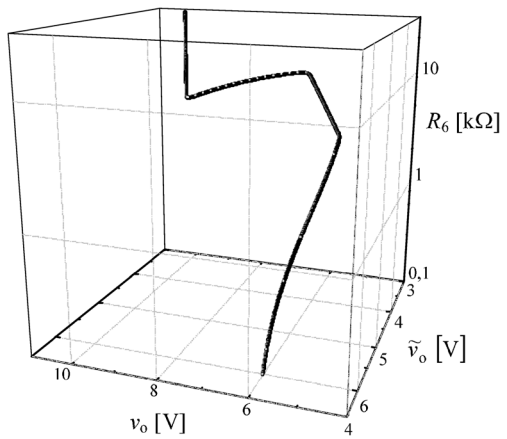

Fig. 8 Characteristic $R_6=p(v_o,\tilde{v}_o)$ in three-dimension space

$i_{n+2}=0$ and $i_{n+3}=0$, the columns $(n+2)$ and $(n+3)$ of matrix $\boldsymbol{H}$ can be removed. On the basis of matrix $\boldsymbol{H}$ the matrix

$$\boldsymbol{M} = -\begin{bmatrix} h_{11} & \cdots & h_{1n} \\ \cdots & \cdots & \cdots \\ h_{n1} & \cdots & h_{nn} \end{bmatrix}$$

is formed. Then the hybrid representation (3) can be rewritten as the set of equations:

$$\boldsymbol{i} = \boldsymbol{M}\boldsymbol{v} + \begin{bmatrix} h_{1,n+1} \\ \vdots \\ h_{n,n+1} \end{bmatrix} y + \begin{bmatrix} s_1 \\ \vdots \\ s_n \end{bmatrix}, \tag{4}$$

$$i_{n+1} = -\left[h_{n+1,1} \cdots h_{n+1,n}\right]\boldsymbol{v} + h_{n+1,n+1}y + s_{n+1}, \tag{5}$$

$$v_{n+2} = -\left[h_{n+2,1} \cdots h_{n+2,n}\right]\boldsymbol{v} + h_{n+2,n+1}y + s_{n+2}, \tag{6}$$

$$v_{n+3} = -\left[h_{n+3,1} \cdots h_{n+3,n}\right]\boldsymbol{v} + h_{n+3,n+1}y + s_{n+3} \tag{7}$$

where $\boldsymbol{i}=[i_1 \cdots i_n]^{\mathrm{T}}$, $\boldsymbol{v}=[v_1 \cdots v_n]^{\mathrm{T}}$, $y=v_{n+1}$. Since i_j is the current and v_j the voltage of j-th ideal diode, then $i_j \geq 0$, $v_j \geq 0$, and $i_j v_j = 0$, $(j=1,\ldots,n)$. In consequence, the following relationships

$$\boldsymbol{i} \geq 0, \boldsymbol{v} \geq 0, \sum_{j=1}^{n} i_j v_j = 0. \tag{8}$$

can be written, where the vector inequalities are meant component-wise. To trace the characteristic $R=p(v_{n+2}, v_{n+3})$ we solve Eq. (4) with constraints (8) for different values of y, using the theory named a linear complementarity problem [4, 7], as described in [27]. During the computation process y is increased or decreased automatically. At an arbitrary k-th step, $y^{(k)}$ and vector $\boldsymbol{v}=\boldsymbol{v}^{(k)}$ are calculated and used to find $i_{n+1}^{(k)}$, $v_{n+2}^{(k)}$, and $v_{n+3}^{(k)}$ employing (5)–(7). On the basis of these results we have $R^{(k)}=y^{(k)}/i_{n+1}^{(k)}$ together with $v_{n+2}^{(k)}$, and $v_{n+3}^{(k)}$. In this way the characteristic that expresses R in terms of v_{n+2} and v_{n+3} is traced. Sometimes v_{n+2} and v_{n+3} are not sufficient to find the unique value of the resistor and an additional voltage accessible for measurement is required. In such a case the characteristic is formed in four-dimension space.

The characteristic allows finding resistance R on the basis of the measured voltages in ideal case when all circuit parameters are nominal and the voltages read in the diagnosis phase are accurate. In real circumstances, however, the fault-free parameters do not stay nominal but are scattered within their tolerance ranges. In consequence, the measured output voltages will differ from the actual ones and the obtained results will be uncertain. To adapt the method to realistic framework a family of characteristics should be traced, considering the deviations of the fault-free parameters from nominal values.

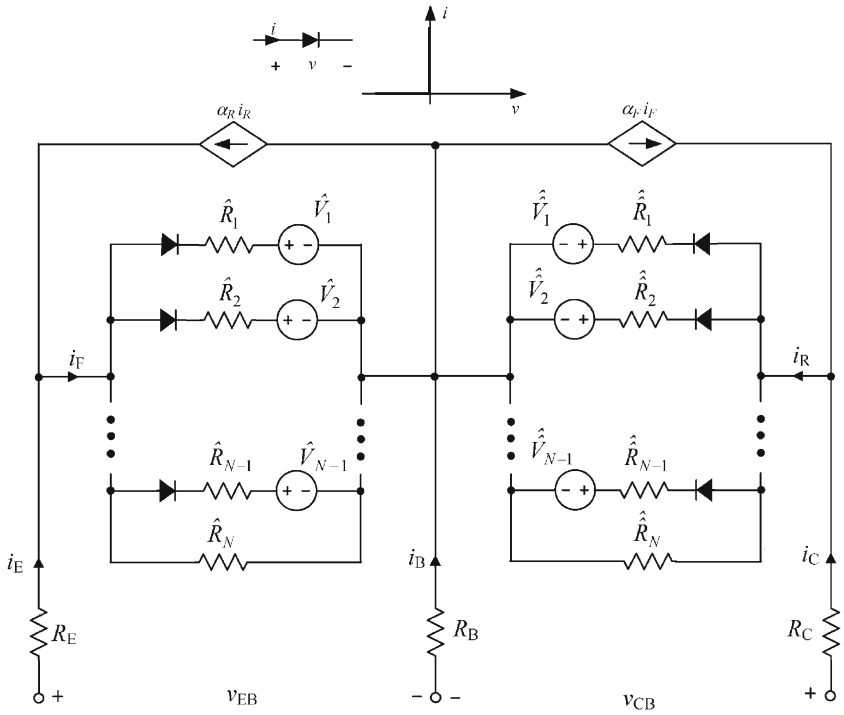

Fig. 9 Piecewise-linear model of a p-n-p bipolar transistor

4 Fault Diagnosis Algorithm

In real framework the traced characteristics are approximate, because the models describing the active devices are not accurate. Moreover, the read test voltages deviate from the actual values due to limited measurement accuracy. In addition, the self-heating of the device that influences the characteristics and the measured voltages is omitted. In consequence, the measured voltages may deviate from the family of characteristics as shown in Fig. 12. To overcome this difficulty the following procedure is proposed.

Let us consider the family of characteristics projected on the plane $\tilde{v} \times \tilde{\tilde{v}}$ (see Fig. 12) and find the distances from the point $\left(\tilde{v}_{\text{read}}, \tilde{\tilde{v}}_{\text{read}}\right)$ to all the projected individual characteristics. Next the minimum distance $d_{\min}$ is selected and all the projected characteristics whose distances to the point $\left(\tilde{v}_{\text{read}}, \tilde{\tilde{v}}_{\text{read}}\right)$ are less than max $\left\{2d_{min}, \hat{d}\right\}$, where $\hat{d}$ is an assumed tolerance, are taken into account. The distances are specified by appropriate points that lie on the projected characteristics. Using the family of characteristics we find the resistances corresponding to these points. The smallest resistance R^- and the largest one R^+ form the range (R^-, R^+) of the spot defect values. Thus, unlike the ideal case, an interval of the values is obtained rather than a single value.

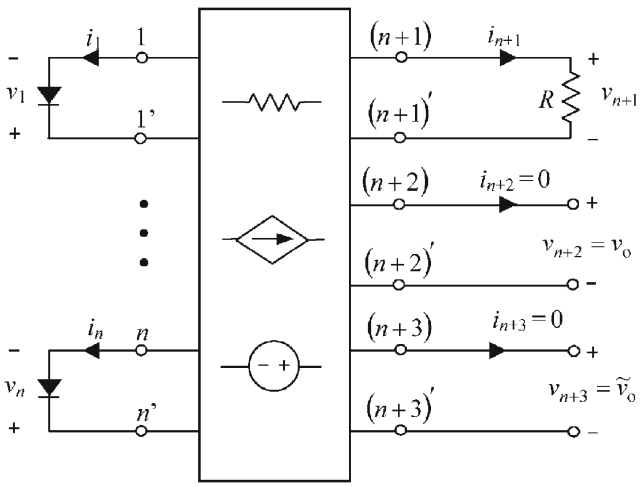

Fig. 10 Circuit with extracted diodes and some branches

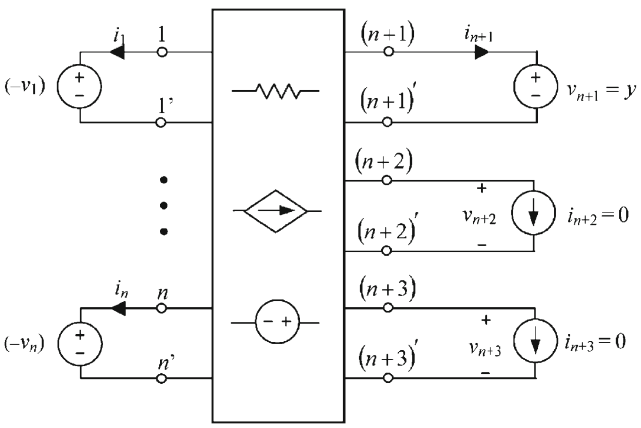

Fig. 11 Rearranged circuit of Fig. 10

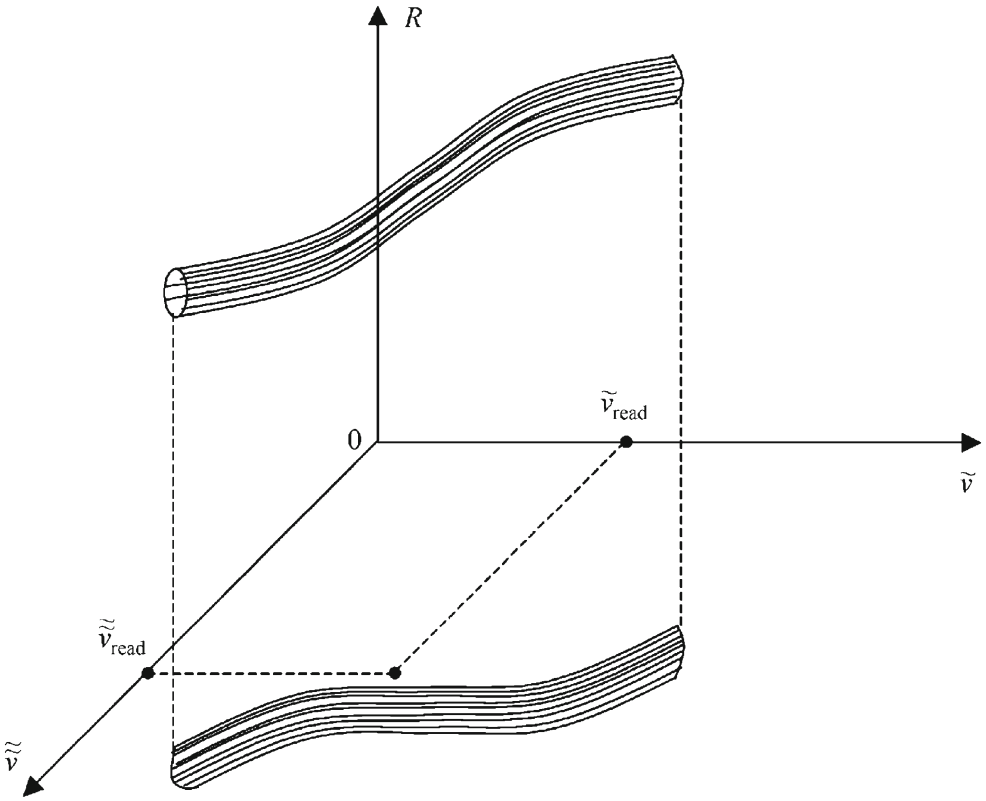

Fig. 12 Family of characteristics and its projection on $\tilde{v} \times \tilde{\tilde{v}}$ plane

4.1 Sketch of the Algorithm

Let n_{sc} (n_{oc}) be the number of the soft shorts (the soft opens) that are considered as potential failures to be diagnosed.

Step 1—Building the fault dictionary.

Fault dictionary consists of the families of the characteristics, corresponding to all the potential defects. The applied method, described in Section 3, traces the characteristics in wide ranges automatically generated.

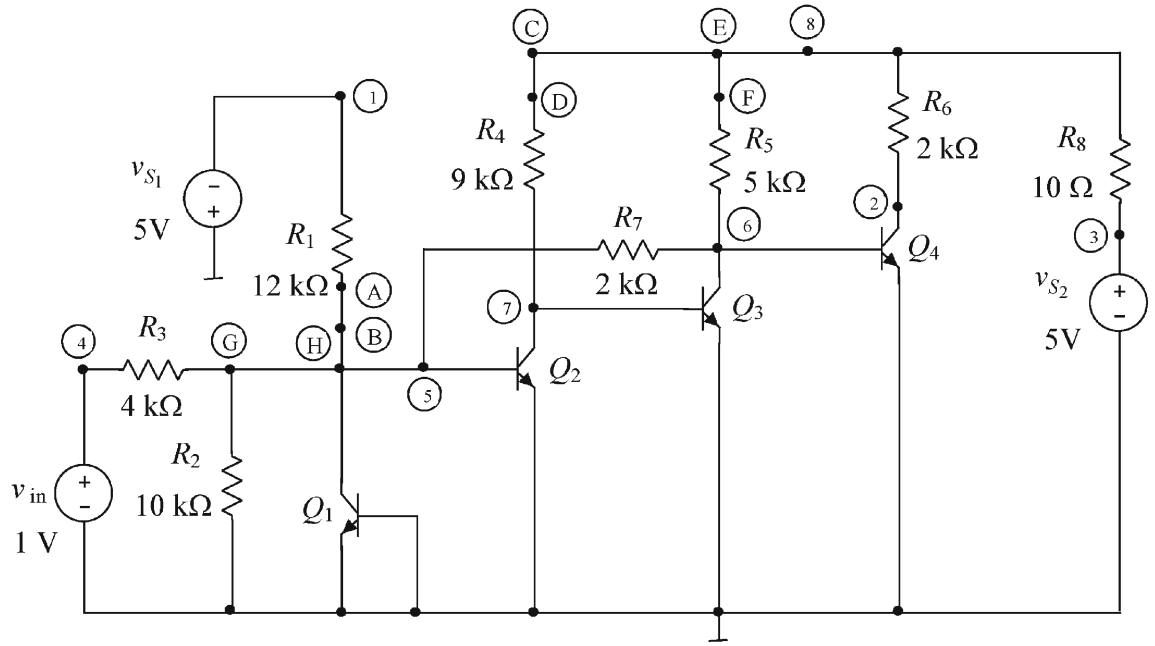

Fig. 13 BJT circuit for Example 1

Each of the families is composed of T characteristics, $R_j^{(i)}=f_j^{(i)}(y_1,\ldots,y_m)$, where $R_j^{(i)}$ is the resistance that simulates i-th defect and corresponds to j-th characteristic; $y_1,\ldots,y_m$ are the test voltages, $i=1,\ldots,n=n_{sc}+n_{oc}$, $j=1,\ldots,T$. Any characteristic is traced in the circuit with the parameters of the fault-free elements randomly selected within the tolerance ranges $\pm\varepsilon$, assuming uniform distribution. To make possible diagnosis the fault-free circuit, T analyses of this circuit, with the mentioned-above parameters, are performed and every time the voltages $y_1,\ldots,y_m$ are computed. As a result the upper and lower bounds on them $[y_1^-,y_1^+],\ldots,[y_m^-,y_m^+]$, are found and added to the fault dictionary. If the circuit has multiple operating points more than one set of the bounds are obtained.

Step 2—Identification of the potential defects.

For this purpose the test is arranged and the voltages $y_1,\ldots,y_m$ are measured. The measured values are labeled $\overline{y}_1,\ldots,\overline{y}_m$. If $\overline{y}_j\in\left[y_j^-,y_j^+\right]$ for all $j=1,\ldots,m$, the circuit is considered as fault-free. Otherwise, the first family of the characteristics is chosen and the distance from the point $(\overline{y}_1,\ldots,\overline{y}_m)$ to the nearest characteristic of the family, projected on the plane $y_1\times y_2\times\cdots\times y_m$, is determined. This is repeated to all the families, leading to the set of distances $\{d_1,\ldots,d_n\}$. From among all the distances, these ones (labeled $\boldsymbol{d}_j$) which are less than d, where d is a small number, are selected. The indices j of the selected distances indicate the potential defects.

Step 3—Finding the ranges (R_j^-,R_j^+) of the potential defects.

For all the potential defects the ranges (R_j^-,R_j^+) are determined using the approach described at the beginning of this section. If (R_j^-,R_j^+) belongs to the feasible range that defines the j-th soft spot defect, it is considered as the actual one. In such a case we compute the average value $\overline{R}_j=1/2\left(R_j^-+R_j^+\right)$.

4.2 Note

Because the spot defects occur at external terminals of the devices inside the chip, the interior elements of the transistor model are fault-free and they are fixed. Forming the hybrid representation, required by the method, is performed automatically on the basis of the netlist created in SPICE. The lines corresponding to the transistors are replaced by the lines containing the description of their piecewise-linear models. The values of the resistors and the voltage sources, that appear in the model, are calculated using the original exponential characteristic of the Ebers-Moll model. The user decides on the number of the points and their location, at the preliminary stage. They are valid for all the transistors of the same type.

5 Numerical Examples

The proposed method has been implemented in MATLAB 2010a and tested using PC Pentium i7-2600, 4 GB. It is assumed that the feasible region of soft short is [10 Ω–10 kΩ] and the feasible region of soft open is [100 kΩ–10 MΩ].

5.1 Example 1

Let us consider the BJT circuit, ¼ MC 1489A, shown in Fig. 13. Nominal values of the resistances are indicated in this figure. The parameters of the Ebers-Moll model of the transistors are as follows: α_F=0.9911, α_R=0.9091, I_{ES}=33.29 fA, I_{CS}=36.30 fA, V_T=25.86 mV, R_E=0.1 Ω, R_C=0.4 Ω, R_B=0.3 Ω. The emitter and collector diodes are modeled using the piecewise-linear representation as shown in Fig. 9 with N=8. We want to diagnose fault-free circuit (F_0), and M=7 soft spot faults (see Fig. 13): F_1 (soft open—AB), F_2 (soft open—CD), F_3 (soft short—1, 7), F_4 (soft short—2, 6), F_5 (soft short—2, 7), F_6 (soft short—6, 7), F_7 (soft short—5, 6). The representative printed circuit board (PCB) circuitry was built and laboratory tested using the measurement nodes 2, 5, and 6. They define the tested quantities: $y_1=v_2$, $y_2=v_5$, and $y_3=v_6$. To perform the fault diagnosis the distance d, the measurement nodes, and the input voltage value are picked on the basis of numerical experiments performed at the preliminary stage of the procedure.

We execute Step 1 of the algorithm, with T=100 and ε=2%, to build the fault dictionary, leading to seven families of the characteristics and the set of ranges of the voltages $[y_1^-,y_1^+]=[4.9847,4.9857]$, $[y_2^-,y_2^+]=[-0.1871,-0.1600]$, $[y_3^-,y_3^+]=[0.0074,0.0077]$, all in volts. The time of the fault dictionary determination is 180 s.

Let us consider in detail three spot defects F_2, F_3, and F_4, in the circuit having the resistances, within the tolerance ranges, as follows: R_1=12.04 kΩ, R_2=9.97 kΩ, R_3=4.03 kΩ, R_4=9.01 kΩ, R_5=5.06 kΩ, R_6=1.98 kΩ, R_7=1.98 kΩ, R_8=10.18 Ω.

The spot defects are as follows: Case 1—the soft open defect F_2 ($R_{F_2}=510\,\mathrm{k\Omega}$), Case 2—the soft short defect F_3 ($R_{F_3}=1\,\mathrm{k\Omega}$), Case 3—the soft short defect F_4 ($R_{F_4}=10\,\Omega$).

In all the cases the measured voltages $\overline{y}_1,\overline{y}_2$, and $\overline{y}_3$ determine the point which is outside the region $[y_1^-,y_1^+]\times[y_2^-,y_2^+]\times[y_3^-,y_3^+]$, hence, the circuits are diagnosed as faulty. To identify the potential defects the procedure described in Step 2 of the algorithm, with d=0.1 V, is used. The results are summarized in Table 1.

In Case 1 the selected distances $\boldsymbol{d}_2$, $\boldsymbol{d}_3$, and $\boldsymbol{d}_6$ show that the defects F_2, F_3, and F_6 should be considered, as described in Step 3 of the algorithm, with $\hat{d}=0.05$V. As a result we obtain the following ranges: $\left(R_{F_2}^-,R_{F_2}^+\right)=(437.2,537.7)\,\mathrm{k\Omega}$, $\left(R_{F_3}^-,R_{F_3}^+\right)=(11.55,12.05)\,\mathrm{k\Omega}$, $\left(R_{F_6}^-,R_{F_6}^+\right)=(1.086,1.140)$

Table 1 The distances d_j corresponding to Example 1

	Measured voltages in volts	d_j[V] of the spot defect F_j						
		d_1	d_2	d_3	d_4	d_5	d_6	d_7
Case 1	$\bar{y}_1 = 4.970\,\text{V}$	0.107	**0.020**	**0.015**	0.459	0.483	**0.015**	0.106
	$\bar{y}_2 = -0.124\,\text{V}$							
	$\bar{y}_3 = 0.112\,\text{V}$							
Case 2	$\bar{y}_1 = 0.016\,\text{V}$	0.689	0.341	**0.007**	0.405	0.361	0.165	0.640
	$\bar{y}_2 = -0.180\,\text{V}$							
	$\bar{y}_3 = 0.665\,\text{V}$							
Case 3	$\bar{y}_1 = 0.044\,\text{V}$	0.179	0.714	0.179	**0.001**	0.132	0.179	0.179
	$\bar{y}_2 = -0.173\,\text{V}$							
	$\bar{y}_3 = 0.017\,\text{V}$							

The distances less than d are maked with bold numbers

kΩ. Two of them $\left(R^-_{F_2}, R^+_{F_2}\right)$ and $\left(R^-_{F_6}, R^+_{F_6}\right)$ belong to the feasible ranges of the soft defects F_2 and F_6. The average values of the defects are: $\overline{R}_{F_2} = 487.4\,\text{k}\Omega$, $\overline{R}_{F_6} = 1.113\,\text{k}\Omega$. Thus, the method finds the actual defect F_2 and the virtual one F_6. In Case 2 the selected distance $\boldsymbol{d}_3$ shows that the defect F_3 occurs. The range of the defect values obtained by performing Step 3 is $(R^-_3, R^+_3) = (0.908, 0.993)\text{k}\Omega$, with the average value $\overline{R}_3 = 0.950\,\text{k}\Omega$. In Case 3 the selected distance $\boldsymbol{d}_4$ shows that the defect F_4 occurs. The obtained range of the defect values is: $(R^-_4, R^+_4) = (10.22, 11.75)\Omega$, with the average value $\overline{R}_4 = 10.99\,\Omega$. The time of performing the diagnosis on the basis of the fault dictionary does not exceed one second in each of the cases.

Moreover a fault-free circuit is tested leading to the following results. The diagnostic test gives the values of the measured voltages: $\bar{y}_1 = \bar{v}_2 = 4.985\,\text{V}$, $\bar{y}_2 = \bar{v}_5 = -0.179\,\text{V}$, $\bar{y}_3 = \bar{v}_6 = 7.5\,\text{mV}$. All of them are inside the ranges $[y^-_j, y^+_j]$, (j=1,2,3), hence, the circuit is fault-free.

Since the technique is specialized to a limited number of analog faults diagnosing, a question arises as to what will happen if a different spot defect, not considered during the dictionary construction, occurs. To answer this question new spot defects were introduced to the circuit shown in Fig. 13 and numerically tested using the proposed algorithm. They comprise soft shorts of the points (6, 8), (5, 7), (1, 2), (1, 6), (5, 8), (2, 5) and soft opens of the points (E, F), (G, H). The values of the failures were randomly selected from the feasible regions taking 30 values in each of the cases, together 240 values of the defects. In all the cases the algorithm classifies the circuit as faulty, in 71.7 % without identification of the defect. In 28.3 % the algorithm wrongly indicates some faults, considered in the fault dictionary construction, as the actual ones. The obtained statistically coverage of the faults not considered during the dictionary construction seems to be good. Moreover, if the defects used to build the dictionary are selected on the basis of the layout, by choosing the points where the failures are the most probable, the above-discussed problem is not dominant.

To apply the proposed method to CMOS circuits the MOS transistors are characterized using the Shichman-Hodges model in the form described in Section 3. The diodes that appear in the model are described by the equations

$$i_1 = i_{EF} = \begin{cases} k\left(v_{gs} - |v_{t_0}|\right)^2 & \text{for} \quad v_{gs} \geq |v_{t_0}| \\ 0 & \text{for} \quad v_{gs} < |v_{t_0}| \end{cases}, \tag{9}$$

$$i_2 = i_{CF} = \begin{cases} k\left(v_{gd} - |v_{t_0}|\right)^2 & \text{for} \quad v_{gd} \geq |v_{t_0}| \\ 0 & \text{for} \quad v_{gd} < |v_{t_0}| \end{cases}, \tag{10}$$

where v_{t_0} is the threshold voltage, $k = \frac{K_p}{2}\frac{W}{L}$, where K_p is the transconductance parameter, W and L are the channel width and length, respectively. The characteristics (9) and (10) are modeled using the piecewise-linear representation with N=8.

5.2 Example 2

Let us consider the CMOS circuit [27] shown in Fig. 14. The nominal values of the channel width W and length L in μm are indicated in the figure. Nominal values of the other transistor parameters are as in reference [27]. The circuit was numerically tested using the nodes 6, 7, and 5. They define the tested voltages: $y_1 = v_6$, $y_2 = v_7$, and $y_3 = v_5$. We want to diagnose fault-free circuit (F_0) and M=4 soft short spot defects (see Fig. 14): F_1 (6, 0), F_2 (4, 5), F_3 (3, 5), F_4 (5, 6). To build the fault dictionary we perform Step 1 of the algorithm, with T=21

Table 2 The distances d_j corresponding to Example 2

	Voltages in volts	d_j [V] of the spot defect F_j			
		d_1	d_2	d_3	d_4
Case 1	$\overline{y}_1 = 0.000\,\mathrm{V}$	2.070	**0.000**	0.711	3.344
	$\overline{y}_2 = -0.017\,\mathrm{V}$				
	$\overline{y}_3 = 4.516\,\mathrm{V}$				
Case 2	$\overline{y}_1 = 4.999\,\mathrm{V}$	0.085	**0.009**	0.259	0.059
	$\overline{y}_2 = -0.001\,\mathrm{V}$				
	$\overline{y}_3 = 0.070\,\mathrm{V}$				
Case 3	$\overline{y}_1 = 0.244\,\mathrm{V}$	0.699	**0.004**	**0.027**	2.079
	$\overline{y}_2 = -0.012\,\mathrm{V}$				
	$\overline{y}_3 = 3.124\,\mathrm{V}$				

The distances less than d are maked with bold numbers

and the tolerance of the parameters k and v_{t_0}, ε=5 %. The dictionary includes four families of the characteristics and the set of ranges of the voltages: $[y_1^-, y_1^+]$=[4.999, 5.000], $[y_2^-, y_2^+]$=[−0.001, 0.000], $[y_3^-, y_3^+]$=[0.000, 0.001]. The time of the fault dictionary determination is 125 s. Let us consider in detail three cases: Case 1—the soft short F_2 ($R_{F_2} = 33\,\Omega$), Case 2—the soft short F_2 ($R_{F_2} = 5.1\,\mathrm{k}\Omega$), Case 3—the soft short F_3 ($R_{F_3} = 510\,\Omega$). In all the cases the measured in the test phase voltages are outside the region $[y_1^-, y_1^+]\times[y_2^-, y_2^+]\times[y_3^-, y_3^+]$, hence, the circuits are diagnosed as faulty. The results of selecting the potential faults, using d=0.05, are summarized in Table 2.

In Case 1 the selected distance $\boldsymbol{d}_2$ shows that the defect F_2 should be considered, as described in Step 3 of the algorithm, with $\hat{d} = 0.05\,\mathrm{V}$. As a result we obtain the following range $\left[R_{F_2}^-, R_{F_2}^+\right] = [31.36, 31.98]\,\Omega$, with $\overline{R}_{F_2} = 31.67\,\Omega$. In Case 2 the selected distance $\boldsymbol{d}_2$ shows that the defect F_2 should be considered, as described in Step 3 of the algorithm. As a result we obtain the range $\left[R_{F_2}^-, R_{F_2}^+\right] = [4.294, 6.183]\,\mathrm{k}\Omega$, with $\overline{R}_{F_2} = 5.238\,\mathrm{k}\Omega$. In Case 3 the selected distances $\boldsymbol{d}_2$ and $\boldsymbol{d}_3$ show that the defects F_2 and F_3 should be considered as described in Step 3 of the algorithm. As a result we obtain the following ranges: $\left[R_{F_2}^-, R_{F_2}^+\right] = [304, 328]\,\Omega$, with $\overline{R}_{F_2} = 316\,\Omega$ and $\left[R_{F_3}^-, R_{F_3}^+\right] = [553, 553]\,\Omega$, with $\overline{R}_{F_3} = 553\,\Omega$.

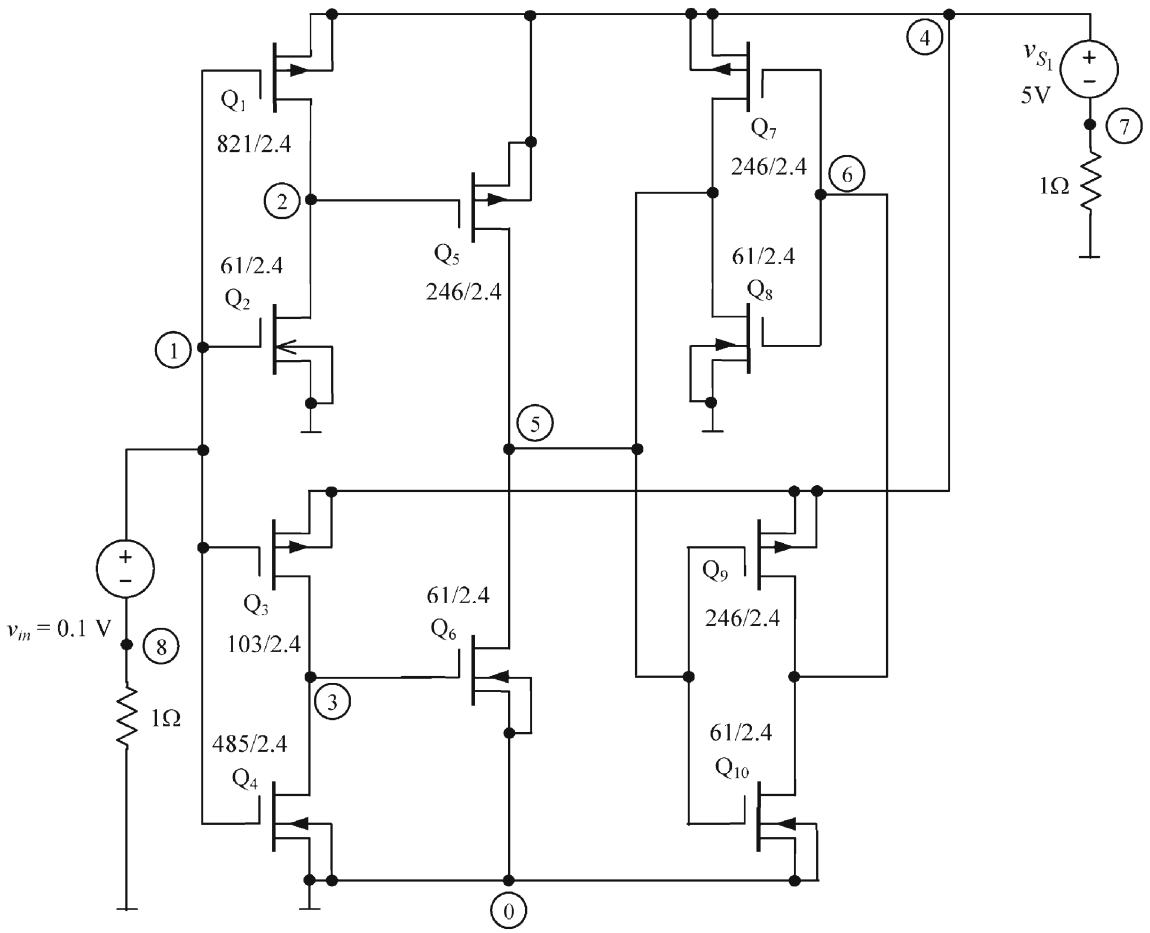

Fig. 14 CMOS circuit for Example 2

Thus, the algorithm gives the actual fault F_3 and the virtual one F_2. The time of performing the diagnosis on the basis of the fault dictionary does not exceed 0.5 s.

6 Conclusion

Shorts and opens, classified as spot defects, represent the majority of defects that are met in production and operation of analog integrated circuits. This paper is focused on soft spot defects, with open defect simulated with finite resistance and short defect with non-negligible resistance. The proposed diagnostic method includes all aspects of the diagnosis, i.e., detection, location, and estimation of the defect value. The main advantage of this method is capability for diagnosis of the nonlinear circuits having multiple operating points. This property is essential and makes the method reliable, because the faulty circuit may have several operating points, even if the fault-free circuit has a unique operating point. Numerical and laboratory experiments support this statement. In addition, deviations of the fault-free parameters within their tolerance ranges are taken into account. The method was verified using exemplary bipolar and CMOS circuits. The representative PCB model of the circuit shown in Fig. 13, comprising bipolar transistors, was built and laboratory tested to verify the proposed approach in realistic framework. The obtained results testify that the method is effective. The applied feasible ranges of the defect values are typical for soft spot defects. The cases of very small (1 Ω) or very large (100 MΩ) resistors can be effectively diagnosed using a different method, developed in reference [27]. Since this method is limited to the extreme cases only, both the methods can be considered as complementary and they form together a tool that allows testing enlarged distributions of the failures. The method described in reference [27] is very fast and should be used at the preliminary stage of the diagnostic process. The method proposed in this paper also allows diagnosis soft shorts in CMOS circuits designed in micrometer technology, using Level 1 transistor model. Intricate transistor models that characterize the transistors fabricated in submicrometer technology cannot be applied, due to some restrictions required by the method for tracing the characteristics leading to the fault dictionary.

The examples presented in this paper exploit a number of internal nodes for the measurement purpose. They bring useful information about the tested circuit. On the other hand the access to internal nodes is very limited in integrated circuits. To reduce the number of the required nodes the following approach, illustrated via Example 1, is proposed. In this example the parametric characteristic was considered in four-dimension space. Alternatively, we can discard one of the internal measurement nodes and trace two characteristics, each in three-dimension space. To diversify them two different sets of the supply source values must be chosen. Both the characteristics are used to create the fault dictionary. According to this approach internal node 6 is omitted and two characteristics, in terms of voltages v_2 and v_5, are traced for each of the spot defects. The corresponding supply source values are: $v_{S_1}^{(1)} = 5\,\mathrm{V}$, $v_{S_2}^{(1)} = 5\,\mathrm{V}$, $v_{in}^{(1)}=1\,\mathrm{V}$ and $v_{S_1}^{(2)} = 14\,\mathrm{V}$, $v_{S_2}^{(2)} = 3.5\,\mathrm{V}$, $v_{in}^{(2)}=5\,\mathrm{V}$. For the cases appeared in Table 1 we obtain, using laboratory test, the following results. In Case 1 the modified method identifies the actual fault F_2 with the range of the defect values $[407.4, 549.5]\mathrm{k}\Omega$ and the virtual one F_6 with the range $[0.966, 1.514]\mathrm{k}\Omega$. In Cases 2 and 3 only the actual faults F_3 and F_4 with the ranges $[0.988, 1.012]\mathrm{k}\Omega$ and $[10.00, 14.45]\Omega$, respectively are identified. Thus, in all the cases the modified version of the method identifies the same faults as the original one and provides similar ranges of the defect values. The disadvantages of this approach are: larger size of the dictionary and longer time of the defects identification.

References

1. Aminian F, Aminian M (2001) Fault diagnosis of analog circuits using bayesian neural networks with wavelet transform as preprocessor. J Electron Test 17:29–36. doi:10.1023/A:1011141724916
2. Aminian M, Aminian F (2007) A modular fault-diagnosis system for analog electronic circuits using neural networks with wavelet transform as a preprocessor. IEEE Trans Instrum Meas 56:1546–1554. doi:10.1109/TIM.2007.904549
3. Chua LO, Lin PM (1975) Computer-aided analysis of electronic circuits, algorithm and computational techniques. Prentice-Hall, Englewood Cliffs
4. Cottle RW, Pang JS, Stone RE (1992) The linear complementarity problem. Academic Press, New York
5. Czaja Z (2013) Self-testing of analog parts terminated by ADCs based on multiple sampling of time response. IEEE Trans Instrum Meas 62:3160–3167. doi:10.1109/TIM.2013.2272867
6. El-Gamal M, Mohamed MDA (2007) Ensembles of neural networks for fault diagnosis in analog circuits. J Electron Test 23:323–339. doi:10.1007/s10836-006-0710-1
7. Garcia CB, Zangwill WI (1981) Pathways to solutions, fixed points, and equilibria. Prentice-Hall, New York
8. Gizopoulos D (2006) Advances in electronic testing. Challenges and methodologies. Springer, Dordrecht
9. Gyvez JP, Di C (1992) IC defect sensitivity for footprint-type spot defect. IEEE Trans Comput Aided Des Integr Circ Syst 11:638–658. doi:10.1109/43.127625
10. Hochwald W, Bastian JD (1979) A DC approach for analog fault dictionary determination. IEEE Trans Circ Syst 26:523–529. doi:10.1109/TCS.1979.1084665

11. Huang K, Stratigopoulos HG, Mir S, Hora C, Xing Y, Kruseman B (2012) Diagnosis of local spot defect is analog circuits. IEEE Trans Instrum Meas 61:2701–2712. doi:10.1109/TIM.2012.2196390
12. Kabisatpathy P, Barua A, Sinha S (2005) Fault diagnosis of analog integrated circuits. Springer, Dordrecht
13. Kim B, Swaminathan M, Chatterjee M, Schimmel D (1997) A novel test technique for MCM substrates. IEEE Trans Components Packag Manuf Technol 20:2–12. doi:10.1109/96.554413
14. Li F, Woo PY (1999) The invariance of node voltage sensitivity sequence and its application in a unified fault detection dictionary method. IEEE Trans Circ Syst I 46:1222–1226. doi:10.1109/81.795835
15. Long B, Li M, Wang H, Tian S (2013) Diagnostics of analog circuits based on LS-SVM using time domain features. Cir Syst Signal Process 32:2683–2706. doi:10.1007/s00034-013-9614-3
16. Maly W, Strojwas AJ, Director SW (1986) VLSI yield prediction and estimation: a unified framework. IEEE Trans Comput Aided Des Integr Circ Syst 5:114–130. doi:10.1109/TCAD.1986.1270182
17. Quarles TL, Newton AR, Pederson DO, Sangiovanni-Vincentelli A (1993) SPICE-3, version 3F5 user's manual. Dep. of EECS, Univ. California, Berkeley
18. Rodrigez-Montanes R, de Gyves JP, Volf P (2002) Resistance characterization for weak open defects. IEEE Des Test Comput 19:18–26. doi:10.1109/MDT.2002.1033788
19. Schreiber HH (1979) Fault dictionary based upon stimulus design. IEEE Trans Circ Syst 26:529–537. doi:10.1109/TCS.1979.1084666
20. Spyronasios AD, Dimopoulos MG, Hatzopoulos AA (2011) Wavelet analysis for the detection of parametric and catastrophic faults in mixed-signal circuits. IEEE Trans Instrum Meas 60:2025–2038. doi:10.1109/TIM.2011.2115550
21. Tadeusiewicz M (2001) Global and local stability of circuits containing MOS transistors. IEEE Trans Circ Syst I Fundam Theory Appl 48:957–966. doi:10.1109/81.940186
22. Tadeusiewicz M, Hałgas S (2010) A method for fast simulation of multiple catastrophic faults in analogue circuits. Int J Circ Theory Appl 38:275–290. doi:10.1002/cta.570
23. Tadeusiewicz M, Hałgas S (2015) A new approach to multiple soft fault diagnosis of analog BJT and CMOS circuits. IEEE Trans Instrum Meas 64:2688–2695. doi:10.1109/TIM.2015.2421712
24. Tadeusiewicz M, Kuczyński A (2013) A very fast method for the DC analysis of diode–transistor circuits. Circ Syst Signal Process 32:433–451. doi:10.1007/s00034-012-9469-z
25. Tadeusiewicz M, Hałgas S, Korzybski M (2002) An algorithm for soft-fault diagnosis of linear and nonlinear circuits. IEEE Trans Circ Syst I 49:1648–1653. doi:10.1109/TCSI.2002.804596
26. Tadeusiewicz M, Hałgas S, Korzybski M (2012) Multiple catastrophic fault diagnosis of analog circuits considering the component tolerances. Int J Circ Theory Appl 40:1041–1052. doi:10.1002/cta.770
27. Tadeusiewicz M, Kuczyński A, Hałgas S (2015) Catastrophic fault diagnosis of a certain class of nonlinear analog circuits. Circ Syst Signal Process 34:335–375. doi:10.1007/s00034-014-9857-7
28. Zhihua W, Gielen G, Sansen W (1998) Probabilistic fault detection and the selection of measurements for analog integrated circuits. IEEE Trans Comput Aided Des Integr Circ Syst 17:862–872. doi:10.1109/43.720321

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