Drop Test Reliability of Lead-free Chip Scale Packages

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Abstract

This paper presents the drop test reliability of 0.5mm pitch lead-free chip scale packages (CSPs). Fifteen 0.5mm pitch CSPs were assembled on a standard JEDEC drop reliability test board with Sn3.0Ag0.5Cu lead-free solder. Eight boards were edge-bonded with a UV-cured acrylic; eight boards were edge-bonded with a thermal-cured epoxy; and twelve boards were assembled without edge bonding. Half of the edge-bonded test boards were subjected to drop tests at a peak acceleration of 1500G with a pulse duration of 0.5ms, and the other half subjected to drop tests at a peak acceleration of 2900G with a pulse duration of 0.3ms. Half of the test boards without edge bonding were subjected to drop tests at a peak acceleration of 900G with a pulse duration of 0.7ms, and the other half subjected to drop tests at a peak acceleration of 1500G with a pulse duration of 0.5ms. Two drop test failure detection systems were used in this study to monitor the failure of solder joints: a high-speed resistance measurement system and a post-drop static resistance measurement system. The high-speed resistance measurement system, which has a scan frequency of 50KHz and a 16-bit signal width, is able to detect intermittent failures during the short drop impact duration. Statistics of the number of drops to failure for the 15 component locations on each test board are reported. The effect of component position on drop test reliability is discussed. The test results show that the drop test performance of edge-bonded CSPs is five to eight times better than the CSPs without edge bonding. However, the drop test reliability of edge-bonded CSPs with the thermal-cured epoxy is different from that with edge-bonded CSPs with the UV-cured acrylic. The solder crack location and crack area are characterized with the dye penetrant method. The fracture surfaces are studied using scanning electron microscopy (SEM).

I. Introduction

Mobile and handheld electronics devices such as digital cameras, cell phones, and personal digital assistants (PDAs) are prone to be dropped in their lifetime. The drop event may result in failure of solder joints inside these devices. Recently the European Union (EU) Restriction of Hazardous Substances (RoHS) and other countries' lead-free directives banned the use of lead in consumer electronics products. Thus, it is critical to study the drop test reliability of lead-free solder joints.

There has been a significant amount of research done in the last few years on drop impact reliability. The JEDEC standard JESD22-B111 [1] for the board level and related standards [2, 3] for subassembly level have been developed for drop testing handheld electronics. Lim and Low [4] proposed a method to examine the drop impact responses of portable electronic products at different impact orientations and drop height. The impact behavior has been studied at the product level [5]. After comprehensive drop tests, failure analysis, and simulations on two ball grid array (BGA) packages at the board level, Tee, et al. [6] developed a life prediction model for board level drop testing. The effect of different solder alloy compositions on drop reliability has been studied by Syed, et. al. [7]. Since SnAgCu (SAC) solder alloy performs poorly compared with SnPb solder under drop test, several studies have been done to improve the reliability of lead-free solder joints by adding micro-alloying additions [8, 9] or lowering Ag content [10].

Underfill materials were originally developed to improve the solder joint reliability of ball-grid array (BGA) and flip chip packages during temperature cycling. Recently studies have shown that underfill can improve drop test reliability as well [11, 12]. However the application of underfills increases both the cost of production and assembly cycle times in manufacturing and this must be considered against the reliability improvements. To reduce the costs of underfill application, corner bonding and edge bonding processes have been developed. In the corner bonding process, the adhesive is applied near the package corners before BGA or CSP packages are placed and reflowed. In edge bonding processes, the adhesive is applied after the BGA or CSP packages are placed and reflowed. The reliability of corner-bonded CSPs has been investigated [13, 14].

Failure detection systems and failure criteria used in the literature vary widely. There are three main failure detection methods used in drop test reliability: post-drop (static) resistance measurement [12, 15], event detection [16], and in-situ high-speed data acquisition [17]. The post-drop resistance measurement method measures resistance of solder joints after each drop. The event detection method determines if a failure event temporarily occurs during a single drop. The in-situ high-speed data acquisition method measures the dynamic resistance of solder joints during and after the drop impact and board vibrations. Different researchers have used different failure criteria, for example, a resistance threshold of 300Ω [18], 1000Ω [1], or 1500Ω [16], a resistance change of 10% [12], or 20% [15]. In a sense, all of these criteria are subjective, because, at this time, no scientific research has been done on the interconnection failure criteria. Determination of appropriate failure criteria is extremely important in order to observe first failures and when failures advance to different failure stages [17]. This variety of failure detection systems and failure criteria used by different researchers make the comparison of results difficult. This study discusses the reliability of CSPs in drop impact, with and without edge-bonded underfill, using two

failure detection systems and presents the component failure sequence as observed by each system.

II. Test Vehicle Design and Assembly

The test vehicle was designed according to the JEDEC standard [1]. It uses an eight-layer FR4 material board with a size of 132mm by 77mm and a thickness of 1 mm. The component used was 0.5mm pitch Amkor CSP having 228 I/O and with a size of 12mm by 12mm. The CSP has daisy-chained connections with an input and output trace located at one package corner. The boards have Organic Solderability Preservatives (OSP) surface finish on non-solder mask defined (NSMD) pads, while the components have electro-plated nickel-gold surface finish on solder mask defined (SMD) pads. The test vehicle with components assembled is shown in Figure 1.

Sn3.0Ag0.5Cu (SAC305) Multicore 318LF lead-free solder paste (Type 3) was stencil printed using a DEK machine through a 4 mils thick electro-polished stencil with 12 mils square apertures. Solder paste height and volume were measured by a CyberOptic machine to ensure high printing quality. The component was picked and placed by a Siemens F5 machine. A Heller EXL1800 oven with seven heating zones and one cooling zone was used for solder reflow. The reflow oven processing was done in air. The reflow profile is shown in Figure 2.

Post-assembly cross-sectioning and SEM showed good solder joints with some small voids as shown in Figure 3. Visual and X-ray inspection showed shiny, round and well collapsed solder joints with no bridging.

The test boards were divided into three cells, one of which was edge-bonded with a thermal-cured epoxy, one of which was edge-bonded with a UV-cured acrylic, and the third cell having no edge-bonding. The edge-bond was applied on all four package corners by an Asymtek Century series machine. The edge bond had an average length of 3.81 mm (150 mils) along each side (per corner) after the assembly process was complete, and had an average length of 1.2 mm fillet leg after being cured. Figure 4 shows an example of the finished edge-bond.

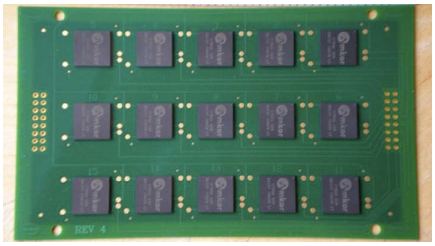

Figure 1. Test vehicle with components

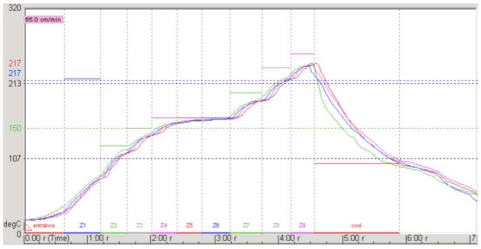

Figure 2. Solder reflow profile

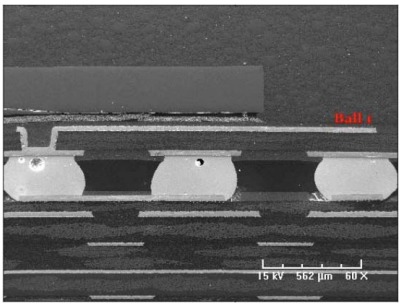

Figure 3. SEM of solder joints after assembly

Figure 4. An edge-bonded CSP

III. Drop Test Methodology

The drop tests were conducted using a Lansmont M23 TTSII shock test system, which applies a single half-sine shock impact pulse to the test vehicle for each drop. Multiple impacts were prevented by a pneumatic rebound brake system that slowly brings the table to a stop with minimal effect on board vibration. This shock test system represents a typical board level drop test setup.

For this study the test vehicle was mounted with the board in a horizontal position with the components facing downward which is the most severe orientation for board deflection [1, 19]. Four corner shoulder screws with 12 mm standoff supported the board mounted on the drop table. The drop table was secured between two guiding rods and could travel only along the vertical direction. When dropped from the chosen height, the drop table falls vertically and impacts the stationary seismic shock mounted table base. This impact transfers an input acceleration pulse to the test board through the four corner supports. The acceleration peak value and pulse duration are controlled by the drop height, friction against guiding rods, and impact surface.

Three acceleration conditions were chosen from the JEDEC recommendations [2]: 900G, 1500G, and 2900G, with 0.7 ms, 0.5 ms, and 0.3 ms durations respectively. These are JEDEC condition F, B, and H. The input acceleration pulse was monitored for each drop by an accelerometer attached to the table base plate using a Test Partner TestPal signal conditioner and software. For each drop height and impact surface selected, the average result of two accelerometers was used as shown in Figure 5. The table impact surface varied between acceleration conditions, with a felt pad used for 900G and several sheets of watercolor paper used for 1500G and 2900G. The drop heights used were 368 mm (14.5 inch), 572 mm (22.5 inch), and 762 mm (30 inch). The drop height was adjusted incrementally to maintain consistent acceleration conditions during test cycles and the acceleration was measured on every drop. One deviation was made from the JEDEC standard in that the gap between the shoulder screw and board surface was controlled to

within only 100 microns rather than the standard 50 microns [1]. A misalignment of tooling for the drop test support screws prevented use of the specified gap limitation.

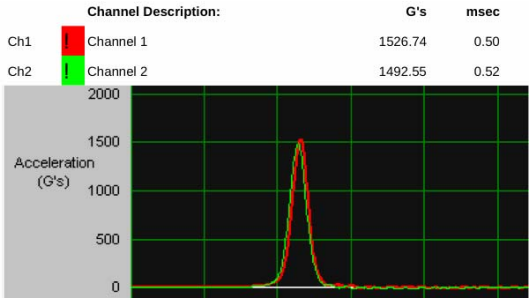

Figure 5. Input acceleration pulse of 1500G - 0.5ms, condition B

The test vehicles were split into two groups as shown in Table 1, one per failure detection system, with each group having 8 edge bonded boards (4 for each edge-bond material) and 6 boards without edge bond. Those groups were split so that each group would have 3 non-edge bonded boards at 900G, 3 non-edge bonded boards and 4 edge bonded boards at 1500G, and 4 edge bonded boards at 2900G. One additional board without edge bond was dropped at 2900G (no matching board was tested by post-drop).

Table 1. Number of boards per drop test variable cell

Failure Detection	DAQ System		Post-drop System	
Edge-bonding	Yes	No	Yes	No
900G	0	3	0	3
1500G	4	3	4	3
2900G	4	1	4	0

IV. Failure Detection Systems

This study compares drop impact failures with two failure detection systems: in-situ high-speed data acquisition (DAQ) with analog-to-digital conversion (ADC) yielding dynamic resistance measurement, and post-drop static resistance measurement. These systems will be referred to as the data acquisition system and the post-drop system for purposes of discussion.

The high-speed data acquisition system uses a National Instruments (NI) ADC, a desktop computer, and a voltage divider network to evaluate the resistance of the component daisy chain during the drop impact at a sampling frequency of 50KHz and 16-bit accuracy. This sampling rate of the system provides 50 sample points per millisecond for each component (50,000 per second), so that several samples are taken during the initial shock pulse (as short as 0.3 ms for 2900G). The primary deflection time of the board and first harmonic vibration frequency in a 1500G drop are near 4 ms and 240Hz [20]; with a 50Khz sampling frequency this system provides more than 200 samples per board deflection cycle. During each drop the ADC records every data point taken from the fifteen components and supply voltage and saves a data file for later analysis. A simple and proven method of achieving dynamic daisy-chain resistance measurement at near real-time was used [21]. The daisy chain is placed in a DC series circuit with a static resistor (R_s) of known value (in this case 100Ω) to construct a voltage divider circuit as shown in Figure 6. The DAQ records the voltage (V_c), divided across the component resistance and static resistance. The voltage (V_c) relates to the resistance (R_c) by Eq. 1, where V_{DC} is the DC voltage source set to 5V. As the component electrically fails, the resistance rises ($R_c \Rightarrow \infty$) and the DAQ registers a rise in voltage ($V_c \Rightarrow V_{DC} = 5V$).

$$R_C = \frac{V_c \cdot R_s}{V_{DC} - V_c} \quad (1)$$

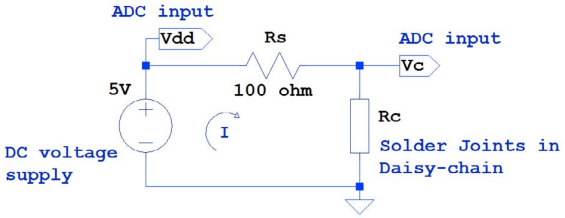

Figure 6. DC series voltage divider circuit

A cable was connected to the test vehicle by soldering the 16 wires (15 channels and common ground) directly into plated through-holes on the short side of the board. The cable was secured to the drop tester base plate to prevent loading against the solder connections during impact. The failure criterion used for the high-speed data acquisition system was taken directly from the JESD22-B111 standard [1]: a 100Ω resistance in the component daisy chain at any time during the drop impact or subsequent vibration is considered a failure, and the failure must be repeated in at least three out of five successive drops. Since a 100Ω static resistor and 5V DC supply voltage are used, the failure condition of 100Ω is the equivalent of measuring 2.5V on the component daisy chain. The electrical continuity of the cable-to-board through-hole solder joints was verified at regular intervals during and after drop testing to eliminate false positive failures due to broken cable connections.

The post-drop resistance measurement system used a LabView program and Keithley digital multimeter to read the daisy-chain resistance, once for each component after each drop, through a cable connected to the test vehicle after the vibration ceases. For this system no cable is connected to the board during the drop event. The failure criterion for the post-drop resistance measurement system of a static 10Ω rise (or more) from initial resistance is used.

The two failure detection systems use failure criteria that are necessarily different. The post-drop system is detecting a class of permanent failures only, which may be a solder crack that may be partially seated together when the board is at rest; the change in the resistance of the daisy chain due to this crack is small. The 10Ω static rise threshold was chosen to detect that small change. The data acquisition system detects intermittent failure, which may have insignificant resistance change when the board is at rest but a larger change during board deflection. The data acquisition system uses a temporary 100Ω resistance threshold, although data samples taken after the board vibration ceases could also be used to detect failure with the post-drop criteria.

The high-speed data acquisition system is capable of detecting intermittent failures as shown in Figure 7 during the

board deflection and vibrations, whereas due to the single static measurement taken per drop the post-drop system can only detect permanent failures. In the example shown the static resistance rise from the initial condition is negligible and would not be detected as failure by the post-drop system since the static resistance rise is less than 0.1 ohm from the initial condition.

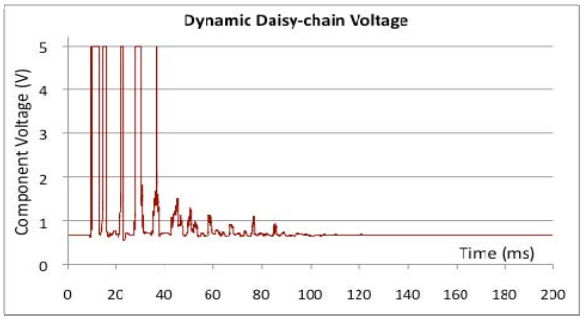

Figure 7. Intermittent failure detected by DAQ system, 10,000 data points shown in a 0.2 second window

V. Results and Discussion

Because the JEDEC standard drop test induces a complex strain pattern across the test board, causing varied stresses in the solder joints, JEDEC recommendations divide the components on the board into six groups (denoted A-F) that are expected to have similar failure rate due to the symmetry of their locations [1]. The issue of component location has been shown in a number of studies to be critical; the stress and strain in solder joints, and their failure rate, is partially dependent on the component location on the board [22, 23]. Che, et al. found that the maximum acceleration location occurs at the board center and is much higher than the input acceleration, however the maximum board strain occurs under components along the board edges and near the supports [22]. Therefore it is necessary to discuss failures in context of component location. The component locations are numbered as shown in Figure 8, and for this study the DAQ system cable is always soldered in thru-holes at the board edge near component 6.

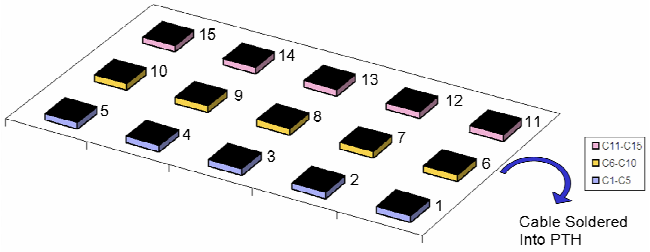

Figure 8. Board component location numbers for 15 components

A. CSP reliability without edge bonding

The drops to failure for each component location and test board without edge bonding are shown in Table 2 for the DAQ system and in Table 3 for post-drop system. In both tables, each column represents one board except the first column. The first row is the input acceleration condition used for that board and the second row is the total number of drops the board was subjected to.

It is clear that the drops-to-failure is different between the DAQ system and the post-drop system. One of the most obvious differences is that component C5 failed for every post-drop system board at 900G and 1500G but not at all for the DAQ system for those conditions. C14 and C9 also have similar differences between the detection systems, both failing more for the post-drop system than data acquisition. The reason for this difference in failure between systems is not clear yet, however it may be due to the attachment of the data acquisition cable to the board, which is believed to have an effect on board dynamics.

The component location plays a significant role in the drop test reliability. The components along the board center (C3, C8, C13) tend to fail earliest and most frequently for both failure detection systems, although C3 did not fail as often for the DAQ system. Components C4 and C12 also failed consistently for both systems, but the symmetrical board locations of C2 and C14 did not fail as often or as early; C2 did not fail consistently for either system, but C14 did fail for the post-drop system. The failure locations have other symmetry issues as well; with C9 failing on the post-drop system but the symmetrical match C7 failing infrequently.

Table 2. Drops to failure by data acquisition, no edge bond

Accel (g)	900	900	900	1500	1500	1500	2900
Drops	75	75	100	70	40	60	50
Edge Bond	None	None	None	None	None	None	None
Component							
C1				**37**	**29**		**7**
C2							**25**
C3	**62**				**14**	**33**	**4**
C4	**26**	**26**	**34**	**26**	**6**	**23**	**4**
C5							**5**
C6					**21**	**35**	**3**
C7					**19**		**42**
C8	**28**	**44**		**50**	**3**	**13**	**7**
C9					**30**		**21**
C10							
C11					**5**		**11**
C12	**16**	**6**	**43**	**13**	**2**	**6**	**4**
C13	**15**	**11**	**40**	**9**	**1**	**5**	**2**
C14					**21**	**32**	**38**
C15							**50**

Table 3. Drops to failure by post-drop, no edge bond

Accel (g)	900	900	900	1500	1500	1500
Drops	75	70	100	70	40	60
Edge Bond	None	None	None	None	None	None
Component						
C1			**82**	**55**		**38**
C2						**22**
C3	**7**	**31**	**15**	**8**	**3**	**11**
C4	**10**	**43**	**17**	**7**	**5**	**36**
C5	**65**	**2**	**14**	**1**	**5**	**14**
C6	**54**					**45**
C7			**61**			**9**
C8	**13**	**13**	**16**	**7**	**5**	**2**
C9	**53**	**16**	**11**	**28**	**8**	**14**
C10						
C11	**29**		**55**			**12**
C12	**6**	**9**	**18**	**5**	**3**	**3**
C13	**5**	**28**	**16**	**5**	**3**	**3**
C14	**1**		**37**	**5**	**34**	**4**
C15	**44**		**75**	**26**		

It is interesting to note that the drops-to-failure vary significantly between different boards for the same component location. It is clear that higher G-level results in lower drops-to-failure. Every component except C10 in a board without edge-bonding failed after 50 drops when subjected to 2900G. Most of the components fell off the board after less than 20 drops.

B. CSP reliability with edge bonding

The drops to failure data for edge-bonded boards are reported in Tables 4 and 5. The total number of drops for each board is listed in row 2, and the edge bonding material (either thermal-cured epoxy or UV-cured Acrylated Urethane) is listed in row 3.

It is clear that edge-bonding improves the drop test reliability significantly by comparing the orange highlighted columns in Table 4 (2900G) to the last column of Table 2 (also 2900G). Eight components failed on a board without edge-bonding after 7 drops when subjected to 2900G as shown in Table 1, while first eight failures occurred for boards with edge-bonding after 36, 44, 100, and 133 drops when subjected to 2900G as shown in Table 4. For an input acceleration of 2900G, the edge-bonded boards show a 5-8 times reliability improvement.

The component location plays a significant role in the drop test reliability. Similarly to the boards without edge bonding, components C4 and C12 fail earlier than components C2 and C14, in the symmetrically mirrored board locations. Again as with the boards without edge bonding, components C7 and C9 show significant symmetry mismatch in both board failure detection systems. This issue is explored further in the failure analysis section where the determined cause is explained.

The drop counts to failure are higher with edge bond applied for the majority of boards and component locations, and for both failure detection systems. However, the data acquisition system observed some intermittent failures that occurred for up to 150 consecutive drops in edge-bonded components without ever advancing to a permanent failure stage. In some of these cases the post-drop system would not have recorded failure when drop testing was stopped.

Table 4. Drops to failure by data acquisition, edge-bonded

Accel (g)	1500	1500	1500	1500	2900	2900	2900	2900
Drops	325	350	279	355	190	170	175	173
Edge Bond	Heat	Heat	UV	UV	Heat	Heat	UV	UV
Component								
C1						151	66	61
C2		342	276		133	127		119
C3	80	292	33	101	70	72	12	103
C4	236	255	257		63	16		100
C5						36	73	91
C6		55				44	37	60
C7						35	69	158
C8	201			85	113	20	84	83
C9				292		25	29	124
C10			277			12	59	
C11		193	178	103		65	38	
C12	66	76	52	162	53	24	23	16
C13	61	129	73	77	42	13	18	14
C14		232				42	44	120
C15	107		268		44	22	25	90

Table 5. Drops to failure by post-drop, edge-bonded

Accel (g)	1500	1500	1500	1500	2900	2900	2900	2900
Drops	237	350	279	300	170	170	175	173
Edge Bond	Heat	Heat	UV	UV	Heat	Heat	UV	UV
Component								
C1		304	62			12	23	
C2			101				34	98
C3	2		180	81	74	72		23
C4	2	292	99	242		25	13	
C5	60		62	262		40		151
C6	112	282	180			151		
C7		6						
C8	88			108		68	30	21
C9		132		283	116	106	53	
C10		112						
C11	3	292				112		
C12	1	36	188	162	137	57	154	128
C13	159	99	188	133	6	144	36	43
C14	60			243			151	
C15				297				

The data acquisition system does not always show failures in fewer drops (earlier detection) as was expected since it can detect the intermittent failure, but it recorded more total failures of the 2900G set than the post-drop system did. The capability of detecting failure earlier may be partially offset by the requirement of adding wired connections to the board during the drop impact; the wire may influence board deflection and vibration characteristics, and subtly effect drop reliability results.

VI. Failure Analysis

Failure analysis was performed on a subset of the failed test boards after drop tests. The outer row of solder joints of two components on two boards each was cross-sectioned. Scanning electron microcopy (SEM) images indicate the intermetallic layer thickness was 1-1.3 micron on the board side and 1.3-2 microns on the component side. To investigate the extent of cohesive failure resulting from the drop tests, the dye penetrant test was performed on eight boards, four with and four without edge-bond. Optical microscopy was used to identify dyed areas and determine failure location, root cause, and how widespread the under-pad resin cracking problem was for each component location.

A. Failure Modes

The most common failure observed was trace/pad breakage at the neck from the trace to pad as shown in Figure 9. The dyed area in the right of Figure 9 shows the resin cracked under the copper pad on the board side. The trace break was mainly due to the cohesive failure of resin between the copper pads and the fiberglass dielectric layer. Figures 10-12 show cross-sectioned solder joints where resin cracking is visible underneath the pads in the dielectric layer. The pad cracking was commonly seen for both boards with and without edge bonding. Similar failure mode of trace broken has been reported by Chong, et al. [24], and the resin crack been observed by Mattila, et al. [16], Chong, et al. [24] and Wong, et al. [25].

All the components examined by dye penetrant that were electrically failed were categorized as solder failure, trace

failure, both, or unknown. Of those components with electrical failure:

- 58% showed I/O trace failure with cracking under pads
- 12% showed solder joint fracture on the board side
- 19% showed both solder joint fracture and I/O trace failure
- 11% showed daisy chain trace failure and pad cracking

The 58% of electrical failures were due to one or two input/output trace connections broken away from the copper pad. Another 11% had pad cracking that led to daisy chain trace failure within the array (not at the I/O traces). The large ratio of electrical failures resulting from I/O traces cracked away from pads compared to solder joint fracture may be partially related to the test vehicle design and trace routing. Figure 13 shows a single CSP pad location with all four corners where corner 2 has two traces running outward from the component. These two traces are the daisy-chain input and output connections. Traces connected to the other three corners lead to test pads and are not part of the daisy chain. The orientation of every package on the test vehicle is the same, with corners 1 and 2 parallel to the short board axis, corners 2 and 3 parallel to the long board axis, and the orientation of the trace layout is also the same for each. Due to resin crack under the copper pad, the transition of the trace to the I/O pad is the weakest point, which causes copper trace/pad cracking. A copper pad crater and part of one of the corner 2 I/O traces is shown in Figure 14, which is the board side match of the failure shown in Figure 9. The frequency of this failure indicates that if the corner solder joint pads were allowed to lift off the board while maintaining electrical continuity (the daisy chained trace between solder pads may lift up), then the drop impact reliability of the assembly might be overestimated. A test vehicle utilizing typical PWB layout for CSPs in electronic devices, such as traces to vias rather than pad to pad daisy chains, may be more appropriate for evaluating board level drop impact reliability.

The secondary failure mode was solder joint fracture. Figure 15 shows a fracture near the board side Cu_6Sn_5 intermetallic layer. Solder fracture failures were observed at the board side only and no solder failures were found at the component side. Both complete and partial solder fractures were found by dye penetrant analysis as shown in Figure 16. It is interesting to note that both a solder joint fracture and a broken trace can lead to electrical failure as shown in Figure 17. The pad on the left side of the image in Figure 16 has resin cracking which led to trace breakage as the pad lifted away from the board with the component during board deflection.

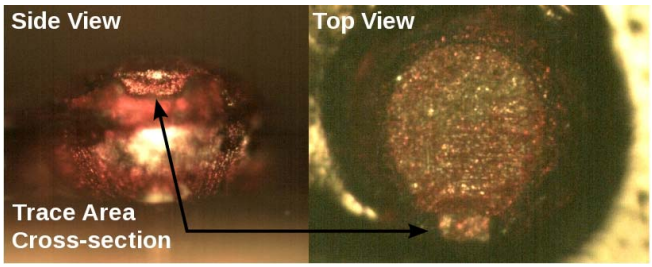

Figure 9. Trace cracked away from solder joint (left) and the same solder joint with pad dyed (view of component surface)

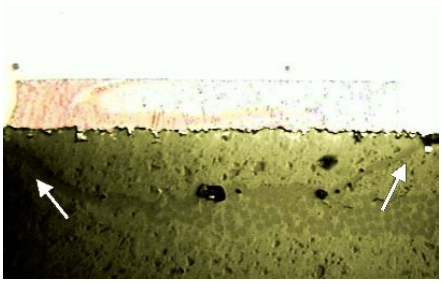

Figure 10. Cracked resin under the board side pad (dark line), edge bonded

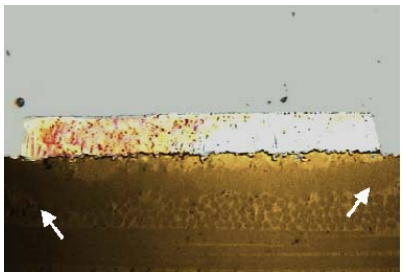

Figure 11. Crack in board resin underneath pad (thick dark area), no edge bond

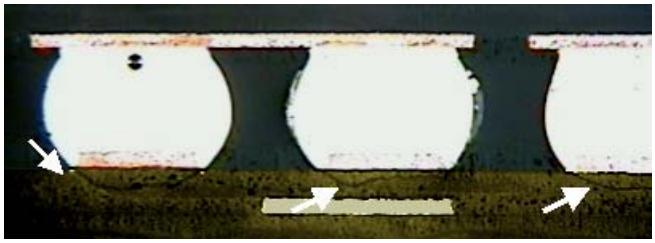

Figure 12. Cracked resin layer under pads for several solder joints, edge bonded

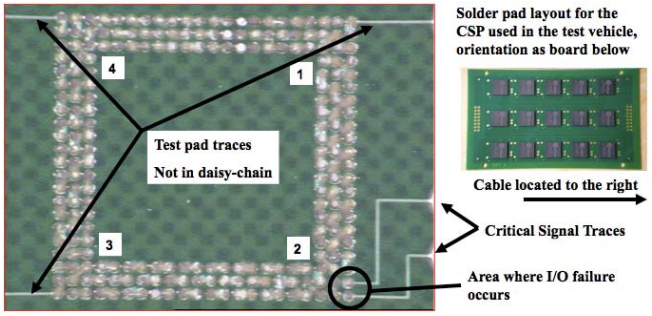

Figure 13. CSP I/O traces and component orientation

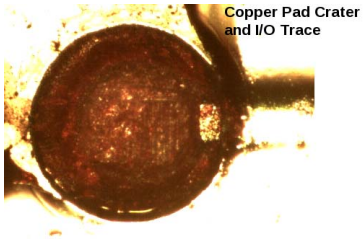

Figure 14. Copper pad crater with dyed board fibers

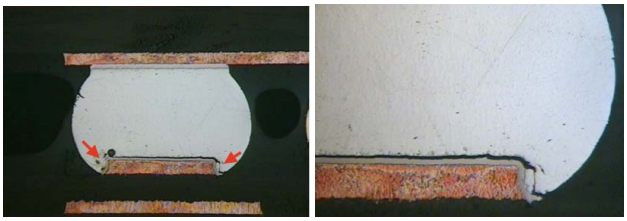

Figure 15. Solder joint fracture near the board-side IMC layer

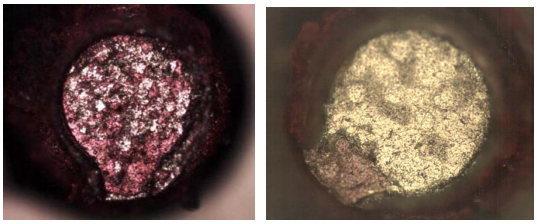

Figure 16. Complete fracture (left) and partial fracture (right)

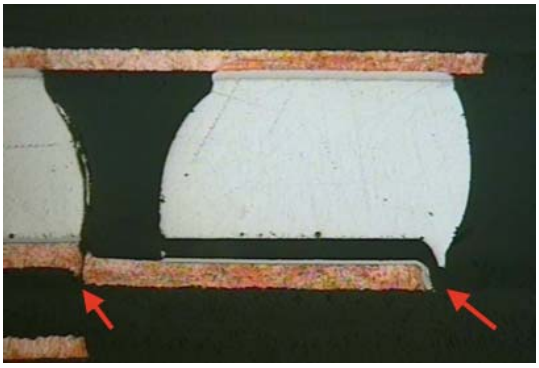

Figure 17. Board side solder fracture and broken trace

The extent of resin cracking under copper pad was examined for all components of the eight boards that were dye penetrant tested. Out of these 120 components (15 components per board times 8 boards), the relationship between electrical failure and resin cracking is summarized in Table 6. Table 6 shows that 72% of components were electrically failed and had resin cracking under the copper pad, while 19% of components were not electrically failed but had resin cracking. The remaining 9% of components did not have resin cracking. This indicates that the solder joints are not the weakest link area of the assembly. It is recommended that board laminate materials be improved.

Table 6. Relationship between electrical failure & resin cracking

		Electrical failure	
		Yes	No
Resin cracking under pads	Yes	72%	19%
	No	6%	3%

B. Differences between edge bond material failures

There are notable differences in the mechanical failure mode between the two edge-bond materials. The epoxy material tends to fracture through the edge-bond material as shown in Figure 18. More than 20 components that were edge bonded with the epoxy material, or more than 10% of all the components in the group, dropped off the board during testing. This fracturing was observed to occur before electrical failure happened. The acrylic edge-bond material did not fracture, but delaminated from the package sides. The acrylic was not observed to be delaminated from the board surface. Figure 19 shows that four undamaged edge bonds remained on the board after the component fell off. The properties of these two edge-bond materials are believed to contribute to the difference in the mechanical failure mode.

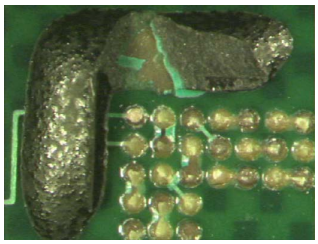

Figure 18. Fractured thermally cured epoxy edge bond

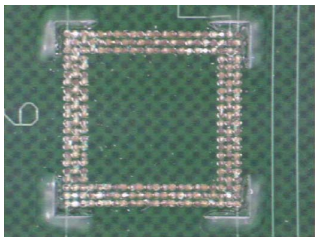

Figure 19. Four UV cured acrylic edge bonds on a board

VIII. Conclusions

The drop test reliability of 0.5mm pitch CSPs assembled on the JEDEC test vehicle with lead-free SAC305 solder are studied by two failure detection systems. The following conclusions can be drawn from this research:

1. The component location plays a significant role in the drop test reliability. Generally speaking, components at the center of the board are more prone to fail due to higher strains. But the differences in drops-to-failure between the two different failure detection systems indicate that additional mass on the board changed the distribution of strains along the board, which resulted in different failure locations.
2. Higher impact force or G-level resulted in lower drops-to-failure. But there are large variations in drops-to-failure between different boards under the same drop conditions.
3. Edge bonding can significantly improve drop test reliability. The edge bonded CSPs typically survived 5 – 8 times longer at 2900G-0.3ms drop impacts, and 8 – 10 times longer at 1500G-0.5ms drop impacts. But the performances of the two different edge-bond materials are different.
4. The majority of drop test failures were trace breaking caused by cohesive failure of resin between the copper pads and the fiberglass dielectric layer. This indicates that solder joints are not the weakest link area of the assembly. This pad cratering issue suggests that PCB laminate materials should be improved and the laminate specification and testing method should be included in a future JEDEC drop testing standard.

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