Light Extraction Improvement of GaN-based Light Emitting Diodes using Patterned Undoped GaN Bottom Reflection Gratings

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ABSTRACT

The Gallium Nitride (GaN) Light-Emitting-Diode (LED) bottom refection grating simulation and results are presented. A microstructure GaN bottom grating, either conical holes or cylindrical holes, was calculated and compared with the non-grating (flat) case. A time monitor was also placed just above the top of the LED to measure both time and power output from the top of the LED. Many different scenarios were simulated by sweeping three parameters that affected the structure of the micro-structure grating: unit cell period (A) from 1 to 6 microns, unit cell width (w) from 1 to 6 microns, and unit cell grating height (d) from 50 to 200nm. The simulation results show that the cylindrical grating case has a 98% light extraction improvement, and the conical grating case has a 109% light extraction improvement compared to the flat plate case.

Keywords: Gallium Nitride, light-emitting-diode, grating

1. INTRODUCTION

As a result of our energy conversation efforts, lighting sources have become one of the hot areas of research due to their applications in a variety of fields such as lighting displays, bulb technology, and photonics. The demands of these applications require low power consumption, yet a high brightness and luminosity with minimal heat. We can even control the color contrast of the device and create a full color set with red, green, and blue Light-Emitting-Diodes (LEDs) [1]. LEDs have been used in many applications, however the light extraction efficiency is still very low for GaN LEDs due to several factors: Gallium Nitride (GaN) has a low critical angle that traps light inside the device [2], absorption of light within the device due to dislocations and defects within the GaN crystal [3], and device design and structure has not been optimized (ie. epitaxial side up vs. epitaxial side down chip structures) [4]. It is crucial that we improve GaN LED light extraction efficiency and reduce energy consumption.

The major limitation to the light extraction efficiency is the light trapping due to GaN's low critical angle. This applies to any large change of the refraction index existing between layers, such as between the solid state LED and air, and the solid state LED and a resin. It has been shown that resins increase the extraction efficiency due to the more gradual change in refraction, allowing more light emitting out due to the larger escape angle [5]. Many methods of improving LED efficiency are currently being explored. Almost all of these methods are seeking to extract the trapped light in greater quantity and faster speed. Those methods being explored are placing photonic crystals or nanostructure grating on one of LED layers to modify the effective index of refraction at the boundary [6-7], randomized roughening on the surface of the device [7-8], slanted device configurations that result in pyramidal shapes [7], and inverted "flip-chip" designs that put the epitaxial side upwards or downwards [4] [9].

The second inefficiency of GaN LEDs is the loss of light from absorption due to dislocations and defects within the GaN crystal. These are impurities that absorb the light, an issue when light is trapped inside the LED. The longer it takes to extract the trapped light, the more the photons suffer from absorption. So, it is critical that we find methods to extract light quickly from the LED before the energy is taken by absorption [10-11]. A grating structure helps

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solve this issue by creating more angles of escape. Various structures exist, such as conical, pyramidal, spherical, cylindrical, and so on, but only a few can be realized with current fabrication techniques. To help mitigate losses due to absorption and facilitate the quick extraction of photons, gratings can be patterned on the surface of or within the layers of the LED device, providing more escape angles than flat interface. For example, through modified laser lift-off (M-LLO), air holes at a 4 micron period are patterned on undoped GaN (U-GaN) instead of just roughening the surface of an LED. The technique uses a sapphire backplane, UV light, and a high power KrF laser to etch the nanostructure onto U-GaN [12]. In the experiment of PKU, grating depths varied from 75nm to 120nm [12]. Other fabrication techniques exist such as imprint lithography that can produce similar air holes that measure 180nm in diameter, with a depth of 100nm, and a period of 295nm [13]. Our simulations will be based off of the M-LLO manufacturing process of PKU [12], a model with a patterned U-GaN bottom grating layer attached to a reflective Ag film is persented. The grating height plays a role in transmittance and reflection, since the larger the grating height, the more gradual the effective refraction index will be, and hence, the more photons that will be transmitted versus reflected and absorbed by impurities [6] [14].

The light trapping issue is commonly solved by etching a periodic structure at the light extraction surface and/or the bottom reflective layer of the LED [2]. This paper focuses on micro-scale grating structures at the bottom of the device. To simulate the effects on extraction efficiency, we use a Finite-Difference Time-Domain (FDTD) GaN LED model at 460nm wavelength to study different reflection gratings. The GaN reflection gratings using cylindrical-hole bottom, conical-hole bottom, and non-grating structures are simulated and optimized. In the paper, the simulation model is presented in section 2, simulation results are presented in section 3, and the conclusion is in section 4.

2.   SIMULATION MODEL

The presented simulation model accounts for the effects of refraction in device materials, reflection due to linear dispersion or total internal reflection, transmission of escaping light from the LED, and scattering at the grating [3]. The form of analysis used in the simulation is the common solution for the light wave propagation in arbitrary geometries, the Finite Difference Time Domain (FDTD) technique. This allows for the most accurate solution, since FDTD is based directly on Maxwell's curl equations, which can accurately calculate all four of the above cases. In conjunction with Maxwell's equation, a Yee mesh is used (shown in Fig. 1), which enables analyzing the electromagnetic fields on a grid of three-dimensional space and time. By defining an incremental variable for each parameter in space and time, namely Δx, Δy, Δz, and Δt, the E and H fields for a specified grid are obtained. The model allows simulations of any geometrical structure of LEDs. An important point to consider is that the smallest increment must be no smaller than the smallest feature of the structure, or the model will not be able to accurately calculate the exact features of the structure. The GaN simulation model has the parameters shown in Fig. 2. The actual LED is mounted on a very thick layer of Si submount with an Ag reflector plate directly on top of it. The Ag fills the U-GaN air holes in either a conical or cylindrical unit cell shape (only conical is shown in Fig. 2). Adding the submount layer will add a large amount of calculation times. However, the Ag is a strong reflective layer and effects of submount on the EM field are very trivial compared to other layers. Therefore, the submount is not included in the modal. Finally, an n-GaN, quantum wells, and p-GaN are placed on top of the grating. The time monitor is used to measure the time-varied light output of the whole device and is separated from the LED by a distance of 100nm.

The model has cylindrical holes or conical holes on the bottom of the undoped GaN layer as shown in Fig. 2 and Fig.3. The conical and cylindrical shapes represent Ag material, which is a reflective layer. For a visual representation of the grating types, the conical grating model is demonstrated in Fig. 3(a), while the cylindrical grating model is demonstrated in Fig. 3(b). To define a regular spacing between unit cells in a crystal lattice arrangement, we employ three parameters: unit-cell period (A), unit-cell height (d), and unit-cell width (w), all shown in Fig. 3. The unit-cell period is the length from center-to-center between unit cells. In 3-D, the parameter w, represents a diameter in the case of a circular structure (ie. sphere, cone, and cylinder) or a length of a side in the case of a box structure (ie. cube, rectangular cube). The unit-cell height d is the depth of the bottom hole. The limits of the parameters are the following: $50 \leq d \leq 200nm$, $w \leq A$ to prevent overlap, and the smallest element must be bigger than the smallest grid size. The grating height parameters, which are fabricated, range from 75nm to 120nm [12]. This determines our simulation rang. More over, the smallest grating height d value is determined by the minimum grid size limit. If d< 50nm, the simulation requires much smaller girds and simulation time. And our data

also show little improvement of light extraction at d smaller than 60nm. Further more, the width parameter must be less than or equal to the unit cell period since a larger value would indicate overlap of the cell structure, an invalid state. Finally, the last limitation is that the smallest element must be greater than or equal to the smallest grid size, as specified in the Yee's mesh simulation. If the grid was not fine enough to "see" the layer, then it may be missed when calculating for the E and H fields using Maxwell's curl equations. This also determines the minimum distance of the power monitor to the device in Fig. 2, which is set to 100nm above the LED. The detailed simulation values are shown in Table 1. Fractions of microns for A and w are allowed in the simulation, however they were not used. The overall size of FDTD simulation area is also fixed, which is $100\mu m \times 100\mu m$. If A=1μm, there are 100 unit cells. For A=6μm, there are only 16.67 unit cells. The grating is a squared matrix as shown in Fig.3. A point-source layer with constant wave is placed at the center of quantum well region.
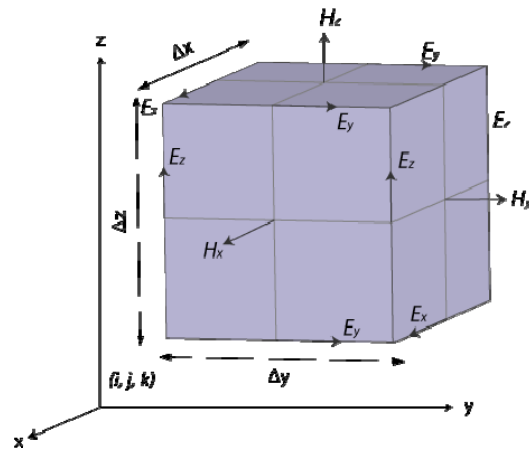

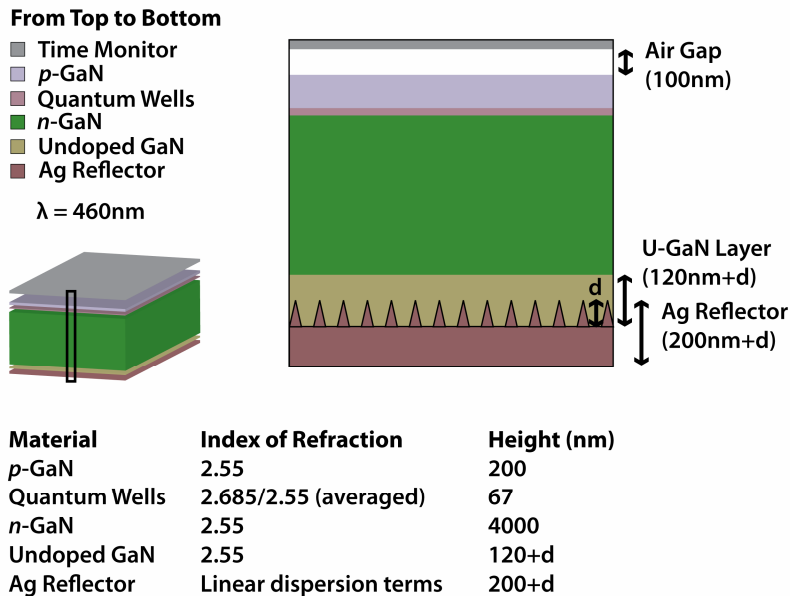
Fig. 1. Yee's Mesh Solution to Solve Maxwell's Equations

From Top to Bottom
- Time Monitor
- *p*-GaN
- Quantum Wells
- *n*-GaN
- Undoped GaN
- Ag Reflector

λ = 460nm

Air Gap (100nm)

U-GaN Layer (120nm+d)

Ag Reflector (200nm+d)

Material	Index of Refraction	Height (nm)
p-GaN	2.55	200
Quantum Wells	2.685/2.55 (averaged)	67
n-GaN	2.55	4000
Undoped GaN	2.55	120+d
Ag Reflector	Linear dispersion terms	200+d

Fig. 2. GaN LED simulation model

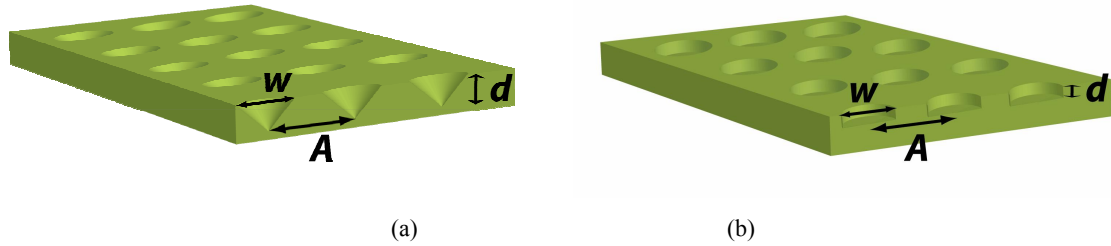(a)   (b)

Fig. 3. Grating unit cells shape on GaN material (bottom view): (a) Conical and (b) Cylindrical

Table 1. Range of the Simulation Parameters

GaN LED Model Simulation Parameters		
Simulation Parameters	Descriptions	Simulated Ranges
Parameter:	*Brief Description:*	*Range:*
A	The period of the unit cells	1 to 6 microns
w	The width of each unit cell	1 to 6 microns
d	The height of each unit cell	50 to 200 nm

3.   SIMULATION RESULTS AND DISCUSSIONS

The start of the simulation is when the LED turns on from an off state. There is a monitor at a distance of 100nm above the LED to collect the light emission. For each structure simulation, we must wait until the LED/monitor reach a steady state, after which we can extract the constant wave (CW) average power. Each simulation sweep of the parameters produces a set of 20000 data points (2000fs at 0.1fs/step), and from this data set, we determine average power over the last 500fs. In this range, maximum steady-state power is radiated due to the CW source and reflections from the grating. This procedure is done for each case.

Fig. 4 shows the results of a GaN conical-hole grating simulation, sweeping from A=1μm to A=6μm, w=1μm to w=6μm, and d=50nm to 150nm. Similarly, Fig. 5 shows the results of a GaN cylindrical-hole grating simulation, sweeping over the same range. The flat plate (non-grating) results are shown for each graph for comparison. The average powers in the plots are the maximum average output power of the LED on the last 500fs of the simulation at steady state. For the conical-hole grating, there is maximum light extraction around the grating height d=90nm. The average power increases as grating height increases when d<90nm, and the average power decreases as the grating height increase from 90nm to 150nm for most cases. For the same grating period, the smaller grating width achieves the better light extraction. For the transmission grating, the maximum transmission results from the largest grating width case [15]. In this paper, the reflection gratings are simulated. Since the reflected power summed with the transmitted power equals the total incident power, a maximum transmission structure is A=w. Then the maximum reflection grating structure must differ, and in fact be opposite, from the maximum transmission structure. When w increases at the same d, the total light extraction reduces and more approaches to the flat case. For the same A and w, the interface angle of the grating section changes when d varies. When d=0, which is flat case, there is no improvement. However, it is very hard to simulation small d values case. With d increasing, the interface angle increases, more light will be extracted at small d<90nm. When d is approaches infinite, the grating section is too thick and it is harder for the reflected light to pass through and be extracted. Therefore the light emission efficiency drops at higher d values. There is maximum design point for this particular structure, which is around d=90nm. The best case in our simulation is 109% light extraction improvement at grating period A=6μm, grating width w=1μm, and grating height d=90nm. For the conical-hole grating case, there are two effects of period width w: 1) The percentage of grating area compared to the total device area. If width w=0, there is no effects and no improvement

of the light extraction. When w increases from zero, more lights should be able to be extracted. However, we didn't simulation w<1μm (nano-structure). 2) For the same period A and grating height d, but different width w, the angle of the Ag and GaN interface are different. When w increases, the angle decreases and should be much closer to the flat case. Therefore, at large w, the light extraction should decrease as w increase. Summarizing above two cases, there is a maximum w design point for each grating, which should be shown in Fig. 6(a). However, our data is only calculated down to w=1μm gating. The maximum grating design should be somewhere below 1 μm (nano-structure). But for the fabrication view point, it is not necessary to design the grating to nano-structure at our current fabrication capability. In the theoretical part, the other factors should also be considered for the nano-grating design, i.e. the structure is compatible or smaller than the light wavelength.

For the GaN cylindrical hole grating simulation, shown in the Fig. 5, if the grating width w equals to the grating period, there are very little light extraction improvement. In most case, the light extraction efficiency is even worse compared to the no grating case. Light emission improvement can only be achieved at w<A cases. Similar to the GaN conical hole grating simulation, the smallest grating width produces the highest average power output. There are two cases, which give the maximum average power output: one is 97.9% light extraction improvement at the grating period A=2 μm, grating width w=1 μm, grating height d=60nm and the other is 94.8% light extraction improvement at the grating period A=6 μm, grating width w=1 μm, grating height d=90 nm. For the cylindrical grating, w=A is a very special case, since the shape of the grating is totally different. There are only four separated islands of GaN on the four corners of the unit cell. Our results show this case is worse than the flat surface interface. Our data also show that the small grating period is not preferred for the micro-grating design, such as A=1 and 2 μm. This is contrast to conical case, for A=1 or 2μm, there are still reasonable grating design at d=90nm.
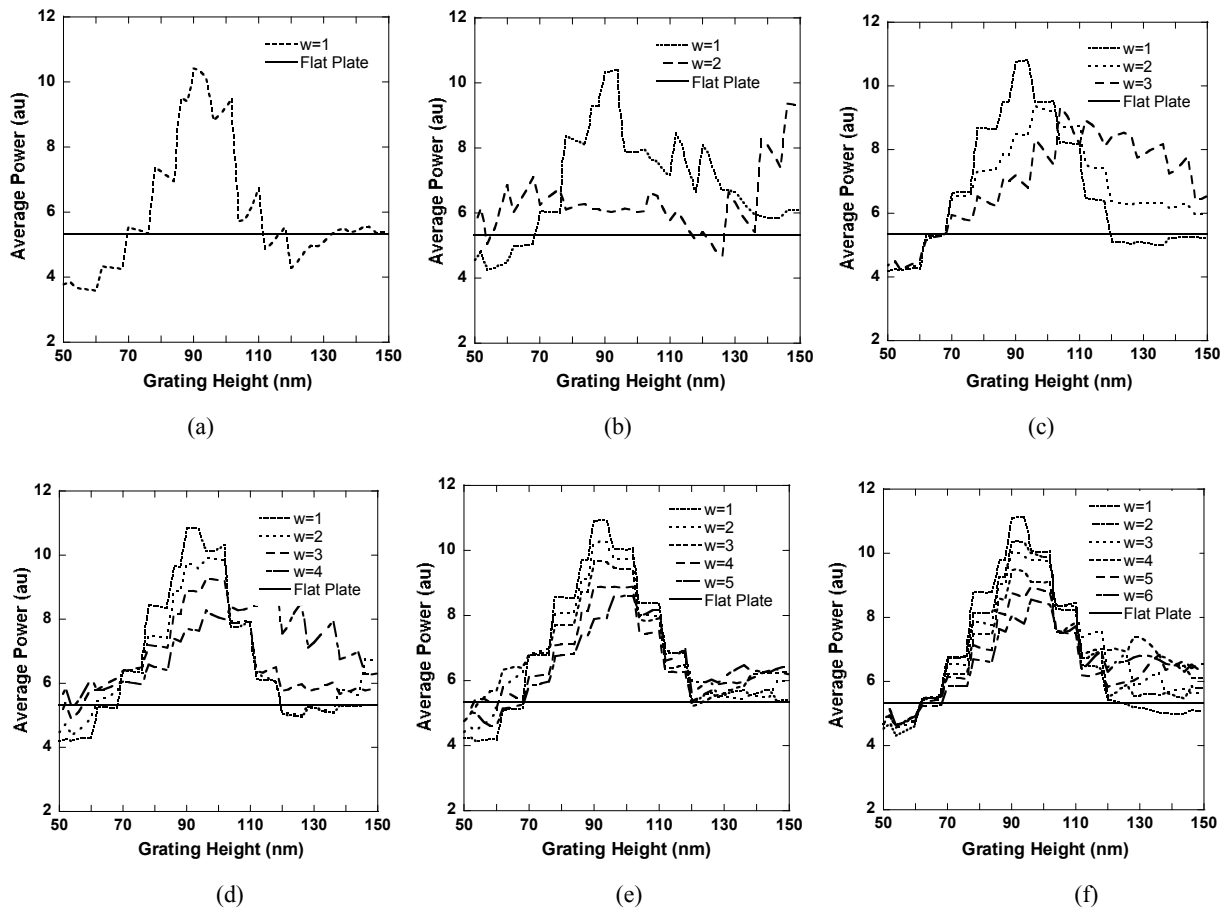

Fig. 4. Average power for the conical hole grating Case: (a) A=1, (b) A=2, (c) A=3, (d) A=4, (e) A=5, and (f) A=6 μm.

The summary of maximum power for the GaN conical- and cylindrical-hole grating is shown in Fig. 6. In general, larger grating periods have higher maximum power for both cases. This is a very important result to guide our fabrication and design. This implies that the large-grating design is preferred in micro-levels. The maximum power linearly decreases with increase of grating width w. Compared to cylindrical-hole grating, the conical grating maximum power is higher at larger w value. The conical gratings are less sensitive to A and w values for the maximum power output, which is also preferred by fabrication. For smaller grating width, i.e. w=1 μm, the two cases (conical and cylindrical) has little difference, which is also shown in Fig. 7. Since w=1 μm case is the best case for most circumstances, the comparison of the conical- and cylindrical-hole grating for the w=1 μm case is shown in Fig. 7. For the simulated range, Fig. 7 (a) shows the peak power generated by each unit cell shape and for each grating period. Also, the grating heights in nm for those maximum powers are shown in Fig. 7(b), also plotted against the grating period A. The cylindrical grating case has a 98% improvement compared to the flat plate case at a grating period of A=2μm, and a unit cell width of w=1μm. The conical grating has a 109% improvement compared to the flat plate case at a grating period of A=6μm, and a unit cell width of w=1μm. However, the maximum power or peak power locations are almost same, round the grating height d= 90nm for both grating cases at larger grating period (A>2μm). In the other words, the optimized the grating height is 90nm for most cases. In summary, it is better design the reflection gratings (conical or cylindrical) at larger grating period A=6μm, smaller grating width w=1μm, and the grating height d round 90nm. Compared to cylindrical gratings, the conical grating has more design tolances on the grating width w and period A.
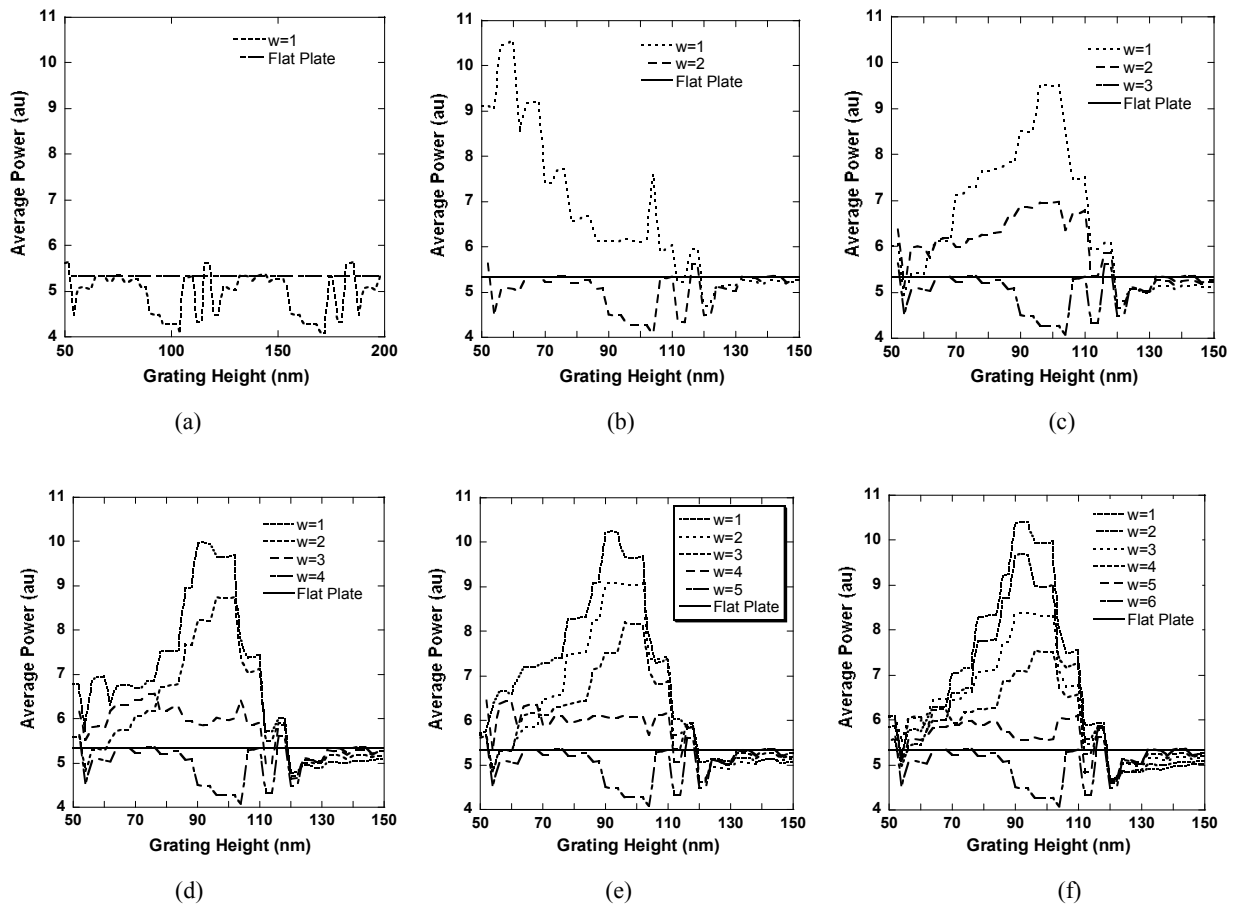

Fig. 5. Average power for the cylindrical grating case: (a) A=1, (b) A=2, (c) A=3, (d) A=4, (e) A=5, and (f) A=6 μm.
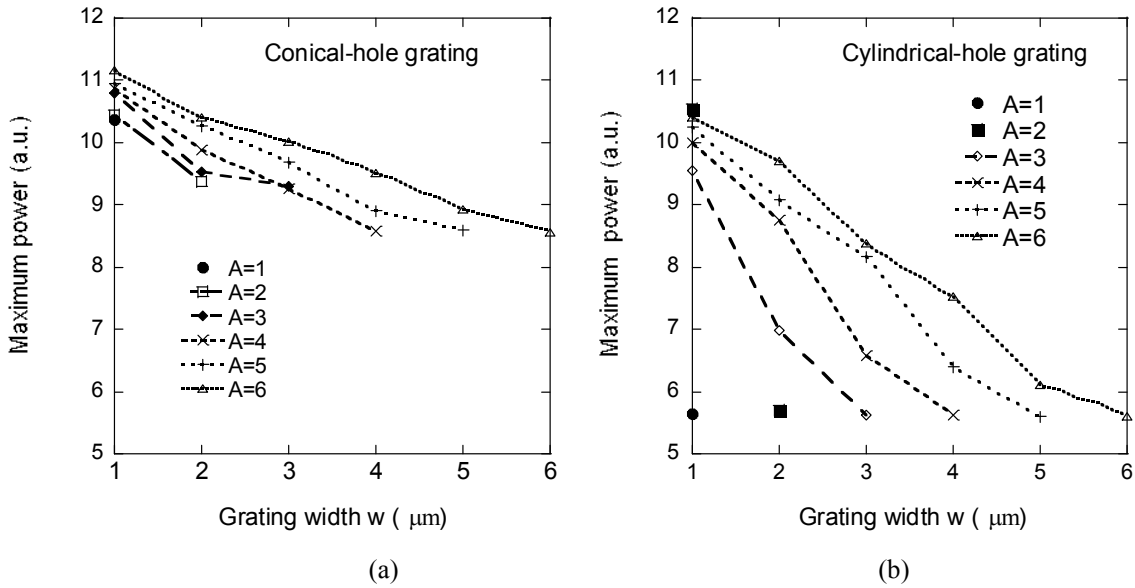
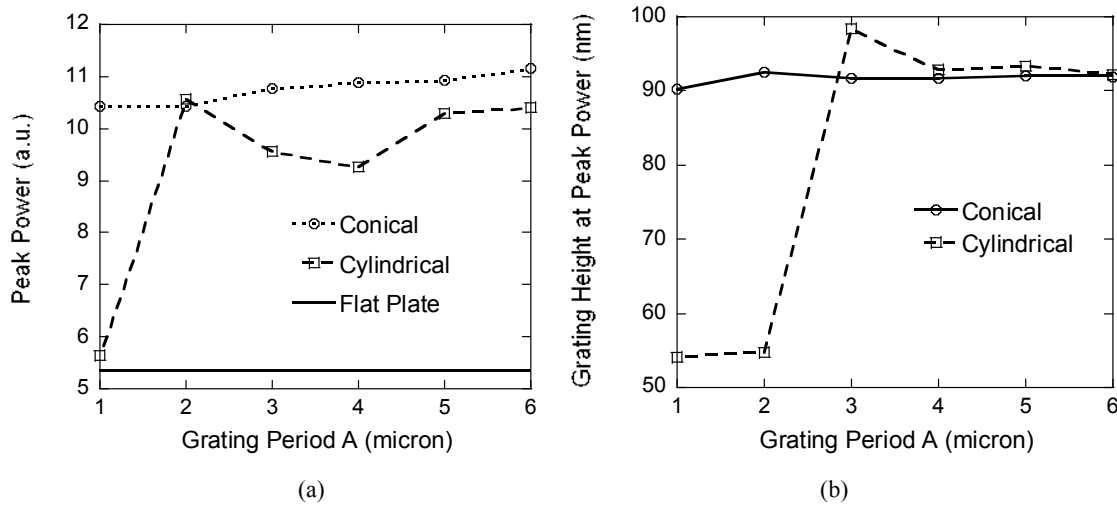Fig. 6 Maximum power for each grating period A and grating width w: a) conical-hole grating and b) cylindrical-hole grating.

Fig. 7. Comparison of the conical- and cylindrical-hole grating for the w=1μm case (a) peak power and (b) the grating height at peak power.

4.   CONCLUSION AND FUTURE WORK

A simulation model using FDTD and Yee Mesh to calculate GaN LED light extraction efficiency was used. Three grating parameters: A, w, and d are studied. The simulation results show that the cylindrical grating case has a 94% improvement of the light extraction, and the conical grating case has a 109% improvement compared to the flat plate case. The highest efficiency in a reflection grating results when w=1μm. As w becomes small compared to A, the maximum average output power increase. For both conical- or cylindrical-hole reflection gratings, it is better design the reflection gratings at larger grating period, (i.e. A=6μm), smaller grating width, (i.e. w=1μm), and the grating height d round 90nm.Our simulation didn't reach the optimized w value, which should be less than 1micron. However, when simulating grating with w<1μm, nano-grating characteristics should be addressed, which is our

future work. Further more, other grating matrix, such as triangular matrix, hexagon matrix, 8 Quasi-periodic Photonic Crystals (QPCs), and 12QPCs, should also be investigated in the future as well.

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