Constant Conduction Angle Biasing for Class C Monolithic RF Power Amplifiers

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ABSTRACT

Constant Conduction Angle Biasing for Class C Monolithic RF Power Amplifiers

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In modern wireless communication systems, a base station typically serves a few hundred users within its cell coverage. To combat the near-far problem – the situation where a nearby user's strong cellular signal masks the cellular signal of a faraway user – base stations continually enforce power control. That is, nearby users must lower their transmit power. In CDMA technology, power control can be as large as 70-80dB. At low power outputs, this greatly impacts the performance of the RF power amplifier (PA) in the cellular device. For small RF drives, the magnitude of the output RF current approaches the magnitude of the DC current and thus the efficiency suffers. Operating the RF PA in class C operation improves the efficiency, but results in poor linearity.

Several methods of so-called dynamic biasing have been proposed. These strategies entail lowering the bias of the PA as the RF drive increases. The proposed methods, however, fail to explain how to achieve linearity and low third-order intermodulation distortion. Additionally, the methods utilize open-loop implementations.

This work presents a novel dynamic biasing topology that results in a much improved linear class C PA. The topology utilizes a closed loop that cleverly senses the operating conditions of the "power device." Particularly, the loop operates on the principle of keeping the conduction angle remarkably constant and thereby ensuring linearity. The work details a thorough design methodology that should provide assistance to a designer wanting to implement the topology in an RF integrated circuit. Agilent ADS simulations and laboratory results from a functional PCB prototype bring merit to the topology.

Acknowledgments

This project would not have been possible without the guidance and gracious support of many individuals. Special thanks should be given to my advisor, Dr. Vladimir Prodanov, whose guidance was essential to the progress of this project. I also want to thank the Electrical Engineering Department Faculty at Cal Poly who provided me with opportunities to explore and utilize practical and theoretical knowledge in the subject of electrical engineering. A round of regard goes to my fellow electrical engineering colleagues – Matthew Bloom, Ervin and Yuri Carrillo, Kenny Schmutz, Tom Poonsopin, Eric Escudero, Jong Aquino, Matthew King, and everyone else – who have been a pleasure to study alongside over the course of my years at Cal Poly. Although it goes without saying, but I must thank my parents for everything they have provided for my sister and me.

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This thesis is dedicated to Satguru without whom none of this would be possible.

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1

Introduction

1.1 Introduction

Amplification of electrical signals has played an important role in electronics ever since the invention[1] of the vacuum tube triode (originally named the Audion) by Lee de Forest in 1906 [1]. Particularly, power amplifiers (PAs) played a significant role in the development of radio, television, and telephone communications in the last century. The main reason for their significance comes from the fact that as waves and signals propagate in electrical circuits, coaxial cables, or in the air as radio waves, they suffer attenuation. Thus, they require suitable amplification to be interpreted by the receiver. In the early days, electrical engineers formulated “recipes” for designing PAs using vacuum tubes. The design methodology matured with the advent of the solid state transistor. At the end of the 20th century and the beginning of the 21st century, the introduction of integrated circuit (IC) technology and consumer demand in cellular technologies brought new challenges in PA design.

[1] Robert von Lieben also developed a triode independently around the same time. As politics would have it, this incited a lawsuit between the two [4].

To ease the reader into the PA design methodology, this chapter begins by covering the essential PA basics. It then delves into the different PAs classes, the "hockey-stick" shaped I-V transistor curve, and the power control dilemma in modern wireless communications. The chapter concludes with a summary of the prior art.

1.2 Background

1.2.1 Radio Frequency (RF) PAs Basics

High power control enforcement and high peak-to-average power ratios (PAPR) in modern digital communications present significant technical challenges in RF PA design. RF PAs used in cellular technologies typically operate with an output power range of 0-30dBm [1]. Table 1.1 shows the frequency band allocations for a few wireless standards. This table reveals the narrowband nature of these RF signals, having a worst-case relative bandwidth of 4.4%. Under narrowband conditions and over a short number of the carrier cycles, these RF signals are practically sinusoidal. The magnitude and the phase of the signals change slowly over many carrier cycles. This crucial point validates analyzing PA circuits under sinusoidal operating conditions [1].

Table 1.1 Frequency Bands and Available Bandwidths for Common Wireless Systems. Adapted from *"Power Amplifier Principles and Modern Design Techniques,"* by V. Prodanov & M. Banu, 2008, *Relative Signal Bandwidth for Most Modern PAs.* Copyright 2008 by Taylor & Francis.

	Licensed Bands				
	US Cellular	**R-GSM**	**DCS**	**PCS**	**IMT2000**
Uplink (MHz)	824-849	876-915	1710-1785	1850-1910	1920-1980
Downlink (MHz)	869-894	921-960	1805-1880	1930-1990	2110-2170
Total BW (MHz)	25	39	75	60	60
Relative BW (%)	~3.0	~4.4	~4.3	~3.2	~3.1

	Unlicensed Bands		
	ISM-2.4	**UNII-5.2**	**UNI-5.8**
Carrier (MHz)	2400-2483.5	5150-5350	5725-5825
Total BW (MHz)	83.5	200	100
Relative BW (%)	~3.4	~3.8	~1.7

1.2.2 Does a "Power Amplifier" Amplify Power?

In the first part of the 19th century, James Prescott Joule performed a series of experiments studying the nature of heat. His study led to the theory of conservation of energy, thus leading to the formation of the first law of thermodynamics. Put simply, the theory of conservation of energy states that within an isolated system, energy can neither be created nor destroyed; the total energy of the system must be conserved. The energy, however, may take several forms (e.g. heat, mechanical, or electrical) and can change from one form to another, as long as total energy of the system is conserved.

When designing robust engineering systems, we would like 100% conversion of energy from one form to another ("conversion" efficiency). However, in practice, this is hardly the case. For example, conventional gasoline engine vehicles convert chemical energy from the petrol or diesel to power at the wheels with efficiencies of 17-21%; On the other hand, electrical vehicles convert energy from the DC battery to power at the wheels with efficiencies of 59-62% [2]. In the aforementioned cases, the energy not converted to the power at the wheels is converted to heat[2].

So, returning to the primary question of this section: does a power amplifier amplify power? The answer is no; it simply converts direct current (DC) power supplied by the power lines to RF[3] signal power under the control of the RF input. As a result, the RF power delivered to the load is larger than the RF power consumed at the input of the PA. Figure 1.1 shows the practical flow of power in a RF PA. The flow of power expressed in equation form follows:

$$P_{RFin} + P_{DC} = P_{RFout} + P_{Loss}(Heat) \tag{1.1}$$

[2] Since conventional gasoline engines are inefficient, they emit a lot of heat.
[3] RF describes a subset of alternating current (AC) waves – those with oscillation rates in the range of 3kHz to 300GHz [3].

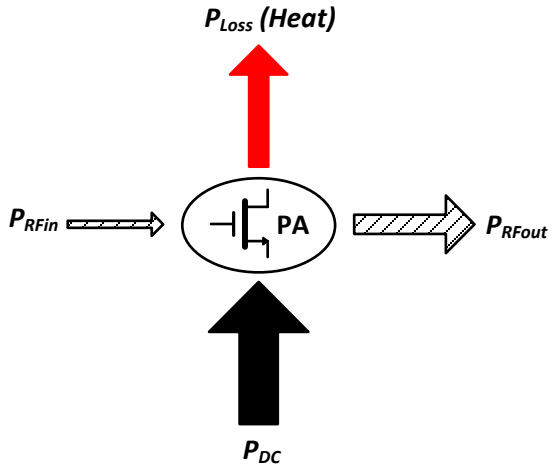

Figure 1.1 Power flow in a practical RF PA.

1.2.3 Single-Transistor PAs, Efficiency, & Linearity

Figure 1.2 shows a traditional single-transistor PA. The DC biases are provided through the RF chokes (RFCs)[4]. At conventional RF frequencies, the electrical length of the interconnected wires become significant in comparison to the wavelength and thus we must consider matching the input impedance, in addition to the output impedance, in order to obtain high return loss and maximum power transfer [3]. RF devices are typically matched to 50 or 75Ω because interconnections such as coaxial cable tend to have optimum power handling and low loss (dB/meter) at these impedances [4].

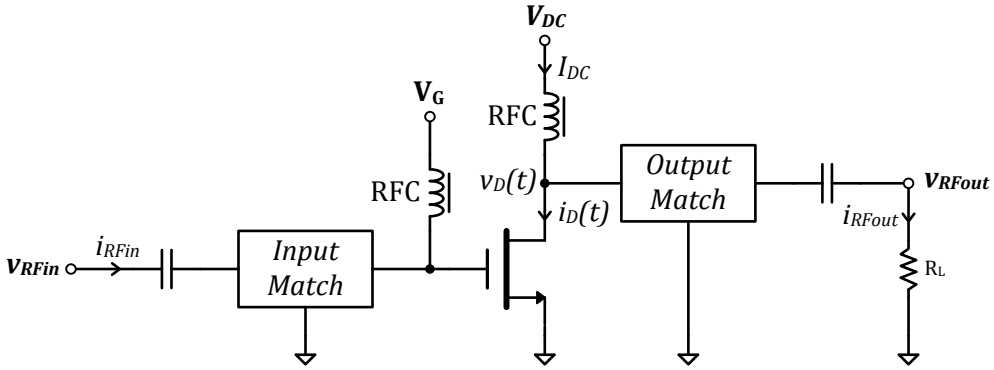

Figure 1.2 A single-transistor current PA.

[4] RF chokes block RF current from passing through, but allow DC current to pass.

In order to evaluate the performance of the PA, we consider two power efficiency metrics:

$$PE = \frac{P_{RFout}}{P_{DC}} \tag{1.2}$$

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \tag{1.3}$$

Power Efficiency (PE) refers to how efficiently the DC power from the power supply is converted to output RF fundamental[5] power. Power Added Efficiency (PAE) takes into consideration the power consumed at the input. Observing Figure 1.2, we write several power relations:

$$P_{DC} = V_{DC} I_{DC} \tag{1.4}$$

$$P_{RFout} = \frac{1}{2} v_{RFout} i_{RFout} \tag{1.5}$$

$$P_{Loss} = \frac{1}{T} \int_0^T i_D(t) v_D(t) \tag{1.6}$$

In regards to a linear PA, the input and output power are clean RF band-pass signals with no harmonics. These types of PAs are operated in the linear region of the transistor I-V curve in order to provide linearity; however, they are inherently inefficient with a theoretical maximum obtainable efficiency of 50%. PAs operated in the nonlinear region tend to have much higher efficiency (theoretically approaching 100%), but tend to produce significant harmonic content. This paper addresses an amplifier that is internally highly nonlinear, but quite linear in terms of the system input-output relationship.

[5] We hope to design a linear system and filter out any harmonic when operating the transistor in a nonlinear mode.

1.3 PA Classes & the "Hockey-Stick" I-V Curve

1.3.1 PA Families

Depending on how transistor PAs are operated, they fall under certain "class" designations (i.e. A, B, C, etc.). The PA family tree in Figure 1.3 shows that PAs divide into two branches depending upon how they are operated. If we operate the main amplifying transistor as a V-I converter, the device is known as a current PA and operates on the principle of the conduction angle (θ). Class A, B, and C PAs fall into this category; this is the focus of the following section. If, however, we operate the transistor as a switch, the device is known as a switching PA; these include classes D, E, and F. Since these PAs are by definition, overdriven, they cannot process amplitude modulated signals such as nQAM (*n* quadrature amplitude modulation) used in LTE [5].These amplifiers find application in single channel or constant envelope systems that utilize FSK, GMSK, QPSK, or DQPSK [6]. The work in this paper is concerned with the first branch of the PA family tree, or the current PAs.

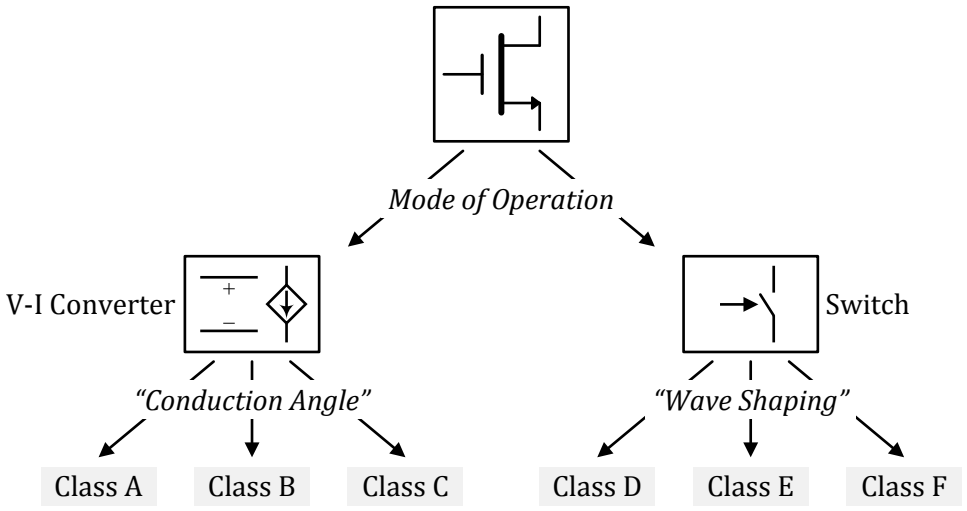

Figure 1.3 PA family tree. Adapted from *"Power Amplifier Principles and Modern Design Techniques,"* by V. Prodanov & M. Banu, 2008, *Types of PAs and the Concept of Conduction Angle.* Copyright 2008 by Taylor & Francis.

1.3.2 *Class A, B, & C Operation & the "Hockey –Stick" I-V Characteristic*

To understand how class A, B, and C PAs work, we need to look at the I-V transistor characteristics of the transistor device. Figure 1.4 shows an idealized I-V curve for a FET device, which relates the drain current to the gate voltage[6]. Biasing the amplifying transistor in the linear portion of the curve results in class A operation, biasing at the knee[7] results in class B operation, and biasing below the knee results in class C operation. The theoretical maximum efficiency is 50% for class A, 78.5% for class B, and asymptotically approaching 100% for class C. Class A is characteristic of a drain current with a DC level that remains constant regardless of drive. In class B operation, however, the DC level of the current changes with drive. For class C operation, the DC level and the conduction angle of the current change with drive.

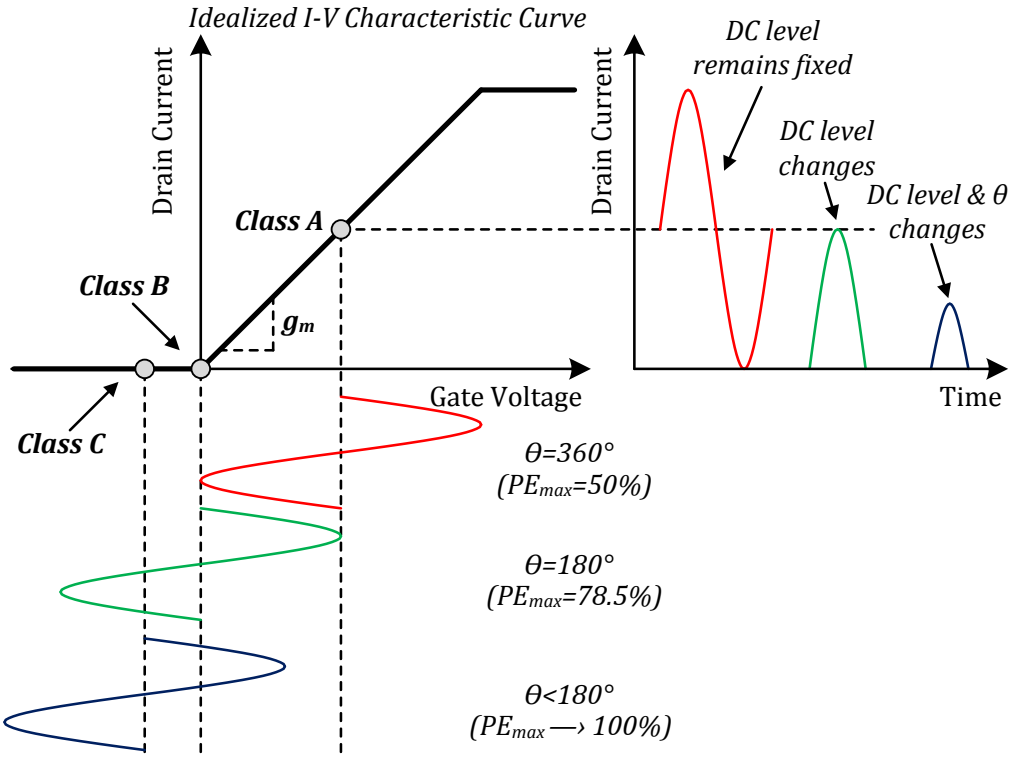

Figure 1.4 Class A, B, & C operations on an idealized I-V transistor characteristic.

[6] A PA device is biased in active move to utilize a transistor's amplifying ability.
[7] The knee is the point at which the idealized curve goes to zero.

Figure 1.5 illustrates the aforementioned characteristics of class A, B, and C operations.

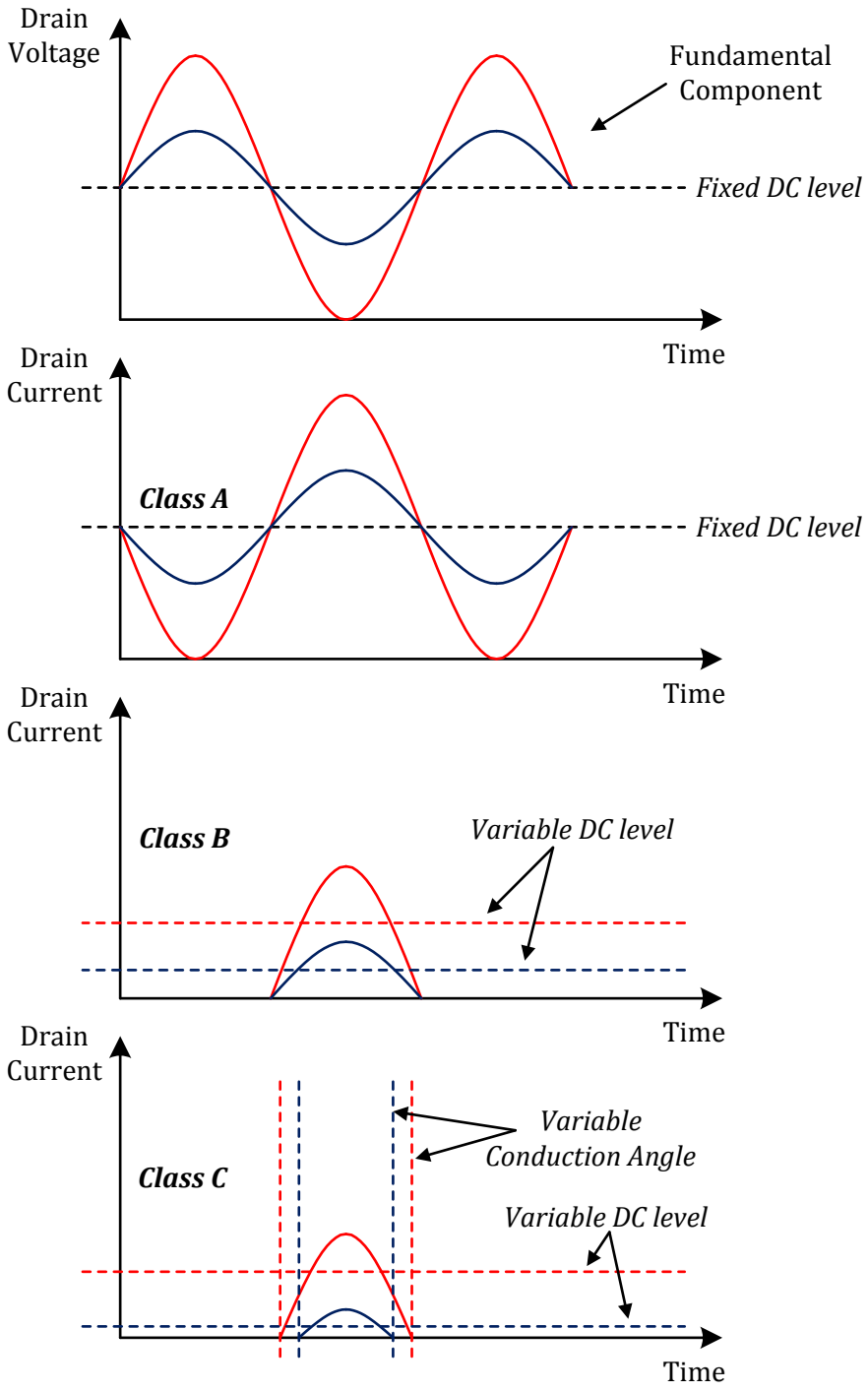

Figure 1.5 Drain voltage and current characteristics for Class A, B, & C operations.

Observe that the ideal I-V curve shown in Figure 1.4 has a sharp knee. Realistic transistors, however, have a more gradual turn-on – their I-V characteristics have a soft knee as shown in Figure 1.6. This characteristics is “weakly” nonlinear as opposed to the ideal characteristic presented earlier.

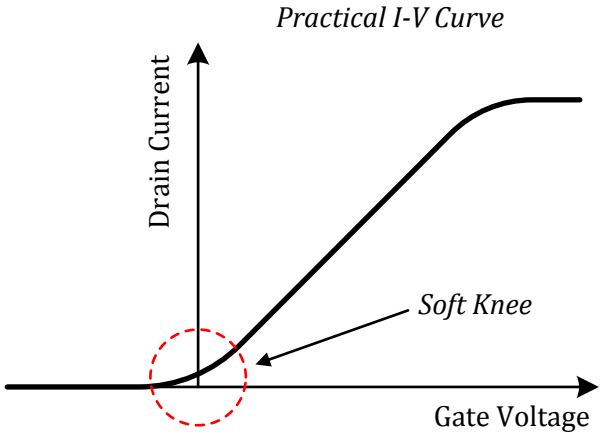

Figure 1.6 I-V curve of a practical transistor.

1.4 Challenges in Wireless Communication PAs

1.4.1 High Peak-to-Average Ratios

In modern wireless communication systems, we encounter digital modulation schemes that have high peaks relative to the average signal level over many cycles of the carrier. The figure of merit that quantifies this is the peak-to-average ratio (PAR). High PAR presents challenges in designing linear and efficient PAs. Particularly, the small and large signal components of the composite digital signal must amplify in the same dose to ensure linearity. Overall linear operation will hold true for class A and even class B operation, but we encounter issues operating the PA in Class C operation. The design methodology presented in this paper attempts to address this issue. The next section deals with power control - perhaps the most challenging issue in designing PAs for wireless communications.

1.4.2 Power Control

A typical base station may serve a few hundred users within its cell coverage. The most pressing issue with handling all the users is the so-called near-far problem. This problem entails the condition where the base station receives a strong signal from a nearby user and in the process masks a weaker signal from a faraway user. Since CDMA shares the same transmission bandwidth and timing, this problem greatly afflicts CDMA systems [7]. Due to this near-far problem, base stations enforce power control. Table 1.2 shows power control specifications for several wireless standards. As mentioned power control is critical for CDMA – it requires 70-80dB of power control. This power control and its corresponding PAR present significant difficulties in the design of RF PAs.

How does power control affect the performance of an RF PA? In this discussion, we refer to Figure 1.7. Initially, assume that the nominal output power corresponds to the RF input drive shown in red. This results in a drain current with a peak current much larger than the DC bias current. Assuming the peak fundamental component[8] (half the peak current for class B operation) is also much larger than the DC current, the PA operates efficiently. The PE is proportional to the ratio of the peak fundamental RF current to the DC bias current.

$$PE \propto \frac{i_{RF,0}}{I_{BIAS}} \tag{1.7}$$

The blue curves indicate the case where the base station has directed the PA to reduce its output power. This results in a peak fundamental component that is almost proportional to the DC current, indicating poor efficiency. Clearly, there is a need for better design.

[8] We hope to filter out all the harmonics with our matching network / harmonic trap.

Table 1.2 PAR, Bandwidth, and Power Control Specification. Adapted from *"Power Amplifier Principles and Modern Design Techniques,"* by V. Prodanov & M. Banu, 2008, *Current PA Technology and Recent Developments*. Copyright 2008 by Taylor & Francis.

Wireless Standard	PAR (dB)	Signal Bandwidth (MHz)	Power Control (dB)
AMPS, GSM, GPRS, EDGE	Low (~0-3.2)	Small (≤0.2)	Moderate (≤30)
CDMA, CDMA2000, WCDMA	Moderate (3-5)	Large (1.23, 3.84)	Very large (70-80)
IEEE 802.11a, IEEE 802.11g	Large (>7)	Very large (~17)	N/A

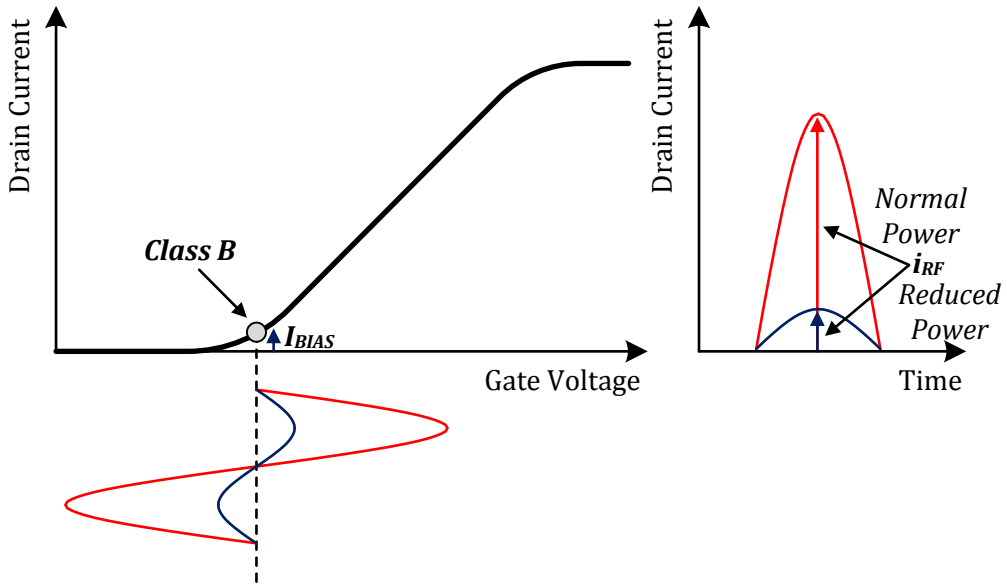

Figure 1.7 Implications of power control on RF PAs.

1.4.3 Prior Art

In order to address the inefficiency problem discussed in the previous section, it may be tempting to solve the issue by reducing the bias (approach class C operation) as shown in Figure 1.8. However, dynamic signals with large PARs will undergo uneven power gain. This reasoning comes about from the fact that the conduction angle under class C operation does not stay constant (see Figure 1.5). When the conduction angle varies for different RF drives, the shape of the drain current essentially changes (i.e. we have nonlinearity).

From the previous discussion, we conclude that in order to obtain a linear PA, we need to hold the conduction angle constant. Much of the prior art in adaptive biasing[9] solutions seems to neglect this important detail. The inventor of the patent in [8] seems to understand that linearity and constant conduction angle are related, but doesn't formally acknowledge this. Figure 1.9 shows a block diagram of the topology described by the patent. The RF signal feeds into a driver transistor[10] and a sampling transistor (sampling stage) converts the input drive into a current drive at its output. The averaging stage consists of a two-stage cascaded current mirror with an RC filter in each stage. This filtering serves to yield an average value of the current. The output of this stage feeds into a resistive divider that converts this current into a voltage, which is applied to the base of the class C PA. This circuit topology aims to reduce the DC bias as RF drive increases. Despite the claim by the inventor stating that the circuit should maintain the conduction angle, there is no clear evidence to the matter. The adaptive biasing strategies described in [9, 10, 11] follow a similar type of strategy. They seem to adjust "hidden" knobs in order to obtain best linearity and lowest third order intermodulation distortion (IMD_3).

[9] It is worth noting papers in this field of study often mention "envelope injection" when referring to adaptive biasing schemes. Since wireless modulation methods such as nQAM have amplitude modulation, the DC bias must follow the envelope of the RF signal for adaptive biasing to work.
[10] The author vaguely mentions that this can be biased in class B but offers no explanation.

The most significant issues with the prior art are the following:

- The implementations use an open-loop strategy for adaptively biasing. They don't sense the operating conditions (the state of the drain current) of the actual class C PA, which truly defines the conduction angle.

- In addition, some of the approaches pass the RF signal through a driver stage, which can prove troublesome if device mismatches occur over time; these conditions could adversely affect efficiency and linearity.

- There is really no clear-cut consensus on how to obtain class C linear operation; [8] seems to suggest, but not outright claim, that linearity and constant conduction angle are interwined.

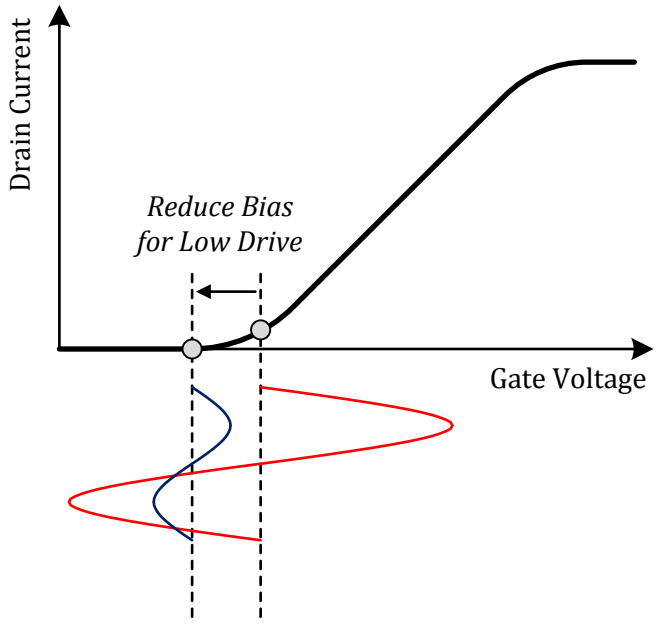

Figure 1.8 Reducing bias for low drives.

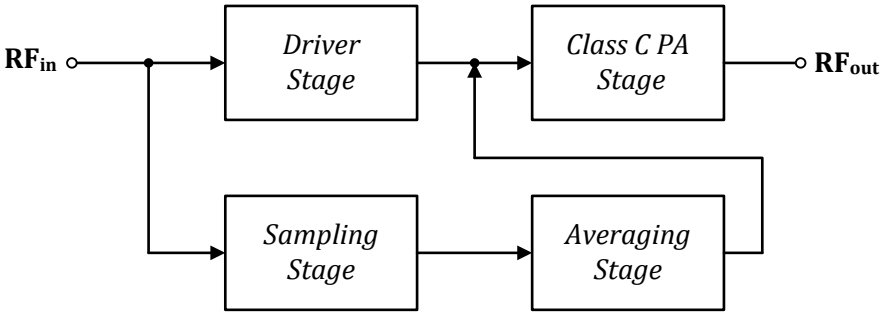

Figure 1.9 Approach to adaptive biasing used by **[8]**.

2

Constant Conduction Angle Biasing

2.1 Theory

As mentioned in the previous chapter, when we operate in class C, the conduction angle (conduction period) changes with drive. The conduction angle increases with an increase in RF drive and this indicates nonlinearity. Figure 2.1 illustrates this issue. To understand this analytically, we need to first look at the I-V characteristics of a transistor.

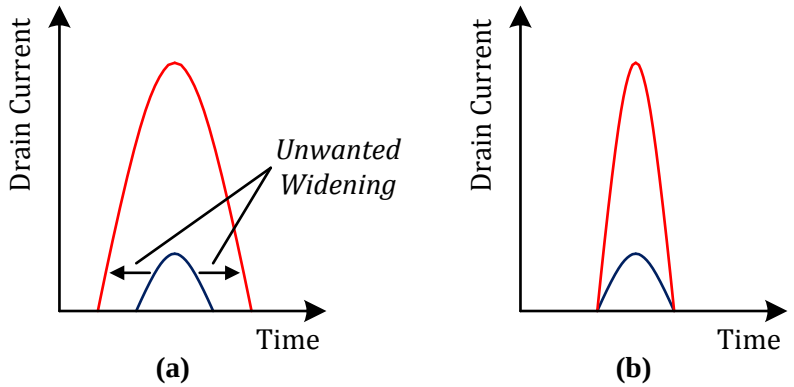

Figure 2.1 (a) Non-ideal widening of drain current with conventional class C biasing; (b) Desired class C operation.

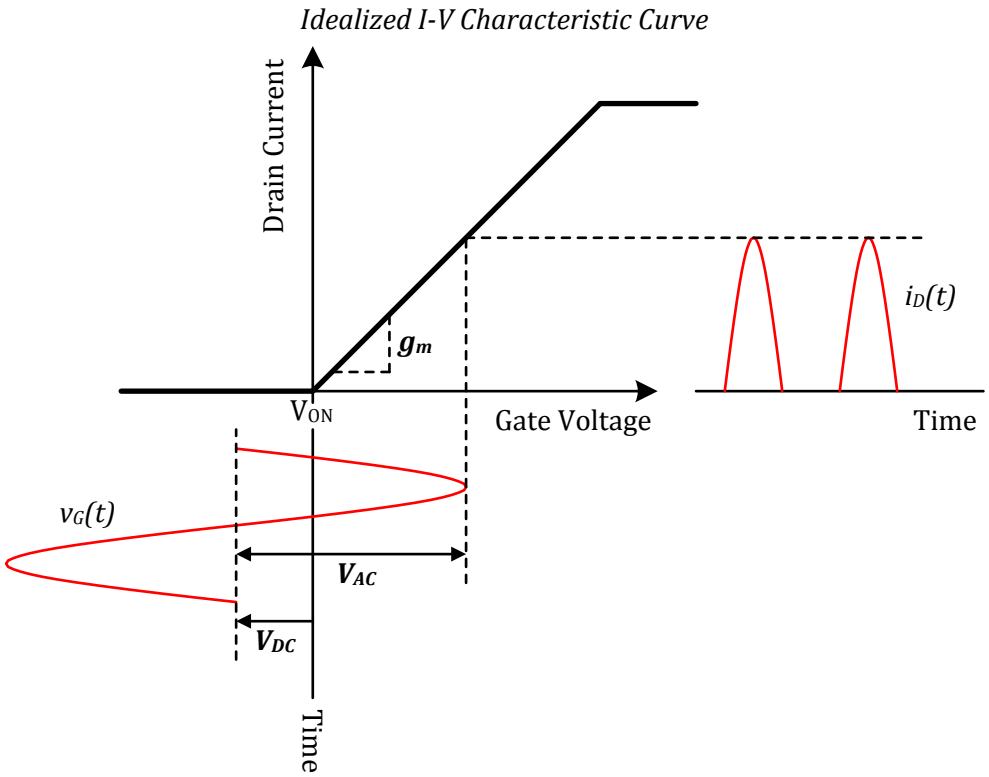

Figure 2.2 Voltage-to-current conversion of an ideal transistor with a "hockey-stick" I-V characteristic.

Figure 2.2 shows the I-V curve for an ideal transistor with a sharp turn-on. After some detailed analysis, to which we direct the reader to Appendix A, we obtain several important equations. Equation (2.1) relates the DC to AC[11] ratio to the conduction angle[12]. Equations (2.2) and (2.3) relate the DC and fundamental current, respectively, to RF drive and conduction angle.

$$\frac{V_{DC}}{V_{AC}} = -\cos\left(\frac{\theta}{2}\right) \tag{2.1}$$

$$I_{DC} = \frac{g_m V_{AC}}{\pi}\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right] \tag{2.2}$$

$$I_{\omega_0} = \frac{g_m V_{AC}}{2\pi}[\theta - \sin(\theta)] \tag{2.3}$$

[11] This refers to the peak value of the RF voltage swing, and what we hitherto called RF drive.
[12] The conduction angle is in units of radians.

The aforementioned DC and fundamental drain current expressions show that as long as the conduction angle holds constant, linearity is ensured. The next few sections will explore methods on how to implement this. For brevity, we will use the abbreviation, CCA, to refer to constant conduction angle throughout the rest of this paper.

2.2 A Poor-Man's CCA Biased Class C PA

It is important to give credit where it's due. This section summarizes the approach, issues, and conclusions from the work performed by Greg LaCaille, in conjunction with Professor Prodanov, when the CCA idea was in its infancy.

2.2.1 Ideal Class B Operation

We beging by noting that a conduction angle of 180° corresponds with an ideal class B operation. Substituting this conduction angle into (2.2) and (2.3) leads to the following results:

$$I_{DC} = \frac{g_m}{\pi} \cdot V_{AC} \tag{2.4}$$

$$I_{\omega_0} = \frac{g_m}{2} \cdot V_{AC} \tag{2.5}$$

Thus an ideal class B PA is linear irrespective of RF drive.

2.2.2 CCA Biasing using a Pair of Scaled Replica Transistors: Equal RF Drive, Unequal DC Ratio Method

Consider that we have two identical (the same transconductance or g_m) and matched devices that are driven by the same RF drive. They differ only by how they are biased – one is biased in class C and the other is biased in class B.

We write the expression for the DC current of the class C:

$$I_{DC,C} = \frac{g_m V_{AC}}{\pi}\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right] \tag{2.6}$$

The DC current of the class B follows:

$$I_{DC,B} = \frac{g_m}{\pi} \cdot V_{AC} \tag{2.7}$$

Notice that the ratio of the DC currents yields:

$$\frac{I_{DC,C}}{I_{DC,B}} = \sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right) \tag{2.8}$$

Thus, if we can keep the DC currents of the class B and C devices in constant proportion the conduction angle stays significantly[13] constant. A strategy to accomplish this is by implementing a fixed-biased[14] class B device which produces a "reference" low-frequency current, $I_{DC.B}$, based upon the RF drive. A servo loop than provides the gate bias of the class C device in a manner such that the ratio of the DC currents of the class B and C devices remain in constant proportion regardless of RF drive. Setting the ratio of the DC currents determines the conduction angle of the class C device.

Designed properly, with a servo loop that has enough bandwidth to accommodate the bandwidth of the modulated RF signal, the class C device should have low IMD_3 in the face of complex modulation schemes used in wireless communication systems.

Figure 2.3 shows the block diagram of the approach investigated by LaCaille. A fixed DC source biases the class B transistor, while the feedback loop provides the bias for the class C transistor and the 100x scaled replica class C power transistor. The RF capacitively couples to all three devices. This approach assumes respectable matching of the like components and good thermal matching.

[13] We say "significantly" here because our analysis is based on an ideally sharp knee when in reality the knee is soft for a practical solid state transistor.
[14] Biased at the gate for a FET, or base for a BJT.

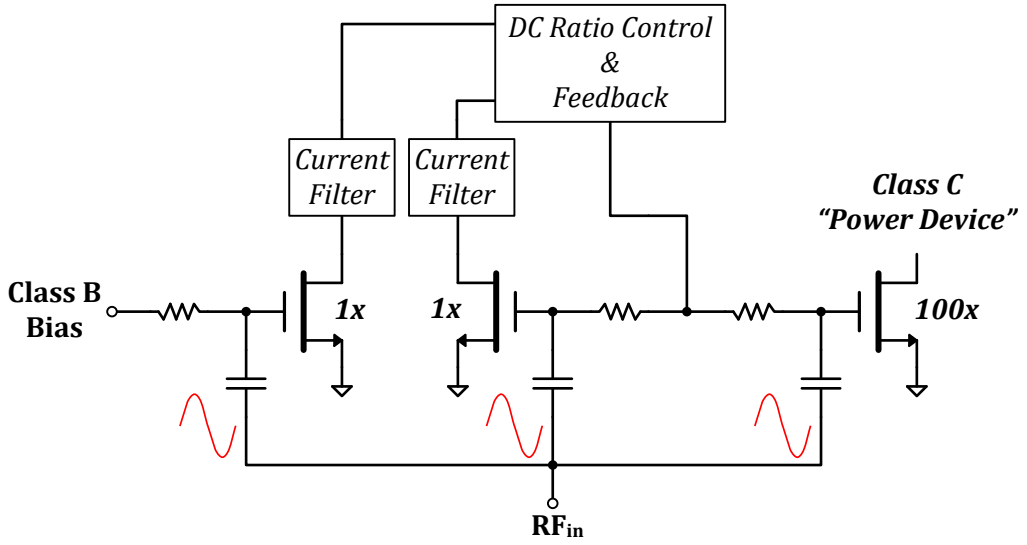

Figure 2.3 Simplified block diagram of LaCaille's CCA biasing approach.

2.2.3 The Major Drawback with the Approach

By virtue of the design discussed in the previous section, the RF drives to the class B and C devices must be the same. This requirement proves a significant problem for the class C PA. Referring to Figure 2.4, we see that the class B transistor reaches its maximum output current first. Note that beyond this point, the class B transistor will saturate and no longer provide a valid DC current reference for the class C PA. Thus, this point sets the maximum allowable input RF drive to the PA. Since the class C PA cannot use the full extent of the practical I-V curve, this invalidates the proposed design.

Perhaps, a less serious issue with the design is the use of capacitive coupling to three different points in the circuit from one source. Not only is it impractical to couple into three points, but the capacitors introduce more poles into the system.

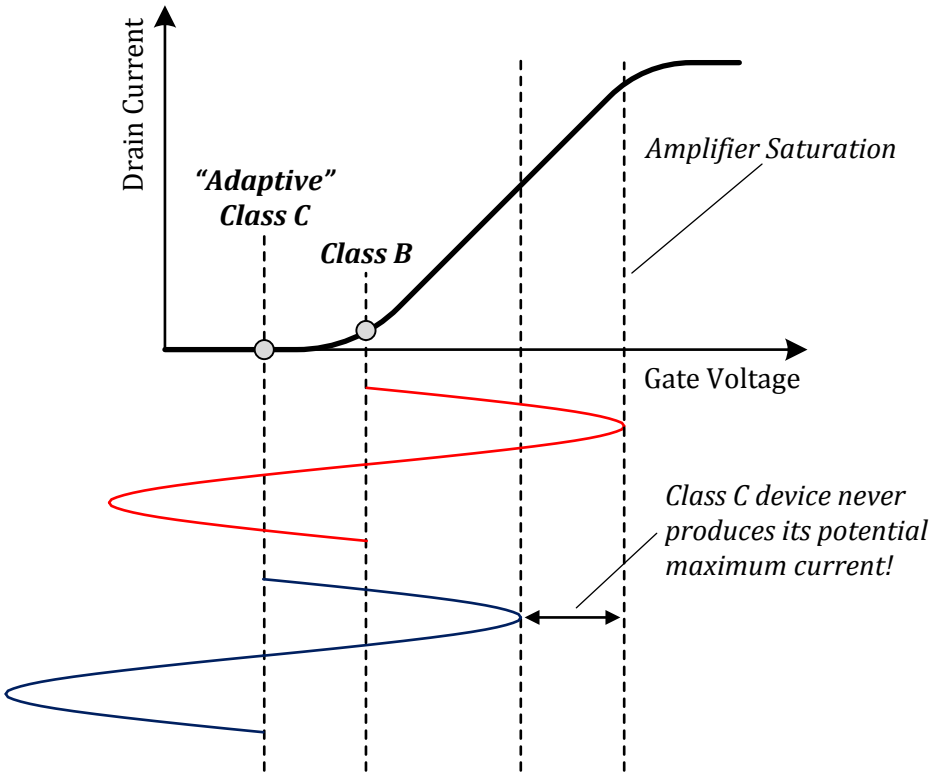

Figure 2.4 Underutilization of Class C PA with equal RF drive and unequal DC current ratios method.

2.3 An Improved CCA Biased Class C PA

The following strategy was explored and simulated by Stephen Garber and implemented by Michael Spahn.

2.3.1 CCA Biasing using a Pair of Scaled Replica Transistors: Unequal RF Drive, Equal DC Ratio Method

Assuming identical devices as before, consider now the RF drives are different. We have the following expressions for the DC currents:

$$I_{DC,C} = \frac{g_m V_{AC,C}}{\pi}\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right] \tag{2.9}$$

$$I_{DC,B} = \frac{g_m}{\pi} \cdot V_{AC,B} \tag{2.10}$$

Forcing the DC currents equal, we obtain the following relation for the ratio of the RF drives:

$$\frac{V_{AC,B}}{V_{AC,C}} = \sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right) \tag{2.11}$$

This proves better than the previous strategy of "equal RF drive, unequal DC current ratio", since the class C has a larger drive than the class B device allowing it to have a higher maximum current. However, apparent from Garber's work[15], it still can't deliver the maximum possible current. The block diagram for this concept is shown in Figure 2.5. The associated detailed schematic of the circuit[16], which was built by Spahn, is shown in Figure 2.6. The RF coupling and drive scaling are impractical, the current-setting resistors are too small, and there are issues with loop stability (observed by Spahn in the lab). We address the specifics of the loop stability in Chapter 3.

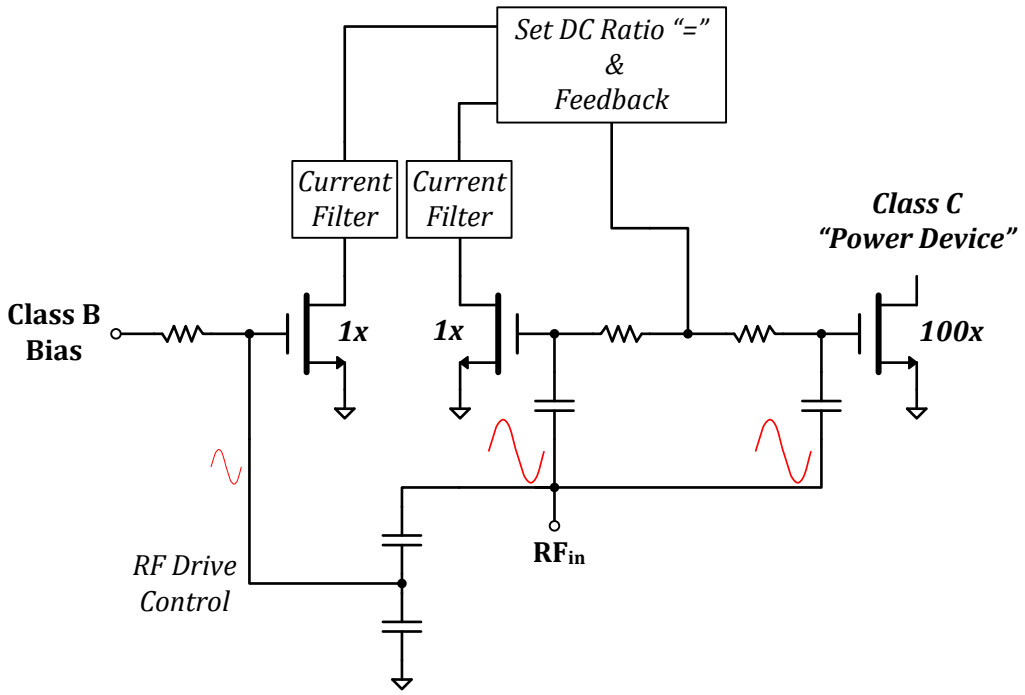

Figure 2.5 Simplified block diagram of Garber's CCA biasing approach.

[15] The peak swing of the class B devices is always greater than the class C device at any time.
[16] This implementation uses BJTs but this is valid because the I-V characteristics are very similar to a FET device. The difference lies in the fact that BJTs are current-controlled devices and require a small amount of base current to operate.

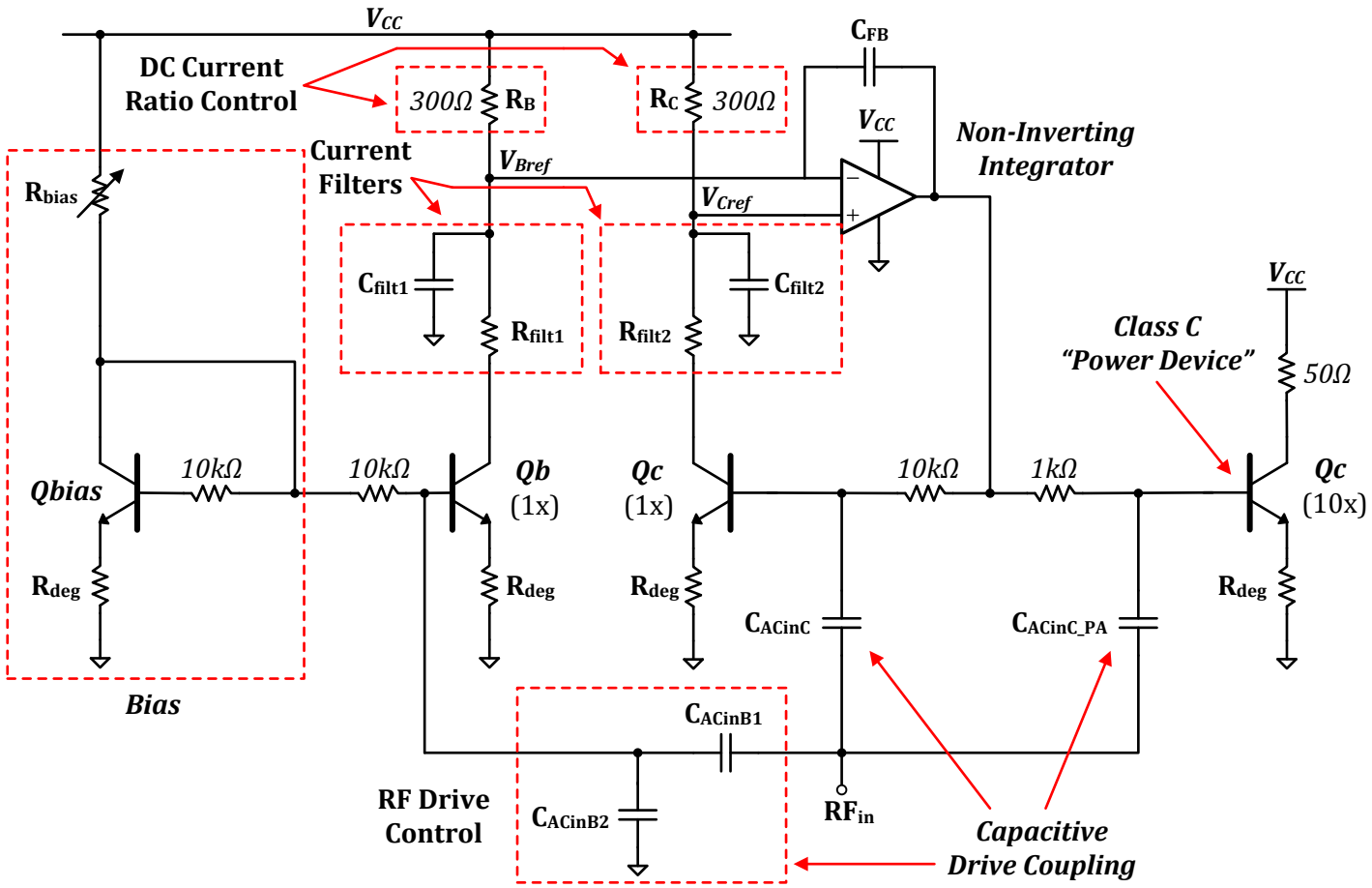

Figure 2.6 Detailed schematic of the CCA biasing circuit built by Spahn.

2.3.2 *CCA Biasing using a Pair of Scaled Replica Transistors: Hybrid Control*

In addition to showing that a CCA can be achieved using different RF drives, Garber also noticed a mixed possibility. Notice that the previous schemes are the extreme cases of the more general scheme:

$$\frac{I_{DC,C}}{I_{DC,B}} \cdot \frac{V_{AC,B}}{V_{AC,C}} = \sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right) \tag{2.12}$$

The first case assumes that the second quantity has a ratio of 1 and the second case assumes the first quantity has a ratio of 1. Thus for the same conduction angle there are an infinite amount of possible solutions and in the ideal case they are all equivalent. However, in the case of a practical transistor with a soft knee, there should be an optimum solution. This solution should yield the most linear fundamental response and the lowest IMD_3.

2.4 An Optimum Hybrid Approach

Previously we mentioned the issue of Class C device never achieving the maximum possible drain current. How do we do this? We need to ensure equal peak excursions of the class B and C devices. To begin the peak excursions of the two devices follow:

$$V_{pk,B} = V_{AC,B} \tag{2.13}$$

$$V_{pk,C} = V_{AC,C} + V_{DC,C} \tag{2.14}$$

Using (2.1), we rewrite (2.14) to the following form:

$$V_{pk,C} = V_{AC,C}\left[1 - \cos\left(\frac{\theta}{2}\right)\right] \tag{2.15}$$

In order to determine the optimum RF drive ratio, we equate (2.13) and (2.15):

$$\left(\frac{V_{AC,B}}{V_{AC,C}}\right)_{opt} = 1 - \cos\left(\frac{\theta}{2}\right) \tag{2.16}$$

To determine the optimum DC current ratio, we substitute (2.16) into (2.12):

$$\left(\frac{I_{DC,C}}{I_{DC,B}}\right)_{opt} = \frac{\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)}{1 - \cos\left(\frac{\theta}{2}\right)} \tag{2.17}$$

The optimum RF drive and DC current ratios constrain us to one set of requirement per conduction angle. The requirements for a range of class C conduction angles are shown in Figure 2.7. Figure 2.8 shows a pictorial representation of the idea of equal peak excursion. Notice that we can now drive the class C PA to its maximum output current.

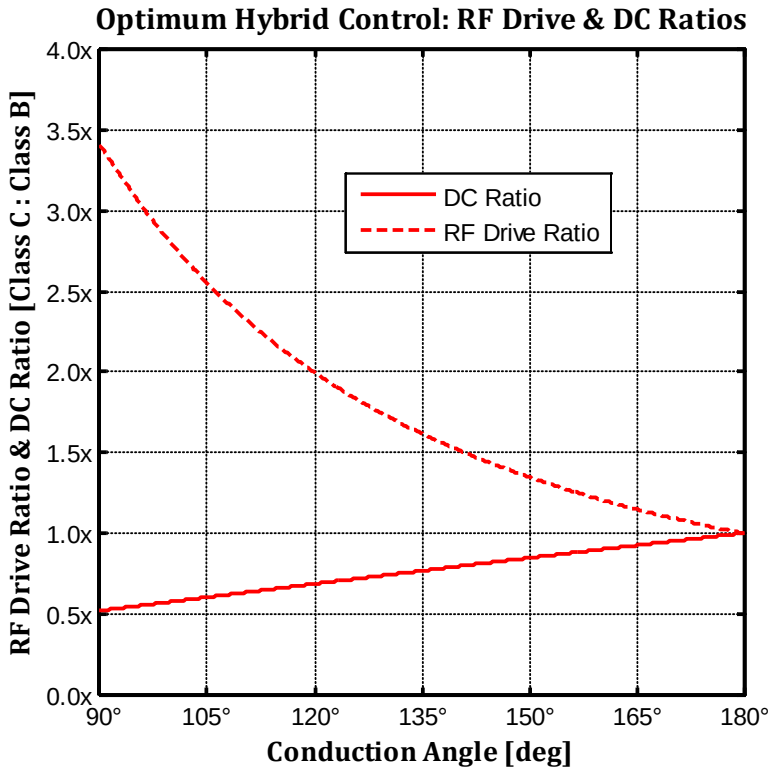

Figure 2.7 Optimum hybrid control ratio requirements for various conduction angles. Plot generated in MATLAB.

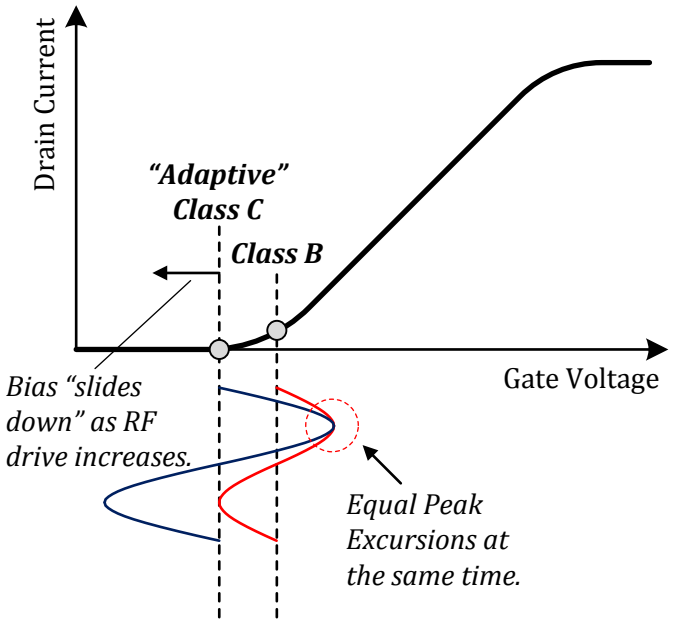

Figure 2.8 Pictorial depiction of optimum hybrid control.

2.5 Fundamental Throughput and Efficiency Tradeoff

Before concluding this chapter, the implications of different conduction angles, in terms of how much fundamental current is produced and the associated efficiency, require some discussion.

For this discussion, we observe Figure 2.9. This plot shows the harmonic content of the drain current for each conduction angle. It also plots the maximum possible efficiency[17] for the conduction angles. The reader may refer to Appendix A to find the drain current expressions used to plot the harmonics. For the efficiency[18] expression we have the following:

$$\eta = \frac{P_{RFout}}{P_{DC}} = \frac{\frac{1}{2}V_{out}I_{out}}{V_{DC}I_{DC}}$$

For maximum swing on the output, $V_{out} = V_{DC}$. Thus we have on the following page:

[17] The case when the output impedance is set for maximum swing.
[18] When calculating efficiency we are concerned with the fundamental components. The expression used here is also found in Appendix A.

$$\eta = \frac{\frac{1}{2}V_{DC}I_{out}}{V_{DC}I_{DC}} = \frac{\frac{1}{2}\frac{g_m V_{AC}}{2\pi}[\theta - \sin(\theta)]}{\frac{g_m V_{AC}}{\pi}\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right]} = \frac{\theta - \sin(\theta)}{4\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right]} \tag{2.18}$$

From the figure, we notice a few things. First, the second harmonic is particularly strong for class C operation – strongest at a conduction angle of 120°. This conduction angle corresponds to an efficiency of about 90%! Another important characteristic to notice is that the fundamental component starts dropping off steeply as the conduction angle becomes smaller. The conduction angle of 120° seems to be a reasonable practical point of tradeoff between fundamental throughput and efficiency. After this point, the fundamental starts dropping off too steeply. Depending on what type of tradeoff the specific application requires, the designer may choose the appropriate conduction angle in the range highlighted in the figure.

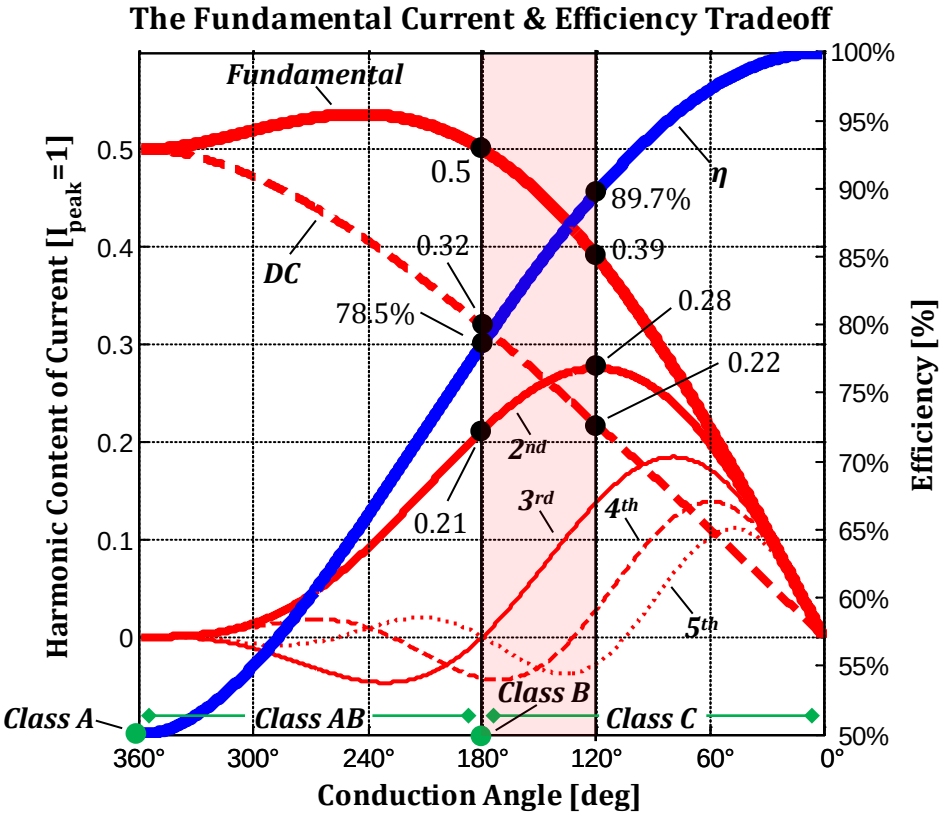

Figure 2.9 Harmonic drain current and efficiency vs. conduction angle. Plot generated in MATLAB.

3

CCA Biasing Design & Simulation

3.1 Approach

The use of matching networks and tuning sometimes puzzles analog electronic design engineers. Similarly, microwave engineers sometimes get into trouble with stability when designing DC bias networks for amplifiers. So, for a design concept such as the one[19] presented, we want to approach the problem in a modular approach – first working out the basic "analog issues" and then scaling the concept to the application frequency. Instead of trying to design the circuitry at the cellular band frequency, we instead scale down the frequency to avoid dealing with transmission line effects. This chapter deals with the development and design of the practical CCA biasing topology, analysis of its control loop, and its performance in terms of linearity and IMD_3.

[19] This is especially important because we have a control loop in the system and if designed improperly we quickly run into stability issues.

3.2 Proposed Design Topology

Figure 1.2 shows the conceptual schematic of the CCA. We begin by describing the different sections of the proposed design. First, notice that we have solved the issue of multiple capacitive coupling by only capacitively coupling into one point. The class B transistor sensor obtains its RF drive by virtue of the transformer/narrowband choke. The class C transistor sensor in this design is a part of the power device – it is one finger of the whole[20]. Each of these fingers is a "small" transistor (the same size as the class B sensor) that carries the same current as the others. So, we just need to sample one of these fingers in order to sample the operating condition of the class C PA. In an integrated circuit (IC) implementation, we would place the class C sensor in the middle of the cascade so that it would best compensate for real-time transistor thermal conditions.

The current filters remove the fundamental and harmonic components of the drain current to yield the DC levels of the currents. The non-inverting integrator[21] senses the DC levels of the class B and C sensors by the voltage drops that occur across resistors R_B and R_C, respectively. The integrator then forces the "error" to zero; i.e. it will adjust the gate voltage of the class C to cause the voltages V_{Bref} and V_{Cref} to be equal. Thus, the ratio of the "current-sense" resistors determines the DC current ratio. The drive ratio is simply controlled by the secondary windings of the transformer[22].

The output network consists of an impedance matching section. The impedance required for maximum swing will typically differ from the terminating load impedance. Thus we scale the impedance with a matching network. Also, note, we can design a matching network to incorporate filtering of the harmonics produced by the class C PA. We discuss this issue in more detail in Chapter 4.

[20] This is known as a multi-fingered transistor and is essentially a composite transistor consisting of many "small" cascaded transistors in order to create a power transistor in an IC.
[21] We are ensured negative feedback by the transistor which inverts the signal by 180°.
[22] The class B transistor will always be driven less than the class C as shown in Figure 2.7.

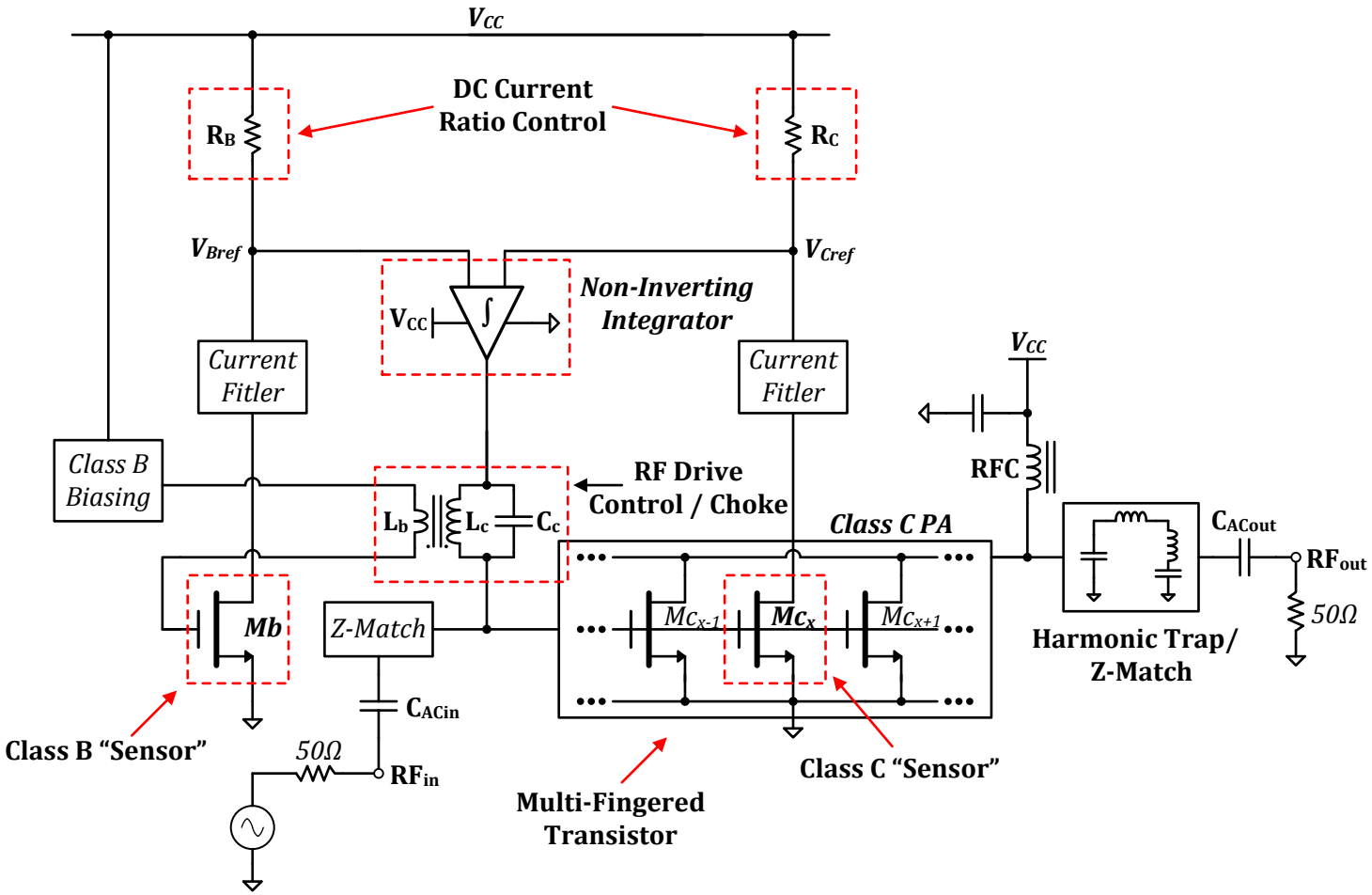

Figure 3.1 A conceptual schematic of the optimized CCA biasing topology.

3.3 Implemented Design Details

Ideally we want to fabricate the circuit in an IC with matched devices in order to test the full extent of the design. Such an endeavor is bold and requires a significant amount of additional research and coordination. However the priority, initially, is to develop a "quick and dirty" proof-of-concept. This is the motivation of the present work.

In order to demonstrate a multi-fingered PA, we used the CA3086 IC, which consists of 5 NPN BJTs each. We discuss the details of the actual prototype implementation in the next chapter. Notice, that although we performed our CCA analyses based upon FETs, the I-V characteristics of FETs and BJTs are similar. Thus, the proposed topology should hold the conduction angle of a BJT constant as well.

For the feedback, we use an LM6134 rail-to-rail operational amplifier (op-amp). A rail-to-rail capability allows for the ability to bias the class C low enough. Additionally, the op-amp has a gain-bandwidth product (GBW) about 10 times the design frequency of 1MHz. This allows for a more "ideal" integrator at the design frequency and we need not worry about the op-amp dynamics effecting CCA biasing operation.

Originally, simulations were performed in LTspice. However, LTspice performs poorly in the frequency-domain, when analyzing the non-linear behavior of reduced-conduction angle mode devices. This prompted the change to move to Agilent ADS to perform the simulations. The harmonic balance method[23] used in ADS allows for effective frequency-domain simulations especially in determining intermodulation distortion in circuits.

Figure 3.2 shows the detailed schematic of the design explored in this paper. The next few sub-sections contain discussions on the details of the circuit.

[23] Much regard goes to Matthew King for his assistance in learning this simulator in ADS.

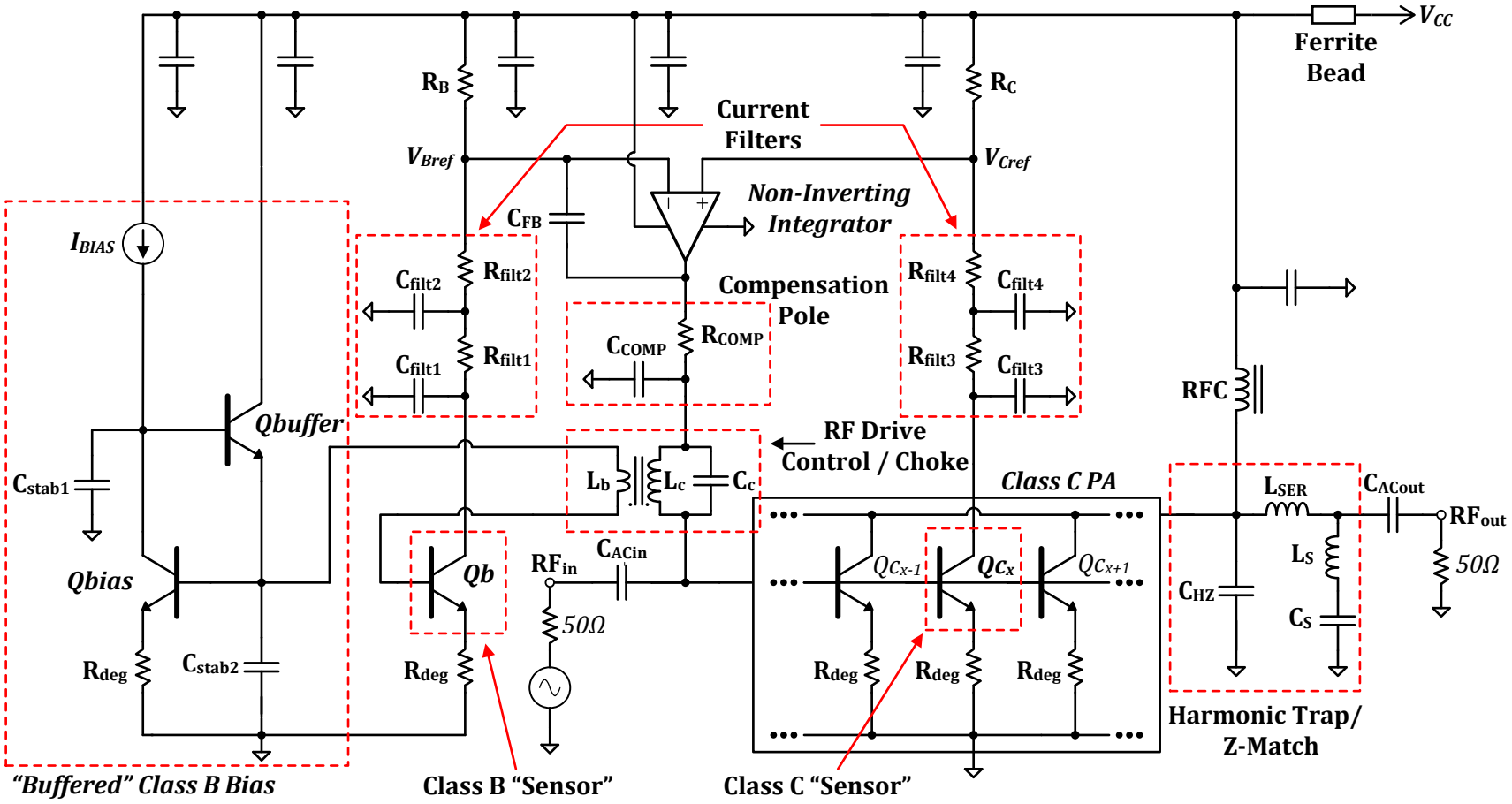

Figure 3.2 The detailed schematic of the designed and simulated CCA biasing topology.

3.3.1 The Emitter Degeneration

In the design presented, notice that the transistors are emitter degenerated. Emitter degeneration[24] simplifies the design of a common emitter (CE) amplifier by making the DC bias and AC gain more reliable as described in [12]. Additionally, RF power devices typically a parasitic emitter resistance that "degenerates" the response, making the I-V characteristic more linear.

Figure 3.3 shows a plot of the I-V characteristic of a single transistor of the CA3086 IC, for the cases of degeneration versus no degeneration. In the case of no degeneration, the curve is very steep. This implies that any slight variations in the I-V characteristics of the transistors in the IC may lead to widely varying collector currents. In addition, we want the class B and C sensors to dissipate negligible power in comparison to the class C PA. Thus, as seen in the figure, a degeneration resistance of 22Ω provides a much more appealing I-V curve for the CCA biasing design.

Finally, we give a brief statement on the I-V curve of an emitter degenerated CE amplifier. The degeneration essentially changes the transconductance, or g_m, and gives rise to an effective transconductance, as described in [13]. We can write the effective transconductance as:

$$g_{m(eff)} = \frac{g_m}{1 + g_m R_{deg}} \tag{3.1}$$

For a large transconductance, the effective transconductance approaches $1/R_{deg}$.

[24] Emitter degeneration is a type of "negative feedback"

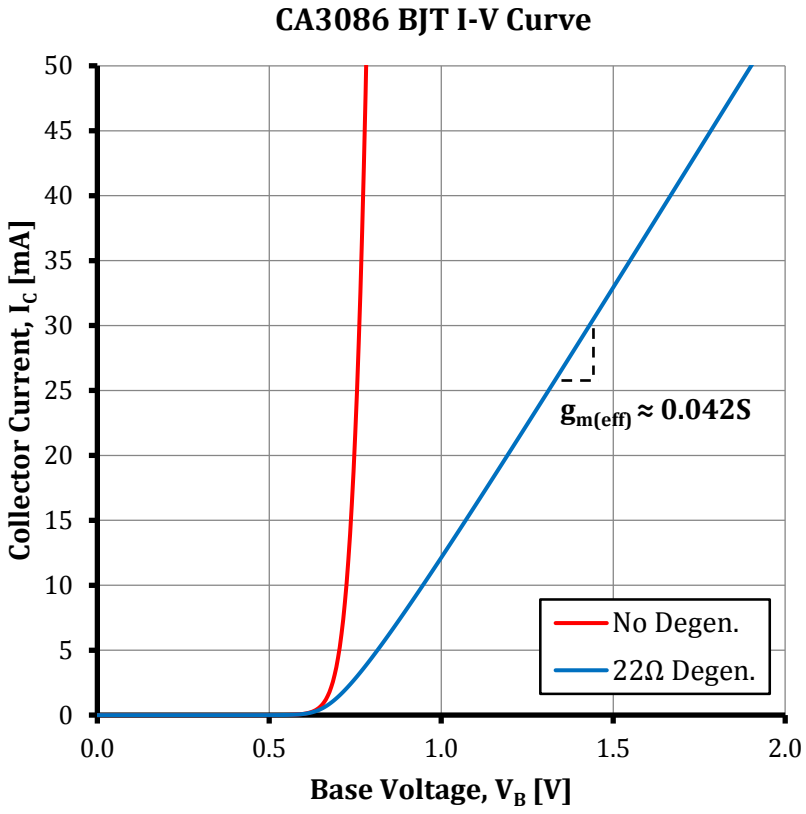

Figure 3.3 Effect of degeneration on the I-V characteristics of an NPN CA3086 BJT. Simulated in ADS.

3.3.2 The "Buffered" Class B Bias & Benefit of Inductive Coupling

For this discussion, we refer the reader to Figure 3.4.The class B sensor obtains its bias via current mirror action. This current mirror topology is slightly different from the classical topology. In place of the collector-base diode-connection of the bias transistor, we place a transistor in the path as shown. The reasoning for this design comes from the fact that a BJT is in essence a current controlled current device. It requires some amount of base current to produce the desired collector current. This implies that as the input drive to CE amplifier increases, more and more base current is requested by the base.

Thus in the configuration presented, the transistor placed between the collector and base of the biasing transistor provides the current requested by the class B sensor. It essentially acts as a buffer. Recall, that the current requested by the base of a CE BJT is β (CE current gain) times smaller. Thus, the buffer needs only to provide this small amount of current[25] for the class B device; the base current drawn by the buffer will be another β times smaller (i.e. very negligible). This approach prevents "current starving" the bias transistor when driving the class B sensor with large RF drives.

The approach to inductively couple the RF signal to the class B device is very appealing since it does so without disturbing the bias branch. Additionally, since an inductor presents itself as a short to DC, the bias and class B transistors share the same base bias voltage regardless of RF drive. We obtain a fixed bias for the class B sensor as required by the CCA biasing topology.

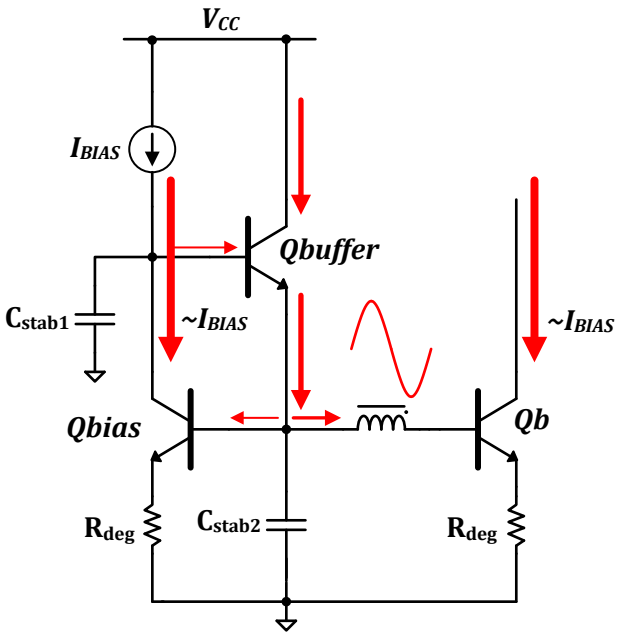

Figure 3.4 The "buffered" biasing of the class B sensor.

[25] Depending upon the RF drive presented to the class B sensor.

3.3.3 *Sections of the Control Loop & the Rest of the Circuit*

As RF drive is applied to the circuit, the class B sensor starts producing current with a conduction angle of about 180°. This current flows through a two-stage CR filter to remove the fundamental and harmonic content, yielding the average or DC current on the other side. The class C sensor performs in the same manner. The op-amp integrator then acts to bring the steady state error to zero by biasing the class C sensor to force V_{Bref} to equal V_{Cref}. The ratio of the DC currents is therefore set by the ratio of the resistors R_B and R_C. These resistors should be large enough in value to produce a suitable voltage drop for small RF drives in order to be sensed by the op-amp as a difference. We defer the analysis of the integrator, compensation pole, and loop to the next section.

In regards to the transformer/narrowband choke, we resonate using an LC in order to produce high impedance to RF without the use of very large valued inductors – especially at 1MHz!

Finally, in terms of the class C PA, it is implemented as a cascade of 12 CA3086 BJTs[26] with their bases and collectors tied together. The class C sensor is placed in the "middle" of this cascade[27] with only its base tied to the rest of the transistors. The composite collector of theses transistors is connected to the DC power supply through an RF choke. In order to filter the harmonics generated by class C operation, we utilize the filtering properties of the matching network (required to scale the impedance for maximum collector voltage swing). A more detailed discussion on the design of the matching network is found in Chapter 4.

[26] These were spread amount 3 ICs since each CA3086 contains 5 BJTs.
[27] This is done to attempt to compensate for temperature differences between at least 2 of the ICs.

3.4 Loop Analysis

Perhaps the most important issue to discuss is the control loop. The design of loop proves critical in obtaining stability and optimum loop bandwidth. In the CCA biasing topology, we need enough loop bandwidth to accommodate the changing envelope of the incoming modulated RF signal. If the bandwidth of the signal exceeds the bandwidth of the loop, the signal will typically start to encounter phase problems; the IMD_3 of the PA will as a consequence increase tremendously. For a typical integrator, the loop bandwidth is the width of the region with loop gain above[28] 0dB. Figure 3.5 shows a pictorial of this for an inverting integrator.

In the next section, we provide a model of the control loop in the CCA biasing circuit. We then present simulations in regards to the open-loop response.

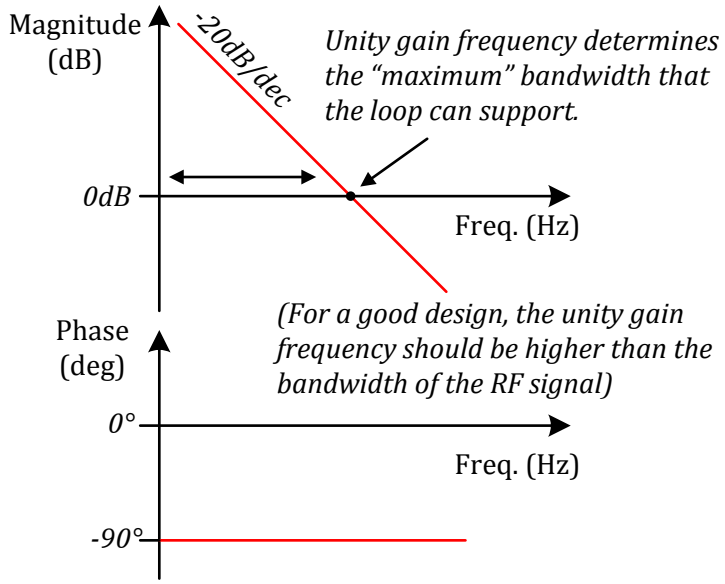

Figure 3.5 The magnitude and phase response of an inverting integrator.

[28] The feedback will start to become ineffective for signal components close to 0dB gain. Thus, when designing the system, we would like our 0dB frequency to be a good degree higher than the maximum bandwidth of RF signal to be injected in the system.

3.4.1 The Loop Model

Figure 3.6 shows an open-loop model for the CCA biasing circuit. We begin our discusion at the inputs of the operational amplifier. The class B filter presents only the "DC[29]" reference to the integrator.The filter on the class B side does not have a significant affect on the open-loop response. The non-inverting[30] integrator consists of the class B current-setting resistor and the feed back capacitor. To understand the reasoning for the compensation pole following the integrator, we first write the integrator's transfer function:

$$H = \frac{1 + sR_BC_{FB}}{sR_BC_{FB}} = \frac{1 + \frac{s}{\omega_Z}}{\frac{s}{\omega_0}} \tag{3.2}$$

From the transfer function, we realize that it has a left-hand plane zero, which is quite problematic since this the zero prevents the gain response from continuing to drop off after reaching 0dB. Although we achieve improved phase margin, we lose gain margin. This should not be understated since the class C sensor provides a significant amount of gain (proportional to g_m). In order to alleviate the problem, we add a compensation pole since

$$H \cdot \frac{1}{1 + \frac{s}{\omega_Z}} = \frac{1}{\frac{s}{\omega_0}} \quad .$$

The values of compensation components have to equal the values of the components that form the zero. Thus, $R_{COMP} = R_B$ and $C_{COMP} = C_{FB}$

In terms of the other components we have the transformer/choke, which due to its resonance produces a significant phase swing at the RF carrier frequency. This however, does not pose a problem since the open-loop gain, at this point, is below 0dB. The input

[29] The low-frequency, baseband, content for a dynamic signal.
[30] Note, we use a non-inverting integrator because the class C amplifier inverts the signal such that there is negative feedback. Clearly, if we used an inverting integrator, we have an unstable system.

AC capacitance also introduces slight effects on the loop behavior. The transconductance stage (i.e. the class C sensor) that follows ads a significant gain to the response. This gain, what we call G_{Meff}, is related to the transconductance and the conduction angle by the following equation:

$$G_{Meff} \approx \frac{g_m}{2\pi} \cdot \theta \; [rad] \tag{3.3}$$

The derivation of this equation can be found in Appendix B. Note that for an emitter degenerated case, simply replace g_m in the above equation with $g_{m(eff)}$.

Finally, the last stage of the loop is the output of the class C sensor's collector which feeds into a two-pole filter. This presents a significant effect on the response. Particularly, a tradeoff exists between how well the signal is filtered and the loop bandwidth. The following section presents some simulations that show how the different sections of the loop affect the response.

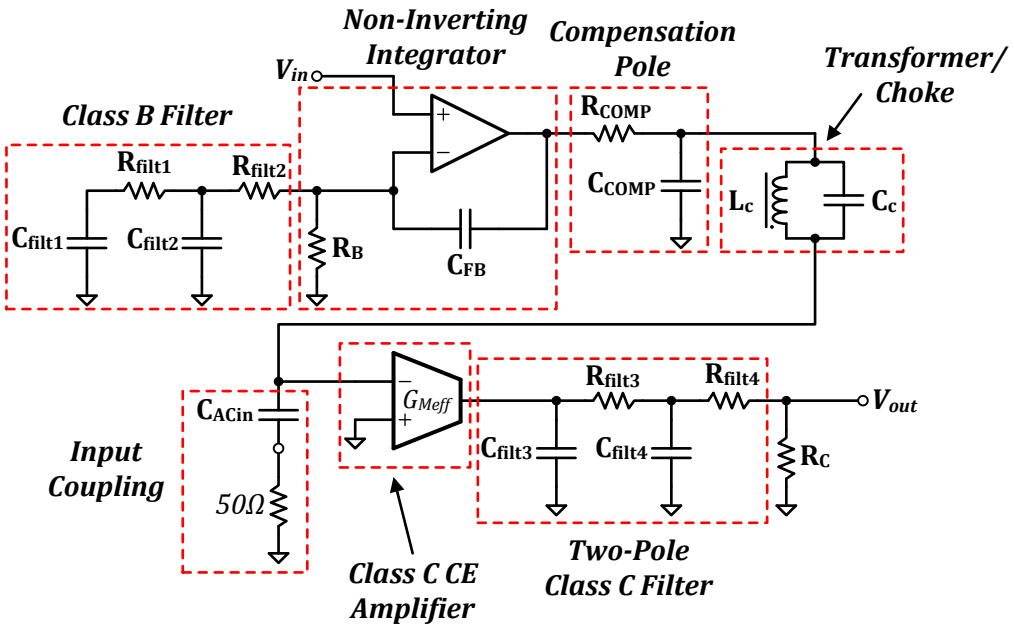

Figure 3.6 Open-loop model of the CCA biasing circuit.

3.4.2 Simulations of the Open-Loop Response

In the work presented, we focus on one conduction angle (θ=120°) to really understand how the system performs. The idea behind the work is to present a strategy to best design the CCA biasing circuit for a given conduction angle. In any case, we present some simulations of the open-loop response. The values used in the simulation reflect the final design values and are tabulated in Table 1.1 below.

In addition to values shown, the effective transconductance due to the emitter degeneration is 0.042*S* (see Figure 3.3). For a conduction angle of 120°, the G_{Meff} calculates to 1/3 of this value, or 0.014*S*. We use this value in simulating the open-loop response in ADS.

It is important to state that stability is ensured if the phase is greater than 180° for magnitudes of 0dB or greater. So, we begin by showing the impact of the two pole filter in the collector of the class C sensor in Figure 3.7. We see that although the the filter reduces the loop bandwidth by a certain degree (~10kHz), it impact the phase considerably. The phase starts "rotating" much earlier. This problem may be alleaviated if we increase the cutoff frequency of the current filter. However this comes at the expense of filtering out the fundamental and harmonics[31].

Table 3.1 Values used in simulating CCA biasing circuit for θ=120°.

$\boldsymbol{R_{filtx}}$	1kΩ	$\boldsymbol{C_{filtx}}$	2.7nF
$\boldsymbol{R_B = R_{COMP}}$	1kΩ	$\boldsymbol{R_C}$	1.46kΩ
$\boldsymbol{L_C}$	76.8μH	$\boldsymbol{C_C}$	330pF
$\boldsymbol{C_{ACin}}$	10nF	$\boldsymbol{C_{FB} = C_{COMP}}$	100nF

Figure 3.8 shows the effect of compensation on the overall open-loop response. As mentioned before, we achieve phase margin (PM), but lose gain margin (GM)[32].

[31] This is undesirable because we want only the DC component.
[32] $PM=\angle H(s)_{|H(s)|=0dB}+180°$, $GM=0dB-20\log_{10}|H(s)|_{\angle H(s)=-180°}$; These values should be positive.

The trouble area is around 200kHz, where we still have gain in the system and the phase starts to swing sharply. This phase swing is undesirable and can lead to instability.

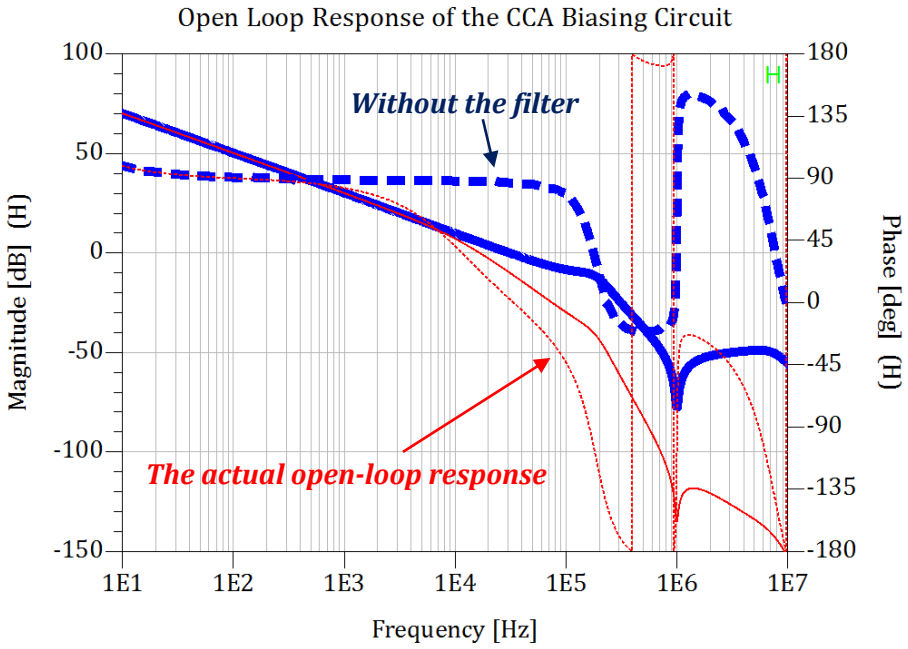

Figure 3.7 Effect of the current filter of the class C sensor on the open-loop response. Dotted Lines – *Phase*, Solid Lines – *Magnitude*.

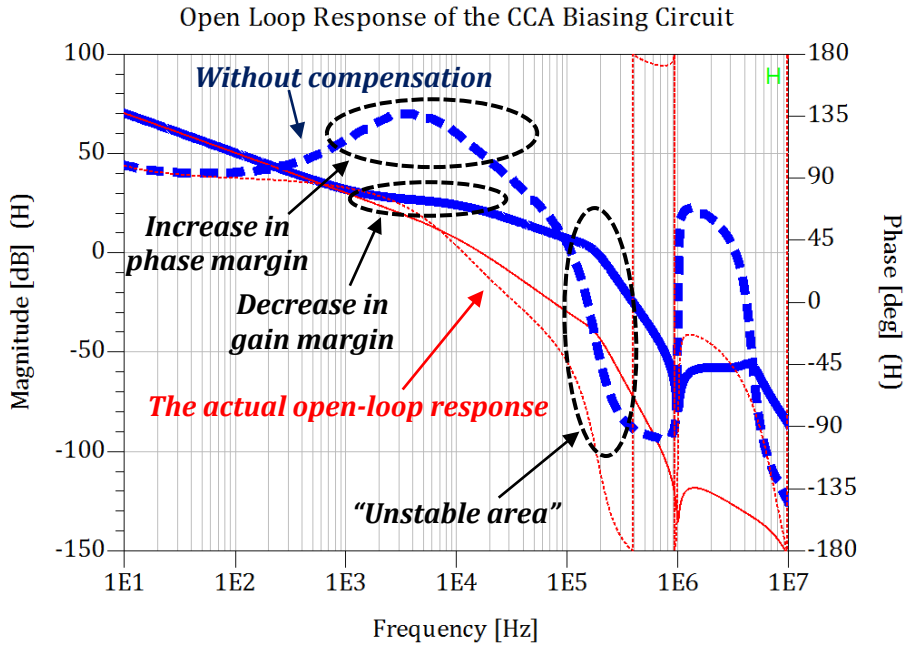

Figure 3.8 Effect of the compensation on the open-loop response. Dotted Lines – *Phase*, Solid Lines – *Magnitude*.

When we take a second look at the open-loop model it becomes clear why we have the two phase swings. One of the phase swings is associated with the parallel resonance of the LC while the other is due to the inductor series resonating with the AC coupling capacitor. What implications does this series resonance have? In the case of no compensation, we have gain in the system at this resonance; thus, any noise in the system can accumulate energy at this frequency and cause the system to oscillate. We will take a look at the transient response with no compensation versus compensation in the "system performance" section.

Figure 3.9 shows the effect on varying the AC coupling capacitor on the open-loop response. We see increasing its value causes the phase to start rotating earlier, decreasing the bandwidth slightly. So even though we want a large coupling capacitor, to act as a "short" to the input RF signal, we sacrifice phase margin and bandwidth.

Finally, Figure 3.10 shows the effect of changing the feedback capacitance[33]. With smaller values for the feedback capacitor, the response has significantly more gain with a phase that continues to drop throughout the range of the spectrum. Remember, for an ideal integrator response – one that gives zero steady state error - we want a magnitude response with a constant 20dB/dec drop and a flat phase response of 90° (for a non-inverting integrator).

[33] And the compensation capacitance.

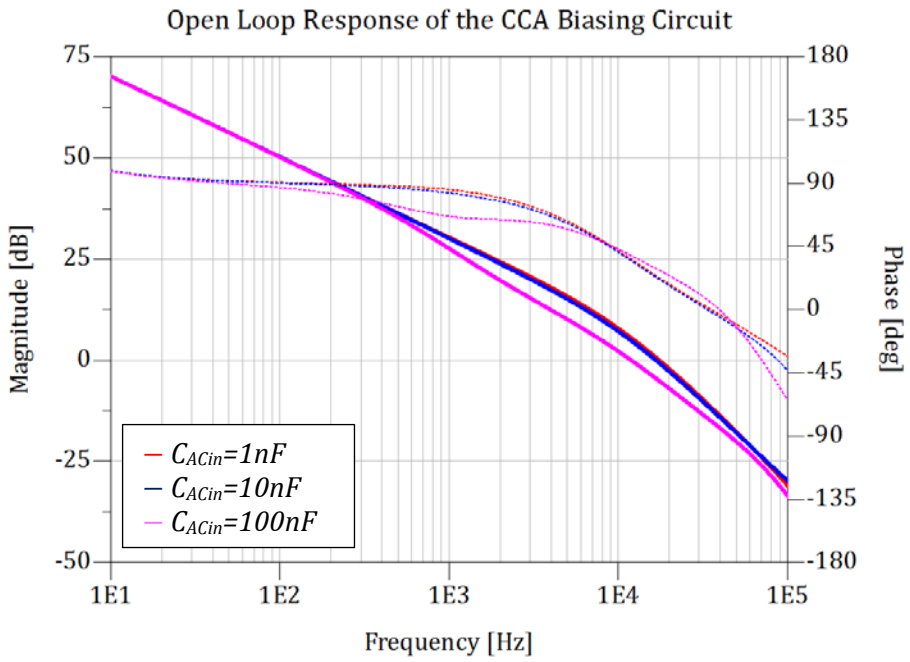

Figure 3.9 Effect of varying the AC coupling capacitor on the open-loop response. Dotted Lines – *Phase*, Solid Lines – *Magnitude*.

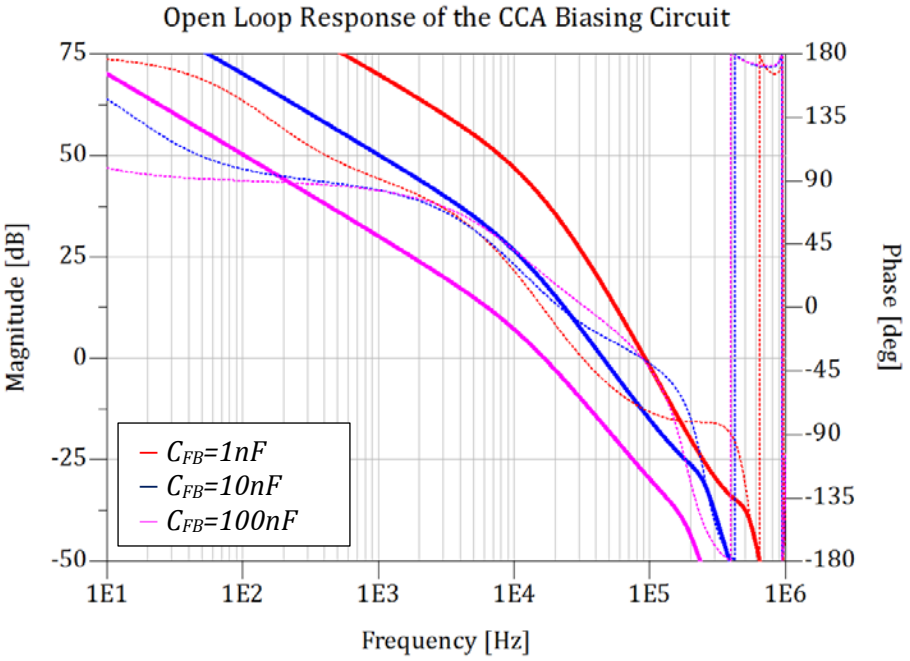

Figure 3.10 Effect of varying the feedback capacitor on the open-loop response. Dotted Lines – *Phase*, Solid Lines – *Magnitude*.

3.5 System Performance

3.5.1 A Discussion on the Simulator

In the following sections, we provide simulations that show the performance of the system in several key aspects. We perform simulations in Agilent ADS due its ability to efficiently perform frequency domain analysis on highly nonlinear analog circuits. The tool used to perform these analyses in ADS is harmonic balance. In essence, the simulator finds the frequency-domain voltages and currents and directly calculates the steady-state spectral content of the voltages and currents of the circuit [14]. The simulator also reconstructs the time-domain waveforms from the harmonics. The simulation runs much quicker than a transient simulation. To learn more about the harmonic balance simulator in ADS, we refer the reader to [14].

Despite the benefits of harmonic balance, with dynamic circuits such as the one presented in this paper, we run into issues. If the circuit is unstable, the harmonic simulator does not reveal this and the simulation seems valid. However, running a transient simulation uncovers the instability. Thus we follow the approach of first running a transient simulation in order to verify stability and then utilize harmonic balance. When using harmonic balance[34], it is important to utilize enough harmonics to properly reconstruct the time-domain waveforms.

Figure 3.11 illustrates the biasing circuit, used in simulation, with the "nominal" values that should, in theory, yield a conduction angle 120°. Note the biasing buffer transistor used is a discrete 2N3904 BJT. Initially, we developed a prototype and then realized that the biasing BJT was losing collector current to the base of the class B device for large drives. To solve this issue, we added the discrete package instead of an IC.

[34] The Krylov Solver is a suggested solver to use when using harmonic balance for its reduced computation time and memory usage, ableit less robust than the direct solver.

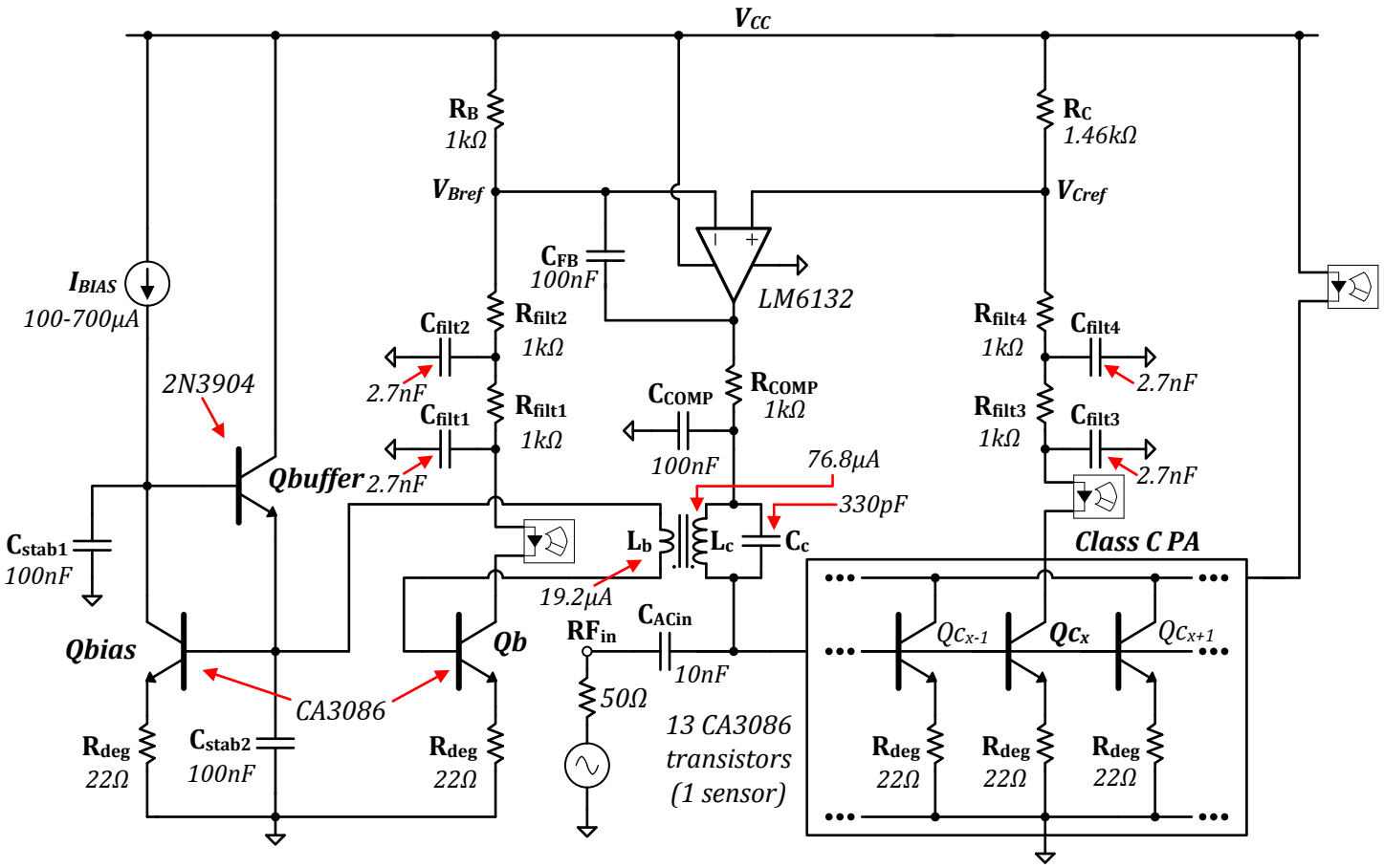

Figure 3.11 The CCA biasing circuit showing values used in the final design. The output network built in the prototype is not shown.

3.5.2 *A Discussion on the Class B Bias*

Naturally an important question the reader may ask is where to bias the class B sensor since a realistic transistor has soft knee. In the real world, there is no class B operation, but what is called class AB operation. Nevertheless, we operate at the knee "as close as possible" to the so-called class B bias. It would seem that as explained in Chapter 2, we want the class B sensor to have a linear fundamental response. However, extensive simulation has shown this not to be true. In fact, we find that a class B response that is slightly class C characteristic produces the best class C PA linearity. However, if we are able to produce a linear class C, the details of whether the class B sensor is linear or not is of no consequence.

3.5.3 *Finding the Optimum Bias, Single Tone Sweeps*

In the previous section, we mentioned that a bias "sweet spot" exists on the knee of the transistor I-V curve that produces the best linearity for the class C PA. To find this we perform single tone sweeps in ADS for various biases. The results from the simulations are shown in Figure 3.12. From the plot, a bias of 300μA appears to yield the best linearity. Additionally, Figure 3.13 shows the currents of the class B and C sensors. This figure shows what we mentioned in the previous section – the most linear class C response does not require the class B response to be linear. The reasoning for this comes from the fact the I-V curve is real and has a soft knee.

To show the benefits of the CCA biasing strategy, using the 300μA bias, we find the adapted DC bias of the class C PA for maximum RF drive. We then apply a fixed DC bias of this value to the class C PA. The result from sweeping the fundamental over the same RF drive range is shown in Figure 3.14. Clearly the CCA biasing strategy has merit.

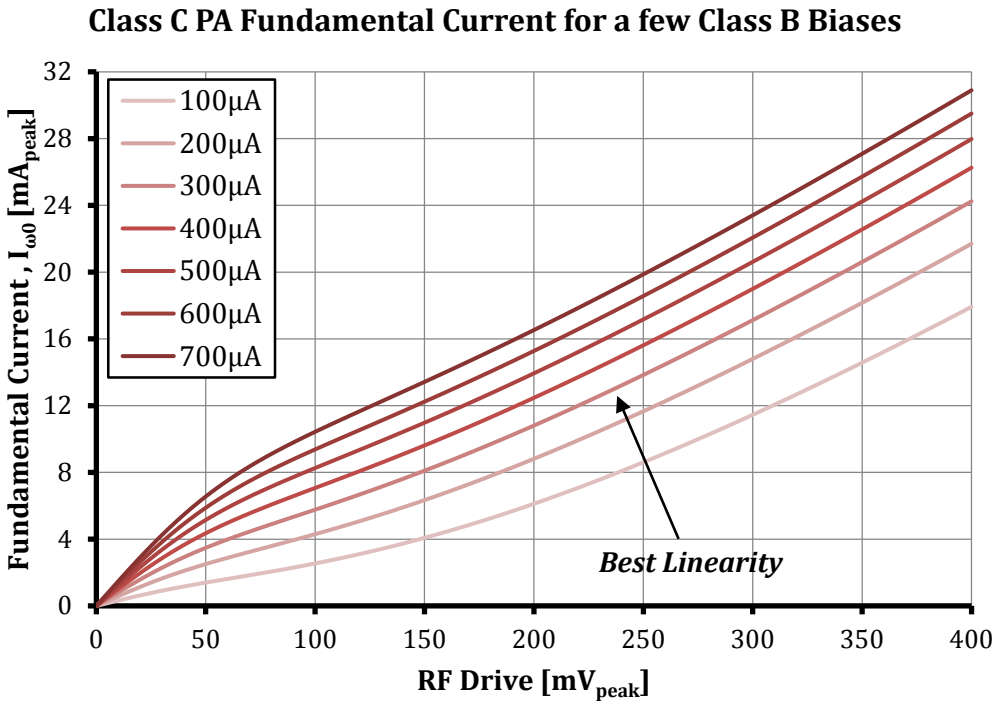

Figure 3.12 Sweep of the fundamental class C PA current for various biases.

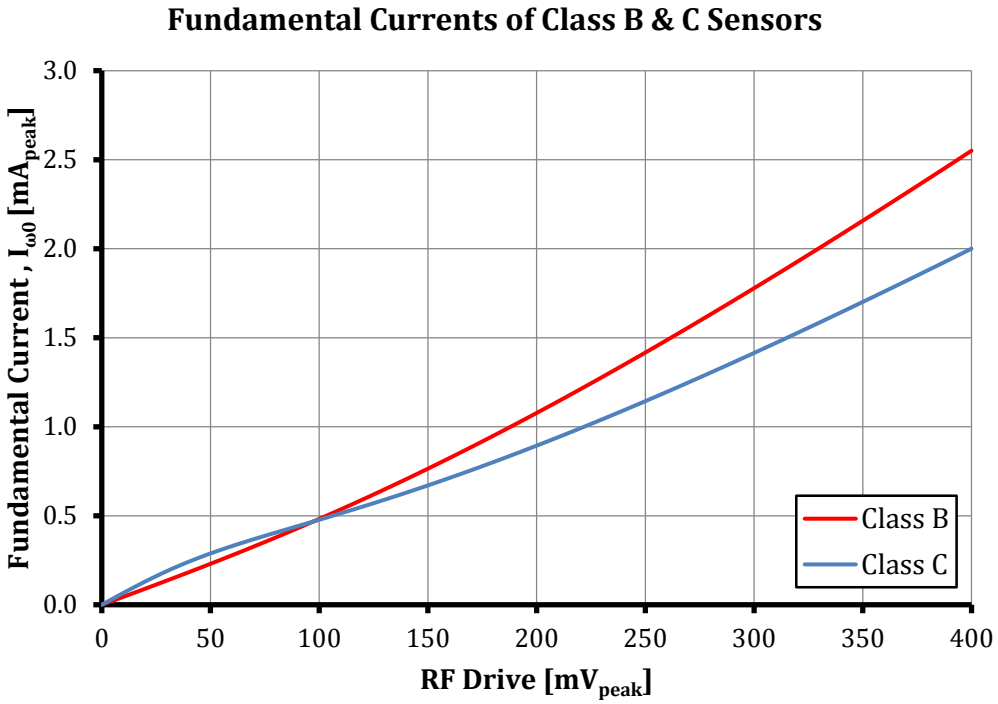

Figure 3.13 Fundamental current of class B and C; I_{BIAS} = 300µA.

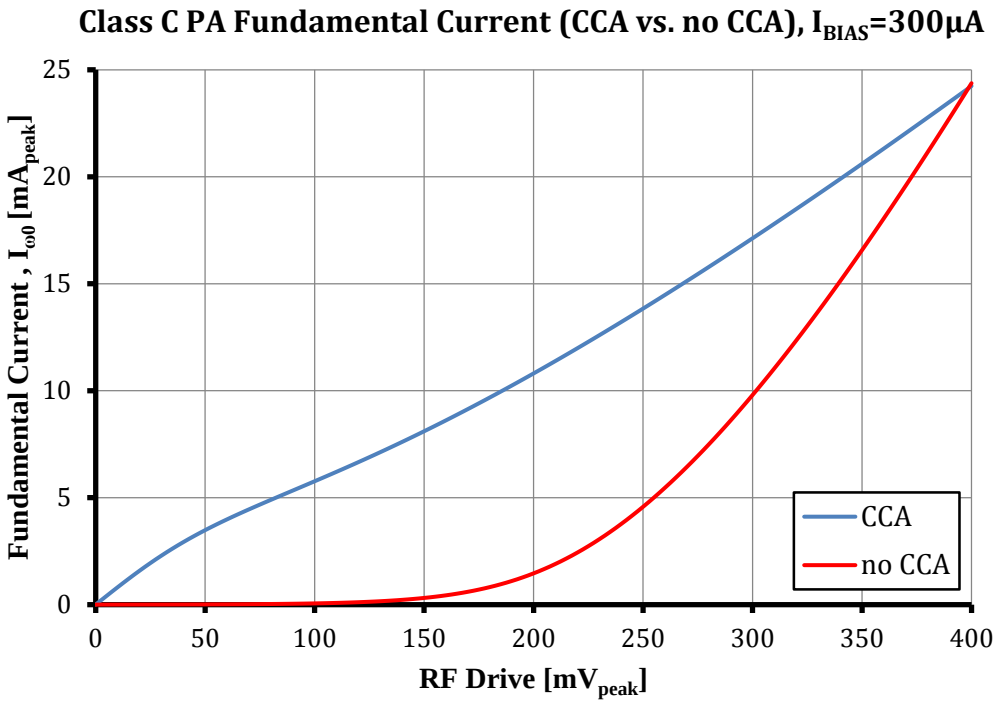

Figure 3.14 Sweep of the fundamental class C PA current for CCA biasing vs. no CCA biasing; I_{BIAS} = 300µA.

3.5.4 A Look at Stability in the Time-Domain

To test the stability of the loop, we ground the input terminal of the amplifier and apply a current impulse[35] sink to one of the "sensor legs". The current impulse applied has a magnitude of 100µA and duration of 1µs. For various bias currents, the simulation reveals a stable loop. An example loop response for the case of a bias current of 300µA is shown in Figure 3.15.

However, when we remove the compensation pole, the loop destabilizes for bias currents above 460µA[36]. The base voltage of the class C PA for the case of a bias current of 500µA is shown in Figure 3.16. Clearly, compensation is a necessity for the CCA biasing circuit presented.

[35] This is the method of "simulating" noise in simulation.
[36] For these bias currents the class C sensor provides enough gain for unwanted oscillation to occur.

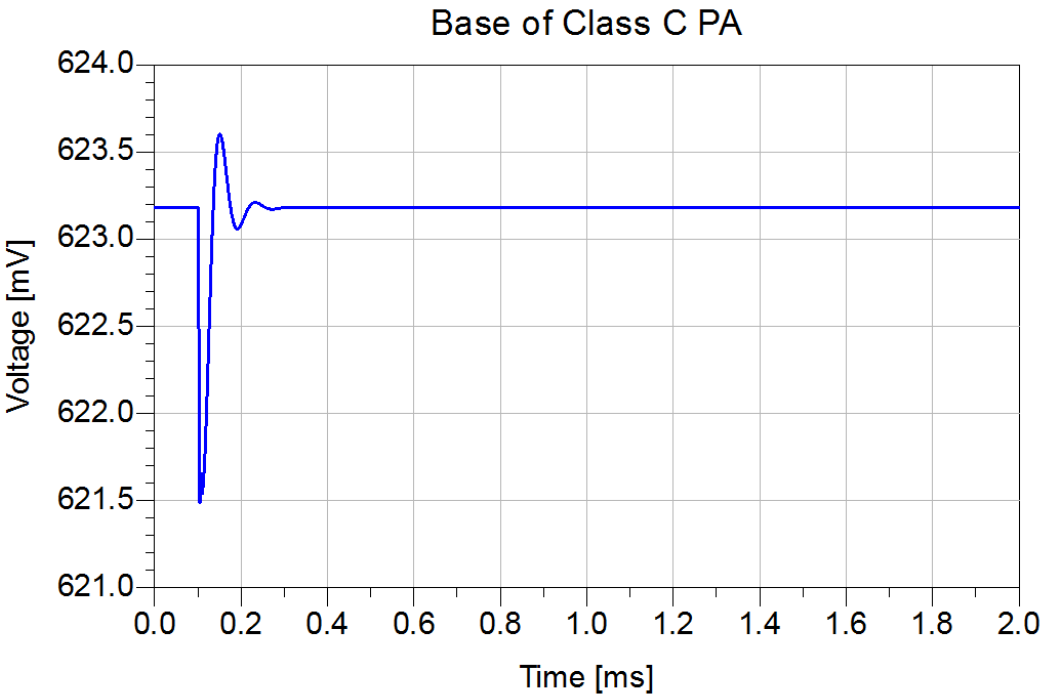

Figure 3.15 Response of the class C PA base due to a current impulse in the loop; I_{BIAS}=300µA.

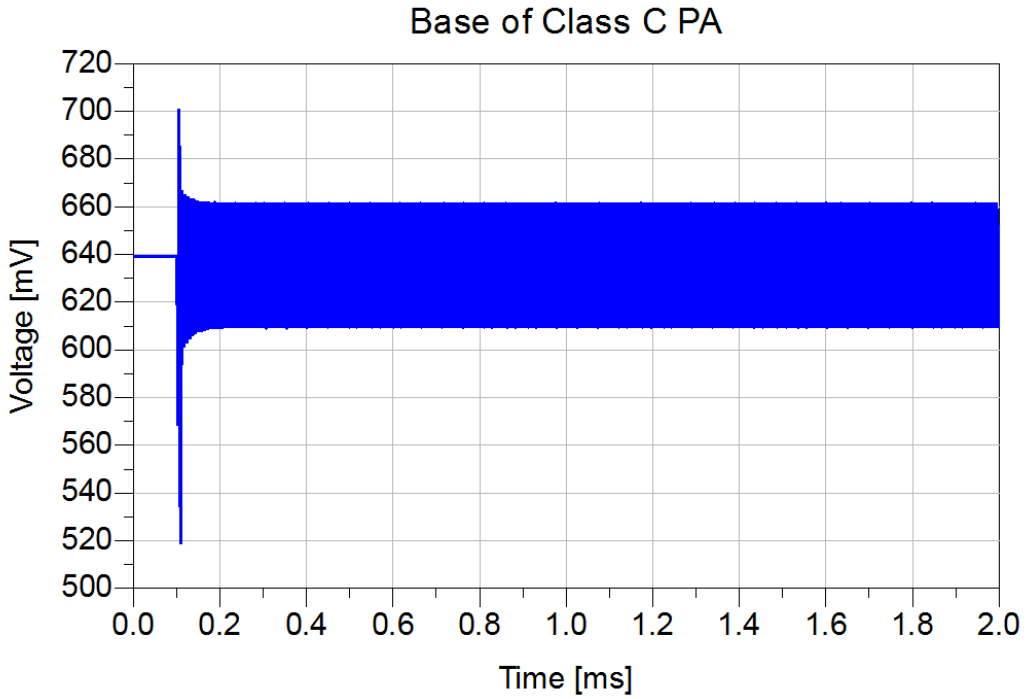

Figure 3.16 Response of the class C PA base due to a current impulse in the loop; I_{BIAS}=500µA. No Compensation.

In our discussion earlier, we showed the effect of changing the feedback capacitance on the open-loop response. What implications does the capacitance have in the time-domain? Consider an input RF signal that undergoes a sudden increase in its amplitude from $100mV_{peak}$ to $400mV_{peak}$. Figure 3.17 shows the class C bias response to this change for three different feedback capacitor values. Although increasing the capacitance reduces the ringing, there is a compromise in the settling time. This settling time is closely related to the bandwidth (Δf) that the system can support and is proportional to the inverse of the settling time (T_S).

$$\Delta f_{max} \propto \frac{1}{T_S} \tag{3.4}$$

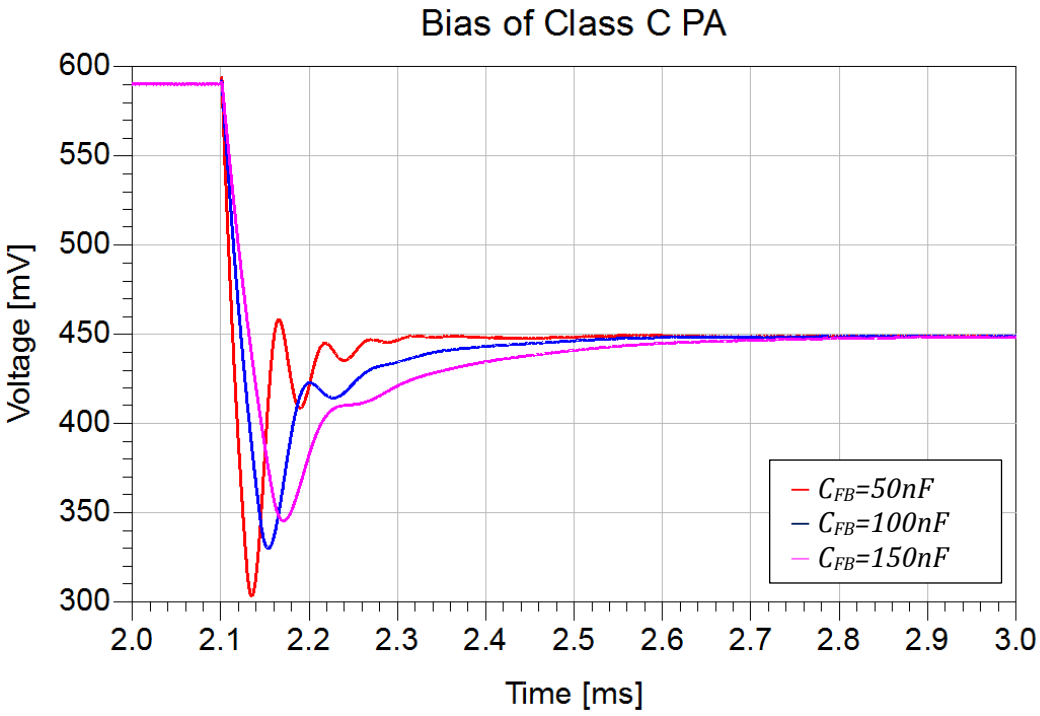

Figure 3.17 Response of the class C PA biasing to a sudden signal increase in the loop for different feedback capacitor values.

3.5.5 *Important Waveforms in the Time-Domain*

In this section we present time-domain waveforms showing correct operation of the CCA biasing circuit. Since a 300μA bias for the class B sensor yielded the most linearity of the fundamental collector current, only simulations at this bias are presented.

Figure 3.18 shows a simulation of the RF input voltages to the class B sensor and the class C sensor and PA[37] for an RF drive of $400mV_{peak}$. As indicated by the figure, the class C PA input voltage waveform reaches the same peak at the same time as the input voltage waveform of the class B device. As discussed in Chapter 2, we are now able to fully utilize the class C PA and produce maximum fundamental collector current.

Figure 3.19 shows how the DC base bias of the class C PA varies linearly with RF drive – the bias decreases as drive increases. However, it is apparent that as the RF drive approaches zero the DC bias curve flattens out. We attribute this "flattening" to the soft knee of transistor I-V curve for a real transistor device such as the CA3086.

Finally, Figure 3.20 shows the collector currents of the class B and C sensors for RF drives up to $400mV_{peak}$. The conduction angle of the class B sensor is constant as expected by the theory. In addition, the class C sensor has a collector current with a conduction angle that is held exceptionally constant. Figure 3.21 shows the class C PA total output current for various RF drives. The difference from the idealized theory is apparent for very small RF drives. Due to the soft knee, there is 360° conduction in these cases. This leads to the nonlinearity seen in the sweep of the fundamental current. However, the fundamental current characteristic is greatly improved to the fixed biased case as shown in Figure 3.14.

[37] Recall that the class C sensor is a "finger" of the whole class C PA.

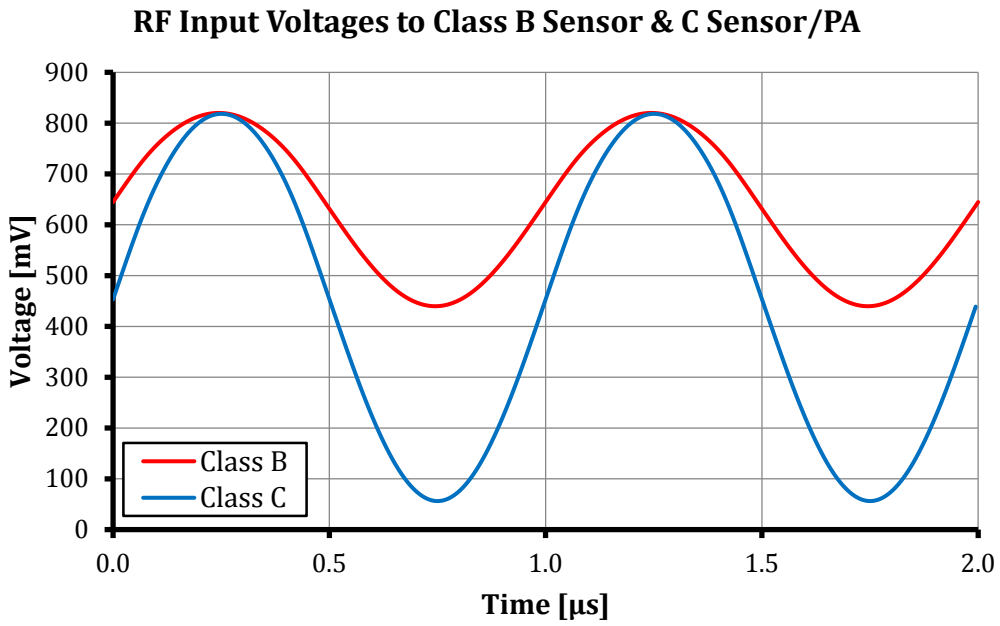

Figure 3.18 Equal peak excursions of class B and C devices; V_{RFin}=400mV_{peak}.

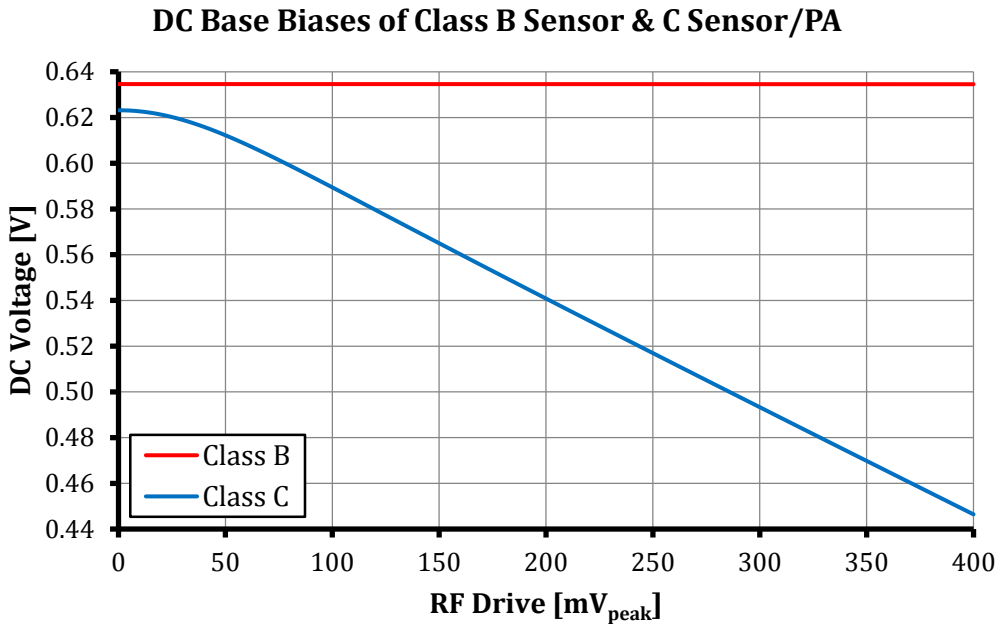

Figure 3.19 Variation of the DC base bias of the Class C PA with respect to RF drive.

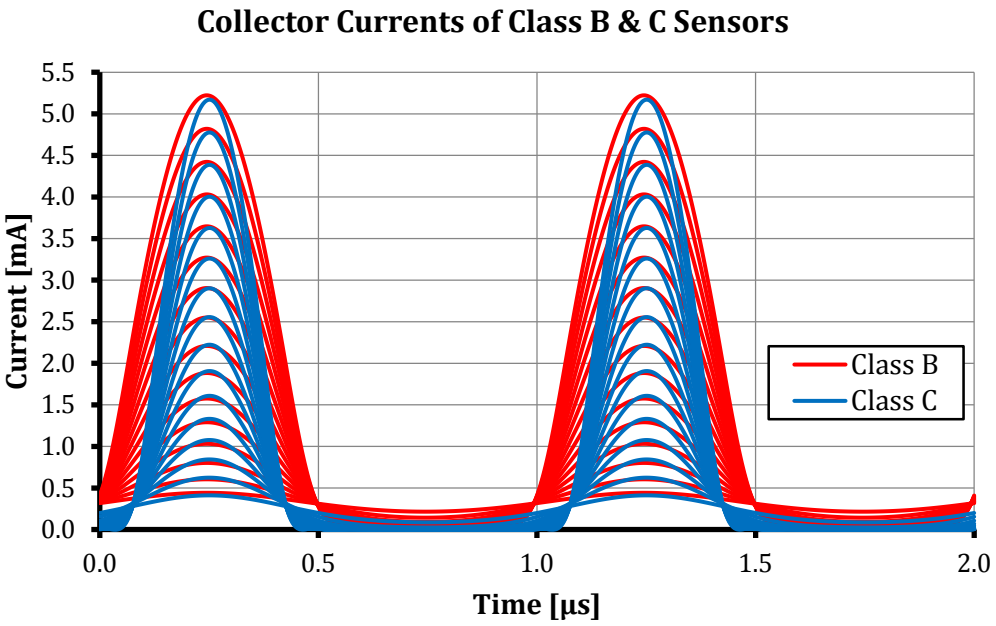

Figure 3.20 Constant conduction angle of the class C sensor collector current over a range of RF drives in addition to the reference class B sensor collector current.

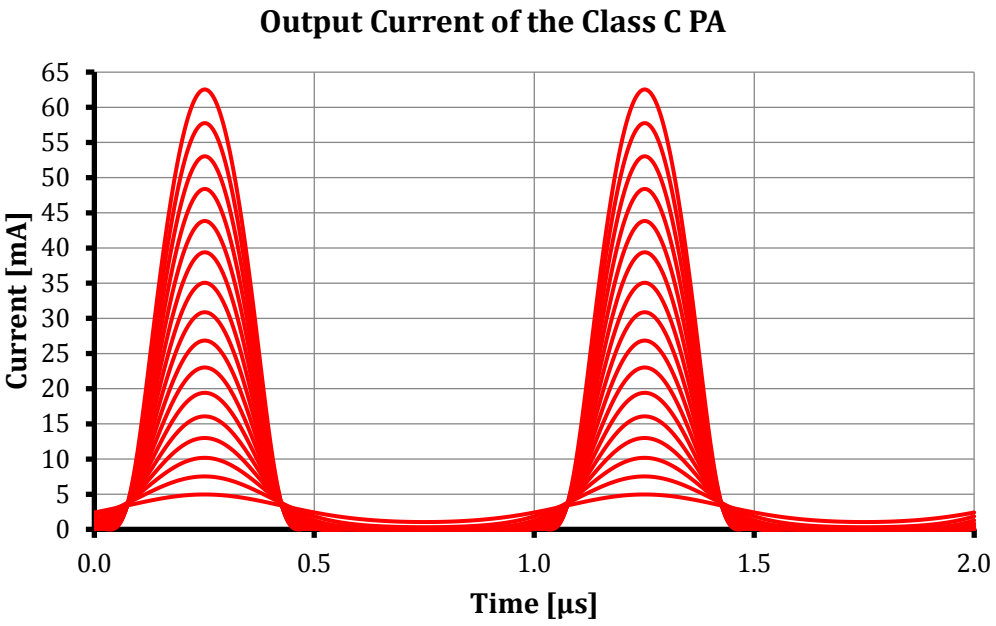

Figure 3.21 Constant conduction angle of the class C PA output current over a range of RF drives.

3.5.6 *Intermodulation Distortion (IMD)*

When designing RF PAs intermodulation distortion, or IMD, is an important issue to take into consideration. It is particularly apparent in the nonlinear class C operation. IMD occurs when two or more frequencies are present at the input of semiconductor devices [15]. Essentially products of these frequencies are produced at the output of the devices. In the case of two tones, the intermodulation products are:

$$\mathrm{M}f_1 \pm \mathrm{N}f_2 \text{ for } \mathrm{M}, \mathrm{N} = 0,1,2, \ldots \tag{3.5}$$

The third-order intermodulation products (IP_3) present the biggest problems in design. They are the closest to the fundamental frequencies and thus hard to filter as illustrated in Figure 3.22.

Since modern RF signals have complex modulation techniques, they consist of multiple frequencies. In practice a "two-tone" test is performed to test the severity of IMD_3 since it is easier to generate two continuous-wave (CW) RF signals than it is to modulate a carrier [16]. The two tones are separated by the bandwidth of the anticipated modulated RF signal[38]. An additional issue with modulated RF waveforms is that the intermodulation bands tend to spread out; this is known as "spectral regrowth" sidebands in the literature [16]. This presents problems in multiple channel communication systems. As channels are closely spaced, these products will tend to leak into the adjacent channels causing distortion and increasing bit error rates (BERs). Thus, it is important to design RF PAs with low IMD_3. Another common term that the reader may encounter in the literature is adjacent channel power ratio (ACPR) which refers to the ratio of the power outside the bandwidth of the main signal to the power of the main signal. The band that defines the adjacent channel is loosely defined and varies from application to application.

[38] The spectrum of this two tone signal is like that of a double sideband suppressed-carrier (DSB-SC).

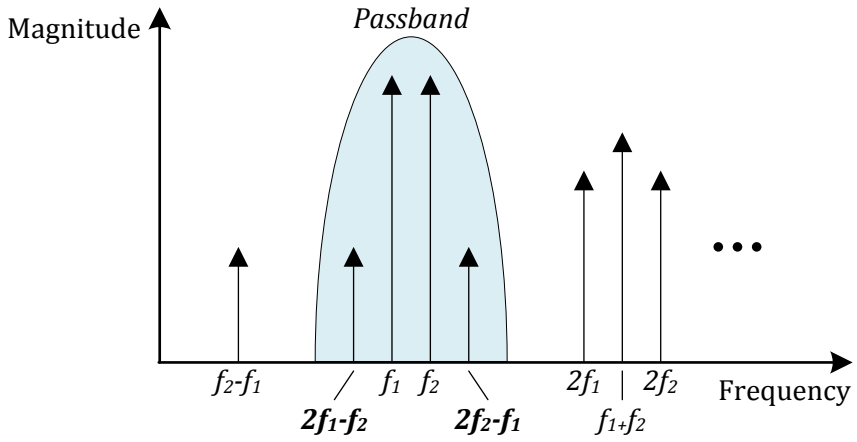

Figure 3.22 Illustration of IMD and the problem of IP_3.

To test the IMD_3, we inject two tones into the CCA biasing circuit. This is easily done in ADS which allows a voltage source with multiple tones to be specified. The IMD_3 relative to the carriers is measured in dBc. Initially a test is done with a small tone separation of 500Hz. The result of this test for biases of 300μA and 700μA is shown in Figure 3.23. Observing the figure, we see that the IMD_3 for the 300μA case is better, as expected, due it having a more linear fundamental characteristic. In addition the IMD_3 approaches a maximum distortion and thereafter improves and approaching a constant value. This non-monotonic response is consistent with reduced conduction angle PAs including class AB PAs.

Holding the bias constant at 300μA, the tone separation is varied and the resulting IMD_3 is shown in Figure 3.24. As expected the IMD_3 becomes worse as tone separation increases. This increase comes from the fact that the system starts to run out of loop gain (see section 3.4.2). In time domain, this can be thought of as the system not responding fast enough to follow the envelope of the RF signal. This failure typically shows itself as phase error in the response.

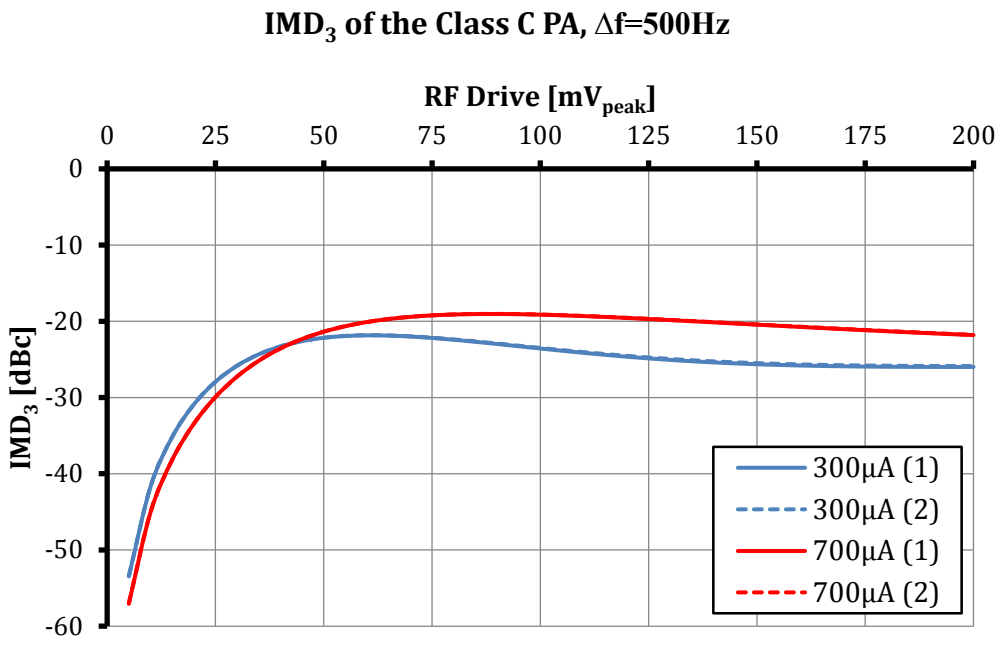

Figure 3.23 IMD_3 of the class C PA; Δf=500Hz, I_{BIAS}=300µA, 700 µA.

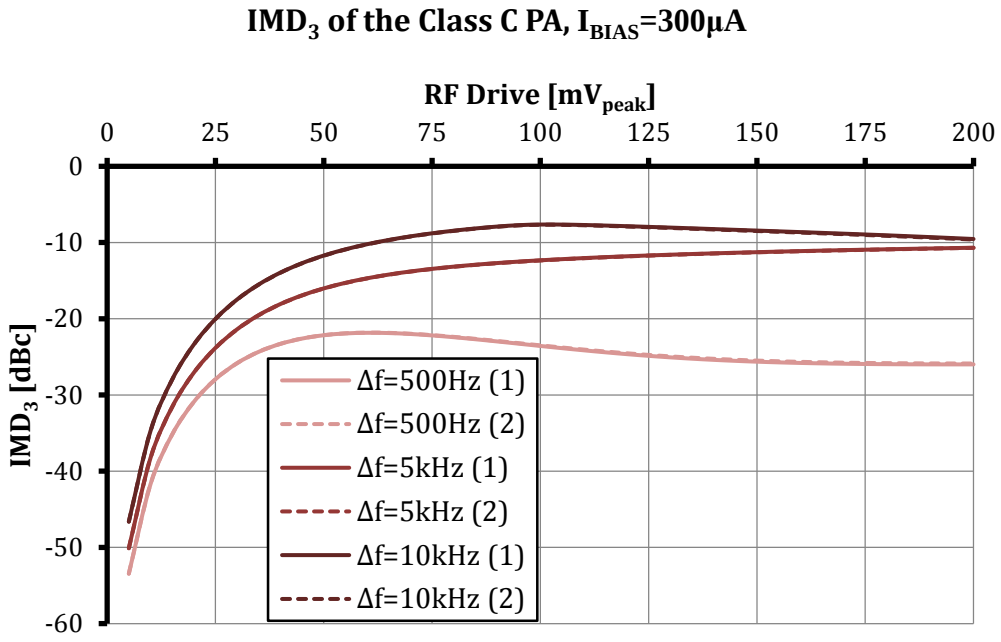

Figure 3.24 IMD_3 of the class C PA for various tone separations; I_{BIAS}=300µA.

4

CCA Biasing Prototype & Lab Results

4.1 The Prototype Designs

To quickly prototype the CCA biasing circuit, an initial prototype was built on a solderable breadboard (FR4). At 1MHz, this is a feasible design. A 1MHz signal has a wavelength[39] of about 300m assuming a propagation velocity of the speed of light (c). In actuality depending upon the material (particularly the dielectric constant) this will be somewhat less. In the case of FR4, which typically has a dielectric constant of 4.2, the propagation velocity is about half c [17]. Thus, the wavelength would be about 150m. The breadboard used in the preliminary prototype measures about 17.5cm in length. For all practical purposes the voltage at any given time is constant over this length.

In parallel to building the first prototype, a PCB layout was done in Cadsoft Eagle. This popular PCB design software comes in a free light edition which allows the user to generate a layout with two signal layers and a board area limited to

[39] Recall wavelength (λ) equals the propagation velocity (v) divided by the frequency (f).

100 x 80mm. Although detailed tutorials are found on the Cadsoft Eagle website[40], Appendix C contains a simple tutorial developed by Matthew Bloom[41].

The first PCB board fabricated, however, did not have a buffered bias and the placement of some parts was inconvenient. After some deliberation and realizing the need to buffer the biasing transistor, a second PCB board was fabricated with revisions. The reader can find the layout of the initial prototype and the schematic and layout of the final design in Appendix D.

4.1.1 The Initial Prototype

Figure 3.9 shows a picture of the top and bottom view of the initial prototype constructed on breadboard. As shown, three CA3086 ICs are used to implement the biasing, class B and C sensors and the class C "power transistor." A couple of important comments regarding the implementation follow. First, each of the ICs has a substrate connection connected to the emitter of one of the 5 NPN BJTs. The substrate connection must be connected to the most negative point of the system to maintain isolation between the transistors in the array and ensure normal transistor behavior [18]. Secondly, the CA3086 ICs have a pair of transistors that are connected as a differential pair (i.e. their emitters terminals are tied together). These transistors are used as a part of the class C power transistor with 11Ω of degeneration, instead, to provide same effect as 22Ω for two isolated BJTs.

The LM6134 IC provides two op-amps in a package. As we only utilize one of the op-amps for the non-inverting integrator stage in the CCA biasing topology, the other op-amp must be properly terminated. In our implementation, we grounded the op-amp input and left the output open. This did not result in any adverse effects. However,

[40] See http://www.cadsoftusa.com/training/tutorials/.
[41] A dedicated student and great friend, who know works for NASA's Jet Propulsion Laboratory.

Maxim Integrated specifies a better method in dealing with uncommitted op-amps in [19].

In terms of the biasing stage, the LM334 adjustable current source is used to source the biasing stage with a good degree of constant current regardless of supply variation. We configure the current source as shown in Figure 4.2. The variable resistor R_{SET} sets the current by the following relation:

$$I_{BIAS} = \frac{227\ \mu V/°K}{R_{SET}} \xrightarrow{@Room\ Temerature} \frac{\sim 67mV}{R_{SET}} \tag{4.1}$$

The 1kΩ resistor placed in series with the current source allows easy measurement of the current by virtue of the voltage drop across the resistor. As mentioned in Chapter 3, we use a discrete 2N3904 NPN BJT to "buffer" the bias-setting transistor.

The transformer used to drive the class B sensor is made by making two windings of 26 AWG (American Wire Gauge) magnetic wire on an FT37-43 ferrite core. Figure 4.3 shows a pictorial on how to wind the coils such that the voltages are in phase. In addition, (4.2) show the relationship voltage-, turns-, and inductance-ratio of the secondary and primary sides. One side resonates to act as a choke for the base biasing of the class C device; this side is designed first and measured on a Vector Network Analyzer (VNA).

$$\frac{V_s}{V_p} = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}} \tag{4.2}$$

The output network shown in Figure 3.9 is designed by first measuring the inductors and then choosing the capacitors to elicit the best response. The toroidal inductors, pictured on the top side of the board, are in series and act as the series inductance for the matching network.

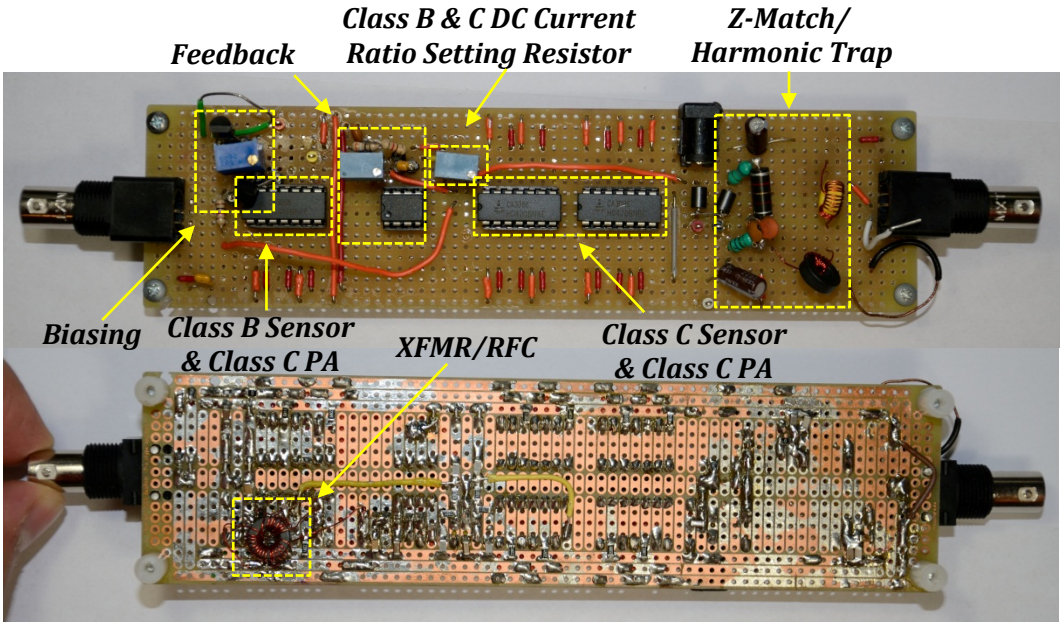

Figure 4.1 Top and bottom, respectively, of initial CCA biasing prototype.

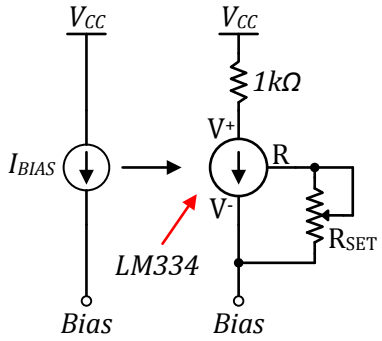

Figure 4.2 Implementation of bias current source using an LM334 adjustable current source.

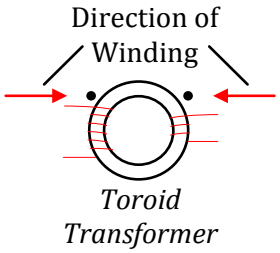

Figure 4.3 Winding a toroidal transformer for in-phase coupling.

4.1.2 The Final PCB Design

Figure 4.4 shows a picture of the top and bottom sides of the PCB prototype of the CCA biasing circuit. As in the initial prototype, IC sockets are used for the ability to conveniently replace a bad IC. As in the case of a true RF circuit design, the bottom layer is used as a ground plane. However, there are a few traces such as power and the class C base connection that are also run on the bottom layer. They are seen as the insulated traces on the bottom in Figure 4.4. We run the class C base line on the bottom layer since it is naturally lower power than the class C collector line. Again, as in the case of good RF circuit design practice, ground via fences are added along the main collector line[42]. Also, a few test points (see the figure) are added to view different waveforms on the prototype.

In order to have a prototype which could be "tuned" to a different conduction angle, a potentiometer is used for class B DC current-setting resistor. However, the secondary windings of the transformer used to deliver the signal to the class B sensor, would need changed when selecting a different conduction angle.

The output network contains several tunable inductors used to implement the impedance matching and short the harmonics. The supply is filtered with a series of capacitors as shown in the figure. We use a ferrite bead in the path of the DC supply to prevent the resonance of the AC filtering capacitors with the inductance of the long lead length of the supply lines. The output AC coupling capacitor does not impact the performance of the CCA biasing circuit and thus a large 1μF valued capacitor is used to act as a "short-circuit" to the 1MHz signal.

[42] At 1MHz, these via fences likely affect the response by much. However, for designs in the GHz frequencies, they help reduce crosstalk tremendously designed correctly [23].

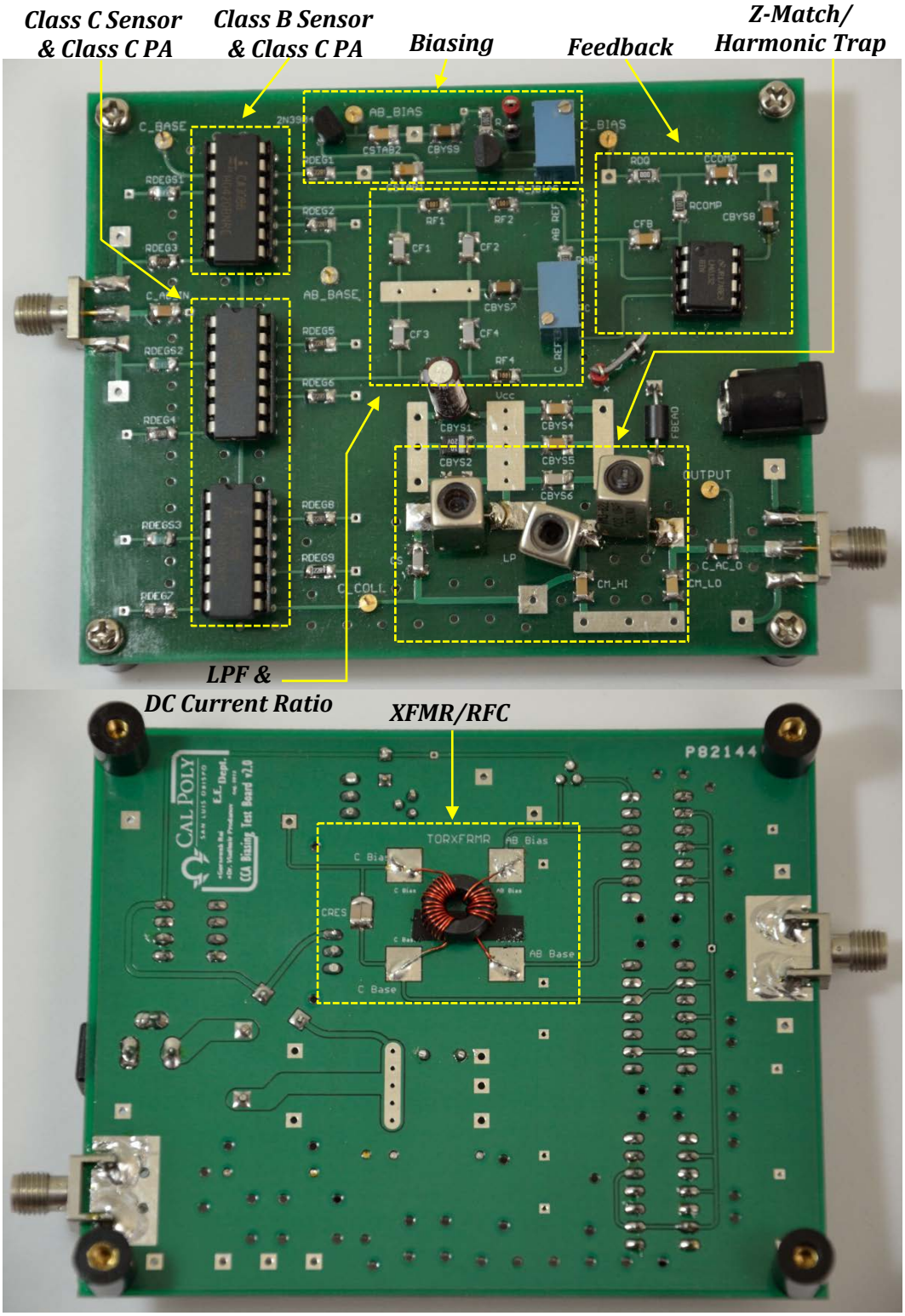

Figure 4.4 Top and bottom, respectively, of final PCB CCA biasing prototype.

4.1.3 The CA3086 I-V Characteristics

Terminating the prototype in 50Ω at the input and output terminals and measuring the class B bias voltage resulted in a 60mV difference from simulation. In order to understand where this difference came from, we decided to measure the practical I-V curve. To do this, we diode-connected a CA3086 BJT as shown in Figure 4.5 and applied the LM334 current source. The measured source current[43] and base voltage is plotted as an I-V curve in Figure 4.6; the I-V curve from simulation is also plotted to show comparison. Apparent in the figure, there is about a 60mV increase in the base voltage of the actual device for the same current. Testing several CA3086 ICs resulted in the about the same shift in characteristics.

Despite this strange difference, the operation of the CCA biasing is not compromised as this shift only increase the voltage. This increase is consistent with all the CA3086 transistors in the three ICs used and thus the criterion for matched transistors is still met. However, a caveat of this shift in the I-V curve is that DC power dissipation increases.

[43] The collector current will be practically the same as the source current as the base will draw a much smaller current.

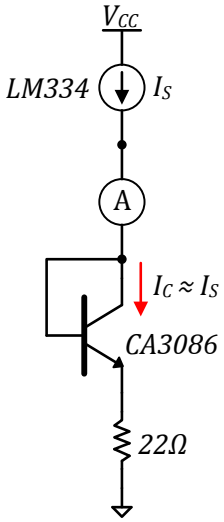

Figure 4.5 Test setup to measure the CA3086 I-V curve.

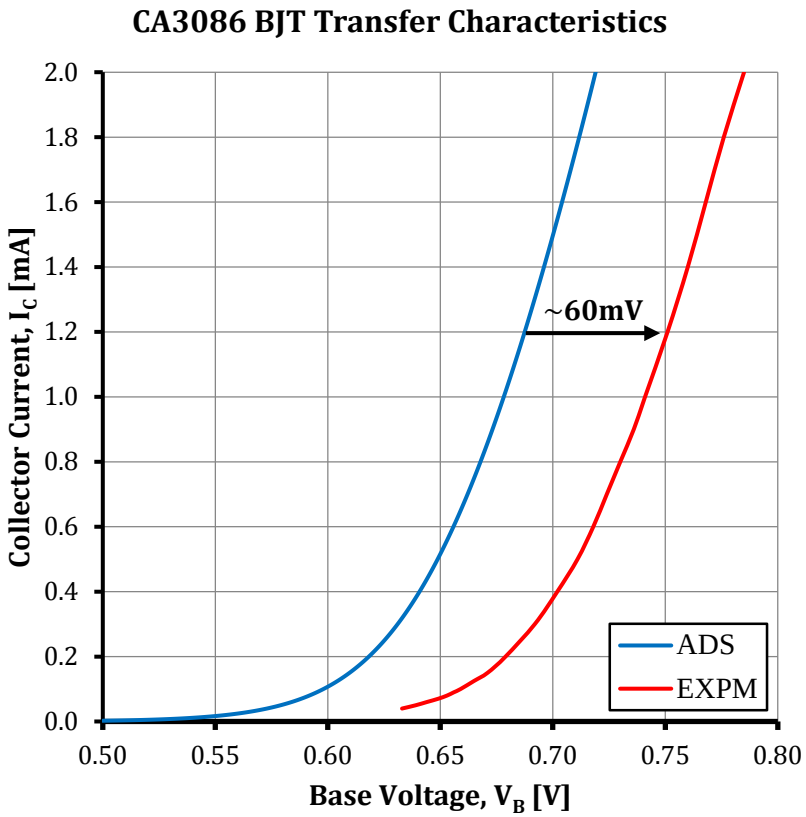

Figure 4.6 Measured and simulated I-V curve for CA3086 with 22Ω degeneration.

4.2 Bias Choke & Output Stage Design

In this section we discuss the design and measurement of the bias choke and the output stage. In measuring the inductors and the impedance responses we used the HP8753A VNA shown in Figure 4.7. Copper top boards like the one shown in Figure 4.8 were constructed to make the measurements.

VNAs deal with S parameters which relate incident and reflected waves in a two-port network. We refer the reader to [20] for a discussion of S parameters and why they are useful in RF measurements. The input reflection coefficient (S11) is of most concern to us as it is proportional to the input impedance as indicated by (4.3). Note, Z_0 is the characteristic impedance of the system and is 50Ω for VNAs.

$$Z_{IN} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{4.3}$$

Figure 4.7 HP8753A VNA used to measure inductors, capacitors, and impedance responses of the bias choke and output network.

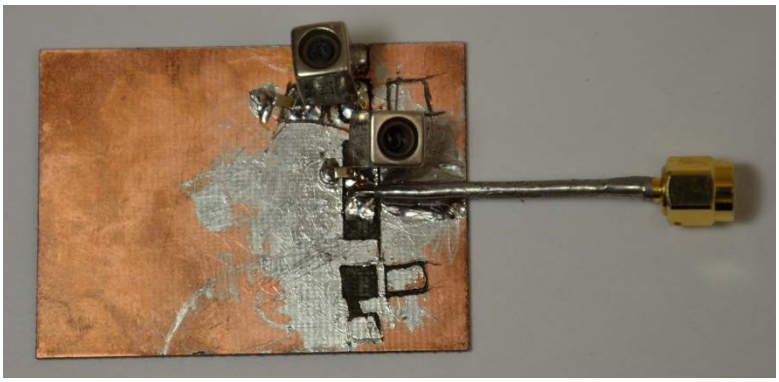

Figure 4.8 Example "prototype" copper top board used to measure components and the impedance response of the bias choke and output network.

4.2.1 The Class C Bias Choke

The class C bias choke serves two purposes: to couple the signal to the class B sensor via the toroidal transformer and to act as a choke to the RF current of the input signal. The measured inductance of the primary side of the toroidal transformer was about 73.7μH. For resonance at 1MHz, this requires a parallel capacitor with a value of about 344pF. In the implementation, we used a 330pF in parallel with 12pF. The measured impedance response is shown in Figure 4.9. Figure 3.19 shows that the choke provides 8kΩ or more impedance for a relative bandwidth[44] of 5% or less.

[44] Relative bandwidth refers to the ratio of the bandwidth to center frequency.

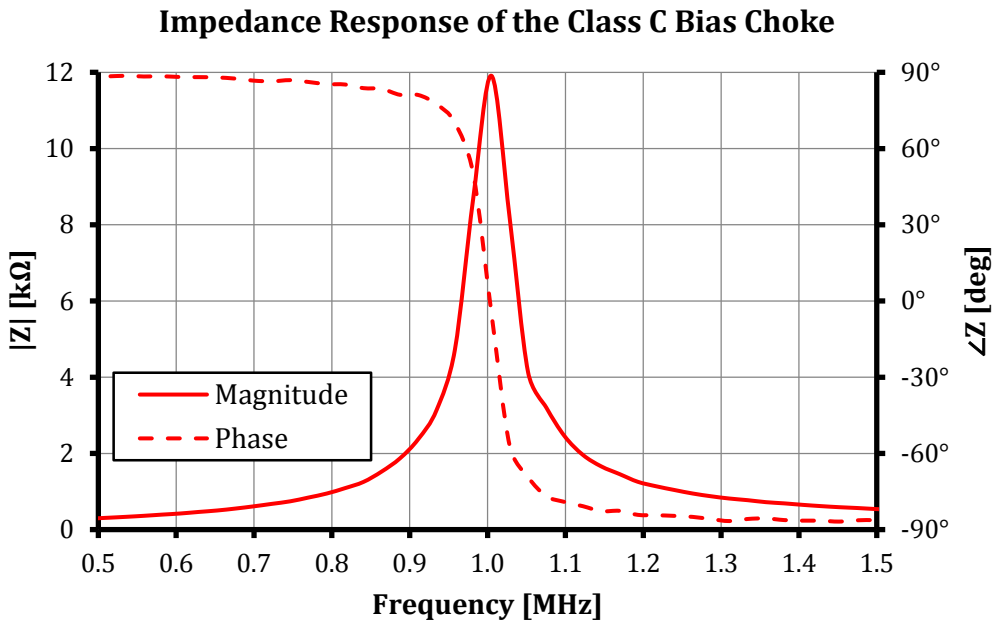

Figure 4.9 Measured impedance response of the class C bias choke.

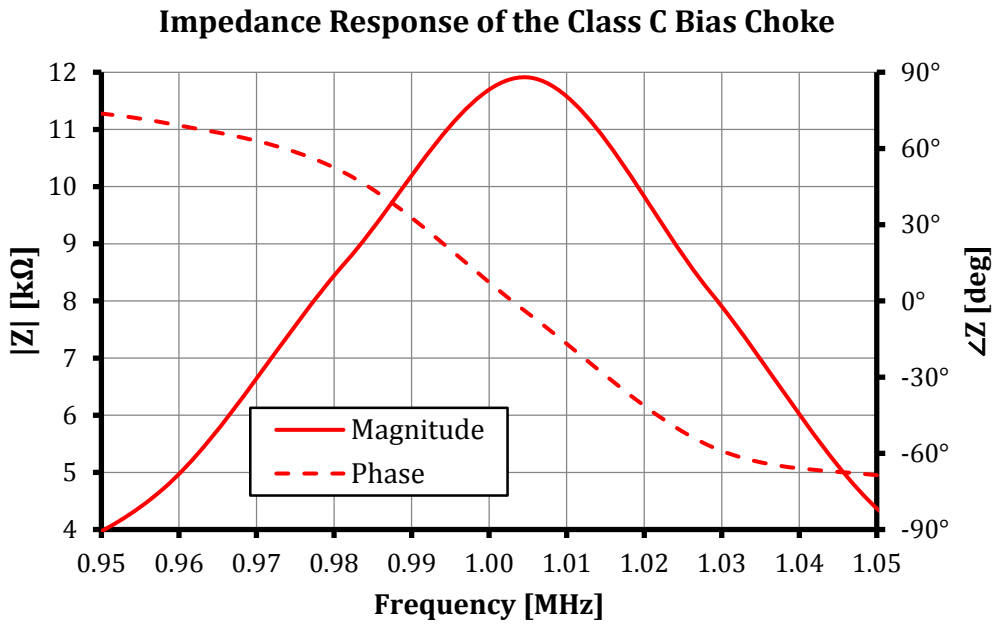

Figure 4.10 Impedance response 50kHz above and below 1MHz.

4.2.2 The Output Stage

In Chapter 3 we made briefly mentioned the output network and its need. In this section we emphasize the importance of the filtering and impedance matching. Observing Figure 4.11, the output current of the class C PA will be the reduced conduction angle current discussed throughout this paper. However, it contains harmonic content (particularly the second harmonic) that we don't want to deliver to the load. Thus we filter this out with a harmonic trap as shown in the figure. A second important point to note in the figure is that for the maximum current, the ideal maximum voltage swing in the case of BJT or FET device would be from 0V to twice the supply voltage. In practice, we would back off slightly on this swing so as not to saturate the transistor when the voltage swings down to 0V. Nevertheless, the optimum load is therefore the ratio of the peak voltage and fundamental current.

$$R_{opt} = \frac{V_{load,peak}}{I_{f_0,peak}} \tag{4.4}$$

This method of selecting[45] the load resistor is known as "loadline" matching and is discussed in [21]. Since this optimal load resistance is almost always different from the standard 50Ω load encountered in RF systems, we must use an impedance matching network. The matching network essentially lowers the voltage swing while increasing the current swing in order to transfer the full power to the load.

The popular lowpass pi-type matching network shown in Figure 4.12 has an advantage over two-element matching network in terms of flexibility in design, especially in fine-tuning the response. It allows for quality factor specification. The values may be solved for analytically as shown in [22] or through the use of a Smith chart as shown in [23]. In our design, we used an online calculator[46] that was quite accurate.

[45] In practice load pull techniques are used to find the optimum load impedance.
[46] See http://www.vk2zay.net/calculators/piMatchingNetwork.php.

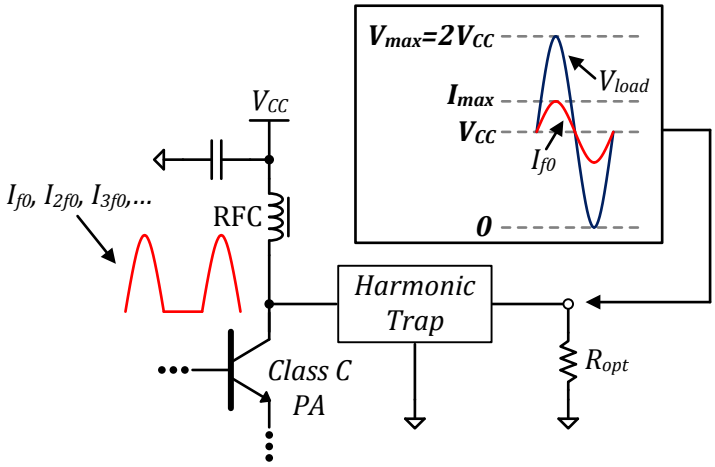

Figure 4.11 Class C PA output stage description of voltage and current waveforms.

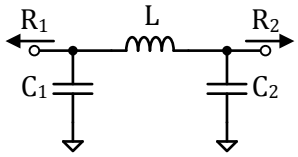

Figure 4.12 Schematic of a lowpass pi matching network.

4.2.3 The Design of the Matching Network/Harmonic Trap

Figure 4.13 shows two designs that were considered for the output network. The fundamental difference between the designs is that one utilizes resonance to prevent the fundamental current from passing through while the other utilizes a large inductor or RF choke (RFC). The first design has obvious benefits at the design frequency of 1MHz, because a large RFC in the hundreds of microhenries to a millihenry would be required in order to use the second design. Notice in the figure, that a series LC is shown in the place of a capacitor. In both designs, this acts as an effective capacitor at the fundamental frequency and a short-circuit to the second harmonic current. This is necessary as a class C PA has a particularly strong second harmonic. The design of this series LC is discussed in Appendix E.

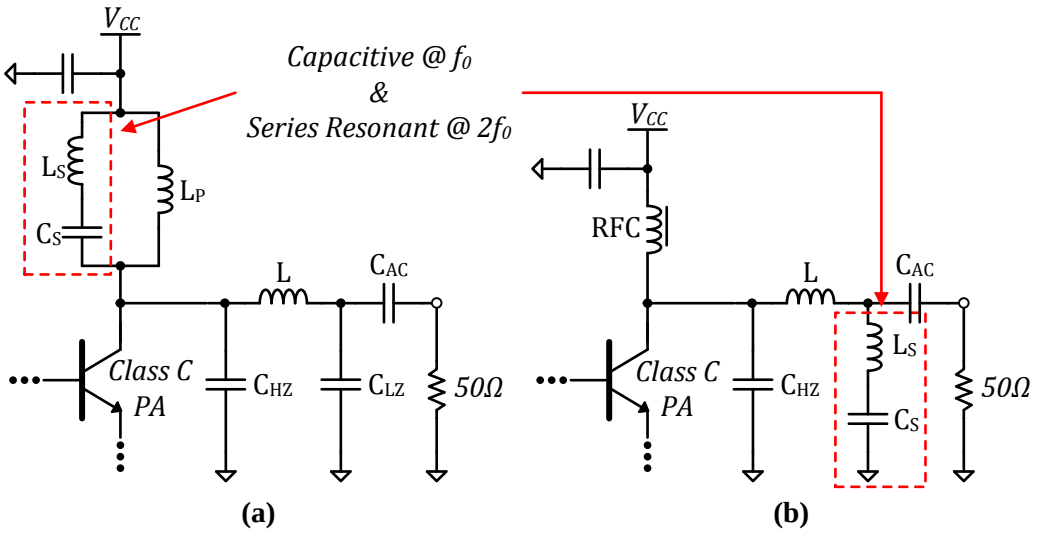

Figure 4.13 (a) Matching network and harmonic trap design #1; (b) Matching network and harmonic trap design #2.

The networks[47] in Figure 4.13 were built on copper top boards like the one shown in Figure 4.8 and tested using the HP8753A VNA. As discussed in the previous section, we want to design a match that elicits maximum collector voltage swing at maximum fundamental current output. In the CCA biasing implementation, the maximum fundamental current was somewhat unclear. A fundamental output current of $26mA_{peak}$ was chosen since the corresponding class C RF input reaches ground on its downward swing. Since the implementation is done in a CA3086 IC with its substrate grounded, we would not like the input to drive below ground as this could possibly forward bias the substrate and destroy the IC[48]. In terms of the collector voltage, the voltage can swing from 0 to twice the supply voltage. However, in order to prevent saturation of the transistor and the swing is designed for 7V (the supply is 8V). This results in a load resistance of 270Ω. Thus, we must match from 50Ω to 270Ω.

[47] In the case of design #1, the network connected to V_{CC} was tied to ground when tested on the VNA. In design #2, the RFC was not included during testing.
[48] Practically, the device should not be affected for a swing of up to a few hundred millivolts below ground.

Using the online calculator mentioned earlier, the pi matching network components were generated for a nodal Q design of 9 (see Figure 4.14). In order to implement the output networks, we used tunable inductors from Coilcraft and surface mount capacitors and a 50Ω surface mount resistor for the load impedance. The tunable inductors used and their inductance ranges are shown in Table 4.1.

Figure 4.15 shows both output network designs with the values required to match 50 to 270Ω. The resulting impedance response (as seen by the collector of the power transistor) for both networks after tuning is shown in Figure 4.16. Despite, quite an effort put in tuning, the response was not able to tune to 270Ω at 1MHz. This may have been due to the capacitors being off and since we did not have any tunable capacitor's we could not see the effect of varying the capacitors on the impedance response. The more likely issue may be that the inductors used did not have enough Q to support this impedance scaling. In any case, we see that design #1 does a good job at filtering the second harmonic. However, there is a second resonance that occurs between 2 and 2.5MHz. This resonance is small and occurs at a non-harmonically related frequency. The second design, although doesn't have a second resonance, does not do a good job in filtering the second harmonic.

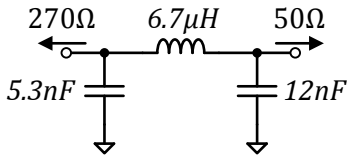

Figure 4.14 PI matching network, matching 50 and 270Ω with a Q of 9.

Table 4.1 Coilcraft tunable inductor inductance ranges, specified and measured.

Tunable Inductor	Specified Range	Measured Range
7M2-821	0.738-0.902μH	N/A, tested at 0.72μH
7M3-153	11-19μH	~20-30μH
7M3-822	6.6-9.8μH	~4-12μH

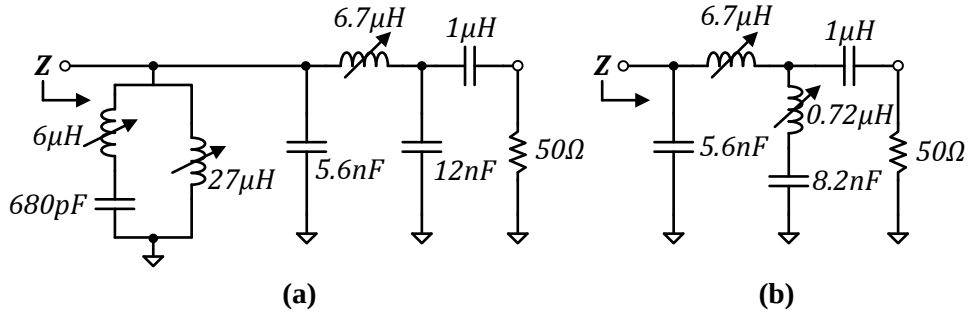

Figure 4.15 (a) Component values used to match 50 to 270Ω in design #1; (b) Values used to match 50 to 270Ω in design #2.

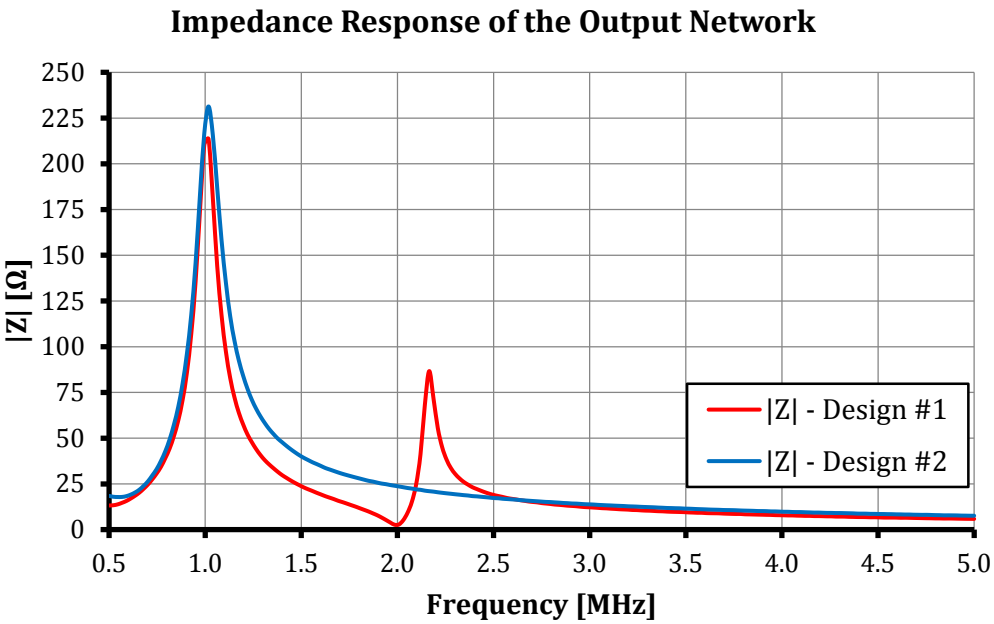

Figure 4.16 Measured and tuned impedance response of the output network for both designs.

4.2.4 Tuning the Response on the VNA using the Smith Chart Display

The Smith chart is a powerful graphical tool used in solving many problems in the RF discipline. The reader may find a wealth of information on the internet on Smith charts. In our discussion here, we are concerned with the impedance aspect of the Smith chart. Figure 4.17 shows some important characteristics of the Smith carth. Particularly, the top half represents inductive impedances and the bottom half represents capacitive impedance. The middle represents purely resistive impedances. Impedances along the outer circle are purely reactive. From the left to the rigth, impedance increases from short circuit to open circuit. In addition, there are constant resistance circles where the resistive part of the impedance stays constant while the reactive part changes. Constant reactive curves represent the opposite scenario.

The output response of design #2 is shown in Figure 4.18. Although, the measurement is S_{11}, the Smith chart shows input impedance of the network. In addition, the complex impledance is shown on top of the chart (indicated in the figure). The impedance curve moves in a clockwise direction with frequency.The cross-over point between inductance and capacitance is where there is parallel resonance. As seen in the figure, the resonance is mistuned at a higher frequency then 1MHz. The series resonance is also mistuned as it is not at the short-circuit point on the Smith chart. Using the tunable inductors, we tune the the response such that the fundamental resonates at the correct impedance. The tuned response is shown in Figure 4.19. Consistent with the unfortunate result seen in the last section, the 50Ω load is not matched to 270Ω but rather about 221Ω as seen in the figure. In addition, the circuit still presents some impedance at the second harmonic. The aformentioned tuning process was performed on design #1 (not shown since a screen capture was not taken at the time).

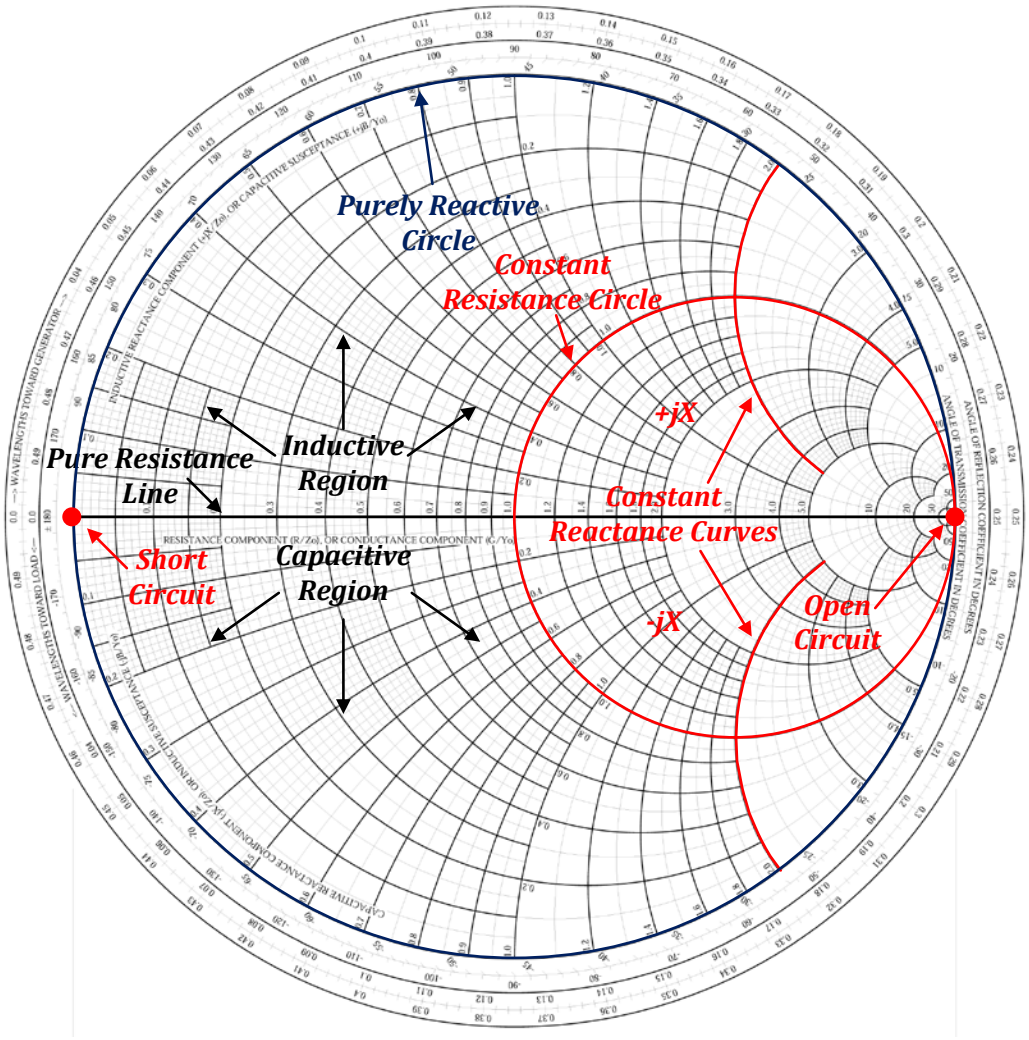

Figure 4.17 A Smith chart showing several key impedance characteristics.

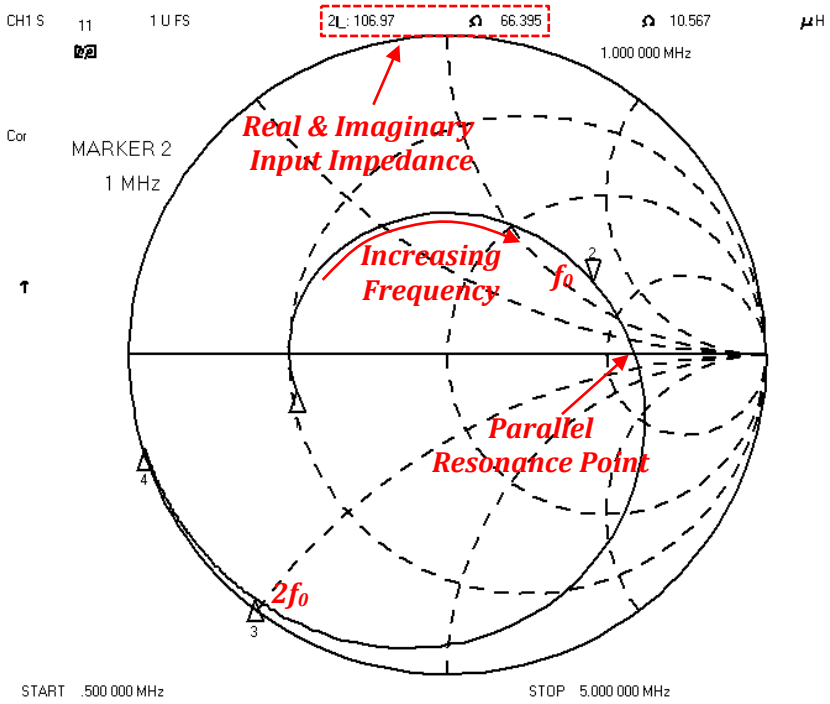

Figure 4.18 S_{11} response of untuned output network (design #2). Smith chart.

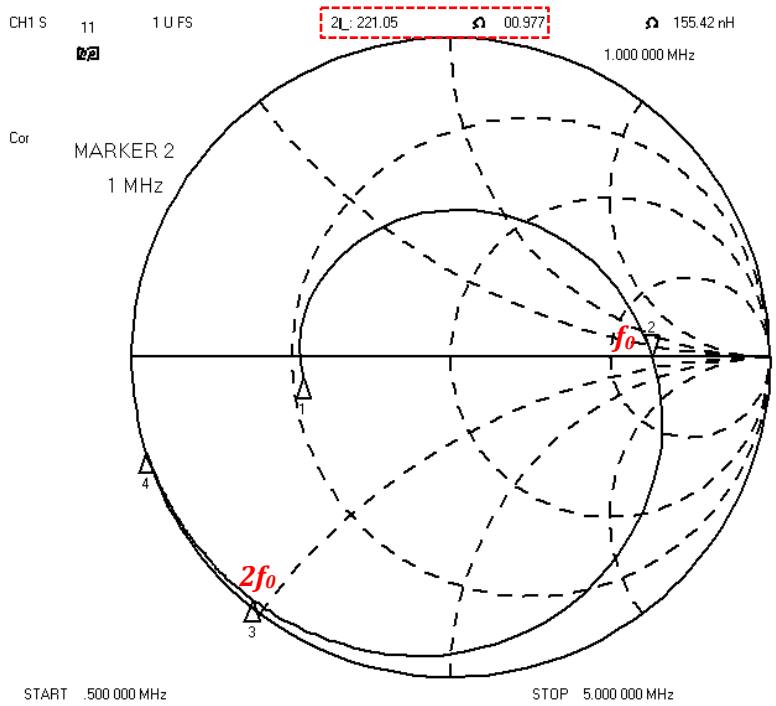

Figure 4.19 S_{11} response of tuned output network (design #2). Smith chart.

4.3 System Performance

In this section, we provide lab results that closely agree with the simulations. The results prove the real-world merit of the CCA biasing topology. We begin by verifying the optimum bias predicted in simulation, then explore stability, view CCA waveforms, measure IMD_3 and finally make a quick investigation of the efficiency of the class C PA.

The main test equipment used is shown in the following figures.

Figure 4.20 The Agilent MSO-X 2012A function generator/oscilloscope used as the RF source to the PA and used to view waveforms on the prototype.

Figure 4.21 The Rigol DG1022 function generator used to source to two-tones for the IMD_3 measurements.

Figure 4.22 The Agilent CXA N9000A spectrum analyzer used perform spectral analysis on the class C PA.

4.3.1 The Optimum Bias and Harmonic Content

Prior to adding the matching network and tank, we configured the output of the class C PA as shown in Figure 4.23. The 330µH inductor acts has a high impedance to the output current and so all the current couples into the spectrum analyzer (SA). As in simulation, we swept the drive and measured the fundamental current for the same set of biases. Figure 4.24 shows the resulting plot which is in a great deal of agreement with the simulation results. Here again, we confirm that a class B 300µA bias yields the best linearity in the class C PA.

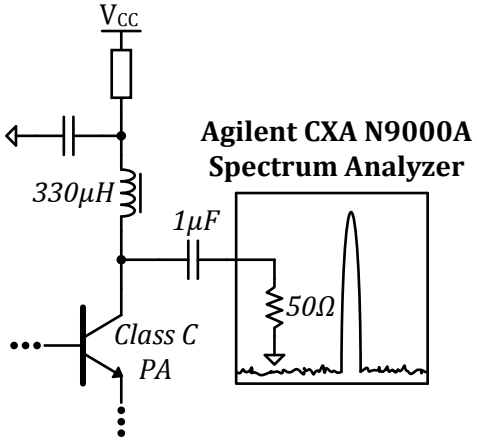

Figure 4.23 Initial test setup for measuring the output current of the class C PA.

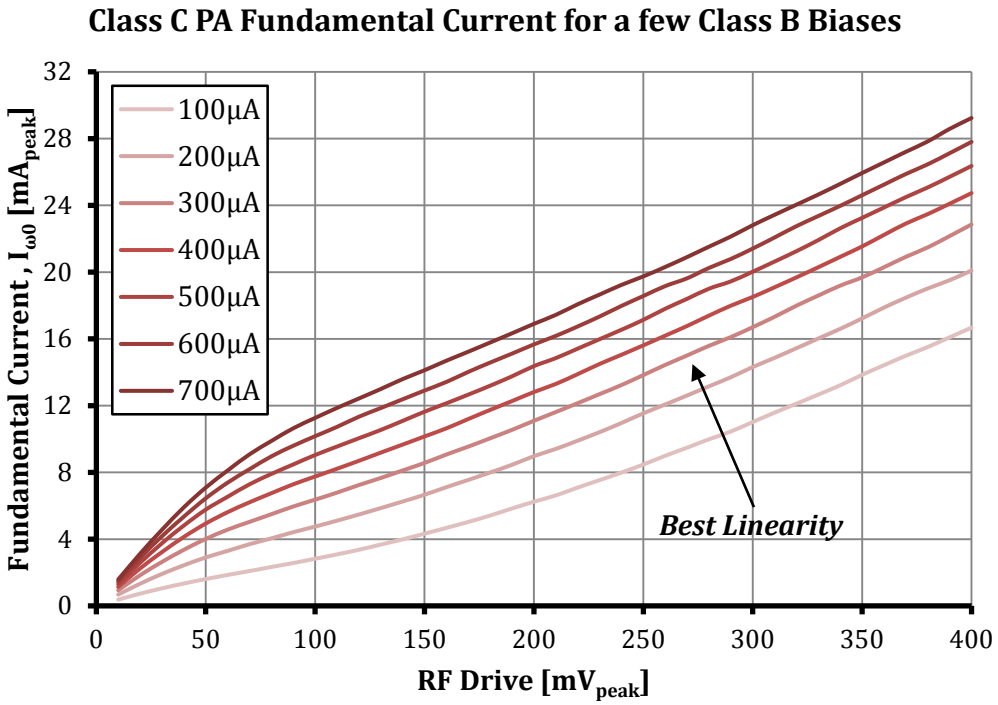

Figure 4.24 Sweep of the fundamental class C PA current for various biases.

As we did in simulation, we found the adapted bias of the class C PA for the RF drive of 400mV_{peak} (about 0.552V). We then removed the feedback and directly biased (via the class C base choke) the class C PA at this fixed value. Observing Figure 3.14, we see a result that closely resembles the simulation in Chapter 3.

An additional set of data was taken measuring the harmonic content for a range of RF drives. The plot of this data (Figure 4.26) shows how second harmonic is quite strong as predicted by the analysis in Chapter 2. From the figure, we see that harmonics above the 3rd harmonic are relatively weak.

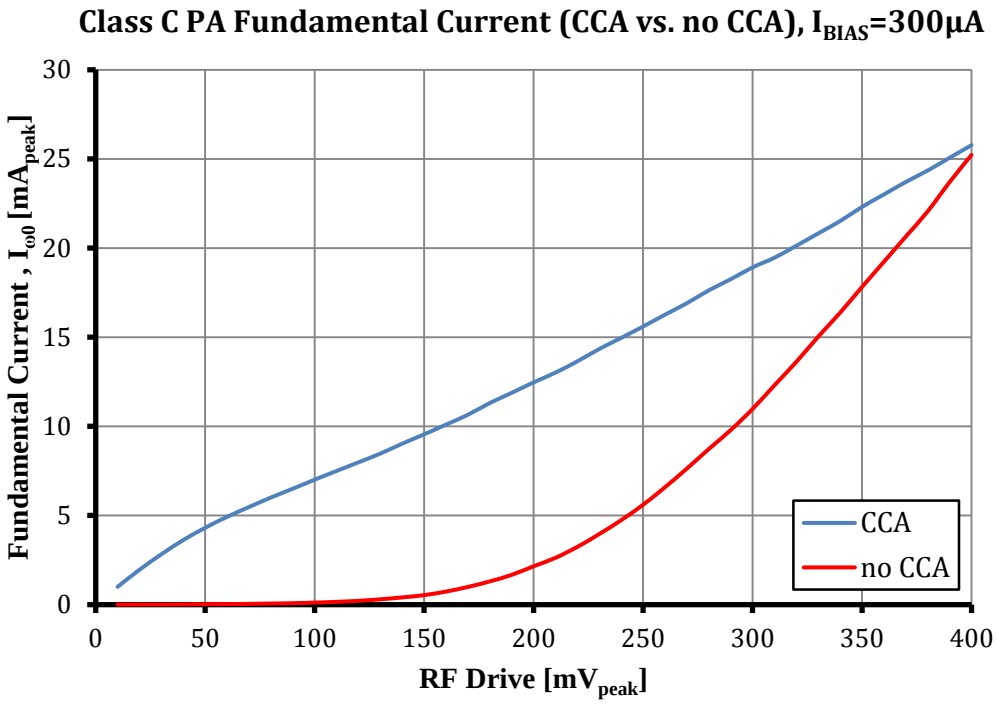

Figure 4.25 Comparison of CCA biasing vs. no CCA biasing; I_{BIAS}=300µA.

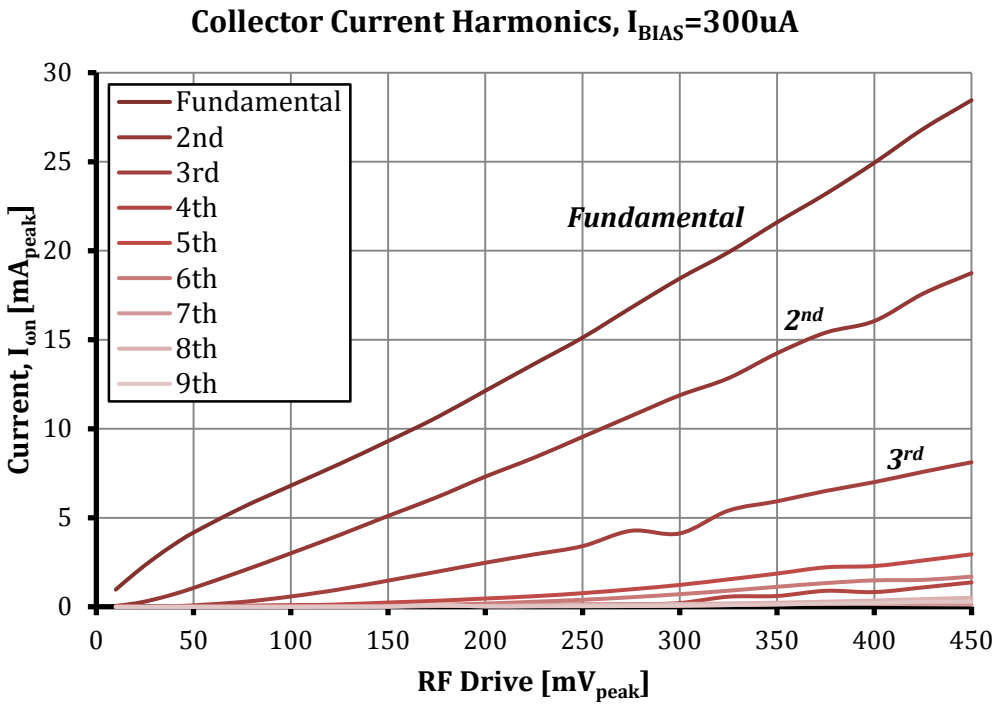

Figure 4.26 Sweep of the harmonic current of the class C PA; I_{BIAS}=300µA.

4.3.2 Stability

In an initial test of the stability, we began by terminating the amplifier in 50Ω at the input (see Figure 4.27). The output automatically "terminated" in 50Ω as it was connected to the SA. Powering the PA on and biasing the class B sensor at 300μA, we then observed the spectrum on the SA. As seen in Figure 4.28, there is a small amount of energy around 462kHz. This may be caused by noise in the control loop that is amplified to the output by the PA. However, when the system is active with an input signal, the noise floor rises and masks this energy (see Figure 4.29). In any case, this energy does not have an impact on the performance of the system.

In Chapter 3, we emphasized the importance of the compensation pole. In order see impact of the compensation pole, we intentionally removed the compensation pole from the prototype[49] and observed the output. The resulting spectrum, shown in Figure 4.30, clearly shows instability. There is considerable power spread in the spectrum. This proves the necessity of the compensation pole in the CCA biasing circuit that was built.

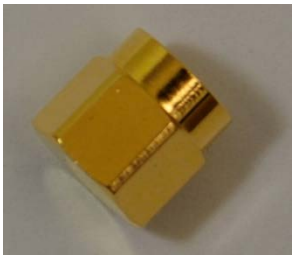

Figure 4.27 SMA Male 50Ω termination.

[49] The supply voltage was lowered so the circuit would not be damaged if the circuit became unstable.

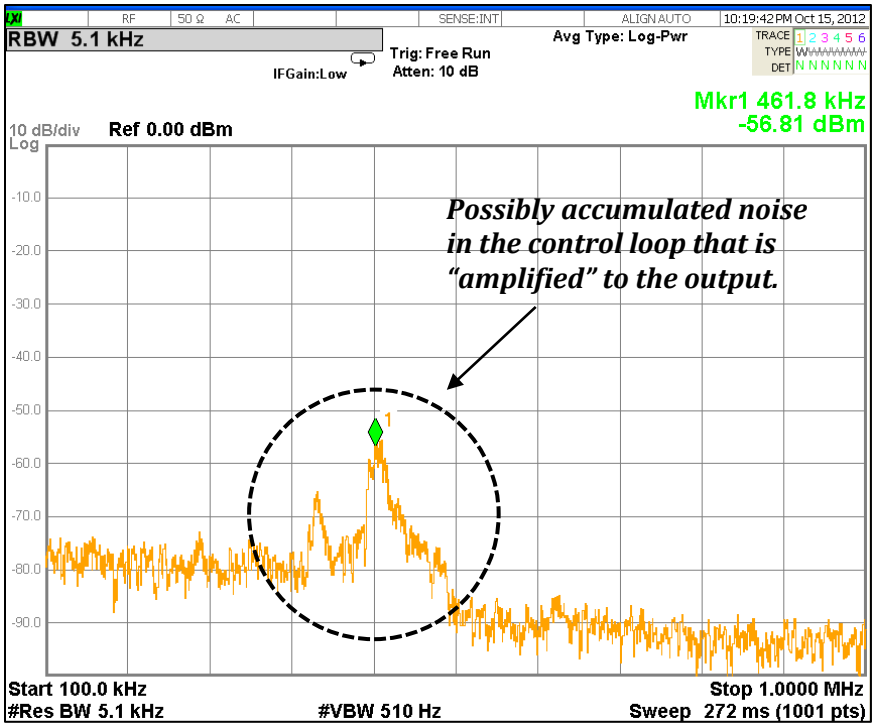

Figure 4.28 Spectrum at the output of the class C PA with the input terminated; I_{BIAS}=300μA.

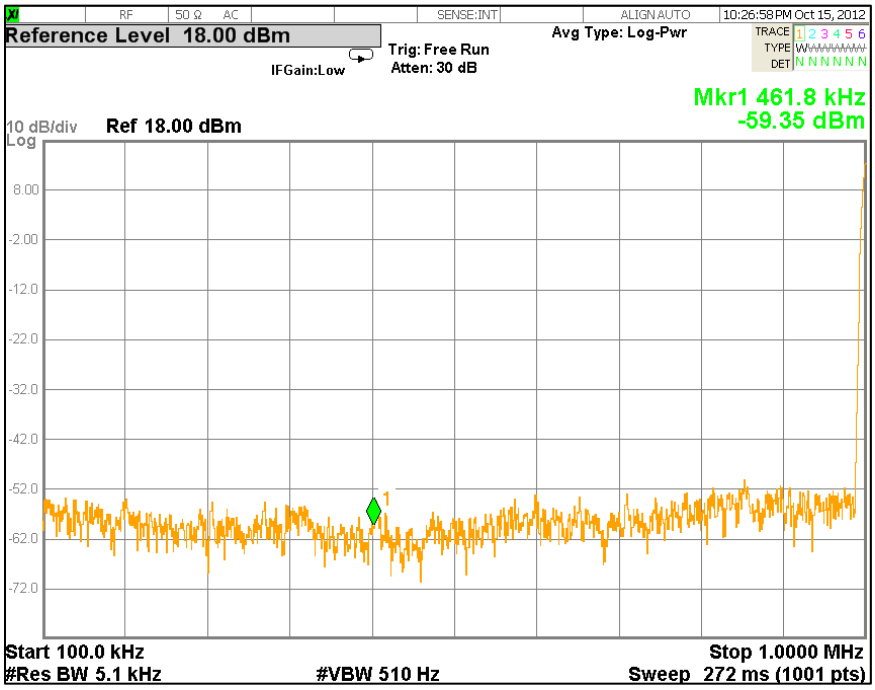

Figure 4.29 Spectrum at the output of the class C PA with an input of 400mV$_{peak}$; I_{BIAS}=300μA.

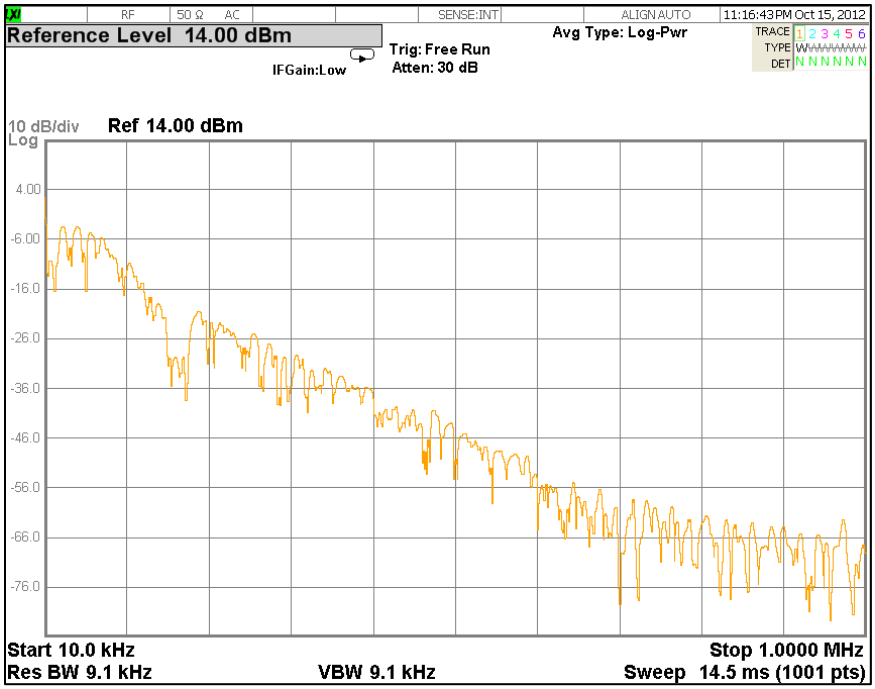

Figure 4.30 Spectrum at the output of the class C PA with the input terminated and no compensation pole in the feedback, I_{BIAS}=300μA.

As a final test of the stability of the system, we used the burst capability of the Rigol DG1022 function generator. In this mode, a signal is output to the circuit at intervals. Essentially, the RF signal turns on for an interval and then turns off for an interval[50]. This test not only tests if the loop is stable but how well it can respond. From Figure 4.31, we see there is an initial ripple and the loop tries to adjust the bias. Observing the time divisions, the loop takes about 200-300μs to reach a steady state value. Figure 4.32 shows the response of the loop to the signal turning off. The circuit responds quicker[51] and takes about 80-100μs.

[50] The effective signal is similar to an amplitude shift keying (ASK) signal.
[51] Note that for this figure the divisions are in 20μs steps.

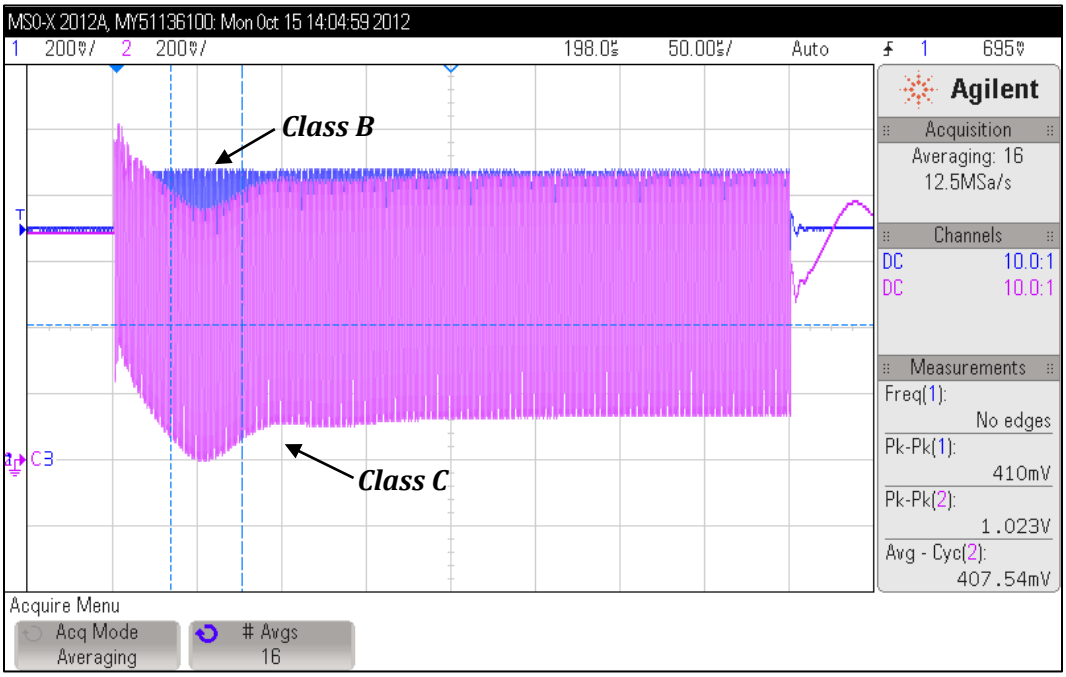

Figure 4.31 Step input of the RF signal and loop response.

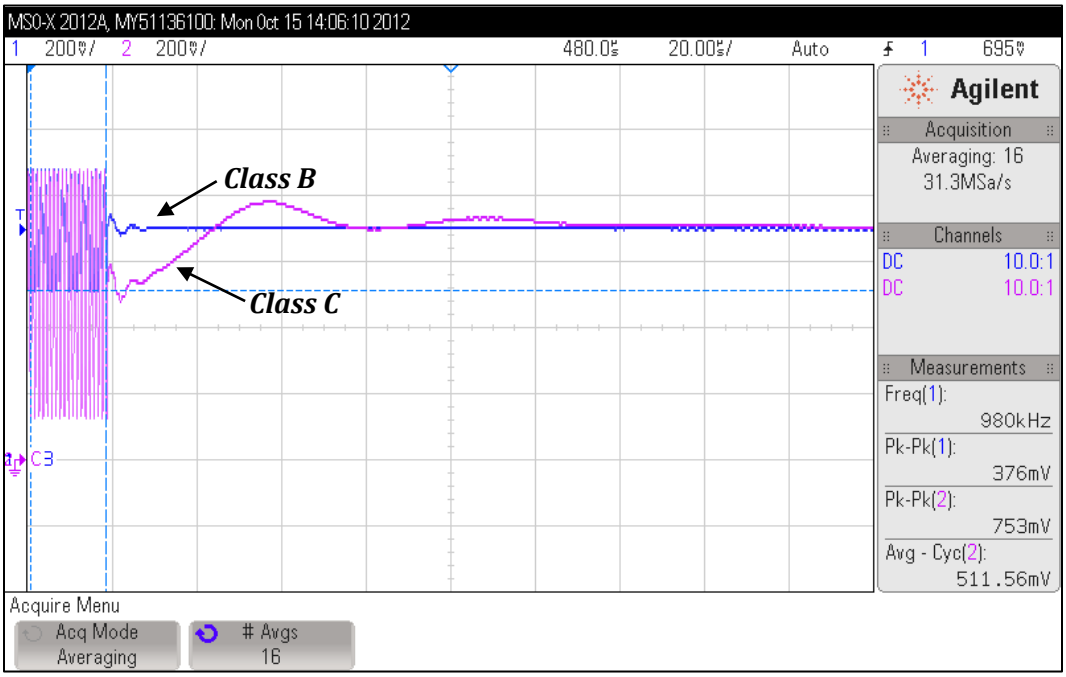

Figure 4.32 Loop response after the signal is suddenly turned off.

4.3.3 Constant Conduction Angle & Time Domain Waveforms

In this section we present several laboratory data that support the results seen in simulation in Chapter 3. The data is taken for a class B bias of 300μA unless otherwise specified. First, observe that Figure 4.33 shows correct operation of the CCA biasing circuit as the peak voltages of the inputs to the class B and C devices reach the same point at the same time. Also, as required for a conduction angle of 120°, the class C device is driven twice has hard as the class B device. Figure 4.34 shows how the DC bias of the class C PA decreases linearly with drive. This is consistent with the simulation and theory.

In order to view the shape of the current waveform and to see if the conduction angle stays constant with drive, we initially placed a 50Ω resistor[52] in the output of the class C PA as shown in Figure 4.35. We then probed the "cascaded" collector of the class C PA and the supply voltage. Using the math function on the scope, we subtracted the collector voltage from the supply voltage to obtain the voltage drop across the resistor and thus a scaled waveform of the current[53]. As seen in Figure 4.36, the conduction angle is held significantly constant. Also apparent from the figure is that for very small drives the current conducts over the whole period of the signal due to the soft knee of the transistor.

Finally, with output network of Figure 4.15a integrated to the class C PA output, Figure 4.37 shows the class C PA base and collector voltage waveforms for a large drive. Figure 4.38 shows the class C PA collector and output voltage waveforms for the same drive. From the figures, we observe that the harmonic tank does a good job in filtering the harmonics.

[52] Chosen such that the voltage drop was not large enough to bring the PA into saturation.
[53] Recall, from elementary circuit analysis that the current through and voltage across a resistor are in phase.

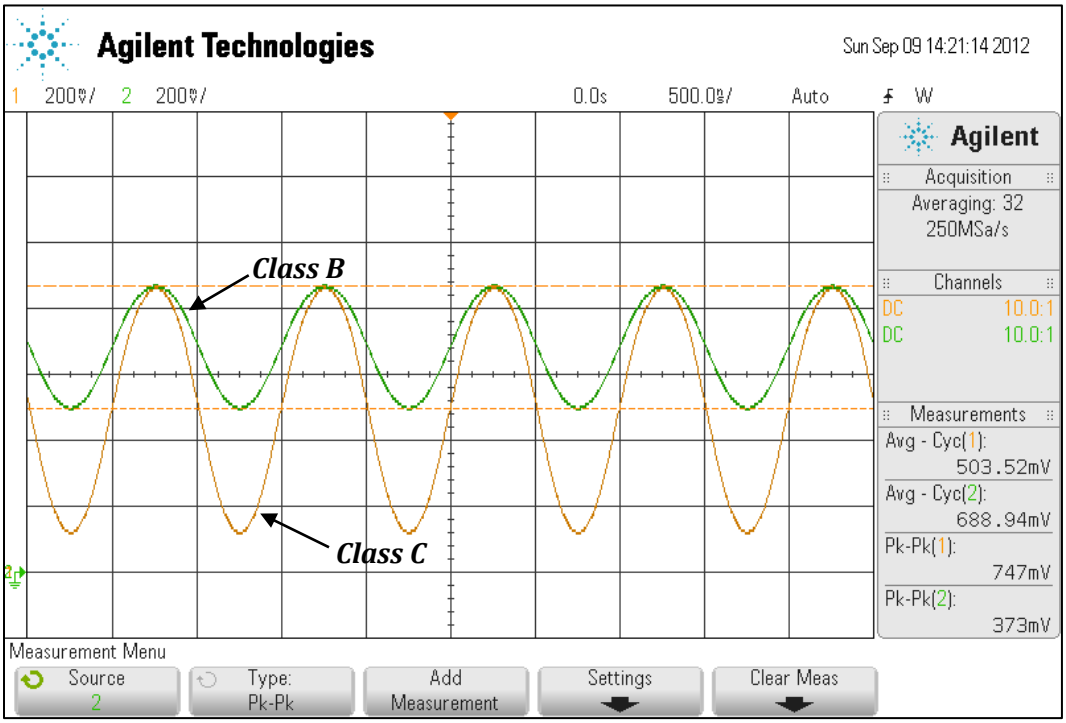

Figure 4.33 Equal peak excursions of class B and C devices; V_{RFin}=400mV_{peak}.

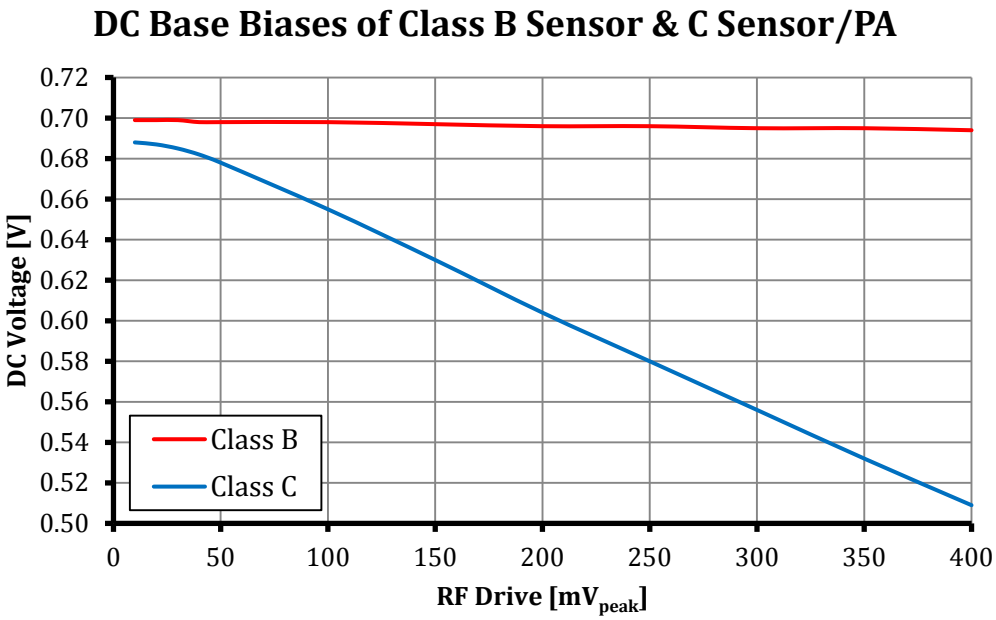

Figure 4.34 The DC base bias of the class C PA and the class B sensor.

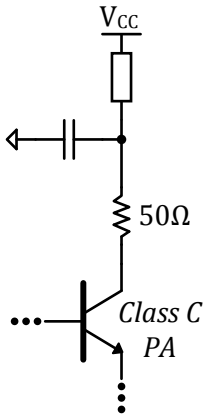

Figure 4.35 Circuit implementation to sample the output current of the class C PA.

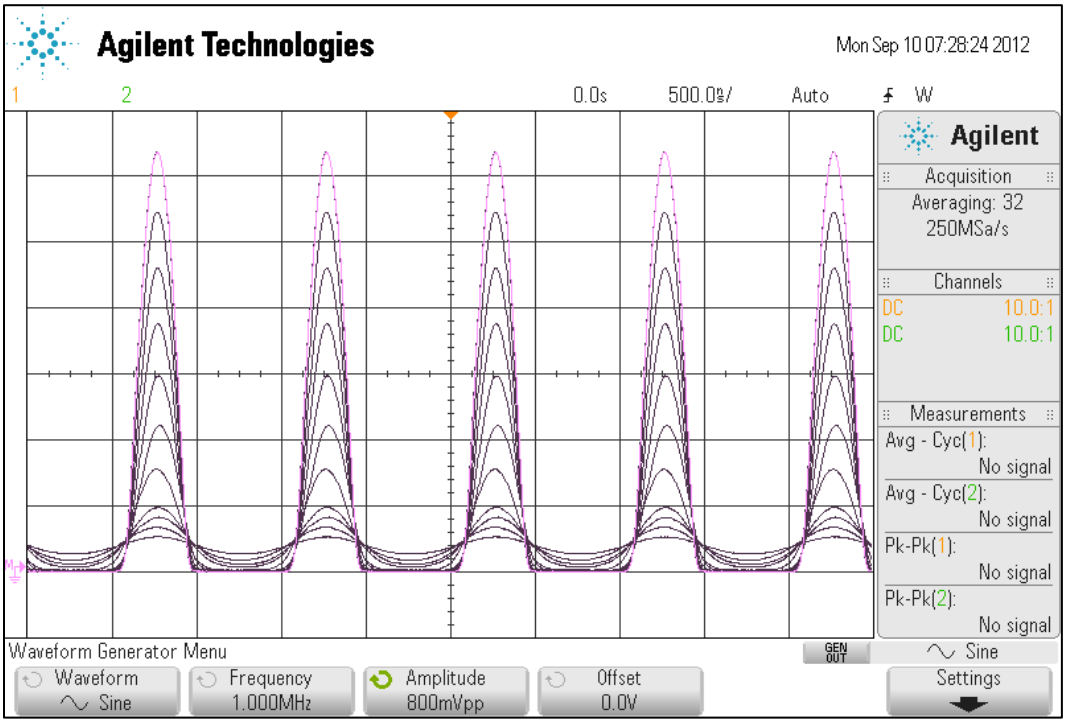

Figure 4.36 Constant conduction angle of the class C PA.

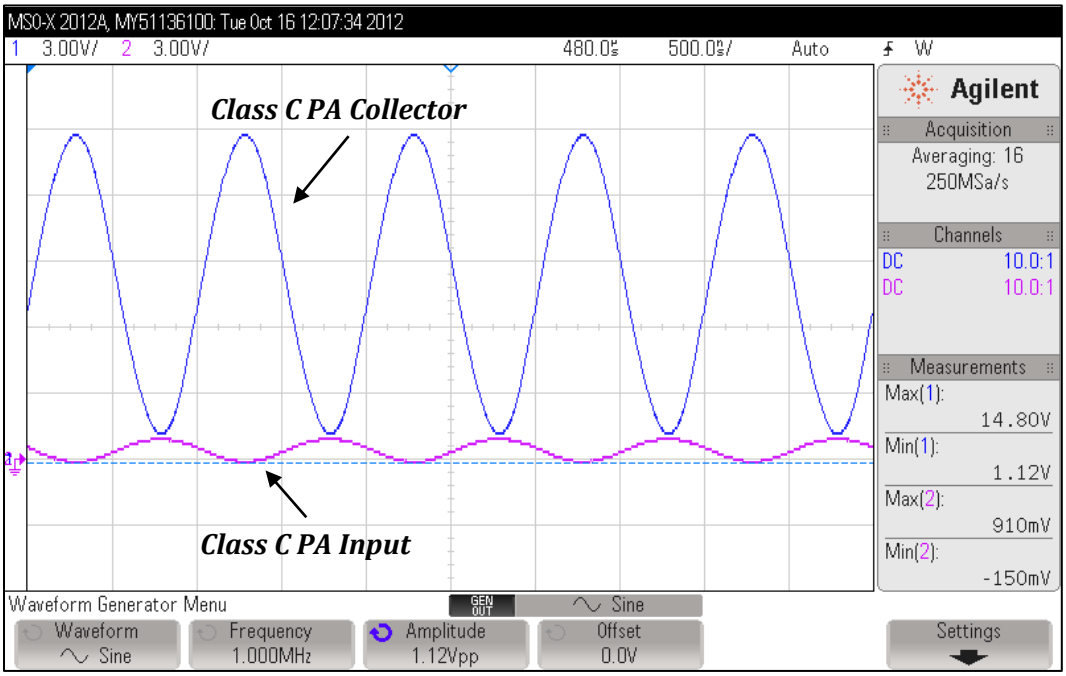

Figure 4.37 Class C PA base and collector voltages; V_{RFin}=560mV_{peak}

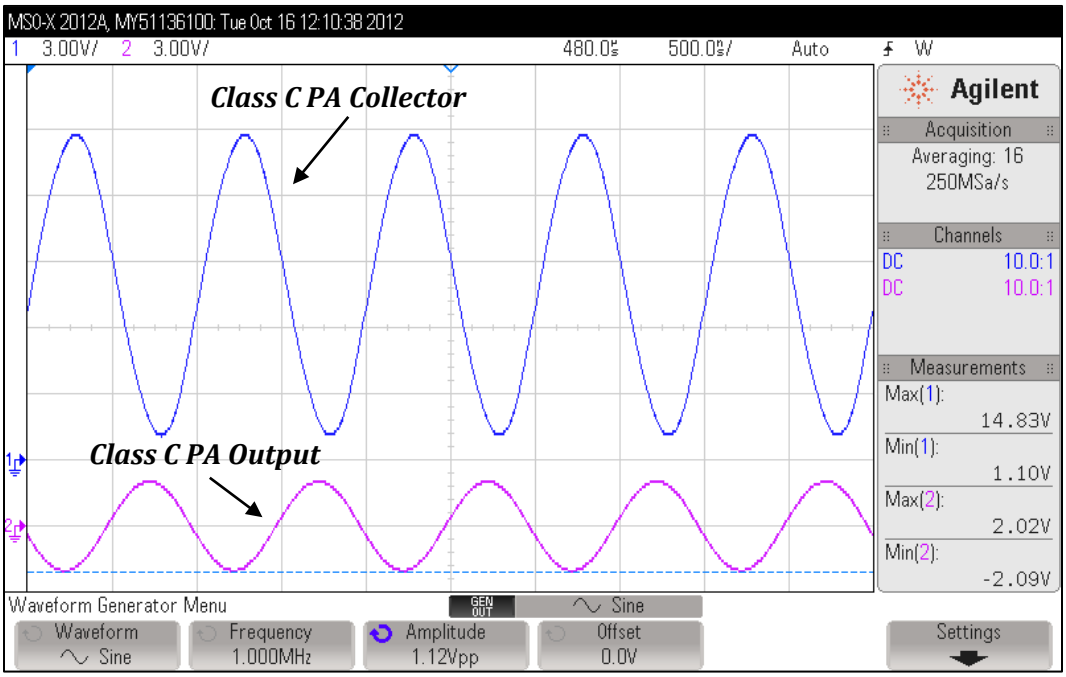

Figure 4.38 Class C PA base and output voltage; V_{RFin}=560mV_{peak}

4.3.4 IMD Testing

To perform IMD measurements, we performed a two-tone test as discussed in Chapter 3. To combine the tones, initially a 6dB[54] resistive power combiner (Figure 4.39) was made on a copper top board. This board was used in the two-tone testing of the initial prototype. In the two-tone testing of the final PCB prototype, the ZFSC-2-6+ zero degree, 3dB power combiner (Figure 4.40) was used. Figures 4.41 and 4.42 show the spectral performance of these combiners. The clear advantage of "inductive" combiner is its isolation[55] of the input ports - about 37dB at 1MHz as specified in the datasheet.

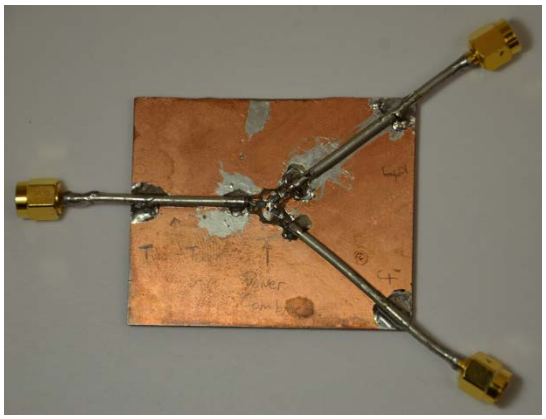

Figure 4.39 The 6dB resistive power combiner.

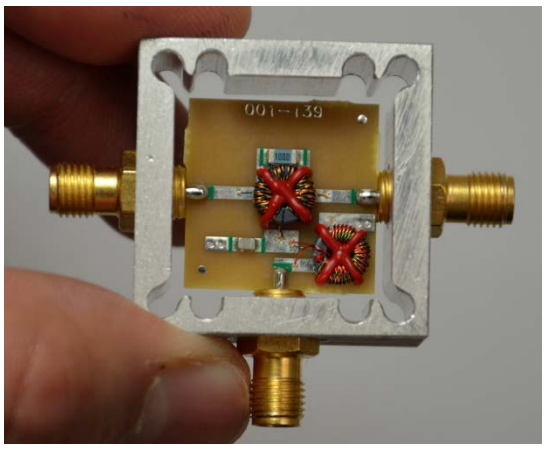

Figure 4.40 The ZFSC-2-6+ zero degree, 3dB power combiner

[54] This "6dB" indicates the power loss in each tone.
[55] The isolation of a resistive combiner is equal to its insertion loss and is thus 6dB.

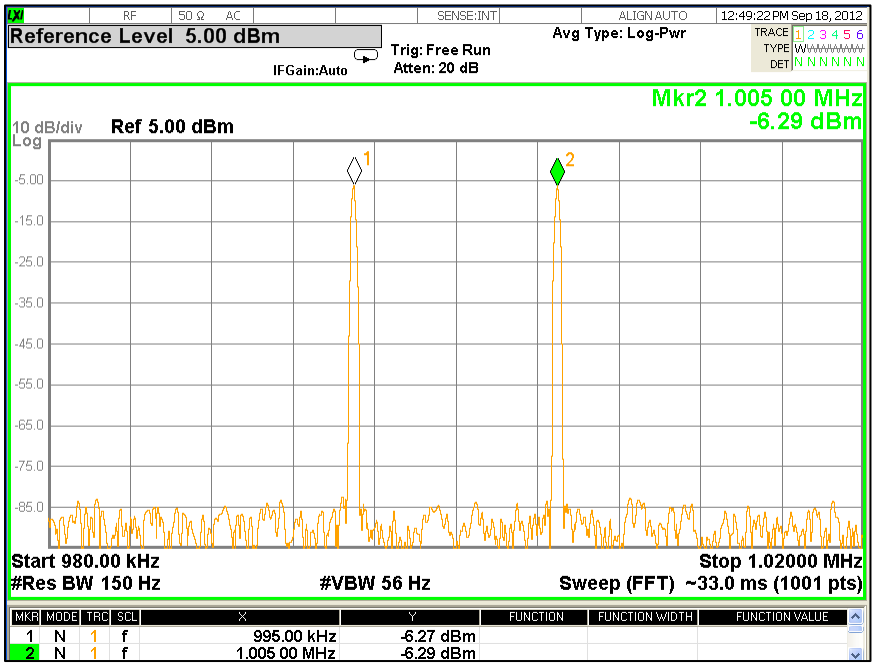

Figure 4.41 Output of the 6dB resistive power combiner for two tone inputs at 0dBm each; f_1=0.98MHz & f_2=1.02MHz.

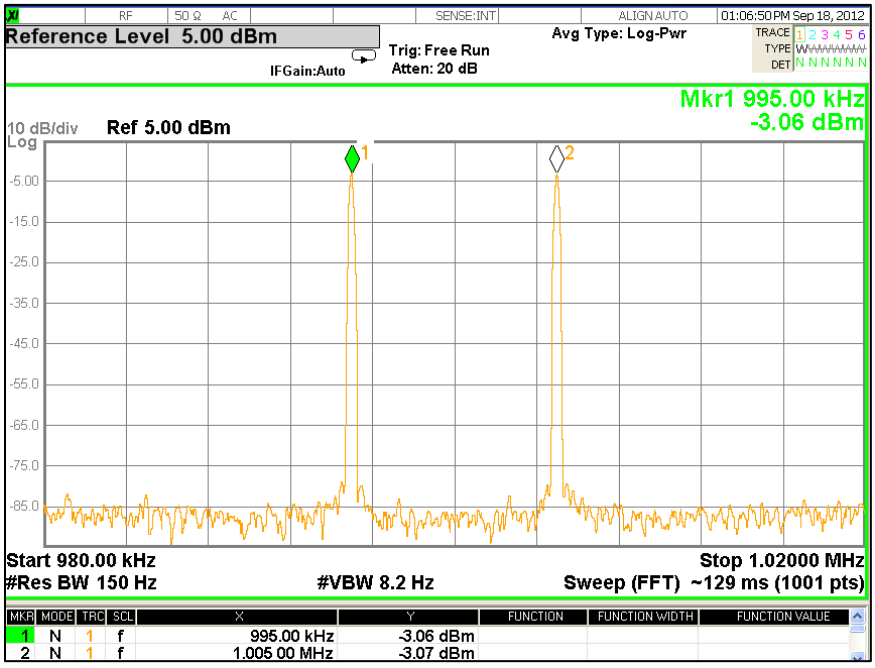

Figure 4.42 Output of the ZFSC-2-6+ zero degree, 3dB power combiner for two tones input at 0dBm each; f_1=0.98MHz & f_2=1.02MHz.

The two-tone tests that follow were performed with the output stage integrated. Figure 3.23 shows IMD_3 measurements, for a tone spacing of 500Hz, taken at two class B biases – 300 and 700μA. The 300μA bias IMD_3 response shows lower IMD_3. This is consistent with the simulation in Chapter 3. However, apparent in the figure, we see the IP_3 products are slightly asymmetrical in magnitude. This is a "memory effect" that may be caused by phase error in the loop[56].

As in the Chapter 3 simulation, we held the bias constant at 300μA and took measurements of the IMD_3 for a few tone separations (see Figure 3.24). The IMD_3 characteristics seen in the resulting plot are consistent with the simulation and theory – if the bandwidth of a signal is larger than the loop bandwidth, the control loop will not be able to effectively follow the envelope and thus IMD_3 will significantly increase.

Figures 4.45 to 4.47 show the spectrum of the class C PA output when two tones are input[57] at $300mV_{peak}$ for tone spacings of 500Hz, 5kHz, and 10kHz, respectively. For a tone spacing of 500Hz, we see the asymmetry of the IP_3 products due to the aforementioned "memory effects." In addition to the IP_3 products, we see all of the other intermodulation products, which taper off in magnitude.

[56] This is caused by the system not being fast enough to follow the envelope of input signal.
[57] To the combiner, that is.

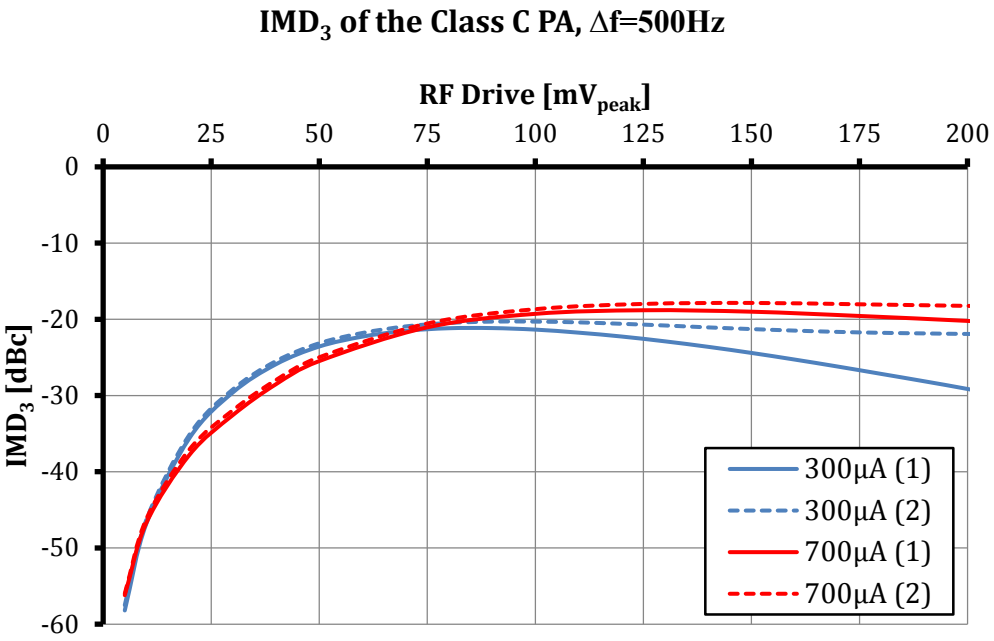

Figure 4.43 IMD_3 of the class C PA; Δf=500Hz, I_{BIAS}=300µA, 700 µA.

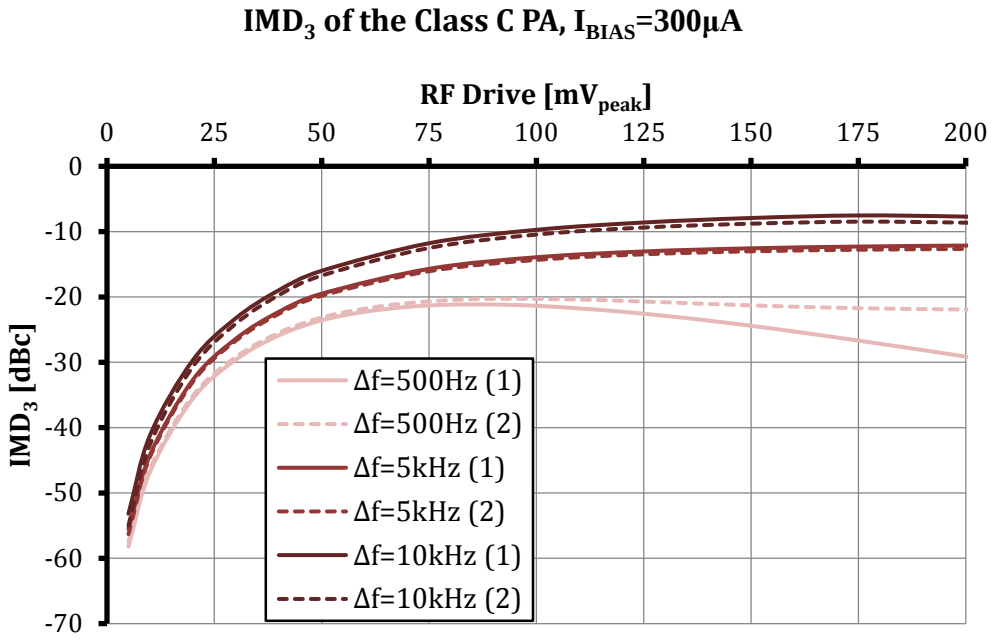

Figure 4.44 IMD_3 of the class C PA for various tone separations; I_{BIAS}=300µA.

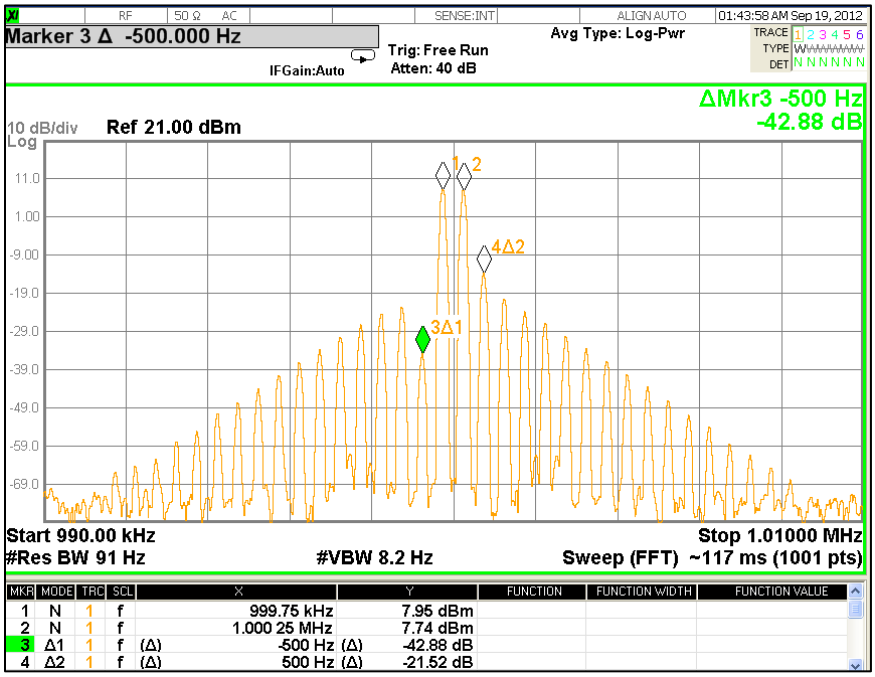

Figure 4.45 Class C PA IMD spectrum, Δf=500Hz; I_{BIAS}=300µA, V_{tone}=300mV_{peak}.

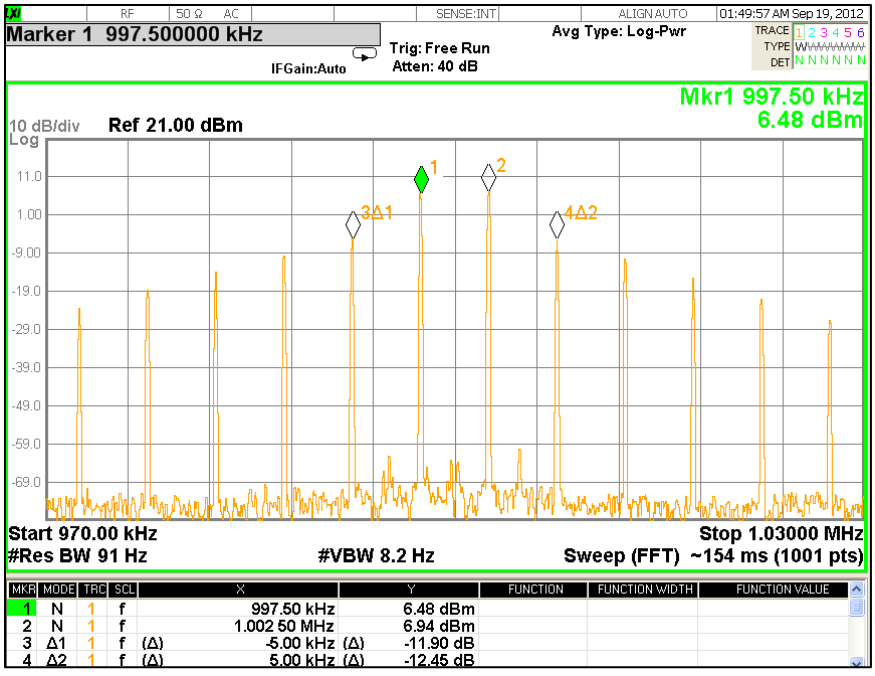

Figure 4.46 Class C PA IMD spectrum, Δf=5kHz; I_{BIAS}=300µA, V_{tone}=300mV_{peak}.

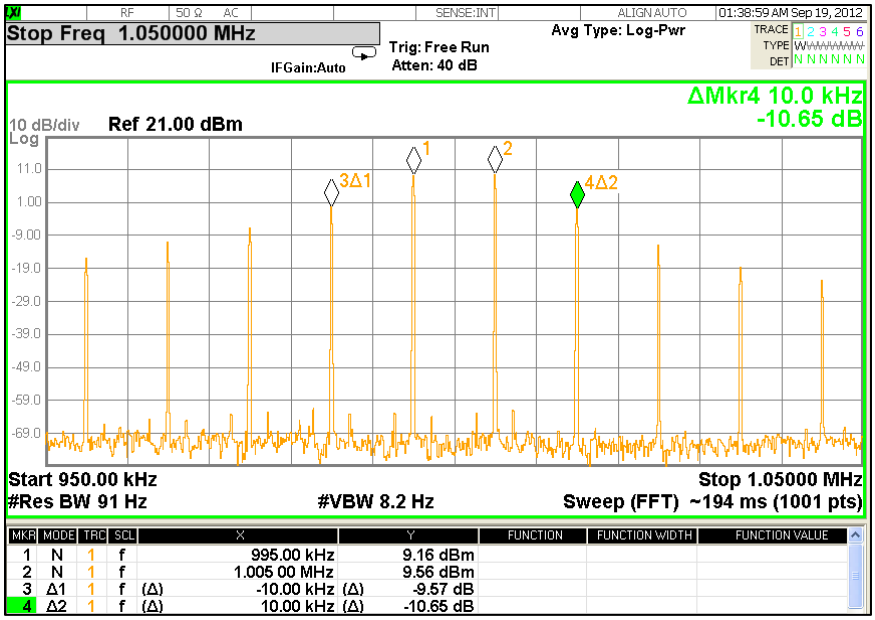

Figure 4.47 Class C PA IMD spectrum; Δf=10kHz, I_{BIAS}=300μA, V_{tone}=300mV_{peak}.

4.3.5 Effect of the Impedance Mismatch & Losses on the Class C PA Efficiency

In regards to the output network that was built and tuned, we were unable to match from 50 to 270Ω, but achieved a match to about 215Ω. This is most probably due to the Q of the inductors used in addition to not being able to tune the capacitors. The mismatch and the lossy nature of the practical inductors used led to lower power efficiency than observed in simulation. Figure 4.48 shows the DC-to-RF power efficiency simulated in ADS and measured in the lab. The ADS simulation utilized the output network of Figure 4.15a.

In an IC implementation, we could design a much more accurate output network. Nevertheless, the ADS simulation shows the possibility of a highly efficient RF PA.

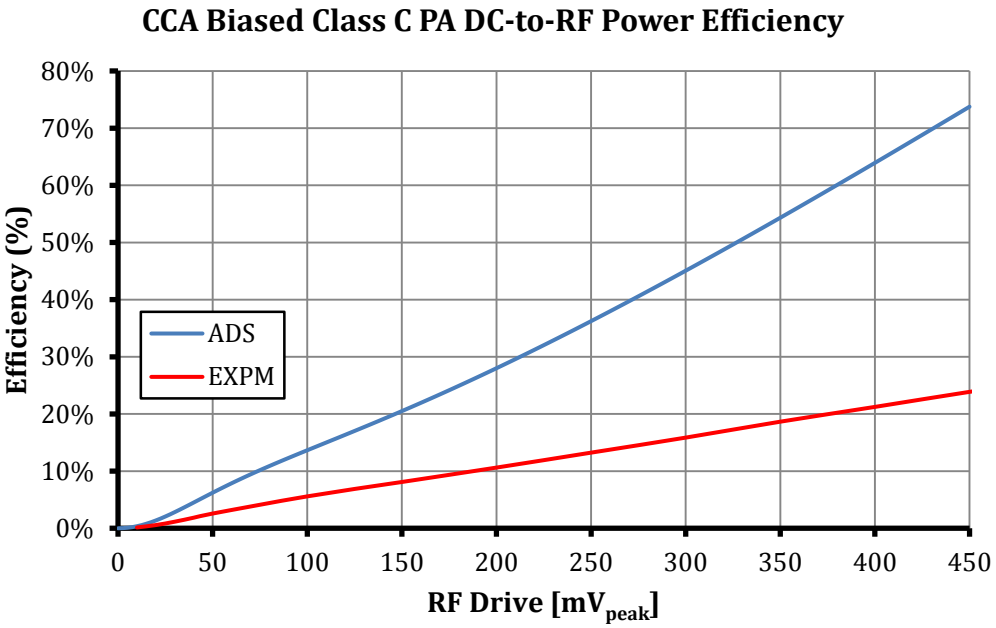

Figure 4.48 DC-to-RF efficiency of the CCA biased class C PA.

5

Conclusion & Future Prospects

The CCA biasing idea was first researched and worked on in 2010 by Greg LaCaille working alongside Professor Prodanov. In his work, LaCaille showed the relationship of the fundamental and DC drain currents to the input signal drive and conduction angle. This relationship led to the conclusion that if the conduction angle is held constant, the fundamental and DC currents will linearly depend on the signal drive. In addition, an ideal class B device has a constant conduction angle and thus the fundamental and DC currents of it also linearly depend on the signal drive. This led to the idea of using two scaled replica devices[58] of the actual "power device". Each device is driven by the same drive and the "DC" currents of the devices are sensed and forced in a certain ratio by virtue of the feedback. As a consequence of the feedback, the base bias of the class C "power device" is set. A fundamental problem, however, existed with this approach – the class C PA was underutilized. It could never achieve its maximum potential current since the class B device would reach the saturation point of the I-V curve first.

[58] One device biased in class B and the other biased at the same point as the power device.

In 2011, Stephan Garber was the second individual to work with Professor Prodanov on CCA biasing idea. He showed that the conduction angle could be kept constant by equal RF drive and unequal DC current ratio-ing, unequal RF drive[59] and equal DC current ratio-ing, or unequal RF drive and unequal DC current ratio-ing. Additionally, he simplified the control loop. Although the class C PA was able to be driven "harder" with the unequal RF drive and equal DC current ratio-ing method, it still couldn't be driven to produce its maximum output current. Finally, in terms of a practical implementation, Michael Spahn built a prototype based on Garber's work. When testing the prototype, he noticed some evidence of instability.

The work presented in this paper served to address the aforementioned issues. An optimum hybrid control was proposed. This optimum control allowed for the class C PA to exercise the full extent of the "hockey-stick" I-V curve – a significant improvement over previous iterations of the CCA biasing idea. Secondly, the coupling and drive strategy was improved. The class C sensor was "embedded" as a "finger" of the class C PA and shared the same base voltage as the other "fingers". The class B sensor was driven by a transformer via the class C base-biasing choke. Additionally, an accurate open-loop model of the control loop was developed. To test the validity of the design, a robust prototype was developed and tested. The prototype results showed strong correlation with simulation and ultimately gave merit to the CCA biasing topology.

The next step in the evolution of the CCA biasing circuit is to implement the topology in a single IC at the intended cellular frequency. In the implementation, the non-inverting op-amp should be replaced with an operational transconductance amplifier (OTA) as opposed to a "full-blown" op-amp. An OTA is much faster as it is not burdened by the extra stages of a conventional op-amp.

[59] We drive the class C device "harder" than the class B device.

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Appendix A
Harmonic Drain Current Expressions

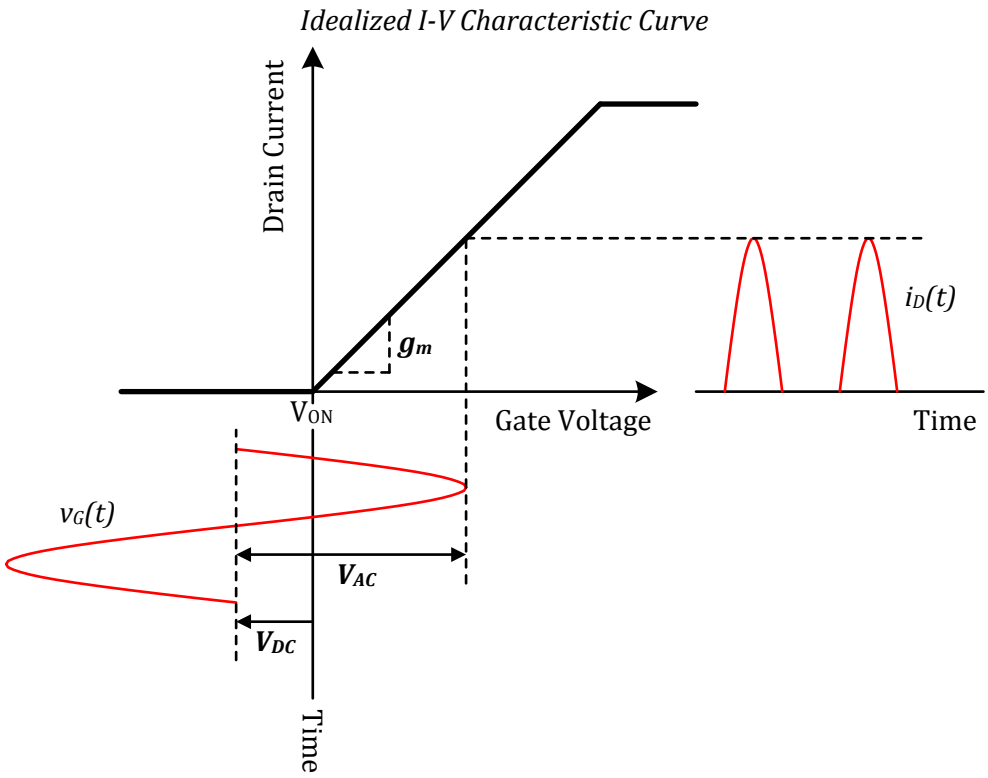

Figure A.1 Voltage-to-current conversion of an ideal transistor.

Considering an ideal transistor amplifier with the I-V characteristic shown in Figure A.1 we write the drain current as follows:

$$i_D(t) = \begin{cases} 0, & v_G(t) \le 0 \\ g_m v_G(t), & v_G(t) > 0 \end{cases} \tag{A.1}$$

Note that V_{ON}, in the figure, represents the voltage that defines the knee of a real transistor[60]. We set this to zero to simplify the analysis[61]. From (A.1), we write the input sinusoid[62]:

$$v_G(t) = V_{AC}\cos(\omega t) + V_{DC} \tag{A.2}$$

The conduction angle (θ) defines the portion of the input sinusoid that the transistor conducts current.

$$\theta\ [rad] \stackrel{\text{def}}{=} 2\pi \cdot \frac{t_{on}}{T} \tag{A.3}$$

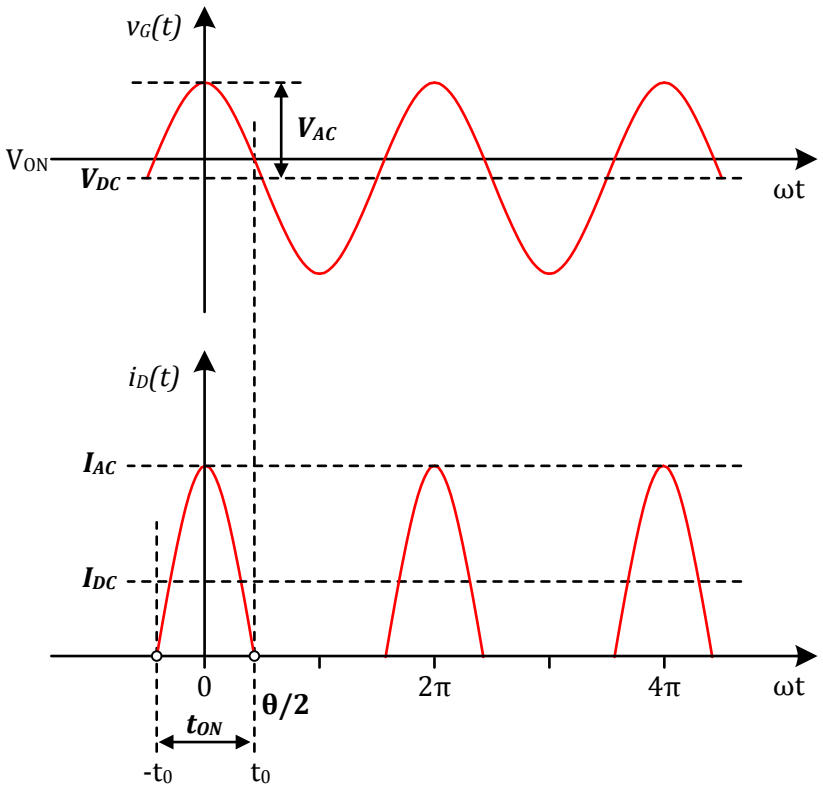

Figure A.2 Relationship between drain current and gate voltage.

[60] As in the case with silicon BJTs, the "turn-on" voltage is typically ~0.7V.
[61] To account for this quantity simply add this term to the quantity "V_{DC}".
[62] We use the cosine function to describe the input waveform, due its symmetry about zero on the time axis.

Using (A.2), (A.3), and Figure A.2, we find relationship between the conduction angle and DC-to-AC ratio:

$$t_{ON} = 2t_0$$

$$v_G(t_0) = V_{AC}\cos(\omega t_0) + V_{DC}$$

At time instance, t_0, the gate voltage is zero. Thus we have:

$$V_{AC}\cos(\omega t_0) + V_{DC} = 0$$

$$t_0 = \frac{\cos^{-1}\left(-\frac{V_{DC}}{V_{AC}}\right)}{\omega} = \frac{\pi - \cos^{-1}\left(\frac{V_{DC}}{V_{AC}}\right)}{\omega}$$

Finally, we write the conduction angle:

$$\theta = \frac{t_{on}}{T}[rad] = \frac{2\dfrac{\pi - \cos^{-1}\left(\frac{V_{DC}}{V_{AC}}\right)}{\omega}}{\dfrac{1}{\omega}} = 2\left[\pi - \cos^{-1}\left(\frac{V_{DC}}{V_{AC}}\right)\right] \tag{A.4}$$

Take care to note that DC voltage is taken as a negative quantity in the above expression.

Using (A.1), (A.2), and Figure A.2, we can write the following:

$$i_D(t) = g_m V_{AC}\cos(\omega t) + g_m V_{DC}$$

where,

$$\underline{I_{AC} = g_m V_{AC}} \text{ and } \underline{I_{DC} = g_m V_{DC}}$$

We can also write the DC-to-AC ratio in terms of the conduction angle:

$$\frac{V_{DC}}{V_{AC}} = -\cos\left(\frac{\theta}{2}\right) \tag{A.5}$$

To determine the harmonic content of the drain current, we first write an expression for the drain current using, (A.1) , (A.2), and (A.5).

$$\begin{aligned} i_D(t) &= g_m v_G(t) \\ &= g_m[V_{AC}\cos(\omega t) + V_{DC}] \\ &= g_m\left[V_{AC}\cos(\omega t) - V_{AC}\cos\left(\frac{\theta}{2}\right)\right] \end{aligned}$$

Letting $x = \omega t$, to simplify analysis, we have:

$$i_D(x) = g_m V_{AC}\left[\cos(x) - \cos\left(\frac{\theta}{2}\right)\right] \tag{A.6}$$

Next, we need to take the Fourier series of the expression in (A.6). Note that the conduction period is defined by the interval, $x \in \left(-\frac{\theta}{2}, \frac{\theta}{2}\right)$.

Solving for the DC term:

$$I_{DC} = \frac{1}{T}\int_T i_D(x)\,dx$$

$$= \frac{1}{2\pi}\int_{-\theta/2}^{\theta/2} g_m V_{AC}\left[\cos(x) - \cos\left(\frac{\theta}{2}\right)\right] dx$$

$$= \frac{g_m V_{AC}}{2\pi}\int_{-\theta/2}^{\theta/2}\left[\cos(x) - \cos\left(\frac{\theta}{2}\right)\right] dx$$

$$= \frac{g_m V_{AC}}{2\pi}\left[\sin(x) - x\cos\left(\frac{\theta}{2}\right)\right]\Big|_{-\frac{\theta}{2}}^{\frac{\theta}{2}}$$

$$= \frac{g_m V_{AC}}{2\pi}\left\{\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right] - \left[\sin\left(-\frac{\theta}{2}\right) - \left(-\frac{\theta}{2}\right)\cos\left(\frac{\theta}{2}\right)\right]\right\}$$

$$= \frac{g_m V_{AC}}{2\pi}\left[2\sin\left(\frac{\theta}{2}\right) - \theta\cos\left(\frac{\theta}{2}\right)\right]$$

$$I_{DC} = \frac{g_m V_{AC}}{\pi}\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right] \tag{A.7}$$

Solving for the nth harmonic term:

$$I_{n\omega_0} = \frac{2}{T}\int_T i_D(x)\cos(nx)\,dx$$

$$= \frac{2}{2\pi}\int_{-\theta/2}^{\theta/2} g_m V_{AC}\left[\cos(x) - \cos\left(\frac{\theta}{2}\right)\right]\cos(nx)\,dx$$

$$= \frac{g_m V_{AC}}{\pi}\int_{-\theta/2}^{\theta/2}\left[\cos(x)\cos(nx) - \cos\left(\frac{\theta}{2}\right)\cos(nx)\right] dx$$

$$I_{n\omega_0} = \frac{g_m V_{AC}}{\pi}\left\{\underbrace{\int_{-\theta/2}^{\theta/2}[\cos(x)\cos(nx)]\,dx}_{\#1} - \underbrace{\int_{-\theta/2}^{\theta/2}\left[\cos\left(\frac{\theta}{2}\right)\cos(nx)\right]\,dx}_{\#2}\right\} \qquad \text{(A.8)}$$

To simplify the analysis, we solve for the #1 and #2 individually.

Solving for #1[63]:

$$\begin{aligned}\int_{-\theta/2}^{\theta/2}[\cos(x)\cos(nx)]\,dx &= \frac{1}{2}\int_{-\theta/2}^{\theta/2}\{\cos[x(1-n)]+\cos[x(1+n)]\}dx \\ &= \frac{1}{2}\int_{-\theta/2}^{\theta/2}\{\cos[x(n-1)]+\cos[x(n+1)]\}dx \\ &= \frac{1}{2}\left\{\frac{1}{n-1}\sin[x(n-1)]+\frac{1}{n+1}\sin[x(n+1)]\right\}\Big|_{-\frac{\theta}{2}}^{\frac{\theta}{2}}\end{aligned}$$

$$\int_{-\theta/2}^{\theta/2}[\cos(x)\cos(nx)]\,dx = \frac{1}{n-1}\sin\left[\frac{(n-1)\theta}{2}\right]+\frac{1}{n+1}\sin\left[\frac{(n+1)\theta}{2}\right] \qquad \text{(\#1)}$$

Solving for #2:

$$\begin{aligned}\int_{-\theta/2}^{\theta/2}\left[\cos\left(\frac{\theta}{2}\right)\cos(nx)\right]\,dx &= \cos\left(\frac{\theta}{2}\right)\int_{-\theta/2}^{\theta/2}\cos(nx)\,dx \\ &= \cos\left(\frac{\theta}{2}\right)\frac{\sin(nx)}{n}\Big|_{-\frac{\theta}{2}}^{\frac{\theta}{2}} \\ &= \frac{2}{n}\cos\left(\frac{\theta}{2}\right)\sin\left(n\frac{\theta}{2}\right)\end{aligned}$$

Simplifying[64]:

$$\frac{2}{n}\cos\left(\frac{\theta}{2}\right)\sin\left(n\frac{\theta}{2}\right) = \frac{2}{n}\cdot\frac{1}{2}\left\{\sin\left(\frac{\theta}{2}+n\frac{\theta}{2}\right)-\sin\left(\frac{\theta}{2}-n\frac{\theta}{2}\right)\right\}$$

[63] We use the Trig. Identity: $\cos A\cos B = \frac{1}{2}[\cos(A-B)+\cos(A+B)]$.

[64] Here we use the Trig. Identity: $\cos A\sin B = \frac{1}{2}[\sin(A+B)-\sin(A-B)]$.

$$\int_{-\theta/2}^{\theta/2}\left[\cos\left(\frac{\theta}{2}\right)\cos(nx)\right]\,dx = \frac{1}{n}\left\{\sin\left[\frac{(n+1)\theta}{2}\right]+\sin\left[\frac{(n-1)\theta}{2}\right]\right\} \quad (\#2)$$

Substituting #1 and #2 in (A.8), we have:

$$I_{n\omega_0} = \frac{g_m V_{AC}}{\pi}\left\{\frac{1}{n-1}\sin\left[\frac{(n-1)\theta}{2}\right]+\frac{1}{n+1}\sin\left[\frac{(n+1)\theta}{2}\right] - \frac{1}{n}\sin\left[\frac{(n+1)\theta}{2}\right]-\frac{1}{n}\sin\left[\frac{(n-1)\theta}{2}\right]\right\}$$

$$= \frac{g_m V_{AC}}{\pi}\left\{\left[\frac{1}{n-1}-\frac{1}{n}\right]\sin\left[\frac{(n-1)\theta}{2}\right]+\left[\frac{1}{n+1}-\frac{1}{n}\right]\sin\left[\frac{(n+1)\theta}{2}\right]\right\}$$

$$= \frac{g_m V_{AC}}{\pi}\left\{\frac{1}{n(n-1)}\sin\left[\frac{(n-1)\theta}{2}\right]-\frac{1}{n(n+1)}\sin\left[\frac{(n+1)\theta}{2}\right]\right\}$$

$$I_{n\omega_0}\Big|_{n\geq 1} = \frac{g_m V_{AC}}{n\pi}\left\{\frac{1}{(n-1)}\sin\left[\frac{(n-1)\theta}{2}\right]-\frac{1}{(n+1)}\sin\left[\frac{(n+1)\theta}{2}\right]\right\} \quad (A.9)$$

In order solve for the fundamental component (n=1), we need to use L 'Hôspital's Rule. To use the rule, we first put (A.9) in the form a single fraction:

$$I_{n\omega_0} = \frac{g_m V_{AC}}{\pi}\left\{\frac{\sin\left[\frac{(n-1)\theta}{2}\right]}{n(n-1)}-\frac{\sin\left[\frac{(n+1)\theta}{2}\right]}{n(n+1)}\right\}$$

$$= \frac{g_m V_{AC}}{\pi}\left\{\frac{(n+1)\sin\left[\frac{(n-1)\theta}{2}\right]-(n-1)\sin\left[\frac{(n+1)\theta}{2}\right]}{n(n+1)(n-1)}\right\}$$

$$I_{n\omega_0} = \frac{g_m V_{AC}}{\pi}\left\{\frac{(n+1)\sin\left[\frac{(n-1)\theta}{2}\right]-(n-1)\sin\left[\frac{(n+1)\theta}{2}\right]}{n^3-n}\right\} \quad (A.10)$$

Now, the rule states that in order to find the case where n=1, we must take the limit as n approaches 1 of quantity that represents the derivative of the numerator divided by the derivative of the denominator. This analysis is done on the following page

$$I_{\omega_0} = \lim_{n\to 1} \frac{g_m V_{AC}}{\pi} \frac{\left\{(n+1)\sin\left[\frac{(n-1)\theta}{2}\right] - (n-1)\sin\left[\frac{(n+1)\theta}{2}\right]\right\}'}{\{n^3 - n\}'}$$

$$= \lim_{n\to 1} \frac{g_m V_{AC}}{\pi} \left\{ \frac{\sin\left[\frac{(n-1)\theta}{2}\right] + (n+1)\cos\left[\frac{(n-1)\theta}{2}\right]\frac{\theta}{2}}{3n^2 - 1} - \frac{\sin\left[\frac{(n+1)\theta}{2}\right] + (n-1)\cos\left[\frac{(n+1)\theta}{2}\right]\frac{\theta}{2}}{3n^2 - 1} \right\}$$

$$= \frac{g_m V_{AC}}{\pi}\left[\frac{\theta - \sin(\theta)}{2}\right]$$

$$I_{\omega_0} = \frac{g_m V_{AC}}{2\pi}[\theta - \sin(\theta)] \tag{A.11}$$

Thus, observing (A.7) and (A.11), the fundamental and DC components linearly relate to the RF drive (V_{AC}) if the conduction angle is held constant.

Appendix B
Effective Transconductance of a Reduced Conduction Angle Mode PA

The following analysis is used to find the effective transconductance (G_{Meff}) of a transistor operating in a reduced conduction angle mode such as class B or C. This, G_{Meff}, allows us to better model the loop stability of the CCA biasing control circuit.

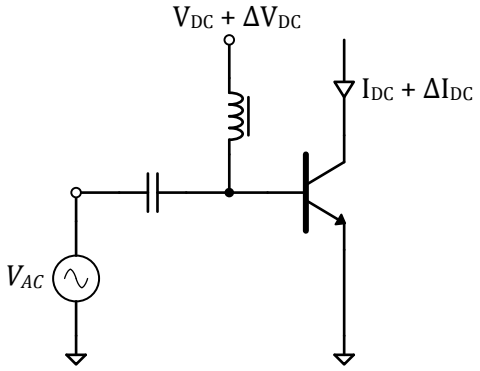

Figure B.1 Transistor depiction of the CCA biasing of a class C device.

Equations (B.1) and (B.2), derived earlier, are needed in determining G_{Meff}.

$$\frac{V_{DC}}{V_{AC}} = -\cos\frac{\theta}{2} \tag{B.1}$$

$$I_{DC} = \frac{g_m}{\pi} \cdot \left(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2}\right) \cdot V_{AC} \tag{B.2}$$

We can make the following formalizations:

$$\theta \rightarrow \frac{V_{DC}}{V_{AC}} \xrightarrow{G_{M_{eff}}} I_{DC} \tag{B.3}$$

The conduction angle specifies a certain DC bias-to-AC drive ratio and this therein gives rise to a DC drain/collector current by virtue of the so-called "G_{Meff}" we are solving for.

To solve for G_{Meff}, let's consider a small change in the DC bias voltage which gives rise to a small change in the DC drain/collector current.

$$V_{DC} + \Delta V_{DC} \rightarrow I_{DC} + \Delta I_{DC} \tag{B.4}$$

And also the nominal conduction angle is related by:

$$\theta \rightarrow \frac{V_{DC} + \Delta V_{DC}}{V_{AC}} \tag{B.5}$$

The form of the desired effective transconductance is given as:

$$\Delta I_{DC} = G_{M_{eff}} \Delta V_{DC} \tag{B.6}$$

Observing (B.2), the quantity in parenthesis is dependent on the conduction angle which is related by the expression in (B.3). Thus we can write:

$$I_{DC} + \Delta I_{DC} = \frac{g_m}{\pi} \cdot \mathcal{F}\left[\frac{V_{DC} + \Delta V_{DC}}{V_{AC}}\right] \cdot V_{AC}$$

where,

$$\mathcal{F}\left[\frac{V_{DC} + \Delta V_{DC}}{V_{AC}}\right] = sin\frac{\theta}{2} - \frac{\theta}{2}cos\frac{\theta}{2} \tag{B.7}$$

This expression can be approximated and simplified as follows:

$$\begin{aligned} I_{DC} + \Delta I_{DC} &\approx \frac{g_m}{\pi} \cdot \left(\mathcal{F}\left[\frac{V_{DC}}{V_{AC}}\right] + \alpha \frac{\Delta V_{DC}}{V_{AC}}\right) \cdot V_{AC} \\ &= \underline{\left(\frac{g_m}{\pi} \cdot \mathcal{F}\left[\frac{V_{DC}}{V_{AC}}\right] \cdot V_{AC}\right)} + \left(\frac{g_m}{\pi} \cdot \alpha \frac{\Delta V_{DC}}{V_{AC}} \cdot V_{AC}\right) \end{aligned} \tag{B.8}$$

The underlined expression in (B.8) is just I_{DC} and we can further simplify overall expression and write $G_{M_{eff}}$.

$$\cancel{I_{DC}} + \Delta I_{DC} = \cancel{I_{DC}} + \frac{g_m}{\pi} \cdot \alpha \frac{\Delta V_{DC}}{\cancel{V_{AC}}} \cdot \cancel{V_{AC}}$$

$$\Delta I_{DC} = \left(\frac{g_m}{\pi}\alpha\right) \cdot \Delta V_{DC}$$

$$G_{M_{eff}} = \frac{g_m}{\pi}\alpha \tag{B.9}$$

So how do we find α, the effective transconductance scaling factor? It is dependent upon the conduction angle and the procedure for empirically finding α for a given conduction angle is outlined next.

We start with the conduction angle of interest and calculate the associated V_{DC}/V_{AC} ratio. This is the starting point of the analysis and we want to observe the change about this point. The independent variable given in (B.5) is explicitly shown in (B.10).

$$\frac{V_{DC} + \Delta V_{DC}}{V_{AC}} = \frac{V_{DC}}{V_{AC}} + \delta \tag{B.10}$$

where,

$$\delta = \frac{\Delta V_{DC}}{V_{AC}}$$

To solve for the dependent variable, $\mathcal{F}\left[\frac{V_{DC}+\Delta V_{DC}}{V_{AC}}\right]$, we first need to solve for the conduction angle using (B.10).

$$\theta = 2\cos^{-1}\left(\frac{V_{DC}}{V_{AC}} + \delta\right) \tag{B.11}$$

Now, we need to solve the dependent variable for a slew of points close to the nominal V_{DC}/V_{AC}. We can then plot the function in Excel and use the curve-fit capability of Excel to find an equation for this line, in order to extract the slope.

Now, why is the slope important? Well, if we plot the function we will obtain an equation of line in the form shown below.

$$\mathcal{F}\left[\frac{V_{DC}+\Delta V_{DC}}{V_{AC}}\right]=m\left(\frac{V_{DC}+\Delta V_{DC}}{V_{AC}}\right)+b$$

which simplifies to:

$$\mathcal{F}\left[\frac{V_{DC}+\Delta V_{DC}}{V_{AC}}\right]=m\frac{V_{DC}}{V_{AC}}+m\frac{\Delta V_{DC}}{V_{AC}}+b \tag{B.12}$$

Remember, earlier we approximated the dependent variable to:

$$\mathcal{F}\left[\frac{V_{DC}+\Delta V_{DC}}{V_{AC}}\right]\approx\mathcal{F}\left[\frac{V_{DC}}{V_{AC}}\right]+\alpha\frac{\Delta V_{DC}}{V_{AC}} \tag{B.13}$$

Therefore, equating (B.12) and (B.13) we obtain:

$$\mathcal{F}\left[\frac{V_{DC}}{V_{AC}}\right]=m\frac{V_{DC}}{V_{AC}}+b \tag{B.14}$$

where,

$$\alpha=m \tag{B.15}$$

Using the aforementioned method α was solved for conduction angles of 90° to 180° in 10° steps. In keeping consistent and accurate, the step size (δ) was set such that the conduction angles only varied by about 3% from the nominal conduction angle. The resulting plot is shown in Figure 2 on the next page.

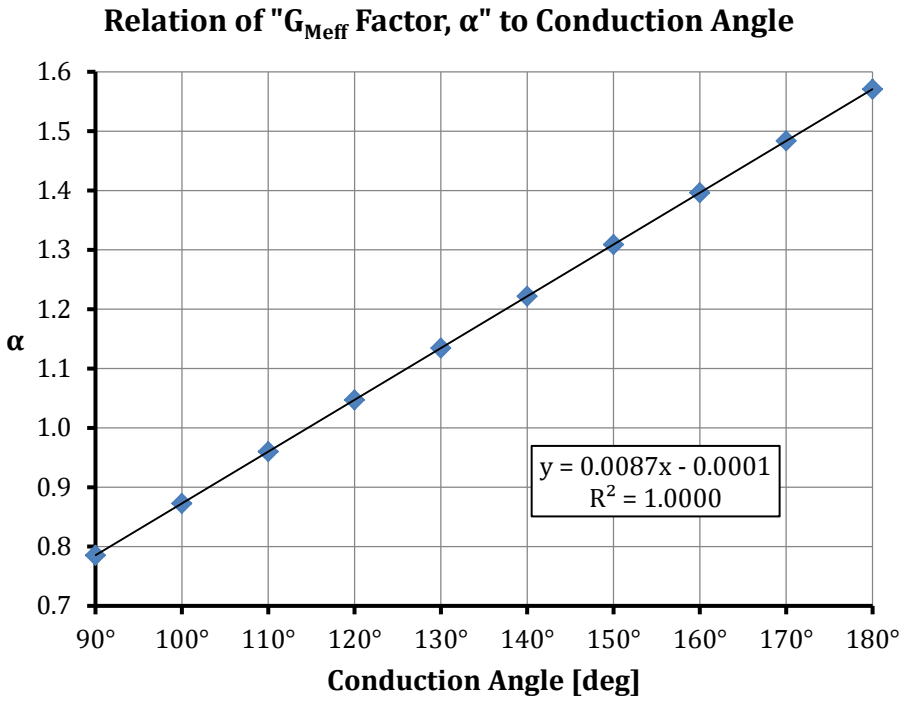

Figure B.2 Relationship between alpha & the conduction angle[65].

The result is very appealing. We can write the following expression for alpha:

$$\alpha \approx 0.00873 \cdot \theta = \frac{\theta\ [deg]}{114.5°} = \frac{\theta\ [rad]}{2} \tag{B.16}$$

Plugging this in the G_{Meff} expression, we obtain:

$$G_{M_{eff}} \approx \frac{g_m}{2\pi} \cdot \theta[rad] \tag{B.17}$$

[65] The "R^2" value in the excel chart represents how well the "curve" fits the data.

Appendix C
Cadsoft Eagle Tutorial: Package, Schematic, and Layout Creation by Matthew Bloom

PCB Design: Package Creation

Download the free version of Cadsoft Eagle from http://www.cadsoftusa.com/download-eagle/?language=en. There are usually three steps involved in the entire PCB process: package creation, schematic entry, and PCB layout. The package creation step, in some cases, can be skipped if the package/footprint for a specific part is already given.

Start by creating a new library in Eagle (refer to Figure C.1). After a new library window appears, name the library file and save it to the "lbr" directory where Eagle was installed to (example: JohnDoeCustom.lib).

During the component creation process, there are three steps the user must proceed through to make the final part. The three steps are Package Creation, Symbol Creation, and Device Creation. Package Creation involves creating a footprint for the component, which will consist of laying out land patterns (surface mount, through hole, etc.), silk screens, and so forth. Symbol Creation involves creating the schematic symbol for the component. Component Creation links the package to the schematic symbol. Refer to Figure C.2 for the library window.

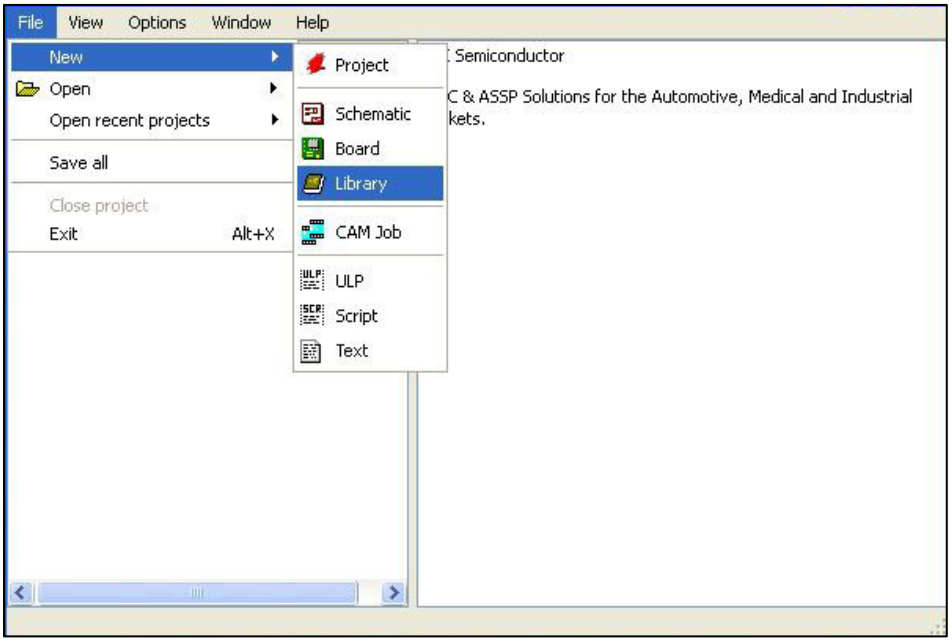

Figure C.1 Cadsoft Eagle main window – starting a custom library.

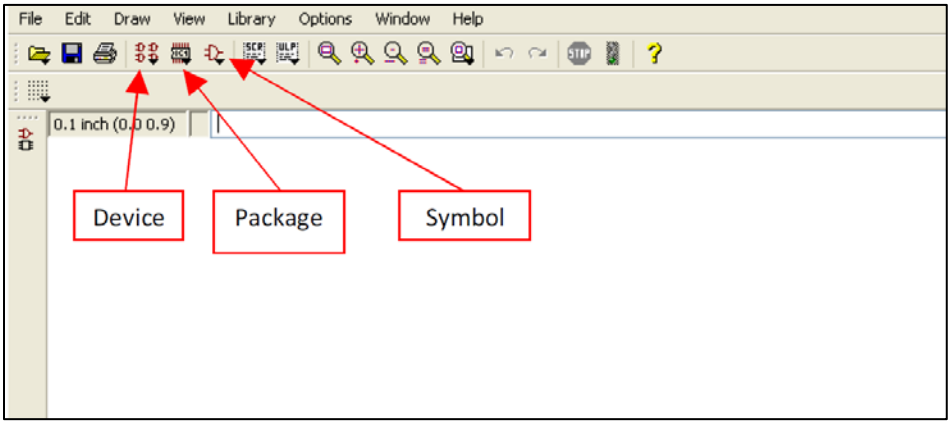

Figure C.2 Cadsoft Eagle library window.

Begin component creation by selecting the package button. When the “Edit” window appears, name the package after the component’s package type, and then save the name. A black background with a grid should appear; the window has now changed to the package creation window. Before setting up the package in the workplace, the user should consult the component’s datasheet for recommended land patterns. Once the land pattern is found, start the process by setting up the work space’s grid (Figure C.3). After setting a desired grid area, start placing either surface mount pads (SMDs) or through-hole pads onto the workspace using the recommended land patterns from the datasheet. The size and shape of each pad can be altered by going to the top of the work space and changing the dimensions (Figure C.4). To make a circular SMD, set the roundness to 100%.

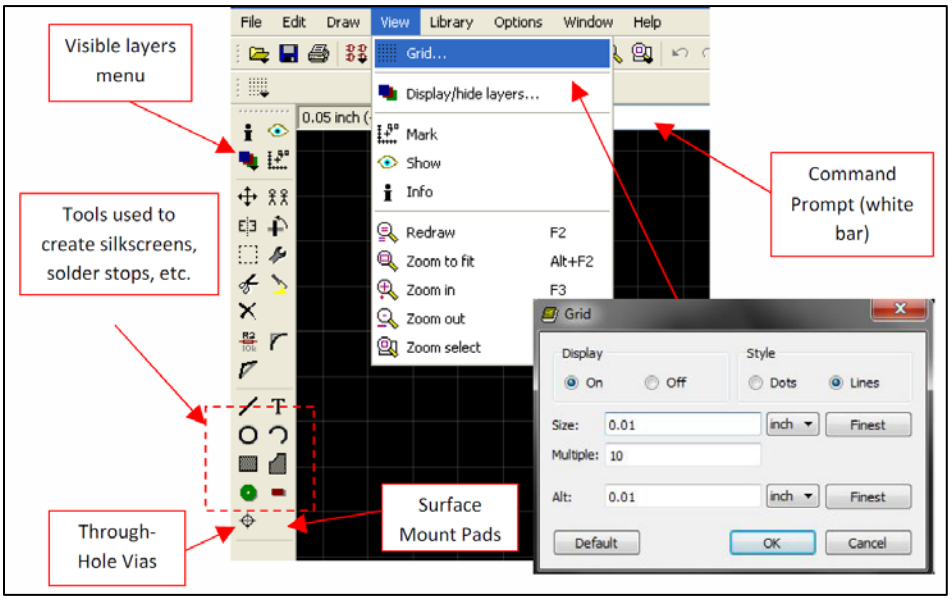

Figure C.3 Package creation work space with typical grid settings.

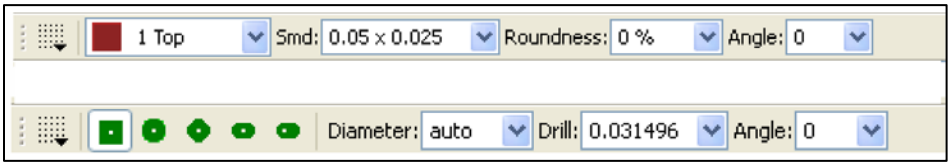

Figure C.4 SMD and through-hole size/dimension options, respectively.

Note that the SMDs should be on the “Top” (copper) layer, and the through-hole pads should be on the “Pads” layer. To check if certain aspects of the design are on the right layers, select the visible layers drop down and select/deselect layers. After placing pads, silkscreens can be placed to outline the component’s package and display the component’s schematic reference number and manufacturer number. Component outline silkscreens can be created using the ***Wire*** and ***Circle*** tools on the left toolbar, while the reference number (Name) and manufacturer’s part number (Value) silkscreens can be created using the ***Text*** tool. Note that during component creation, the reference number and part number should be set as “>Name” and “>Value.” The actual designators will be placed onto the layout workspace once the schematic is created. The component outline silkscreens should be created on the “tPlace” layer while the Name and Value silkscreens should be placed on the “tName” and “tPlace” layers, respectively. The "t" in each layer represents the top layer ("b" would then represent the bottom layer). As an example, a finished part is shown in Figure C.5 (8-pin DIP socket for the TL072).

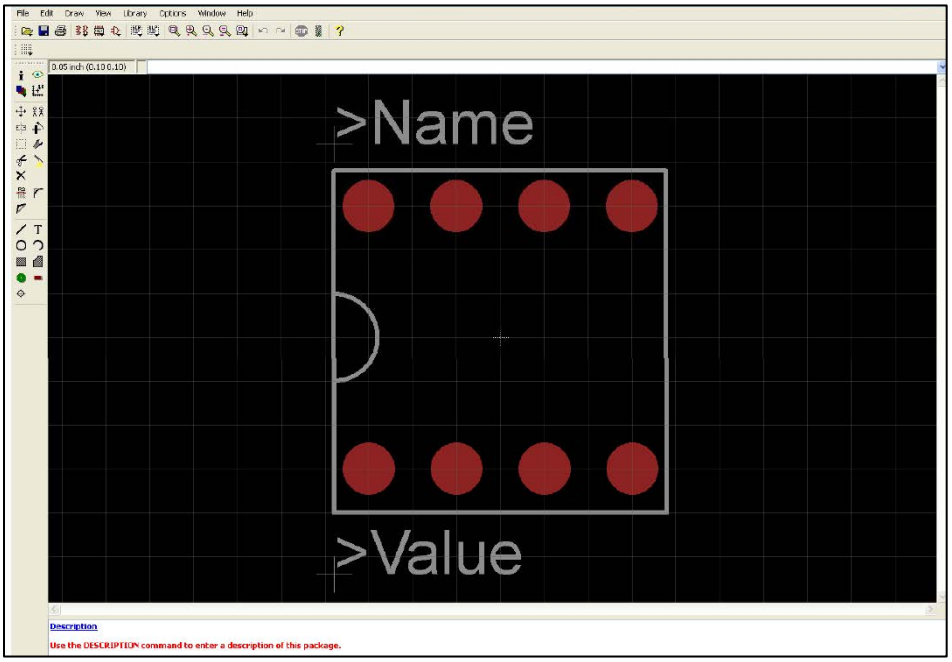

Figure C.5 Package design example – 8-pin DIP socket for TL072.

A few tips about the package creation process should be mentioned. The first is the shortcut to place pads down through coordinate commands. At the top of the work space is a white command prompt bar. Instead of clicking and dragging pads to a specific coordinate, each point can be entered in an (x y) format. For example, if a pad is required 60mils x 100mils from the origin (and the units are in inches), the coordinate command would be (0.060 0.100) (type the coordinates and press enter).

The second tip revolves around the use of the crosshair at the center of the workspace. The crosshair is used as an indicator for how a part will be placed onto the user's cursor when being dragged and placed onto the workspace during the layout stage. Therefore it is a matter of preference for the user on how the part will be oriented onto the workspace during the package stage. A general method used is to center the bottom-left most pad onto the cross-hair and design the package from there. Once the package is completed, select the ***Group*** tool and drag a selection box over every single package element. Once the package is highlighted, select the ***Move*** tool and right-click near the package. At the bottom of the tool-tip that shows up, select ***Move: Group***. Center the package around the center cross-hair and save the design.

The third tip is in regards to pad naming. To make connections between the schematic symbol and the package simple, each pad can be given a name. Type “Name” into the command prompt and select each pad. A new window will come up where the respective pin name or designator can be edited. The same process should be performed during schematic symbol creation when handling pin names.

Next, create a schematic symbol by selecting the associated icon. An “Edit” prompt will appear much like during the package process. Name the schematic symbol after the

manufacturer's part name and proceed. A window similar to the package creation work space will appear, but the background will be white (Figure C.6). The default grid configuration should be acceptable for this process, but can also be altered to the user's preferences. The entire schematic process is similar to that of the package process, where each pin will receive a name/designator and the symbol will be labeled with the >Name and >Value conventions. An example symbol can be seen in Figure C.7 (8-pin DIP socket for the TL072).

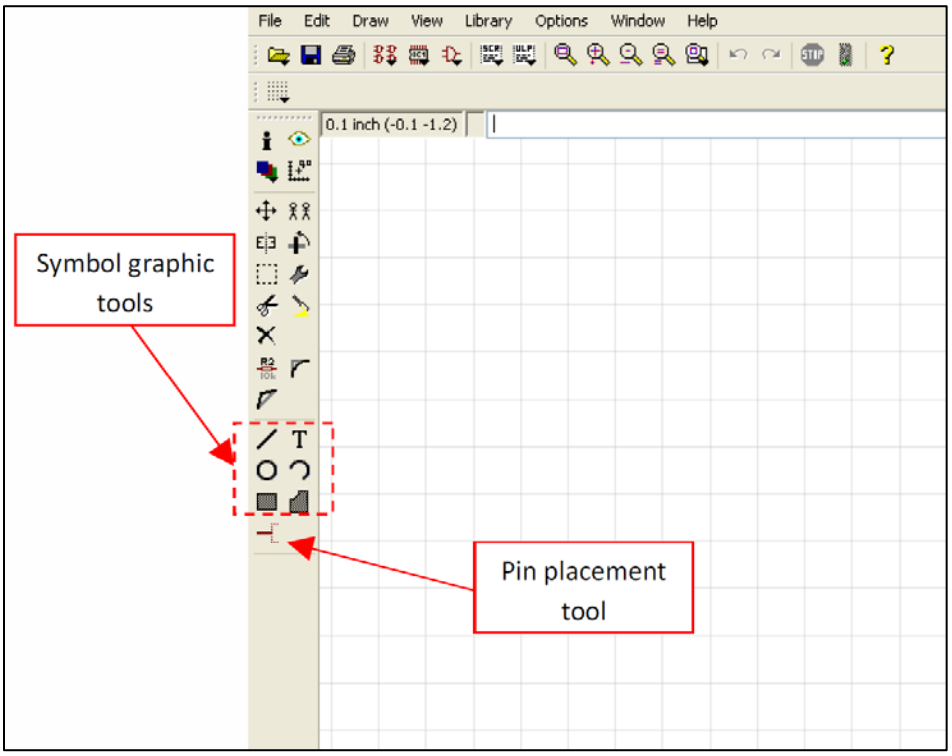

Figure C.6 Schematic symbol creation work space.

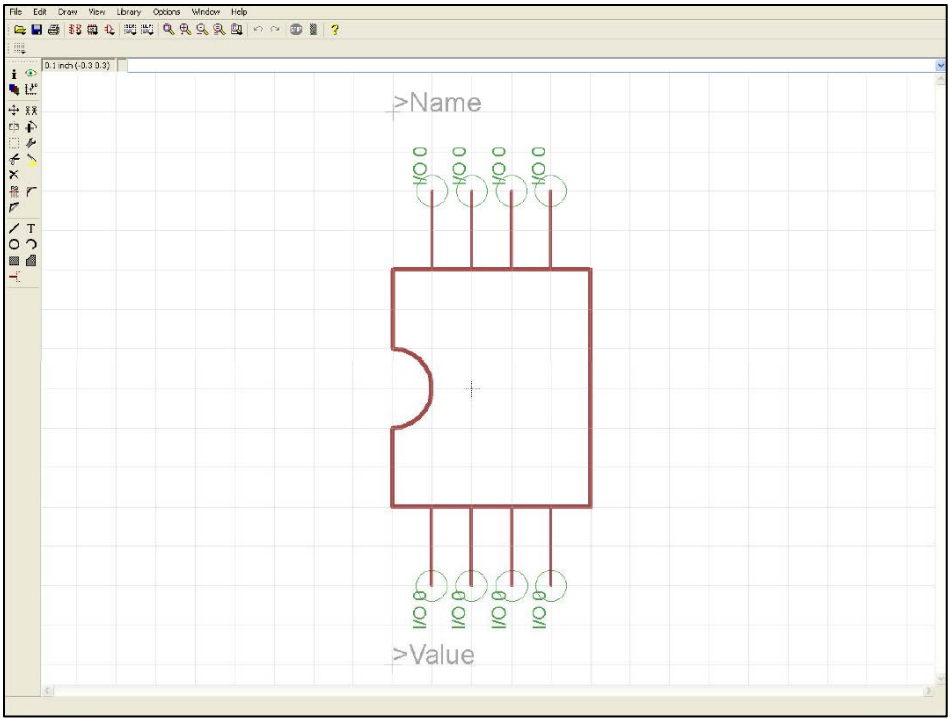

Figure C.7 Schematic symbol design example – 8-pin DIP socket for the TL072.

Finally, select the ***Device*** icon to complete the component creation process. A new window should appear as seen in Figure C.8. First, click the ***Add*** button and select the schematic symbol that was created. Next, click the ***New*** button and add the created package symbol. Finally, press the ***Connect*** button to link the schematic and package symbols together. The connection window should look like Figure C.9. If the pads and pins from the previous processes were given their respective names, they should line up directly with one another as seen in Figure C.9. If not, the user will have to search for and select the connections between each associated pad and pin. By the end of the connection process, the "Connection" section in the last-third of the window should be full. Press "OK" to complete the component process.

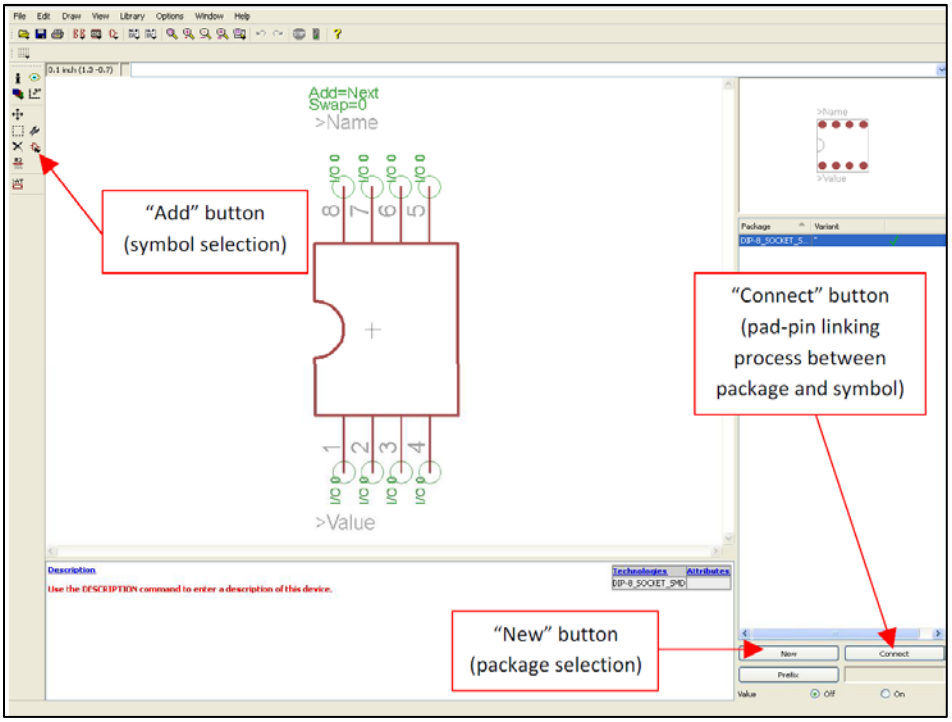

Figure C.8 Device creation work space.

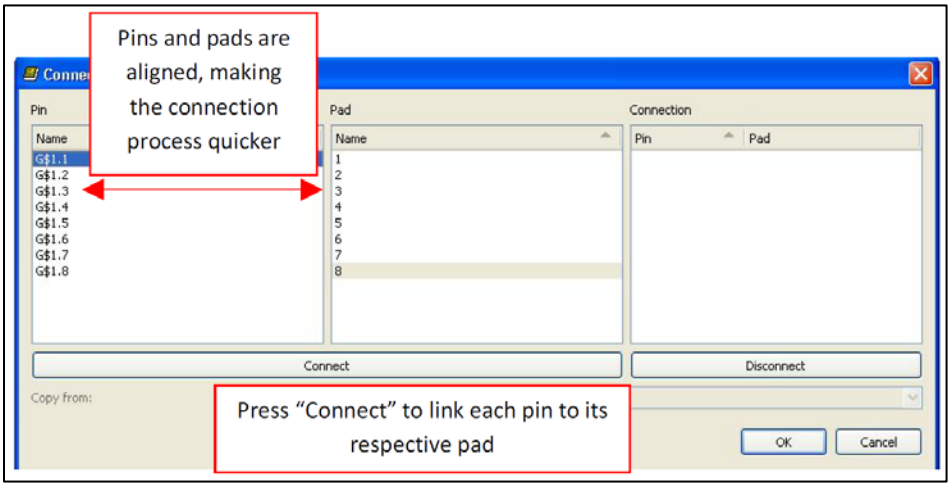

Figure C.9 Schematic and package symbol connection window.

PCB Design: Schematic and Layout

Start a new project in Eagle by referring to Figure C.10and then start a new schematic as seen in Figure C.11.

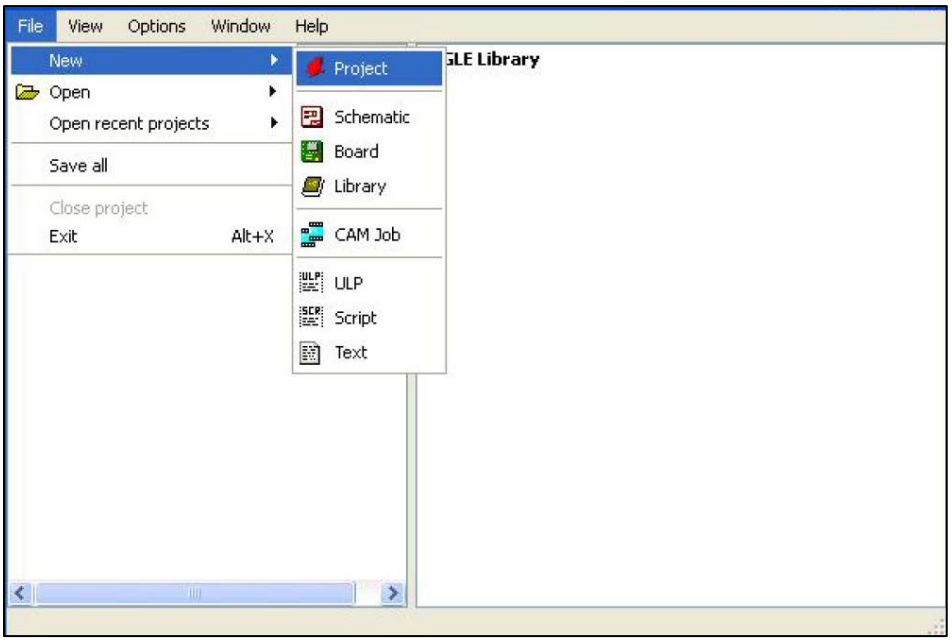

Figure C.10 Starting a new project in Eagle.

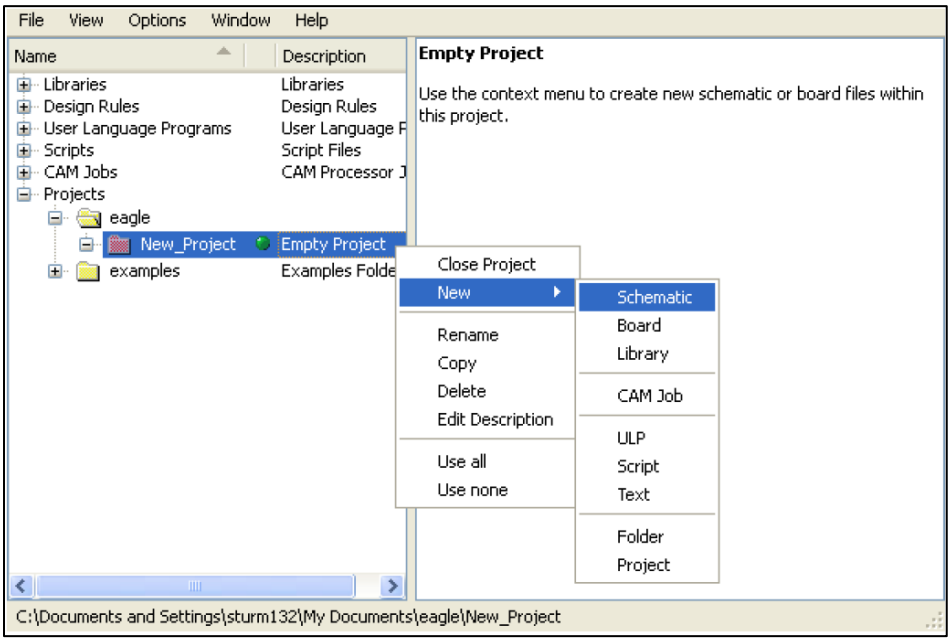

Figure C.11 Starting a new schematic in the project directory.

A new schematic work space should appear, as seen in Figure C.12. All parts should be accessible via the ***Add*** button (including parts from the custom-made library). Place parts onto the schematic work space and wire them together using the ***Wire*** tool. All components can have their reference names and values changed by selecting the ***Name*** and ***Value*** tools. One useful tool to use is the ***Group*** tool when having to move or copy multiple components at any given time. For example, group all desired components together by creating a selection box with the Group tool. Once all desired components are highlighted, select either the move or copy option, and then right-click the work space. Finally, when the tool-tip appears, select "Group: "<Action>," where <Action> is either move, copy, or another command. After completing the schematic entry, press the ***Board*** button at the top of the work space to generate a board layout from the schematic.

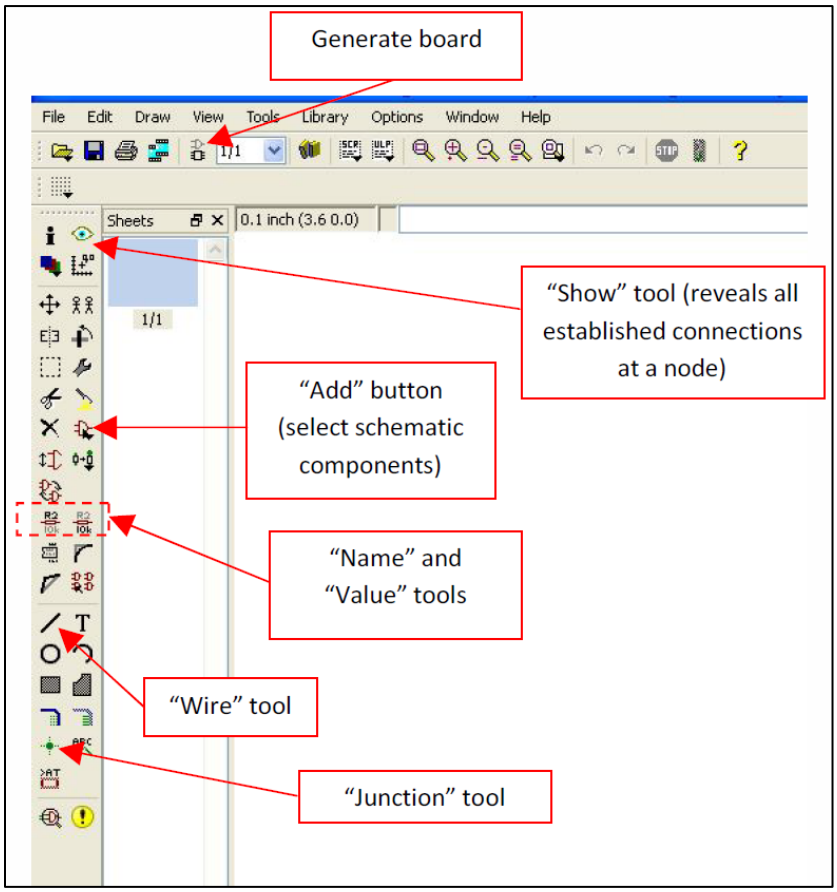

Figure C.12 Schematic workspace.

When Eagle generates the board layout, the program will create a component pile at the bottom left corner of the layout work space (Figure C.13). Before routing the board, it is usually wise to specify the design rules for the board, which follow the guidelines established by the board fabricator. To access the design rules, go to **Tools > DRC**… and input the necessary fabrication limitations.

As seen in Figure C.13, the white rectangular boundaries within the work space are the board dimensions for the PCB. The boundaries can be adjusted by clicking and dragging the polygon. Each of the components on the screen can also be clicked and dragged onto the PCB area. Note how each connected component from the schematic is now connected by a yellow line known as a "netlist." All components can either be manually routed by following each netlist, or an auto-route feature can be used by selecting the ***Auto*** button on the left toolbox. When routing components, a majority of the routing will take place on the "Top" layer (rustic-colored). However, routing can also take place on the "Bottom" layer (blue-colored). Because the board is a 2-layer design, the top layer is usually the component layer whereas the bottom layer is specified as ground.

To set the bottom layer as ground, select the ***Polygon*** tool in the left toolbox, and then select the layer to be "Bottom" from the layer pull-down menu at the top of the work space. Create a rectangular polygon around the inner sides of the PCB boundary (keep a small amount of buffer room between the ground plane and board edges). After the polygon is created, right-click on the polygon, select "Properties," and rename the signal name to "GND." Once connections are made

to the GND netlist, the bottom layer should automatically fill up from the blue polygon GND layer. If not, press the “Ratsnest” button. Use the steps above to complete the PCB layout.

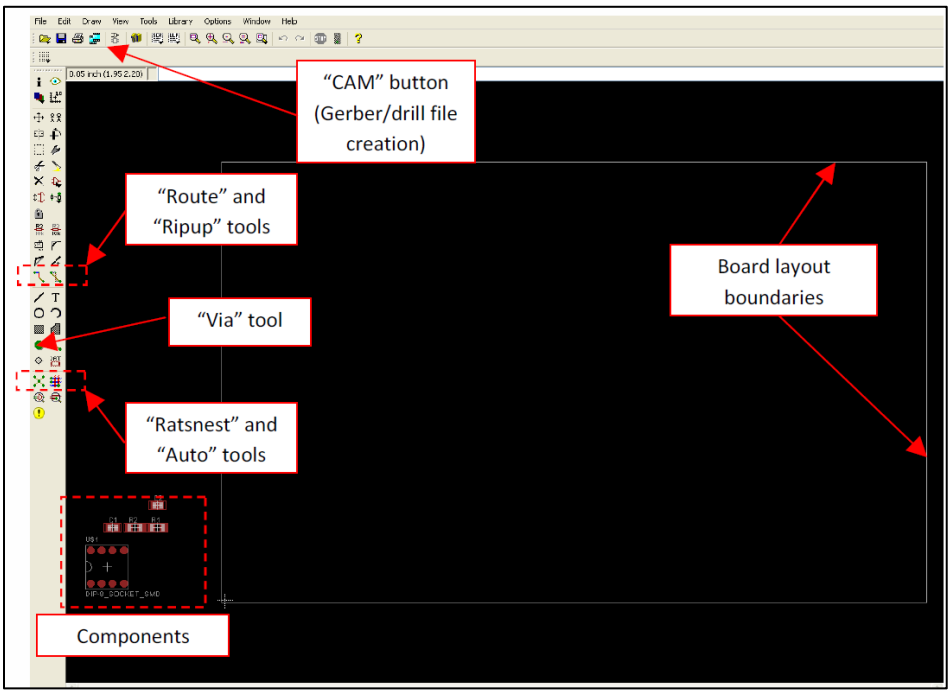

Figure C.13 Layout workspace.

PCB Design: Gerber File Generation

To generate the Gerber and drill files, select the “CAM” button at the top of the work space (refer to Figure C.13). When the CAM processor window opens, a job must be selected to generate the Gerber files for a 2-layer board (refer to Figure C.14). Next, select the “gerb274x.cam” job file, which is a default job created specifically for 2-layer boards.

Once the job is selected, the Cam processor window should now look like Figure C.15. Take notice of the tabs that appear at the top of the window. Gerber files should be generated for the component layer, ground layer, component silkscreens, component

layer solder-mask stop, and ground layer solder-mask stop. For each layer, the affected board attributes are highlighted in blue. Click “Process Job” when all parameters are configured.

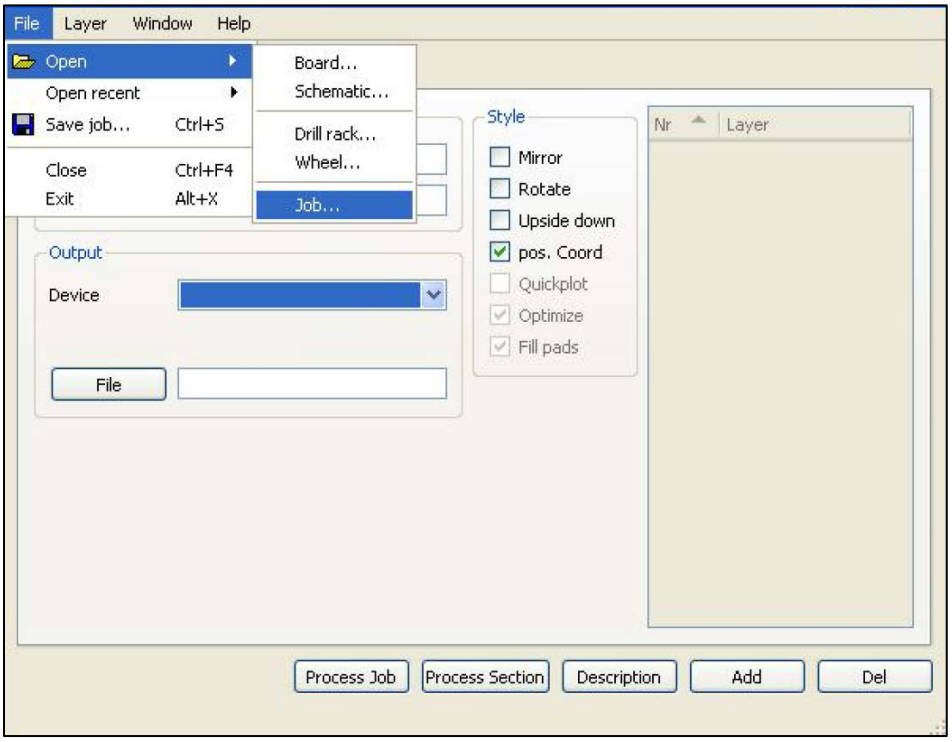

Figure C.14 CAM processor window.

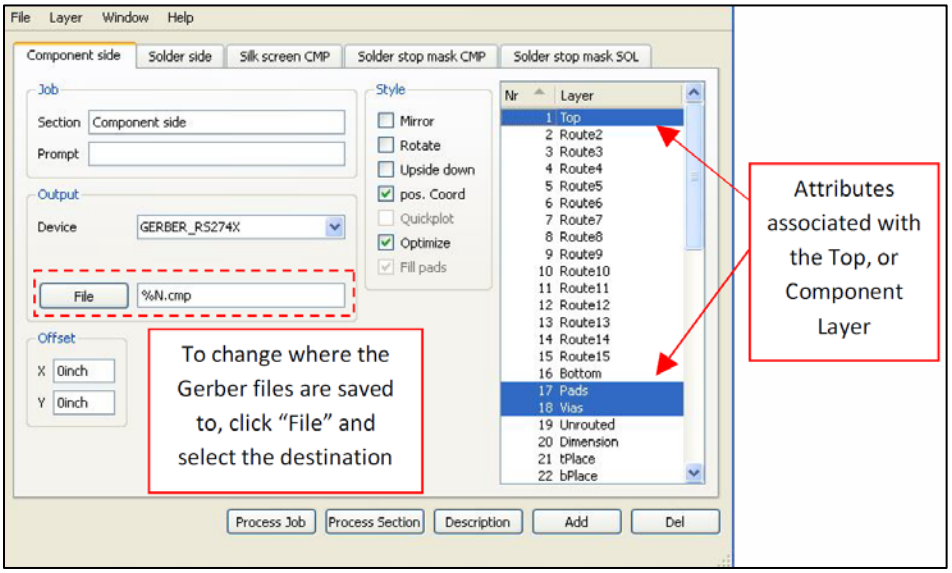

Figure C.15 Gerber file configuration for a 2-layer board job.

After the Gerber Files are saved, select File > Open > Job… and select the "excellon.cam" job to create the drill files for the board. A similar screen like Figure C.15 should appear. Again, once all parameters are set, click "Process Job." When sending the Gerber and drill files to a board fabrication house, certain files are necessary in the board fabrication process. For this project, the company Advanced Circuits (www.4pcb.com) was used as a board fabrication vendor. Table 1 lists the files necessary to have Advanced Circuits fabricate a board.

Table C.1 Necessary Gerber and drill files for board fabrication.

File	Description
.cmp	Component side data
.sol	Solder side data
.plc	Component side silk screen data
.stc	Component side solder stop mask data
.sts	Solder side stop mask data
.drd	Excellon drill description

Appendix D
Breadboard Layout & PCB Schematic, Layout

PCB Design: Package Creation

Figure C.1 shows the layout of the initial breadboard prototype from the perspective of looking up from the bottom side of the board. Three buses line the breadboard prototype on the right and left sides of the boards. To conveniently connect the class C power transistor, two of the lines on each side are designated for the base and collector. As a ground connection is necessary throughout, one of the busses is designated for ground. The power line is run by an external wire. As radiation was apparent from the lines, the excess portions of the busses were cut.

The PCB Schematic & Layout

Figure D.2 shows the Eagle schematic of the final PCB prototype. This schematic was used to generate the layout shown in Figure D.3. The bottom layer traces are shown in blue and the top layer traces are shown in red. With the exception of the isolated traces (shown with wide borders), the bottom layer is entirely ground. Vias are shown in green and holes are shown in white. The board layout measures 4 x 3.2 inches – the board size limit for the free version of Cadsoft Eagle.

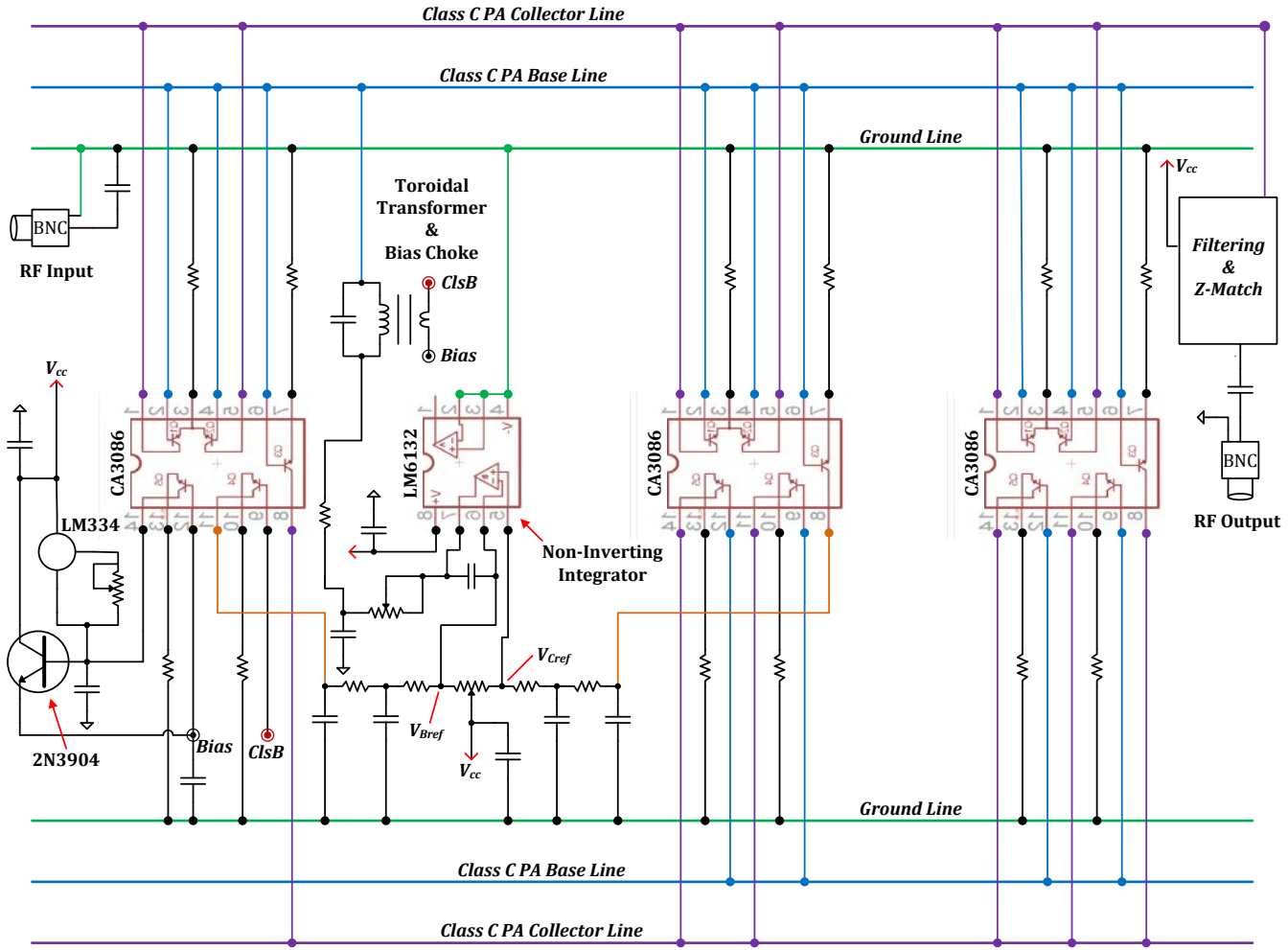

Figure D.1 Initial prototype layout as seen when looking from the perspective of the bottom.

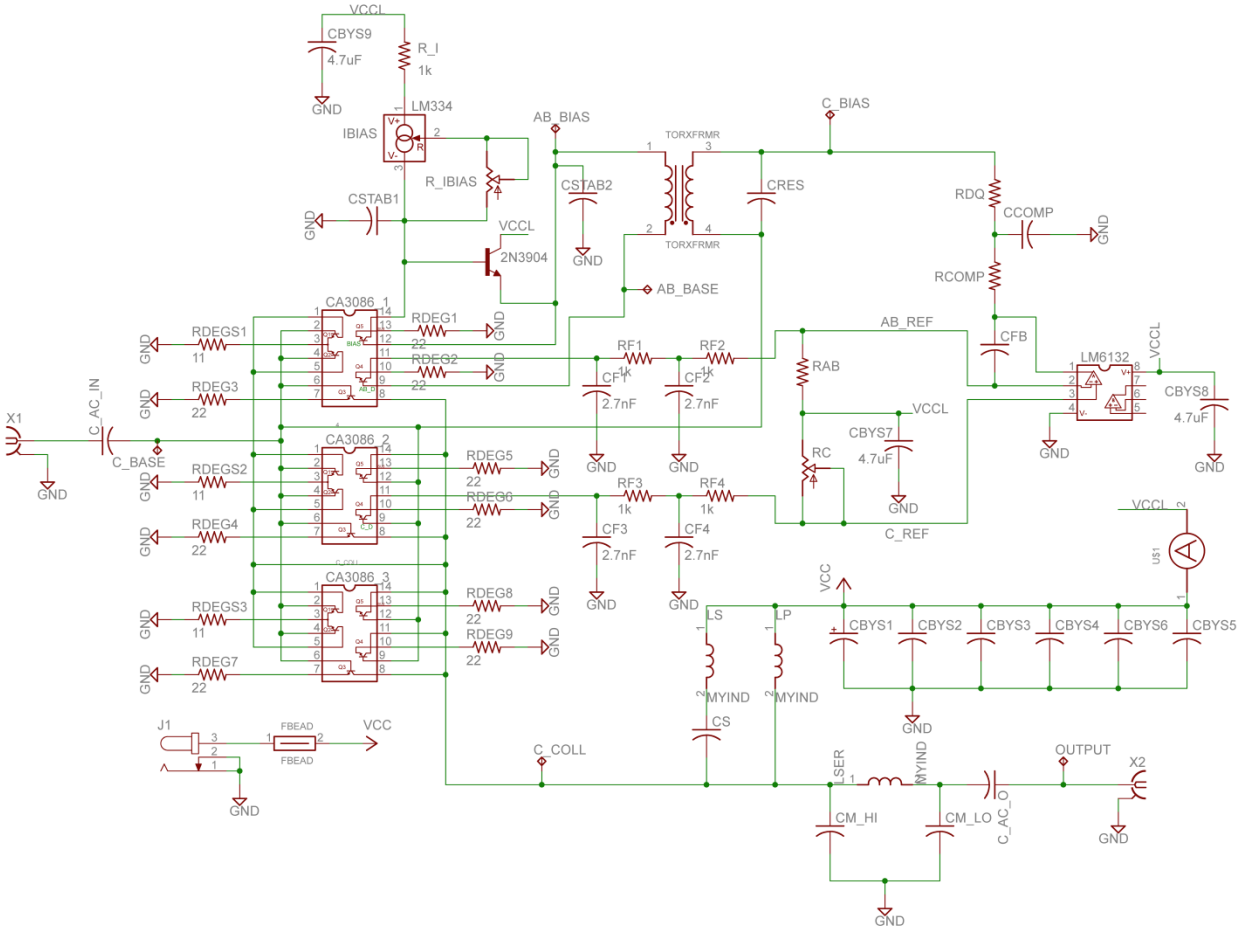

Figure D.2 Final PCB Eagle schematic.

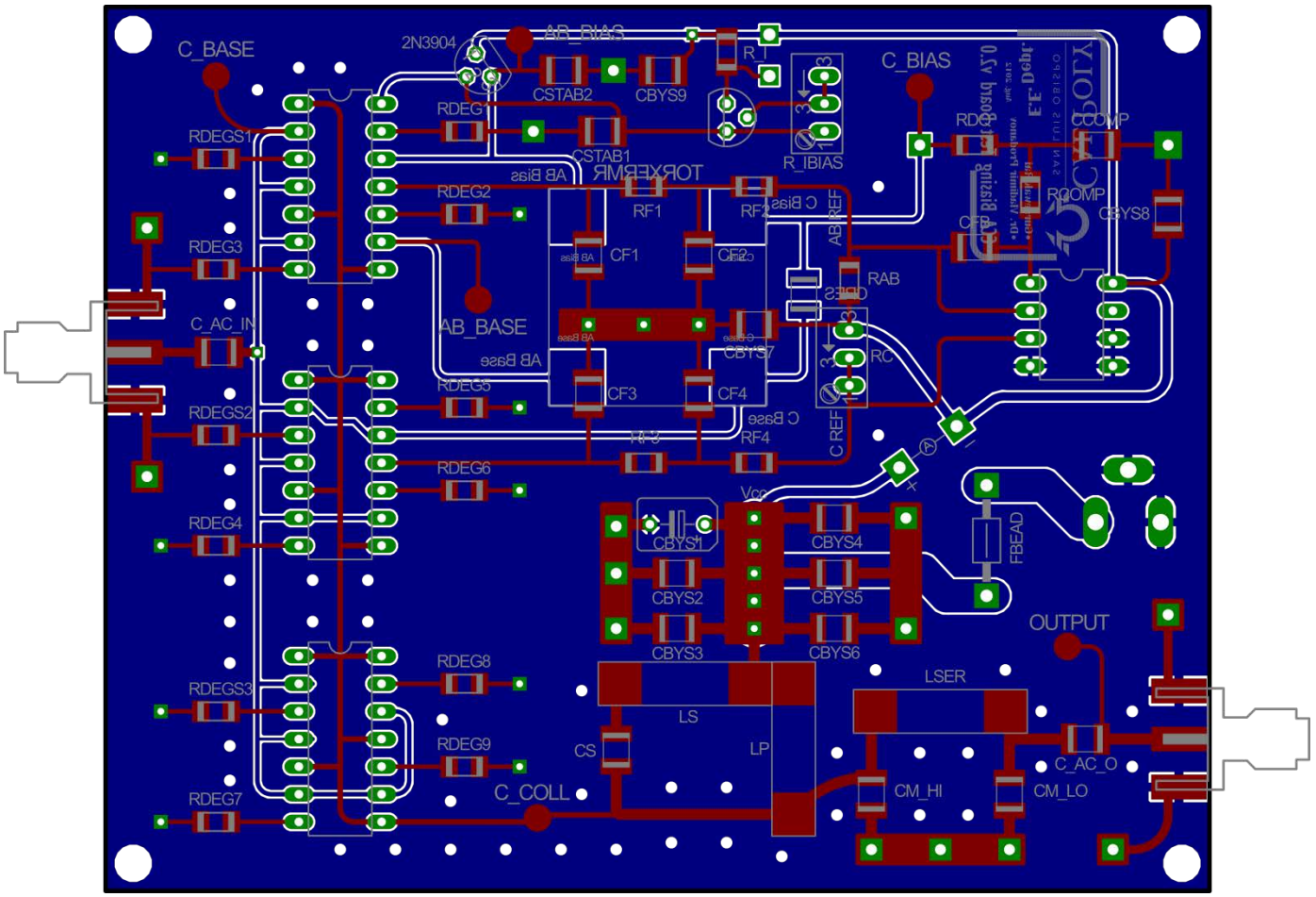

Figure D.3 Final PCB Eagle layout.

Appendix E
The Harmonic Short

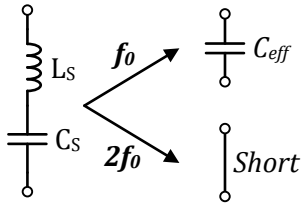

Figure E.1 A series LC which acts as a capacitor at the fundamental and a short for the second harmonic.

The circuit in Figure A.1 serves to short circuit the second harmonic while act as an effective capacitance at the fundamental. We can derive the design equations for selecting the appropriate component values to obtain aforementioned desired response.

We begin by defining the variable ω_0 as the fundamental frequency and ω_0^S as the series resonance frequency. The series resonance formula is given by:

$$\omega_0^S = \frac{1}{\sqrt{L_S C_S}} \tag{E.1}$$

We also write the reactance of the effective capacitance, C_{eff}:

$$X_{C_{eff}} = \frac{-1}{\omega_0 C_{eff}} \tag{E.2}$$

This reactance can also be expressed in terms of the sum of the series inductor and capacitor reactances.

$$X_{C_{eff}} = X_{L_S} + X_{C_S} = \omega_0 L_S - \frac{1}{\omega_0 C_S} \tag{E.3}$$

We then write L_s in terms of $X_{C_{eff}}$ by replacing C_s using (A.2).

$$X_{C_{eff}} = X_{L_S} + X_{C_S}$$

$$= \omega_0 L_s - \frac{1}{\omega_0 C_s}$$

$$= \omega_0 L_s - \frac{1}{\omega_0 \left[\frac{1}{(\omega_0^s)^2 L_s}\right]}$$

$$= \omega_0 L_s - \frac{(\omega_0^s)^2 L_s}{\omega_0}$$

$$= \frac{(\omega_0)^2 - (\omega_0^s)^2}{\omega_0} L_S$$

$$L_s = \frac{\omega_0}{(\omega_0)^2 - (\omega_0^s)^2} X_{Ceff} \tag{E.4}$$

Since we desire series resonance to occur at the second harmonic, $\omega_0^s = 2\omega_0$. Therefore, $L_s$can be rewritten as the following:

$$L_s = \frac{\omega_0}{\omega_0^2 - (2\omega_0)^2} X_{Ceff} = \underline{-\frac{X_{C_{eff}}}{3\omega_0}} \tag{E.5}$$

Similarly C_s is written as:

$$C_S = \frac{1}{(2\omega_0)^2 L_S} = \frac{1}{4\omega_0^2 \left(-\frac{X_{C_{eff}}}{3\omega_0}\right)} = \underline{-\frac{3}{4\omega_0 X_{C_{eff}}}} \tag{E.6}$$

Thus design procedure for the harmonic short that is integrated into the output network of the CCA biasing circuit consists of two steps:

1) Solve for the reactance of C_{eff}.
2) Plug this reactance into (E.5) and (E.6) to solve for the series inductance and capacitance, respectively.