FINAL DESIGN REVIEW

Design of an Integrated Solar Cell Array to Power a Solar Ear Hearing Aid Battery Recharger

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EXECUTIVE SUMMARY

As the energy of fossil fuel supplies are fast depleting due to high consumptions of energy by human beings, the need for other sources of energy, such as solar energy, has become a viable option. By creating solar cell arrays the desired voltage can be generated. The overall goal of the Solar Ear project is to create an array of photovoltaic cells connected with aluminum tracings to recharge batteries that are specifically used for hearing aids. The goal embodies two main areas: the design of a processing method to connect the cells during a micro-fabrication process and the creation of an array that produces enough voltage and current to power low-power applications like a hearing aid battery recharger. We have successfully designed and fabricated a device with two cells connected in series thus far to make sure the interconnections in our design were capable of connecting cells in an array. An aluminum bridge across an insulating channel of SU-8 was created as an interconnection to connect both cells on the silicon-on-insulator (SOI) wafer. Although we successfully addressed the first goal to connect the cells, this two-cell device did not produce the desired voltage and current. To address this problem we optimized the manufacturing process by creating larger doped regions and forming an oxide over the wafer surface with vias to create the aluminum contacts. These modifications were enacted during spring quarter when we fabricated a 12-cell device. These final devices exhibited good cell interconnection and a maximum of 5.5V was obtained from one of the final wafers. The current produced by these devices, however, was nearly 10 times less than expected and failed to reach the levels necessary to charge a hearing aid battery.

INTRODUCTION

SPONSOR BACKGROUND AND NEEDS

The intended goal of this project is to create a solar cell array to power a battery recharger, specifically for recharging hearing aid batteries. Our goal is to design, fabricate and test a small solar cell array capable of generating power for a portable hearing aid recharger. The stakeholders of our project are the future users of the product. At least two thirds of the 250 million people who experience hearing loss do not have access to advances in hearing aid technology and live in developing countries (Kumar 2001). We want to target the markets in third world countries where power sources and/or batteries are not readily available.

In order to better understand the specific requirements of our stakeholders, we conducted an interview with a local audiologist, Jacqueline M. Carr of Hearing Aids Audiology, Inc. Through this interview we determined that the current market for hearing aid rechargeable batteries is not very prominent. GN Resound, one of the world's largest providers of hearing aids and audiological instrumentation, had previously released a rechargeable device for hearing aids. It was discontinued in February 2009 with complaints from consumers for the product's lack of durability. Carr also mentioned that the alternative and main power source of hearing aids today, button batteries, are also not the most convenient way to power a hearing aid. The biggest complaint from customers is the fact that these disposable batteries do not last very long. Each battery, depending on size, can last from a minimum of 3-5 days to a maximum of 1-2 weeks before a replacement battery is needed. A pack of 6 medium sized batteries, each lasting about a week, costs about $7.25. Costs to replace these batteries add up quickly, especially if consumers experience bilateral hearing loss, like most of Carr's patients.

If our main stakeholders are residents of developing countries, then there are certain obstacles that our team must overcome in order to help solve this problem. By creating a solar cell array that can fully charge a battery within 8 hours of direct sunlight we will eliminate the use of disposable batteries and can transition to using only rechargeable batteries in hearing aids.

BACKGROUND

IMPORTANCE OF THE SOLAR CELL

Solar cells are a very useful way of providing electricity to remote areas where the use of electricity may be essential but the availability may not be feasible. One example where solar energy and solar cells are necessary is in space. For many years, satellites have been using solar panels to catch the sun's rays to provide power to the equipment on board. Solar cells can be aligned as an array. There are many advantages of using a solar cell array with various panels such as the ability to combine various numbers of cells to provide a greater output of electricity. This method makes solar electricity a viable option to contribute to powering small devices, such as batteries, and large devices, such as the homes we live in. Fossil fuel supplies of energy are fast depleting and they may take thousands of years to be reformed. The consumption of energy in the form of fuel and electricity by human beings is so high, that fossil fuels would not be able to sustain human activity for much longer. The switch over to a clean, efficient and available source of energy would be beneficial. Solar cells have provided us with a free, renewable and clean source of energy that has the ability to be used anywhere there is sunlight.

SCIENCE BEHIND THE SOLAR CELL

A solar cell is built from a p-n junction in a semiconductor material such as silicon, meaning a material with extra protons (positive charge) is in contact with a material with extra electrons (negative charge). Energy from a photon of light striking the solar cells knocks the extra valence electrons loose, allowing it to flow through a circuit to the p-region while a hole simultaneously flows to the n-region. If individual solar cells are connected together in series, a solar array is created (Figure 1).

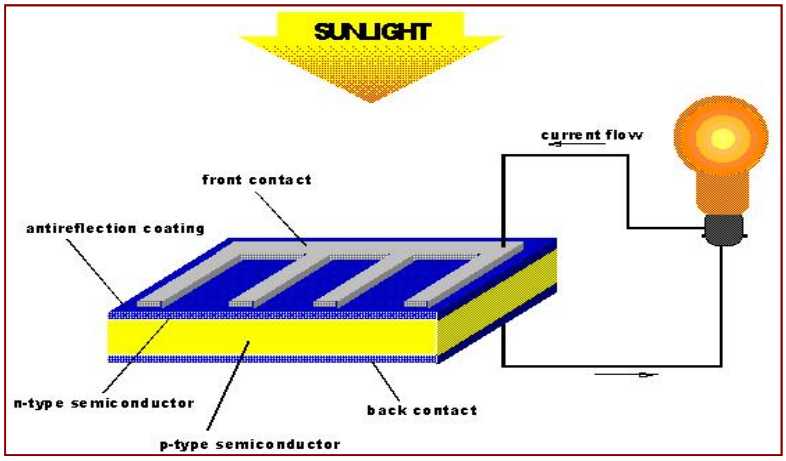


Figure 1: Solar cells convert incident sunlight into electric energy.

The lifespan of most solar cells is at least twenty years. This period is assuming the cell continues to create electricity without any significant drop in efficiency. On average, solar cells tend to degrade to about 85% efficiency of their original performance after 25-30 years. Even with this consideration, our device can decrease costs of owning a hearing aid device by negating the need to constantly purchase batteries. Many different charging methods for batteries exist, but the most common methods include normal (trickle) charging, fast charging, and delta V charging. Trickle chargers provide a very small current to avoid the risk of overcharging the battery. This method is usually used for nickel-cadmium and nickel-metal hydride cells or batteries (Figure 2).

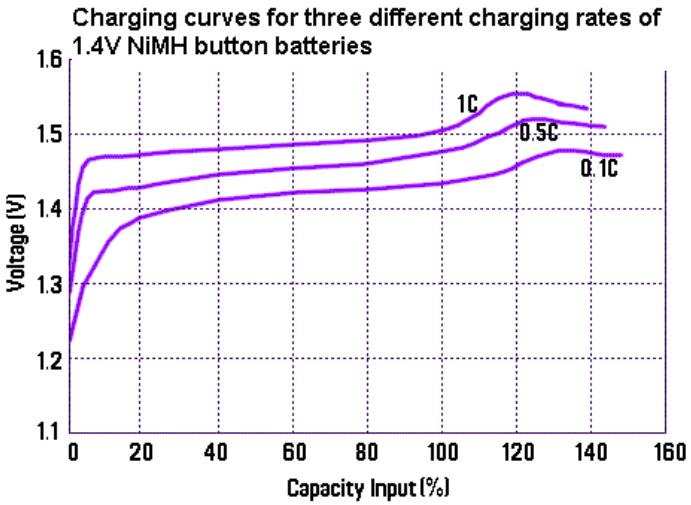


Figure 2: Charging curves for 1.4V NiMH hearing aid batteries.

Constant voltage can be used to charge Lithium-Ion batteries (Figure 3). In all cases, it is important not to overcharge the batteries. If there is no special circuitry to prevent overcharging, it is recommended to charge at a rate no faster than about 10% or the rated battery capacity per hour.

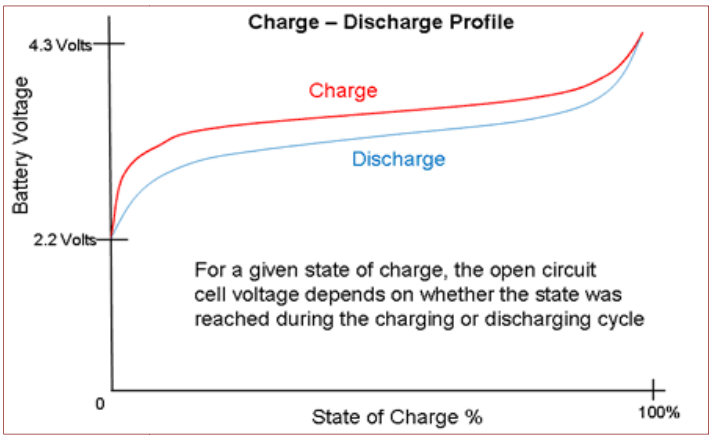


Figure 3: Voltage requirements to charge a lithium-ion battery.

EXISTING TECHNOLOGY

A non-profit organization, The Godisa Trust, currently offers technology and services in third world countries for the relief of hearing disabilities (McPherson, Brouilette 2004). They have recognized that hearing aids marketed in developed countries are not suitable for third world countries for various reasons: high costs of hearing aids/ batteries, lack of availability, lack of local repair or maintenance, non-durable through shipments and etc. Their aim is to mitigate these problems by developing products that are more appropriate in these countries' conditions. An initial idea was to create a solar aid Behind-the-Ear (BTE) hearing aid using a conventional rechargeable cell (Figure 4); similar to what this project is aiming for. Their product had gone through field-testing and was found to hold charge for about 4 days under 6 hours of direct sunlight. Their current products are inexpensive to manufacture, easy to charge, and use low cost NiMH batteries that are resistant to outside elements and can be sold at affordable prices in developing countries. In addition, a company, PowerOne, manufactures a NiMH Rechargeable battery in size 13 which are the most common size for hearing aids. The battery is rated for 1.2 V and 30 mAh. What Godisa and PowerOne have developed is similar to what our group is aiming to develop.

Figure 4: Godisa solar powered battery recharger. (McPherson, Brouilette 2004)

PREVIOUS PROJECTS

Last year Jeremy Lenhof and Sadao Takabayashi attempted to integrate the solar cells in series during the microfabrication process by creating an interconnect between cells on a single wafer. They were unsuccessful in creating a working design. The previous team's design is shown below, with shorts and disconnects pointed out (Figure 5).

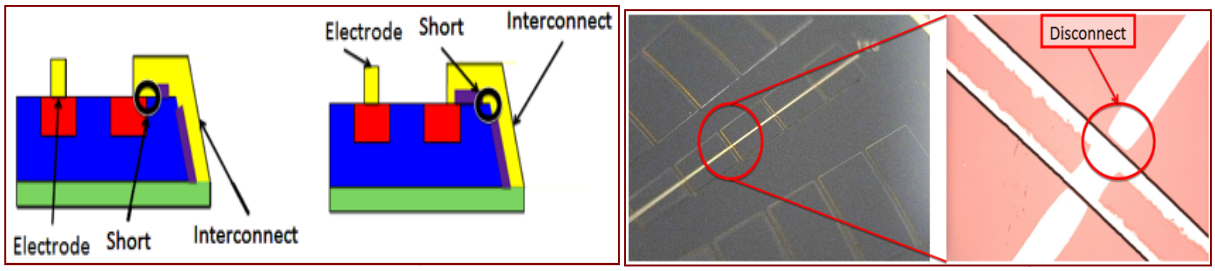


Figure 5: The previous possible problems areas for disconnects and shorts were at the corners of the islands containing the junctions.

Last year's team attempted to bridge the gap between the cells by placing the aluminum along the bottom of the chamber, shown on the left. This means the aluminum had to start at the top of the cell, coat the side of the channel down to the bottom, and back up to the top of the next cell. Based on the optical microscope images shown on the right, the team believed that there were disconnects in the aluminum traces at the corners. The second possible problem was a short at the junctions where the insulating layer failed to prevent the aluminum from contacting the positive and negative regions of one cell.

DESIGN DEVELOPMENT

FORMAL PROBLEM DEFINITION

Our team decided that the most critical component of our device was the connection between the cells in the array. These interconnects were the primary cause of failure in past years' projects due to shorting and disconnects. The challenges in fabricating interconnects are keeping the cells isolated from one another while creating a continuous circuit across the wafer.

The contacts of the solar cell connect the cell to the outside world. The contacts act like terminals on a battery, while interconnects connect each individual cell into an array of cells. The p-region of one cell is connected to the n-region of another cell and so on to create the electrical circuit. It is very important that the p-regions or the n-regions of any two cells are not connected together. This would cause a short circuit and render the cell useless. These contacts will be formed by patterning a sputtered aluminum layer. The interconnections will be formed by aluminum sputtered across an insulated channel between the cells. The formal problem is a need for a process to interconnect cells in an electrical circuit on a silicon wafer in such a way that the cells to produce enough power a hearing aid battery recharger.

OBJECTIVE/SPECIFICATION DEVELOPMENT

Our objective is to develop a manufacturing process to fabricate integrated solar cell arrays, connecting the cells in series through micro-fabrication processes rather than manually wiring them together. The performance requirements for the final deliverable for this project are presented in Table I.

Table I: Primary and Secondary Performance Requirements

Primary Requirements	**Cells must connect with low resistance (>50 Ω)**	**Produce a minimum of 2.5V**	**Enough current to power a low current device, such as an LED**
Secondary Requirements	Transfer power to charging circuitry	Packaging must be portable, handheld	Packaging should be transparent

CONCEPTUAL DESIGN

To address the disconnect issue identified by last year's team, our design solution involves depositing the aluminum contacts on top of an insulating SU-8 layer which will be sequestering the cells from one another. This will eliminate the need for the aluminum to maintain a continuous connection across a corner. Our design solution solves the shorting problem by doping the p-type regions out to the edges of each cell. An iteration of this design solution is shown below (Fig 6).

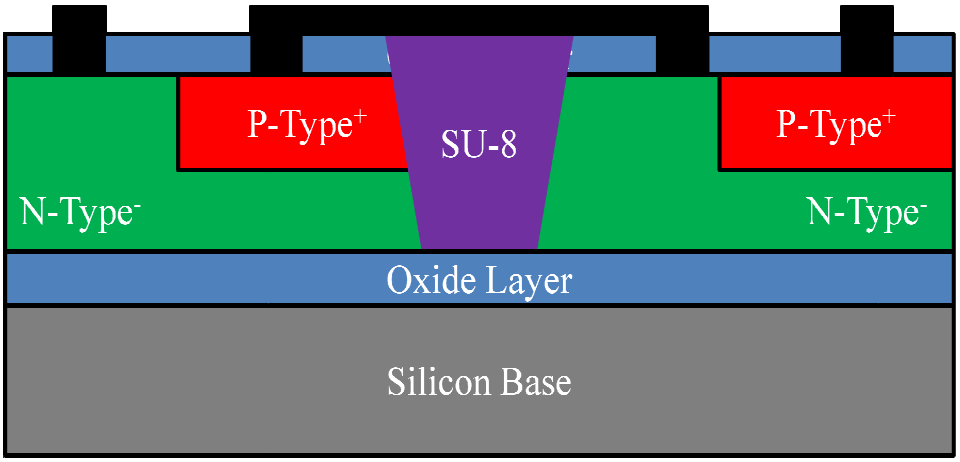


Figure 6: The SU-8 layer isolates the cells and supports the interconnecting traces. The p-regions are positioned to eliminate the possibility of a short.

MICRO-FABRICATION PROCESSES FOR SOLAR CELLS

We proposed two methods of processing to fabricate solar cell arrays. Both of the methods involve the formation of aluminum interconnects on top of an insulating SU-8 channel in order to connect the cells in the array. In the first method, the p-n junction is created first and the channels are formed after. In the second method, the channel is created before the p-n junction is doped and diffused. This method requires an additional cycle in the furnace. See Appendices A and B for full process descriptions. The choice in final method was based upon the inherent risks present in each method.

RISK AREAS

The first method had two primary risk areas. First, it would have been necessary to thermally grow an oxide after the boron dopant has been driven in. This could have caused excess diffusion and affected the efficiency of the p-n junctions. Second, the SU-8 in the channels had to be flush with the wafer surface. This would have required a high degree of control in the etch rate of SU-8.

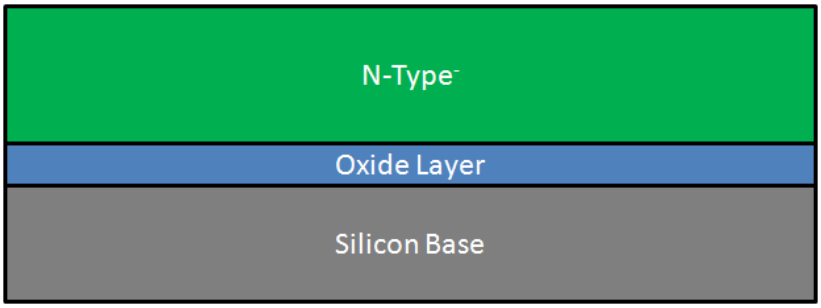
The second method had four areas of concern. The first two were the same concerns as method 1. Third, doping into the channels to create the junctions could have created some leakage current (shorts) between the cells under the SU-8. Fourth, the surface doped in the channel would have been covered in SU-8, which is not optically clear. This could have reduced the viable junction area, which could reduce the electrical performance of the cells.

CONCEPT SELECTION

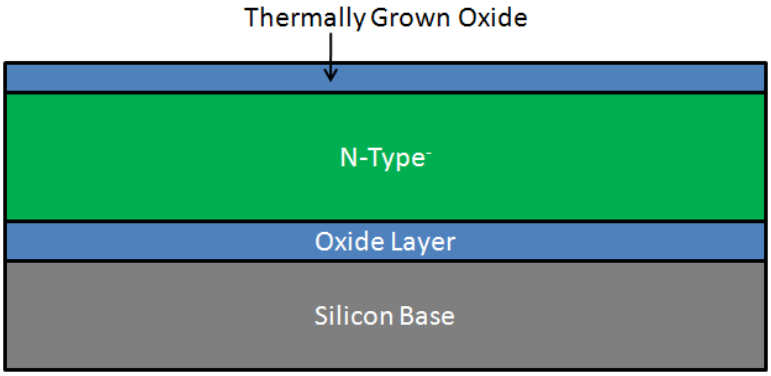
The first process presented fewer risks so it was chosen as the desirable process. The process was implemented to create a two cell module with some success and will be optimized to create the final design.

DESCRIPTION OF SELECTED MANUFACTURING PROCESS

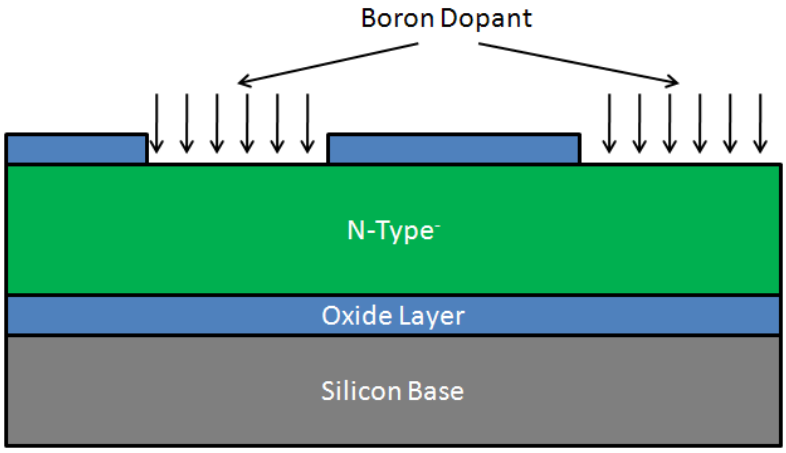
We begin with a SOI (silicon on insulator) wafer. To start with a clean surface the wafer is submerged in Piranha at 70 ℃ for 10 minutes to remove organic particles. From there, the wafer is placed in the buffered oxide etchant (BOE) for 30 seconds to remove the native oxide and then placed into the spin, rinse, and dry to clean and dry. This would produce a cross-section like the one shown below.



Once we have properly cleaned the wafers, an oxide is grown on the surface of the wafer. This is achieved by wet oxidation in which the wafers are placed in a furnace at 1050 ℃ for 2.75 hours in an O_2 atmosphere (during the heating and cooling process N_2 in pumped through the horizontal furnace to maintain an inert atmosphere). This creates a cross-section like the one shown below.

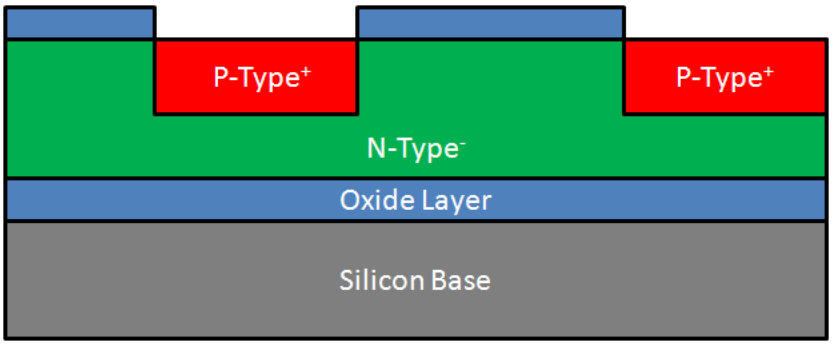


The oxide is then patterned to create exposed regions. To begin the patterning process, we cleanse the wafer. The cleansing process includes a dip in Piranha at 70 ℃ for 10 minutes, a BOE dip for 10 seconds to remove any contaminants from the surface of the oxide, and a spin, rinse, and dry. The wafer is then placed on the spin coater and 3mL of primer are placed on the surface. The spin coater runs for 30 seconds at 300 rpm followed by 20 seconds at 3000 rpm. The spin coater is then stopped and 4-5mL of room temperature photoresist is added. The spin coater is then run for 20 seconds at 200 rpm, 10 seconds at 500 rpm, and 5 seconds at 300 rpm. The wafer is placed on a hotplate for 60 seconds at 90℃. This removes some of the solvent present in the photoresist to make the polymer more photosensitive. The wafer is exposed in an aligner, with mask #1, for 24 seconds and developed for 4 minutes. The wafer is hard-baked on a hot-plate at 150 ℃ for 60 sec. The exposed oxide is removed by submerging the wafer in BOE for 22 minutes. Once the wafer is inspected to confirm the oxide is gone, the photoresist is removed in resist strip, held at 60 ℃, for 5 min and then spin, rinse, and dry. This would produce a cross-section like the one shown below.

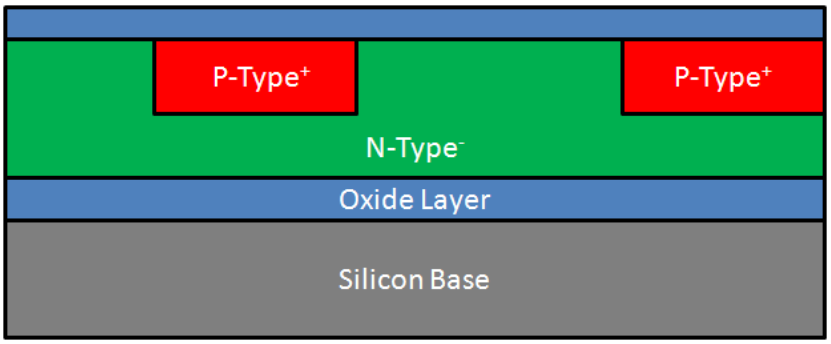


The p-type doped regions are created by doping boron in the exposed regions created by mask #1. We begin by cleaning the mask with a Piranha clean and spin, rinse, and dry. The dopant is spun with the spin coater run at 20 seconds at 200 rpm, 10 seconds at 500 rpm, 10 seconds at 2000 rpm, 20 seconds

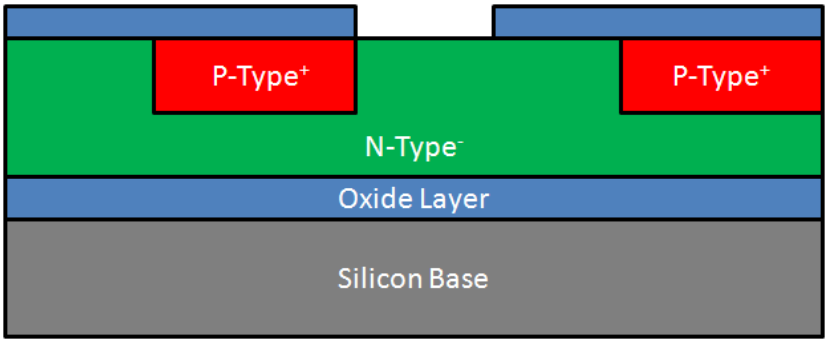
at 3000 rpm, and 5.5 seconds at 300 rpm. This wafer is then baked on a hot plate for 5 minutes at 200 ℃. The pre-dep diffusion of boron is done by dry oxidation in a horizontal tube furnace. The wafer is placed in an oxygen atmosphere at 1050 ℃ for 90 minute to achieve a cross-section like the once below.



Next, the remaining oxide is removed by submerging the wafer room temperature BOE for 22 minutes. To drive in the boron and grow an oxide the wafer is placed back in the furnace, under wet oxidation, at 1050 ℃ for 1.25 hours to achieve a wafer like the one below.

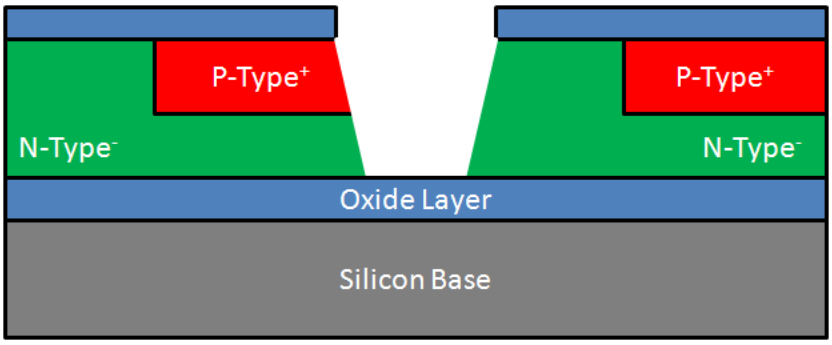


The channels to isolate the separate pn-junctions are created with a second mask. In this process, room temperature primer and photoresist are added to the surface of the wafer using the same process parameters as explained previously. Again, the wafer is exposed in the aligner for 24 seconds and developed. The exposed oxide is removed in a BOE bath for 22 minutes then a Piranha bath for 10 minute to create a cross-section shown below.

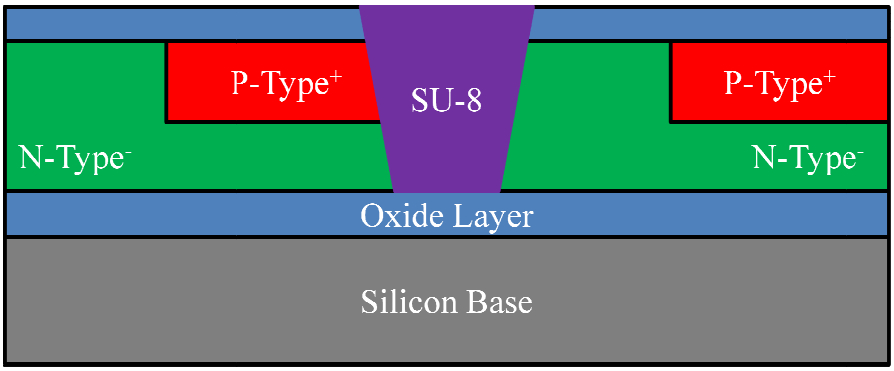


The channel through the silicon is created by deep-etching the silicon at 130 ℃, stirring at the solution with a stir bar set at 2, for 25 minutes. The wafer is etched at a rate of 30 microns/hour. For our wafers,

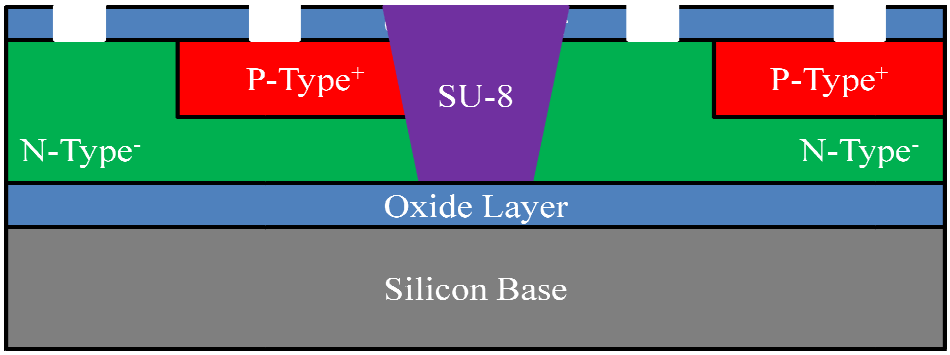
the etching stops once it reaches the oxide from the SOI to create a cross-section like the one below. A profilometer is used to verify the depth of the channel.



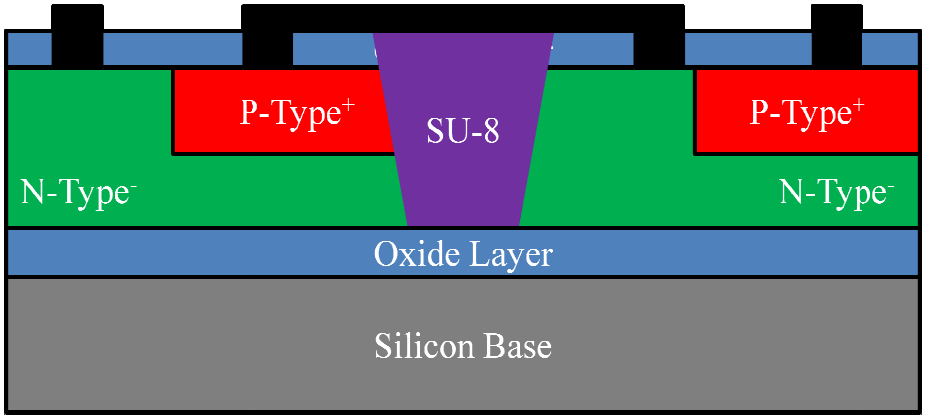
The channels are filled with an insulating material, in this case the polymer SU-8, to prevent short-circuiting between the cells and create a platform for the contact bridge between the cells. SU-8 is deposited by spin-coating the polymer with a spin cycle of 20 seconds at 400 rpm, 40 seconds at 1000 rpm, and 10 seconds at 200 rpm. The wafer is then soft-baked for 5 minutes at 50 ℃ and 10 minutes at 85 ℃. The wafer is then exposed in the aligner, again using the second mask, for 155 seconds. This is followed by a post expose bake at 60 ℃ for 4 minutes and 95 ℃ for 10 minutes to form cross-links in the polymer. The wafer is developed in SU-8 developers for 6 minutes and dried with nitrogen gas to create the cross-section below.



Using a profilometer we can characterize the height. To achieve an acceptable smoothness the wafer is polished with polishing pads. The pads used achieve 5 microns, 2 microns, 1 micron, and 0.5 microns smoothness. The lip of the SU-8 in polished until the lip is below 2 microns high like the cross-section shown below. Contact vias are then created through the oxide layer to the doped silicon below. The vias create an exposed area for an aluminum contact while keeping an oxide to provide insulation.



The aluminum contacts are deposited using a sputtering system. The wafer is placed under vacuum overnight to remove contamination then sputtered for 30 minutes with a power of 90 Watts. The aluminum is patterned using the same photoresist process described above but without adding the initial primer. The wafer is exposed for 15 seconds in the aligner with a third mask then developed for 2 minutes and baked on a hot plate at 150 ℃ for 60 seconds. The aluminum is removed by submerging the wafer in aluminum etchant for 2 minutes. After inspection, the photo resist is removed with resist strip for 3 minutes to leave the final product, shown below.



Now the cell is ready for use (Fig. 7).

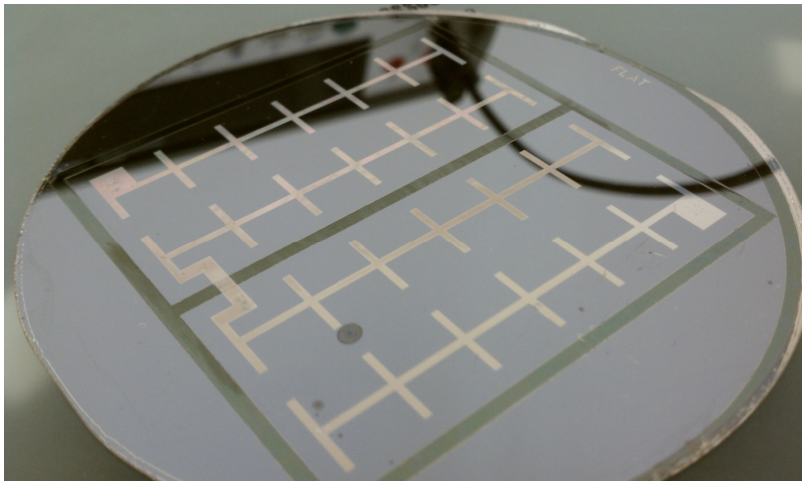


Figure 7: The completed 2-cell device.

TESTING METHODOLOGY

Once a wafer has been fabricated it needs to be tested to determine if the device meets our specifications. The performance goals for the solar cell arrays are to produce a total voltage of 2.5-6.0 volts and a total current of up to 20-30 milliamps. The testing methodology, therefore, defines a test that determines if the devices meet the performance goals and allows comparisons between separate solar cell arrays and individual modules.

Current/voltage curves were be plotted in order to determine the power output of the devices. In this procedure, a solar cell was placed under a quartz halogen light source to simulate the sun. The light source used for testing the two-cell devices had two light output settings: low and high. The light source was placed directly above the solar cell. The solar cell itself was placed directly onto the surface of the table; by placing the solar cell flat, the angle of the light onto the solar cell remained consistent. In addition, the table acted as a heat sink, allowing the solar cell to maintain a consistent temperature throughout testing. The final 12-cell devices were tested using a brighter halogen lamp source with no fiber optics (to reduce losses) that had a variable brightness control.

The solar cell was connected to the instrumentation using a 2-wire connection to reduce lead resistance errors. Alternatively, separate metal traces could also be sputtered down to facilitate the soldering of test wires to the cells. The measurement instrument used was a a Keithley 2400 SourceMeter connected in parallel with a variable load resistor and the solar cell to create the test circuit in Figure 8.

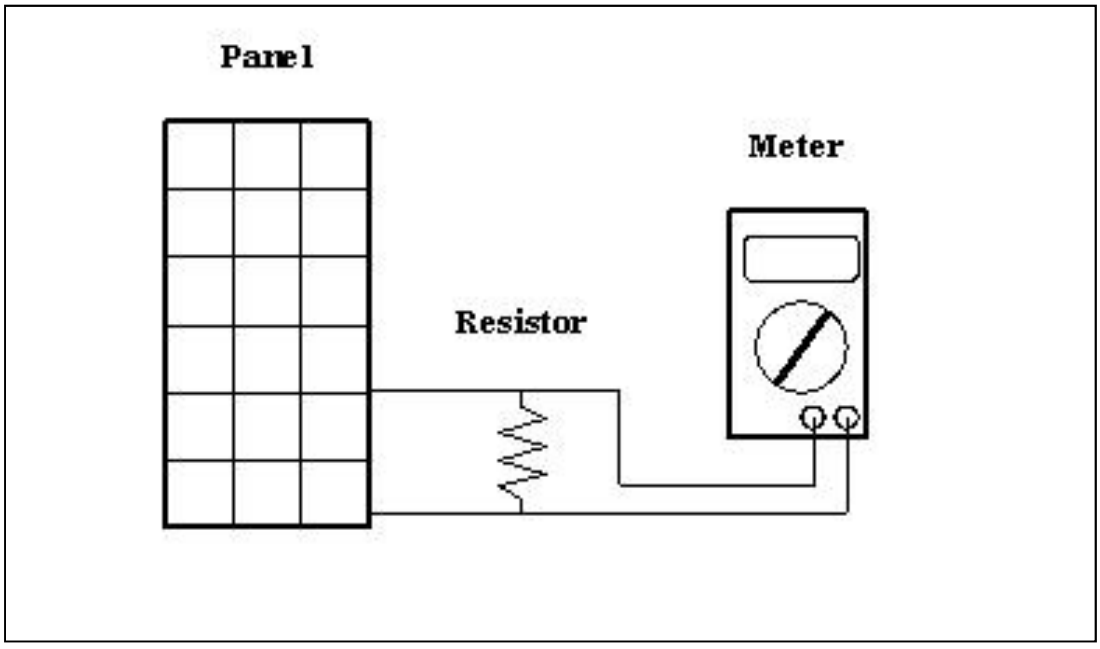


Figure 8: Method used to test solar cells.

This circuit was be used to measure the current and voltage created by radiance from the light source. To begin, the light source was turned on to its lowest setting and the lowest variable load will be used. The instantaneous voltage and current was then measured and recorded. Then the load was increased. The new instantaneous voltage and current was measured and recorded. The voltage and current was measured for every load. The data will be presented in a table for both low and high light levels (Fig. 9).

Light Level 1			
	Voltage	Current	Power
Open Circuit			
10 Ω			
5 Ω			
1 Ω			
Short Circuit			

Figure 9: Representation of data table for solar cell testing. Similar tables will be used for all light levels tested.

The voltage and current at each point was then collected in order to create an I-V curve. This curve provides the short circuit current, I_{SC}, the open circuit voltage, V_{OC}, and the max power, P_{max} (Figure 10).

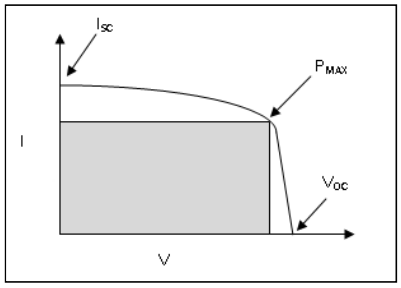


Figure 10: The maximum power achievable in the circuit can be calculated by multiplying the voltage by the current.

The fill factor is the second most important parameter of solar cell performance, after efficiency. The fill factor is the ratio of maximum power to open circuit voltage multiplied by short circuit current ($P_{Max}/(I_{SC}*V_{OC})$). It measures the energy yield of a PV cell, and is generally greater than 0.7 for a commercial solar cell.

2-CELL DESIGN

RESULTS OF OVERALL VOLTAGE, CURRENT, AND POWER FOR 2-CELL DEVICE

Theoretical

Ideally, a solar cell acts as a current source. As can be seen in Figure 24, the diode in parallel with the current source turns on at the p-n junction at approximately 0.5V. When this happens, the current shorts through the diode and ceases to flow to the load. In Figure 11 that can be visualized as the current dropping to zero at the diode turn on voltage.

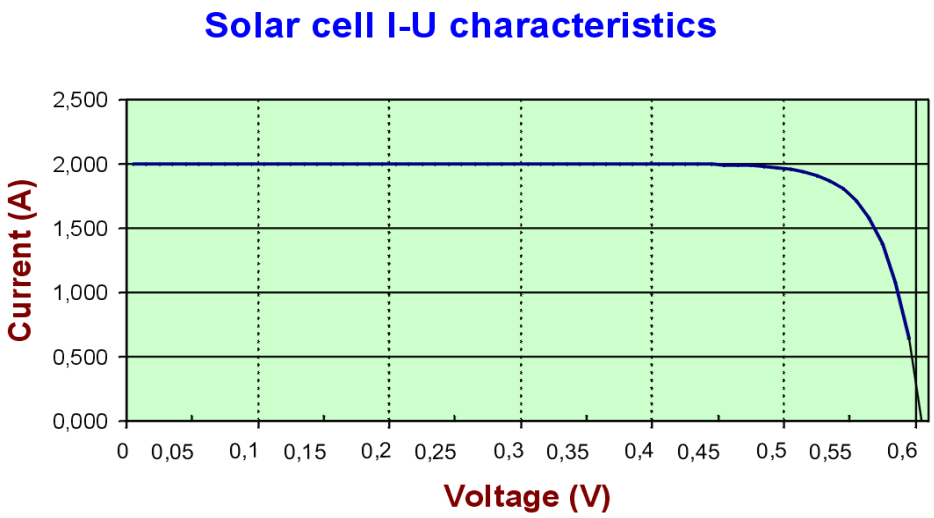


Figure 11: Theoretical current vs. voltage graph of a single solar cell. (ignore values when comparing to multi-cell but graph should keep same basic shape)

The maximum power occurs at the knee of the graph in Figure 11. At that point, the voltage and current are such that the power (P=V*I) is at its maximum value (Fig. 12).

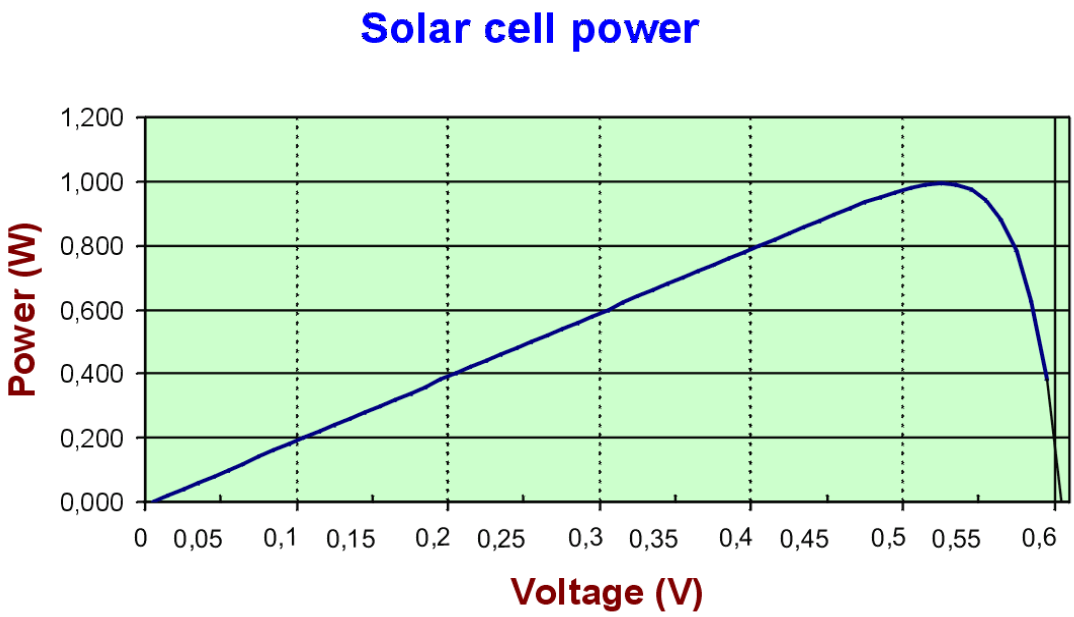


Figure 12: Theoretical power vs. voltage graph of a single solar cell. (ignore values when comparing to multi-cell but graph should keep same basic shape)

Experimental

We measured both the 2-cell device as a whole and each cell individually to compare the performance relative to the theoretical.

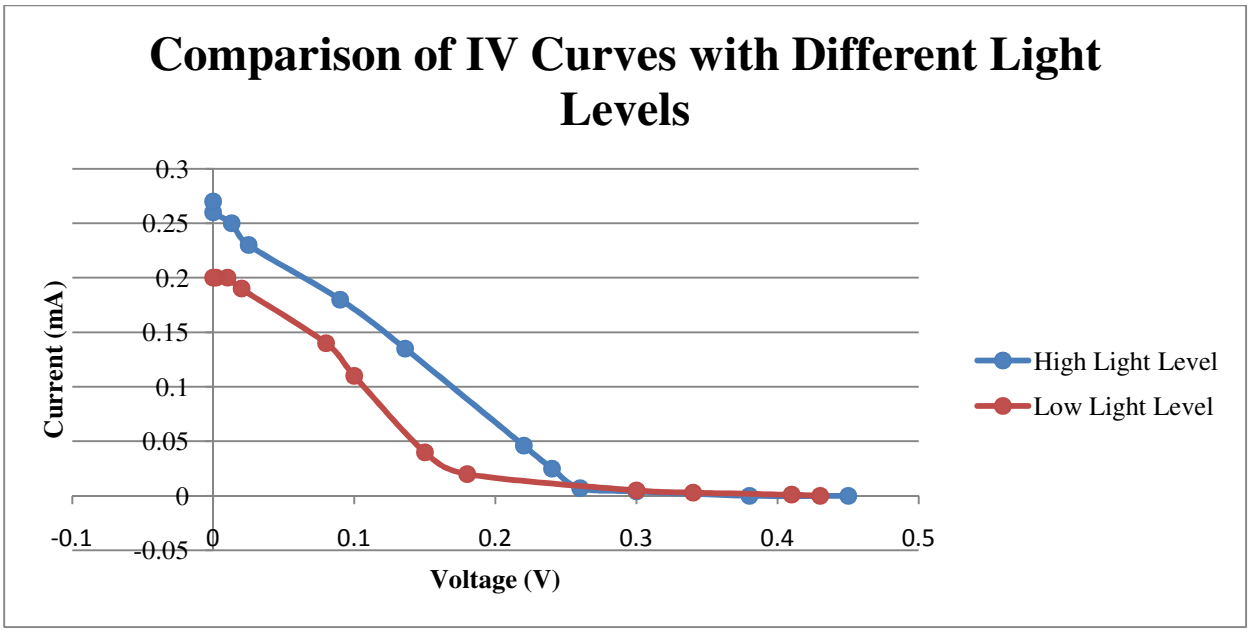


Figure 13: Comparison of IV Curves with Different Light Levels.

The low light level decreased the maximum current by about 20%, as is expected for a solar cell. The shape (being a straight line) differs greatly from the theoretical graph. This indicates a low shunt resistance present within the solar cell.

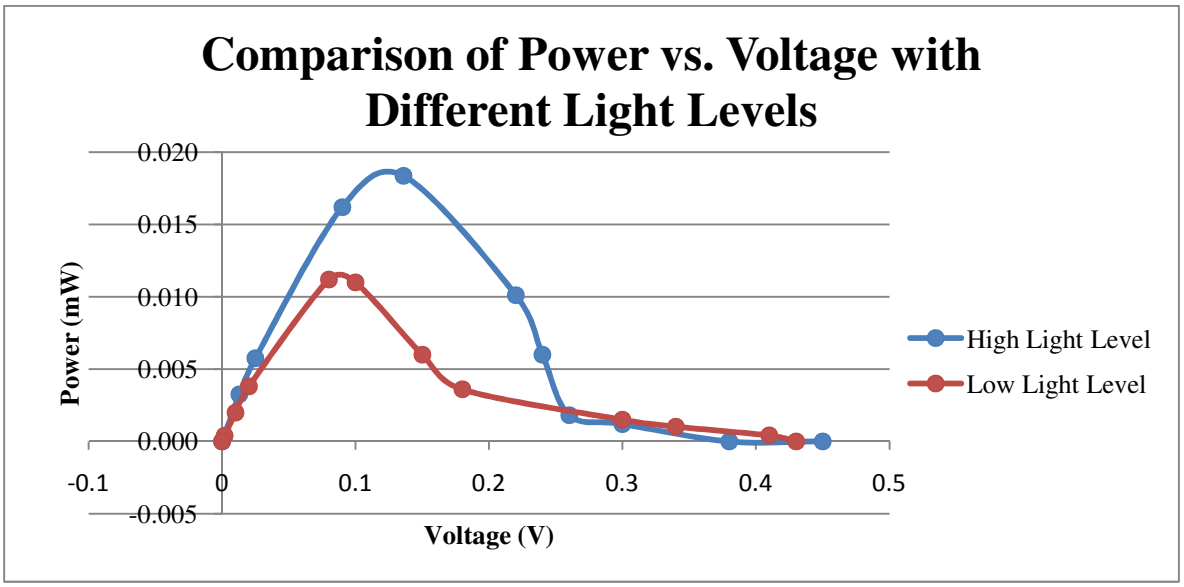


Figure 14: Comparison of Power vs. Voltage with Different Light Levels.

The low light level decreased the maximum power by about 40%. These results emphasize the importance of full illumination of the cell while taking measurements. The shape of the graphs at varying light levels stays pretty consistent which is encouraging, although they differ greatly from the theoretical plots.

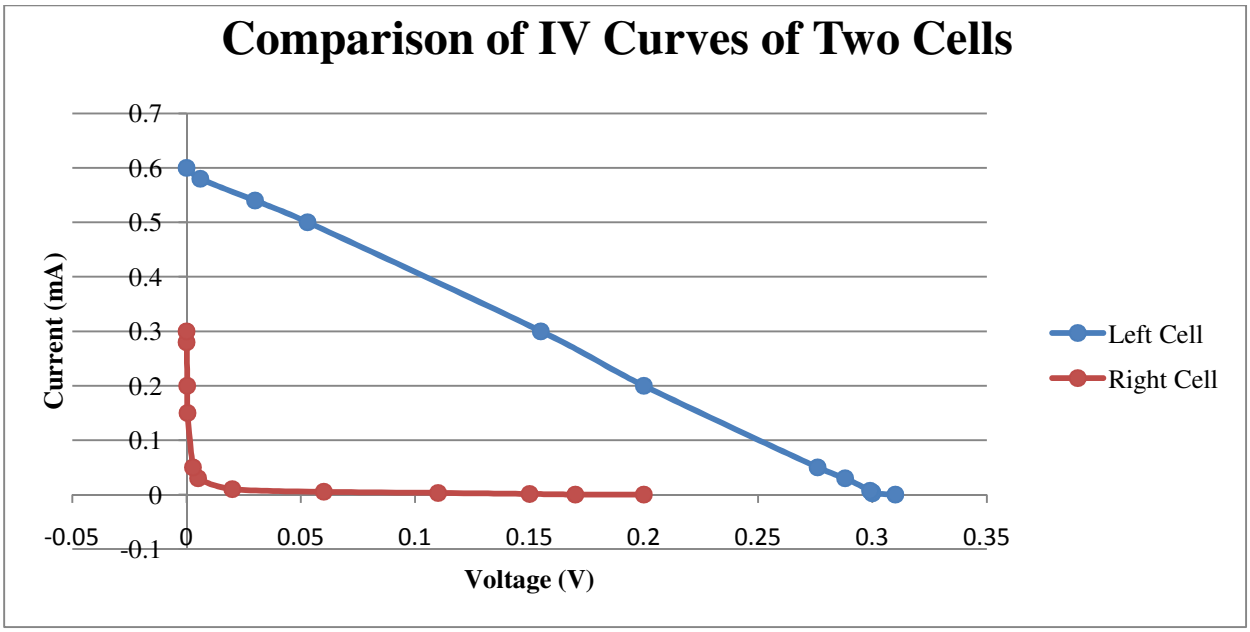


Figure 15: A comparison of the current and voltage of the left cell to the right cell

The left cell came fairly close to producing the current and voltage anticipated from the results of the single cell design. However, the right cell did not. Since these are connected in series, the right cell is crippling the entire device.

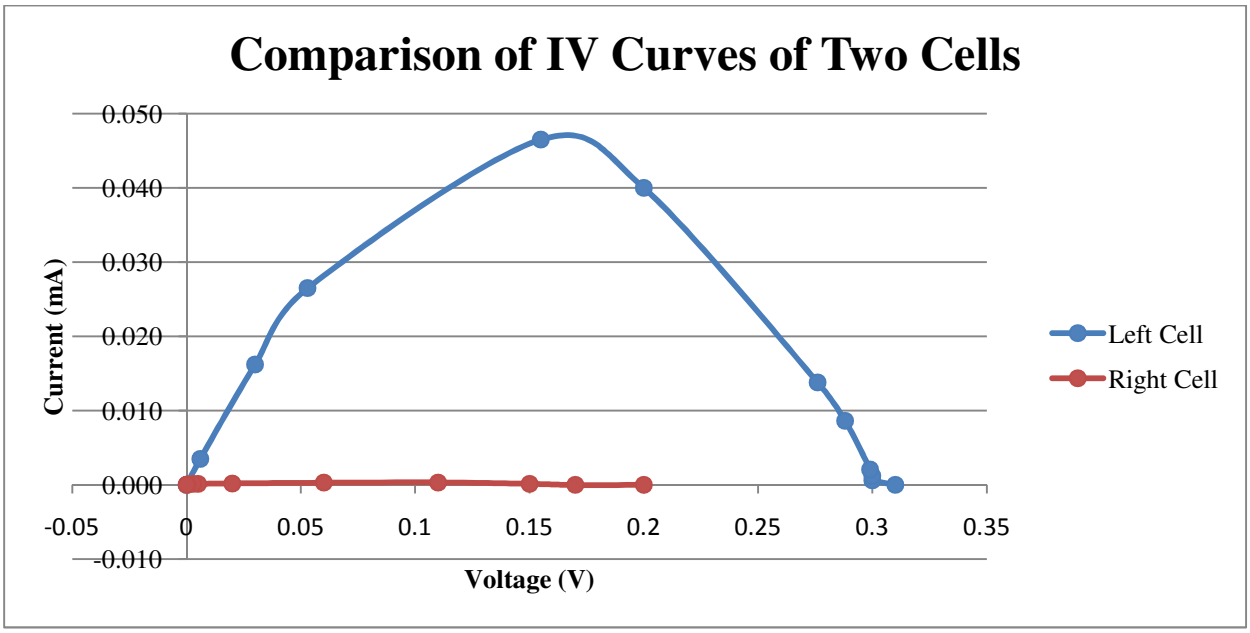


Figure 16: A comparison of the power and voltage of the left cell to the right cell

The power produced by the right cell is negligible, which cripples the entire device. We need to further investigate possible causes of this to ensure it does not happen in the 12-cell device.

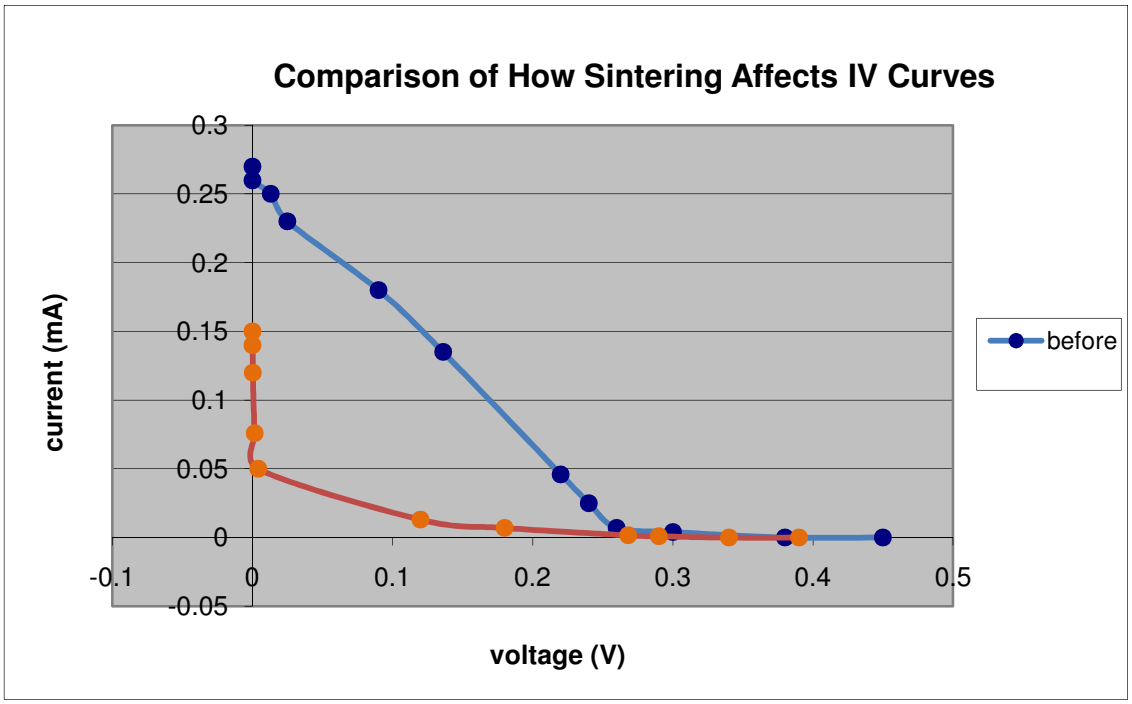


Figure 17: Current vs. voltage of the 2-cell device after sintering

Sintering drives the aluminum contacts into the silicon slightly which theoretically decreases the contact resistance therefore increasing current. Our results did not reflect this, so we are going to investigate this process further. It is possible that the sintering degrades the SU-8 insulating layers in some harmful way.

PROBLEMS AND POSSIBLE SOLUTIONS

Current

The first problem we needed to tackle was the lack of current being produced by the cells, especially in the right cell. One possible solution to this problem was to create a passive layer, a layer of oxide on top of the exposed junction area. This could have decreased the current leakage through the silicon and directed most of the current to the contacts instead.

Another solution was to reduce contamination during the aluminum deposition process. To start, we needed to create a clean surface to sputter on. We tested the effect of SU-8 in BOE and found that the etchant had no effect on the polymer. Therefore, we could submerge the processed wafers in BOE to eradicate the native oxide that formed on the surface without affecting the polymer's ability to isolate the individual cells. By removing any oxide present, we increased the contact quality, allowing more current between the aluminum contacts and the wafer's surface.

Once the wafer surface was clean, we could pump down the aluminum sputtering chamber overnight rather than for one hour. By creating a better vacuum, the amount of contamination present decreased which in turn decreased the amount of contamination in the aluminum contacts. In addition, aluminum could be sputtered simultaneously with silicon. By using an aluminum source that is already saturated with silicon, the diffusion between the wafer and aluminum would be reduced. This could prevent junction spikes from shorting and possibly increase the current (Figure 18).

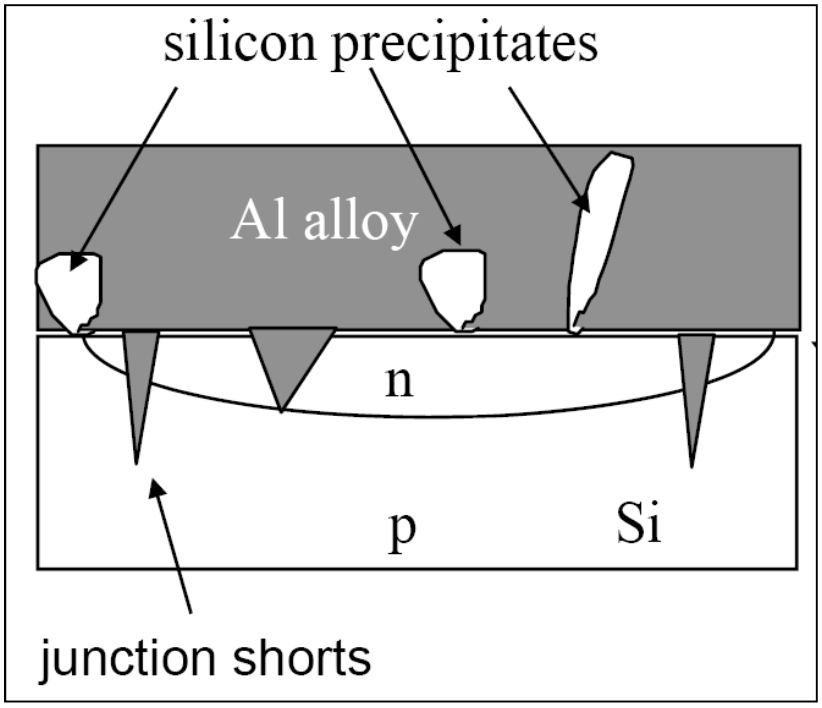


Figure 18: Diffusion between silicon and aluminum can create spikes through the doped region to create shorts. (Source: Dr. Savage MatE430 Lecture Slides)

Once the aluminum contacts have been created, they can be sintered. In this process, the wafer is heated at a low temperature (<450 ℃) to allow limited diffusion between the aluminum and the surface of the wafer. This lowers the resistance between the contact and the surface, reducing the power loss from resistance. However, the effect of sintering on SU-8 is still unknown. While sintering is useful in single solar cells, our two-cell wafer's performance was reduced after sintering. Our two-cell device was sintered and exhibited a decrease in performance, as of yet in our lab no advantage is seen to be gained from sintering.

Voltage in Right Cell

The testing of the individuals cells in our two cell device showed a clear distinction in performance between the two cells. The right cell produced greatly reduced voltage and current values. To increase the uniformity and performance of all the cells on the wafer, we needed to be extremely careful and consistent during the micro-fabrication process, ensuring each process is done cleanly and without contamination. In particular, we needed to make sure the oxide was completely etched off all of the exposed junction regions before doping. This ensured that an even junction depth was created during diffusion.

Internal Shunt Resistance

Internal shunt (R_p) resistance is caused by defects in the structure. The defects allow electrons to flow along the edge rather than solely through the aluminum contacts. These defects acts like many small shorts, reducing the current as the electrons move through paths parallel to the aluminum. In an ideal circuit the internal shunt resistance is infinite, causing all of the current to flow through the aluminum contacts. The R_p can be calculated empirically by determining the slope of the I-V curves. Our data from both cells at the high light level yields an internal shunt resistance of 2.1 kΩ. When testing the cells, the load resistance is varied up to 100 kΩ. Because the internal shunt resistance is much lower than the load

resistance, the majority of current is lost as it chooses the path of least resistance of 2.1 kΩ. Methods for correcting and measuring shunt resistance are still being explored in the lab.

FINAL 12-CELL DESIGN

DESCRIPTION OF DEVICE

The final design solution was designed to produce ~20mA of current at ~2.5V-3V, thus being able to charge a standard hearing aid rechargeable battery. Since the theoretical average output voltage of a silicon p-n junction is 0.5V, this output level requires that between three and six cells be serially connected. However, our initial testing performed on the one cell and two cell devices indicated that due to quality limitations in Cal Poly's clean room and losses in the connections between cells, our cells would put out approximately half of their theoretical maximums. Thus we chose to include 12 serially connected cells in our final design. The designs for the masks that were used to create the final design are shown below to highlight the various design features.

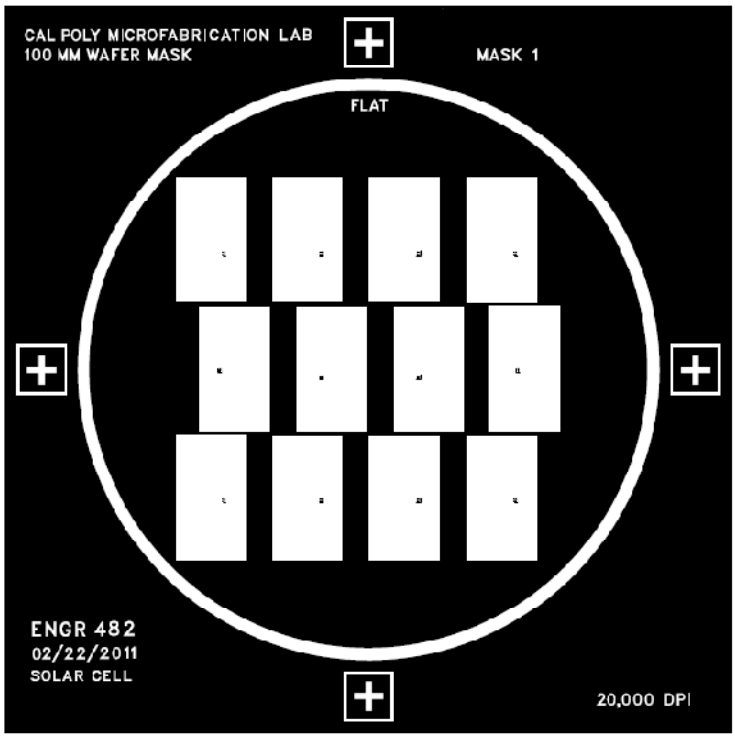


Figure 19: Mask for creating the junction areas.

The current produced in the early designs was an issue, being an average of 10x less than theoretically possible. Current production is proportionate to exposed junction area, junction consistency and contact quality. In our final design, the total junction area was decreased by approximately 33% as compared to the two-cell device (see Fig19). The masks were designed with the junction area covering the majority of the cell to increase cell current production and overall performance.

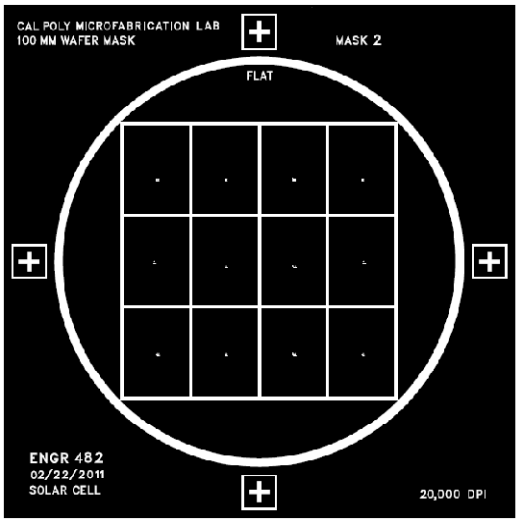


Figure 20: Mask for creating isolating grooves between cells.

Other measures were taken to reduce loss in the system based on the inspection and analysis of previous devices and their performances. For example, the grooves isolating the cells (Fig. 20) were increased from one millimeter to two millimeters wide. This reduced opportunities for resistive defects in the bridges between cells. Also, exposure marks were included in each cell to aid in troubleshooting performance issues and will allow us to locate possible problems at each alignment step.

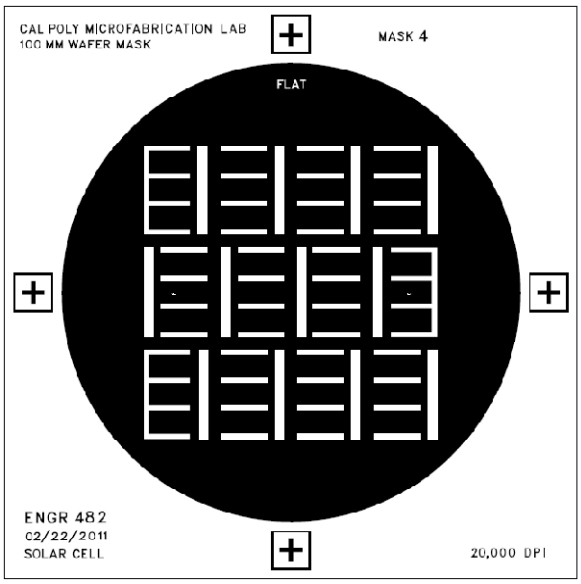


Figure 21: Mask for patterning oxide for aluminum contacts.

A fourth mask (Fig. 21) was added to the 12-cell process design in response to the resulting current of the 2-cell design. In the 2-cell process the aluminum contact was sputtered directing on the silicon. In an attempt to increase current, an oxide layer was left between the silicon and aluminum. A fourth mask, shown above, was added to pattern the oxide. This was done to allow the aluminum to contact only at the exposed regions, hopefully decreasing the chance of junction spikes and other

defects, thus increasing the current. The effect of this design feature was tested with successful results on a single-cell device before applying it to the final design.

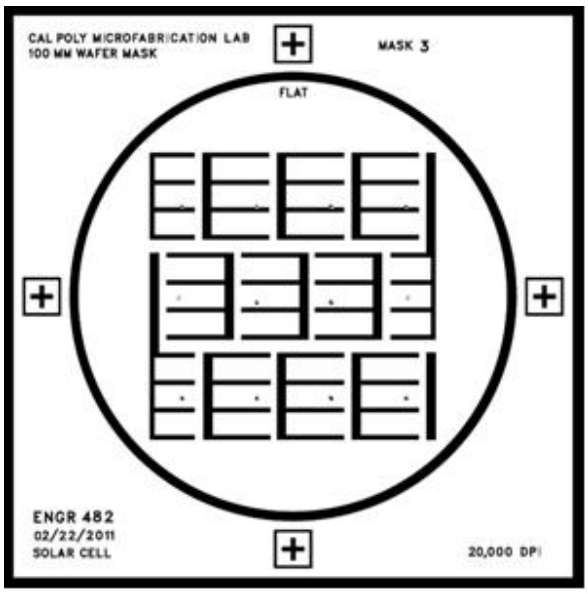


Figure 22: Mask for creating contacts to serially connect all 12 cells.

Also, several bridges per cell (in parallel) were used to connect the cells together (Fig. 22), giving the system redundancy protection against disconnects and reducing the resistance between cells to that of the lowest resistance bridge. A simple cross section of two cells and the general layout from the final design is seen below (Fig. 23 and 24).

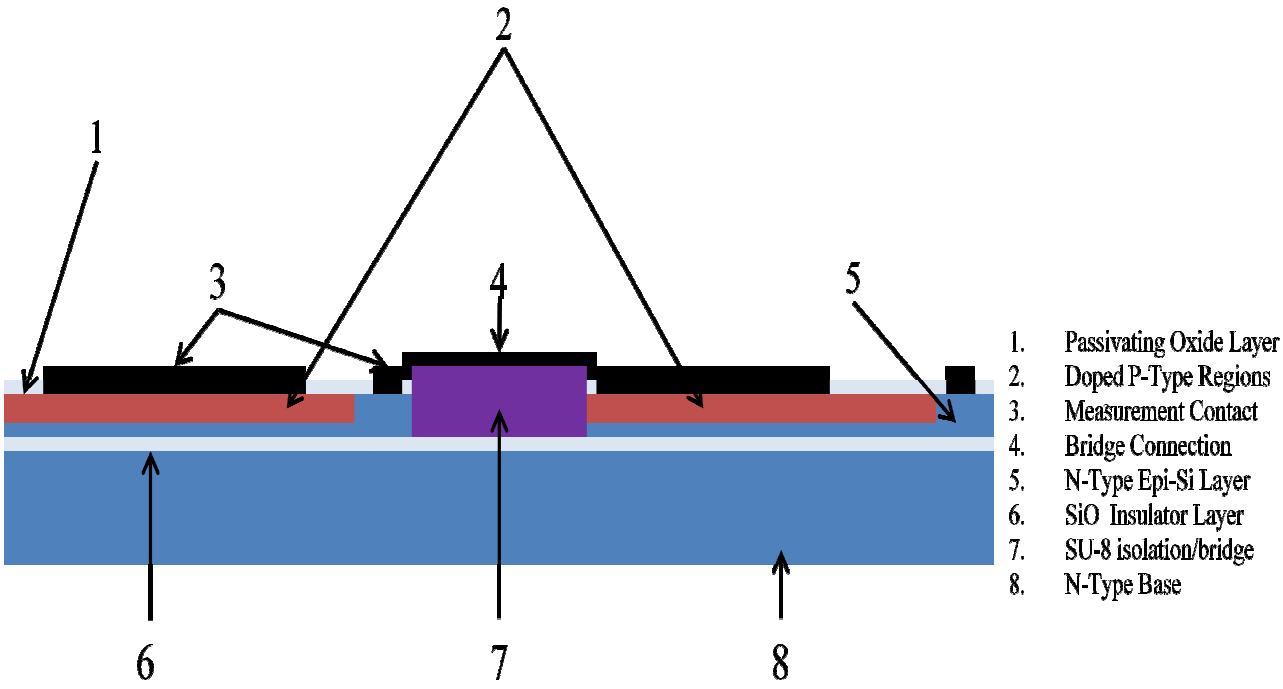


Figure 23: Cross sectional view of two cells in the final design.

The cross sectional view displays all of the improvements over the two-cell module, the thinner bridge between cells, passivating oxide layer, larger proportional junction area per cell, deeper junction depth, and higher quality aluminum contacts. Note that the SU-8 bridge rises above the oxide layer. While this is not ideal, it was found that some amount of extra material always extended above the surface. However, careful grinding with fine sanding paper (2 µm grit) was proven to be effective in minimizing the amount of material rising above the oxide layer and the "sharpness" of its profile. The overall layout (Fig. 23) of the final design included the change in contact design, which was meant to maximize charge carriers collected and junction area exposed. Also visible are the multiple bridges seen in Mask #3 above.

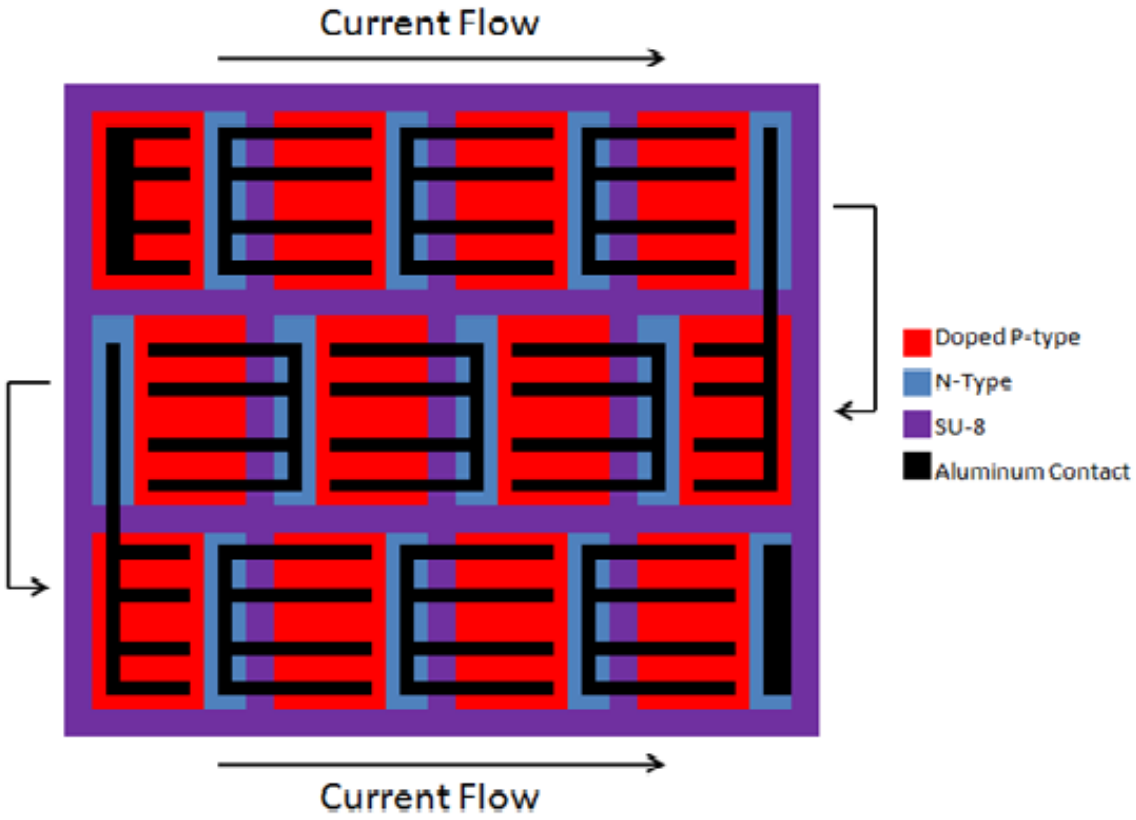


Figure 24: Top view of the overall layout of the cells.

RESULTS OF OVERALL VOLTAGE, CURRENT, AND POWER FOR 12-CELL DEVICE

We fabricated four 12-cell devices in order to increase the number of data points that could be collected. Of the four, only Wafer 1 exhibited complete low resistance (<50Ω) interconnection. In the 12-cell design we chose to make the aluminum "bridges" half as wide as they were in the 2-cell design. We did this so that we could use more than one bridge between each cell, however it turns out that the thinner aluminum traces are much more likely to contain a defect than wider ones. For the other wafers, we painted over the bridges with colloidal silver to reduce resistances and fix circuit discontinuities. Wafer 2 produced no voltage or current due to alignment issues during the creation of the isolation trenches between cells. Wafer 3 and Wafer 4 both required us to fix some of the aluminum "bridges" with colloidal silver. The current-voltage curve for Wafer 1 can be seen in Figure 25.

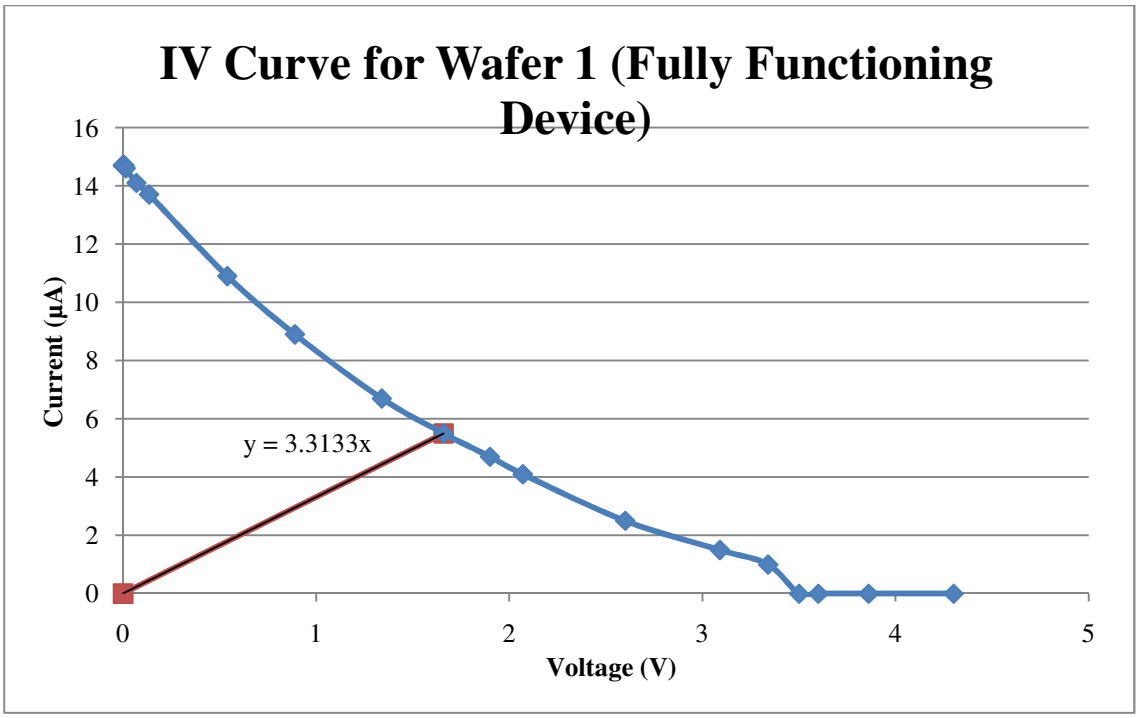


Figure 25: IV characteristic for wafer 1

The maximum power point is at (I=5.5µA, V=1.66V) and is approximately 9.8µW. The inverse slope of a line drawn from the maximum power point to the origin is proportional to the internal resistance of the solar module 301.8kΩ. The fill factor for wafer 1 is 0.144. The power vs. voltage curve for Wafer 1 can be seen in Figure 26.

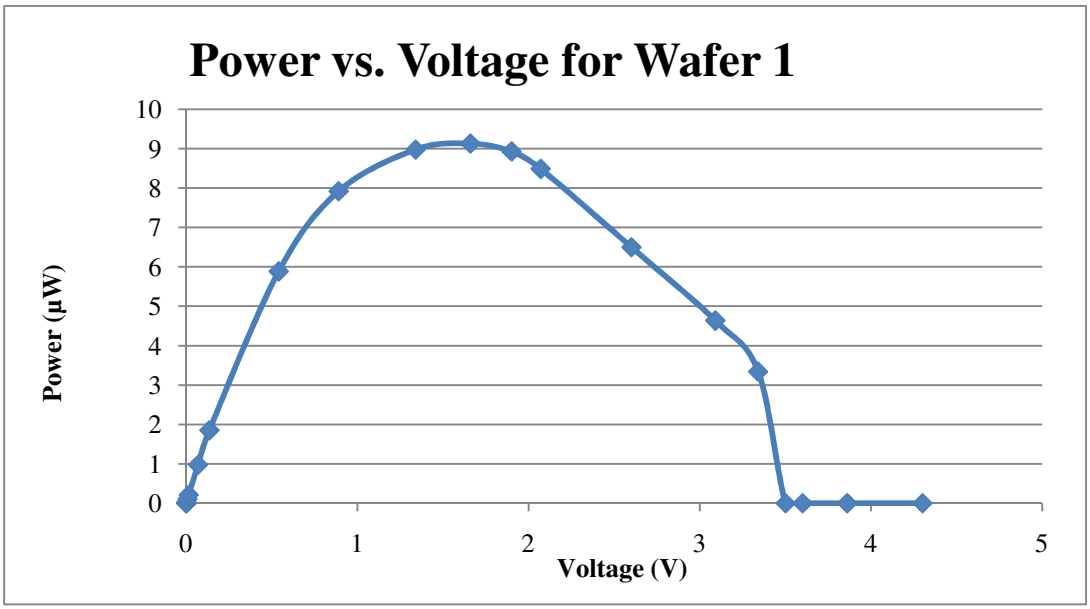


Figure 26: Power vs. Voltage for wafer 1

The shape of this graph is fairly close to that of the 2-cell device, although it still differs greatly from the theoretical plot. Once the two faulty bridges were fixed with colloidal silver, Wafer 4 worked the best out of all three functioning devices, so we compared the I-V characteristic of Wafer 4 under our test light and outside on a sunny day (~25℃) (Figure 27).

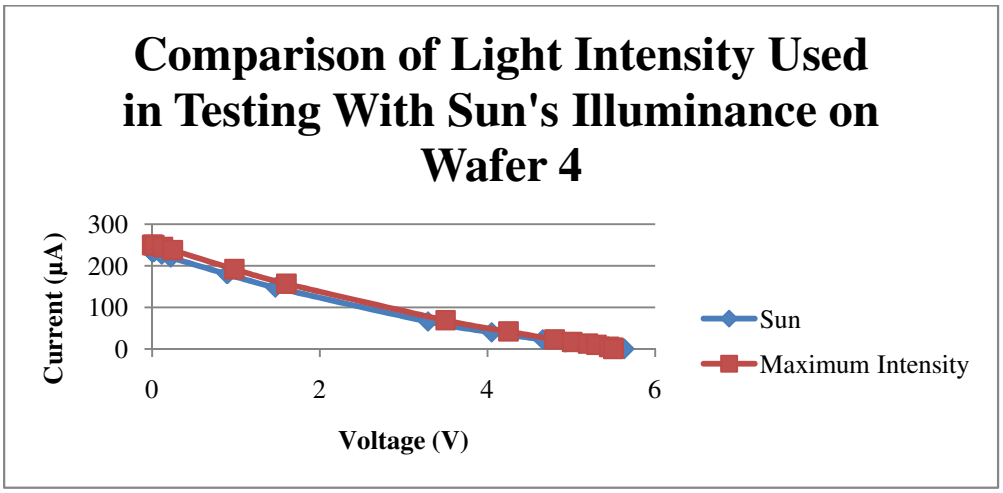


Figure 27: IV curves of the test light used in lab and the sun.

The maximum power of wafer 4 was reduced by 15% under the illumination of the sun when compared to its performance under the lamp's maximum light output level. However, both curves lack the shape of the ideal curve, indicating that electron-hole generation is not being caused as it should be. Figure 28 shows the power vs. voltage plots for all three functioning wafers. It can be seen that the shape of the graph remains relatively the same, even though Wafer 4 performs more ideally than the other two devices.

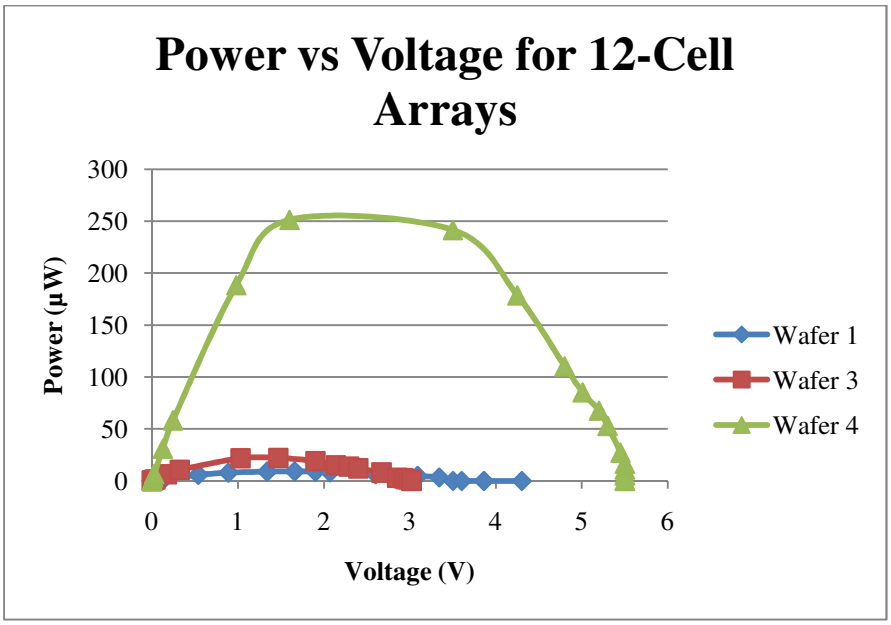


Figure 28: Power vs. Voltage for the three functioning wafers.

The same is also true for the IV plots (Figure 29).

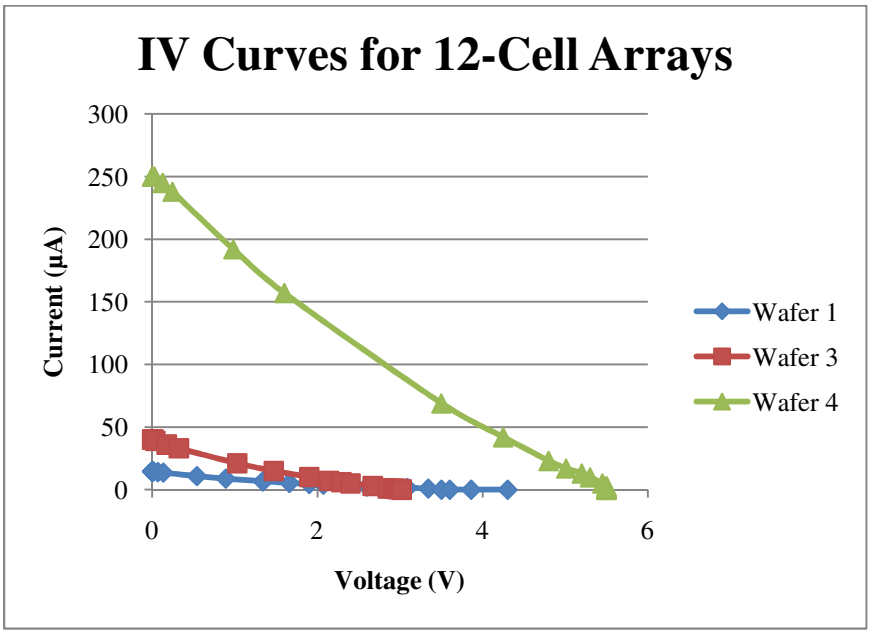


Figure 29: IV plots for the three functioning wafers.

The maximum power point for wafer 3 is at 22µW (I=15µA, V=1.47V) and a fill factor of 0.18. Wafer 4 had a maximum power of 251µW (I=157µA, V=1.6V) and a fill factor of 0.183.
The charging times for a 30mAh battery and summarized performances are shown in Table II.

Table II: Summary of wafer performance.

Wafer	Successful Bridges	Max Voltage (Open Circuit)	Max Current (Short Circuit)	Max Power	Charging Time (hours) (for 30mAh battery)
1	11/11	4.3 V	15 µA	9.8 µW	2000
2	0/11	N/A	N/A	N/A	N/A
3	0/11	3.0 V	40 µA	22 µW	750
4	9/11	5.5 V	240 µA	251 µW	125

ANALYSIS OF 12-CELL DEVICES

Theoretically, 12 cells in series should produce about 6V due to each cell producing 0.5V. We designed the 12-cell devices to produce ~2.5V-3V with 12 cells in series according to the losses observed in the 2-cell wafers. However, due to the extra care we took in the manufacturing process, we got a maximum of 5.5V out of wafer 4. Wafer 4 also produced the maximum current at 240µA and maximum power at 251µW. Even at maximum current, it would still take wafer four approximately 125 hours to charge a 30mAh battery, which is far too long. The current produced by these wafers needs to be increased by at least a factor of 10 in order to charge the batteries in any reasonable amount of time. Even though wafer 4 worked the best, it did require some colloidal silver paint to fix two failed bridges. Wafer 1, the only wafer which functioned without additional processing, was also the worst performing

wafer electrically. This leads us to assume that the bridge connections still contain high amounts of resistance and higher quality contacts.

ELECTRICAL SYSTEM OF THE DEVICE

Figure 30 shows the equivalent circuit diagram of the solar cell and test load. The two parasitic resistances we had to battle with are the series and shunt resistances. To obtain a graph as close as possible to the theoretical current-voltage plot, we wanted to minimize the series resistance and maximize the shunt resistance.

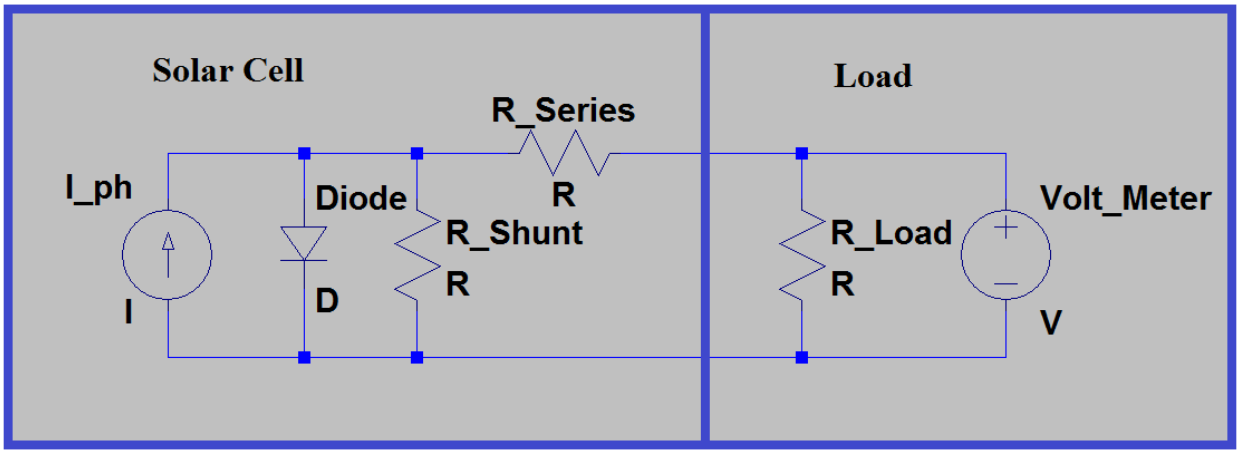


Figure 30: Circuit diagram of solar cell and test load.

Overall voltage and current for 1-cell device

Solar cells optimally generate approximately 500mV per cell. The current produced is proportional to the junction area and is about 35mA/cm^2. The average current produced by the single solar cells produced in our lab is about 2mA. The junction area of the full wafer single cells is approximately 38cm^2. This means that ideally, the single cells should produce 1.3A of current which is 650 times higher than the 2mA actually generated.

Overall voltage and current for 2-cell device

In our 2-cell design our junction area was approximately 9.6cm^2, therefore the theoretical current generated should have been 336mA. The maximum current measured turned out to be only 0.25mA which is 1344 times smaller than theoretical. This means that our 2-cell design was performing about half as well as the single cells.

Overall voltage and current for 12-cell device

In our 12 cell design the junction area was 3.12cm^2 which is theoretically capable of an optimal current of 109mA (using the two-cell device performance as a baseline measurement). This current would be sufficient to charge a battery, however extrapolating from our previous data, we calculated that the actually current generated would be about 0.1mA. In reality, our functioning, non-augmented 12-cell device produced 0.0098mA. This was much smaller than the theoretical and extrapolated estimations. The current is too small to charge a battery in a reasonable amount of time.

Safety, maintenance, and repair considerations

Chemical safety is a key concern in the micro-fabrication lab. The most severe risk is hydrofluoric acid (HF) which is used to etch silicon oxide. HF makes up part of the buffered oxide etchant (BOE). This acid is severely harmful to humans; exposures to 2% of the body's surface have proven to be fatal. During exposure, the acid penetrates the tissue, ultimately reacting with calcium in the bones creating toxic levels of calcium ions.

Solar cells cannot be repaired. Therefore, extreme care must be taken during initial manufacturing. Human contamination is the largest source of error in micro-fabrication. Controllers are required to wear proper attire, including gloves, lab coats, hair nets, and safety glasses during the entirety of the process. During and after the fabrication process, the wafer can be protected by housing it within plastic containers to reduce contamination and chances of breaking.

DISCUSSION OF RESULTS

The voltage of 5.5 V achieved by Wafer 4 indicates that the individual cells are working properly and performing close to expected levels. This means that there are depletion regions being created with near ideal widths. However, the lack of sufficient current could be explained by several theories:

- First, too few photons with high enough energy to create electron-hole pairs are reaching the p-n junctions. This would most likely be due to the junction depths being too deep (as a result of spending too long in the diffusion furnace).
- Second, the distance from the junction to the contacts is too great. This would mean that the mean free path (average distance traveled by an electron before being reabsorbed by a hole) of the generated electrons is too low for the majority of the current to reach the contacts on the surface of the wafer. This could be due to the contacts being spaced too far apart.
- Third, the overall resistance between cells is too high. This resistance would mainly be located between the contacts and the silicon, and because the cells are in series, the resistances for each cell could be adding to a value high enough to suppress, in large part, the generated current from the cells.

While the current produced by our wafers is far too low to accomplish our objective of charging a battery in 8 hours or less, the voltage produced on all of the wafers indicates that we have reached our objective of connecting integrated solar cells on a silicon wafer. The resistance requirement of <50Ω were met on Wafer 1 and nearly met on Wafer 4 (which was fixed with colloidal silver paint). We were able to dimly light a small LED with Wafer 4, but not with the other wafers. Overall, we have solved the interconnection problems from previous projects and taken strides in understanding the factors that affect cell performance.

Final embodiments of this design would differ from our prototypes in contact and junction quality, which would negate the need for performance-enhancing steps such as the colloidal silver paint and create devices with uniform performances.

PROJECT PLAN

The project was split into three main portions: literary research and creation of a simple 1-cell photovoltaic, the fabrication and testing of a 2-cell device, and the fabrication and testing of a 12-cell device. The simple cell and initial research was done during fall quarter. The 2-cell was created during winter quarter, during which we addressed many processing issues that were discovered during

fabrication. The 12-cell device was created spring quarter. The completed tasks are shown in a Gantt charge in Appendix D.

FUTURE RECOMMENDATIONS AND CONCLUSIONS

The purpose of this project was to confirm the processing technique for bridging multiple cells and to provide further information on how processing affects the current and voltage derived from each cell. This project embodied two main areas: the design of a processing method to connect the cells during a micro-fabrication process and the creation of an array that produces enough voltage and current to power low-power applications like a hearing aid battery recharger. We have produced a method (with an attached SOP) (Appendix E) for the first objective and were successful in our attempts to connect integrated solar cells. Our devices do produce the necessary voltage for recharging a hearing aid battery; however, the current produced is lower than needed for a reasonable charge time. After testing and obtaining results from each wafer we have come up with future recommendations in order to help future teams solve some of the problems we encountered while working on this project.

Design masks with wider aluminum traces

Creating thinner aluminum traces on our 12-cell wafers allowed us to create more than one bridge on each cell but these bridges were more likely to contain defects. The broken bridges were temporarily fixed by painting a coat of colloidal silver on top of the broken bridges. This temporary fix could possibly be avoided with wider aluminum bridges.

Different metal as traces

Aluminum was the primary metal used as a trace material on each cell. A different metal, such as gold, could be used instead. The highly conductive and non-oxidizing properties of gold could create better results within wafers by preventing junction spikes and decreasing resistance within the traces.

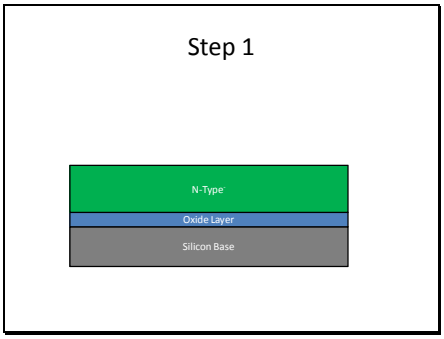
Experiment with shallower junctions

Shallower junction depths would theoretically allow more photons with enough energy to create electron hole pairs to reach the p-n junctions by reducing the mean free path required of the incident photons, thus increasing the current.

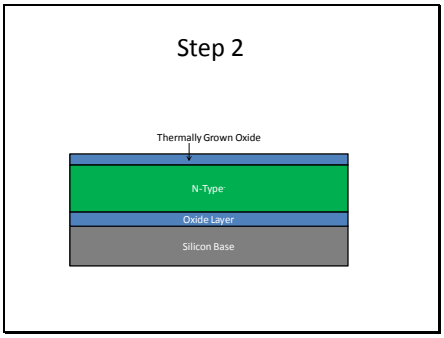
Use modeling to determine the optimum cell area and contact area/shape

Through experimentation, a balanced creation between contact areas and exposed areas can be done. Since current produced is proportional to the cell area but contact area determines the path length generated electrons and holes must travel to be used, a careful balance of cell area and contact area must be achieved. Also, consider the distance from the junctions to the contacts as the mean free path of electrons in silicon is limited (we have not characterized this for our wafers) and any current generated at a junction must migrate to a nearby contact in order to be collected to flow through the circuit.

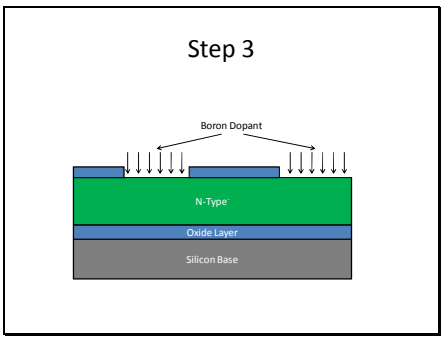
APPENDIX A: PROCESS 1



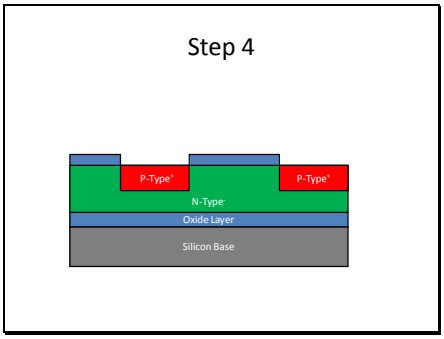
Purchase SOI wafers with n-type doped silicon.



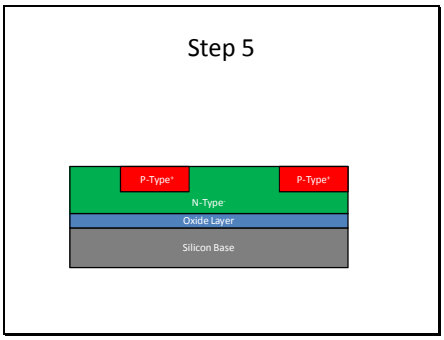
Thermally grow an oxide layer on top of the n-type silicon.



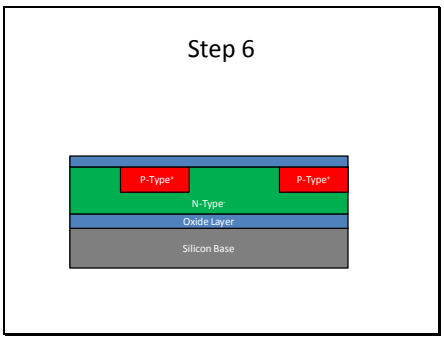
Mask the oxide layer and etch to create an exposed area for the p-type doped regions.



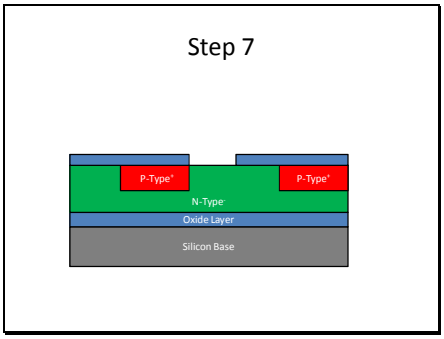
Spin on and diffuse boron to create the p-type regions.



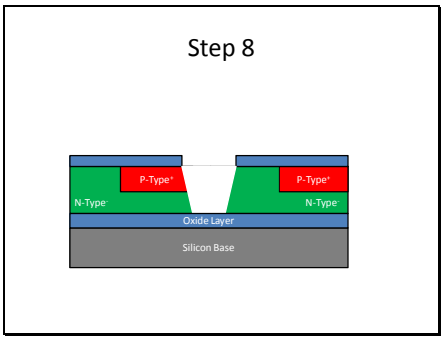
Etch off the oxide layer (if needed).



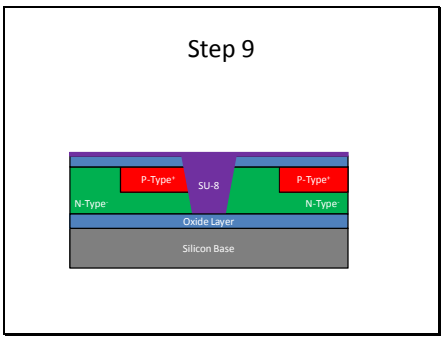
Grow another oxide layer.



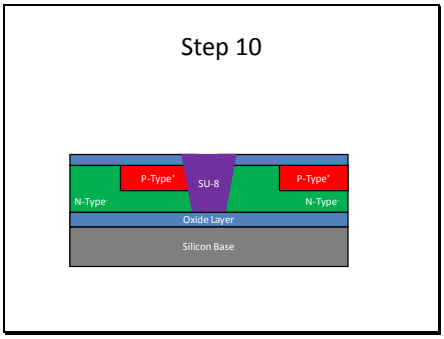
Mask and etch the oxide layer between the cells.



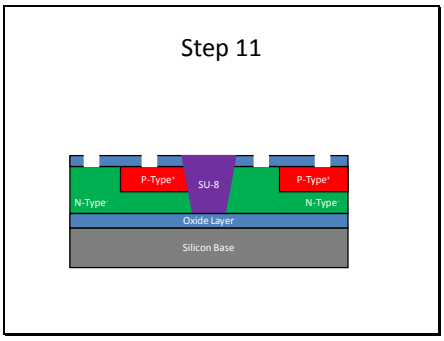
Deep etch the silicon to create the channel for the insulating barrier between the cells.



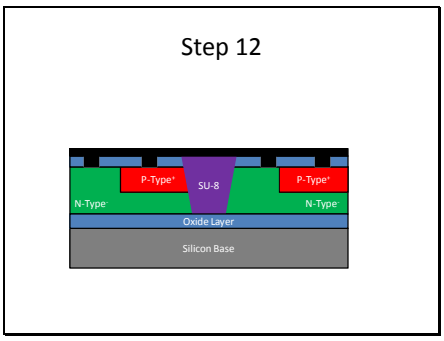
Spin on SU-8 to act as the insulator between the cells.



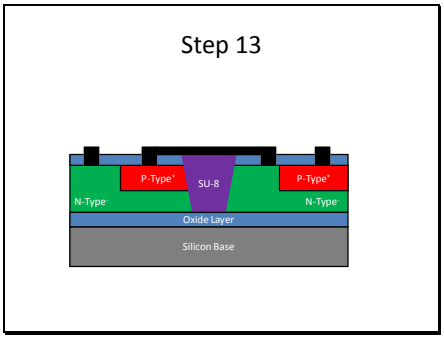
Remove the SU-8 that is on top of the oxide layer. This process is one of our major risks. We have to remove just enough to eliminate the residual SU-8 on top of the oxide layer but not so much that it cuts into the insulating channel.



Mask and etch the oxide layer to create the contact points.

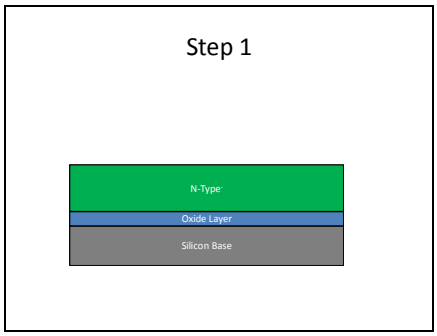


Sputter on aluminum to create the interconnects.

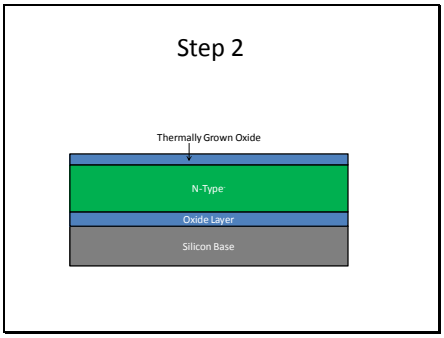


Pattern the aluminum traces to create the finished product.

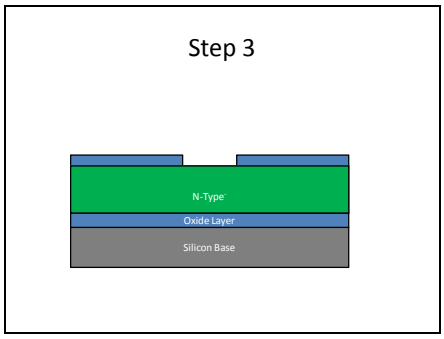
APPENDIX B: PROCESS 2



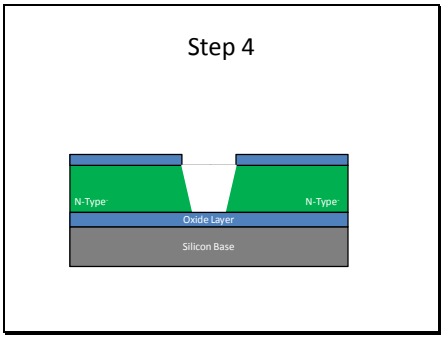
Purchase SOI wafers with n-type doped silicon.



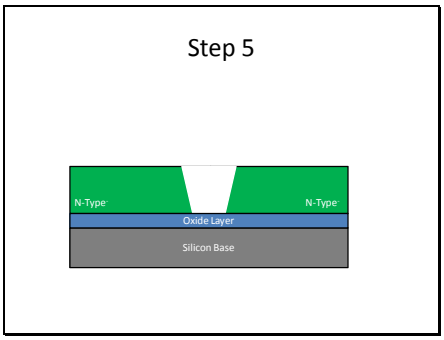
Grow an oxide layer on top of the n-type silicon.



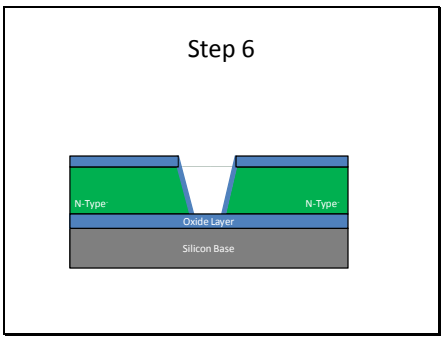
Mask and etch the oxide layer in anticipation of creating an insulation barrier between the cells.



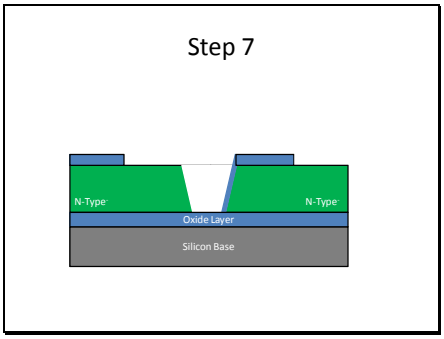
Etch the silicon to create the hole for the insulating barrier between the cells.



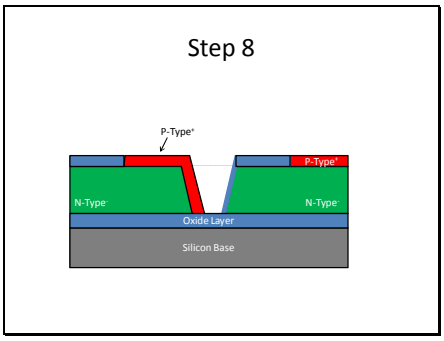
Etch off the oxide layer.



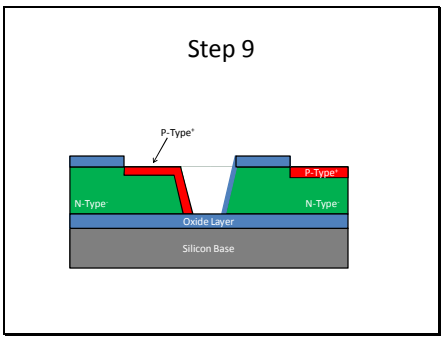
Grow another oxide layer.



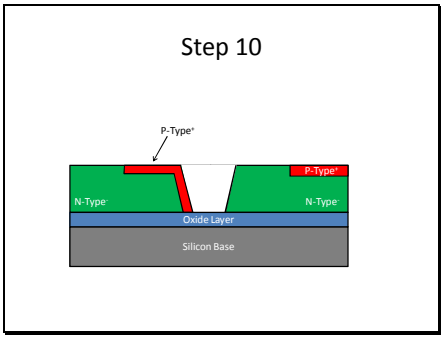
Mask and create an oxide layer to leave only the p-type doped regions exposed.



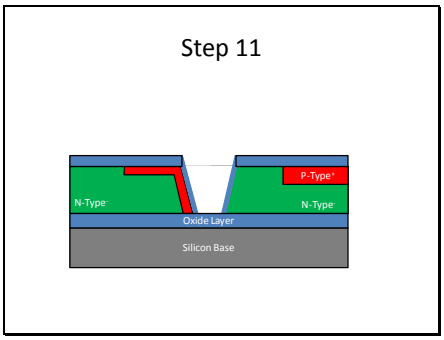
Spin on boron.



Diffuse boron to create the p-type regions.

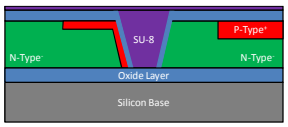


Etch off the remaining oxide layer (if needed).



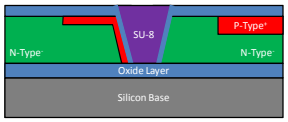
Grow another oxide layer.

Step 12



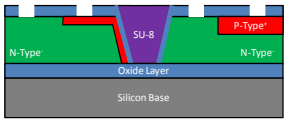
Spin on SU-8 to act as the insulator between the cells.

Step 13

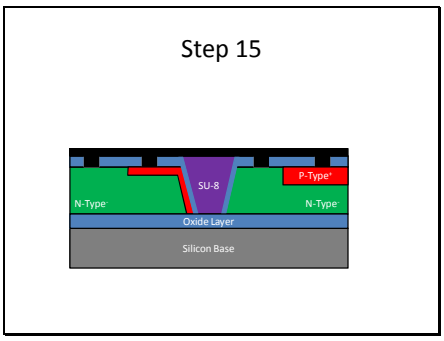


Remove the SU-8 that is on top of the oxide layer. This process is one of our major risks. We have to remove just enough to eliminate everything on top of the oxide layer but not so much that it cuts into the insulating barrier.

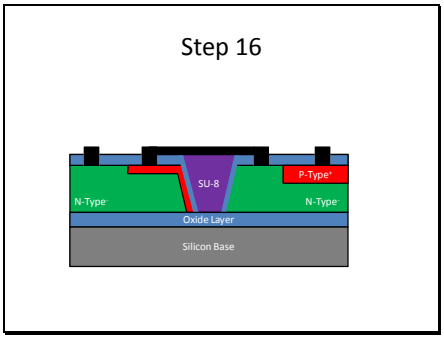
Step 14



Mask and etch the oxide layer to create holes for the aluminum contacts.



Sputter on aluminum to create the interconnects.



Pattern the aluminum traces to create the finished product.

APPENDIX C: REFERENCES

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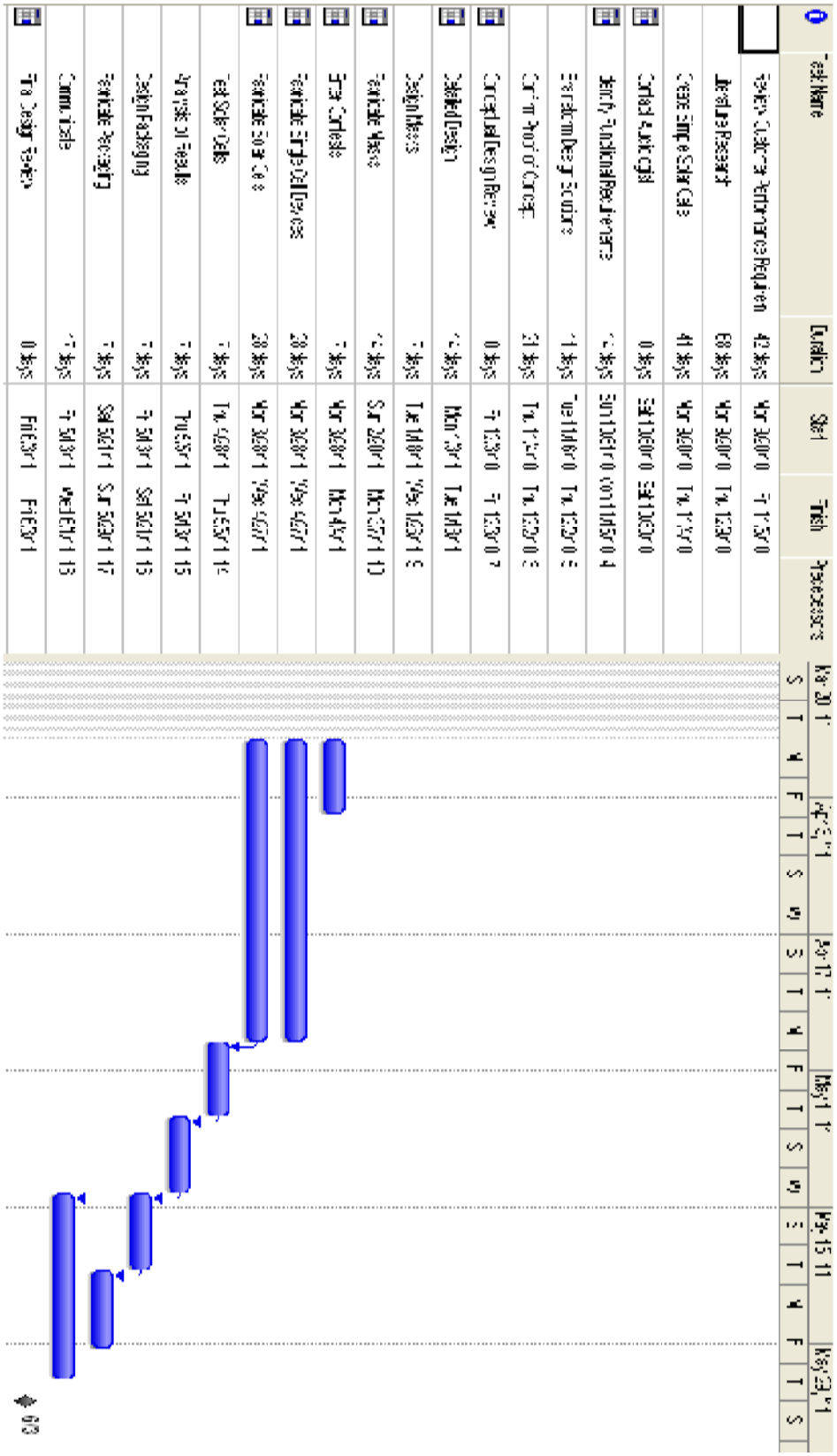
APPENDIX D: GANTT CHART



APPENDIX E: STANDARD OPERATING PROCEDURE

Clean Wafers

1. Piranha at 70 ℃ for 10 minutes
2. Remove native oxide (BOE for 30 sec)
3. Spin rinse and dry

Grow Oxide

4. Turn on Nitrogen until oven reaches 1050 ℃ and then start the O2 and stop the N2. Wet oxidation (top furnace) at 1050° for 2.75 hours (start at 900 to preheat – dials at end should read front 500 – middle 700 – back 500) then wait for an hour. Once the oven reaches 900 ℃ set dials to front 750 – middle 850 – back 500
5. Take out photoresist for next day
6. Take out boron dopant for next day

Mask #1

7. Turn on diffusion oven to 1050 ℃ (front 500 – middle 700 – back 500) until the oven reaches 600℃. At 600℃ turn on N2. At 900℃, turn O2 gas on dry
8. Piranha at 70 ℃ for 10 minutes
9. BOE dip for 10 sec
10. Spin rinse and dry
11. Spin on primer and photoresist (stop after step 2 to apply PR) – (1. 30sec-300rpm 2. 20sec-3000rpm 3. 20sec-200rpm 4. 10sec-500rpm 6. 5sec-300rpm)
12. Softbake at 90℃ for 60 sec (then chill)
13. Expose in aligner (light intregal 6.0)
14. Develop for 4 min
15. Hardbake at 150 ℃ for 60 sec
16. Etch oxide in BOE for 22 min
17. Resist strip at 60 ℃ for 5 min
18. Spin rinse & dry

Dopant Regions

19. (Same Day)
20. Spin on dopant (1. 20 sec - 200rpm 2. 10 sec – 500 rpm 3. 10 sec – 2000rpm 4. 20 sec-3000rpm 5. 5 sec-300rpm)
21. Bake at 200 ℃ for 5 min

Diffusion

22. Once furnace reaches 900℃, turn on O_2 gas (dry) and load wafers.
23. Increase furnace temp to 1050℃ (front-750 middle-850 back-500)
24. Cook for 90 minutes.
25. Switch to N_2, turn off furnace.

26. Switch off gas at 700℃.
27. Let cool overnight.
28. Strip remaining oxide in BOE.
29. Oxidize wafer in oven for 1.25 hr at 1050℃.
30. Take out photoresist for next day.

Mask #2

31. Turn on Deep etch system (Temp: 130℃, Spin setting: 2, put rear thermocouple into solution)
32. Piranha at 70℃ for 10 min.
33. BOE dip for 10 sec
34. SRD.
35. Spin on primer and photoresist.
36. Soft bake at 90 C for 1 min
37. Expose under mask #2 in aligner (LI: 6.0)
38. Develop for 4 min.
39. SRD
40. Hard bake 150 for 1 min
41. Etch oxide
42. Resist strip
43. Once deep etch solution reaches ~60℃, insert front thermocouple, turn on lower box, hit circle arrow button 4 times until “run” flashes.
44. Once temp reaches 85℃, insert wafers in brown boat.
45. Etch for proper time (30 micron/hour etch rate).
46. Test depth and roughness in profilometer.
47. Get out SU-8 for next day.

Su-*8

48. Piranha at 70℃ for 10 min.
49. BOE for 10 sec
50. SRD.
51. Spin on SU-8
    a. 20 sec @ 400rpm, 40 sec @ 1000rpm, 10 sec @ 200rpm
    b. Soft Bake: 5 min @ 50℃, 10 min @ 85℃
    c. Align and expose with mask #2 at LI: 60 (manual for 4 mins)
    d. Bake at 60℃ for 4 min, 10 min @ 95℃
    e. Develop for 6 min
    f. Hand dry with N_2 (IPA if needed, no water!)
52. Use profilometer to test SU*8 profile
53. Use 5, 2, .5, and .05 micron paper to smooth bridge areas as much as possible. Polish for hours!, or use machine for 5 mins!
54. Hard Bake: 20 min at 200℃.
55. Take out photoresist for next day.

Contact Holes

56. BOE dip for 10 sec.
57. Spin-on photoresist.
58. Soft bake at 90°.
59. Expose under Mask #4 (contact hole mask).

60. Develop for 4 min.
61. SRD/inspect
62. Hardbake for 60 sec at 150°C.
63. BOE etch for 15 min.
64. Resist strip for 5 min at 60°C.
65. Store wafers under vacuum if needed before sputtering. (Native oxide will render aluminum ineffective.)
66. Get out photoresist for next day.

Aluminum

67. Clean Torr chamber with Piranha.
68. Pump down Torr overnight with wafer inside.
69. Sputter aluminum for 25-30 min @ 90 watts.
70. Remove wafer.
71. Spin on photoresist.
72. Expose and align with mask #3.
73. Develop for 4 min
74. SRD
75. Hardbake 150°C for 60 seconds
76. Use Aluminum etchant 50°C until shape is clear.
77. Strip resist at 60.
78. SRD
79. Test.
80. Pray to the cleanroom gods that it works.