

**NEGATIVE CONDUCTANCE LOAD MODULATION**  
**RF POWER AMPLIFIER**

A Thesis Presented to the  
Electrical Engineering Department of  
California Polytechnic State University,  
San Luis Obispo

In Partial Fulfillment  
of the Requirements for the Degree  
Master of Science in Electrical Engineering

by  
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June 2010

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## ABSTRACT

Negative Conductance Load Modulation RF Power Amplifier

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The number of mobile wireless devices on the market has increased substantially over the last decade. The frequency spectrum has become crowded due to the number of devices demanding radio traffic and new modulation schemes have been developed to accommodate the number of users. These new modulation schemes have caused very poor efficiencies in power amplifiers for wireless transmission systems due to high peak-to-average power ratios (PAPR). This thesis first presents the issue with classical power amplifiers in modern modulation systems. A brief overview of current attempts to mitigate this issue is provided. A new RF power amplifier topology is then presented with supporting simulations.

The presented amplifier topology utilizes the concept of negative conductance and load modulation. The amplifier operates in two stages, a low power stage and a high power stage. A negative conductance amplifier is utilized during peak power transmission to modulate the load presented to the input amplifier. This topology is shown to greatly improve the power added efficiency of power amplifiers in systems with high PAPR.

Keywords: Power Amplifier, Peak-to-Average Power Ratio (PAPR), CDMA, OFDM, Power Added Efficiency (PAE), Load Modulation, Doherty Amplifier.

## ACKNOWLEDGMENTS

This thesis would not have been possible without the extensive support and advice from Dr. Vladimir Prodanov. Much thanks goes to Dr. Prodanov for his patience, guidance, and insight into amplifier design.

I would also like to thank Dr. Cheng Sun and Jeffrey Gerfen for their participation as members of my thesis committee.

I thank the people in the Cal Poly Research and Graduate Programs for their support clerically and financially on this thesis.

A special thanks to my lovely wife, Grace, for her patience with my busy schedule and for her amazing cooking.

I thank my parents and siblings for their continual support throughout my life. I would not have made it to Cal Poly without their encouragement, guidance, and love.

Above all, I thank the Lord Jesus Christ for giving me life and the abundance of blessings that have gotten me here today.

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# **1 Introduction**

The purpose of this thesis project is to design and validate the operation of a new type of RF power amplifier. The amplifier presented is designed to improve the efficiency of power amplifiers in wireless transmission systems that suffer from high peak-to-average power ratios. This thesis presents a guideline for designing the proposed amplifier topology as well as simulation results validating the theory of operation. The focus of this project is for validation of amplifier operation and therefore further study is needed for optimization of the amplifier performance.

## **1.1 Document Overview**

This thesis is comprised of three main sections: a summary of the problems in current technologies caused by signals with high peak-to-average power ratios, a brief overview of current research attempting to mitigate the issues associated with these signals, and the proposed theory of operation of the negative conductance load modulation amplifier with supporting simulation results.

## **1.2 Software Platform**

Agilent's Advanced Design System 2009 Update 1 was used throughout this thesis for high frequency simulation. Harmonic Balance simulations were used for all circuit performance simulations with an order of 10 harmonics. A fundamental frequency of 1.9GHz was used, corresponding to the frequency in many cellular telephone systems.

## 2 Background

Portable mobile devices are becoming more and more common in everyday life.

Consumers have continually driven these technologies to be smaller and cheaper with more applications for wireless connectivity while demanding longer battery life. Due to a sharp increase in the amount of wireless devices, the radio spectrum has been flooded with users and frequency bands have become crowded. New modulation techniques have been developed to allow more users to operate in the same radio band. These techniques have caused unforeseen issues in hardware that arise while trying to keep up with consumer demands, specifically the size and battery life of electronics.

### 2.1 Modulation Techniques

With the rise in portable mobile devices, traditional analog modulation techniques cannot handle the vast number of devices demanding radio communication traffic. These analog techniques rely on frequency and time slots to allow multiple people to communicate with a single point, known as a many-to-one channel. In cellular phone applications using analog modulation, any given cellular area allotted to a single cell tower can handle less than 60 channels, not nearly enough to handle the number of mobile devices in urban areas.<sup>[8]</sup> Spread spectrum modulation techniques were designed to greatly increase the number of available users per cell tower, as well as several other advantageous characteristics.

### 2.1.1 CDMA: Code Division Multiple Access

CDMA is a spread spectrum modulation technique that relies heavily on a pseudorandom spreading code as well as power control among all mobile users. The spreading code deals with the method of modulation and demodulation of data, which will not be discussed in this thesis. However, power control among mobile devices is the driving factor that causes such low efficiencies in traditional power amplifiers. CDMA requires all mobile devices transmitting to a cell tower to transmit at equivalent power levels. Stated differently, “the power at the cellular base station received from each user over the reverse link [mobile-to-tower] must be made nearly equal to that of all others in order to maximize the total user capacity of the system.”<sup>[8]</sup> This means that a mobile device must vary its transmitted power such that, when the RF signal is received at the cell tower, the received power level is the same as all other mobile devices within the same cell.

There are several things that affect the power level received from a mobile device, most of which can be described by Rayleigh fading. Rayleigh fading is “a statistical model for the effect of a propagation environment on a radio signal, such as that used by wireless devices.”<sup>[12]</sup> Therefore, the distance between a mobile device and cellular tower, the absence of a direct line-of-sight between the tower and phone caused by buildings, structures, and terrestrial landmarks, and many other environmental aspects will cause the received power from a mobile device to vary. This leads to the mobile device having a high peak-to-average power ratio (PAPR), putting a huge burden on the efficiency of the mobile device, as seen in section 2.3.

### 2.1.2 OFDM: Orthogonal Frequency-Division Multiplexing

Orthogonal Frequency-Division Multiplexing is a system used often in Wi-Fi, WiMAX, and upcoming 4G wireless communications. This transmission scheme is an ultra-wideband network in which the data to be sent is broken up into several subcarrier channels. This scheme also suffers from poor PAPR levels because the independent phases of the subcarriers lead to constructive interference at various points during transmission.<sup>[11]</sup> This can be seen in Figure 2.1 with just four subcarrier channels resulting in an extremely high PAPR. The more subcarrier channels an OFDM system uses, the higher the possible PAPR will be, resulting in a tradeoff between overall data transfer rates and PAPR values, among other considerations. Note that Figure 2.1 is merely an over-simplified example and therefore the frequency spacing does not accurately represent an OFDM system.

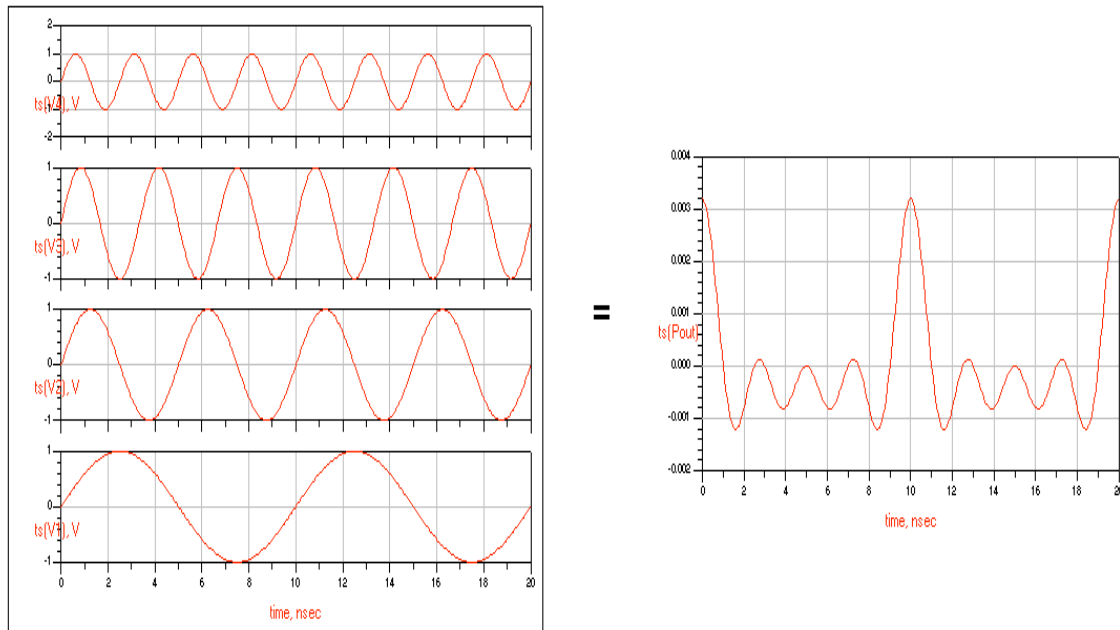


Figure 2.1 OFDM Signal Example Showing High PAPR

## 2.2 Peak to Average Power Ratio (PAPR)

Peak to Average Power Ratio (PAPR), also known as crest factor, is a measurement of the peak amplitude of a waveform divided by the RMS value of the waveform, as seen in Equation 2.1

$$C = \frac{|P|_{peak}}{P_{rms}}$$

Equation 2.1

A few simple examples of PAPR calculations are shown in Figure 2.2.<sup>[9]</sup>

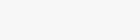
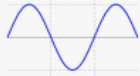
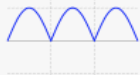



Wave type	Waveform	Peak magnitude (rectified)	RMS value	Crest factor	Crest factor (dB)
DC		1	1	1	0.0 dB
Sine wave		1	$\frac{1}{\sqrt{2}} \approx 0.707$	$\sqrt{2} \approx 1.414$	3.01 dB
Full-wave rectified sine		1	$\frac{1}{\sqrt{2}} \approx 0.707$	$\sqrt{2} \approx 1.414$	3.01 dB
Half-wave rectified sine		1	$\frac{1}{2} = 0.5$	2	6.02 dB
Triangle wave		1	$\frac{1}{\sqrt{3}} \approx 0.577$	$\sqrt{3} \approx 1.732$	4.77 dB
Square wave		1	1	1	0 dB

Figure 2.2 PAPR/Crest Factor Calculation Examples<sup>[9]</sup>

### 2.3 Conventional Power Amplifiers

Single ended class AB power amplifiers are widely used in transmission systems. Class AB amplifiers, as seen in their designation, are a hybrid combination of a class A and a class B amplifier. They are biased at a point between classes A and B, allowing the designer to work with a tradeoff of high linearity (class A) and high efficiency (class B). Class AB amplifiers, like many amplifiers, achieve their highest efficiency when operated near saturation.<sup>[6]</sup> A typical class AB efficiency curve is shown in Figure 2.3.

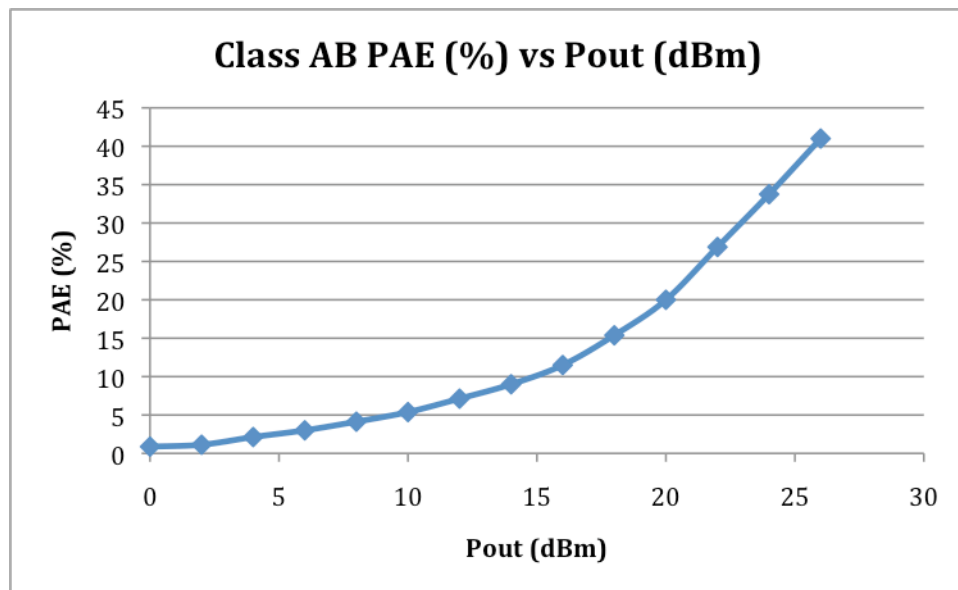


Figure 2.3 Typical Class AB Power Amplifier Power Added Efficiency

These amplifiers have worked well in linear single-sideband (SSB) modulation applications with low PAPR, where low distortion and high efficiency are required. As seen from Figure 2.3 above, the efficiency of an amplifier is high when the output power is closest to the 1dB compression point. However, when modulation schemes have a high PAPR, the amplifier operates at power levels well below the 1dB compression point for a

majority of the time. This translates to average efficiency values as low as 12% in many of the modern transmission systems. For applications such as cellular phones, where the main power draw comes from the RF Power Amplifier, efficiencies of 12% are nowhere near acceptable.

For example, the maximum allowable transmit power from a handheld cellular phone in a TDCDMA system is 21dBm, or 125mW.<sup>[7]</sup> If the handheld device operates a majority of the time at an output back-off (OBO) power of 8dB, then the average output power for the device is 13dBm, or about 20mW. Therefore, while a majority of the time the phone transmits only 20mW of power, at 12% efficiency, the amplifier requires 222mW. This is a huge burden on a battery that has a rating of 720mAh, such as the Nokia BL-4C Li-Ion cell.<sup>[13]</sup> It is because of this poor efficiency that the talk time of cell phones is drastically lower than the standby time.



### **3 Efficiency Improvement Methods To-Date**

Until the recent boom in wireless mobile devices, the issue of signals with high PAPR has almost been non-existent. In recent years, however, there has been a lot of research into methods for improving the efficiency of amplifiers in these systems. Described below are a few of the more popular areas of research; however this is not an exhaustive list of all methods being pursued.

#### **3.1 PAPR Reduction Methods**

One area of interest that has been studied and implemented in current systems is methods for reducing the value of the PAPR. The desire for pursuing this area is obvious, if one can lower the PAPR of a specific modulation scheme, then one would be able to operate the power amplifier closer to its 1dB compression point; thereby achieving a higher average efficiency without any modifications to the amplifier itself.

##### **3.1.1 Software/Coding Methods**

There are several software and coding methods that have been pursued in an attempt to minimize the PAPR of these modulation schemes. These methods include: clipping, block coding, active constellation extension, nonlinear companding transform, partial transmit sequences, and selective mapping. Selective mapping has proven to be a popular area of interest due to its ability to reduce PAPR without additional distortion, however it is useful only in systems such as OFDM that use multiple subcarrier channels.<sup>[14]</sup>

Selective Mapping is a simple concept with a not-so-simple implementation. The

software generates a sequence of statistically independent values related to the available subcarrier channels as well as individual phase sequences. An inverse fast Fourier transform (IFFT) is performed on this sequence, resulting in a map of possible expected output PAPR values for a given set of subcarrier channels and phases. The software then selects the lowest expected PAPR from the sequence. This process requires multiple IFFT operations that in turn require significant computational power and complexity. However, further study is showing alternative methods for computing selective mapping that reduces the computational complexity required.<sup>[14]</sup>

### 3.1.2 Predistortion

The modulation schemes presented above in section 2.1 all require highly linear signals for data transmission. When a power amplifier is pushed towards its 1dB compression point and beyond, nonlinearities are introduced into the signal due to power supply clipping. Because the signals are required to be linear, the amplifier operates well below its 1dB compression point. However, if one distorts the RF signal before amplifying it, or in other words intentionally add nonlinearities to the signal, such that the nonlinearities in the power amplifier are cancelled out, one can operate the power amplifier closer to the 1dB compression point.

Heung-Gyoon Ryu, from Chungbuk National University, Korea, studied the reduction of PAPR using a combination of selected mapping (Software/Coding Method) and a predistorter. He states that “Predistortion is a linearization method in which the input signals are conversely predistorted before the HPA [High Power Amplifier]. Through the

predistortion and nonlinear HPA, the overall characteristic can be linearized.” From his study, he was able to reduce the PAPR by 3dB with selected mapping and predistortion.<sup>[5]</sup>

### 3.2 Chireix’s Outphasing Amplifier

Chireix’s Outphasing Amplifier was developed in 1935; however, it received little interest due to the lack signals causing low efficiency in power amplifiers during that era.<sup>[3]</sup> Today, there is an increased interest in this circuit due to its potential for increased efficiency. The basic circuit diagram of the Outphasing Amplifier is shown in Figure 3.1 below.

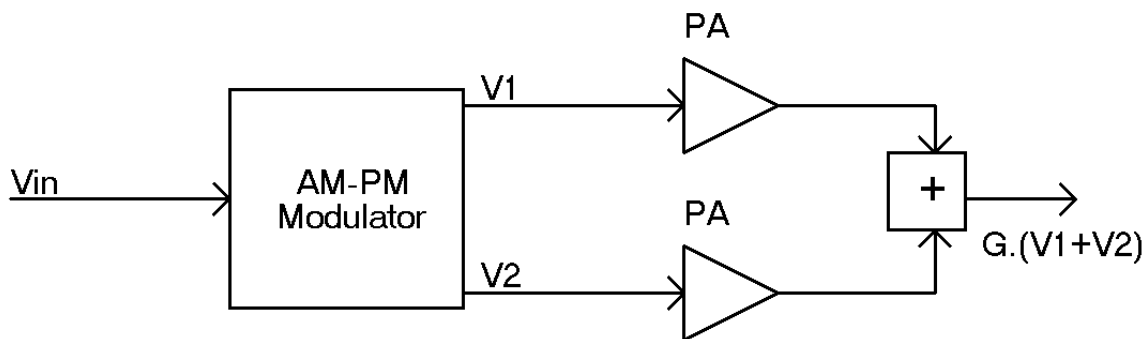


Figure 3.1 Basic Chireix Outphasing Amplifier Topology

In this topology, two amplifiers are used in parallel; however, both of these amplifiers operate at a fixed power level and can be highly nonlinear. The concept is somewhat similar to the predistorter in respect to the idea of using two nonlinear devices to generate a linear signal. Here, we apply an amplitude modulated signal, or a signal with a high PAPR, into a phase modulator to produce two equal, fixed amplitude, phase modulated signals with opposite sense. The final output is the sum of the fixed amplitude

signals, after passing through their respective power amplifiers, reproducing the modulated output. Equation 3.1 shows the mathematical calculations for this topology, where G represents the amplifier voltage gain and A(t) represents the modulated amplitude of the input signal.

$$\begin{aligned}
 V_{in}(t) &= A(t)\cos(\omega t) \\
 V_1(t) &= \cos\{\omega t + \cos^{-1}[A(t)]\} \\
 V_2(t) &= \cos\{\omega t - \cos^{-1}[A(t)]\} \\
 V_{out} &= G[V_1(t) + V_2(t)] = 2GA(t)\cos(\omega t)
 \end{aligned}$$

**Equation 3.1 Chireix Outphasing Amplifier**

Nonlinearities at the output are dependant on the integrity of the AM-to-PM modulator, not the nonlinearities of the power amplifiers. Therefore, the key element to the outphasing amplifier is the AM-to-PM modulator. Also, it should be noted that, while the individual amplifiers are operating at high efficiency, the overall system may operate with poor efficiency. This is due to the fact that low power signals are amplified to the same power level as high power signals; hence the constant power levels in the power amplifiers. Therefore, the same power is required to amplify the low power and high power signals, irrespective of the fact that the overall output power may be low when the two signals are summed together. This loss in power can be compensated with shunt reactance's, leading to very promising efficiency levels. See Steve Cripps *RF Power Amplifiers for Wireless Communications* for a full explanation of these compensation reactance's.<sup>[1]</sup>

The limiting factors for Chireix's Outphasing Amplifier are the integrity of the AM-PM modulator as well as the compensation reactance's. During the era that this amplifier was

designed, it would have been very difficult to design an AM-PM modulator that was extremely accurate and fast; however, this is a more achievable goal with today's technology. Also, the compensation reactances must be carefully chosen due to their dependency on the outphasing angle. If a reactance is chosen that is too low, the amplifier will achieve good efficiency at low power levels, but poor efficiency at high power levels, and vice versa. These components also present bandwidth restrictions on the signal.<sup>[1]</sup> Finally, the output of the amplifiers must pass through an RF power combiner, which is often bulky and difficult to fit in to smaller mobile devices.

Sang-Ki Eun from Korea Aerospace University studied the Chireix Outphasing Amplifier, as seen in the IEEE paper *A High Linearity Chireix Outphasing Amplifier Using Composite Right/Left-Handed Transmission Lines*.<sup>[3]</sup> The results of his testing show a maximum efficiency of 49% at 30dBm output power and an efficiency of about 18% at an OBO of 8dB, as seen in Figure 3.2. Overall, this circuit should be studied in more detail to determine its full potential and attempt to mitigate its disadvantages.

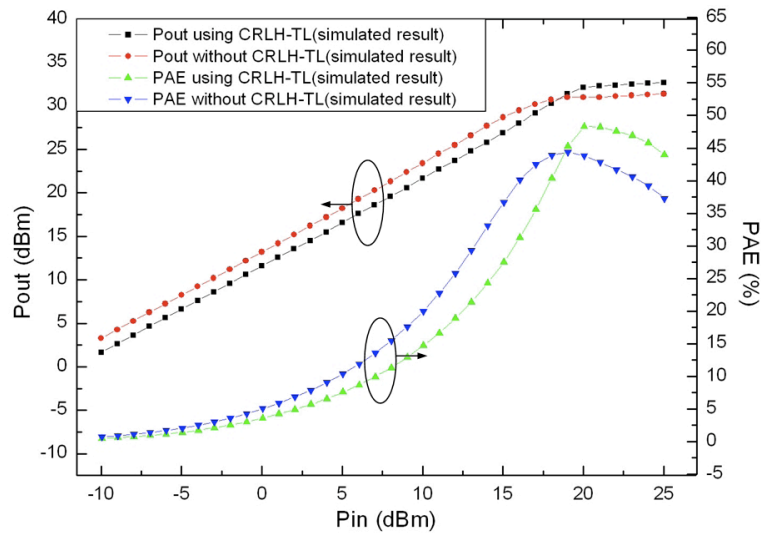


Figure 3.2 Chireix Outphasing Amplifier PAE<sup>[3]</sup>

### 3.3 The Doherty Amplifier

W. H. Doherty at Bell Telephone Laboratories developed the Doherty Amplifier in 1936. The original concept of the Doherty is shown in Figure 3.3, as seen in the 1936 publication from Bell Labs.<sup>[2]</sup> Today the “Tube” amplifiers would be replaced with high frequency transistor amplifiers.

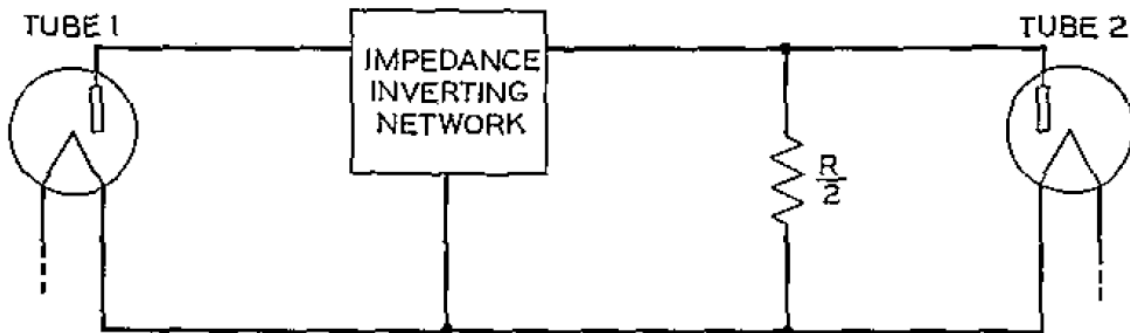


Figure 3.3 Simplified Schematic of the Original Doherty Amplifier<sup>[2]</sup>

This amplifier topology works in two separate stages. The first stage occurs during the low power region, the region in which a conventional class AB amplifier would be highly inefficient. The second stage operates during the higher power region where the conventional amplifier is near saturation. During the first stage, tube 1, the carrier amplifier, is designed such that it reaches its saturation voltage at the edge between the low power region and the high power region. In this region, where today's modulation techniques operate a majority of the time, tube 1 can achieve high efficiency. Note that both tube amplifiers are driven by the input signal, requiring the signal power to be split evenly between both tubes.

The value  $R$  represents the desired load for the amplifier. The Doherty Amplifier provides a load that is  $\frac{R}{2}$ , half of the desired load. An impedance inverter, typically a quarter-wave transmission line, is used between the carrier amplifier and the load. This inverter transforms the load impedance seen by the carrier amplifier from  $\frac{R}{2}$  to  $2R$ . This forces the saturation point of the amplifier to deliver half the power that it is capable of delivering. At the point between stage 1 and stage 2, the carrier amplifier has reached its maximum output voltage but only half of its maximum output current. During stage one, tube 2, the peaking amplifier, is turned off and consumes almost no power. Today this is achieved using a class B or class C amplifier biased to turn-on at the low-to-high power transition.

As the carrier amplifier begins to saturate and the signal enters the high power region, the peaking amplifier begins to turn on. The peaking amplifier serves two purposes; add

additional power to the load as well as modulate the load from  $\frac{R}{2}$  to R, or 2R to R as seen by the carrier amplifier through the impedance transformer. This technique is known as active load-pull, or load modulation. As the input signal delivers more power, the output load appears to reduce in magnitude, allowing the carrier amplifier to deliver more current while maintaining a constant voltage.

The peaking amplifier also provides power to the load. Assuming two identical transistors are used, the overall power available to the load is about twice that of the individual power available from each transistor. Once the peaking amplifier has fully turned on and enters saturation, the Doherty topology operates at maximum efficiency.

Figure 3.4 shows the ideal current and voltage magnitudes of each amplifier throughout each stage.<sup>[1]</sup>

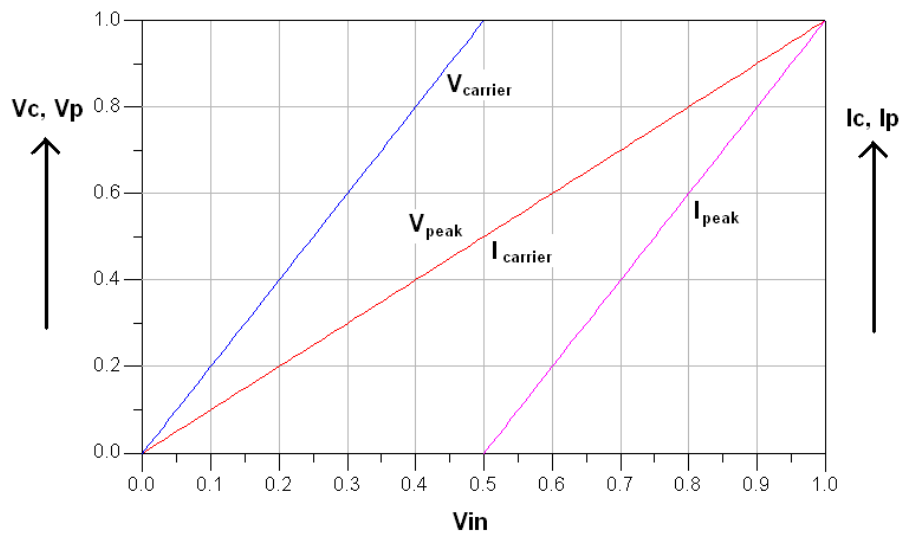


Figure 3.4 Ideal Doherty Amplifier Voltage and Current Magnitudes



At the time of conception of the Doherty Amplifier, mobile wireless devices were almost nonexistent. A majority of communication signals had a very low PAPR and therefore conventional amplifiers could be used with almost the same efficiency as the Doherty. Because of this, the Doherty Amplifier sat dormant for almost 70 years, until modern modulation techniques introduced large PAPR. Just before the turn of the century, only a select few knew about the Doherty topology; now there are numerous papers and research projects pertaining to the Doherty.

One research project done at Seoul National University in Korea shows the following efficiency curve in Figure 3.5.

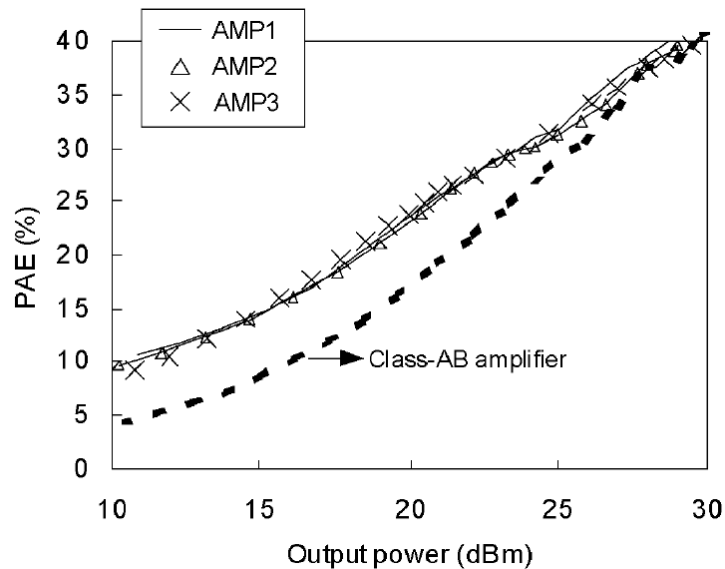


Figure 3.5 Modern Doherty PAE<sup>[4]</sup>

AMP1 represents a typical Doherty topology, while AMP2 and AMP3 are slight variations of the Doherty topology. Figure 3.5 compares the efficiency of the modern Doherty amplifier with that of a conventional class AB amplifier. Both amplifiers provide a maximum efficiency of 40% at 28dBm output power. However, at an output back-off of

8dB, the Doherty amplifier achieves an efficiency of 23%, while the class AB amplifier achieves only 16%. When considering the battery life of mobile applications, an efficiency improvement of 7% over the previous topology is a major breakthrough.

The Doherty has a few design issues that have prevented it from being easily implemented into mobile handsets, one in particular being the size of the required components. Figure 3.6 shows a modern schematic implementation used in research done at Seoul National University, Korea. The classical Doherty amplifier utilizes a bulky 3dB hybrid coupler at the input to split the signal between the carrier and peaking amplifiers. There are also two  $\lambda/4$  transmission lines that can tend to be large for the frequencies of use in mobile devices. The sizes of these components are too large to fit into handheld mobile devices. This research attempts to circumvent this problem by using an active phase splitter in place of the RF coupler as well as T and  $\pi$  networks for the  $\lambda/4$  transmission lines. Their research shows promising results for minimizing the size of the classical Doherty amplifier while maintaining the same beneficial characteristics of the Doherty amplifier.

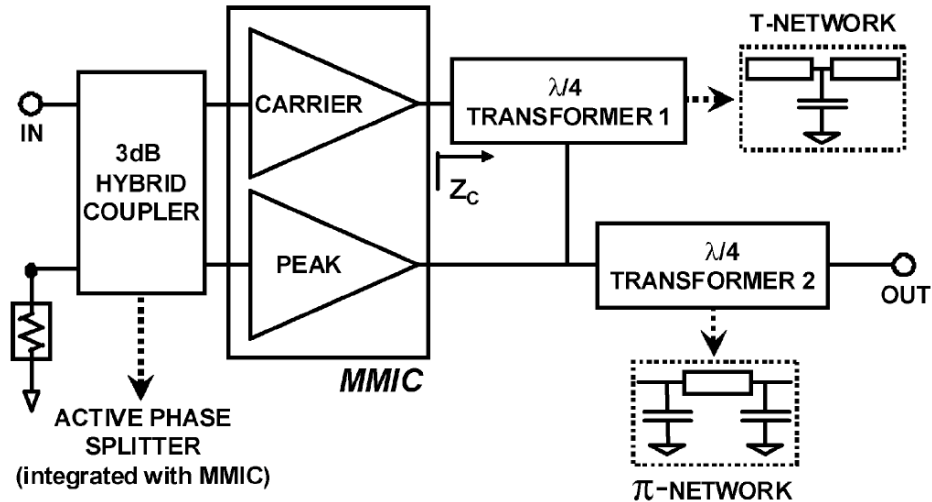


Figure 3.6 Modern Doherty Circuit Topology<sup>[4]</sup>

There are several other issues that need to be addressed in the classical Doherty amplifier. Because the two amplifiers are run in parallel and the peaking amplifier is biased at such a low quiescent point, the input impedance of the peaking amplifier changes drastically from the transitions of stage 1 to stage 2. This can cause problems with any method used for splitting the input signal due to a large change in the reflection coefficient seen by the splitter. Also, splitting the signal into two separate paths splits the input power into two paths. This leads to half of the input power being wasted on a peaking amplifier that is turned off during the low power stage, decreasing the overall achievable power added efficiency at lower power levels.

The Doherty Amplifier also suffers from linearity issues, especially during the high power region of the amplifier. In CDMA systems, Adjacent Channel Power Ration (ACRP), a measurement of amplifier linearity, must be met over the entire output power region. Doherty amplifiers often times suffer from poor ACPR measurements as well as large phase shifts over varying output powers, known as AM-PM. Figure 3.7a is a plot

from a study at the University of California San Diego showing the typical output phase shift vs output power of a Doherty amplifier. It shows as much as a  $35^\circ$  phase shift, causing potential linearity and demodulation issues of the transmitted signal. The presented study from UCSD is able to reduce the output phase shift by  $20^\circ$  by modifying the phase delay of the peaking amplifier. The results of their study are shown in Figure 3.7b.<sup>[15]</sup>

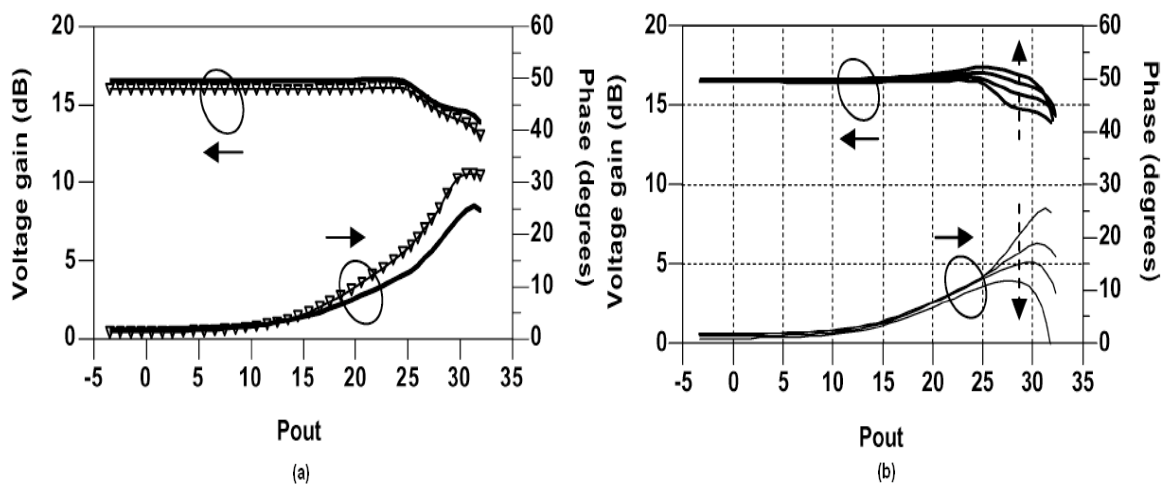


Figure 3.7 AM-PM Output Phase shift of (a) typical Doherty Amplifier and (b) modified Doherty Amplifier

## 4 Negative Conductance Load Modulation Amplifier

This thesis presents a new amplifier topology with the goal of increased efficiency in systems with a high PAPR. The following will describe the theory of operation of this amplifier, discuss the process of designing the amplifier, and present simulation and experimental results of this study.

### 4.1 Theory of Operation

The amplifier proposed in this project utilizes the idea of load modulation, like that found in the Doherty Amplifier. Figure 4.1 shows a simplified block diagram of the proposed amplifier.

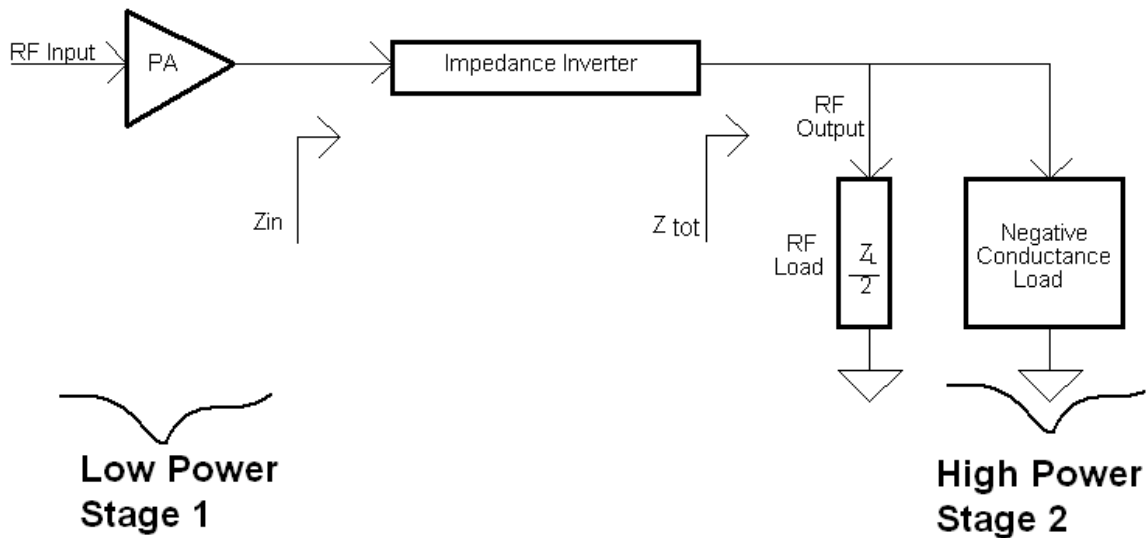
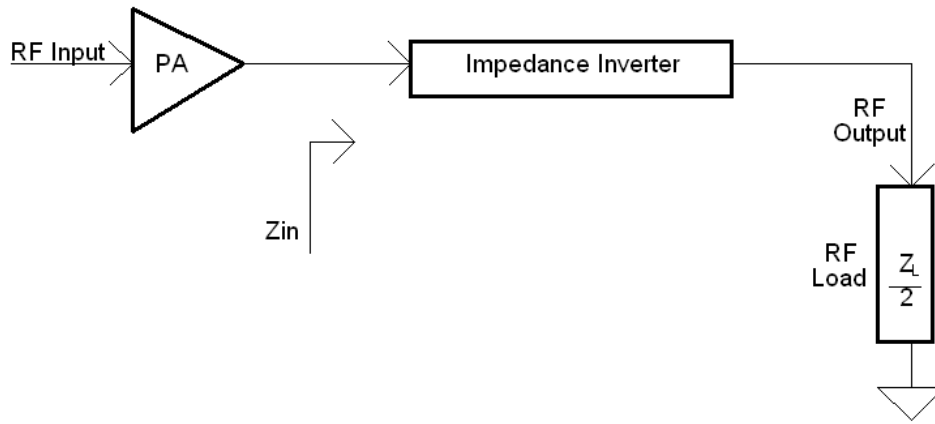


Figure 4.1 Simplified Block Diagram of Negative Conductance Load Modulation Amplifier

The amplifier topology works in two stages, a low power stage and a high power stage. During the low power stage, the negative conductance load is turned off and consumes

almost no power. This is equivalent to a very large impedance in parallel with the RF load  $\frac{Z_L}{2}$ . This large impedance has almost no effect on the load impedance presented to the input power amplifier, and, assuming an ideal situation, can therefore be ignored during the first stage of operation. Figure 4.2 represents the equivalent circuit during the low power stage of operation.



**Figure 4.2 Simplified Block Diagram of Stage 1 Operation of Negative Conductance Load Modulation Amplifier**

The RF Load,  $\frac{Z_L}{2}$ , is chosen such that, if  $Z_L$  were presented directly to the power amplifier without an impedance inverter,  $Z_L$  would produce maximum efficiency in the power amplifier. The impedance inverter transforms the load from  $\frac{Z_L}{2}$  to  $Z_{in} = 2Z_L$ , seen by the input amplifier. If  $Z_L$  had been chosen to provide maximum power, then providing a load of  $2Z_{L_{max\_power}}$  would force the transistor to saturate at about half the maximum current  $|I_{max}|$ , as seen in Equation 4.1.

$$\begin{aligned}\bar{P}_{\max} &= \bar{V}_{\max} \bar{I}_{\max} \\ |I_{\max}| &= \frac{|V_{\max}|}{Z_{L_{\max\_power}}} \\ |I_{stage\_1}| &= \frac{|V_{\max}|}{2Z_{L_{\max\_power}}} = \frac{|I_{\max}|}{2}\end{aligned}$$

#### Equation 4.1 Max Voltage, Half Current

Because we chose  $Z_L$  to achieve maximum efficiency, the point at which we reach the saturation voltage will not directly correspond to  $\frac{|I_{\max}|}{2}$ , but should be somewhere near the same value. For ease of calculations and understanding, we will assume that we reach  $|V_{\max}|$  and  $\frac{|I_{\max}|}{2}$  at the same time.

During stage 1, we can view the system as a simple class AB amplifier, or class B depending on the design, similar to the conventional class AB amplifiers mentioned in Section 2.3 earlier. From Figure 2.3 we saw that the PAE of a class AB amplifier at an output back-off of 8dB is about 15%. If the design stopped here, both the stage 1 amplifier (low power stage) and the class AB amplifier would achieve poor efficiencies at an 8dB OBO. However, when the voltage on the collector of the input amplifier reaches its maximum voltage, the presented design continues on to stage 2, the high power stage. During stage 2, the negative conductance load operates, extending the maximum output power of the total system by modulating the load presented to the input amplifier as well as providing additional power to the load. As seen in Figure 4.3, the extension of power not only increases the available power from the system but also

increases the power level corresponding to 8dB OBO, increasing the PAE significantly at this point.

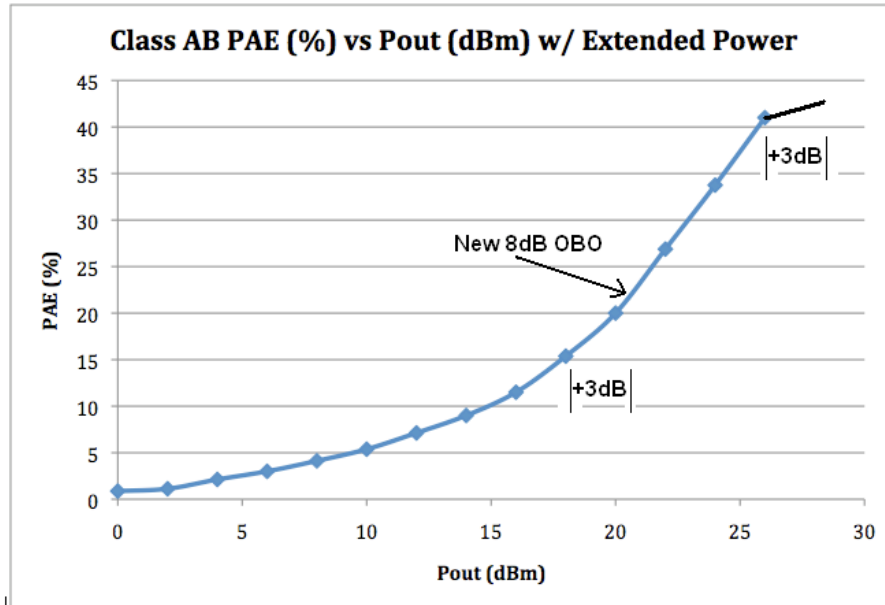


Figure 4.3 Class AB PAE with Extended Power Range from Negative Conductance Load

The negative conductance block represents a network that provides power when driven by a voltage as opposed to consuming power like a standard load. Equation 4.2 shows the effect of having a negative conductance load. Assuming that the applied voltage is positive, the current into the network must be negative. A negative current implies current leaving the network, delivering power out of the negative conductance load.

$$\frac{I}{V} = -G$$

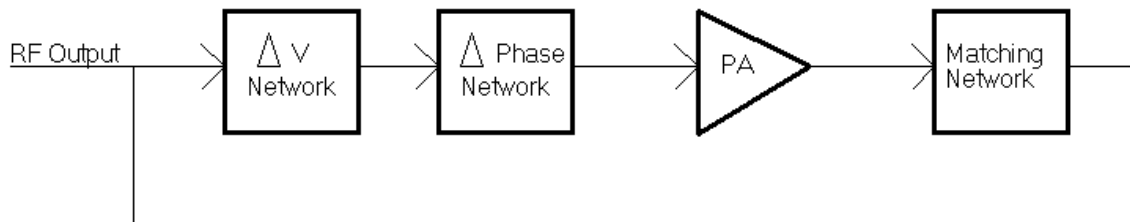
$$V \geq 0$$

$$\therefore I \leq 0$$

Equation 4.2 Negative Conductance



The negative conductance network is achieved using a transistor power amplifier with positive feedback. It acts much like a controllable class C power oscillator, class C designating that the transistor is turned off for low input voltages, such as those during stage 1 operation. Figure 4.4 shows the basic block diagram of the negative conductance network.



**Figure 4.4 Basic Negative Conductance Load Block Diagram**

At this point, it is important to note that the impedance inverter in Figure 4.2 also has the characteristic of changing the input power amplifier from a current source to a voltage source. This is important because the negative conductance network also “see’s” the input amplifier as a voltage source. A detailed description of the operation of the negative conductance network will be discussed later in Section 4.3.3. For now we will assume that this circuit performs as described.

As the input amplifier begins to saturate at the edge of the low power stage, the system transitions from stage 1 to stage 2. The negative conductance network begins to turn on, providing power to the RF load and having a negative conductance. The impedance of the RF load in parallel with the negative conductance load increases as the negative conductance load becomes more negative. Figure 4.5 and Equation 4.3 show an example

of how negative conductance in parallel with positive conductance increases the total impedance. For simplicity, we will assume that both loads are purely real loads.

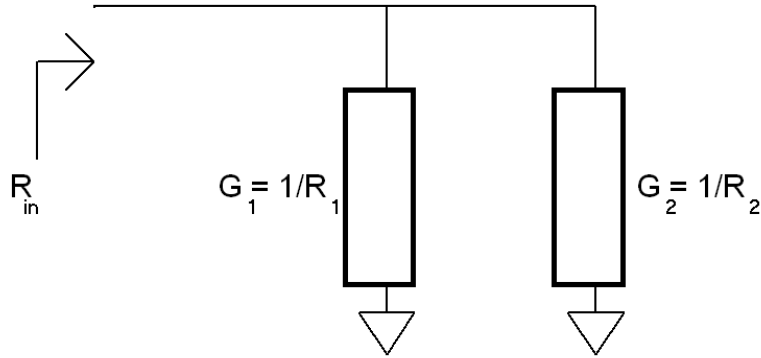


Figure 4.5 Negative Conductance in Parallel with a Positive Conductance

$$R_{in} = \frac{R_1 R_2}{R_1 + R_2} = \frac{\frac{1}{G_1 G_2}}{\frac{1}{G_1} + \frac{1}{G_2}} = \frac{1}{G_1 + G_2}$$

Equation 4.3 Input Resistance of Parallel Negative and Positive Conductance Loads

Assuming that  $G_2 \leq 0$ , negative conductance, and  $|G_1| \geq |G_2|$ , the overall input resistance will always be positive. As  $G_2$  becomes more negative, the denominator  $G_1 + G_2$  decreases, causing an increase in  $R_{in}$ .

Applying this to  $Z_{tot}$  in Figure 4.1, we see that  $Z_{tot}$  shifts from  $\frac{Z_L}{2}$  towards  $Z_L$ .

Transferring this shift through the impedance inverter, we see that  $Z_{in}$  shifts from  $2Z_L$  towards  $Z_L$ , the desired load impedance for maximum efficiency. Note that  $Z_{in}$  is decreasing in magnitude as the negative conductance network turns on. Using this load

modulation, we can maintain a constant voltage on the input amplifier by linearly increasing the output current at the same rate as we decrease the magnitude of  $Z_{in}$ .

$$V = \uparrow I \downarrow Z_{in}$$
$$P = \uparrow I^2 \downarrow R$$

Equation 4.4

RF Power to the load continues to increase due to the squaring factor of the current in Equation 4.4. Recall that the impedance inverter transforms the power amplifier from a current source to a voltage source. Therefore, while the voltage output from the power amplifier is held constant, the voltage on the RF load continues to increase due to the increased output current from the amplifier. The further we increase the RF Output voltage, the further we turn on the negative conductance network, forcing it to become more negative and maintain a constant voltage on the input amplifier. Using this technique, we are able to operate the transistor in a high efficiency state, near saturation, over a larger range of output power.

Recall that the negative conductance network is a power amplifier itself. Assuming that the same transistor is used for both the input amplifier and the negative conductance amplifier, we can deliver approximately twice as much power as what is available from a single transistor. This is obviously an ideal case, assuming that no power is lost through the negative conductance circuit, but nonetheless a fair estimation.

## 4.2 Power Amplifier Design Concepts

### 4.2.1 Amplifier DC Biasing

DC biasing of transistor amplifiers is often the first step of any amplifier system design.

The point at which the transistor is biased will determine the general linearity and efficiency of the amplifier. Classes of amplifier biasing have been designated for commonality among different designs. The first four classes are shown in Figure 4.6, where  $V_b$  represents the DC voltage on the base of the transistor and  $I_c$  represents the DC current through the collector of the amplifier.

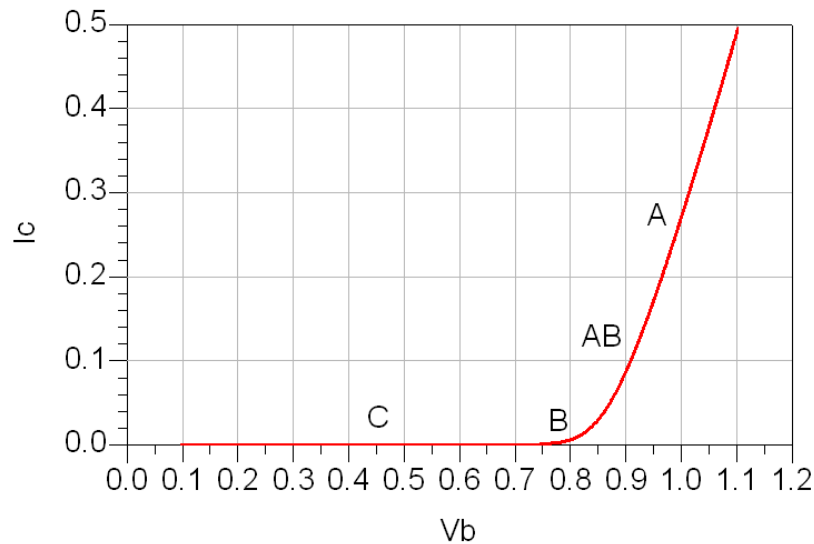


Figure 4.6 Amplifier DC Biasing and Classes

Class A amplifiers are biased completely in the linear region, producing a linear output. The amplifier conducts over the entire input cycle, producing an output that is a scaled up version of the input without clipping. This can be seen in Figure 4.6, as any small signal voltage change on the base produces a linear change in the collector current. These

amplifiers suffer from poor efficiency because the transistor is continually conducting a finite amount of current, drawing power from the supply. They are often used for small signal amplification where the bias current is small enough for the power draw to be insignificant on the overall system design.

Class B amplifiers are biased on the knee of the transistor, the point where the transistor turns on. They conduct for half of the input cycle, as seen in Figure 4.6. A positive voltage change on the base will push the collector current into the linear region while a negative voltage change on the base will hold the collector current at zero. These amplifiers are much more efficient than class A amplifiers because they only conduct half the time; however, they only accurately reproduce half of the input signal while clipping the other half.

Class AB amplifiers are a tradeoff between class A linearity and class B efficiency. They are biased in the region between class A and class B where they will conduct more than half of the input signal, but not the entirety of the signal. This biasing is often used in power amplifiers where both linearity and efficiency are important.

Class C amplifiers are biased such that less than half of the input cycle is conducted through the transistor. This produces highly efficient amplifiers because the transistor is turned off a majority of the time. However, the output is a highly distorted version of the input. These amplifiers are used for wireless transmitters in systems where linearity is less important and can be partially recovered with tuned loads. Amplifier conduction angles are shown in Figure 4.7 below.

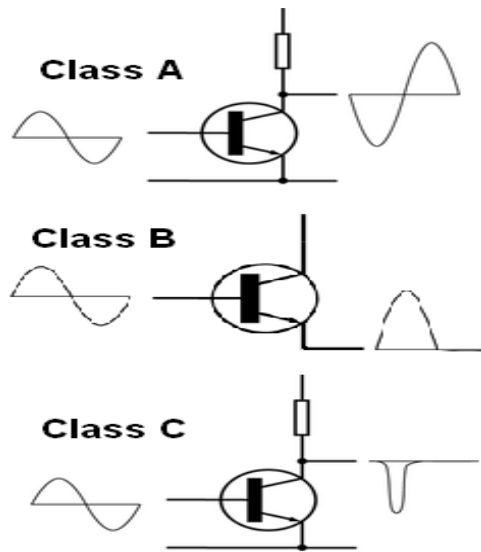
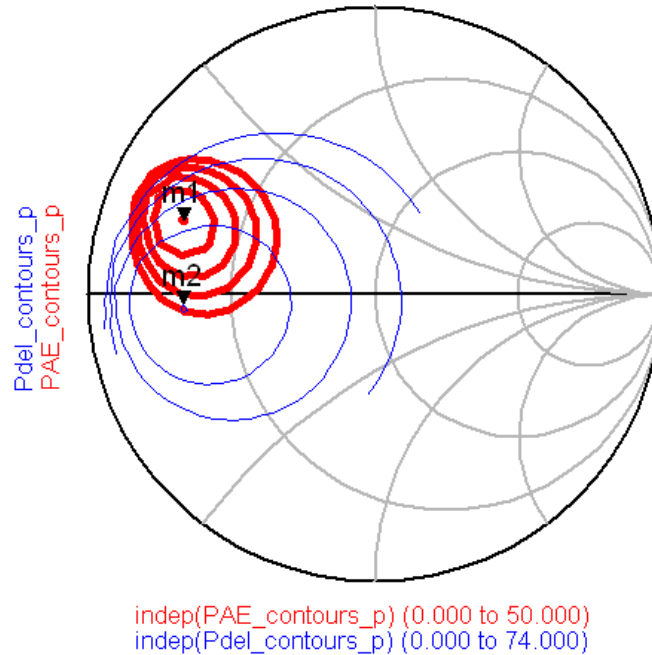


Figure 4.7 Amplifier Conduction Angles<sup>[10]</sup>

#### 4.2.2 Load Pull and Source Pull Analysis

Steve Cripps wrote in his book *RF Power Amplifiers for Wireless Communications*, “Load-pull data has been the mainstay of RF and (especially) microwave PA design for many years.”<sup>[1]</sup>

The concept of load pull and source pull analysis is quite simple, while the real world laboratory implementation can be very difficult. In a simplistic sense, load pull analysis involves a device under test (DUT), in our case a transistor amplifier, and a calibrated tuning device on the output.<sup>[1]</sup> The input of the DUT is driven at a particular frequency while the output device is swept over various load impedances. Output power and efficiency is measured over the swept load values and plotted on a smith chart for constant power and efficiency contours, like the ones seen in Figure 4.8.



**Figure 4.8 Load Pull with Power and Efficiency Contours**

The power (thin trace) and efficiency (thick trace) contours show load impedance values that produce constant output power or constant efficiency. Markers M1 and M2 in Figure 4.8 are the center of the contours, which represent the loads for maximum efficiency and maximum power, respectively. These impedances can be used to match the load to a particular value and produce the desired performance.

Source Pull is a similar concept except the impedance of the source is swept over various values. Usually, load pull and source pull are done together because of the dependency of output power on input impedance in many transistors, particularly bipolar transistors.<sup>[1]</sup>

### 4.3 Design and Simulation

The following describes the process used to design the proposed amplifier and the simulation results throughout the design.

### 4.3.1 Transistor Characteristics and Selection

For any engineering design, it is crucial to select components that will perform well for a specific application. It is especially crucial in high frequency design where components at a particular frequency work as desired but may do the complete opposite at a slightly different frequency. For the design of our amplifier, it was important to find a transistor that works well at 1.9GHz, designed for class AB operation and lower, can output medium power (about 23dBm), highly efficient, designed for a typical Li-Ion battery voltage of 3.6V, readily available to purchase, and preferably has a simulation model or SPICE parameters given.

We decided to use the BFG21W bipolar UHF power transistor from NXP. It is specifically designed for wireless communication applications at 1.9GHz, providing experimental data at that frequency. It is also designed for rugged class AB pulsed operation, capable of withstanding a VSWR of 6:1. NXP provided complete SPICE parameters for simulation models, as well as S parameters for many different voltage and bias conditions. NXP also released a model of the transistor for Agilent's Advanced Design System (ADS), the software used for simulations in this design. The transistor can provide a maximum power of 26dBm at 3.6V and 500mA DC collector current.

### 4.3.2 Input Amplifier Design

The input amplifier was designed to achieve maximum efficiency while maintaining good linearity. The bias condition was first chosen just above the knee voltage, in a deep class AB mode, for good efficiency and decent linearity. Figure 4.9 shows the dc biasing schematic and the corresponding simulation results in Figure 4.10. The test setup sweeps



the input DC current into the base of the transistor,  $I_{in}$ , from 0 to 10.55mA. The voltage on the base and the collector current are measured and plotted vs. each other, allowing us to choose an appropriate bias voltage for the desired collector current and angle of conduction.

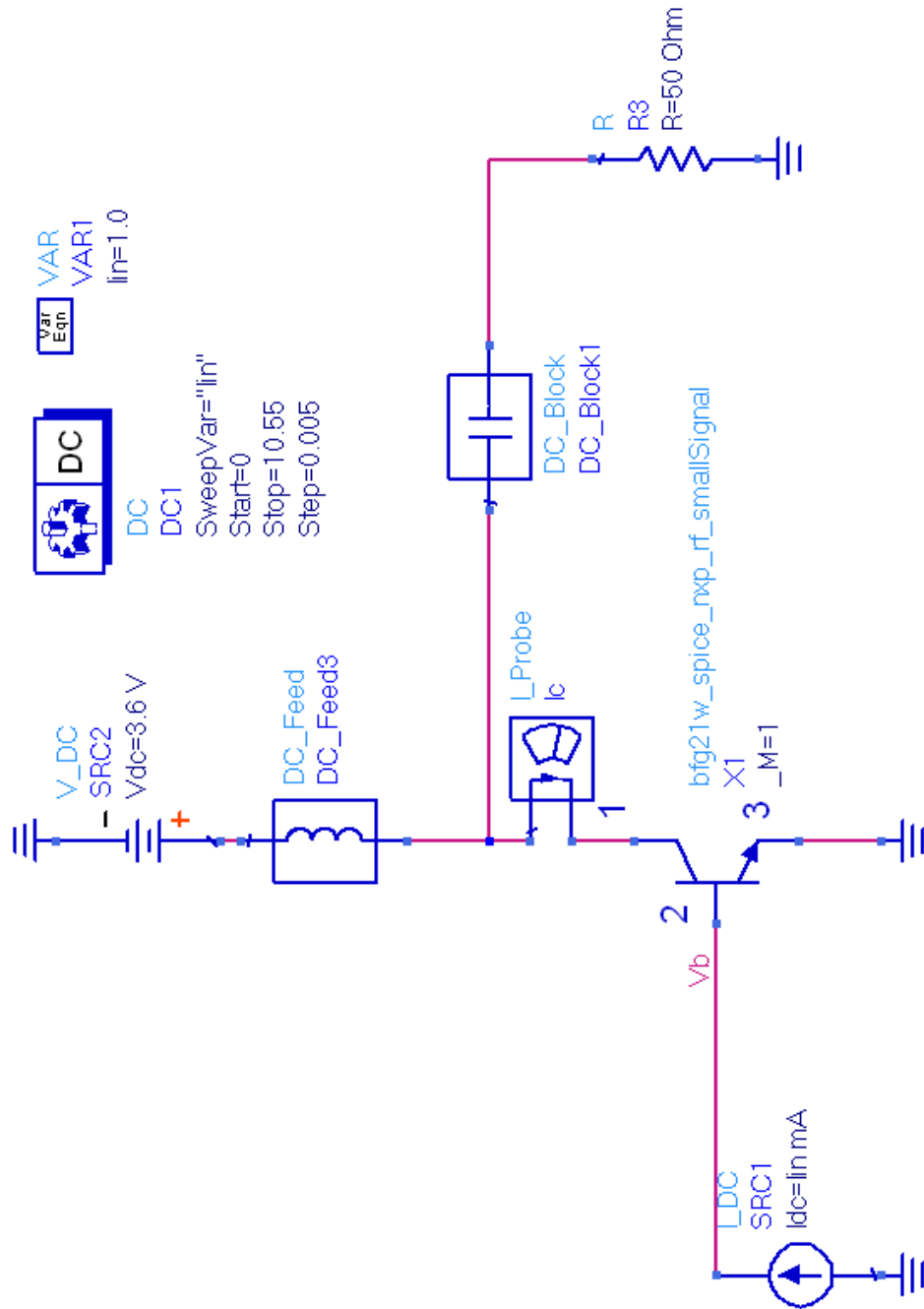


Figure 4.9 DC Biasing Test Setup for BFG21W Bias Conditions

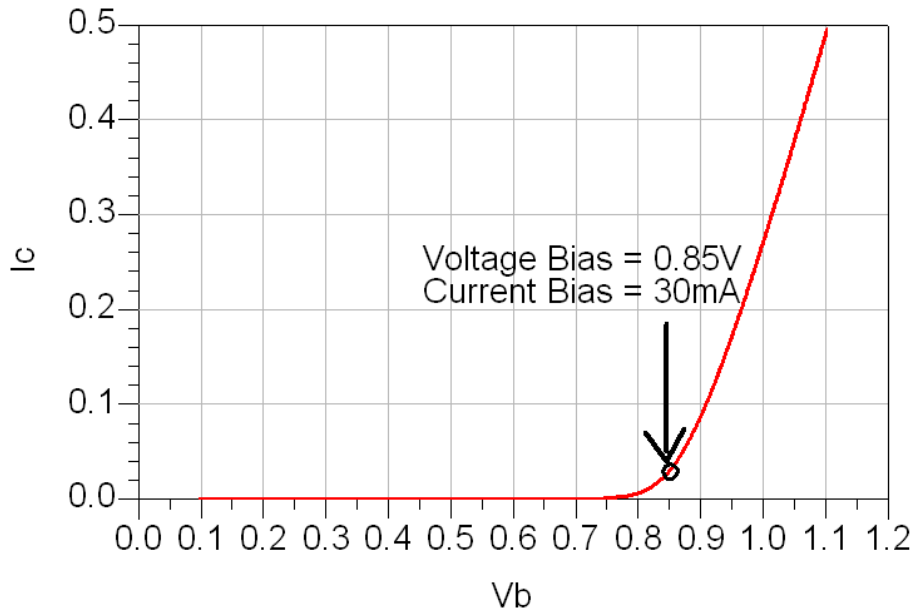


Figure 4.10 BFG21W Biasing Simulation Output

Once the DC bias point is chosen, load and source pull analysis is simulated. Figure 4.11 and Figure 4.12 show the schematics used for the load and source pull analysis, respectively. Load and source pull were done iteratively, meaning that load pull analysis was done first with a source impedance of 50 ohms. The load corresponding to maximum efficiency was used as the load during the first source pull analysis. The source impedance corresponding to maximum power was used for a second load pull analysis, and so forth, with the results from each simulation shown in Table 4.1.

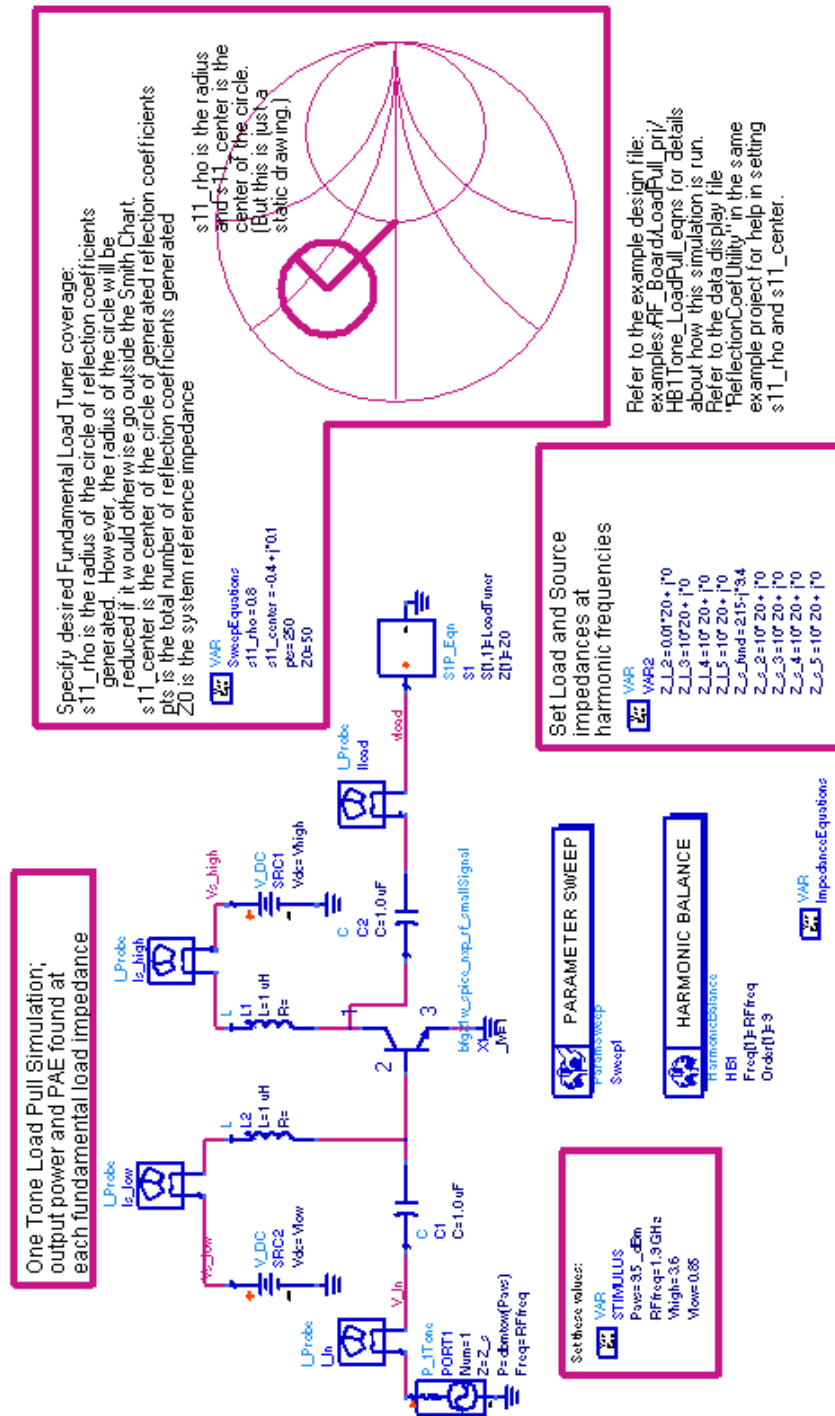


Figure 4.11 Load Pull Analysis Simulation Schematic

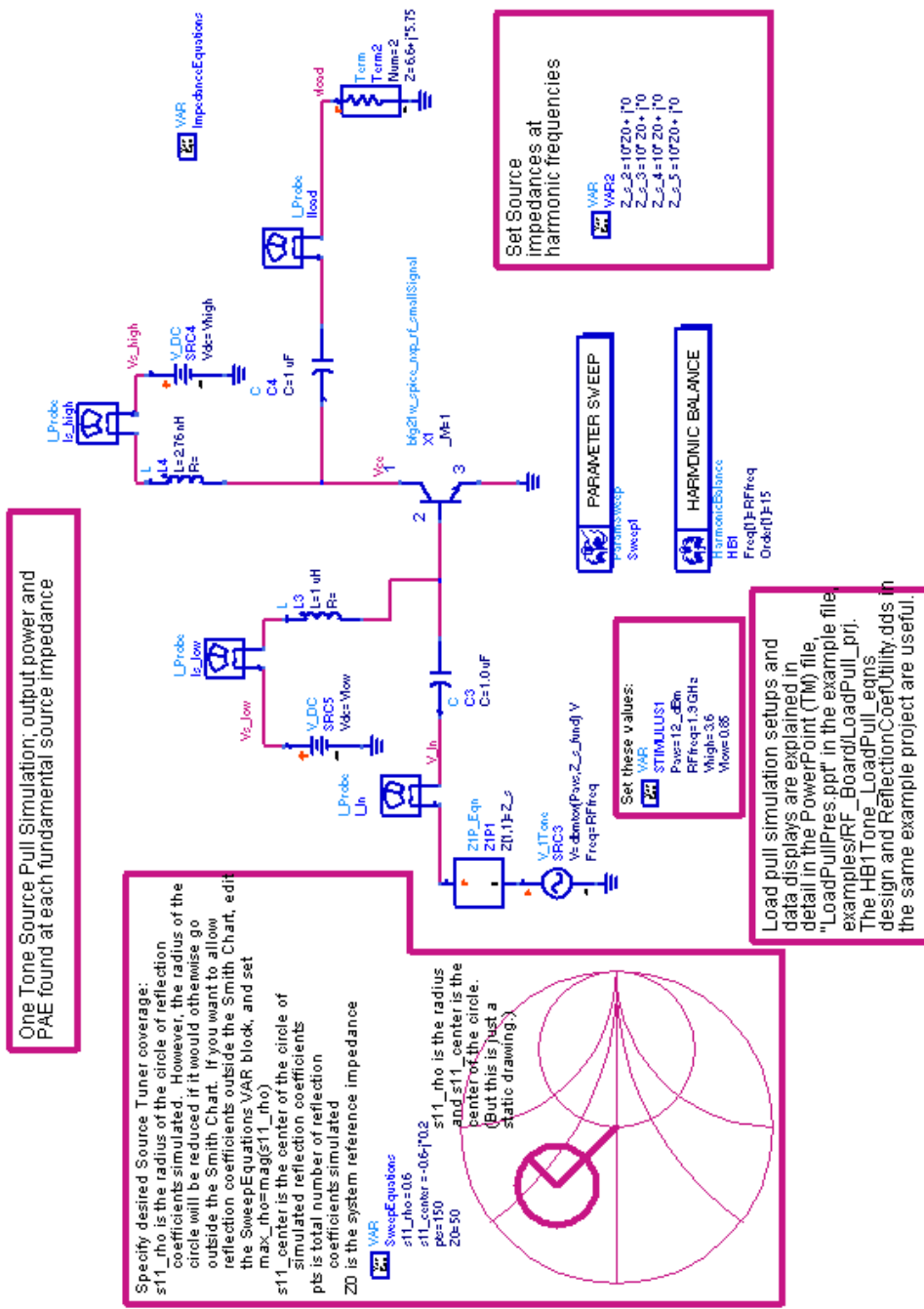


Figure 4.12 Source Pull Analysis Simulation Schematic

For both load and source pull simulations, S11\_rho and S11\_center had to be chosen in order to find the center of the contours. The simulations test impedances in a circular region of the smith chart, as seen from the “Simulated Load Impedance” box on the bottom right hand side of Figure 4.13. S11\_rho is the radius of the circular region and S11\_center is the center of the circular region. Because our goal is to find the maximum power and efficiency impedances, trial and error was used to find the correct values for S11\_rho and S11\_center. Load and source harmonic impedances were set to be very high,  $10Z_0$ , in order to reject all harmonic frequencies in the simulation results. The results of the final load and source pull analysis are shown in Figure 4.13 and Figure 4.14.

<b>Iteration</b>	<b>Source Impedance</b>	<b>Load Impedance – Max Efficiency</b>	<b>Load Impedance – Max Power</b>
1st LP	50	8.7+j8.95	
1st SP	1.85-j9.85	8.7+j8.95	
2nd LP	1.85-j9.85	6.55+j5.75	
2nd SP	2.15-j9.4	6.55+j5.75	
3rd LP	2.15-j9.4	6.6+j5.75	9.5+j3.65
3rd SP	2.15-j9.35	6.6+j5.75	

\*LP = Load Pull

\*SP = Source Pull

**Table 4.1 Impedance Results from Load and Source Pull Analysis**

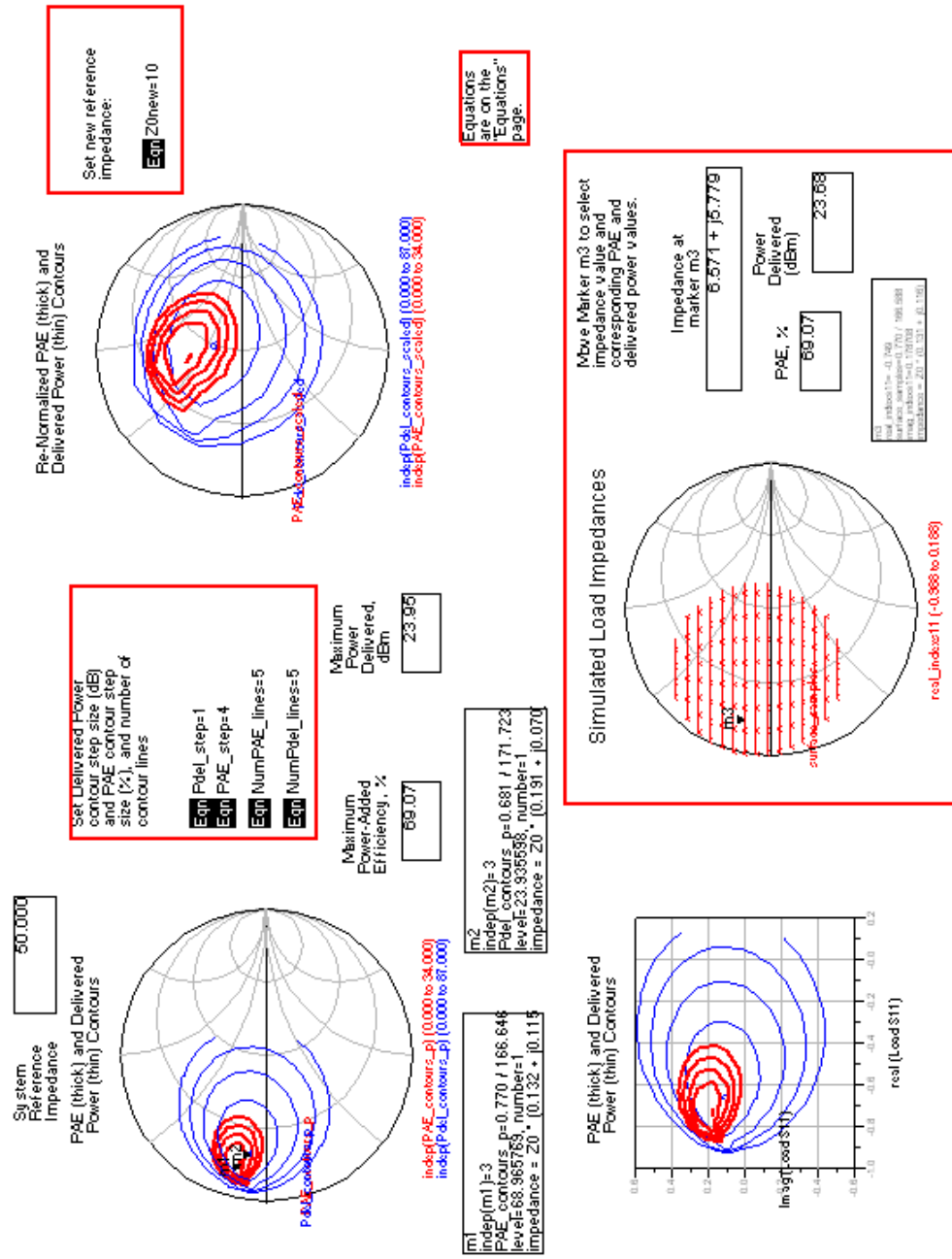


Figure 4.13 Load Pull Analysis Simulation Results

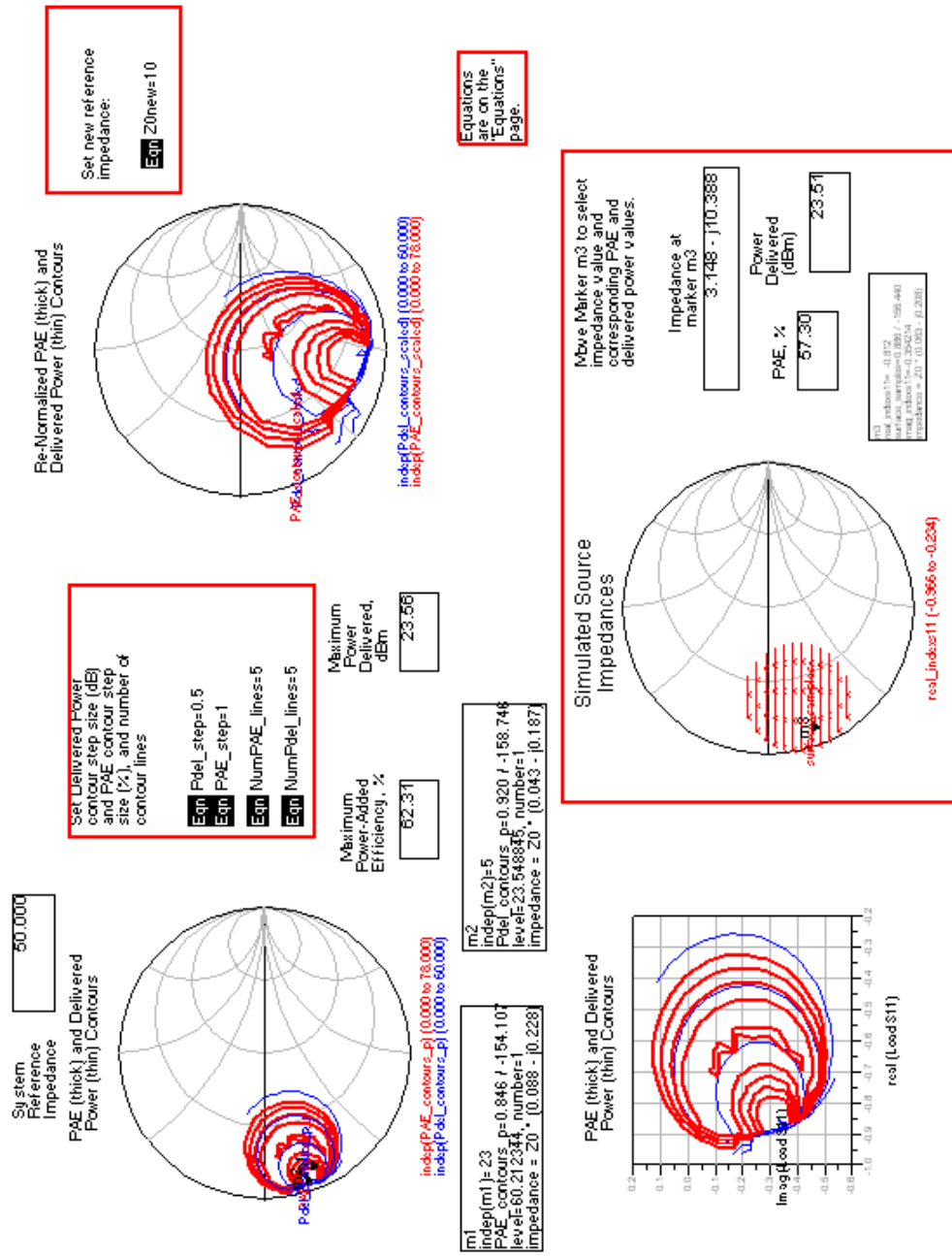


Figure 4.14 Source Pull Analysis Simulation Results



The schematic in Figure 4.15 was simulated to verify operation of the circuit with the new load and source impedances. The results of the simulation are shown in Figure 4.16. The 1dB compression point was found to be 23.38dBm, with a corresponding efficiency of 45.604%.

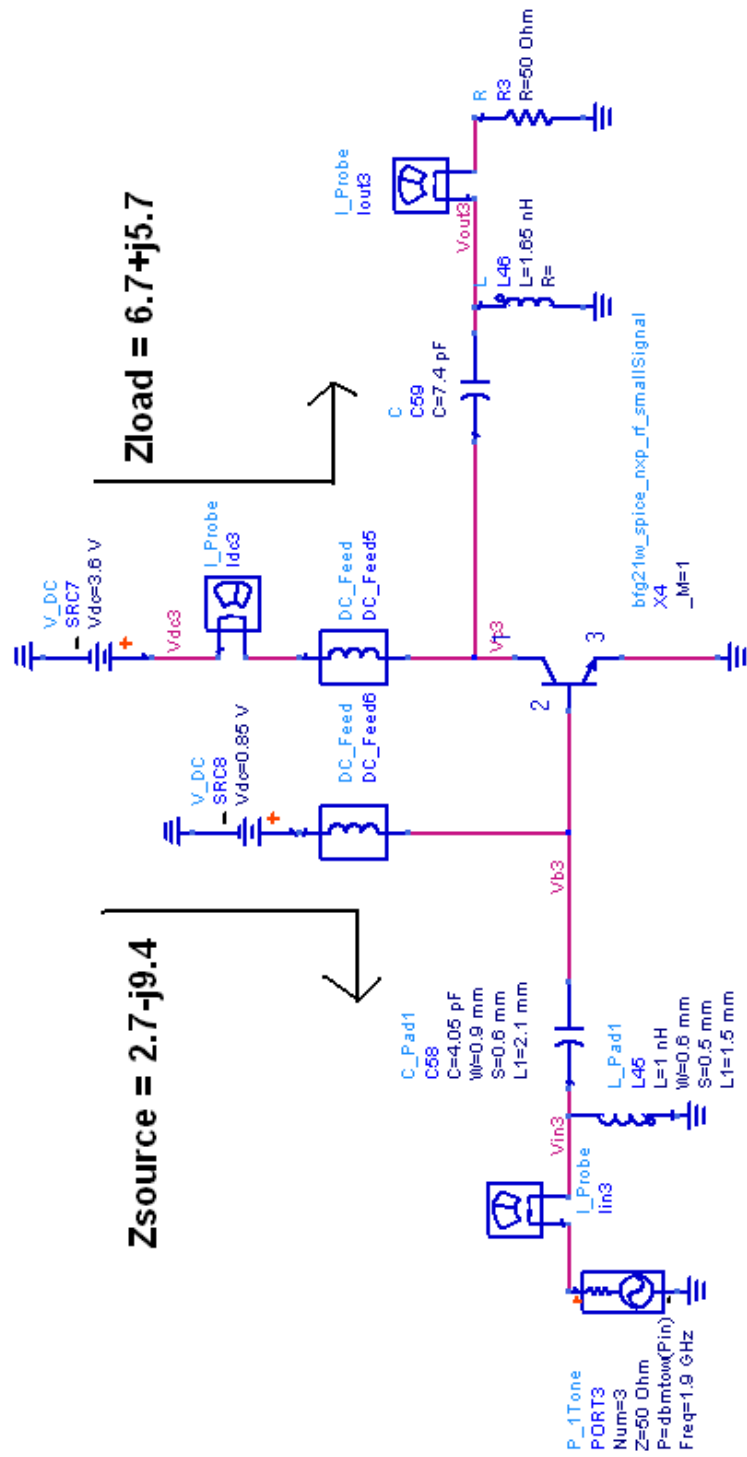


Figure 4.15 Input Amplifier with Optimum Load and Source Matching Schematic

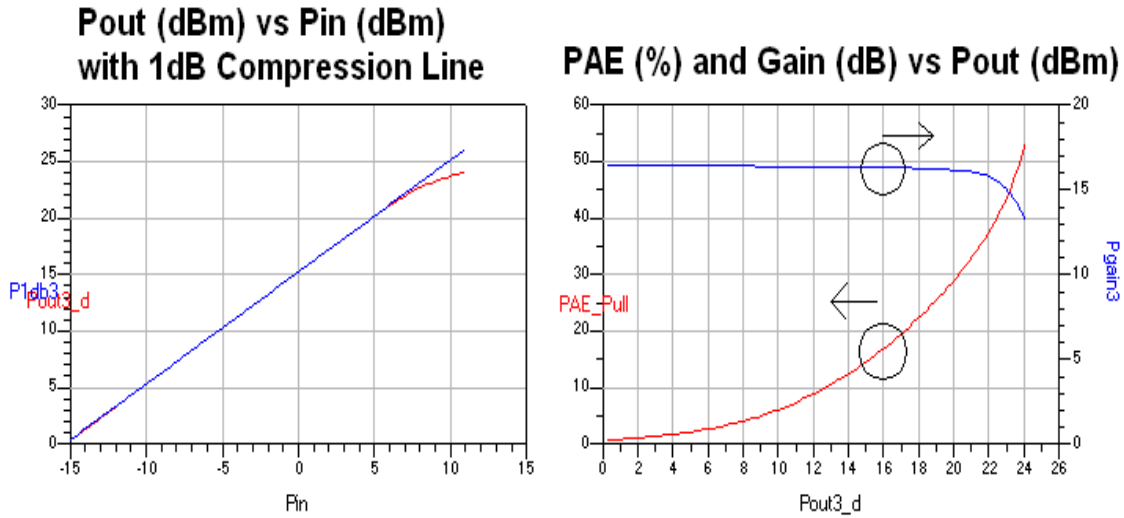


Figure 4.16 Simulation Results for Optimum Input Amplifier Schematic

With the optimum load and source impedances found, the characteristic impedance of the

$\frac{\lambda}{4}$  inverter is designed. For this design, we used a microstrip transmission line with a

length of  $90^\circ$ , or  $\frac{\lambda}{4}$ . In an ideal situation, as described in Section 4.1, the load presented

to the impedance inverter would be  $\frac{Z_{L_{opt}}}{2}$ . It was found that presenting a purely real load

to the impedance inverter produced a better performance and therefore the reactance

portion of  $Z_{opt}$  was minimized. Equation 4.5 was used to design the impedance inverter to

achieve an input impedance of  $2R_{opt}$ .

$$Z_{in} = \frac{Z_o^2}{Z_L}$$

Equation 4.5 Input Impedance of a Loaded Impedance Transformer

The final schematic of the input amplifier with impedance transformer is shown in Figure 4.17 and the corresponding simulation results swept over input power shown in Figure 4.18. The 1dB compression point was found to be 26.1dBm, with a corresponding PAE of 58.3%. The collector current plot in Figure 4.18 shows the transistor operating as a class AB amplifier, conducting more than half of the input signal but not the entire cycle.

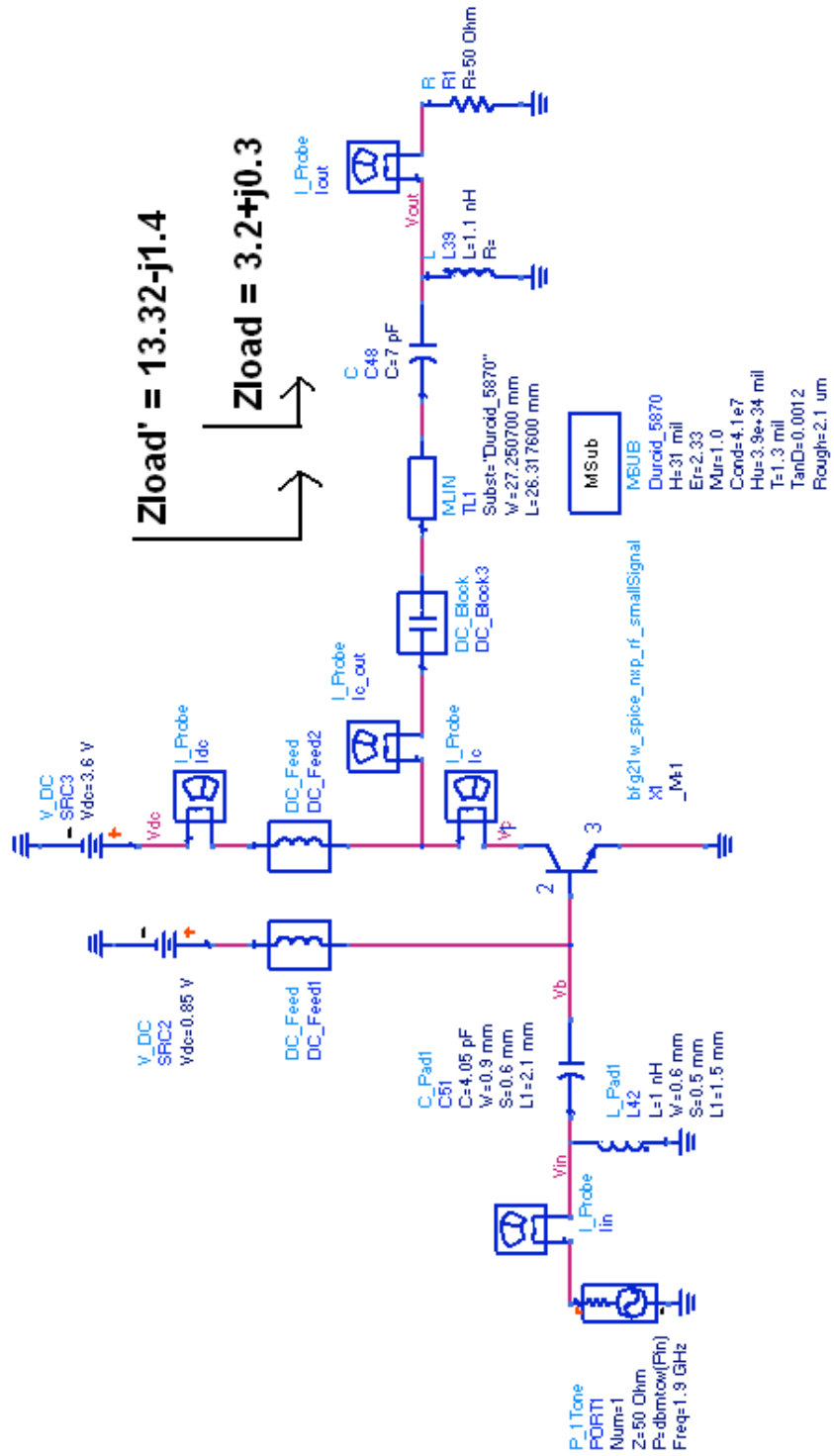


Figure 4.17 Input Amplifier with Impedance Transformer Schematic

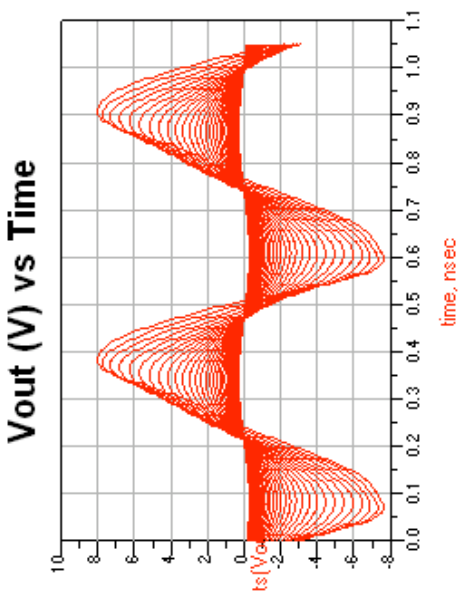
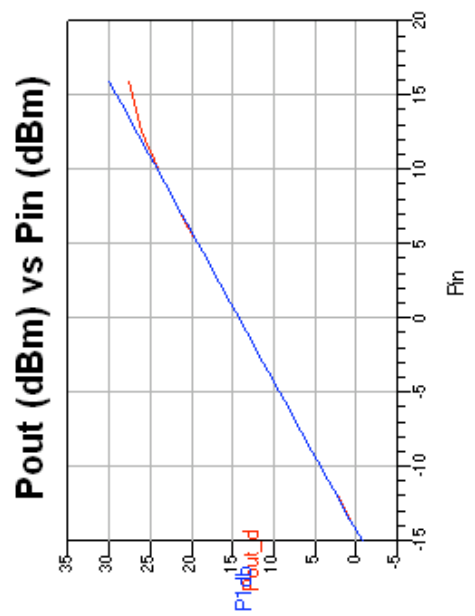
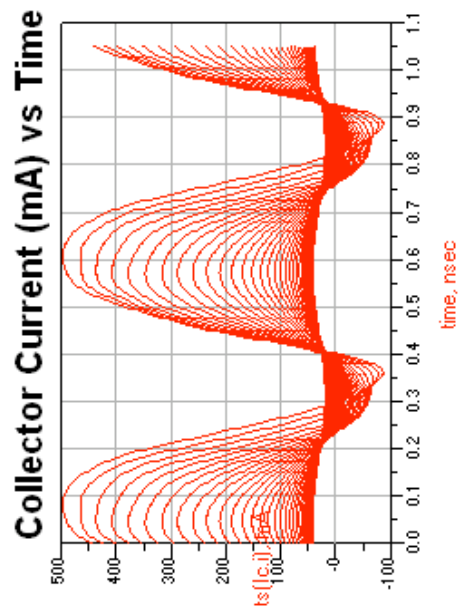
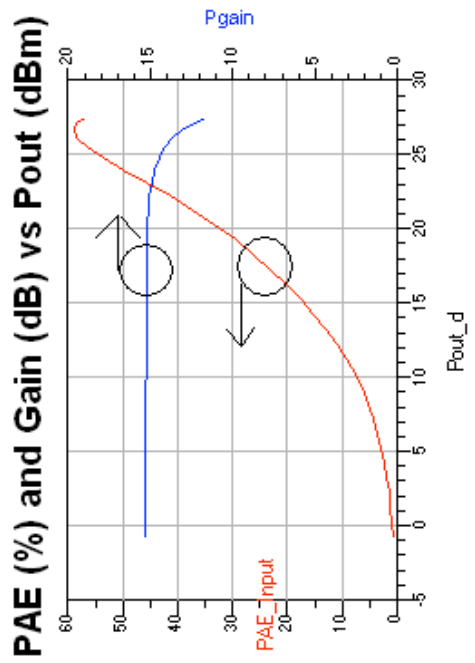


Figure 4.18 Input Amplifier with Impedance Transformer Output Results

### 4.3.3 Negative Conductance Amplifier Design

The negative conductance amplifier is designed much like an amplifier with positive feedback. As seen in Figure 4.4, there are voltage scaling and phase shifting networks on the input of the amplifier and a matching network on the output feedback path.

The amplifier is biased in class C, ensuring that the amplifier is turned off during the low power mode. The actual DC bias voltage is left to the designer to choose during circuit optimization and can be used as a variable throughout the design. An initial bias voltage of 0.4V was chosen as a starting point.

While load pull simulations are not as effective for lower classes of amplifier operation, the simulation was still used as starting point for the design. A load pull simulation was performed with a bias voltage of 0.4V and a source impedance of  $50\Omega$ . The load corresponding to maximum power was chosen to increase the potential range of load modulation and maximize the output power from the complete system. Load pull output data is shown in Figure 4.19. The results show a desired load of  $4.72+j0.63$  for maximum power.

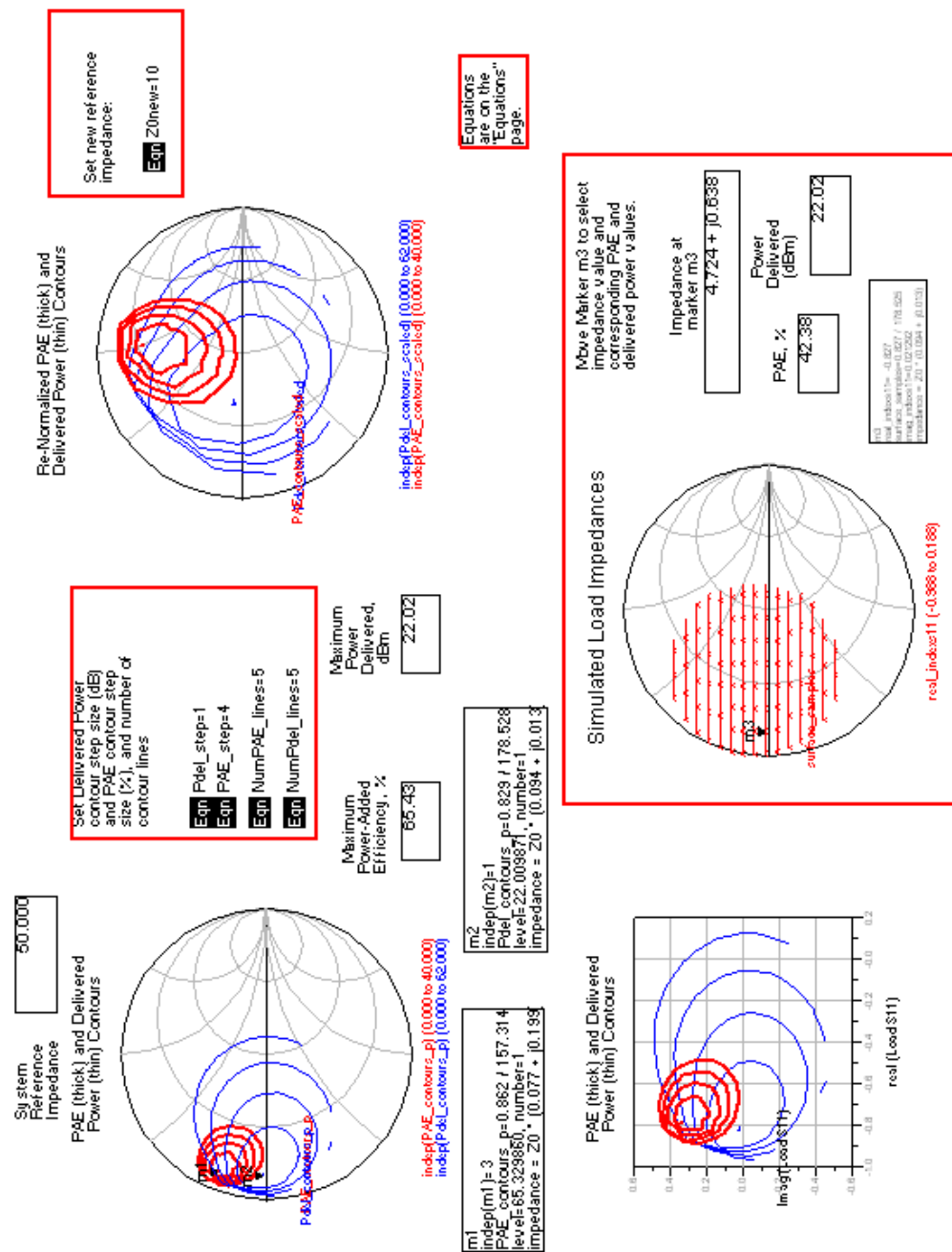


Figure 4.19 Negative Conductance Load Pull Results



Once an initial load impedance is chosen, the negative conductance amplifier is tested, without feedback or input networks, to determine the voltage amplitude required on the base to turn the transistor on. This value is used as a starting point for the  $\Delta V$  network. We will see later that the actual voltage attenuation used is slightly different due to inaccuracies in the expected input impedance of the transistor. The simulation schematic and results for this test are shown in Figure 4.20 and Figure 4.21. It is seen in Figure 4.21 that the magnitude of the output voltage begins to increase at an input voltage of 1.4V, corresponding to a magnitude of  $150\text{mV}_{\text{peak}}$  on the base of the transistor.

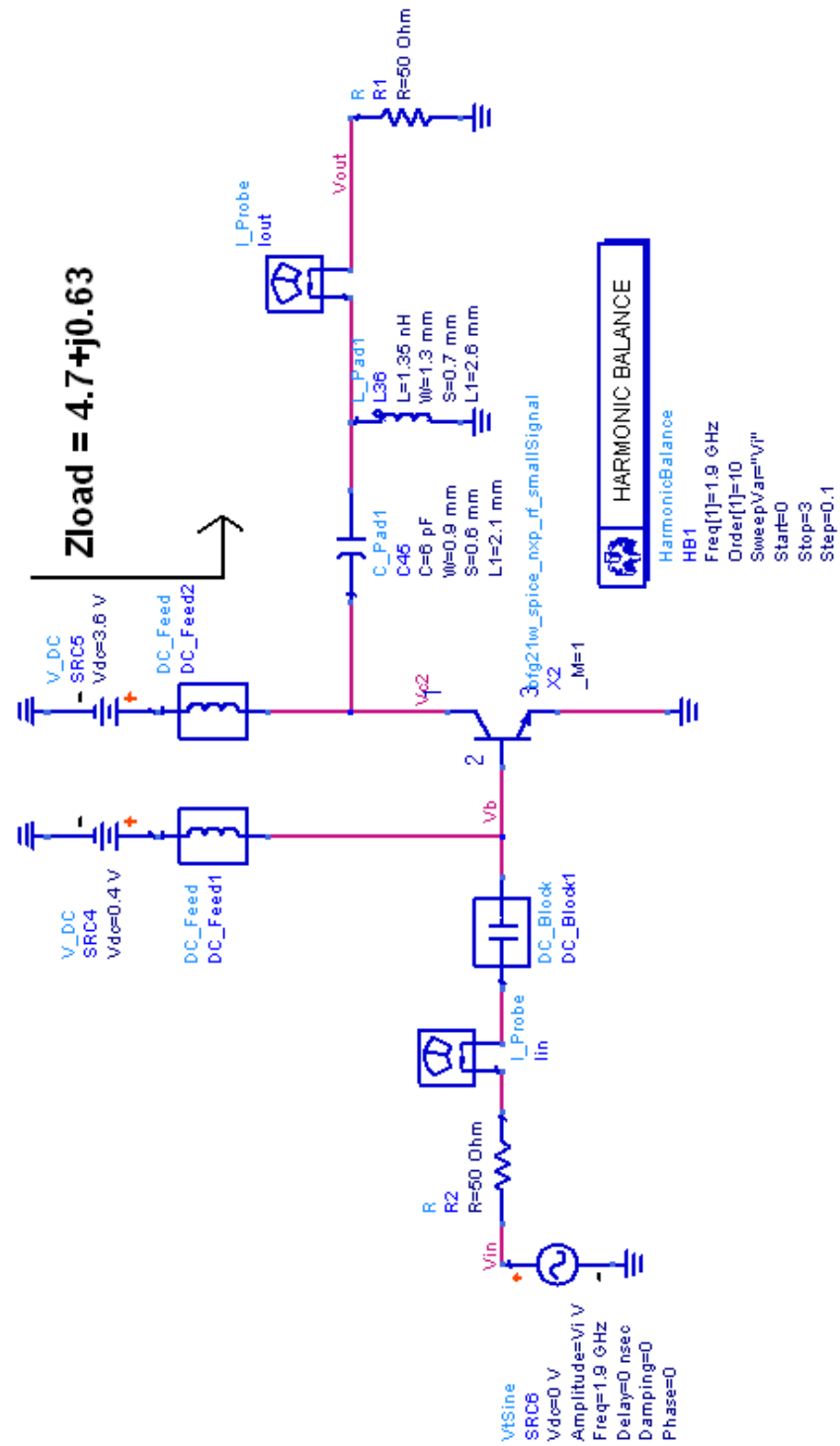


Figure 4.20 Schematic for Determining Turn On Voltage Amplitude of Class C Amplifier

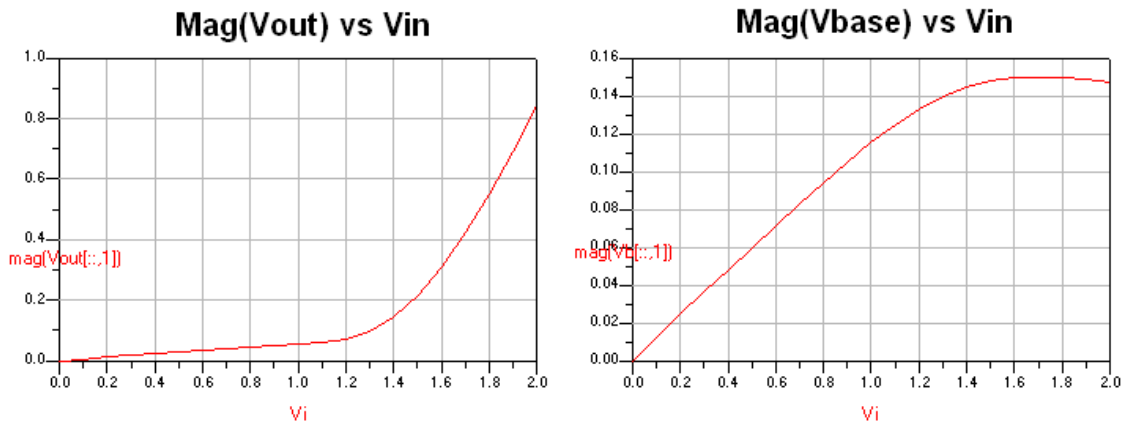


Figure 4.21 Turn On Voltage Amplitude Plots for Class C Amplifier

#### 4.3.3.1 $\Delta V$ and $\Delta\phi$ Networks

The  $\Delta V$  network is designed such that the output voltage during stage 1, just before saturation, is attenuated to the turn on voltage of the class C negative conductance amplifier. Figure 4.18 shows a maximum output voltage of about 6.8V just before saturation of the input amplifier. This leads to a desired  $\Delta V$  network corresponding to 0.022 V/V attenuation. This will provide 150mV at the base of the negative conductance transistor, entering stage 2 operation.

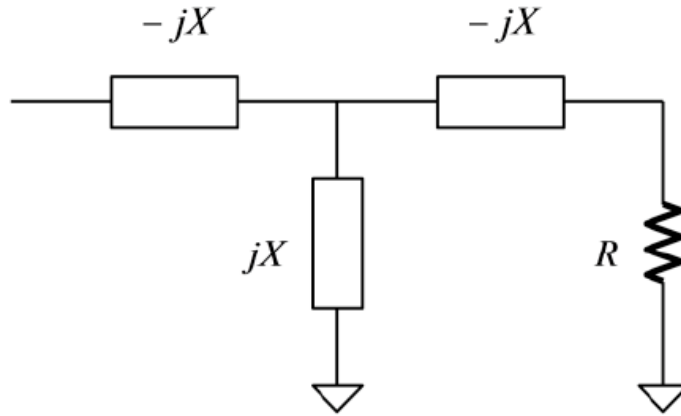


Figure 4.22  $\Delta V$  Network Block Diagram

Figure 4.22 is a generic block diagram for a  $\Delta V$  network with a constant phase shift. The reactance's,  $X$ , can be either capacitive or inductive and the value of  $X$  is chosen to achieve a desired voltage transfer. Equation 4.6 shows the design equations used for the  $\Delta V$  network to achieve the proper gain/loss.

- Input Impedance  $Z_{in} = \frac{X^2}{R}$
- Voltage Transfer Function  $\frac{V_{out}}{V_{in}} = j \frac{R}{X}$
- Voltage Gain/Loss  $\left| \frac{V_{out}}{V_{in}} \right| = \frac{R}{X}$
- Phase Shift  $\angle \left( \frac{V_{out}}{V_{in}} \right) = 90^\circ \times sig(X)$

Equation 4.6  $\Delta V$  Network Design Equations

The phase shifting network ( $\Delta\phi$ ) is needed to provide a  $360^\circ$  phase shift from the input of the  $\Delta V$  network to the output of the matching network. This is required so that the output of the negative conductance transistor does not add destructively with the output of the input amplifier. The  $\Delta\phi$  network can be tuned to add or subtract the desired amount of

phase to achieve an overall  $360^\circ$  phase shift while maintaining a unity voltage magnitude transfer function. Figure 4.23 shows a general block diagram of the phase shifting network, with Equation 4.7 showing the design equations.

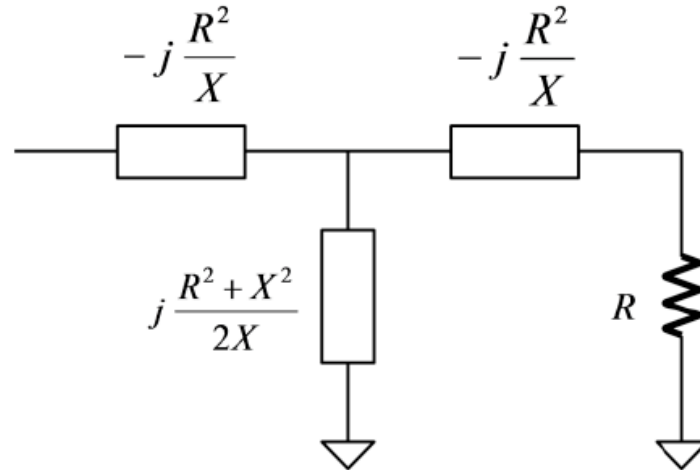


Figure 4.23  $\Delta\phi$  Network Block Diagram

- Input Impedance  $Z_{in} = R$
- Voltage Transfer Function  $\frac{V_{out}}{V_{in}} = \frac{X+jR}{X-jR}$
- Voltage Gain  $\left| \frac{V_{out}}{V_{in}} \right| = 1$
- Phase Shift  $\angle \left( \frac{V_{out}}{V_{in}} \right) = 2\arctan \left( \frac{R}{X} \right)$

Equation 4.7  $\Delta\phi$  Network Design Equations

It is noted that the input impedance of the  $\Delta\phi$  network is constant while the input impedance of the  $\Delta V$  network varies with the change in reactance value  $X$ . Due to this fact, the  $\Delta V$  network should be the first network in the forward path, followed by the  $\Delta\phi$  network and the negative conductance transistor. Using this order will lead to a single value of  $R$ , the input resistance to the transistor, used in the design equations. If the order

were reversed, the resistive load presented to the  $\Delta\phi$  network would depend on the voltage transfer of the  $\Delta V$  network, creating an extra level of complexity for the design of the  $\Delta\phi$  network.

It was decided to use capacitive impedances for the series components of both networks and inductive impedances for the shunt components in order to reduce the number of inductors in the circuit. There are equivalent Pi networks that could be used in place of the T networks; however, T networks were used to reduce the number of components going to ground. The schematic used for simulating the  $\Delta V$  and  $\Delta\phi$  networks with tunable components is shown in Figure 4.24.

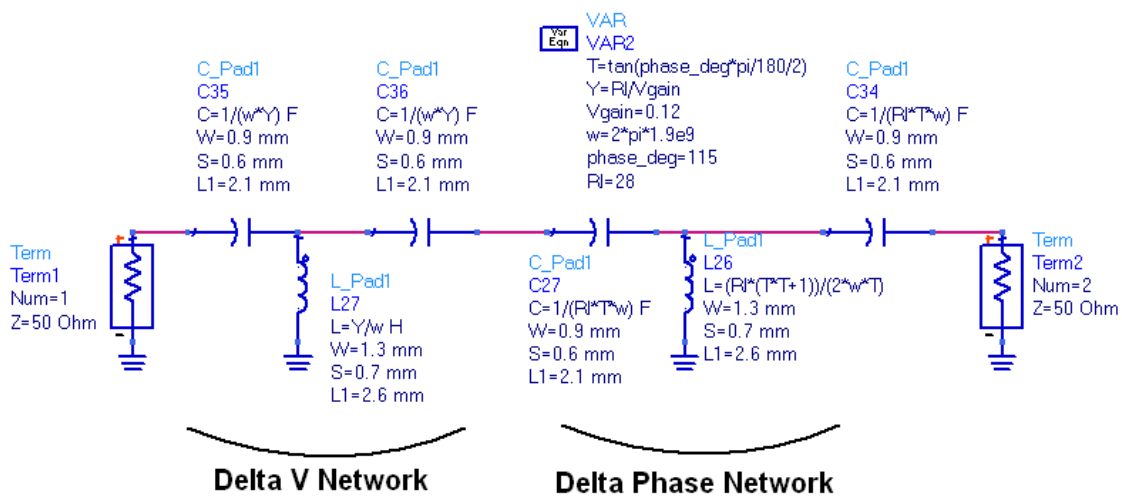


Figure 4.24  $\Delta V$  and  $\Delta\phi$  Network Schematic

The variable block VAR2 in Figure 4.24 contains the variables for selecting R, the expected input impedance of the transistor, as well as the variables for the gain and phase of each respective network. It can be calculated from Equation 4.6 that the component values for the  $\Delta V$  network are:

$$C = \frac{1}{\omega Y}$$

$$L = \frac{Y}{\omega}$$

**Equation 4.8  $\Delta V$  Component Values**

where  $\omega = 2\pi f$ ,  $Y = \frac{R}{V_{gain}}$ , R is the input resistance of the transistor, and  $V_{gain}$  is the voltage gain/loss desired in the  $\Delta V$  network.

Equation 4.9 shows the values for the  $\Delta\phi$  network components, as calculated from Equation 4.7.

$$C = \frac{1}{\omega RT}$$

$$L = \frac{R(T^2 + 1)}{2\omega T}$$

**Equation 4.9  $\Delta\phi$  Component Values**

Where  $T = \tan\left(\frac{\Delta\Phi}{2}\right)$  in degrees and  $\Delta\phi$  is the desired phase shift in degrees.

A simulation was ran to verify proper operation of the networks and the output is shown in Figure 4.25 and Figure 4.26. The voltage gain was swept from 0.1 to 2 and the phase change was swept from  $60^\circ$  to  $120^\circ$ . Note that the  $\Delta V$  network provides an additional constant phase shift, offsetting the output phase by  $90^\circ$ .

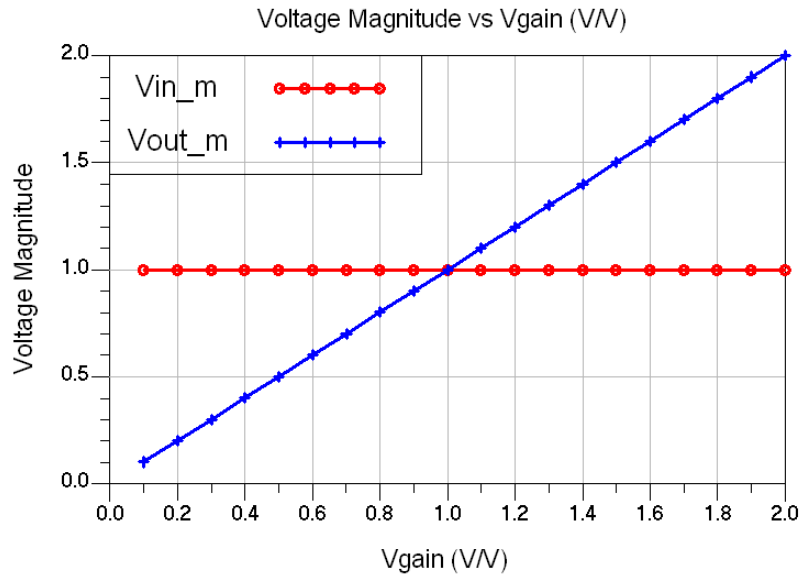


Figure 4.25 Verification of  $\Delta V$  Network Operation

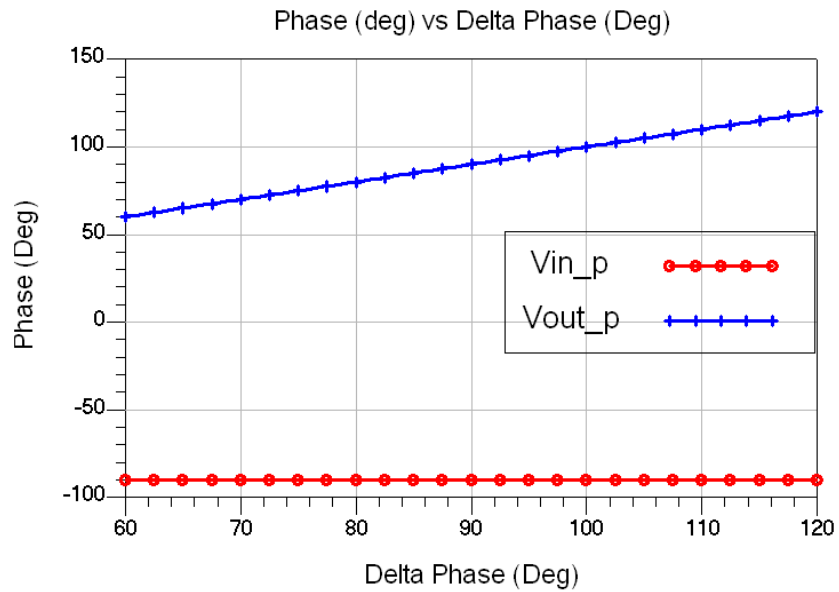


Figure 4.26 Verification of  $\Delta\phi$  Network Operation

Once the type of  $\Delta V$  and  $\Delta\phi$  networks have been chosen and verified through simulation, they are implemented into the negative conductance amplifier schematic. At this point, the feedback path is left unconnected in order to determine a starting point for the  $\Delta\phi$



network, fine tune the starting point for the  $\Delta V$  network, and determine a suitable input resistance  $R$ . Note that the input resistance of the transistor will vary with input drive power, especially due to class C operation, and is therefore an estimate at best. Figure 4.27 shows the schematic used during the initial testing of the negative conductance amplifier.

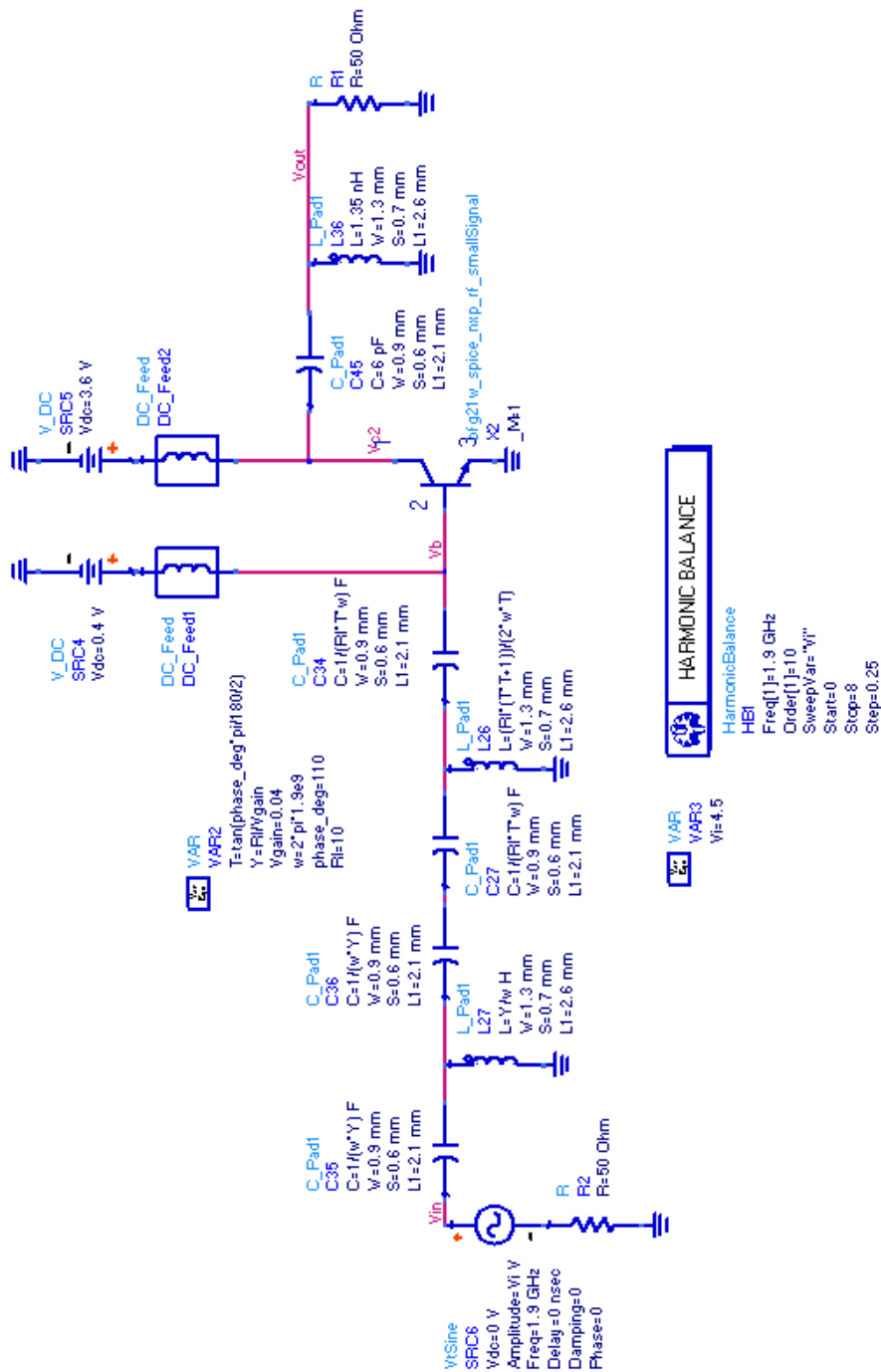


Figure 4.27 Negative Conductance Load with  $\Delta V$  and  $\Delta \phi$  Schematic, no Feedback

First, the  $\Delta V$  network was tested to fine-tune the expected attenuation value. Note that the input resistance of the transistor,  $R$ , was set to  $10\Omega$  as an initial guess. The input voltage,  $V_i$ , was swept from 0V to 8V and the value of  $V_{\text{gain}}$  was swept over the changing input voltages from 0.006 to 0.01. Figure 4.28 shows a desired  $V_{\text{gain}}$  value of 0.04 resulting in the transistor being fully turned on at an input voltage of 6.8V, the expected voltage at the transition from stage 1 to stage 2. However, it is also seen in Figure 4.28 that the output of the transistor saturates exceedingly fast with a very high voltage gain. This will result in a very small region of load modulation when implemented into the overall system. Therefore, the load presented to the transistor was moved away from the maximum power load by decreasing the value of the series capacitor. The amount of change from the maximum power load is left to the designer. However, it should be noted that changing the load will also change the phase shift from input to output, leading to a necessary change in the  $\Delta\phi$  network. For this design, we adjusted the capacitor value from 6pF to 2pF, resulting in a load of  $4.7-j27.28$ . The results of this new simulation, sweeping input voltage and  $V_{\text{gain}}$ , are shown in Figure 4.29.

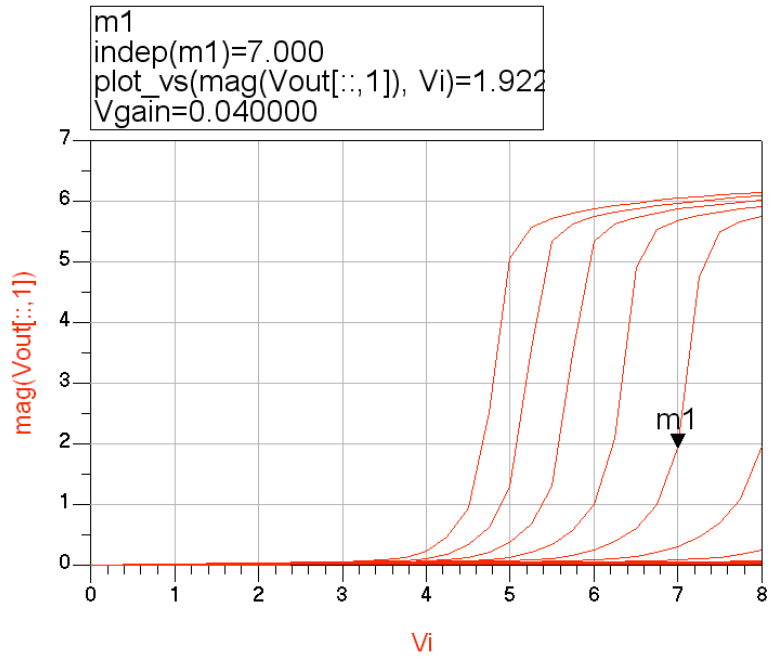


Figure 4.28 Simulation Results for Estimating  $\Delta V$  with Maximum Power Load

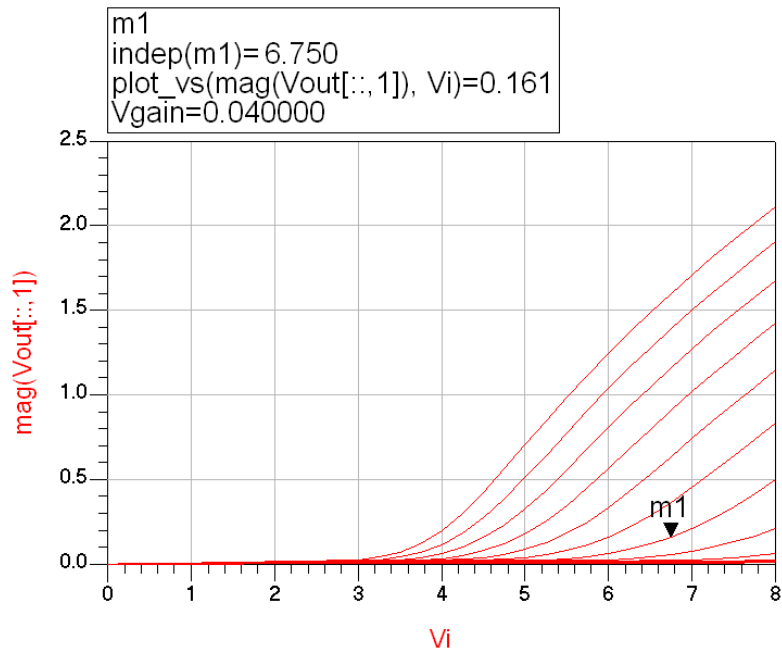


Figure 4.29 Simulation Results for Estimating  $\Delta V$  with Modified Load

The phase network is then fine-tuned to achieve a  $360^\circ$  phase shift from input to output. A voltage amplitude of 7V at 1.9GHz was applied to the input while sweeping the  $\Delta\phi$  value from  $60^\circ$  to  $120^\circ$ . As seen in Figure 4.30, the  $\Delta\phi$  network needs to provide an  $83^\circ$  phase shift in order to be in phase with the input voltage. It is also noted that the  $60^\circ$  sweep in  $\Delta\phi$  caused a  $90^\circ$  sweep on the output phase, with an unexpected phase change during the higher  $\Delta\phi$  values. This is caused by an inaccurate value for the input impedance of the transistor by assuming that the impedance is purely real. A more accurate sweep was achieved using an R value of  $5\Omega$ , however this value did not work well during the final circuit simulations and was therefore changed back to  $10\Omega$ .

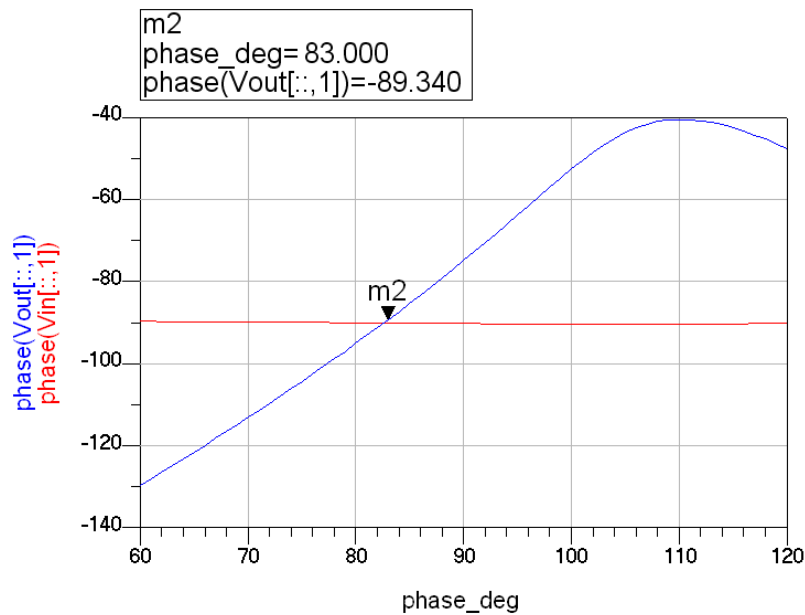


Figure 4.30 Simulation Result for Estimating Required  $\Delta\phi$  Value

#### 4.3.4 Complete System Design

Once the input amplifier has been designed and the negative conductance variables ( $\Delta V$ ,  $\Delta\phi$ ,  $V_{\text{bias}}$ , and  $Z_{\text{load}}$ ) have been estimated, both amplifiers are connected together with the

feedback path added to the negative conductance amplifier. It is expected that the load impedances to both the input amplifier and the negative conductance amplifier will change when connected together and therefore fine-tuning of the circuit variables will be required for the circuit to operate as desired. Figure 4.31 shows the final circuit schematic used for verifying the circuit operation.

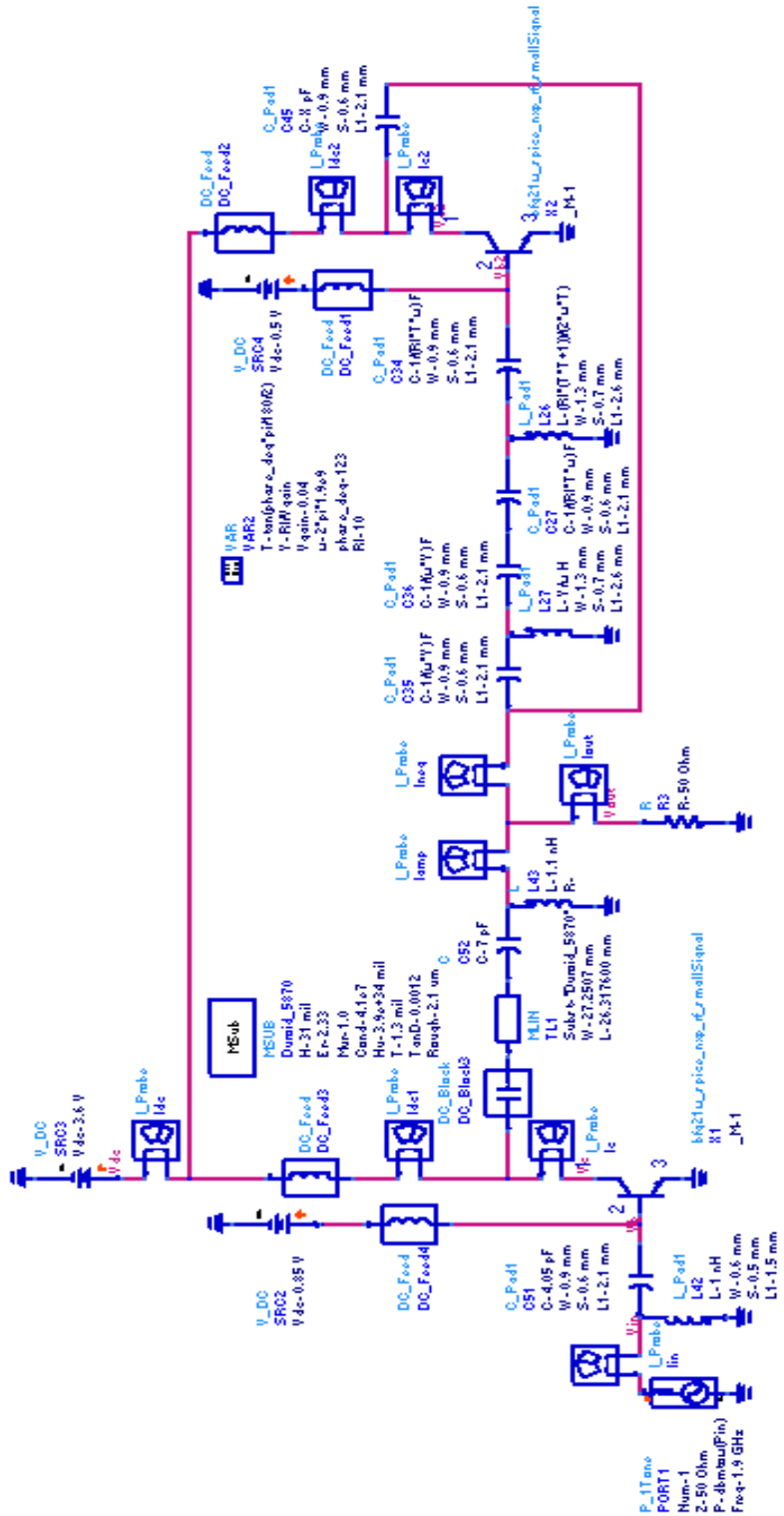


Figure 4.31 Negative Conductance Load Modulation Amplifier Schematic

Note that the shunt inductor in the negative conductance amplifier matching network has been removed in the final design. The shunt inductor in the matching network for the input amplifier is about the same value as the one designed for the negative conductance amplifier and was therefore used to serve as the shunt inductor in both matching networks. Simulations were run to verify improved performance with this inductor removed.

Because the impedances presented to the negative conductance amplifier are clearly different in the full design, the phase shift in the  $\Delta\phi$  network is first swept in order to determine a suitable phase shift. Shifting the phase too far one way or the other will shunt power from the input amplifier to ground, bypassing the RF load. Figure 4.32 shows the output power of the negative conductance amplifier in watts vs. input power, with several values of  $\Delta\phi$  simulated.  $\Delta\phi$  was swept from  $75^\circ$  to  $120^\circ$  in increments of  $5^\circ$ . The results show that the total power leaving the negative conductance amplifier decreases drastically when the phase shift is too small, sinking current for a large portion of time rather than sourcing current. An unexpected response is also shown in Figure 4.32; as the phase shift is decreased further away from the ideal shift, the negative conductance amplifier turned on at lower values of  $P_{in}$ . This may be caused by a change in the source impedance presented to the negative conductance amplifier.



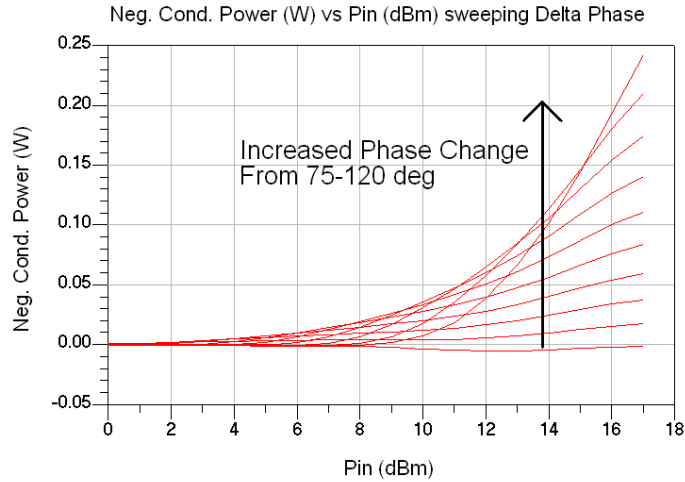


Figure 4.32 Negative Conductance Power with Swept  $\Delta\phi$  Values

The results of Figure 4.32 do not show an optimized value for  $\Delta\phi$  because the output power never plateaus with increased  $\Delta\phi$  to reveal a  $360^\circ$  total phase from input to output. However, the negative conductance amplifier turns on at an input power of 10dBm corresponding to  $\Delta\phi$  of  $120^\circ$ . This is the desired turn-on point, as discussed later in Section 4.3.5, and was therefore decided that the optimized value of  $\Delta\phi$  was near  $120^\circ$ .

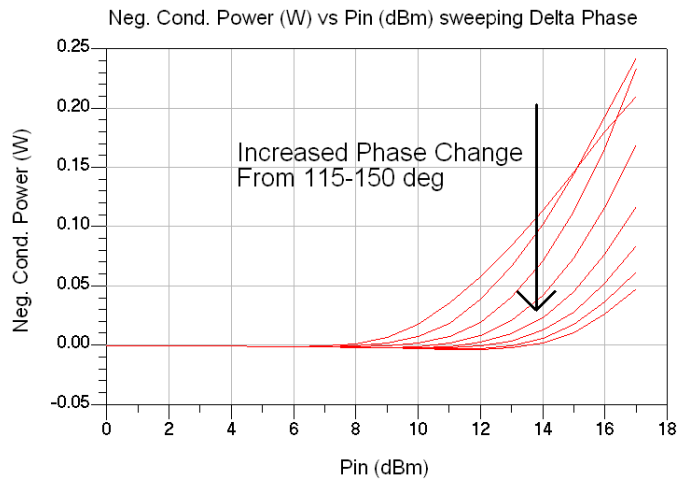


Figure 4.33 Negative Conductance Power with Larger Swept  $\Delta\phi$  Values

$\Delta\phi$  was then swept from  $115^\circ$  to  $150^\circ$  in increments of  $5^\circ$ , as shown in Figure 4.33. The plot shows that increasing the phase change further from  $120^\circ$  results in the negative conductance amplifier turning on later with a slower increase in provided power. The decreased rate of power is the result of sinking power from the input power, reducing the total power provided by the negative conductance load. A  $123^\circ$  phase shift was determined to be a suitable value for further simulations.

The value for  $\Delta V$  was then swept in order to further tune the required attenuation and set the turn on point of the negative conductance amplifier. This simulation was also run to verify the operation of the  $\Delta V$  network in the complete system. The turn-on point is particularly important in the design because it sets the boundaries of stage 1 and stage 2. If the attenuation of the  $\Delta V$  network is too small, the negative conductance amplifier will turn on too soon. This will reduce the amount of output power available from the overall system and lower the PAE. If the attenuation is too large, the negative conductance amplifier will not turn on before the input amplifier saturates completely, rendering the negative conductance amplifier useless. Therefore, setting the boundaries of each stage is a critical part of the amplifier design, especially for optimization of the amplifier performance.

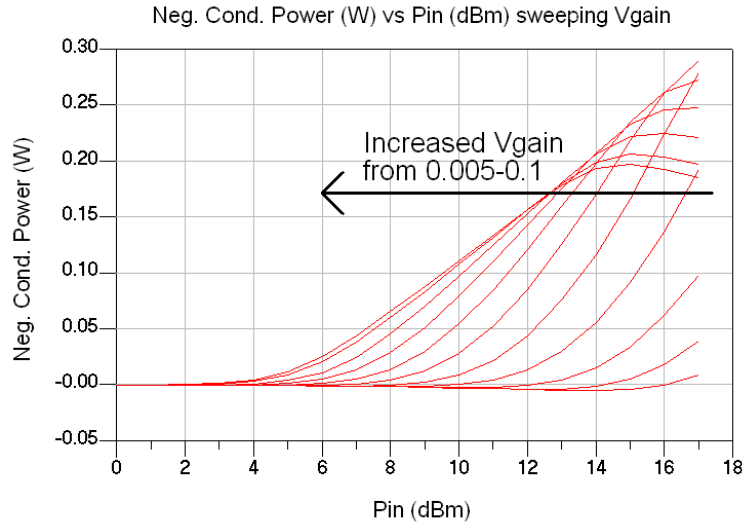


Figure 4.34 Negative Conductance Power with Swept  $\Delta V$  Values

Figure 4.34 shows the power provided by the negative conductance amplifier in watts vs. the input power in dBm, with several different values of  $V_{\text{gain}}$  simulated.  $V_{\text{gain}}$  was swept from 0.005 V/V to 0.1 V/V in increments of 0.01 V/V. This plot shows that the  $\Delta V$  network is working properly; as the value of  $V_{\text{gain}}$  is increased (less attenuation), the negative conductance amplifier turns on sooner. It was determined that a  $V_{\text{gain}}$  value of 0.04 was suitable for proper circuit operation.

The output capacitance in the negative conductance load matching network was then swept from 0.5pF to 5pF. The result of this sweep was as expected; an increased capacitance pushed the output load closer to the transistors maximum power load. This forced the transistor to have a very high gain for voltages large enough to turn the transistor on, reaching saturation very quickly. Figure 4.35 shows the output power of the negative conductance load increasing extremely fast with a small change in input power for larger values of output capacitance. The capacitance used for this design was 2pF.

Table 4.2 includes the final values chosen for negative conductance variables  $\Delta V$ ,  $\Delta\phi$ ,  $V_{\text{bias}}$ , and output capacitance.

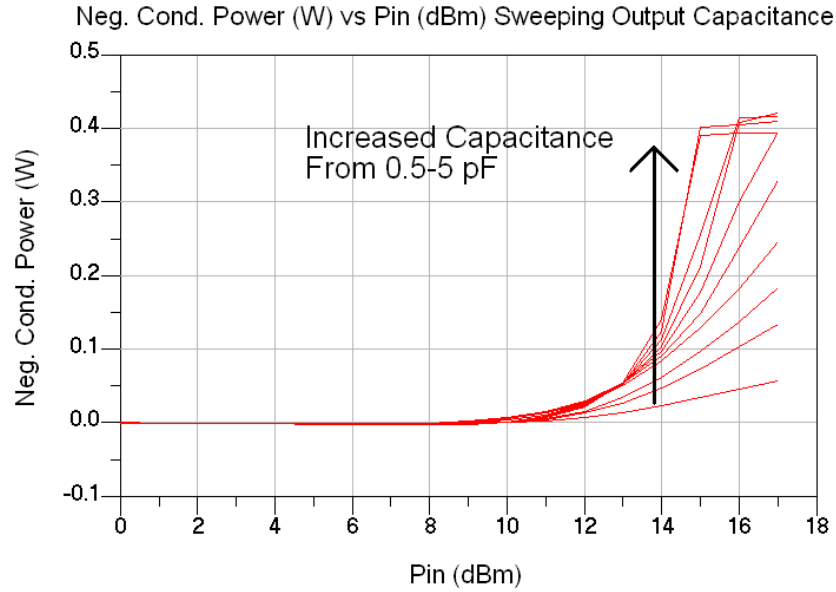


Figure 4.35 Negative Conductance Power with Swept Output Capacitance Values

Delta V (V/V)	0.04
Delta Phase (deg)	123
$V_{\text{bias}}$ (V)	0.5
C (pF)	2

Table 4.2 Tuned Negative Conductance Variables

### 4.3.5 Simulation Output and Performance

The following figures show key output plots that verify the operational theory of this design as well as the designs characterized performance.

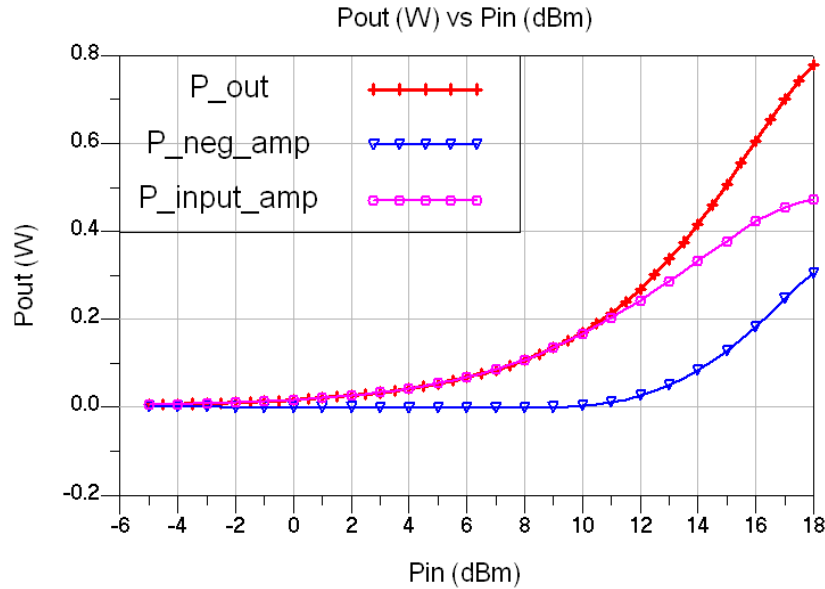


Figure 4.36 Selected Output Powers of the Complete System

Figure 4.36 shows the output power of the input amplifier, negative conductance amplifier, and overall system in watts vs. input power in dBm. The negative conductance amplifier is off during the lower power region, stage 1, and the output power tracks the input amplifier power. Figure 4.18 shows that the input amplifier begins to saturate at about 24dBm. Therefore it is desirable for the negative conductance amplifier to turn on just before this power level. Figure 4.36 shows the negative conductance amplifier begins to turn on at 10dBm input power, corresponding to an output power of 0.17W, or 22.3dBm.

Figure 4.37 below shows the output power of the complete system in dBm vs. input power in dBm. The 1dB compression point is determined to be 28.7dBm, an increase of 2.4dBm. This corresponds to an increase in power of 73.78%, or 173.78% of the total power available from the stand-alone input amplifier.

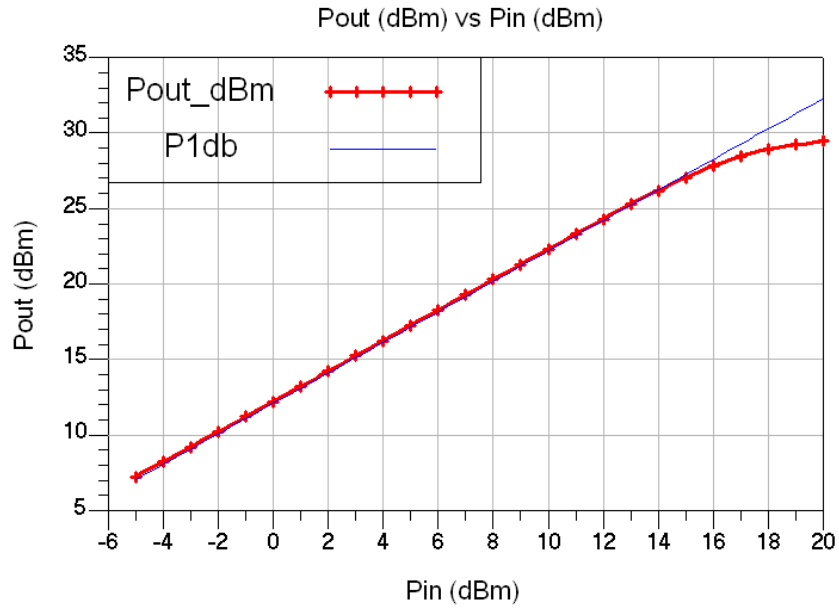


Figure 4.37 Output Power and 1dB Compression of Complete System

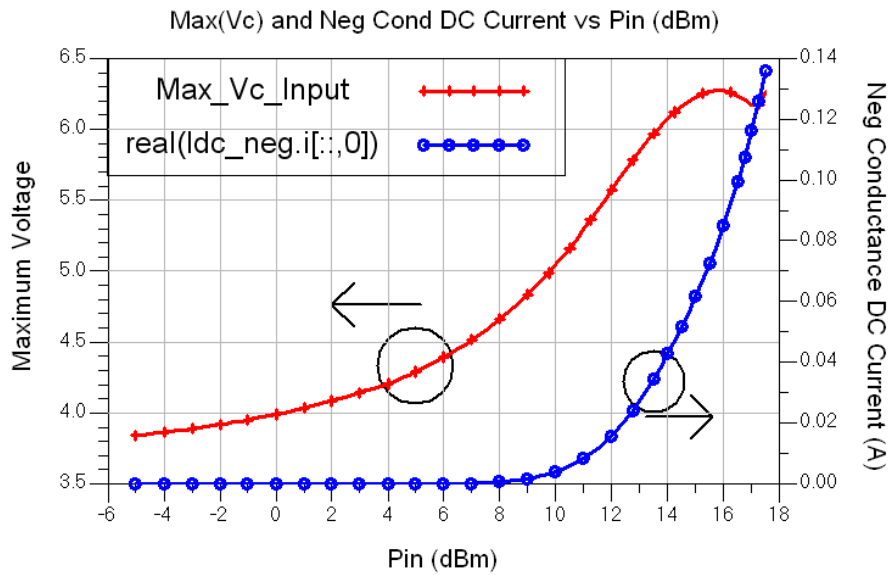


Figure 4.38 Maximum Collector Voltage and Neg. Conductance Amplifier DC Current

Figure 4.38 above shows that the negative conductance amplifier modulates the load presented to the input amplifier. The rate of change of the voltage on the collector of the input amplifier begins to slow as the negative conductance amplifier begins to turn on at

10dBm input power. The collector voltage begins to plateau at 14dBm input power where the negative conductance amplifier is fully turned on.

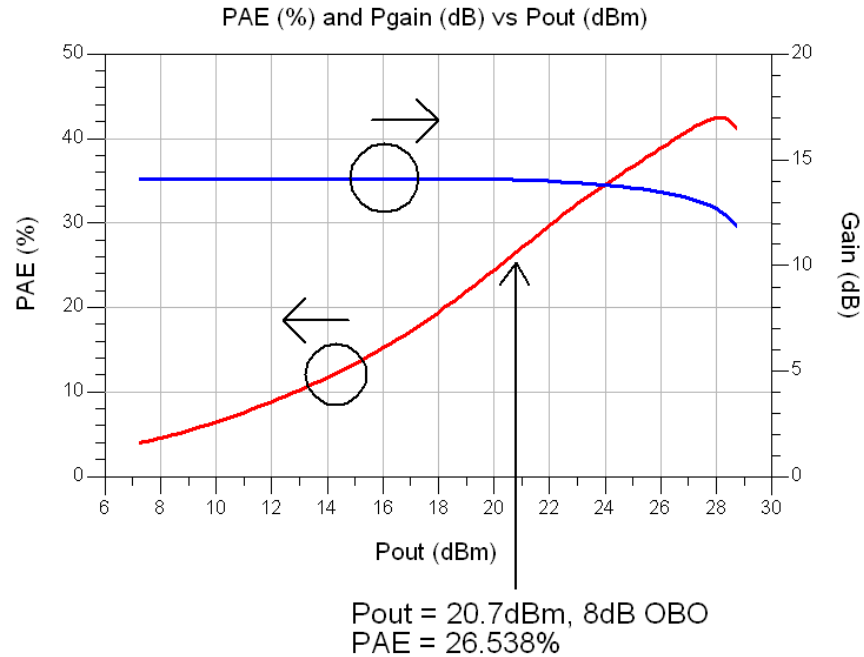


Figure 4.39 PAE and Power Gain Complete System

Figure 4.39 above shows the power added efficiency and power gain of the negative conductance amplifier. At an output back-off power of 8dB, 20.7dBm, the PAE is 26.538%, a significant improvement over a typical class AB amplifier. Comparing this with the research done at Seoul National University in Figure 3.5, we see an improvement over the Doherty Amplifier of about 3% and 10.5% over the class AB amplifier.

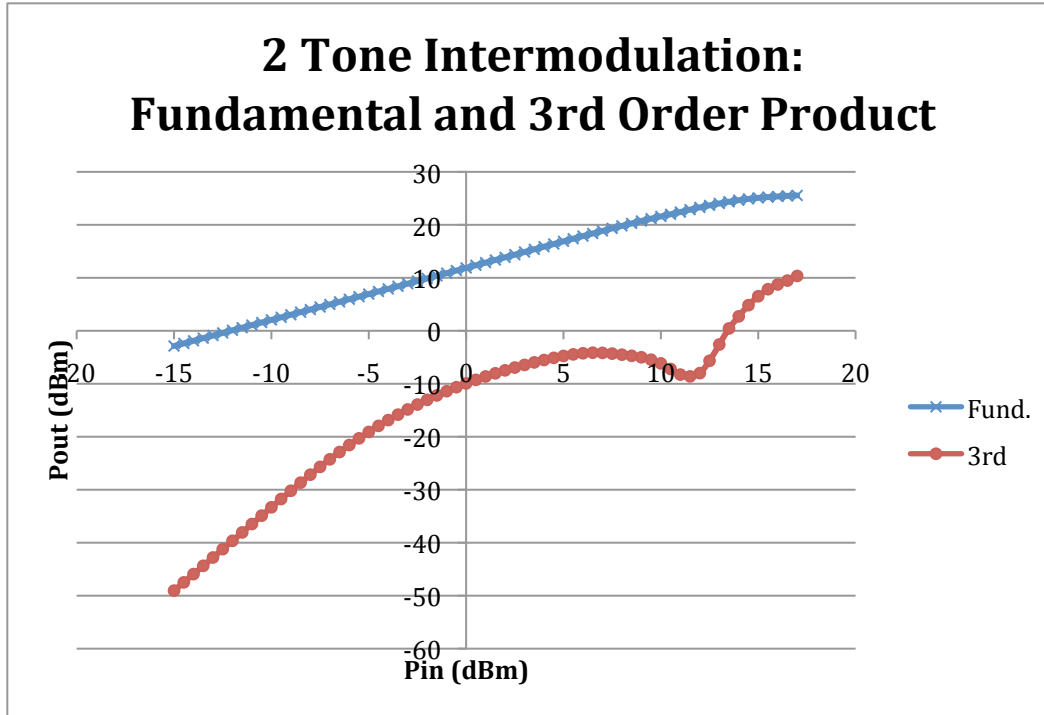


Figure 4.40 2-Tone Intermodulation of Complete System

Figure 4.40 is a plot of the 2 Tone Intermodulation Distortion of the complete system. At the maximum 2-tone output power, 25.5dBm, the 3<sup>rd</sup> order product of the two tones is only -15dBc. This is a significant amount of spectral noise outside the allotted bandwidth; however, it can be reduced with the addition of harmonic traps and filters. Filters and traps were not included in this design as the purpose was to validate the theory of operation. Figure 4.41 below also shows an undesired amount of AM-PM phase shift that should be addressed in a more refined design.



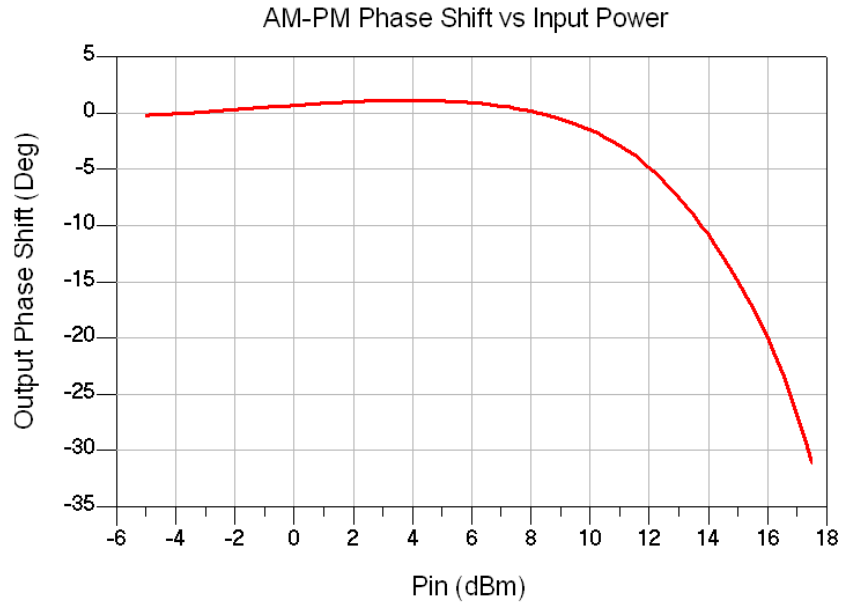


Figure 4.41 AM-PM Phase Shift of Complete System

#### 4.4 Experimental Results

A prototype of the presented amplifier was designed and a layout of the board was printed on Duroid 5870 PBC. It was found that the transistor model in ADS is not accurate enough, especially for load/source pull simulations and expected phase delays, to design a fully working system from simulation only. Three separate amplifiers were printed: a class AB amplifier, the input amplifier of the presented design without the negative conductance load, and the complete system. Note that the  $\lambda/4$  impedance inverter was modified for the prototyped version in order to reduce the width of the trace.

The presented amplifier achieved very low power gain when using the designed source and load impedances, on the order of 7dB. Because 7dB is not an acceptable gain, increasing the gain was the first modification of the design that I pursued. I ran a limited

version of a source and load pull experiment on the input amplifier as well as the complete system. I first swept the source impedance around different areas of the smith chart, attempting to find the central point for maximum gain as seen in the source pull simulations in Figure 4.14. A source impedance of  $7.347-j17.763$  was determined to be suitable, achieving a gain of 10.7dB.

I then swept the load impedance around the smith chart to find the maximum gain. Note that a maximum gain load impedance, as seen by the transistor through the impedance inverter, is not the ideal impedance for this design. Recall that the ideal load impedance is  $2R$ , where  $R$  is the optimum load impedance. However, the gain was too low at 10.7dB and therefore the maximum gain load was desirable at this point in the prototype.  $2.697-j1.024$  was determined to be a suitable load to present to the impedance inverter, producing an overall load impedance of  $87.979-8.688$  to the transistor after the impedance inversion. It is noted that the gain of the input amplifier only vs the complete system were very different throughout the load sweeps, revealing that the negative conductance load presented a significantly different impedance to the input amplifier when connected and turned off. With this new load impedance, the gain of the complete system was about 11dB.

It was found that the negative conductance load turned on but did not appear to extend the range of output power. This is most likely caused by an incorrect phase shift in the  $\Delta\phi$  network. I began sweeping the  $\Delta\phi$  value in an attempt to find the correct phase shift; however, at the time that the prototype was developed, there was a fundamental flaw in the  $\Delta\phi$  and  $\Delta V$  networks. The design value of  $R$ , the expected input impedance of the

transistor, was set at  $28\Omega$ . It was later discovered in simulation that this value was too large, producing an inaccurate phase shift, resulting in a large “luck factor” for finding the correct components in the  $\Delta\phi$  network. A future design is needed using the correct value of R. The gain of the amplifier, however, was affected significantly with adjustments to the  $\Delta\phi$  network, eventually achieving a maximum gain of 12.5dB.

After many different  $\Delta\phi$  values were attempted, it was decided that a new prototype is needed. Because the impedance inverter relies heavily on the load presented to it, modifying the input amplifier matching network shifted the design too far from the ideal theoretical design. A future prototype should be developed using experimentally measured phase delays and optimum load and source impedances. A few selected experimental results are shown below for measured gain values and negative conductance load dc current. Also, the design layout is shown in Figure 4.44.

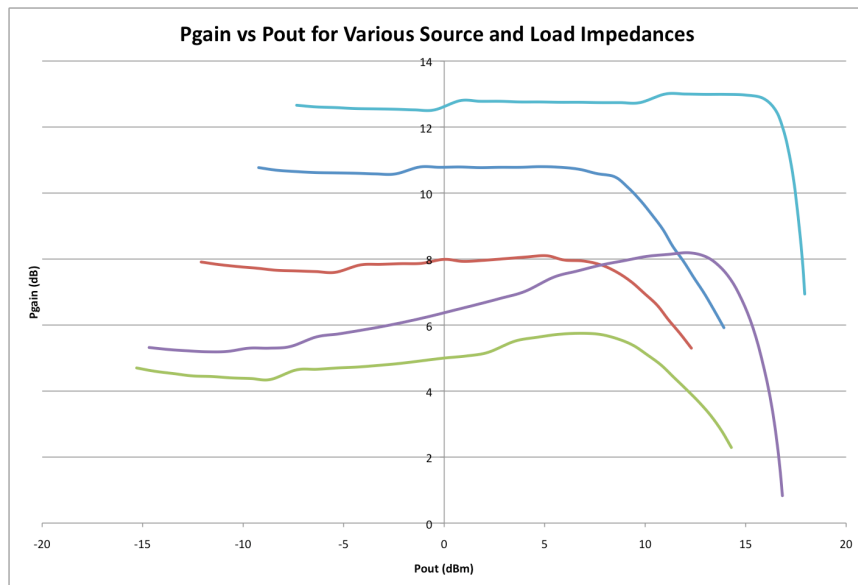


Figure 4.42 Experimental Pgain vs Pout for Various Source and Load Impedances

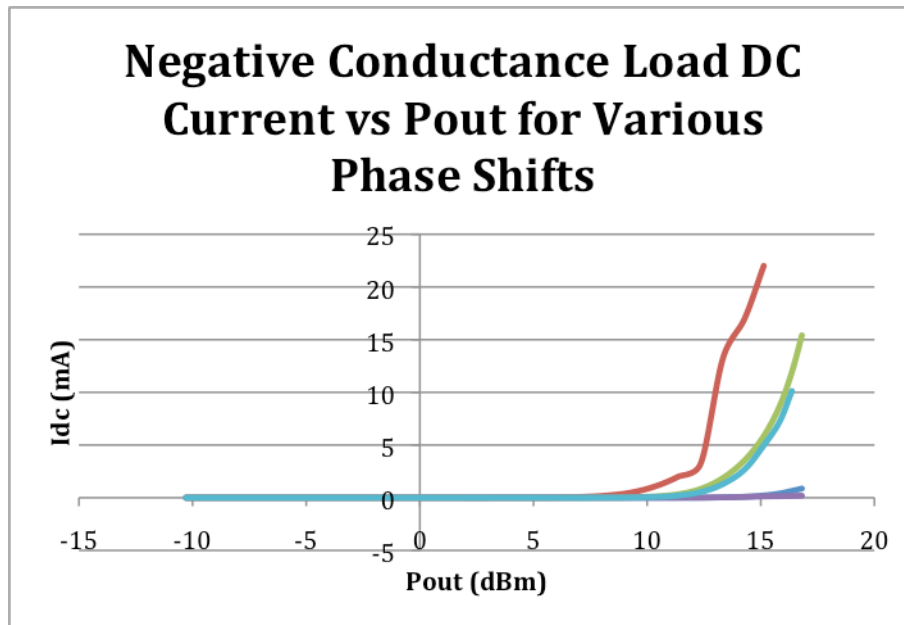


Figure 4.43 Experimental DC Current Through Neg. Cond. Load vs Pout

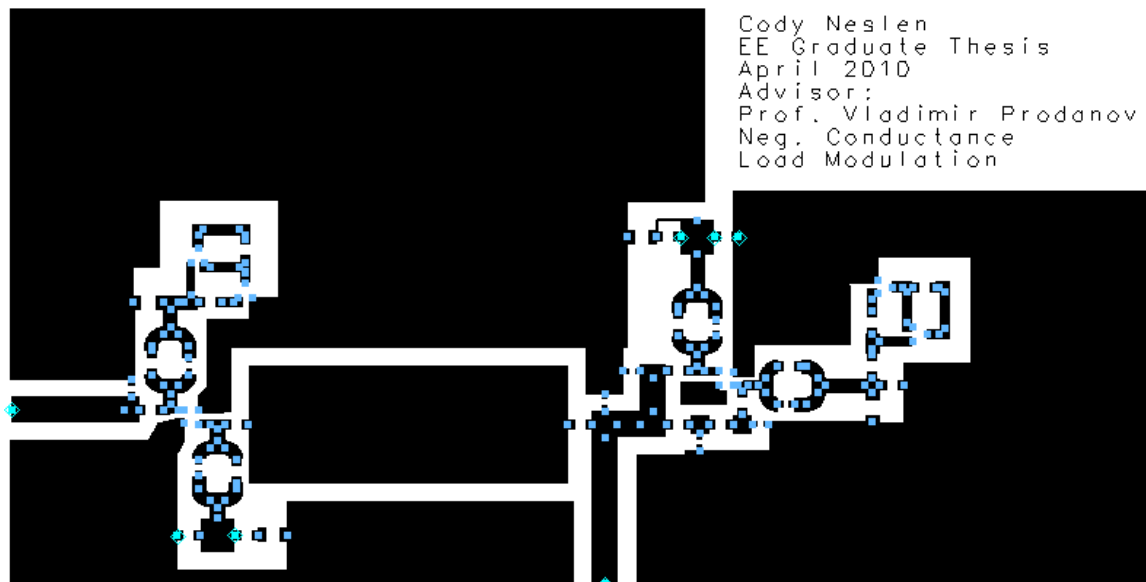


Figure 4.44 Prototype PCB Layout of Negative Conductance Load Modulation Amplifier

## 5 Conclusions and Future Work

The presented approach to designing the negative conductance load modulation amplifier proved successful. The negative conductance load modulation amplifier has an improved power added efficiency of about 11% with an output back-off power of 8dB over the popular class AB methods used today. The amplifier also has an increased PAE of 3% over a typical Doherty Amplifier. The negative conductance load provided an additional 2.4dBm power to the RF load, almost doubling the power from the stand-alone input amplifier.

The amplifier was shown to be particularly sensitive to the phase shift presented in the  $\Delta\phi$  network as well as the matching network presented to the negative conductance load. In a future implementation, the components chosen for this portion of the circuit should be considered critical tolerance components.

As stated in the introduction, the focus of this thesis is on concept validation, and not necessarily circuit optimization. While attempts were made to optimize the circuit performance, there is still much work needed in this area to reveal the strengths and weaknesses of this design. Figure 4.40 and Figure 4.41 reveal two areas of particular concern that need to be addressed in future work. The 2-Tone Intermodulation Distortion, showing -15dBc 3<sup>rd</sup> order product at maximum power, should be easily reduced with the addition of harmonic traps and filters. The phase distortion shown in the AM-PM plot must also be addressed to minimize the phase shift in the medium-to-high power range. One possible cause of the phase shift is due to the internal phase shift of the negative

conductance transistor during turn-on. As the transistor begins to turn on, the phase change from input to output varies until the transistor operates further from the knee voltage. A transistor with a more abrupt turn-on voltage or faster transition should be studied to view the differences in AM-PM distortion.

The design process presented in this project modified the variables in the negative conductance load while leaving the input amplifier components unchanged during the complete system tuning. Possible further optimization should be pursued within modifications to the input amplifier. The load presented to the input amplifier changes when connecting the negative conductance load, especially during stage 2 load modulation, and the effects of these changes should be studied. Also, presenting loads other than half the real part of the maximum efficiency load to the input amplifier should be studied.

While the experimental results were inconclusive for the first prototype, they did reveal that the negative conductance amplifier is turned off for lower power levels and turned on during higher power levels. A new prototype must be developed after experimentally measuring characteristics of the transistor, specifically the phase delay and optimum load and source impedances for large input signals. Also, a more accurate input impedance should be used for the prototype, a value closer to the  $10\Omega$  presented in the simulation design.

The goal of the final stage of design for the presented amplifier topology is to implement it into a monolithic microwave integrated circuit (MMIC). The presented design attempted to use components and design methods that are capable of miniaturization.

Further study is needed to understand the effects of miniaturization, including the possibility of standing waves and alternative methods for building a  $\lambda/4$  impedance inverter.

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