Review
Chinese Science Bulletin
SPECIAL TOPIC
Carbon Nanotubes
January 2012 Vol.57 No.2-3: 135–148
doi: 10.1007/s11434-011-4791-6

High-performance doping-free carbon-nanotube-based CMOS devices and integrated circuits

ZHANG ZhiYong*, WANG Sheng & PENG LianMao

Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing 100871, China

Received April 7, 2011; accepted July 20, 2011; published online November 4, 2011

Ballistic n-type carbon nanotube (CNT)-based field-effect transistors (FETs) have been fabricated by contacting semiconducting single-walled CNTs (SWCNTs) using Sc or Y. The n-type CNT FETs were pushed to their performance limits through further optimizing their gate structure and insulator. The CNT FETs outperformed n-type Si metal-oxide-semiconductor (MOS) FETs with the same gate length and displayed better downscaling behavior than the Si MOS FETs. Together with the demonstration of ballistic p-type CNT FETs using Pd contacts, this technological advance is a step toward the doping-free fabrication of CNT-based ballistic complementary metal-oxide-semiconductor (CMOS) devices and integrated circuits. Taking full advantage of the perfectly symmetric band structure of the semiconductor SWCNT, a perfect SWCNT-based CMOS inverter was demonstrated, which had a voltage gain of over 160. Two adjacent n- and p-type FETs fabricated on the same SWCNT with a self-aligned top-gate realized high field mobility simultaneously for electrons (3000 $cm^2 V^{-1} s^{-1}$) and holes (3300 $cm^2 V^{-1} s^{-1}$). The CNT FETs also had excellent potential for high-frequency applications, such as a high-performance frequency doubler.

carbon nanotube, field-effect transistor, doping-free, complementary metal-oxide-semiconductor, high frequency

Citation: Zhang Z Y, Wang S, Peng L M. High-performance doping-free carbon-nanotube-based CMOS devices and integrated circuits. Chin Sci Bull, 2012, 57: 135–148, doi: 10.1007/s11434-011-4791-6

Carbon nanotube (CNTs) are hollow cylinders that have been rolled from single- or multi-layer graphene, and they have drawn tremendous attention since they were observed for the first time by Iijima in 1991 [1]. There are two categories of CNTs according to the number of shells: single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs) [2]. A SWCNT is an ideal one-dimensional conductor that typically has a diameter of 1–3 nm and a length of up to several millimeters [3]. Depending on the way that it is rolled from graphene, which can be characterized by the chiral index (n, m), a SWCNT can be a metallic or semiconducting with a band gap inversely proportional to its diameter [2,4]. Metallic CNTs can be used as interconnecting wires in integrated circuits owing to their ultra-strong ability to carry current with density up to 1×10^9 A/cm^2 [2,5]. Semiconducting CNTs have been considered ideal materials for high-performance nanoelectronics owing to their perfect combination of small size, extremely high carrier mobility and long mean-free-path length, large current density, small intrinsic gate delay and high intrinsic cut-off frequency [6–9].

It is well known that silicon complementary metal-oxide-semiconductor (CMOS) technology will reach its physical and technological limits in the very near future, said to be 2020 [10–12]. A new technology must then replace silicon CMOS technology to extend Moore's law. Building field-effect transistors (FETs) on semiconducting materials other than silicon, such as carbon nanotubes [6–9], nanowires [13], and III–V compound semiconductors [14], in which carriers including electrons and holes would flow faster, could be a way to extend Moore's law in the post-CMOS era [12]. Compared with other semiconductors, SWCNTs present ultra high electron mobility, exceeding 100000 $cm^2 V^{-1} s^{-1}$ even at room temperature [15], as well as similarly high

*Corresponding author (email: zyzhang@pku.edu.cn)

mobility for holes. Moreover, owing to their cylindrical structure, CNTs are suitable for building gate-all-around FETs to further improve transconductance [16]. Additionally, compared with their carbon cousin graphene [17], CNTs are more suitable for digital applications, which require a transistor with a larger on/off current ratio, because of the existence of a band gap.

1 n-Type CNT FET and n-type ohmic contact

The first CNT-based FET was fabricated by researchers at Delft University of Technology in the Netherlands in 1998 [18], and the design of carbon-based devices including those made of CNTs and graphene subsequently became the hottest field in nanoelectronics in the past ten years. It is worth noting that the FETs were almost all p-type (i.e., FETs having an abundance of holes) originally, with very large Schottky barriers at contacts. The devices thus performed very poorly owing to poor contacts, which induced small current of tens of nanoamps, and had very low speed.

1.1 Operation principle of CNT FETs

Unlike conventional Si-based metal-oxide-semiconductor (MOS) FETs, for which the polarity of the transistor is determined by doping the conduction channel of the device with suitable dopant atoms, FETs built on intrinsic SWCNTs were found to be Schottky-barrier FETs, for which the polarity of the FETs can be determined by controlling the injection of carriers to the channel [19–22]. The control of the majority carrier type in a semiconducting CNT channel (i.e., electron (n-type) or hole (p-type)) is realized here by the selective injection of electrons or holes into the CNT. If a metal with a high work function is used to contact with the CNT, the Fermi level of the electrode will be close to the valence band of the CNT, affording a smaller Schottky barrier for the hole than for the electron. Therefore, holes are injected into the channel more easily than electrons, and the transistor is a p-type transistor [18–23]. In the same way if a low-work-function metal is used to contact with the CNT, the Fermi level of the electrode will be close to the conduction band of the CNT, leading to an n-type transistor. Initially, stable metals such as Pt and Au were chosen for contact electrodes in CNT FETs [18,23], and the FETs were generally p-type owing to these contacting metals having high work functions exceeding 4.5 eV, which is the work function of an intrinsic CNT. In accordance with this principle, CNT FETs fabricated with high-work-function metals as contacts were surely p-type, while those contacted with low-work-function metals such as Al and Ca were n-type [24,25]. Devices using Ti for contact electrodes were ambipolar FETs owing to the equal Schottky barrier height for the electron and hole [19–22].

It is well known that since there are generally plenty of interface states, the height of the Schottky barrier between the metal and planar semiconductor is not sensitive to the work function of the metal owing to Fermi-level pinning. Therefore, the Schottky barrier height cannot be controlled or adjusted by only selecting the metal for conventional metal-semiconductor (MS) contacts [26]. Fortunately, for a one-dimensional channel such as a CNT, Fermi-level pinning at the metal-CNT interface is weak [27]. This is because in a one-dimensional channel, any interface-state-induced potential change (due to interface dipoles, for example) decays to zero rapidly away from the interface. The Schottky barrier at the metal-CNT interface is thus much thinner than that for a three-dimensional channel and carrier tunneling through the Schottky barrier is important in CNT devices. The Schottky barrier height is primarily governed by the energy difference between the Fermi level of the metal electrode and the position of the valence (p-type) or conduction (n-type) band edge of the CNT. A metal with a large work function, such as Pt (5.65 eV), Au (5.1 eV) or Pd (5.1 eV), thus tends to line up with the valence band of the CNT and forms a p-channel for hole transport through the CNT [18,23,28].

1.2 n-Type ohmic contact

Ohmic contact is a prerequisite condition for fabricating high-performance FETs. As opposed to the conventional method of forming ohmic contact by heavily doping a semiconductor, ohmic contact on CNTs can only be realized by selecting a metal with a work function high or low enough to form a zero or negative Schottky barrier to the carrier since the stable doping of CNTs is not possible. Although the polarity of CNT FETs is affected by the work function of contact electrodes, the work function is not the only factor determining the Schottky barrier at the metal-CNT interface. Therefore, real ohmic contact for CNT FETs was not realized until 2003, when Dai [29] found that palladium can form an excellent p-type ohmic contact with CNTs. The first ballistic CNT FET transistor was then demonstrated at room temperature. For example, the ON-state conductance increased with decreasing temperature and approached the quantum limit at low temperature. Afterward, other metals such as Rh were found to form an ohmic contact with CNTs [30], and the problem of p-type ohmic contact for CNT FETs was completely solved. Compared with p-type ohmic contact, n-type ohmic contact for CNT FETs was difficult to achieve. Although Al and other low-work-function metals were used to contact CNTs and an obvious n-type field effect was observed, large Schottky barriers still existed between the contacts [24,25]. A breakthrough for n-type CNT FETs was not achieved until the end of 2007, when Sc was found to form ideal n-type ohmic contact with CNTs [31]. The excellent performance of the Sc-contacted n-type CNT FETs is due to several favorable factors, including a suitable low work function of about 3.3 eV, and excellent wetting

with the CNT (Figure 1(a)). The properties of Sc-contacted CNT FETs are shown in Figure 1. The device is an n-type FET having an ON state at high V_{gs} (~10 V) and near-ballistic ON-state conductance $G_{on} = 0.49G_0$ ($G_0 = 4e^2/h$) at 250 K (Figure 1(b)). The ON-state conductance increases with decreasing temperature and reaches $G_{on} = 0.62G_0$ at 4.3 K. The metallic-like temperature dependence of the ON-state conductance and the almost perfectly linear I_{ds}-V_{ds} characteristics suggest that electron injection from the Sc electrode into the conductance band of the CNT is effectively barrier free; i.e. Sc forms an ohmic contact with the n-channel (i.e., the conduction band) of the CNT. At low temperature (4.3 K, Figure 1(c)), the I_{on}/I_{off} ratio exceeds 10^9 for $V_{ds} = 0.1$ V.

Although Sc is an ideal electrode metal for n-type CNT FETs, its exorbitant price and scarcity will prevent large-scale applications in the future. Yttrium (Y) was then used to substitute Sc as the contacts for CNT FETs. The performance of the Y-contacted CNT FET was compared directly with that of the Sc-contacted CNT FET, with the FETs fabricated on the same SWCNT adjacent to each other, and was found that the Y-contacted CNT FETs outperform in many ways the Sc-contacted CNT FETs [32]. Since Y is extremely cost effective and widely used in industry, it is expected that Y-contacted devices will be more suitable for fabricating large-scale integrated nanoelectronic circuits.

2 Pushing n-type CNT FETs to their performance limits

In the two years following the realization of p-type ohmic contacts for CNT FETs, Dai and coworkers [33,34] pushed the performance of the p-type CNT FET to its limit by combining ohmic contacts and a high-k gate insulator.

The development of n-type FETs lagged far behind the development of p-type FETs. Traditionally, n-type CNT FETs were fabricated through chemical doping such as doping with K [35]. However, there were two obvious disadvantages of chemically doping CNTs. Firstly, it is uncontrollable and unstable in air. Secondly, the doped atom in the CNT reduces carrier mobility by introducing scattering.

In 2005, researchers at Intel benchmarked CNT devices of the day with some key general parameters including gate delay and the energy-delay product [36]. The intrinsic gate delay represents the speed potential of a device, and the energy-delay product indicates its power dissipation. They found that the p-type CNT devices outperformed the silicon p-MOS in terms of both speed and power dissipation.

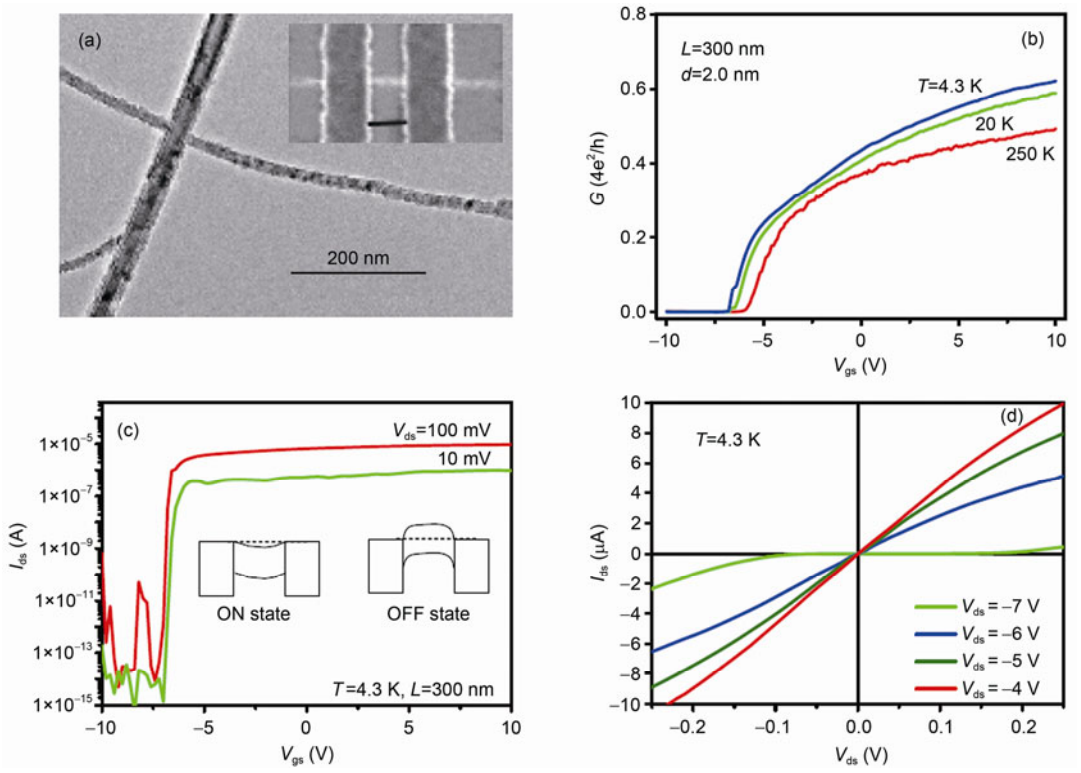

Figure 1 Back-gated SWCNT-based n-type CNT FET. (a) Transmission electron microscope image showing uniformly Sc-coated CNTs of various diameters; insert: scanning electron microscope image of the device; the bar is 300 nm in length. (b) Low-bias conductance G vs gate voltage V_{gs} for an SWCNT with diameter $d = 2.0$ nm and length $L = 300$ nm. (c) Transfer characteristics of the same device as in (b) for different bias at 4.3 K. Inset: schematic ON- and OFF-state band diagrams for a device with no Schottky barrier against electron injection into the conduction band of the CNT. (d) I_{ds}-V_{ds} curves for different V_{gs} at 4.3 K [31].

However, the n-type CNT FETs were far inferior to n-type Si MOS FETs owing to the lack of good contacts.

2.1 Compatibility of the Sc contact and high-κ insulator

In addition to the good contact, a high-quality gate insulator is another key component for high-performance FET devices, especially for high transconductance [37]. High-κ (being the dielectric constant of the dielectric layer) insulators such as HfO_2 were successfully integrated in Pd-contacted CNT FETs through atomic layer deposition (ALD) at low temperature, such as 90°C, and the p-type FETs exhibited excellent ON-state (characterized by transconductance) and OFF-state (characterized by subthreshold swing) properties without obvious degradation of contact quality [33]. In the same way, the performance of Sc-contacted n-type CNT FETs was further improved by integrating HfO_2 High-κ dielectrics as the gate insulator.

Although various high-κ dielectrics have been demonstrated to be technically compatible with carbon-based devices [33,34], it has proven to be very difficult to grow uniform thin high-κ film directly on the surface of CNTs via a general method, such as ALD. This is because of a good-quality CNT or graphene, there is only a delocalized π bond on the surface of the sp^2 hybridization plane, and not many nucleation sites; e.g., defects or dangling bonds [38]. Growing a thick gate dielectric via ALD to bury CNTs is one way to produce a top-gate high-κ dielectric in CNT FETs [33–35,38]. This method is simple to implement but simultaneously limits the ultimate scaling down of the thickness of the gate dielectric. For example, ALD-grown HfO_2 film thicker than 8 nm is needed to fully cover a CNT and to avoid gate leakage [38]. As a result, the corresponding subthreshold swing of the CNT FET fabricated this way remains considerably higher than the theoretical value; i.e., 60 mV/decade.

To realize direct nucleation on the surface of CNTs and consequently grow a uniform high-κ film, several methods have been developed that build nucleation sites via surface treatments before ALD growth. These methods include functionalizations with the introduction of perylene tetracarboxylic acid, deoxyribonucleic acid, NO_2, and O_3. The introduction of noncovalent functionalization layers (NCFLs) or pre-treatments not only adds technical complexity but also affects the transport properties of the fabricated CNT and graphene FETs, leading to electric field variation and extra scattering due to the functionalization molecules, and sometimes even damage to the sp^2 carbon framework.

High-quality yttrium oxide (Y_2O_3) is investigated as an ideal high-κ gate dielectric for carbon-based electronics through a simple and inexpensive process. Utilizing the excellent wetting behavior of Y on an sp^2 carbon framework, ultra-thin (a few nanometers) and uniform Y_2O_3 layers have been directly grown on the surfaces of CNTs and graphene without using noncovalent functionalization layers or introducing large structural distortion and damage. A top-gate CNT FET adopting a 5 nm Y_2O_3 layer as its top-gate dielectric has excellent device characteristics, including an ideal subthreshold swing of 60 mV/decade (up to the theoretical limit of an ideal FET at room temperature) as shown in Figure 2 [39].

2.2 Self-aligned gate

In state-of-the-art silicon CMOS technology, a self-aligned structure is used to ensure the accuracy of the entire fabrication process. As the size of the device becomes smaller and smaller, there is a need for a more precise and reliable way to fabricate MOS FETs automatically, and the self-aligned structure ensures that the edges of the source (S), drain (D) and gate (G) electrodes are precisely and automatically positioned such that no overlapping or significant gaps exist between these electrodes. The use of self-aligned gates is one of the many innovations that have enabled computing power to increase steadily over the last 40 years. A self-aligned structure is therefore necessary for the massive fabricating of high-performance CNT FETs and for the construction of CNT-based CMOS integrated circuits.

A self-aligned structure that utilizes the existence of the native oxide on the surfaces of certain metals, such as Al_2O_3 on Al, has been developed and used to fabricate near-ballistic p-type CNT FETs with near ideal performance [34]. However, this self-aligned structure is not suitable for n-type devices. A novel self-aligned gate structure that is suitable for fabricating both n- and p-type CNT FETs with a desired threshold voltage and indeed for any FETs based on one-dimensional nanomaterials has been presented [40]. For this self-aligned structure, we take advantage of the different growth mechanisms of HfO_2 and Ti films. While the ALD-grown HfO_2 film is continuous with excellent thickness uniformity and step coverage (i.e., uniform film is present even on the sidewalls of the S and D electrodes, which effectively insulates G from S and D), the Ti film grown via e-beam evaporation is basically two-dimensional and is not present on the sidewalls of the S and D electrodes, and therefore, the part of the Ti film between S and D is disconnected from that on top of the S and D or on top of the poly(methyl methacrylate) that defines the gate window. The so-fabricated final structure has precisely positioned edges of the S, D, and G electrodes, and its electrical properties are shown in Figure 3. Both near-ballistic (with a channel length L~120 nm) and long-channel (with L~2 μm) n-type CNT FETs are fabricated with this structure on a single SWCNT with a diameter of ~1.5 nm. Quantitative fitting of the electric characteristics of the long-channel FETs reveals high electron mobility exceeding 4650 $cm^2\ V^{-1}\ s^{-1}$ and a mean-free path $l_m = 191$ nm as shown in Figure 4. A careful evaluation of the 120 nm devices shows that the self-aligned gate can effectively control the channel yielding a very small gate delay time of 0.86 ps and a large

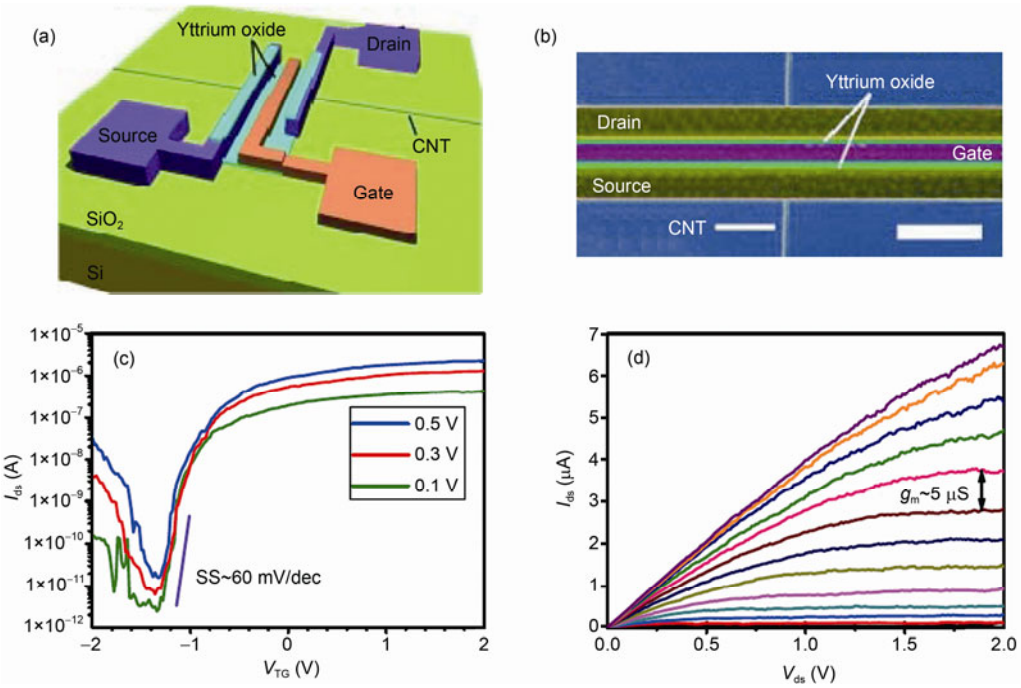

Figure 2 Device geometry and performance of a top-gate CNT FET with a thin layer of Y_2O_3 as the top gate dielectric. (a) Schematic diagram of the device structure. (b) Scanning electron microscope image of an as-made CNT FET device, with the scale bar denoting 4 μm. This CNT device is based on an SWCNT with diameter of 1.2 nm; the channel length of the device is 2 μm and the top-gated length is 1 μm. (c) Transfer characteristics of the device for V_{ds} = 0.1, 0.3, 0.5 V respectively from bottom to top. A subthreshold swing of 60 mV/decade is shown. (d) Output characteristics of the device for V_{TG} varying from −1 V (bottom, black) to 1.4 V (top, purple) with a step of 0.2 V. For all measurements, the back-gate is kept at V_{BG} = 40 V to electrostatically n-dope the un-gated nanotube segments near the contact regions. The arrow indicates a maximum transconductance of 5 μS, or 4200 S/m after normalization with the diameter of the nanotube (d ~1.2 nm) [39].

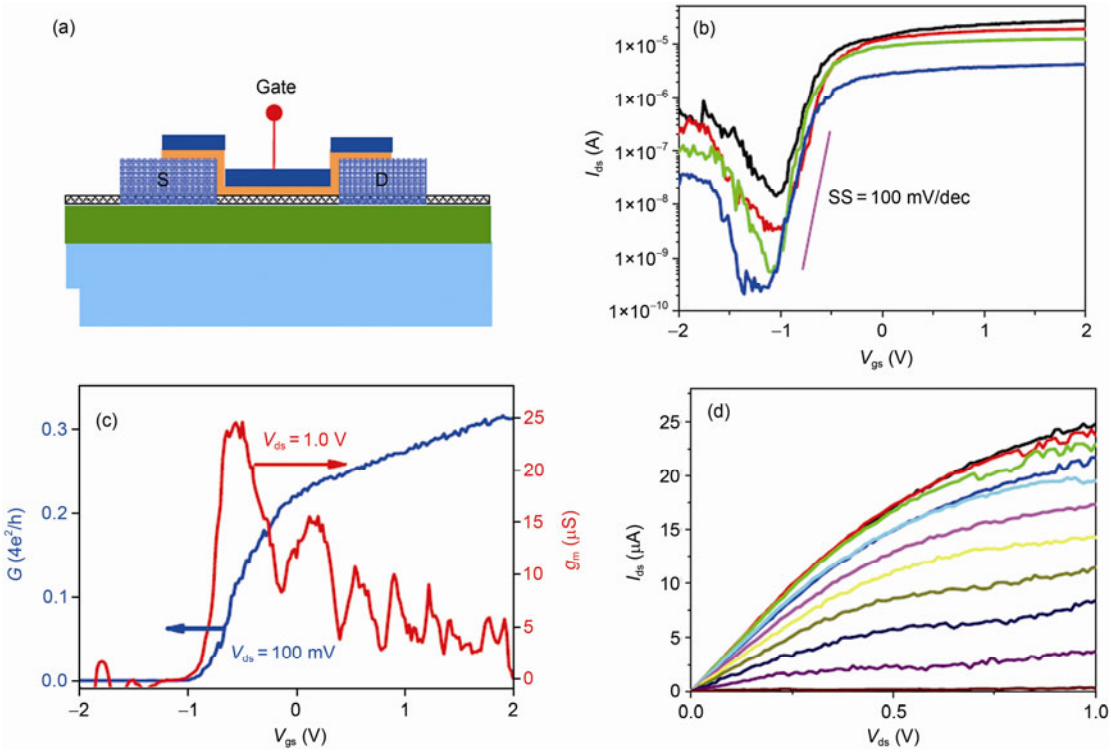

Figure 3 Self-aligned SWCNT FETs. (a) Side-view schematic diagram of the device. (b) Transfer characteristics of a self-aligned n-type SWCNT FET (with channel length L = 120 nm and SWCNT diameter d = 1.5 nm). (c) Gate-voltage-dependent conductance (G) (blue curve, left) and transconductance (g_m) at V_{ds} = 1.0 V. (d) Output characteristics of the device in which V_{gs} is varied from 1.0 V (top) to −1.0 V (bottom) with a step of −0.2 V [40].

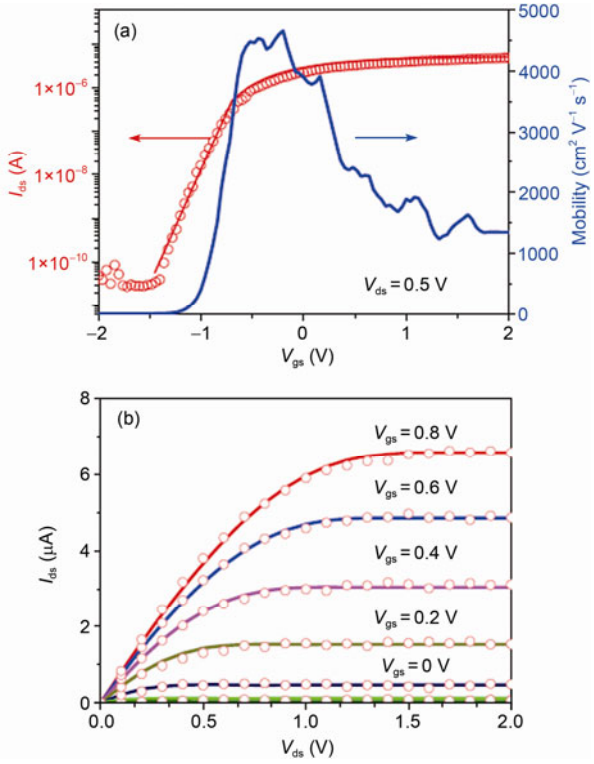

Figure 4 Electrical transport characteristics of a long-channel (L = 2 μm) CNT FET fabricated on the same SWCNT as the 120 nm device shown in Figure 2. (a) Transfer characteristic of the FET at V_{ds} = 0.5 V (red curve) and V_{gs}-dependent electron mobility (blue curve). (b) Output characteristics of the same device in which V_{gs} is varied from 0.8 to –0.4 V in steps of –0.2 V from top to bottom. Symbols are experimental data and solid lines are simulation data obtained using a diffusive FET model [40].

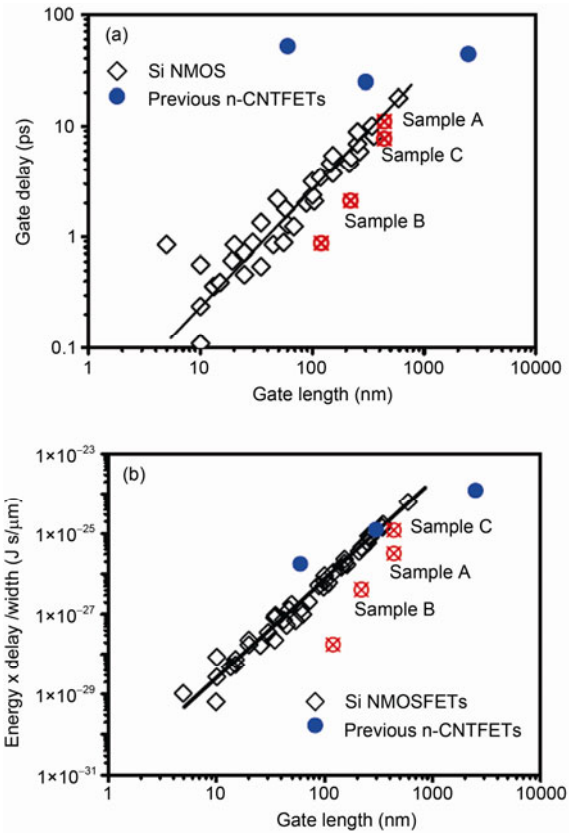

Figure 5 Gate delay (a) and energy-delay product per device width (b) vs. gate length for n-type SWNT FETs [41].

room-temperature I_{on}/I_{off} ratio exceeding 10^4. In addition, the intrinsic gate delay of sub-100 nm CNT devices fabricated using either type of self-aligned structure has been demonstrated to be less than 1 ps, suggesting potential applications of the CNT devices in the terahertz regime.

After optimizing the contacts and structure, the n-type CNT FETs were benchmarked according to the intrinsic gate delay and energy-delay product as shown in Figure 5. Comparison of the intrinsic gate delay and energy-delay product shows that the performance of the n-type CNT FETs substantially exceeds that of the length-dependent scaling of planar n-type Si MOS FETs and is comparable to that of p-type CNT FETs of similar length [41]. It is obvious that the improvement of speed and energy is primarily due to the tremendously enhanced mobility within CNTs.

The frequency response for the CNT device falls far below the intrinsic performance, and this is mainly due to the large parasitic capacitance between the source/drain and gate electrodes, which is typically three orders of magnitudes larger than the intrinsic gate capacitance of the CNT device. It should be noted that in all previously published self-aligned device structures, there exists a high-κ dielectric layer (Al_2O_3 or HfO_2) between the gate and source/drain, and this high-κ dielectric layer remarkably enlarges the parasitic capacitance (by a factor of ~κ). A self-aligned U-gate structure for a CNT FET has been introduced as shown in Figure 6, and shown to yield excellent DC properties and high reproducibility that are comparable to those of the best CNT FETs based on the previously developed self-aligned device structures [42]. In particular, the subthreshold swing of the U-gate FET is 75 mV/decade and the drain-induced barrier lowering is effectively zero, indicating that the electrostatic potential of the whole CNT channel is most efficiently controlled by the U-gate and that the CNT device is a well-behaved FET. The parasitic capacitance of the device has been measured and shown to be one order of magnitude smaller than that of the previously developed self-aligned device structures. The significantly reduced parasitic capacitance of the U-gate device originates mainly from replacing the high-κ dielectric material between the source/drain and gate electrodes in the other two self-aligned device structures with a vacant space with κ~1 [34,40,42].

2.3 Threshold adjustment and control

The threshold voltage V_{th} is one of the most important device parameters to consider when integrating FETs into a complex CMOS circuit. In principle, the threshold voltage of an FET may be adjusted by controlling the doping of its conduction channel, but this method is not suitable for implementing

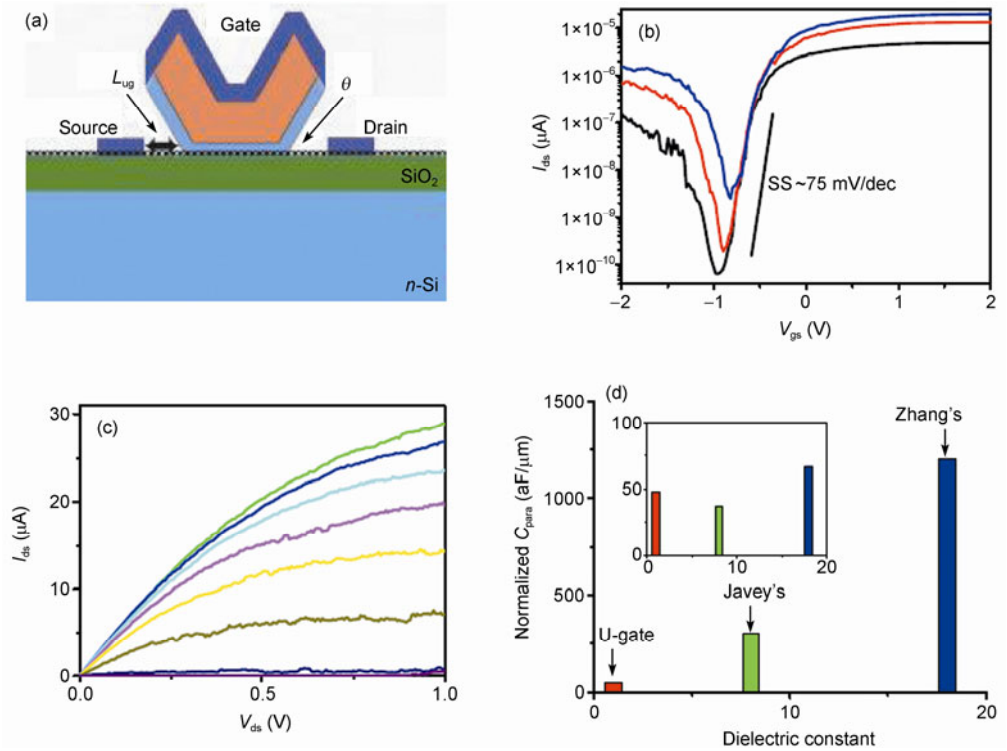

Figure 6 Geometry and characteristics of a self-aligned U-gate CNT FET. (a) A cross-sectional view the CNT FET. (b) Transfer characteristics for V_{ds} = 0.1 V (black), 0.3 V (red), and 0.5 V (blue) respectively from bottom to top. (c) Output characteristics of the device with V_{gs} being varied from 1.4 V (top, black) to –0.7 V (bottom, olive) with steps of –0.3 V. (d) Normalized (by space of 5 nm from the source/drain to the gate) structure capacitance vs. dielectric constant for three types self-aligned device structures per micron contact width. Inset: comparison of structure capacitance for three types of self-aligned structures further normalized by the dielectric constant [42].

CNT-based doping-free CMOS technology. Alternatively, a gate metal with a suitable work function may be selected to control the threshold of the device, and this is the method we used in the doping-free fabrication of CNT-based CMOS circuits.

The main advantage of the self-aligned gate structure is that it can be used for any gate material with a desired property. In particular, this structure allows us to adjust the threshold voltage of the FET by choosing a suitable gate metal with a desired work function to meet the requirement of the circuit design. Two self-aligned FETs with the same channel length were fabricated on the same SWCNT with a diameter of 2.0 nm. The only difference between the two devices is that one FET used Ti for the gate electrode and the other used Pd. The transfer characteristics of the two devices are given in Figure 7(a), showing clearly that the threshold voltage V_{th} of the device with a Pd gate shifted by about 0.51 V along the positive V_{gs} axis with respect to the

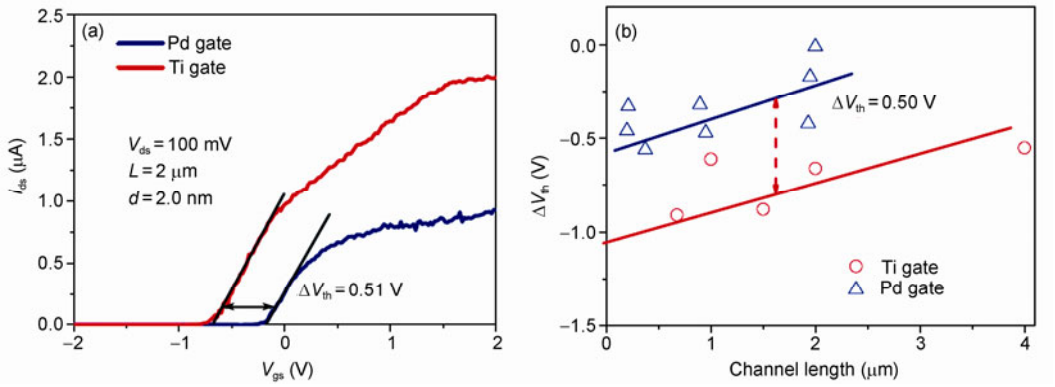

Figure 7 Adjustment of the threshold voltage of CNT FETs via selecting the gate metal. (a) Transfer characteristics for 2 FETs on the same SWCNT. The red (green) curve corresponds to the device with a Ti (Pd) gate. (b) Channel-length dependence of V_{th} for 13 FETs with different top gate electrodes [40].

threshold voltage of the device fabricated using the Ti gate. This shift is found to be dependent on the channel length as shown in Figure 7(b), in which results from 13 devices with different channel lengths but on the same CNT are shown. Among the 13 devices, five were fabricated using a Ti gate and eight using a Pd gate. V_{th} for each device is extracted employing the standard peak transconductance method under a bias of 0.1 V. The channel-length dependence of V_{th} might result from the fact that the electric property of the FETs varies from being channel dominated to being contact dominated as the channel length decreases from a diffusive regime toward a ballistic regime. The V_{th} values for these FETs with a Pd gate are obviously different from those for a Ti gate. For simplicity, two parallel lines are used to fit the data of the two types of FETs, and the V_{th} shift between these two lines is found to be 0.50 V [40].

2.4 Scaling behavior of n-type CNT FETs

The ultimate performance of the CNT FETs is reflected in the scaling behavior of the devices, especially the gate length scaling. CNT FETs were fabricated with gate length from 300 nm to 50 μm, and the transfer characteristics of only five devices among these devices are shown in Figure 8(a) for simplicity. For the FETs with gate length of 5 μm, the field-dependent mobility was calculated using the diffusive model and it is shown in Figure 8(b) [32]. The peak mobility of 5100 $cm^2\ V^{-1}\ s^{-1}$ is greater than all published

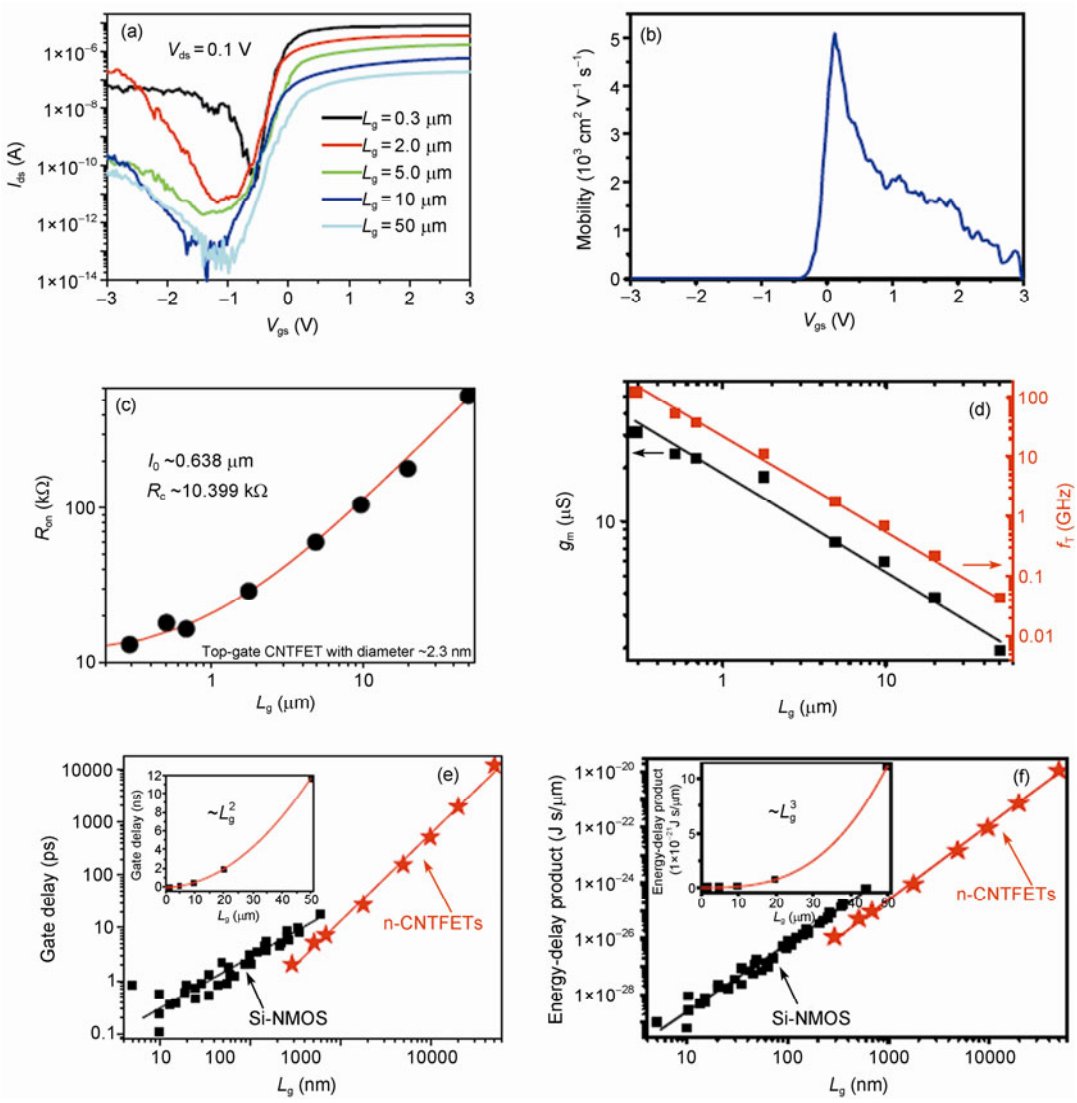

Figure 8 Scaling property of Y-contacted top-gate CNT-FETs. (a) Transfer characteristics of n-FETs fabricated on the same CNT (d = 2.3 nm) with different L_g. (b) Typical field-dependent mobility for the CNT FET with L_g = 5.0 μm. (c) ON-state resistance graph of different top-gate devices with different channel lengths. (d) Scaling property of transconductance (g_m) and cut-off frequency (f_T). (e) Scaling property of n-type CNT FET gate delay and comparison with that of n-type Si MOS gate delay; inset is the polynomial fitting of the gate delay property on linear scale. (f) Scaling property of the n-type CNT FET energy-delay product and comparison with that of the n-type Si MOS energy-delay product; inset is the polynomial fitting of the energy-delay product property on linear scale [32].

electron mobility values for n-type CNT FETs at room temperature. The scaling behavior of CNT FETs was explored by investigating five key device parameters, namely the ON-state resistance, transconductance, intrinsic cut-off frequency, intrinsic gate delay and energy-delay product, which are presented in Figure 8(c) and (d). For a long-channel device, for which the transport is in the diffusive regime, R_{on} is expected to increase linearly with the channel length L_g [43,44]. As the gate length is scaled down to a length much shorter than the electron mean free path L_m, electron transport in the channel becomes ballistic and the channel resistance becomes independent of the channel length. The electron mean free path is retrieved from the R_{on}-L_g curve and reaches 0.638 μm, which means the device with $L_g = 300$ nm is clearly ballistic. The cut-off frequency f_T increases rapidly with decreasing channel length and reaches 123 GHz for L_g~300 nm. It is expected that for a device with a channel shorter than 100 nm, f_T exceeds 1 THz.

The L_g-dependent intrinsic gate delay and energy-delay product for our CNT FETs are shown in Figure 8(e) and (f), together with those of Si-based n-type FETs. The figures show that while the energy-delay product for CNT devices decreases with channel length at a rate similar to that for Si-based devices, the gate delay of CNT devices decreases much more rapidly with decreasing channel length than that of the Si-based device (Figure 8(e)). Continuing with this trend, it is expected that a 30 nm CNT device has a gate delay of ~100 fs, which is among the shortest gate delays ever achieved by a Si-based device for a channel length of less than 10 nm. For long-channel devices, the gate delay scales with the channel length as ~L_g^2, and the energy-delay product as ~L_g^3. Therefore, the CNT FETs have better downscaling potential than Si MOS devices.

3 Doping-free CMOS devices technology

CMOS circuits are a major class of integrated circuits with tremendous advantages of high noise immunity and low static power consumption. CMOS is sometimes referred to as complementary symmetry metal-oxide-semiconductor (or COS-MOS) to emphasize that typical digital circuitry design uses complementary and symmetrical pairs of p-type (hole) and n-type (electron) MOS FETs for logic functions [45]. Unfortunately, perfectly symmetric CMOS has not been realized. This is because the band structures of all important semiconductors are intrinsically asymmetric around their band gaps or between the conduction and valence bands. Typically, electrons have a smaller effective mass than holes, and the performance of n-type FETs is much better than that of p-type FETs. As a result of the intrinsically asymmetric band structures of Si and all major semiconductors (including III–V and II–VI compounds), holes move much more slowly in MOS FET devices than electrons, dragging down the overall performance of the CMOS circuits.

Semiconductor CNTs have an almost perfectly symmetric band structure between the conduction and valence bands and consequently have essentially the same effective mass for electrons and holes. This band structure symmetry may in principle lead to the same electron and hole mobilities and similar performance for n- and p-type FETs, which are necessary for perfect CMOS performance. Unfortunately, perfectly symmetric CNT-based CMOS devices and integrated circuits have not been realized, and this is largely due to the lagging development of n-type devices [46–51].

3.1 Doping-free CNT-based CMOS technology

Unlike conventional Si-based CMOS, where the polarity of the FETs is determined by doping the conduction channel of the device with suitable dopant atoms, in CNT-based CMOS, the polarity of the FETs can be determined by controlling the injection of carriers to the channel [31,52]. While Pd may be used to inject a hole barrier freely into the valence band of the CNT to form high-performance p-type FETs, Sc may be used to inject an electron barrier freely into the conduction band of the CNT to form almost perfect n-type FETs. This is a doping-free process. Figure 9(a) shows that the CNT CMOS inverter with a back gate consists of an n-type CNT FET and a p-type CNT FET, and these CNT

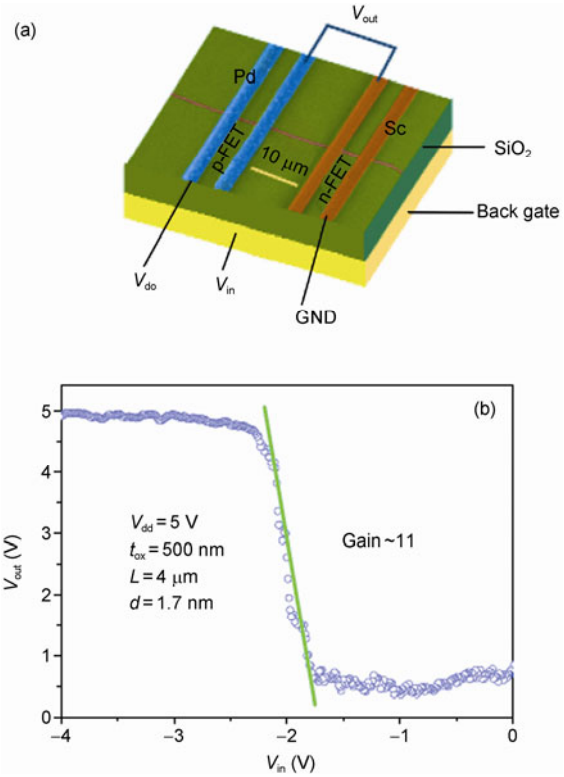

Figure 9 Back-gated ($t_{ox} = 500$ nm) SWCNT CMOS inverter. (a) Scanning electron microscope image of an SWCNT-based complementary inverter involving p- and n-type CNT FETs fabricated on the same SWCNT. (b) Transfer characteristic for a complementary SWCNT-based inverter with a CNT [31].

FETs are fabricated simply by contacting the CNT channel using Pd (p-type) and Sc (n-type) electrodes. The input voltage for the inverter is provided by the common back gate voltage $V_{in} = V_{gs}$ of the n- and p-type CNT FETs, while the output of the inverter is read from the common drain

3.2 Almost perfectly symmetric CNT CMOS devices and circuits

Although symmetric n-type and p-type CNT FETs were fabricated with back-gate structure in our earlier works, these back-gate devices cannot deliver near-perfect performance owing to the intrinsic limitation of the back-gate geometry. To further explore advantages of CNT CMOS devices and circuits, highly efficient self-aligned top-gate geometry should be employed.

Figure 10 shows the structure and electrical properties of a CNT-based CMOS inverter with self-aligned top gate [53]. This inverter comprises a pair of adjacent n- and p-type FETs fabricated on the same SWCNT with $d = 2$ nm and the same gate length of $L_g = 4.0$ μm. The field transfer (Figure 10(b)) and output characteristics (Figure 10(c)) are almost perfectly symmetric between the n- and p-type FETs. The mobility curves (Figure 10(d)) show peak mobility of about 3000 cm^2/V s for the electron and about 3300 cm^2 V^{-1} s^{-1} for the hole for the two adjacent n- and p-type FETs on the same SWCNT. The near-perfect symmetry of the mobility between electron and hole manifests experimentally the intrinsic symmetric band structure of the CNT. The voltage transfer characteristics of the CNT-based CMOS inverter

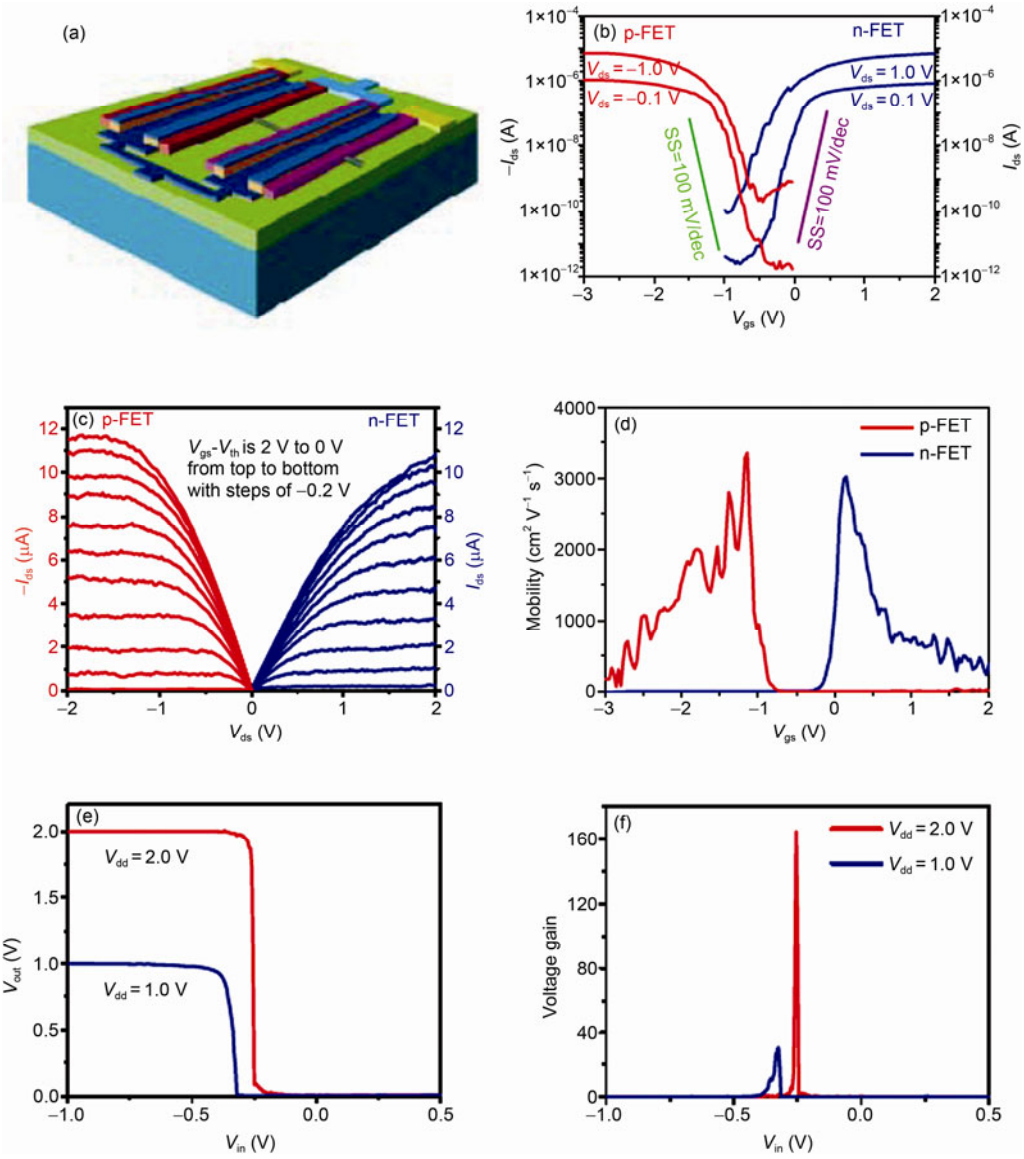

Figure 10 Characteristics of the CNT-based CMOS inverter. (a) Sketch of SWCNT CMOS devices with a pair of p- and n-type FETs. (b) Field transfer characteristic (I_{ds}-V_{gs}). (c) Output characteristic (I_{ds}-V_{ds}) and (d) field-dependent carrier mobility for both the n- and p-type FET devices. (e) Voltage transfer characteristics (V_{out}-V_{in}). (f) Field-dependent voltage gain [53].

show a perfect "1" (with $V_{out} = V_{dd}$) and "0" state (with $V_{in} = V_{GND}$) and the highest-to-date voltage gain of over 160.

CNT-based CMOS devices are not only more symmetric, faster and less power-consuming than Si-based CMOS devices but their fabrication is also simpler. We compare the main process steps of CNT-based and standard twin-well Si CMOS technology before interconnection [54] in Table 1, showing clearly that the CNT-based CMOS technology is much simpler than Si-based CMOS technology. This is largely due to the doping-free and isolating-free process we developed for the CNT-based CMOS process. This process also requires fewer steps in other main processes than the Si-based CMOS process, including fewer steps in lithography, etching and film growth.

4 High-frequency applications of CNT FETs

In principle, CNTs generally have an extraordinary radio frequency (RF) response up to the gigahertz regime owing to their ultra-high carrier mobility, suggesting terahertz working potential for future CNT-based electronic devices [55]. In practice, the cutoff frequency of CNT FETS is well below the performance limit owing to the large parasitic capacitance between electrodes [56]. Therefore, FETs fabricated on parallel CNTs array were used to reduce the parasitic capacitance per tube [56], and a cutoff frequency as high as 80 GHz was then measured [57]. However, it is difficult to produce a parallel array of semiconducting CNTs and the device is not easy to miniaturize. Exploring and increasing the frequency response of an FET based on a single CNT will meet two obstacles. One is the large parasitic capacitance between electrodes, and the other relates to the measurement. This key parameter cutoff frequency can be obtained through standard *S*-parameter measurement using a network analyzer. However, it should be noted that the standard *S*-parameter measurement cannot be applied to measure accurately the frequency response of a single CNT FET in which the output resistance is much larger than 50 Ω, the ideal value for an impedance-matched measurement.

4.1 High-frequency response of devices based on a single SWCNT

Since the real frequency response of a CNT FET is limited by parasitic capacitance instead of the intrinsic limit, there remains much room for reducing the parasitic capacitance and improving the RF performance of the CNT FET via optimizing the geometry of the device. To reduce the main parasitic capacitance between a gate and source/drain, the self-aligned U gate structure has been preferred [42]. The frequency response of the self-aligned U-gate CNT FETs has been assessed via a direct AC measurement, which is usually referred to as a large-signal frequency-domain measurement. Figure 11(a) and (b) shows the geometry of the final device for high-frequency measurement. The setup used to measure the frequency response of CNT FETs is shown in Figure 11(c), where a signal generator is used to apply a sine wave and a spectrum analyzer is used to measure the output crosstalk signal. The measurement results are shown in Figure 11(d), in which $P_{CT+CNTFET}$ is the total signal power and PCT is the crosstalk power with the CNT FET being off. At low frequency (less than 200 MHz), $P_{CT+CNTFET}$ far exceeds P_{CT}. However, as the input frequency increases, $P_{CT+CNTFET}$ and P_{CT} approach each other and almost coincide at about 800 MHz. Since the coincidence between $P_{CT+CNTFET}$ and P_{CT} suggests that the CNT FET no longer works, the cut-off frequency of the device is estimated to be about 800 MHz. It should be noted that this cut-off frequency measured for our SA U-gate device is much higher than any of previously reported value for an FET fabricated on a single CNT recorded by direct measurement. In principle, both the contact width and device channel can be reduced, and the large parasitic capacitance due to the silicon substrate used in this work can be eliminated by replacing the silicon substrate with a more insulating substrate. We expect that the cut-off frequency f_T will be significantly improved by further optimization of the device geometry.

4.2 High-performance frequency doubler based on large CNTs

In addition to typical semiconducting CNTs and typical metallic CNTs, there are CNTs with a small band gap (SBG) and small current on/off ratio of between 1 and 100 [58]. SBG CNTs are characterized by their small band gap, low current on/off ratio, and typically ambipolar field-effect characteristics. These CNTs are therefore not suitable for applications in logic circuits or as interconnects. However, RF applications do not require the device to be in its off state, offering SBG CNTs a promising field of application. The SBG CNTs can also be used to construct frequency doublers, but because they can operate in a strong-signal mode (i.e., unlike previous weak-signal RF transistors, which operate only in the weak-signal region), the SBG CNT-based FETs may operate over a much larger signal range.

Table 1 Comparison of main processing steps for SWCNT-based and standard twin-well Si CMOS technology with shallow trench isolation before interconnection [53,54]

	Lithography	Etching	Ion implantation	Film growth	Total
Si-CMOS	10	6	8	8	32
SWCNT CMOS (this work)	5	5	0	7	17

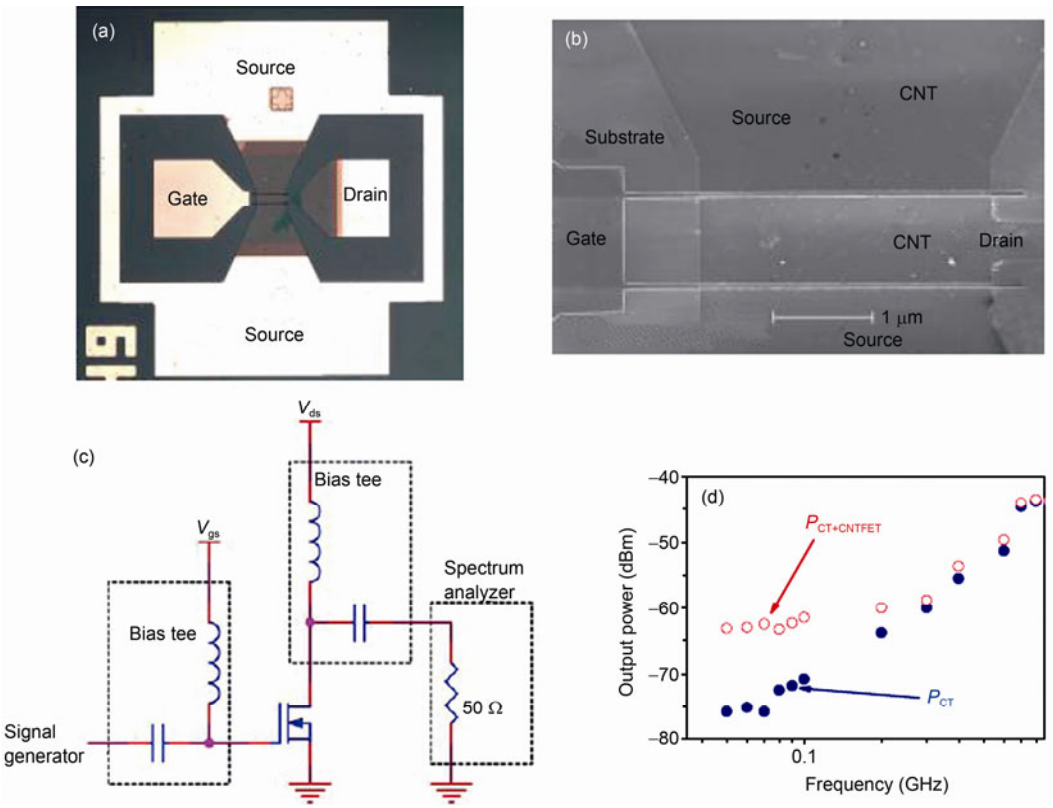

Figure 11 RF characteristics of the self-aligned U-gate CNT FETs. (a) Image of a real device with GSG pads. (b) SEM imshe of the device with a gate length of 0.6 μm and contact width of 30 μm. (c) Experimental setup used to measure the frequency response of the self-aligned U-gate CNT FET. (d) Measurements of the crosstalk power P_{CT} and the total power $P_{CT+CNTFET}$ for the self-aligned U-gate CNT FETs for $V_{gs}=0.5$ V and $V_{ds}=0.5$ V. The input power is −10 dBm [42].

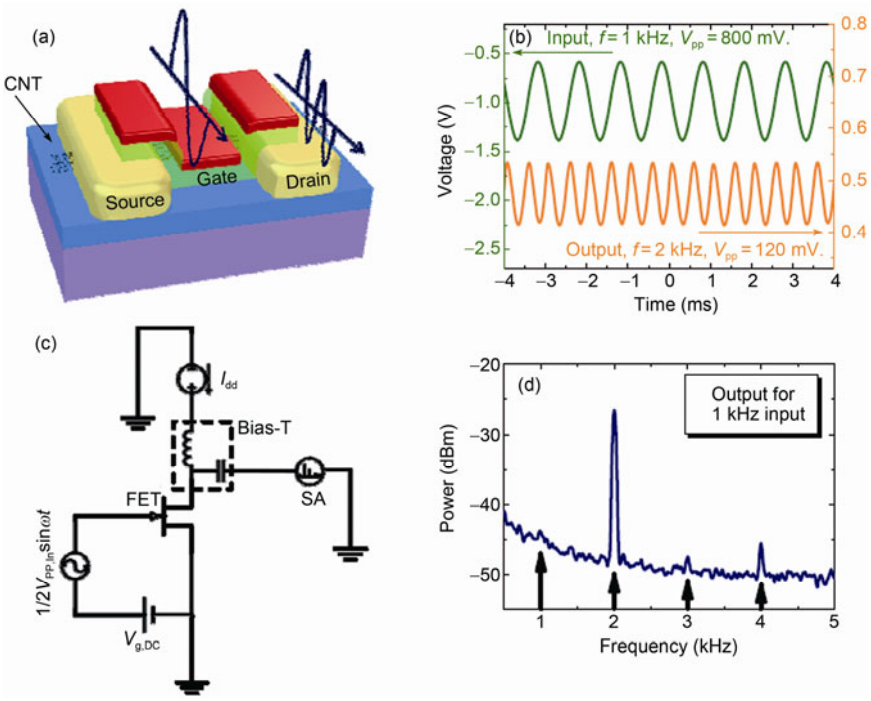

Figure 12 AC performance of a CNT-based frequency doubler. (a) Schematic diagram illustrating the geometry of a CNT-based ambipolar FET and its working principle for a frequency doubler. When a sinusoidal wave is applied to the top-gate electrode of the FET, with the source electrode being grounded, an output sinusoidal wave with doubled frequency is measured at the drain electrode. (b) Input and output waveforms for an input 1 kHz sinusoidal wave with input $V_{pp}=800$ mV and output $V_{pp}=120$ mV. (c) Schematic diagram depicting the measurement setup for frequency spectrum analysis. The input signal is applied to the gate of the CNT FET and the output AC signal is coupled through a bias-T to the spectrum analyzer (SA). (d) Measured output signal spectrum for 1 kHz input [59].

When applied to the gate electrode, the input signal may drive the FET from its p-region to n-region yielding a large output at the drain electrode with more than 95% of frequency power being concentrated at the doubled frequency of the input AC signal as shown in Figure 12 [59]. The SBG CNT-based FETs have not only perfectly symmetric ambipolar transfer characteristics but also extremely high carrier mobility (in principle higher than 100000 $cm^2\ V^{-1}\ s^{-1}$ in CNTs vs about 20000 $cm^2\ V^{-1}\ s^{-1}$ in graphene) on SiO_2 substrate owing to the suppressed substrate scattering. Therefore, the SBG CNT-based FETs could be potentially used to build a high- frequency doubler in the terahertz regime.

5 Conclusion

Ballistic n-type CNT-based FETs have been fabricated by contacting semiconducting SWCNTs using Sc or Y. The n-type CNT FETS were pushed to their performance limits through further optimizing their gate structure and insulator, and they outperformed Si NMOS FETs with the same gate length. In addition, the CNT FETS had better downscaling behavior than Si MOS FETs. Doping-free CNT CMOS technology was then developed. Taking full advantage of the perfectly symmetric band structure of the semiconductor SWCNT, a perfect SWCNT-based CMOS inverter was demonstrated, which had a voltage gain of over 160. For two adjacent n- and p-type FETs fabricated on the same SWCNT with a self-aligned top-gate, high field mobility was realized simultaneously for electrons (3000 $cm^2\ V^{-1}\ s^{-1}$) and holes (3300 $cm^2\ V^{-1}\ s^{-1}$). The CNT FETs also showed excellent potential for high-frequency applications, such as a high-performance frequency doubler.

This work was supported by the Ministry of Science and Technology of China (2011CB933001, 2011CB933002), the Fundamental Research Funds for Central Universities, and the National Natural Science Foundation of China (61071013, 61001016).

1 Iijima S. Helical microtubules of graphitic carbon. Nature, 1991, 354: 56–58
2 Saito R, Dresselhaus G, Dresselhaus M S. Physical Properties of Carbon Nanotubes. London: Imperial College Press, 1998
3 Jin Z, Chu H B, Wang J Y, et al. Ultralow feeding gas flow guiding growth of large-scale horizontally aligned single-walled carbon nanotube arrays. Nano Lett, 2007, 7: 2073–2079
4 Charlier J C, Blase X, Roche S. Electronic and transport properties of nanotubes. Rev Mod Phys, 2007, 79: 677–732
5 Close G F, Yasuda S, Paul B, et al. A 1 GHz integrated circuit with carbon nanotube interconnects and silicon transistors. Nano Lett, 2008, 8: 706–709
6 Avouris P, Chen Z H, Perebeinos V. Carbon-based electronics. Nat Nanotechnol, 2007, 2: 605–615
7 Biercuk M J, Ilani S, Marcus C M, et al. Electrical transport in single-wall carbon nanotubes. Carbon Nanotubes, 2008, 111: 455–493
8 Dai H, Javey A, Pop E, et al. Electrical transport properties and field-effect transistors of carbon nanotube. Nano, 2006, 1: 1–13
9 Rutherglen C, Jain D, Burke P. Nanotube electronics for radiofrequency applications. Nat Nanotechnol, 2009, 4: 811–819
10 Service R F. Is silicon's reign nearing its end? Science, 2009, 323: 1000–1002
11 Chau R, Doyle B, Datta S, et al. Integrated nanoelectronics for the future. Nat Mater, 2007, 6: 810–812
12 International Technology Roadmap for Semiconductors, 2009 ed. http://public.itrs.net/
13 Yan H, Choe H S, Nam S W, et al. Programmable nanowire circuits for nanoprocessors. Nature, 2011, 470: 240–244
14 Passlack M, Zurcher P, Rajagopalan K, et al. High mobility III-V MOSFETs for RF and digital applications. International Electron Devices Meeting, 2007: 621–624
15 Dürkop T, Getty S A, Cobas E, et al. Extraordinary mobility in semiconducting carbon nanotubes. Nano Lett, 2004, 4: 35–39
16 Chen Z, Farmer D, Sheng X, et al. Externally assembled gate-all-around carbon nanotube field-effect transistor. IEEE Electron Device Lett, 2008, 29: 183–185
17 Castro Neto A H, Guinea F, Peres N M R, et al. The electronic properties of graphene. Rev Mod Phys, 2009, 81: 109–162
18 Tans S, Verschueren A, Dekker C. Room-temperature transistor based on a single carbon nanotube. Nature, 1998, 393: 49–52
19 Heinze S, Tersoff J, Martel R, et al. Carbon nanotubes as schottky barrier transistors. Phys Rev Lett, 2002, 89: 106801
20 Martel R, Derycke V, Lavoie C, et al. Ambipolar electrical transport in semiconducting single-wall carbon nanotubes. Phys Rev Lett, 2001, 87: 256805
21 Wind S J, Appenzeller J, Avouris P. Lateral scaling in carbon-nanotube field-effect transistors. Phys Rev Lett, 2003, 91: 058301
22 Appenzeller J, Knoch J, Derycke V, et al. Field-modulated carrier transport in carbon nanotube transistors. Phys Rev Lett, 2002, 89: 126801
23 Yaish Y, Park J Y, Rosenblatt S, et al. Electrical nanoprobing of semiconducting carbon nanotubes using an atomic force microscope. Phys Rev Lett, 2004, 92: 046401
24 Javey A, Wang Q, Kim W, et al. Advancements in complementary carbon nanotube field-effect transistor. IEEE Electron Devices Meeting Technical Digest, 2003, 31.2: 1–4
25 Nosho Y, Ohno Y, Kishimoto S, et al. n-Type carbon nanotube field-effect transistors fabricated by using Ca contact electrodes. Appl Phys Lett, 2005, 86: 073105
26 Sze S M. Physics of Semiconductor Devices. New York: Wiley, 1981
27 Léonard F, Tersoff J. Role of fermi-level pinning in nanotube schottky diodes. Phys Rev Lett, 2000, 84: 4693–4696
28 Chen Z, Appenzeller J, Knoch J, et al. The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. Nano Lett, 2005, 5: 1497–1502
29 Javey A, Guo J, Wang Q, et al. Ballistic carbon nanotube field-effect transistor. Nature, 2003, 424: 654–657
30 Kim W, Javey A, Tu R, et al. Electrical contacts to carbon nanotubes down to 1 nm in diameter. Appl Phys Lett, 2005, 87: 173101
31 Zhang Z Y, Liang X L, Wang S, et al. Doping-free fabrication of carbon nanotube based ballistic CMOS devices and circuits. Nano Lett, 2007, 7: 3603–3607
32 Ding L, Wang S, Zhang Z Y, et al. Y-contacted high-performance n-type single-walled carbon nanotube field-effect transistors: Scaling and comparison with sc-contacted devices. Nano Lett, 2009, 9: 4209–4214
33 Javey A, Guo J, Farmer D B, et al. Carbon nanotube field-effect transistors with integrated ohmic contacts and high-κ gate dielectrics. Nano Lett, 2004, 4: 447–450
34 Javey A, Guo J, Farmer D B, et al. Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays. Nano Lett, 2004, 4: 1319–1322
35 Javey A, Tu R, Farmer D B, et al. High performance n-type carbon nanotube field-effect transistors with chemically doped contacts. Nano Lett, 2005, 5: 345–348
36 Chau R, Datta S, Doczy M, et al. Benchmarking nanotechnology for high-performance and low power logic transistor applications. IEEE Trans Nanotechnol, 2005, 4: 153–158

37 Javey A, Kim H, Brink M, et al. High-κ dielectrics for advanced carbon-manotube transistors and logic gates. Nat Mater, 2002, 1: 241–246
38 Lu Y, Bangsaruntip S, Wang X, et al. DNA functionalization of carbon nanotubes for ultrathin atomic layer deposition of high k dielectrics for nanotube transistors with 60 mV/decade. J Am Chem Soc, 2006, 128: 3518–3519
39 Wang Z X, Xu H L, Zhang Z Y, et al. Yttrium oxide as a perfect high-κ gate dielectric for carbon-based electronics. Nano Lett, 2010, 10: 2024–2030
40 Zhang Z Y, Wang S, Ding L, et al. Self-aligned ballistic n-type single-walled carbon nanotube field-effect transibbstors with adjustable threshold voltage. Nano Lett, 2008, 8: 3696–3701
41 Zhang Z Y, Wang S, Ding L, et al. High-performance n-type carbon nanotube field-effect transistors with estimated sub-10-ps gate delay. Appl Phys Lett, 2008, 92: 133117
42 Ding L, Wang Z X, Pei T, et al. A self-aligned u-gate carbon nanotube field-effect transistor with extremely small parasitic capacitance and drain induced barrier lowering. ACS Nano, 2011, 5: 2512–2519
43 Zhou X J, Park J Y, Huang S M, et al. Band structure, phonon scattering, and the performance limit of single-walled carbon nanobue transistors. Phys Rev Lett, 2005, 95: 146805
44 Purewal M S, Hong B H, Ravi A, et al. Scaling of resistance and electron mean free path of single-walled carbon nanotubes. Phys Rev Lett, 2007, 4: 186808
45 Baker R J. CMOS: Circuit Design, Layout, and Simulationrevised. 2nd ed. New York: Wiley-IEEE Press, 2008
46 Javey A, Wang Q, Ural A, et al. Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators. Nano Lett, 2002, 2: 929–932
47 Liu X L, Lee C H, Zhou C W. Carbon nanotube field-effect inverters. Appl Phys Lett, 2001, 79: 3329–3331
48 Derycke V, Martel R, Appenzeller J, et al. Carbon nanotube inter- and intramolecular logic gates. Nano Lett, 2001, 1: 453–456
49 Chen Z H, Appenzeller Z H, Lin Y M, et al. An integrated logic circuit assembled on a single carbon nanotube. Science, 2006, 311: 1735
50 Cao Q, Kim H, Pimparkar N, et al. Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. Nature, 2008, 454: 495–500
51 Ryu K M, Badmaev A, Wang C, et al. CMOS-analogous wafer-scale nanotube-on-insulator approach for submicrometer devices and integrated circuits using aligned nanotubes. Nano Lett, 2009, 9: 189–197
52 Wang S, Zhang Z Y, Ding L, et al. A doping-free carbon nanotube CMOS inverter-based bipolar diode and ambipolar transistor. Adv Mater, 2008, 20: 3258–3262
53 Zhang Z Y, Wang S, Wang Z X, et al. Almost perfectly symmetric swcnt-based CMOS devices and scaling. ACS Nano, 2009, 3: 3781–3787
54 Plummer J D, Deal M D, Griffin P B. Silicon VLSI Technology: Fundamentals, Practice and Modeling. New Jersey: Prentice Hall, 2000. 51–82
55 Burke P. AC performance of nanoelectronics: Towards a ballistic THz nanotube transistor. Solid-State Electron, 2004, 48: 1981–1986
56 Guo J, Hasan S, Javey A, et al. Assessment of high-frequency performance potential of carbon nanotube transistors. IEEE Trans Nanotechnol, 2005, 4: 715–721
57 Nougaret L, Happy H, Dambrine G, et al. 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes. Appl Phys Lett, 2009, 94: 243505
58 Zhou C W, Kong J, Dai H J. Intrinsic electrical properties of individual single-walled carbon nanotubes with small band gaps. Phys Rev Lett, 2000, 84: 5604–5607
59 Wang Z X, Ding L, Pei T, et al. Large signal operation of small band-gap carbon nanotube based ambipolar transistor: A high-performance frequency doubler. Nano Lett, 2010, 10: 3648–3655