CMOS current mirrors with reduced input and output voltage requirements

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A CMOS current mirror with lower than $V_{DS(sat)}$ input voltage requirement is presented. It is shown that the structure can be modified to provide cascode-type output resistance for output voltages even lower than $2V_{DS(sat)}$. The topology of the proposed current mirror allows low distortion operation from a single 1.5V supply, which makes it attractive for low-voltage applications.

Introduction: The current mirror is one of the most important building blocks of analogue integrated circuits. Modern VLSI systems now operating from single 3.3V supplies and dropping, require high performance current mirrors that can operate with low voltages. The fact that the $V_{GS} - V_t$ of an MOS transistor determines most of its important parameters (e.g. g_m, ω_T) has been used in some topologies to eliminate the V_t dependence of the required minimal output voltage and hence increase the allowable signal swing [1 – 3]. These topologies are commonly referred to as 'high-swing cascodes'. However, the input voltage of most current mirrors reported in the literature does depend on the threshold voltage V_t. This voltage drop (visually in the order of a volt) across the input terminal of those current mirrors may not be tolerable in all low-voltage applications. The use of current mirrors with low input voltage is especially important for inplementation of VLSI test circuits which employ current sensing techniques [4]. Recently a few different current-mirror topologies with reduced input voltage requirements have been reported [4 – 6]. The topology capable of providing both low distortion and high bandwidth while having no hard dynamic range limitation is shown in Fig. 1 [4]. The level-shifter V_b in Fig. 1*a* can be implemented as shown in Fig. 1*b*. In this case, its value is equal to the difference of M_{b2}, M_{b1} gate potentials and can be set by properly selecting the M_{b1} and M_{b2} aspect ratios and the values of current sources I_{b1} and I_{b2}. In general, it is assumed that for linear operation, both transistors forming the current mirror (M_{M1}, M_{M2}) must be kept in saturation. Hence, the required V_b must be smaller than the threshold voltage V_{tn}.

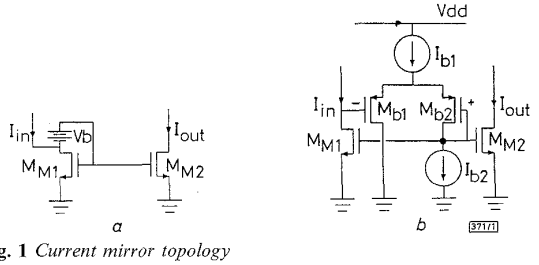

Fig. 1 *Current mirror topology*

a Conceptual schematic diagram of current mirror with reduced input voltage
b Implementation of Fig. 1*a* current mirror [5]

In this Letter we show that even if M_{M1} is biased in the triode region the Fig. 1*a* configuration will perform linear current mirroring. As a result, two new current-mirror circuits with reduced input, output and supply voltage requirements are derived.

Low input-voltage current mirrors using triode-region transistors: For the Fig. 1*a* circuit, assume that V_b is given by

$$V_b = V_{tn} + \Delta V \tag{1}$$

where $\Delta V \geq 0$. Under this condition transistor M_{M1} is biased in triode and its drain current I_{D1} in first approximation is given by

$$I_{D1} = \beta_{M1}(V_{GS} - V_{tn})V_{DS} = \frac{\beta_{M1}}{2}V_{DS}^2 \tag{2}$$

Using eqns. 1 and 2 and the Fig. 1*a* schematic diagram the input current I_{in} can be expressed as

$$I_{in} = I_{D1} = \frac{\beta_{M1}}{2}(V_{GS} - V_{tn})^2 - \frac{\beta_{M1}}{2}\Delta V^2 \tag{3}$$

The last equation shows that a triode-region transistor conducting drain current I_{in} and having a voltage source with the value $V_{tn} + \Delta V$ connected between its gate and drain terminals, has the same gate potential as that of a transistor in saturation conducting current $I_{in} + \beta_{M1}/2\,\Delta V^2$. Since M_{M2} is still assumed to be in saturation the output current of the Fig. 1*a* current mirror must be given by

$$I_{out} = I_{in} + \frac{\beta_M}{2}\Delta V^2 \tag{4}$$

where $\beta_M = \beta_{M1} = \beta_{M2}$.

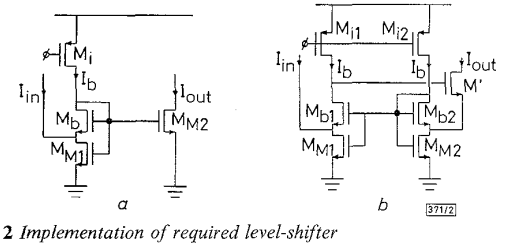

Fig. 2 *Implementation of required level-shifter*

a Simple current mirror using triode-region transistor
b Triode-region current mirror with cascode-type output resistance

There are numerous possibilities for the level-shifter realisation. The level-shifter employed in the Fig. 1*b* circuit may be used providing the difference between the gate potentials of M_{b2} and M_{b1} satisfies eqn. 1, but the minimal supply voltage required in this case must be higher than $V_{tn} + V_{tp}$. Another simpler and more robust implementation of the required level-shifter is used in the Fig. 2*a* current mirror. It consists of a single diode-connected *n*-channel transistor M_b conducting some constant bias current I_b. The V_b of this circuit is thus given by

$$V_b = V_{GSb} = V_{tn} + \sqrt{\frac{2}{\beta_b}I_b} \tag{5}$$

The output current of this structure can be found to be

$$I_{out} = I_{in} + \left(1 + \frac{\beta_M}{\beta_b}\right) I_b \tag{6}$$

It must be noted that the Fig. 2*a* mirror requires lower supply voltages than the Fig. 1*b* mirror. For threshold voltages $V_{tn} \simeq V_t^* \simeq 0.9$V the required V_{dd} is in the order of 1.3 – 1.5V. The main disadvantage of the proposed mirror is that its output current has an offset term.

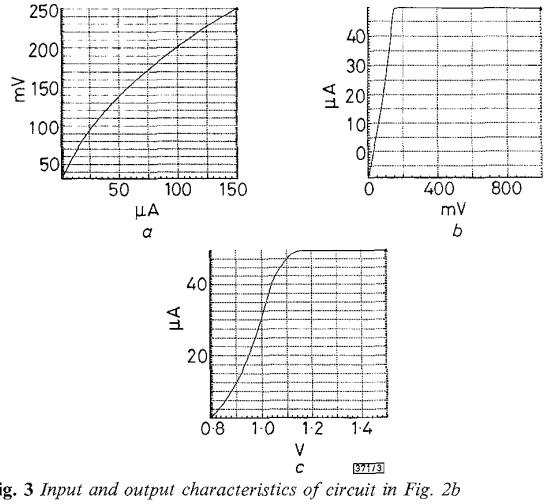

Fig. 3 *Input and output characteristics of circuit in Fig. 2b*

a Input driving-point charactersitic (V_{in} against I_{in}) of Fig. 2*b* circuit
b Output characteristic (I_{out} against V_{out}) for $I_{in} = 50\mu$A
c I_{out} against V_{dd} for $I_{in} = 50\mu$A

A structure which possesses a cascode-type output resistance, has better symmetry and cancels the current offset term is shown in Fig. 2*b*. Here negative feedback is formed by M_{M2}–M_{b2}, M_{M1}–M_{b1} and M_{l1} and the output resistance is approximately given by

$$r_{out} \simeq \frac{\beta_b}{\beta_b + \beta_M} g'_m r'_o (r_{ob} \| r_{oi}) \tag{7}$$

Simulation results: Both circuits shown in Fig. 2 were simulated using a BSIM level-13 model provided for MOSIS 2 micron orbit-analog process. The total harmonic distortion of the Fig. 2*a* and *b* mirrors was better than 0.3 and 0.1%, for input current with amplitude 75μA and frequency 1kHz and I_b = 10μA, respectively. This distortion can be accounted for if a more precise model for transistors in the triode region is to be used. The simulated input and output characteristics and I_{out} against V_{dd} for I_{in} = 50μA of the Fig. 2*b* circuit are shown in Fig. 3. Fig. 4 shows its simulated transfer characteristic and magnitude frequency response. The transistor sizes used were: $M_{M1,2}$ and $M_{b1,2}$ – 100/2, $M_{i1,2}$ – 200/4 and M – 200/2. In all simulations a single 1.5V supply was used. The simulated output resistance of the Fig. 2*b* was 11MΩ for output voltages as low as 250mV.

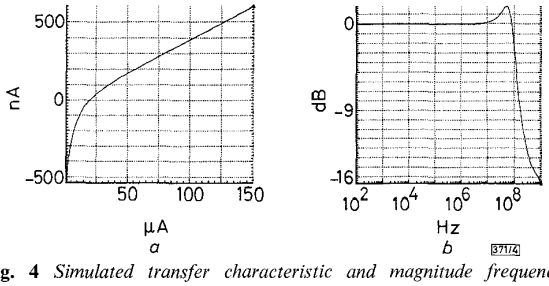

Fig. 4 *Simulated transfer characteristic and magnitude frequency response*

a Mismatch $I_{in} - I_{out}$ against I_{in}
b Magnitude frequency response I_{out}/I_{in} (in dB) of Fig. 2*b* current mirror

Conclusion: MOS current mirrors with reduced input and output voltage requirements are derived. They used suitably biased triode-region transistors and have no hard limit on their dynamic range.

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Precision temperature stabilised tunable CMOS current-mirror for filter applications

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Indexing terms: Current mirrors, Analogue circuits, Circuit theory

A temperature stable external reference resistor is used to accurately control and tune the transconductance of an integrated current-mirror. The technique can be used to tune and optimise the bandwidth of the current-mirror for application in CMOS filters.

Introduction: Current-mode continuous-time filters which exploit a generic CMOS current-mirror are very promising for high frequency applications, and have lately been investigated considerably [1]. In this Letter we present a temperature stable resistive tuning compensation scheme to accurately adjusting the bandwidth of the current-mirror and hence the filter operating frequency.

Basic current mirror: As discussed in [2], the bandwidth of the simple CM can be increased with resistive compensation as shown in Fig. 1*a*. All the CMs in this Letter are assumed to be appropriately biased, so biasing circuits are not shown. For $R_{tu} = 1/g_{m1}$, the resultant bandwidth is doubled (assuming M_1 and M_2 are the same size). This technique is also applicable to first generation switched-current cells and other more complicated CMs such as cascode, regulated cascode and the Wilson CM.

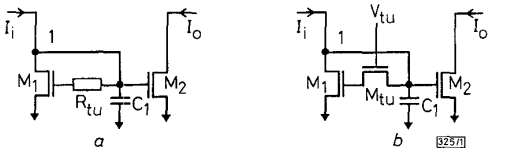

Fig. 1 *Tunable simple current mirror*

For full monolithic integration, R_{tu} can be a passive resistor made of polysilicon, or a diffusion resistor. There are three disadvantages of using such passive resistors in this application. First, the absolute values of the integrated passive resistors have a rather large tolerance. Even with a mature process, the passive and active components can have more than 10% variations. Secondly, the temperature dependence of passive resistors does not track transconductance of the MOS transistors. Third, for optimum compensation, it is required that $R_{tu} = 1/g_{m1}$. Hence, R_{tu} is required to track g_{m1} which varies considerably with process and temperature drifts. For more robust design, R_{tu} can be replaced by a small transistor M_{tu} with its gate voltage V_{tu} tuneable. This will incur little extra power consumption and minimal increase in chip area.

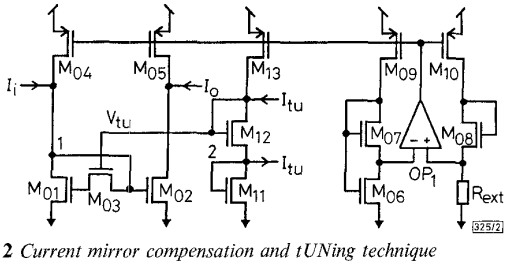

Fig. 2 *Current mirror compensation and tUNing technique*

Active R_{tu} tuning: First, we analyse the resistive compensation. Referring to Fig. 2, M_{11}, M_{12}, and M_{13} produce V_{tu} which controls the gate voltage of M_{03}. The channel resistance of M_{03} needs to match and to track $1/g_{m1}$ for optimum bandwidth [2]. With $(W/L)_4 = (W/L)_{13}$, M_{01} and M_{11} are biased with the same current, I_1. Further, if $(W/L)_1 = (W/L)_{11}$, the voltage at node 1 will be the same as at node 2. With the gate of M_{03} and M_{12} at equal potential $V_{gs3} = V_{gs12}$. To keep the voltage at node 1 and node 2 the same, the tuning current, I_{tu}, which feeds into the drain of M_{12} must be drawn out from its source to maintain $I_1 = I_{11}$ (this can be implemented with a simple sink/source CM). With these conditions, and assuming M_{03} is operating in its linear region, and M_{01}, M_{11}, and M_{12} are biased in saturation, the following equations are derived

$$g_{m1} = \sqrt{2\mu C_{ox}(W/L)_1 I_1} \tag{1}$$

$$r_{ds3} = \frac{1}{\mu C_{ox}(W/L)_3(V_{gs3} - V_t)} \tag{2}$$

$$I_1 + I_{tu} = 0.5\beta_{12}(V_{gs12} - V_{th})^2 \tag{3}$$

where all the symbols have their usual meanings [3]. Eqns. 1 – 3 are combined in eqn. 4 to give a better insight to the tuning and control mechanism.

$$I_{tu} = \left[\frac{\left(\frac{W}{L}\right)_1\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_3^2} - 1\right] I_1 \tag{4}$$

Note that for $I_{tu} = 0$, an optimum transistor size relationship exists which is only dependent on the transistor aspect ratios and it is well controlled,