Review

Chinese Science Bulletin

SPECIAL ISSUE: Graphene

August 2012 Vol. 57 No. 23: 2956–2970
doi: 10.1007/s11434-012-5143-x

Graphene-based ambipolar electronics for radio frequency applications

WANG ZhenXing, ZHANG ZhiYong* & PENG LianMao*

Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing 100871, China

Received December 14, 2011; accepted February 1, 2012; published online April 29, 2012

Graphene is considered as a promising material to construct field-effect transistors (FETs) for high frequency electronic applications due to its unique structure and properties, mainly including extremely high carrier mobility and saturation velocity, the ultimate thinnest body and stability. Through continuously scaling down the gate length and optimizing the structure, the cut-off frequency of graphene FET (GFET) was rapidly increased and up to about 300 GHz, and further improvements are also expected. Because of the lack of an intrinsic band gap, the GFETs present typical ambipolar transfer characteristic without off state, which means GFETs are suitable for analog electronics rather than digital applications. Taking advantage of the ambipolar characteristic, GFET is demonstrated as an excellent building block for ambipolar electronic circuits, and has been used in applications such as high-performance frequency doublers, radio frequency mixers, digital modulators, and phase detectors.

graphene, radio frequency, field-effect transistor, ambipolar electronics, high-κ dielectrics

Citation: Wang Z X, Zhang Z Y, Peng L M. Graphene-based ambipolar electronics for radio frequency applications. Chin Sci Bull, 2012, 57: 2956–2970, doi: 10.1007/s11434-012-5143-x

The 2-dimentional (2D) single layer carbon sheet graphene, in which the carbon atoms are arranged in a hexagonal form, has been an ideal model in theoretical research since early 20th century [1], although in 1930s Peierls and Landau denied that crystals in strict 2D formation could stably exist in actual experiment due to the thermodynamical reasons [2,3]. Owing to the success isolation of single layer graphene by Novoselov et al. [4] in 2004, the obsolete point was broken down and a tremendous research field has been expanded based on the 2D material [5–11], and even the 2010 Nobel Prize in Physics was awarded jointly to A. K. Geim and K. S. Novoselov "for groundbreaking experiments regarding the two-dimensional material graphene" [12,13]. The special 2D structure of graphene provides a series of unique properties in mechanics, thermology, optics, and electronics [10,11,14–19]. Graphene not only provides an experimental platform for basic physics, such as relativistic quantum mechanics (or quantum electrodynamics), which is due to the massless property of the Dirac fermion behaved electrons in graphene [20–22], but also manifests promising application potential in numerous application fields, such as analog radio frequency (RF) field-effect transistors (FETs) [10,23–25], flexible transparent electrodes and touch screen [26], photodetection [11,27,28], and spin transport [29,30]. In this review article, we will focus on the graphene based electronics and applications, especially RF performance of graphene and ambipolar electronics.

1 Basic properties of graphene

1.1 The band structure of graphene

Graphene is a 2D carbon-based material, in which the carbon atoms are organized in a hexagonal structure, as shown in Figure 1(a), and this hexagonal structure can be considered as the "mother" of many other carbon based materials, such as 0D fullerene, 1D carbon nanotubes (CNTs), and 3D bulk graphite. The unit cell of graphene, consisted of two atoms

*Corresponding authors (email: zyzhang@pku.edu.cn; lmpeng@pku.edu.cn)

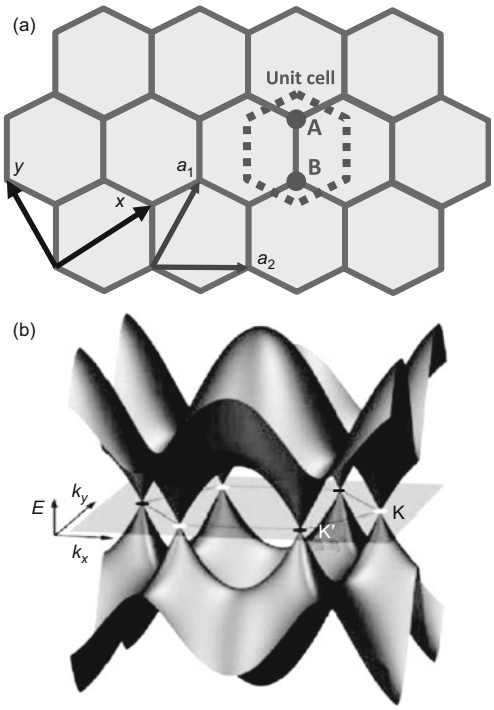

Figure 1 The lattice structure (a) and band structure (b) of graphene. Reprinted of (b) with permission from Ref. [31]. Copyright (2010) American Chemical Society.

(labeled as A and B), forms the entire 2D structure based on a triangular lattice. The lattice base vector can be written as

$$\boldsymbol{a}_1 = \frac{a}{2}\left(3,\ \sqrt{3}\right), \quad \boldsymbol{a}_2 = \frac{a}{2}\left(3,-\sqrt{3}\right), \tag{1}$$

where $a \simeq 1.42$ Å is the distance between the nearest carbon atoms, i.e. atoms A and B.

Based on the tight-binding approximation considering the nearest neighbor hopping, the band structure can be derived as [1]

$$E_{\pm}(\boldsymbol{k}) = \pm t\sqrt{3 + 2\cos\left(\sqrt{3}k_y a\right) + 4\cos\left(\frac{3}{2}k_x a\right)\cos\left(\frac{\sqrt{3}}{2}k_y a\right)}, \tag{2}$$

where $\boldsymbol{k} \equiv (k_x, k_y)$, and $t \simeq 2.8$ eV is the hopping energy between the nearest carbon atoms. The band structure can be plotted in 3D shown in Figure 1(b), where the positive and negative signs in eq. (2) correspond to the conduction and valence band respectively. Clearly there exist six pairs of cones in the band diagram, where the conduction and valence band contact with each other at the peak of the cones, and the peaks can be classified into two different types, denoted as **K** and **K**', points in the diagram. Their positions in the momentum space are

$$\mathbf{K} = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), \quad \mathbf{K'} = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right). \tag{3}$$

If we zoom in the band diagram to the **K** or **K'** point, we can expand eq. (2) near **K** or **K'** point as [1]

$$E_{\pm}(\boldsymbol{q}) \simeq \pm v_{\mathrm{F}}|\boldsymbol{q}| + O\left[\left(\frac{q}{K}\right)^2\right], \tag{4}$$

where $\boldsymbol{q} \equiv \boldsymbol{k} - \mathbf{K}$, and $v_F \simeq 1 \times 10^6$ m/s is the Fermi velocity near K point. From eq. (4), we can tell the linear dependence of E-k relation, similar as that of photon, thus the massless property of the electrons in graphene can be similarly determined. Meanwhile, the electron in graphene will consequently behave like a Dirac particle, which will obey the relative quantum mechanics, and hence they are classified as massless Dirac fermion, an entire new kind of particle. Correspondingly, **K** or **K'** point is also known as Dirac point.

1.2 Methods to obtain graphene

There are many methods to obtain single layer graphene at laboratory, such as mechanical exfoliation via Scotch tape [4], epitaxial growth by thermal desorption of Si atoms from the SiC surface [32], epitaxial growth by chemical vapor deposition (CVD) on transition metals [33,34], chemical reduction of liquid suspension graphene oxide [35], liquid-phase exfoliation [36], chemical exfoliation [37], unzipping CNTs [38], etc. Among all these methods, mechanical exfoliation and CVD growth on SiC or metals are most frequently utilized in experiments. Graphene obtained via mechanical exfoliation is of high electronic quality, with low cost, and easily obtained for a starter, which is the main reason for them being used in high-performance device demonstration and basic physics experiment [20,23]. However, the throughput is very low and it is totally not compatible with traditional chip process flow. While for graphene grown via CVD method, they are of large area, and compatible with the chip process flow. Although the electric transport property of the epitaxial graphene is not as good as the mechanical exfoliation one, and the growth cost is high, it is still worth exploring for future practical graphene-based application which needs large scale fabrication.

Another important reason for graphene rush is the visibility of graphene under optical microscope. Graphene thin flakes are sufficiently transparent, showing a transmittance more than 90% to visible lights [11], and they can add an optical path, which will change their interference color under optical microscope with respect to an empty wafer [39]. The contrast of graphene on substrate is mainly determined by three parameters: the refractive index, the thickness of the substrate, and the wavelength of the light used in the microscope. The contrast can be maximized either by selecting a suitable substrate or filtering the incident light in microscope to select a certain wavelength [39,40]. A well-trained researcher can tell the single-layer graphene from bi- or multilayer graphene just depending on the optical microscope, as shown in Figure 2(a). After the naked eye identification, the single-layer sample will be double checked by a Raman spectroscope or atomic force microscope (AFM) measurement.

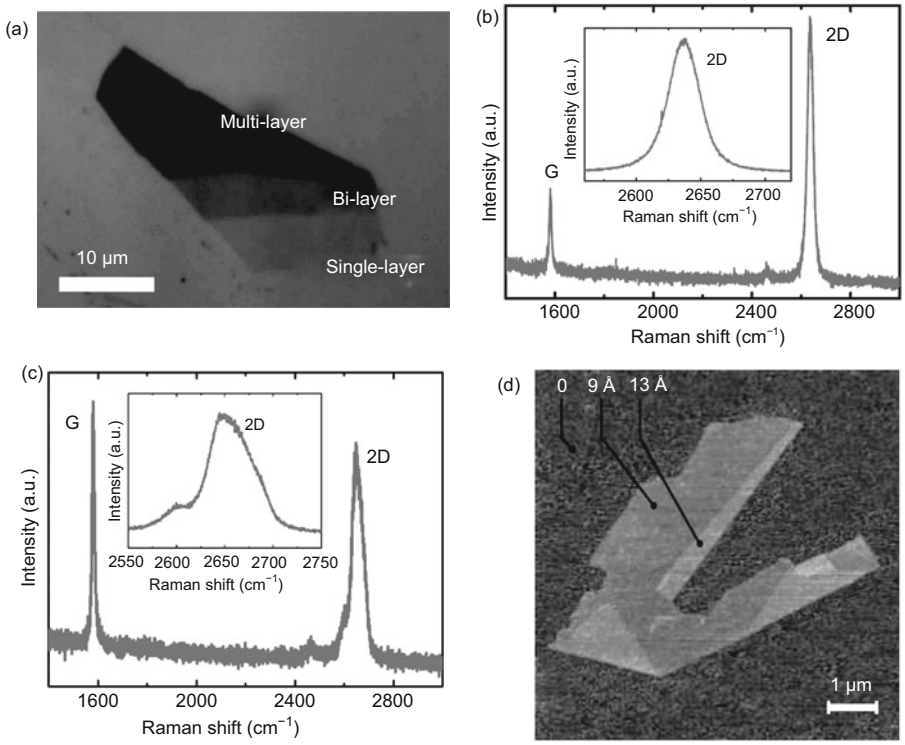

Figure 2 The characterization of single-layer graphene. (a) Graphene with different numbers of layers show different contrasts under optical microscope. (b) The typical Raman spectrum of a single-layer graphene, with symmetric 2D band stronger than G band. (c) The typical Raman spectrum of a bi-layer graphene, with asymmetric 2D band weaker than G band. (d) The AFM image of single-layer graphene on SiO_2, with a typical thickness of less than 10 Å. Reprinted of (d) with permission from Ref. [5]. Copyright (2007) Macmillan Publishers Ltd.

Typical Raman spectrums of a single- and bi-layer graphene are shown in Figure 2(b) and (c) respectively, where the intensity ratio of G/2D band and the symmetric property of 2D band are what we concern [41,42]. Furthermore, the thickness of graphene layer can be easily measured by AFM, and the typical thickness of single-layer graphene on SiO_2 is less than 1 nm. An AFM image demonstrating the thickness of different layer numbers of graphene is shown in Figure 2(d). However, the AFM measurement is not very accurate, depending on the substrate used [43], and the line scanning work mode determine the low throughput of AFM. To sum up, searching graphene under optical microscope, followed by checking in Raman spectroscope, is highly recommended to surely confirm whether the target sample is a single-layer graphene or not.

1.3 Graphene based field-effect transistors (GFET)

Although there exists zero band-gap in single-layer graphene, FETs with ambipolar gate modulation characteristic can still be realized based on it, generally in the structure as Figure 3(a). As shown in Figure 3(b), the field-effect is achieved via the gate modulation on the location of Fermi level. As for low temperature, when the Fermi level locates at the K (or K') point, the valence band is almost full and the conduction band is almost empty, which will lead to a very low concentration of carrier and hence a very high resistance. On the contrary, when the Fermi level moves into the valence or conduction band, the hole or electron conduction begins to dominate the current transport and hence the resistance becomes low. Due to the existing zero band-gap, the GFET can not be turned off completely. The typical transfer and output characteristics of GFET are shown in Figure 3(c) and (d). It is worth noticed the kink property in the output curve at the saturation region, due to the carrier type transition [46].

Owing to the low on/off ratio in GFET, people are eager to open a band-gap in graphene, and there are mainly two methods. One is to tailer the graphene to 1D size, i.e. graphene nanoribbon (GNR), and the quantum confinement to sub-10 nm size will lead to a considerable band-gap (> 100 meV) at room temperature [47,48]. GNRs can be derived from graphene also via chemical solution method [49], unzipping CNTs [38,50], and introducing nanowire (NW) as etching mask [51], etc. Unfortunately, carrier mobility decreases for increasing band-gap [10], since the effective mass increases, attributed to the deviation from the linear *E*-*k* relation, and moreover the edge of GNR will introduce extra scattering to the system. The most attractive advantage of graphene, the ultra high mobility, has to be sacrificed if we want to utilize the band-gap in graphene, and obviously it is not an advisable idea to make such a compromise. The other method is to bias the bi-layer graphene and hence the electric field will induce a band gap up to 250 meV, and the general approach to bias graphene is to apply a dual-gate structure to the device, i.e.

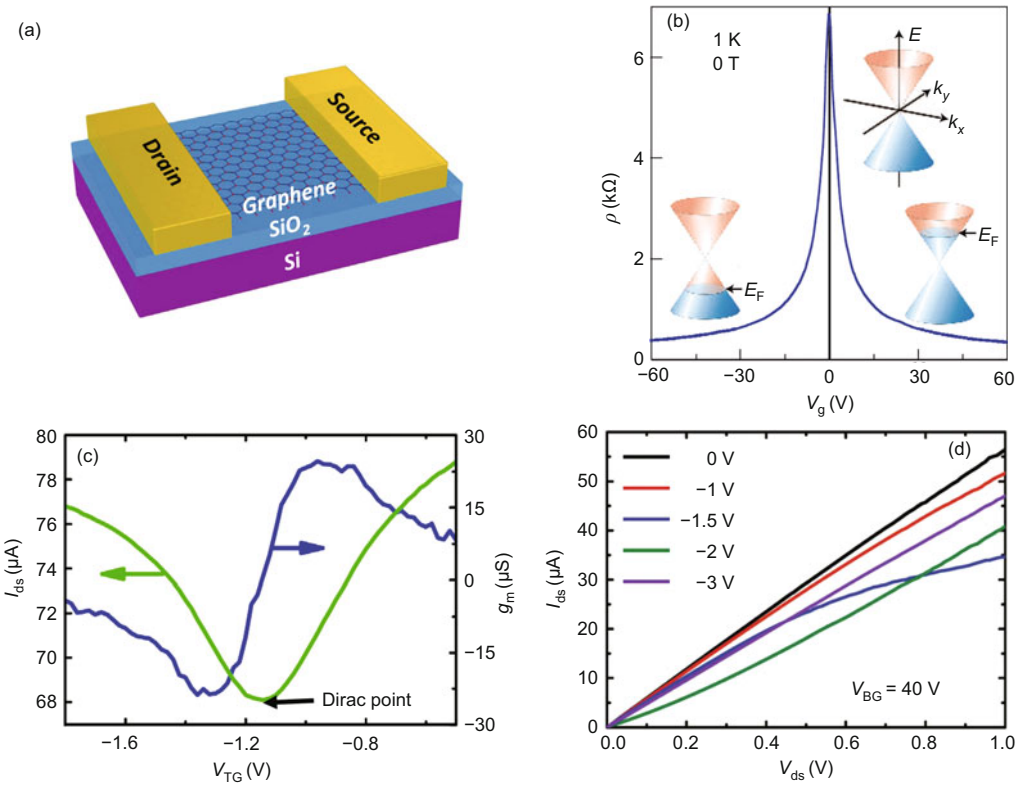

Figure 3 The structure and characterization of GFET. (a) A typical structure of back-gate GFET, with Si/SiO_2 as the gate. (b) The resistance modulation based on GFET, with the depicted band occupid status for high and low resistance state. (c) Top-gate transfer characteristics for a GFET. (d) Top-gate output characteristics of a GFET. Reprinted of (b) with permission from Ref. [5]. Copyright (2007) Macmillan Publishers Ltd. Reprinted of (c) with permission from Ref. [44]. Copyright (2010) American Institute of Physics. Reprinted of (d) with permission from Ref. [45]. Copyright (2010) American Chemical Society.

top-gate along with back-gate structure [52–54]. Besides, there are many other methods to introduce band-gap, such as substrate-induced band-gap [55], molecule adsorption [56], *etc*, but these methods are less reliable and controllable. Based on biased bi-layer graphene with considerable band-gap, digital logic units such as complementary-like NOT-, NOR-, and NAND-gate are all realized [57,58].

2 Gate dielectric for graphene transistors

2.1 High-κ dielectric growth on graphene

If we want to improve the performance of a FET, the most efficient way is to increase the saturation current [59]

$$I_{\mathrm{DS,sat}} = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W}{L_{\mathrm{g}}}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2, \qquad (5)$$

where μ is the mobility of the carrier, C_{ox} is the gate oxide capacitance of unit area, W and L_{g} are the width and length of the channel, V_{GS} and V_{T} are the gate voltage and the threshold voltage respectively. Hence we can increase the current by increasing the material mobility, which is however already fixed for a certain kind of material, and we can also shorten the channel length, which is what the Moore's law tells us to do [60,61]. Besides, we can increase the gate oxide capacitance $C_{\mathrm{ox}} = \epsilon_0\kappa/t_{\mathrm{ox}}$ by shrinking the oxide thickness (t_{ox}) or increasing the dielectric constant (κ). In practice, we have to increase κ instead of shrinking t_{ox} too much, since the oxide with excessive small physical thickness will lead to large leakage current, and consequently increase the standby power. To improve performance and simultaneously avoid leakage current while scaling-down, high-κ dielectrics such as hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), and yttrium oxide (Y_2O_3), are strongly suggested in GFETs, as well as in Si CMOS FETs.

The general method to form the high-κ oxide is the atomic layer deposition (ALD) method, which requires a nucleation layer for the thin film growth. However, for sp^2 hybridization plane, such as graphene and CNTs, there exists no dangling bonds for ALD nucleation. The thin film is not able to grow directly on graphene or CNTs, except for edges or where there are defects as shown in Figure 4(a), so they need functionalization before the ALD growth [62,63]. Non-covalent functionalization layer (NCFL) can be formed prior to ALD growth via molecules like DNA [62], 3,4,9,10-perylene tetracarboxylic acid (PTCA) [63], and NO_2 shown in Figure 4(b) [64–67]. Besides molecules, polymer can also play the role of NCFL, such as NFC polymers [54,68,69], and ozone pre-treatment (Figure 4(c)) is proved to work for ALD growth as well [70]. Moreover, directly constructing nucleation layer via oxidation of thin film of evaporated or sputtered Al (several nm), followed by Al_2O_3 ALD growth, is also a choice to form dielectric on graphene surface [71,72].

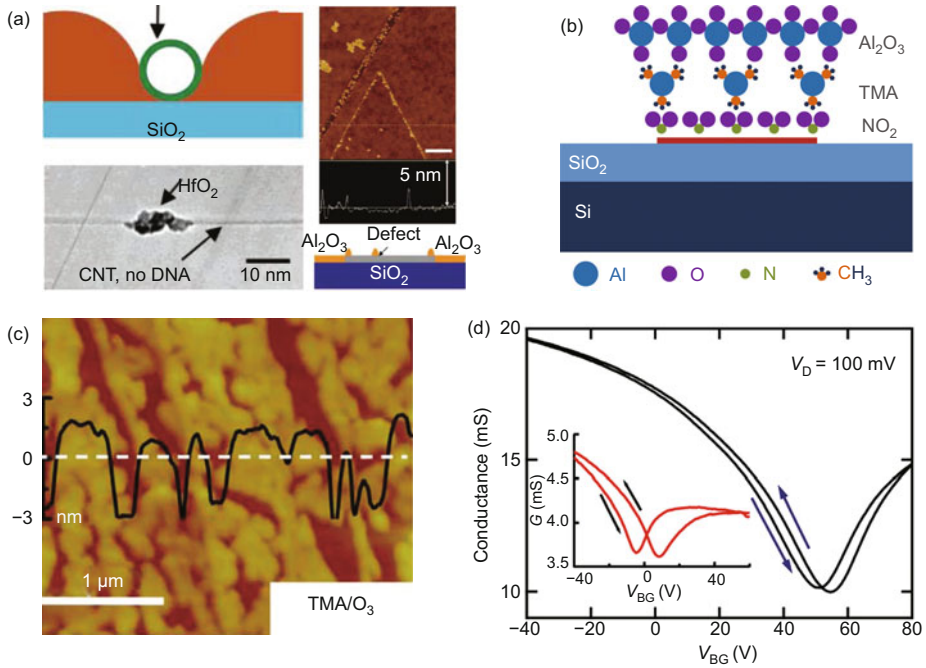

Figure 4 High-κ dielectric growth on graphene. (a) ALD is not compatible with CNT and graphene without any functionalization. (b) NO_2 functionalization before ALD growth on graphene. (c) The AFM image of graphene with ozone treatment before ALD growth. (d) The surface damage introduced by functionalization, which largely degrade the conductance of the GFET. Reprinted of (a) with permission from Refs. [62] and [63]. Copyright (2006) & (2008) American Chemical Society. Reprinted of (c) with permission from Ref. [70]. Copyright (2008) American Institute of Physics. Reprinted of (d) with permission from Ref. [67]. Copyright (2009) American Chemical Society.

Unfortunately, functionalization will cause some problems, such as introducing extra scattering centers and surface damages, hence reducing the current and transconductance as shown in Figure 4(d) [67,73]. The interlayer functional molecule will also introduce a gap between the channel and gate oxide, largely reducing the gate modulation efficiency, and hence weakening the transistor performance.

2.2 Yttrium oxide for graphene top-gate device

Yttrium oxide shows following properties, which ensure it is a suitable dielectric for graphene: (i) excellent wetting property on graphene without functionalization or damage (Figure 5(a)); (ii) good insulation property with low leakage current and high breakdown voltage; (iii) dielectric constant κ as high as 10–20, leading to ideal gate modulation; (iv) simple process flow with several nanometers yttrium evaporation and followed thermal oxidation on a 180°C hot plate for 10 min; (v) cheap source materials (yttrium) benefiting the industry cost [45].

Yttrium oxide can be utilized both on CNTs and graphene. The room temperature theoretical limit subthreshold swing of 60 mV/dec is achieved based on a single-walled CNT, indicating the high efficiency of the oxide. As for graphene, a dual gate FET is successfully realized, with 5 nm Y_2O_3 top-gate and 300 nm SiO_2 back-gate (Figure 5(b)). The top-gate to back-gate capacitance ratio C_{TG}/C_{BG} can be derived from the slope of the V_{BG}-$V_{TG,Dirac}$ curve [71]

$$\frac{C_{TG}}{C_{BG}} = -\frac{\Delta V_{BG}}{\Delta V_{TG,Dirac}}, \tag{6}$$

as high as about 100, suggesting a very efficient gate oxide with unit area capacitance of about 1200 nF/cm^2 (Figure 5(c)). From the transfer curve of graphene, we can extract some parameters such as mobility μ, residual carrier density n_0, and contact resistance R_C by fitting the curve to [71]

$$R_{total} = R_C + \frac{1}{e\mu\sqrt{n_0^2 + n^2}}\frac{L_g}{W}, \tag{7}$$

where $R_{total} = V_{DS}/I_{DS}$ is the total resistance of the device, n is the carrier concentration induced by the gate voltage via

$$V_{GS} - V_{Dirac} = \frac{ne}{C_{ox}} + \frac{\hbar v_F\sqrt{\pi n}}{e}. \tag{8}$$

According to the extracted mobility, from 1200 cm^2/(V s) before growth to 1000 cm^2/(V s) after growth, no large degradation has been observed, indicating a harmless process to the graphene channel (Figure 5(d)).

The property of the yttrium oxide can be further optimized, leading to a ratio C_{TG}/C_{BG} as high as 204 after gate thickness vertically scaling down to 3.9 nm as shown in Figure 5(e), with an equivalent oxide thickness (EOT) of 1.5 nm and a dielectric constant of $\kappa = 10$ [74]. The oxide capacitance of

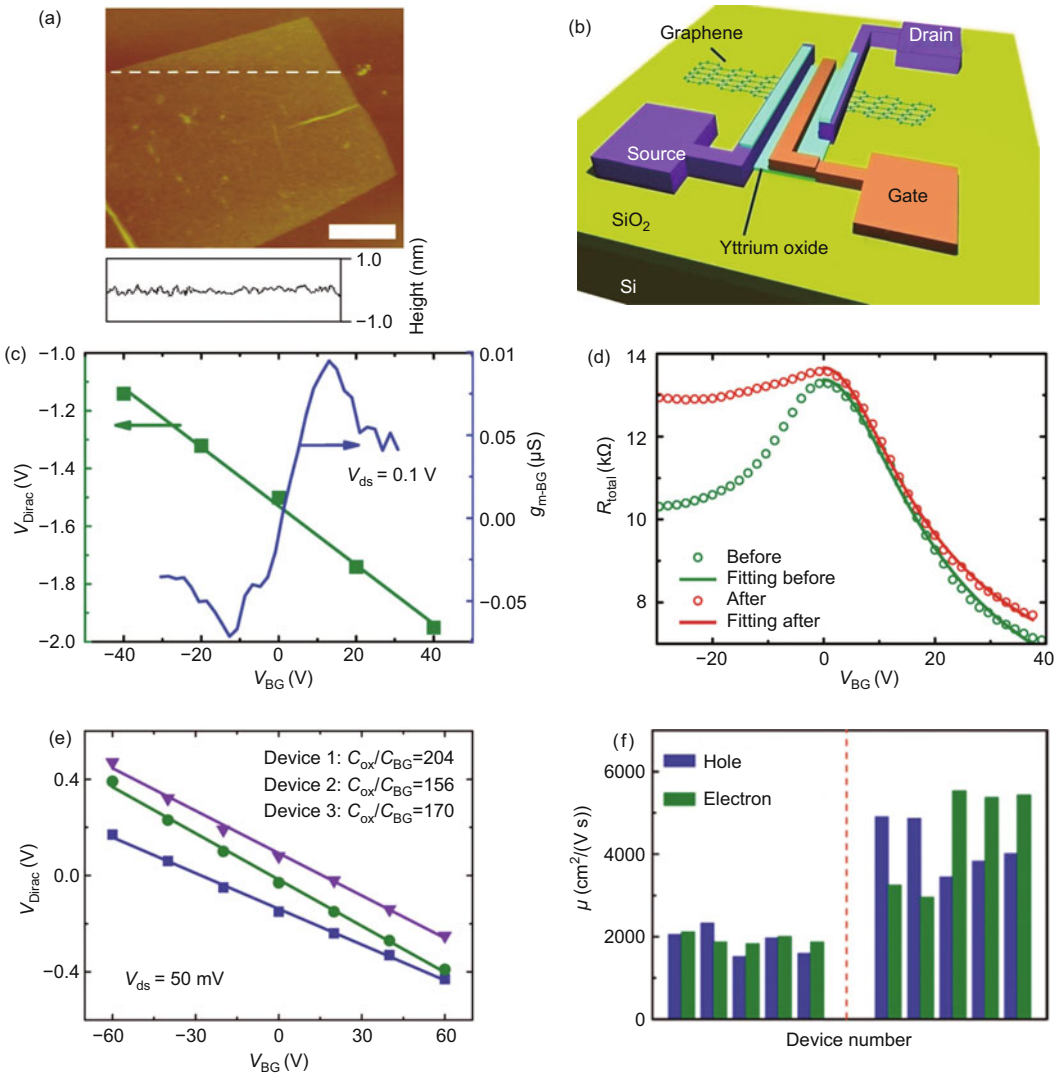

Figure 5 GFETs with Y_2O_3 top-gate. (a) AFM image of graphene covered with about 5 nm Y_2O_3 thin film, indicating a smooth morphology of the Y_2O_3 thin film. Scale bar is 1 μm. (b) The geometry of Y_2O_3 top-gate GFET. (c) Top-gate Dirac point position and back-gate transconductance versus back-gate voltage, and the inverse of the slope of the line gives the capacitance ratio: C_{TG}/C_{BG}. (d) The resistance transfer curve before and after Y_2O_3 deposition, and the mobility can be extracted by fitting the curve to eq. (7). (e) The scaling property of Y_2O_3. (f) The mobility of GFETs is systematically improved by increasing the oxidation temperature of Y_2O_3 from 180 to 270°C. Reprinted of (a)–(d) with permission from Ref. [45]. Copyright (2010) American Chemical Society. Reprinted of (e) with permission from Ref. [74]. Copyright (2011) American Chemical Society. Reprinted of (f) with permission from Ref. [76]. Copyright (2011) American Chemical Society.

Y_2O_3 on graphene is about 2280 nF/cm^2, the largest one realized on solid state GFETs to date, also comparable and even larger than the quantum capacitance of graphene, which can provide sufficient gate control for short channel GFET down to 1 nm and suggests that Y_2O_3 may be the ultimate dielectric material for graphene [74,75]. Meanwhile, if the oxidation temperature is simply increases from 180 to 270°C, the mobility can systematically reaches as high as about 4000–5000 cm^2/(V s) as shown in Figure 5(f) [76]. The transconductance normalized by dimension and drain voltage is found to reach 7900 μF/(V s), which is among the largest of the published data about graphene FETs. Hence, in an as-fabricated graphene FET with a gate length of 310 nm, a peak transconductance of 0.69 mS/μm is realized.

3 High frequency performance of GFET

3.1 Figure of merit for high frequency characterization

From the view of network analysis, GFET can be considered as a two-port network for RF characterization, with gate as input port, drain as output port, and common source grounded as shown in Figure 6(a). The AC signal ($I_{GS,AC}$, $V_{GS,AC}$, $I_{DS,AC}$, $V_{DS,AC}$) and relations between each other are all functions of DC bias along with frequency ($V_{GS,Bias}$, $V_{DS,Bias}$, f), and the target of RF characterization is to find out all these functions. The functions can be represented in many forms, leading to different network parameters. If we label input port as port 1, and output port as port 2, we have impedance parameters (Z parameters, Figure 6(b))

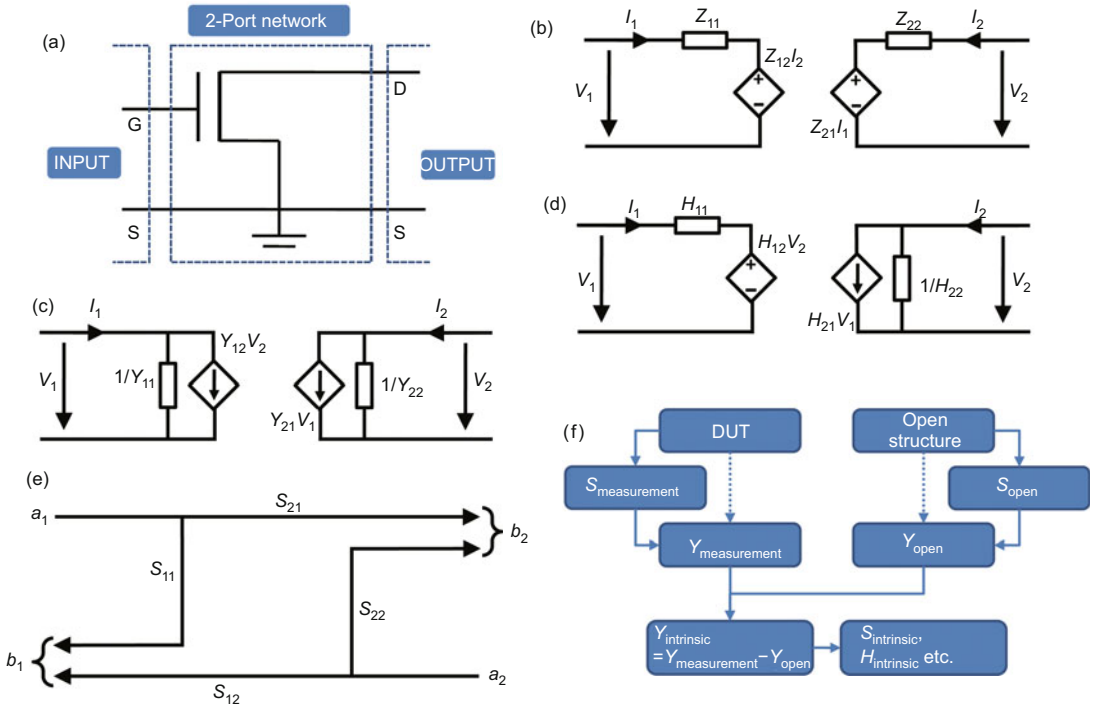

Figure 6 RF characterization of GFETs, based on (a) two-port network and models for (b) Z parameters, (c) Y parameters, (d) H parameters, and (e) S parameters. (f) The de-embedding procedure for intrinsic properties extraction.

in the following relation

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}, \tag{9}$$

where the matrix elements $Z_{11}, Z_{12}, Z_{21}, Z_{22}$ are the Z parameters. Similarly, we have admittance parameters (Y parameters, Figure 6(c)) $\boldsymbol{Y} = \boldsymbol{Z}^{-1}$ in the following relation

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}. \tag{10}$$

Moreover, there are hybrid parameters [H parameters, Figure 6(d)] based on small signal model, shown in the following relation

$$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ V_2 \end{pmatrix}, \tag{11}$$

where H_{11} is the input impedance, H_{22} is the output admittance, H_{12} is the reverse voltage gain, and H_{21} is the forward current gain. From $|H_{21}|$-f curve, we can obtain the most important figure of merit for RF characterization, cutoff frequency (f_{T}), where forward current gain H_{21} reaches unit gain (0 dB).

In RF domain or higher frequency, the concept of wave is suitable to describe the network rather than voltage or current. If we denote the incident waves at port 1 and 2 as a_1 and a_2, the reflected waves at port 1 and 2 as b_1 and b_2, the relation between them can be described by scattering parameters (S parameters, Figure 6(e)) in the following relation

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \tag{12}$$

where S_{11} and S_{22} are the reflection coefficients at input and output ports, S_{12} and S_{21} are the transmission coefficients at output and input ports. People are able to obtain S parameters directly from a network analyzer, and afterwards all the other parameters, including Z, Y, and H parameters, can be deduced based on S parameters [77]. Particularly, we can derive another significant parameter, maximum oscillation frequency (f_{max}), defined as the frequency when maximum available power gain (MAG) reaches unit power gain point (0 dB). There are also Mason's unilateral power gain (U), based on which we can define f_{max} as well, and the figures calculated from different methods are supposed to be almost the same [72]. The figures f_{T} and f_{max} determine the frequency working potential and ability of GFETs, and also provide references for high frequency circuit design.

Furthermore, the extrinsic and intrinsic properties should be addressed here as well. The extrinsic property, which is derived from the direct measurement results, includes the parasitic and non-intrinsic effects of the test pads, probes, coaxial cables, and electric measurement equipment. Mostly, we want to obtain the property of the device itself, as a result we have to extract the intrinsic property from the extrinsic one, which is called a de-embedding procedure, shown in Figure 6(f). It is worth noticing that open structure is needed and Y

parameters play an intermediary role in this procedure.

3.2 Frequency response of GFET

Based on the small-signal mode shown in Figure 7, f_T of GFET can be derived as [10]

$$f_T \simeq \frac{g_m}{2\pi} \frac{1}{(C_{GS}+C_{GD})[1+g_{DS}(R_S+R_D)]+C_{GD}g_m(R_S+R_D)}, \quad (13)$$

where $g_m \equiv \partial I_{DS}/\partial V_{GS}$ is the transconductance of the device, $g_{DS} \equiv \partial I_{DS}/\partial V_{DS}$ is the drain conductance, C_{GS} and C_{GD} are the gate-source and gate-drain capacitances, and R_S and R_D are the source and drain series resistances. From eq. (13), increasing g_m can be a very effective way to improve f_T, and the basic method to enhance g_m is to increase gate capacitance, i.e. C_{GS} and C_{GD}, which will decrease f_T, as a result, trade off should be made between g_m and $(C_{GS} + C_{GD})$ while optimizing f_T. Moreover, decreasing R_S and R_D, such as improving the contact resistance, which is not a well solved problem yet, can be significant for f_T enhancement as well [78]. Besides, biasing the device to saturation region, where $g_{DS} \to 0$, is another key approach to obtain high f_T, although current saturation is not very easy to accomplish and not well behaved as well [46,79]. The intrinsic f_T, excluding the effect of series resistance, can be represented by two limits [80]

$$f_{T,\text{intrinsic}} = \begin{cases} \mu(V_{GS} - V_T)/2\pi L_g^2 & \text{for large } L_g \\ v_{sat}/2\pi L_g & \text{for small } L_g \end{cases}, \quad (14)$$

where v_{sat} is the saturation velocity of the carrier. From eq. (14), we can predict that graphene will perform excellently up to THz frequency region, due to the particularly high carrier mobility and large saturation velocity [10]. The calculated intrinsic carrier mobility limited by acoustic phonon at room temperature reaches as high as 10^5 cm^2/(V s), which has never been predicted in other systems and nevertheless been experimentally confirmed in graphene [81–83]. Meanwhile, for short channel FET, saturation velocity is a key issue while discussing frequency response of the device. For graphene, maximum carrier velocity reaches as high as 4×10^7 cm/s, comparing to 2×10^7 cm/s for GaAs and 10^7 cm/s for silicon (Figure 8(a)). What is more, at ultrahigh electric field the velocity in graphene will never drop drastically as in III-V semiconductors, which will lead to f_T decreasing while scaling down to short channel, as shown in Figure 8(b).

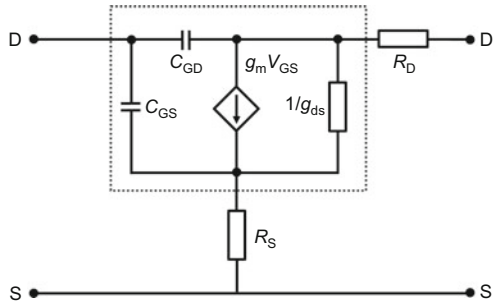

Figure 7 Small-signal equivalent FET circuit.

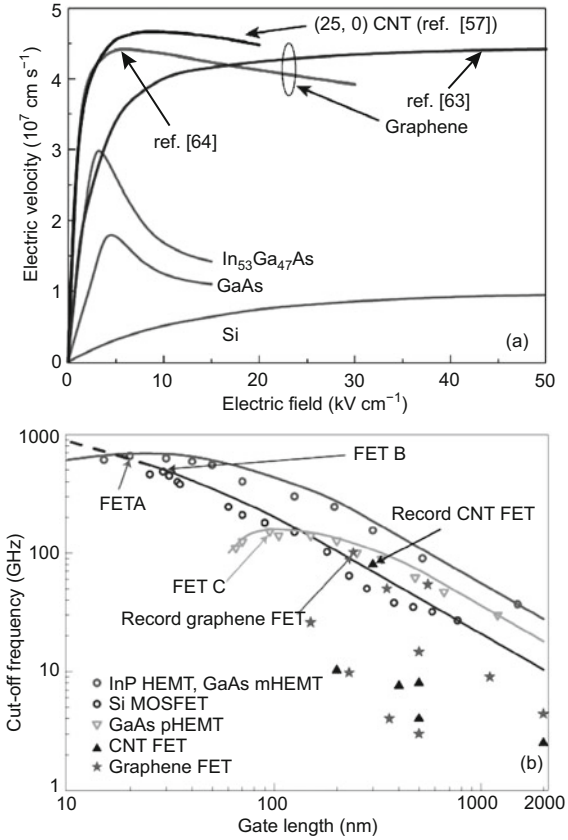

Figure 8 Comparing (a) electron drift velocities and (b) cut-off frequencies for different FETs, including FETs based on common semiconductors (Si, III-V compound), CNTs and large-area graphene. Reprinted with permission from Ref. [10]. Copyright (2010) Macmillan Publishers Ltd.

The first RF test on graphene was performed in 2008, with top-gate geometry and standard S parameter measurement, and a f_T of 14.7 GHz was realized after de-embedding, while $f_{max} < 1$ GHz [84]. The milestone achievements in high frequency performance of graphene are listed in Table 1, with several important factors which are often considered in experiments. We notice that the substrate must be carefully selected, to eliminate the parasitic effect via the substrate and the scattering induced by substrate. For convenient consideration, high resistivity (ρ >10 kΩ cm) Si wafer with SiO_2 as the insulation layer are usually used. Besides, insulating SiC substrate is a better choice, but the cost is much higher than Si wafer. Very recently, diamond like carbon (DLC), amorphous carbon containing a large fraction of sp^3 configuration, was introduced as the substrate for GFET [24]. Comparing to SiO_2, DLC has higher surface phonon energy (165 meV, comparing to 59 meV in SiO_2) and lower surface trap density, which benefit the carrier transport, and DLC is nonpolar, chemically inert as well, leading to a f_T = 155 GHz for 40 nm channel length based on epitaxial graphene, as shown in Figure 9(a) and (b). The realized highest f_T is 300 GHz

Table 1 List of the achievements in high frequency performance of graphene

	L_g	f_T (GHz)	$f_T L_g$ (GHz μm)	f_{max} (GHz)	Substrate	Graphene	Mobility ($cm^2/(V\,s)$)
Meric et al. 2008 [84]	500 nm	14.7	7.35	< 1	Si (ρ =20 kΩ cm)	Exfoliated	1200
Moon et al. 2009 [86]	2 μm	4.2 a)	8.4 a)	14 a)	SiC	CVD on SiC	~1000
Lin et al. 2009 [67]	150 nm	26	3.9	N/A	Si (ρ >10 kΩ cm)	Exfoliated	400
Lin et al. 2010 [87]	350 nm	50	17.5	N/A	Si (ρ >10 kΩ cm)	Exfoliated	2700
Lin et al. 2010 [69]	240 nm	100	24	10 b)	SiC	CVD on SiC	900–1500
Liao et al. 2010 [23]	144 nm	300	43.2	N/A	Si (ρ >18 kΩ cm)	Exfoliated	>20000
Wu et al. 2011 [24]	40 nm	155	6.2	N/A c)	DLC	CVD on copper	500–600

a) Extrinsic value; b) 14 GHz for L_g = 550 nm; c) 20 GHz for L_g = 550 nm, and 13 GHz for L_g = 140 nm.

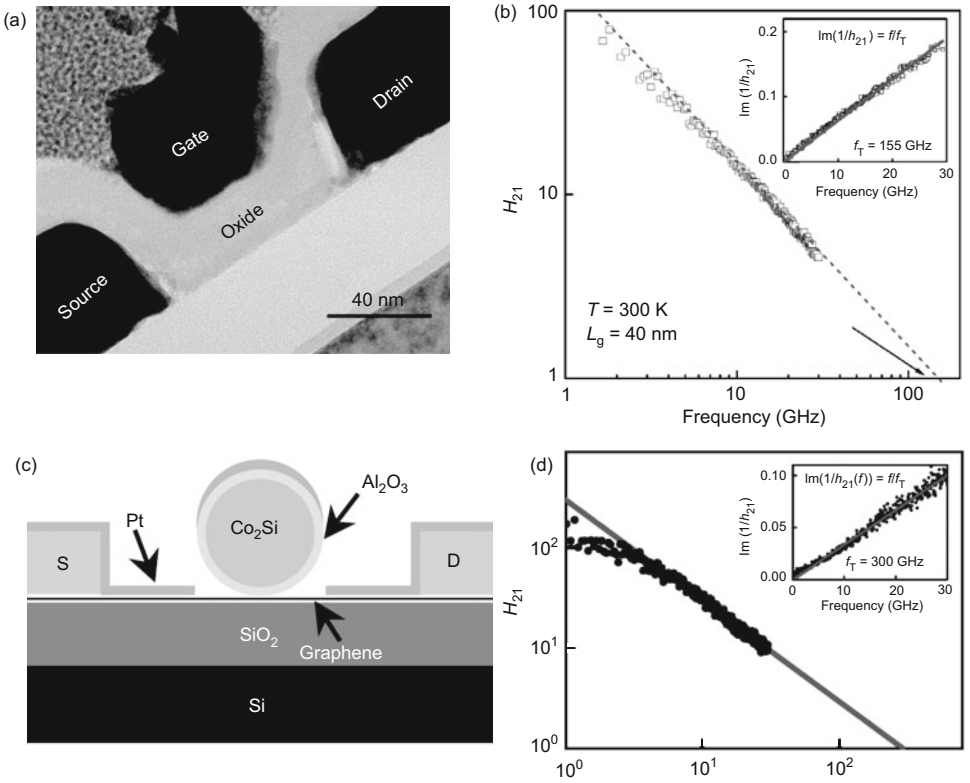

Figure 9 Frequency response characterization for GFET. (a) Cross-section TEM image of a graphene transistor on DLC with a gate length of 40 nm. (b) Cut-off frequency for the device with a gate length of 40 nm at room temperature. The intercept of small-signal current gain $|H_{21}|$ versus frequency relation gives the cut-off frequency as 155 GHz. (c) Schematic of the cross-sectional view of a high-speed graphene transistor with a Co_2Si-Al_3O_3 core-shell NW as the self-aligned top-gate. (d) The intercept of small-signal current gain $|H_{21}|$ versus frequency relation gives the cut-off frequency as 300 GHz for the device with a gate length of 144 nm. Reprinted of (a) and (b) with permission from Ref. [24]. Reprinted of (c) and (d) with permission from Ref. [23]. Copyright (2011) & (2010) Macmillan Publishers Ltd.

after de-embedding based on a Co_2Si-Al_2O_3 core-shell NW self-aligned gate GFET (Figure 9(c) and (d)), although the extrinsic cutoff frequency before de-embedding is 2.4 GHz [23]. However, the achieved highest f_{max} is far below expectation, about 20 GHz, which is due to the detail of the device design such as the gate metal thickness and hence the resistance, for example, a thick T-shaped gate may help to realize high f_{max} [24]. Based on eq. (14) at the small gate length limit, one can tell that $f_T L_g = v_{sat}/2\pi \simeq 60$ GHz μm, where $v_{sat} \simeq 4 \times 10^7$ cm/s, represents the intrinsical high frequency transport property of graphene, and the $f_T L_g$ listed in Table 1 are all below the theoretical value, while the typical $f_T L_g$ value for Si NMOS is only about 9 GHz μm [85].

Besides, as shown in Figure 10, graphene based high frequency voltage amplifier is realized, with ~5 dB low frequency gain and 3 dB bandwidth greater than 6 GHz [88]. The back embedded gate structure with ultra thin gate oxide leads to a current saturation, which enables high frequency

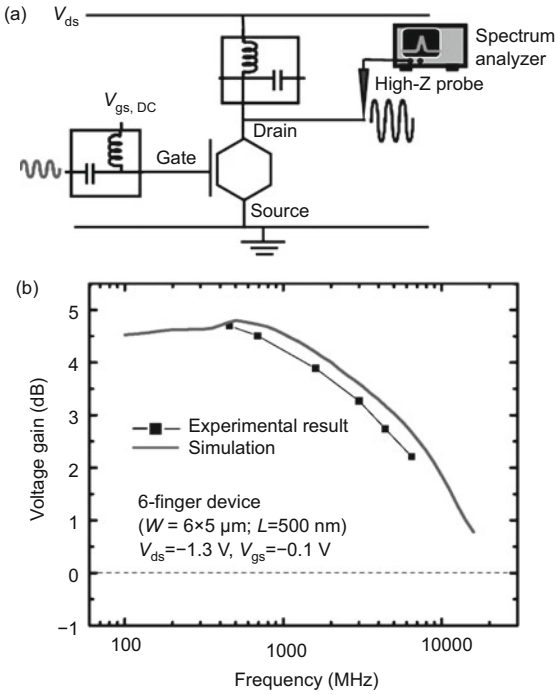

Figure 10 Graphene Amplifier. (a) Schematic of the measurement technique. (b) Measured and simulated frequency response of the amplifier's voltage gain. Reprinted with permission from Ref. [88]. Copyright (2011) American Chemical Society.

voltage gain.

To optimize high frequency performance of graphene, increasing mobility and decreasing access resistance can be crucial [24]. In order to enhance mobility on substrate, the surface need careful treatment before graphene exfoliation or growth on. To decrease the access resistance, there are two approaches, including reducing the contact resistance and utilizing self-aligned gate to shorten the un-gated region without gate control. To properly contact graphene with metal, many efforts have been made and there are seldom useful laws about graphene-metal contact resistance, so the contacting issue is urgently needed to be solved [78]. Besides, a suitable self-aligned gate profile needs to be developed as well.

4 Ambipolar electronics based on graphene

Comparing to sacrificing mobility for band gap opening, directly taking advantage of the ambipolar property of graphene for RF applications seems a better choice. Ambipolar electronics based on graphene has attracted lots of attention in the field of graphene application, such as frequency doublers, mixers, digital modulators, phase detectors, etc. The symmetric I_{DS}-V_{GS} relation around Dirac point plays an importance role in the applications.

$$I_{DS} = a_0 + a_2 (V_{GS} - V_{Dirac})^2 + a_4 (V_{GS} - V_{Dirac})^4 + \cdots . \quad (15)$$

For ambipolar applications, the test is always configured as shown in Figure 11, with the gate electrode as the input port, the output port (drain electrode) biased with V_{DD}

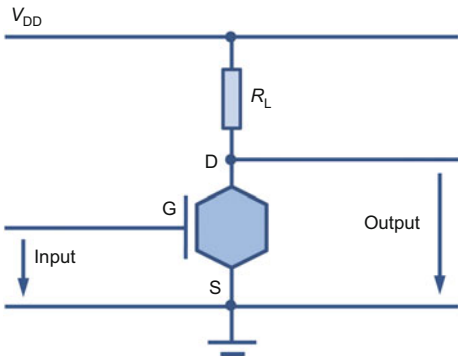

Figure 11 Typical circuit configuration for ambipolar electronics based on GFET.

via a load resistor R_L, and source electrode grounded. Hence, the output voltage can be described as

$$V_{DS} = V_{DD} - I_{DS}R_L, \quad (16)$$

where V_{DS}-V_{GS} relation shows similar shape with I_{DS}-V_{GS} relation but a negative sign.

4.1 Frequency doublers

If I_{DS}-V_{GS} relation of GFET performs perfect parabolic property about Dirac point

$$I_{DS} = a_0 + a_2 (V_{GS} - V_{Dirac})^2 , \quad (17)$$

and the input gate sinusoidal signal is biased at Dirac point with an amplitude of A and radian frequency of ω

$$V_{GS} = V_{Dirac} + A \sin \omega t. \quad (18)$$

From eqs. (16)–(18), we can deduce the output drain voltage as

$$V_{DS} = V_{DS,0} + \frac{1}{2} a_2 R_L A^2 \cos 2\omega t, \quad (19)$$

where $V_{DS,0} = V_{DD} - a_0 R_L - a_2 R_L A^2/2$. Clearly, the output frequency is doubled purely via the simple GFET, and the deviation from the ideal parabolic relation will lead to more even-order harmonics, such as quadruple and sextuple frequencies. Odd-order harmonics will also be introduced to the system once the I_{DS}-V_{GS} relation deviates to an asymmetric shape. Similarly, from the principle illustration in Figure 12(a), we can also easily tell that an input single period of sinusoidal wave will lead to double period at the output port.

Wang et al. [89] reported ambipolar frequency doubler based on exfoliated graphene for the first time in 2009, which showed a frequency response up to 10 kHz and output second-order harmonic wave purity of more than 90%. A single transistor is enough for frequency doubling while filters or rectification units are not necessary. However, the signal gain of the back-gate setup is very low (less than 1/200) due to its small transconductance for typical back-gate GFETs. Afterwards, Y_2O_3 top-gate was introduced and utilized to graphene based frequency doubler as shown in Figure 12(b)–(d) [44]. Benefited by the high-efficiency gate oxide, the signal gain is increased by 10 times (as high as 1/20) compared to that of the back-gate geometry and the working

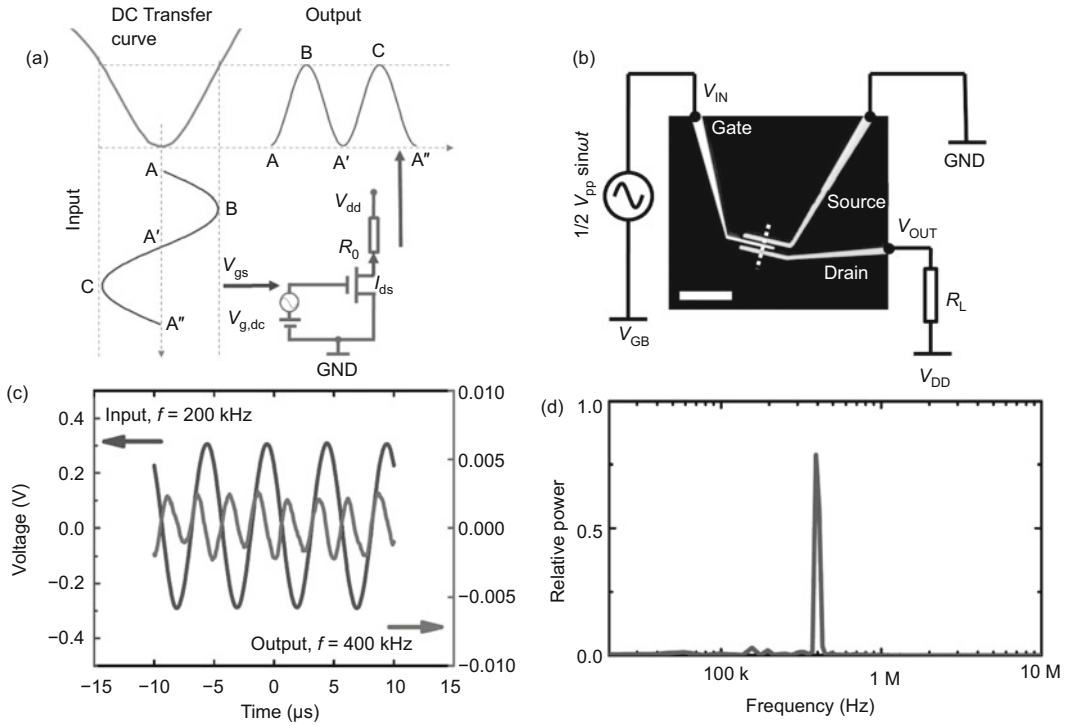

Figure 12 GFET based frequency doubler. (a) Schematic diagram showing the working principle of GFET based frequency doubler. (b) Optical microscope image depicts experimental configuration of the device. (c) Measured input and output waveform of the GFET based frequency doubler, with an input frequency of 200 kHz. (d) Power spectrum obtained via Fourier transforming the output signal in (c). Reprinted with permission from Ref. [44]. Copyright (2010) American Institute of Physics.

frequency was pushed to 200 kHz. The top-gate geometry also clearly improved the symmetric property of the transfer curve, which is needed in the frequency doubling operation. The operation frequency is limited by the testing system, including the substrate, pads, probes and cables, but the intrinsic frequency response of graphene can be very high. Besides, ambipolar frequency doublers based on wafer-scale CVD grown graphene are also realized, with frequency response up to 1.4 GHz, which demonstrated the great potential of graphene for RF applications [90].

Besides, frequency doubler can be also realized based on small band-gap (SBG) CNT, which behaves the similar ambipolar transport property as graphene, as shown in Figure 13(a) [91]. Comparing to graphene, SBG CNT exhibit extremely higher carrier mobility on SiO_2 substrate due to the suppressed substrate scattering, which is shown in Figure 13(b) [92]. Moreover, the easy-obtained saturation behavior of CNT FETs, which is usually hard to be realized in GFETs, is also one of the advantages for achieving a higher operation frequency and gain (more than 0.15), as shown in Figure 13(c). Also, the output of the frequency doubler is of high second-order harmonic purity, as shown in Figure 13(d).

4.2 RF mixers

In telecommunications, a mixer is a nonlinear device that receives two different frequencies at the input port and appears a mixture of several frequencies at the output, including both original input frequencies, the sum of the input frequencies, the difference between the input frequencies, and other intermodulations [93]. If we apply two sinusoidal waves $A_1 \sin \omega_1 t$ and $A_2 \sin \omega_2 t$ to the input port, where A_1, A_2 are the amplitudes and ω_1, ω_2 are the radian frequencies of the two input signal, based on eq. (15) the output will appears no odd-order intermodulations, which can be usually detected in conventional unipolar mixers and affect the dynamic range for circuit operations. Deviation from the ideal symmetric property will introduce some odd-order intermodulations.

While a RF signal and local oscillator (LO) signal with frequencies of f_{RF} and f_{LO} are applied to the input of an ambipolar mixer based on graphene, in the frequency spectrum of the output, the power at even-order frequencies is higher than the power at the odd-order frequencies, which is consistent with the prediction that the odd-order intermodulations are suppressed. The performance of the mixer can be enhanced by improving the symmetry of the transfer property [94]. Afterwards, an integrated circuit including ambipolar mixer and on-wafer inductors for DC coupling, is realized based on graphene epitaxial grown on SiC, and the mixer can work at frequency as high as 10 GHz, also with temperature stability (performance reduction less than 1 dB) between 300 and 400 K, which also revealed the wafer-scale application for graphene based mixer [25].

4.3 Digital modulators

Since graphene can work as both frequency doublers and amplifiers (in-phase or anti-phase), and the working mode can

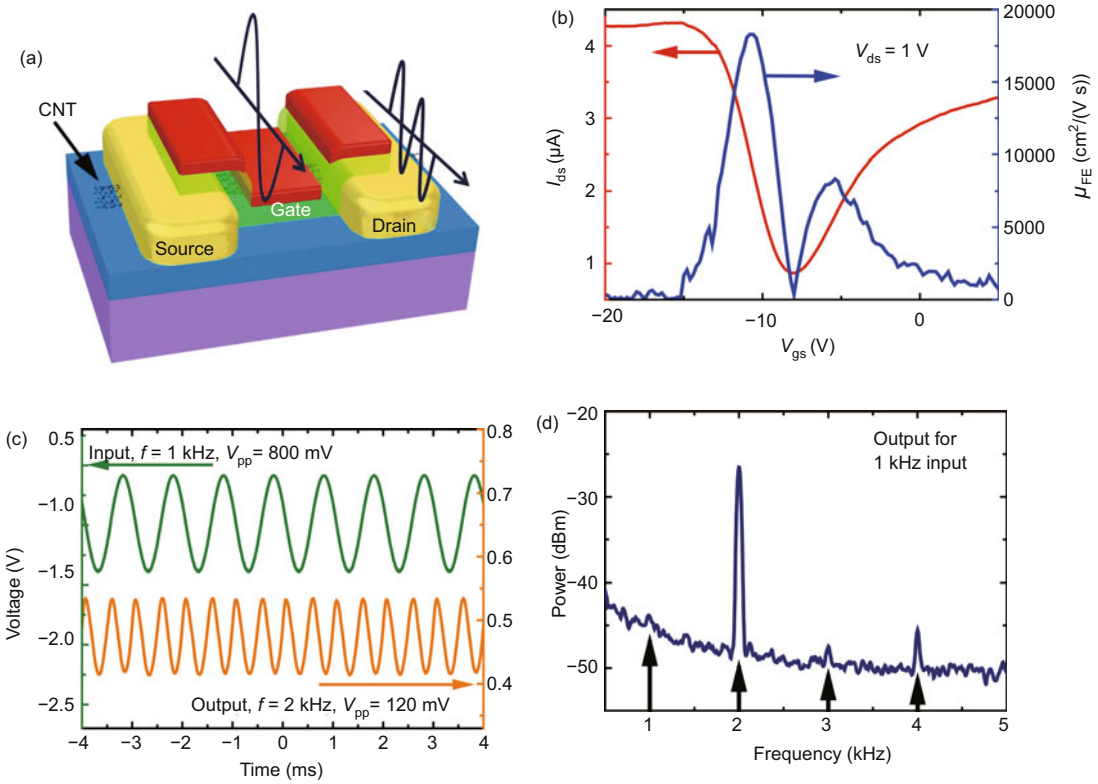

Figure 13 Frequency doubler based on SBG CNTs. (a) Schematic diagram illustrating the geometry of a CNT based ambipolar FET and its working principle as a frequency doubler. (b) Transfer characteristic for a long channel back-gate CNT FET (left scale) and corresponding field-effect mobility curve (right scale). (c) AC performance of a CNT based frequency doubler, with input and output waveform for an input 1 kHz sinusoidal wave. (d) Measured output signal spectrum for 1 kHz input. The four arrows indicate the frequencies of 1, 2, 3 and 4 kHz, respectively from left to right. Reprinted with permission from Ref. [91]. Copyright (2010) American Chemical Society.

be transformed between each other simply by changing the bias voltage of the input signal of the GFET, signal modulators such as phase shift keying (PSK) and frequency shift keying (FSK) can be realized based on ambipolar GFET. As shown in Figure 14(a), we define p-region with negative transconductance as Region I, the region around Dirac point as Region II, and n-region with positive transconductance as Region III, and along with eq. (16) the gain shows different sign with transconductance

$$A_{\rm v} \equiv \frac{\partial V_{\rm DS}}{\partial V_{\rm GS}} = -g_{\rm m}\frac{R_{\rm out}R_{\rm L}}{R_{\rm out}+R_{\rm L}}, \tag{20}$$

where $R_{\rm out}$ is the output resistance of the FET. The gain in Region I is positive due to the negative transconductance and the device acts as an in-phase amplifier, while the gain in Region III is negative due to the positive transconductance and the device acts as an inverted amplifier. In Region II, the device transfers between n-region and p-region alternately, resulting in frequency doubling.

Based on the configuration shown in Figure 14(b), if the bias voltage alters between Region I and III and we denote Region I and III as binary "0" and "1" respectively, each alternation will introduce an inverting to the signal at the output and a transfer between "0" and "1" will be recognized. Hence, a binary phase shift keying (BPSK) is realized and this ambipolar GFET is proved to be used as a digital modulator before signal transmitted (Figure 14(c)). Similarly, the transfer between Region I/III and II will introduce a frequency alternation to the output signal. If we denote the fundamental and doubled frequency as binary "0" and "1" respectively, a binary frequency shift keying (BFSK) is realized based on the single transistor (Figure 14(d)). Yang et al. [95] successfully performed BFSK modulation based on the Kansas City standard (KCS) for audio cassette drives where fundamental frequency f = 1200 Hz and doubled frequency $2f$ = 2400 Hz. The proposed single transistor digital modulator can greatly simplify the circuit design in telecommunication applications.

4.4 Multiplier phase detectors

If we applied a sinusoidal wave $A_1\sin(\omega t+\theta_1)$ and a square wave $A_2\,\mathrm{rect}(\omega t+\theta_2)$ to the input of the phase detector, the DC component of the output can be written as the product of the two input signal [96]

$$A_{\rm d} = A_1A_2\frac{2}{\pi}\sin(\theta_1-\theta_2) \simeq K_{\rm d}\theta_{\rm e}, \tag{21}$$

where $K_{\rm d}$ is the gain of the detector and $\theta_{\rm e}$ is the phase difference in radians between the input signals. Hence, the relation

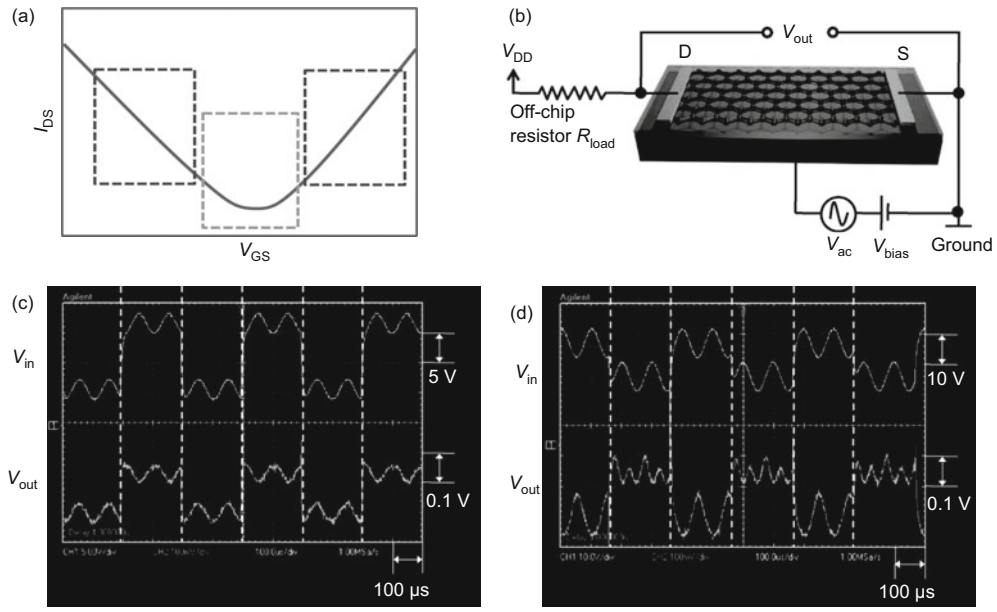

Figure 14 Digital modulators based on GFET. (a) Transfer curve of a typical GFET. (b) The schematic test configuration of the single transistor digital modulators. (c) The waveform for BPSK modulation. (d) The waveform for BFSK modulation. Reprinted of (b)–(d) with permission from Ref. [95]. Copyright (2010) American Chemical Society.

between DC component and the phase difference can be utilized for phase detection. A multiplier is generally needed for this process, which complicates the circuit. While for GFET, a single transistor can fulfill the phase detection and a gain of −7 mV/radian was reached, which can be further largely improved by reducing the series resistance, increasing the gate efficiency, and pushing the transistor to saturation region.

5 Conclusion and prospective

Graphene is a new but popular star in material research field, and especially of large potential for high frequency device and circuit applications, due to its ultra high mobility under low electric field and high saturation velocity under high electric field. By utilizing the ideal gate dielectric Y_2O_3 to the surface of graphene, high-performance GFET can be fabricated. GFET with frequency response up to hundreds of GHz was realized based on both mechanically exfoliated and epitaxial grown graphene, and the compatibility with traditional wafer-scale Si fabrication process flow was experimentally proved. Besides amplifiers with gain, GFET can be also used to build ambipolar devices and circuits such as frequency doublers, RF mixer, digital modulators and phase detectors. Furthermore, the wafer-scale integrated circuits based on graphene are realized, operating RF mixing up to 10 GHz frequency.

In general, graphene is a very promising kind of material for future RF analog ambipolar electronics. With the basic unit of high frequency applications, i.e. mixer and amplifier, and process circuits based on graphene, an integrated RF system can be fabricated solely on a large-area single layer graphene, which is compatible with Si CMOS fabrication process and of higher performance. However, large efforts still needs to be made for the problem that have not been solved, such as decreasing the contact resistance between graphene and metal, developing a suitable gate self-align profile for high frequency graphene devices, realizing controllable saturation property in GFET, and so on.

This work was supported by the Ministry of Science and Technology of China (2011CB933001 and 2011CB933002), and the National Natural Science Foundation of China (61071013).

1 Wallace P R. The band theory of graphite. Phys Rev, 1947, 71: 622–634
2 Peierls R E. Quelques proprietes typiques des corpses solides. Ann I H Poincare, 1935, 5: 177–222
3 Landau L D. Zur Th eorie der phasenumwandlungen II. Phys Z Sowjetunion, 1937, 11: 26–35
4 Novoselov K S, Geim A K, Morozov S V, et al. Electric field effect in atomically thin carbon films. Science, 2004, 306: 666–669
5 Geim A K, Novoselov K S. The rise of graphene. Nat Mater, 2007, 6: 183–191
6 Geim A K. Graphene: Status and prospects. Science, 2009, 324: 1530–1534
7 Avouris P, Chen Z H, Perebeinos V. Carbon-based electronics. Nat Nanotechnol, 2007, 2: 605–615
8 Burghard M, Klauk H, Kern K. Carbon-based field-effect transistors for nanoelectronics. Adv Mater, 2009, 21: 2586–2600
9 Taghioskoui M. Trends in graphene research. Mater Today, 2009, 12: 34–37
10 Schwierz F. Graphene transistors. Nat Nanotechnol, 2010, 5: 487–496
11 Bonaccorso F, Sun Z, Hasan T, et al. Graphene photonics and optoelectronics. Nat Photonics, 2010, 4: 611–622
12 Novoselov K S. Nobel Lecture: Graphene: Materials in the flatland.

Rev Mod Phys, 2011, 83: 837–849
13 Geim A K. Nobel Lecture: Random walk to graphene. Rev Mod Phys, 2011, 83: 851–862
14 Lee C, Wei X D, Kysar J W, et al. Measurement of the elastic properties and intrinsic strength of monolayer graphene. Science, 2008, 321: 385–388
15 Ghosh S, Calizo I, Teweldebrhan D, et al. Extremely high thermal conductivity of graphene: Prospects for thermal management applications in nanoelectronic circuits. Appl Phys Lett, 2008, 92: 151911
16 Seol J H, Jo I, Moore A L, et al. Two-dimensional phonon transport in supported graphene. Science, 2010, 328: 213–216
17 Freitag M, Chiu H Y, Steiner M, et al. Thermal infrared emission from biased graphene. Nat Nanotechnol, 2010, 5: 497–501
18 Castro Neto A H, Guinea F, Peres N M R, et al. The electronic properties of graphene. Rev Mod Phys, 2009, 81: 109–162
19 Das Sarma S, Adam S, Hwang E H, et al. Electronic transport in two-dimensional graphene. Rev Mod Phys, 2011, 83: 407–470
20 Novoselov K S, Geim A K, Morozov S V, et al. Two-dimensional gas of massless Dirac fermions in graphene. Nature, 2005, 438: 197–200
21 Katsnelson M I, Novoselov K S, Geim A K. Chiral tunnelling and the Klein paradox in graphene. Nat Phys, 2006, 2: 620–625
22 Bostwick A, Ohta T, Seyller T, et al. Quasiparticle dynamics in graphene. Nat Phys, 2007, 3: 36–40
23 Liao L, Lin Y C, Bao M Q, et al. High-speed graphene transistors with a self-aligned nanowire gate. Nature, 2010, 467: 305–308
24 Wu Y Q, Lin Y M, Bol A A, et al. High-frequency, scaled graphene transistors on diamond-like carbon. Nature, 2011, 472: 74–78
25 Lin Y M, Valdes-Garcia A, Han S J, et al. Wafer-scale graphene integrated circuit. Science, 2011, 332: 1294–1297
26 Bae S K, Kim H K, Lee Y B, et al. Roll-to-roll production of 30-inch graphene films for transparent electrodes. Nat Nanotechnol, 2010, 5: 574–578
27 Xia F N, Mueller Y, Lin Y M, et al. Ultrafast graphene photodetector. Nat Nanotechnol, 2009, 4: 839–843
28 Mueller Y, Xia F N, Avouris P. Graphene photodetectors for high-speed optical communications. Nat Photonics, 2010, 4: 297–301
29 Trauzettel B, Bulaev D V, Loss D, et al. Spin qubits in graphene quantum dots. Nat Phys, 2007, 3: 192–196
30 Huertas Hernando D, Guinea F, Brataas A. Spin orbit coupling in curved graphene, fullerenes, nanotubes and nanotube caps. Phys Rev B, 2006, 74: 155426
31 Avouris P. Graphene: Electronic and photonic properties and devices. Nano Lett, 2010, 10: 4285–4294
32 Emtsec K V, Bostwick A, Horn K, et al. Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide. Nat Mater, 2009, 8: 203–207
33 Sutter P W, Flege J I, Sutter E A. Epitaxial graphene on ruthenium. Nat Mater, 2008, 7: 406–411
34 Kim K S, Zhao Y, Jang H, et al. Large-scale pattern growth of graphene films for stretchable transparent electrodes. Nature, 2009, 457: 706–710
35 Stankovich S, Dikin D A, Piner R D, et al. Synthesis of graphene-based nanosheets via chemical reduction of exfoliated graphite oxide. Carbon, 2007, 45: 1558–1565
36 Hernandez Y, Nicolosi V, Lotya M, et al. High-yield production of graphene by liquid-phase exfoliation of graphite. Nat Nanotechnol, 2008, 3: 563–568
37 Dong X C, Shi Y M, Zhao Y, et al. Symmetry breaking of graphene monolayers by molecular decoration. Phys Rev Lett, 2009, 102: 135501
38 Jiao L Y, Zhang L, Wang X R, et al. Narrow graphene nanoribbons from carbon nanotubes. Nature, 2009, 458: 877–880
39 Blake P, Hill E W, Castro Neto A H, et al. Making graphene visible. Appl Phys Lett, 2007, 91: 063124
40 Gao L B, Ren W C, Li F, et al. Total color difference for rapid and accurate identification of graphene. ACS Nano, 2008, 2: 1625–1633
41 Ferrari A C, Meyer J C, Scardaci V, et al. Raman spectrum of graphene and graphene layers. Phys Rev Lett, 2006, 97: 187401
42 Malarda L M, Pimenta M A, Dresselhaus G, et al. Raman spectroscopy in graphene. Phys Rep, 2009, 473: 51–87
43 Lui C H, Liu L, Mak K F, et al. Ultraflat graphene. Nature, 2009, 462: 339–341
44 Wang Z X, Zhang Z Y, Xu H L, et al. A high-performance top-gate graphene field-effect transistor based frequency doubler. Appl Phys Lett, 2010, 96: 173104
45 Wang Z X, Xu H L, Zhang Z Y, et al. Growth and performance of yttrium oxide as an ideal high-κ gate dielectric for carbon-based electronics. Nano Lett, 2010, 10: 2024–2030
46 Meric I, Han M Y, Young A F, et al. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. Nat Nanotechnol, 2008, 3: 654–659
47 Son Y W, Cohen M L, Louie S G. Energy gaps in graphene nanoribbons. Phys Rev Lett, 2006, 97: 216803
48 Wang X R, Ouyang Y J, Li X L, et al. Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors. Phys Rev Lett, 2008, 100: 206803
49 Li X L, Wang X R, Zhang L, et al. Chemically Derived, Ultrasmooth graphene nanoribbon semiconductors. Science, 2008, 319: 1229–1232
50 Wang X R, Ouyang Y J, Jiao L Y, et al. Graphene nanoribbons with smooth edges behave as quantum wires. Nat Nanotechnol, 2011, 6: 563–567
51 Liao L, Bai J W, Cheng R, et al. Top-gated graphene nanoribbon transistors with ultrathin high-κ dielectrics. Nano Lett, 2010, 10: 1917–1921
52 Castro E V, Novoselov K S, Morozov S V, et al. Biased bilayer graphene-semiconductor with a gap tunable by the electric field effect. Phys Rev Lett, 2007, 99: 216802
53 Zhang Y B, Tang T T, Girit C, et al. Direct observation of a widely tunable bandgap in bilayer graphene. Nature, 2009, 459: 820–823
54 Xia F N, Farmer D B, Lin Y M, et al. Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. Nano Lett, 2010, 10: 715–718
55 Zhou S Y, Gweon G H, Fedorov A V, et al. Substrate-induced bandgap opening in epitaxial graphene. Nat Mater, 2007, 6: 770–775
56 Balog R, Jørgensen B, Nilsson L, et al. Bandgap opening in graphene induced by patterned hydrogen adsorption. Nat Mater, 2010, 9: 315–319
57 Li S L, Miyazaki H, Hiura H, et al. Enhanced logic performance with semiconducting bilayer graphene channels. ACS Nano, 2011, 5: 500–506
58 Li S L, Miyazaki H, Lee M V, et al. Complementary-like graphene logic gates controlled by electrostatic doping. Small, 2011, 7: 1552–1556
59 Sze S M. Physics of Semiconductor Devices. New York: Wiley, 1981
60 Schaller R R. Moore's law: Past, present and future. IEEE Spectrum, 1997, 34: 52–59
61 International Technology Roadmap for Semiconductors, 2009 ed. http://public.itrs.net/
62 Lu Y R, Bangsaruntip S, Wang X R, et al. DNA functionalization of carbon nanotubes for ultrathin atomic layer deposition of high κ dielectrics for nanotube transistors with 60 mv/decade switching. J Am Chem Soc, 2006, 128: 3518–3519
63 Wang X R, Tabakman S M, Dai H J. Atomic layer deposition of metal oxides on pristine and functionalized graphene. J Am Chem Soc, 2008, 130: 8152–8153
64 Farmer D B, Gordon R G. Atomic layer deposition on suspended single-walled carbon nanotubes via gas-phase noncovalent functionalization. Nano Lett, 2006, 6: 699–703

65 Chen Z H, Farmer D B, Xu S, et al. Externally assembled gate-all-around carbon nanotube field-effect transistor. IEEE Electron Device Lett, 2008, 29: 183–185
66 Williams J R, DiCarlo L, Marcus C M. Quantum hall effect in a gate-controlled p-n junction of graphene. Science, 2007, 317: 638–641
67 Lin Y M, Jenkins K A, Valdes-Garcia A, et al. Operation of graphene transistors at gigahertz frequencies. Nano Lett, 2009, 9: 422–426
68 Farmer D B, Chiu H Y, Lin Y M, et al. Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors. Nano Lett, 2009, 9: 4474–4478
69 Lin Y M, Dimitrakopoulos C, Jenkins K A, et al. 100-GHz transistors from wafer-scale epitaxial graphene. Science, 2010, 327: 662
70 Lee B, Park S Y, Kim H C. Conformal Al_2O_3 dielectric layer deposited by atomic layer deposition for graphene-based nanoelectronics. Appl Phys Lett, 2008, 92: 203102
71 Kim S Y, Nah J H, Jo I, et al. Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric. Appl Phys Lett, 2009, 94: 062107
72 Wu Y Q, Lin Y M, Bol A A, et al. High-frequency, scaled graphene transistors on diamond-like carbon. Nature, 2011, 472: 74–78
73 Lee G S, Lee B K, Kim J Y, et al. Ozone adsorption on graphene: Ab initio study and experimental validation. J Phys Chem C, 2009, 113: 14225–14229
74 Xu H L, Zhang Z Y, Wang Z X, et al. Quantum capacitance limited vertical scaling of graphene field-effect transistor. ACS Nano, 2011, 5: 2340–2347
75 Xu H L, Zhang Z Y, Peng L M. Measurements and microscopic model of quantum capacitance in graphene. Appl Phys Lett, 2011, 98: 133122
76 Xu H L, Zhang Z Y, Xu H T, et al. Top-gated graphene FETs with high normalized transconductance and designable dirac point voltage. ACS Nano, 2011, 5: 5031–5037
77 Pozar D M. Microwave Engineering. 3rd ed. New York: Wiley, 2005
78 Xia F N, Perebeinos V, Lin Y M, et al. The origins and limits of metal-graphene junction resistance. Nat Nanotechnol, 2011, 6: 179–184
79 Bai J W, Liao L, Zhou H L, et al. Top-gated chemical vapor deposition grown graphene transistors with current saturation. Nano Lett, 2011, 11: 2555–2559
80 Rutherglen C, Jain D, Burke P. Nanotube electronics for radiofrequency applications. Nat Nanotechnol, 2009, 4: 811–819
81 Hwang E H, Das Sarma S. Acoustic phonon scattering limited carrier mobility in two-dimensional extrinsic graphene. Phys Rev B, 2008, 77: 115449
82 Chen J H, Jang C, Xiao S D, et al. Intrinsic and extrinsic performance limits of graphene devices on SiO_2. Nat Nanotechnol, 2008, 3: 206–209
83 Morozov S V, Novoselov K S, Katsnelson M I. Giant intrinsic carrier mobilities in graphene and its bilayer. Phys Rev Lett, 2008, 100: 016602
84 Meric I, Baklitskaya N, Kim P, et al. RF performance of top-gated, zero-bandgap graphene field-effect transistors. IEEE International Electron Devices Meeting, 2008. 1–4
85 Schwierz F, Liou J J. RF transistors: Recent developments and roadmap toward terahertz applications. Solid State Electron, 2007, 51, 1079–1091
86 Moon J S, Curtis D, Hu M, et al. Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates. IEEE Electron Device Lett, 2009, 30: 650–652
87 Lin Y M, Chiu H Y, Jenkins K A, et al. Dual-gate graphene FETs with f_T of 50 GHz. IEEE Electron Device Lett, 2010, 31: 68–70
88 Han S J, Jenkins K A, Valdes-Garcia A, et al. High-frequency graphene voltage amplifier. Nano Lett, 2011, 11: 3690–3693
89 Wang H, Nezich D, Kong J, et al. Graphene frequency multipliers. IEEE Electron Device Lett, 2009, 30: 547–549
90 Wang H, Hsu A, Kim K K, et al. Gigahertz ambipolar frequency multiplier based on CVD graphene. IEEE International Electron Devices Meeting, 2010, 23.6.1–23.6.4
91 Wang Z X, Ding L, Pei T, et al. Large signal operation of small band-gap carbon nanotube-based ambipolar transistor: A high-performance frequency doubler. Nano Lett, 2010, 10: 3648–3655
92 Durkop T, Getty S A, Cobas E, et al. Extraordinary mobility in semiconducting carbon nanotubes. Nano Lett, 2004, 4: 35–39
93 Baumgardner J E, Pesetski A A, Murduck J M, et al. Inherent linearity in carbon nanotube field-effect transistors. Appl Phys Lett, 2007, 91: 052107
94 Wang H, Hsu A, Wu J, et al. Graphen-based ambipolar RF mixers. IEEE Electron Device Lett, 2010, 31: 906–908
95 Yang X B, Liu G X, Balandin A A, et al. Triple-mode single-transistor graphene amplifier and its applications. ACS Nano, 2010, 4: 5532–5538
96 Yang X B, Liu G X, Rostami M, et al. Graphene ambipolar multiplier phase detector. IEEE Electron Device Lett, 2011, 32: 1328–1330