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Research Article

Hall Effect Devices with Three Terminals: Their Magnetic Sensitivity and Offset Cancellation Scheme

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This paper discusses properties of Hall effect sensors with only three terminals and compares them to conventional four-terminal devices. It covers both Horizontal and Vertical Hall effect devices. Their Hall-geometry factor is computed analytically. Several modes of operation are proposed and their signal-to-noise ratio is compared. A six-phase offset cancellation scheme is developed. All theoretical results are checked by measurements. The residual offset of Vertical Hall effect devices with three contacts is found to be smaller than the offset of conventional Vertical Hall effect devices with five contacts.

1. Introduction

Traditionally, Hall plates have four contacts and two orthogonal planes of mirror symmetry: two opposite contacts are used to supply the device with electrical energy while the other two opposite contacts are used to tap the output signal. The Hall plate can be supplied by a voltage or a current source and the output signal can be sensed by a voltmeter or an amperemeter. The combination of these possibilities gives four operating modes. For such devices spinning current schemes are known: they swap the two pairs of contacts—inputs and outputs—in consecutive operating phases. Combining the outputs of so-called orthogonal phases cancels out offset errors while keeping the magnetic sensitivity high. The output in each phase has a raw or initial offset, whereas the combination of phases according to the spinning scheme gives a much smaller offset, which is called residual offset. Offset error is stochastic so that one has to measure its standard deviation in order to quantify it. The standard deviation of a Gaussian distributed quantity is equal to its root mean square value, which we denote by rms. Moreover, if we compare different technologies and different types of devices, it is pretty meaningless to specify the offset in microvolts. Instead one should divide the output signal by the magnetic sensitivity in order to get the so-called equivalent offset in microtesla. In silicon technology the raw offset of state-of-the-art packaged Hall plates is roughly 7.5 mTrms and the residual offset of a good spinning current circuit may be as low as 15 μTrms. This is a drastic improvement of the offset error by a factor of 500. Thereby low residual offset is achieved only if either (i) constant current is forced during all spinning current phases into the device while voltage is tapped at the outputs or (ii) constant voltage is forced during all phases across the input terminals of the device while the short-circuit output current is sensed between the output terminals [1]. We call the latter procedure "spinning voltage scheme" to discriminate it against the first one, the "spinning current scheme." If we refer to both schemes, we simply say "spinning scheme" or "dynamic offset cancellation." So it is commonly believed that (i) the current needs to spin around in space during this dynamic offset cancellation procedure, that (ii) both input and output terminals need to be swapped in order to get best suppression of offset errors, and that (iii) the Hall plate must have 90° symmetry for the spinning scheme to work. However, none of these requirements is obligatory, as we will see in the sequel.

With the advent of Vertical Hall effect devices the spatial spinning of current during the "spinning" scheme became obsolete; however, up to now all published dynamic offset cancellation schemes still seem to work with exactly two inputs and two outputs, which are continuously swapped. We call Vertical Hall effect devices VHalls in contrast to Hall plates, which we also call Horizontal Hall effect devices or HHalls. The terms "horizontal" and "vertical" denote

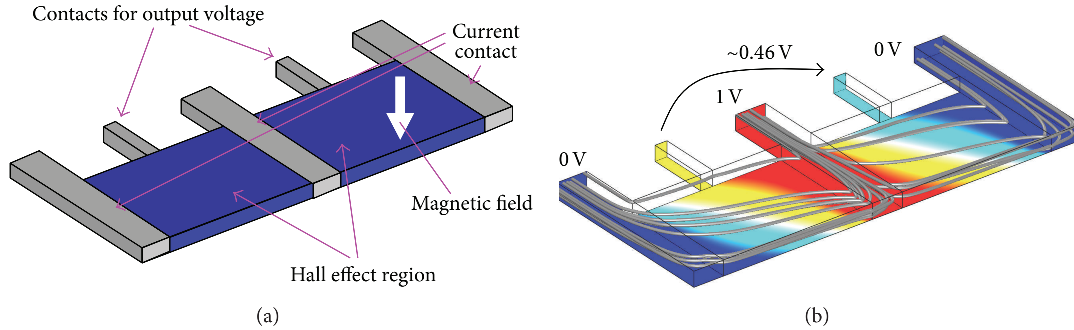

FIGURE 1: A Hall plate with five contacts after [2]. The two small sense contacts are only on one single side of the Hall effect regions. (a) shows the geometry. (b) shows the potential and the current streamlines as obtained by a numerical calculation for a Hall angle of 45°. For small Hall angle the current streamlines become parallel to the long edge of the device.

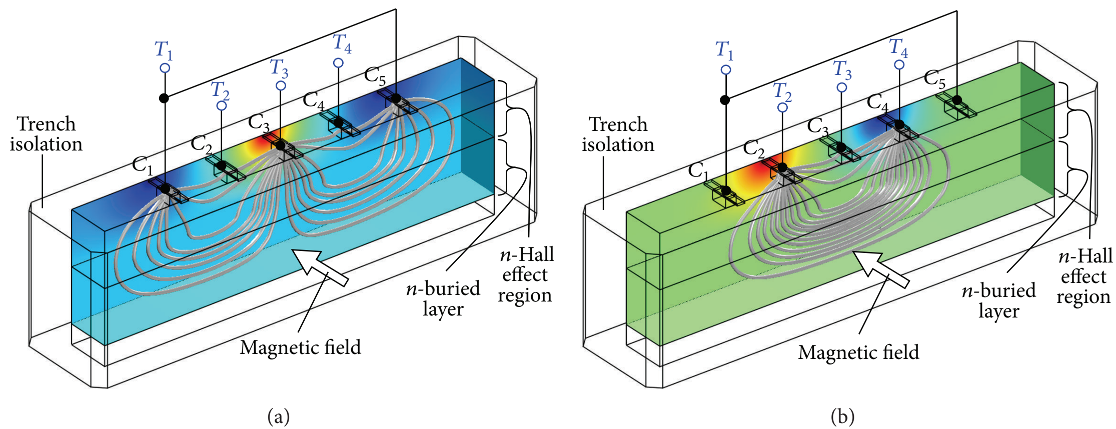

FIGURE 2: A Vertical Hall effect device with five contacts and four terminals in BiCMOS technology with deep trench isolation. The contacts comprise shallow n^+S/D-diffusions and slightly deeper nCMOS-wells. The bottom of the Hall effect region is shorted by a highly conductive n-buried layer at floating potential.

the orientation of the plate-like geometry of the devices with respect to the main surface of the semiconductor die. It is a misconception that VHalls need to have current flowing in vertical direction into the depth of the die. In fact the predecessors of VHalls with *output contacts* only on a single side of the device used a current purely parallel to that side [2] (Figure 1). Of course devices with *input contacts* on the top side of the Hall effect region need some vertical and some horizontal current flow. As a general rule, they tend to have the highest magnetic sensitivity when the share of vertical to horizontal current flow is about 50%.

We specify the number of contact diffusions per Hall effect region: for example, the well known original VHall device of [3] is termed 5C-VHall (see Figure 2). It has five contact diffusions in the Hall effect region, which we label $C_1, C_2, \ldots, C_5$ from left to right. The outmost two of them (C_1 and C_5) are shorted, so that the device offers a total of four terminals T_1, T_2, T_3, T_4; therefore a more precise name for it is 5C-4T-VHall. Recently, a similar device was published, where the contacts C_2 and C_4 are shorted instead of C_1 and C_5, but the number of terminals is still four [4].

2. The Role of Symmetry

Obviously, the degree of symmetry in VHalls is smaller than that in HHalls, because the accessible contacts of VHalls are only on the top face of the Hall effect region, whereas the contacts of HHalls can be arranged symmetrically along the entire perimeter of the Hall plate. Thus, there must be two outmost contacts as long as the Hall effect region has the shape of a straight tub, and these outmost contacts break the symmetry. This might also contribute to the roughly ten times larger equivalent residual offset error of VHalls compared to HHalls. So several people have tried to improve the symmetry. Here we name just a few:

(1) One may apply the principle of forced symmetrization as it is used by HHalls since the 1980s: instead of a single device with four terminals one uses four devices and connects each terminal to a different contact of a different device as shown in Figure 3 [5].

No matter how asymmetric a single device was, the complete network of four devices is symmetric in

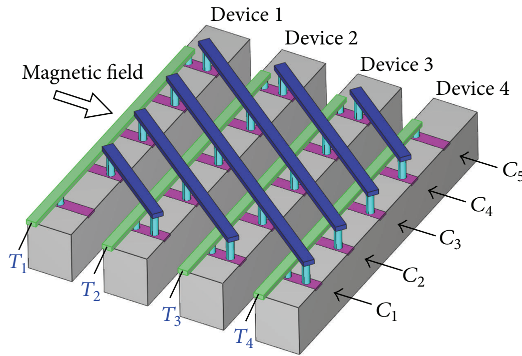

Figure 3: Four 5C-VHalls connected in a forced symmetrization pattern.

an electric sense: the resistance between terminals $T_1 \rightarrow T_2$ is equal to the resistance between terminals $T_2 \rightarrow T_3$, or $T_3 \rightarrow T_4$, or $T_4 \rightarrow T_1$ and the output signal between $T_1 \rightarrow T_3$ is equal to the output signal between $T_2 \rightarrow T_4$. For traditional Hall plates this was used to average out systematic offset errors caused by mask misalignment or mechanical stress. In VHalls it averages out junction field effects and charge modulation effects, too. Such a kind of symmetrization facilitates the task for the Hall biasing and signal conditioning circuits, yet it does not solve the problem for each single device: it is still asymmetric and the forced symmetrization circuit only adjusts the amount of current through it to counterbalance its asymmetry.

(2) One can avoid the two ends of the Hall tub by using a ring-shaped Hall effect region with eight or more contacts [6]. Not all of these contacts are used simultaneously: in [7] one uses five consecutive contacts during a first phase like in the 5C-VHall device, and during subsequent operating phases the group of five contacts is shifted (counter)clockwise. In some technologies like those with deep trench isolation it is not possible to make ring-shaped Hall effect regions, because the boundaries of the trenches must be parallel to the edges of the die. Moreover the large number of MOS-switches needed to route current through so many contacts requires considerable chip space. Besides, there is no theoretical proof yet that the spinning principles applied to these structures cancel out offset in a strict sense: with each new phase at least one further MOS-switch adds its on-resistance to the residual offset. The reported offsets achieved in practice may result simply from the statistical average of the large number of partial devices used.

(3) Another strategy is to use several disjunct Hall tubs and connect them with wires in a ring topology like in Figure 4 [8, 9]. This arrangement is perfectly symmetric; however, the price we pay is that the voltage drop in these two tubs, which have the supply terminals, does not contribute to the Hall effect. So the power efficiency of the device is suboptimal. However, one may connect a large number of devices in a ring circuit. Then the percentage of the two devices with supply contacts is small and the efficiency of the device is higher; however a complete spinning scheme over all devices takes longer and this limits the bandwidth. The residual offset is low because the voltage per device (and thus the nonlinearity caused by the electric field) is low and the large number of devices results in better statistical averaging. The magnetic sensitivity is low, but the SNR is high.

In fact, electrical symmetry is not the main problem for spinning schemes. Even if a four-terminal device would lack any kind of electrical symmetry the spinning scheme would cancel out the offset error perfectly well, as long as the device has linear electrical properties and if we disregard thermoelectric effects [1]. Electrical linearity means that its equivalent resistor circuit is made up of resistors with fixed values which do not depend on applied potential. In practice the active Hall effect region is isolated against its surroundings by reverse biased pn-junctions, whose depletion region widths depend on the potentials, and this voltage dependence changes the shape of the Hall effect region depending on the applied potentials finally leading to electrical nonlinearity. Even if the side-walls of the Hall tub are isolated by trench isolation with thin dielectric layers charge modulation along the perimeter of the Hall effect region will be caused by varying potentials analogous to the channel region of PMOS transistor. Moreover, for small devices the electric field exceeds 100 kV/m which gives rise to velocity saturation in low doped n-type silicon, and this is another source of electrical nonlinearity. For HHalls this is no problem, since one can scale the lateral size of the device until the electric field is low enough. For VHalls one cannot scale the thickness into the depth of the substrate; it is given by the technology: for BiCMOS technologies one may use the epitaxial layer with a thickness around 5 μm, for HV-CMOS technologies one may use a CMOS well of a high-voltage transistor with around 3 μm thickness, and for plain CMOS one has to cope with the logic CMOS n-well of only 1.5 μm thickness. The size and spacing of the contacts on the surface of the Hall tub relate to the thickness of the tub: if the thickness is small also the sizes of the contacts and their spacing need to be small in order to have a reasonably strong Hall output signal. In practice the size of the contacts as well as their minimum distance is limited by layout design rules of the specific technology. And smaller distances between contacts lead to larger electric field, which causes mobility degradation, electrical nonlinearity, and inhomogeneous temperature distribution in the Hall device. All these effects give large residual offset. This leads us to the idea that a device with a minimum number of contacts should have the least problems with contact size and spacing and therefore we hoped that devices with only three contacts may have advantages over traditional ones with more contacts.

It is known for a while that large contacts reduce the Hall output signal, because on the one hand the output contacts draw current away from the Hall effect region (current likes to

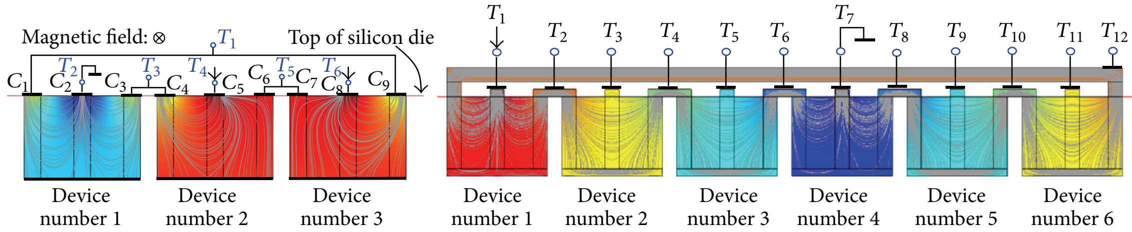

FIGURE 4: Examples of VHalls comprising several disjunct Hall tubs.

flow over the low ohmic contacts instead of flowing through the high ohmic Hall effect region) so that it is not available for the Hall effect any more, and on the other hand the input contacts short a part of the Hall electric field. For these reasons one is inclined to use as few contacts as possible, namely, three.

VHalls in BiCMOS technologies can benefit from the low n-doped epitaxial layer and its relatively large thickness. However, the bottom of the n-epi layer is not isolated by a p-doped region; instead there is a highly conductive n-buried layer, which acts like a contact at the bottom side of the Hall effect region (Figure 2). Yet, it is difficult to connect this n-buried layer contact to a terminal. So it is a floating contact that shorts some portion of the Hall output signal but which cannot be tapped by the circuit to use it as an output signal. In other words, such a device may have, for example, three diffusion contacts at the top of the Hall effect region plus one floating contact at the bottom of the Hall effect region. Obviously, one is trying to reduce the number of additional contacts on the top surface in order to keep the electric field reasonably low. This was the motivation that led us to a closer investigation into Hall effect devices with only three terminals.

In the following we start with Hall plates having only three contacts, derive their equivalent circuit diagram, and discuss various operating modes and their signal-to-noise ratios (SNR). Then we derive a linear theory on spinning schemes for Hall effect devices with three contacts. In the measurement sections we check our theories with 3C-HHall and 3C-VHall and compare them to 4C-HHalls and 5C-VHalls.

3. Magnetic Sensitivity in Various Operating Modes

Figure 5 shows 3C-HHall, 3C-VHall, and their equivalent resistor network at vanishing magnetic field. The 3C-HHall has a 120° symmetry so that it does not change its shape when rotated by ±120°. Therefore the resistors $R_1 = R_2 = R_3$ are nominally equal for the 3C-HHall. Conversely, the 3C-VHall has only mirror symmetry with respect to its center contact C_2, so that the resistors $R_1 = R_2 < R_3$. The shapes of Hall effect regions for the devices in Figure 5 are merely examples; particularly for VHalls there is a large variety of possible geometries: with or without buried layers, all contacts in a row or not, and several disjunct Hall effect regions connected in a ring circuit or not. In the following we discuss the magnetic sensitivity of devices with one or two Hall effect regions.

If current flows between two supply contacts, the potential at the third sense contact depends on the symmetry: in the symmetric case it is close to half of the supply voltage at zero magnetic field; in the asymmetric case it is somewhat closer to that supply potential, whose contact is nearer. When a magnetic field is applied perpendicularly to the plate the potential at the third contact rises or decreases, depending on whether the contact is left or right to the current streamlines. This holds also for asymmetric operation: for example, if current flows from left to center contact of the VHall in Figure 5 the right contact is to the right of the current flow and so its potential decreases when magnetic field pointing out of the drawing plane is applied. With this simple rule, one can figure out easily the sign of the Hall output signals for unconventional Hall effect devices.

Figures 6(a)–6(e) show various modes of operation of a 3C-device. For the sake of simplicity, we choose a symmetric device, but the same principles apply to asymmetric HHalls or VHalls. First we discuss how these devices can be biased and how one can extract an output signal. The underlying motivation is to find one arrangement with optimum magnetic sensitivity, minimum noise, and maximum power efficiency.

Figure 6(a) shows a differential operation, where two devices are supplied with currents flowing through their first two contacts whereby the output signal is tapped between their third contacts. One device has its sense contact to the left hand side of the current path while the other one has its sense contact to the right of the current path. Therefore, the potential on the sense contact of one device rises while it falls on the sense contact of the other device. The output voltage is tapped between the sense contacts of both devices. Each of the two devices has two supply contacts and a single sense contact.

A numerical simulation assumed a conductivity tensor $\underline{\underline{\sigma}} = \sigma_0 \begin{pmatrix} 1 & -\mu_H B_z \\ \mu_H B_z & 1 \end{pmatrix}$ with $\sigma_0 = 62.5\,\mathrm{S/m}$ and a Hall-mobility of $\mu_H = 0.13038\,\mathrm{T}^{-1}$. The Hall effect region is derived from an equilateral triangle with 40 μm long edges, where the corners are cut off by circles with 10 μm radius and the resulting curved boundaries are used as contacts. The thickness of the plate was $t_H = 1\,\mu$m. A current of $I_{in}^{(a)}/2 = 40.1\,\mu$A was injected into contact C_2 of each device. This gave a potential of $V_{in}^{(a)} = 1.0$ V on C_2. At zero magnetic field the potential at C_3 is exactly half of this value and it rises by 1.66 mV if a magnetic field of $B_z = 50$ mT is applied to the left device. So

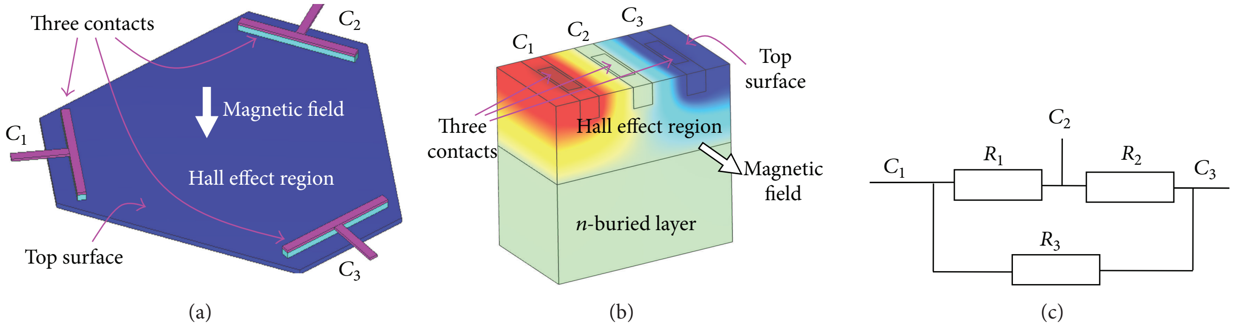

FIGURE 5: A symmetrical 3C-HHall device (a), an asymmetrical 3C-VHall device (b), and an equivalent circuit diagram for general 3C-Hall devices (c).

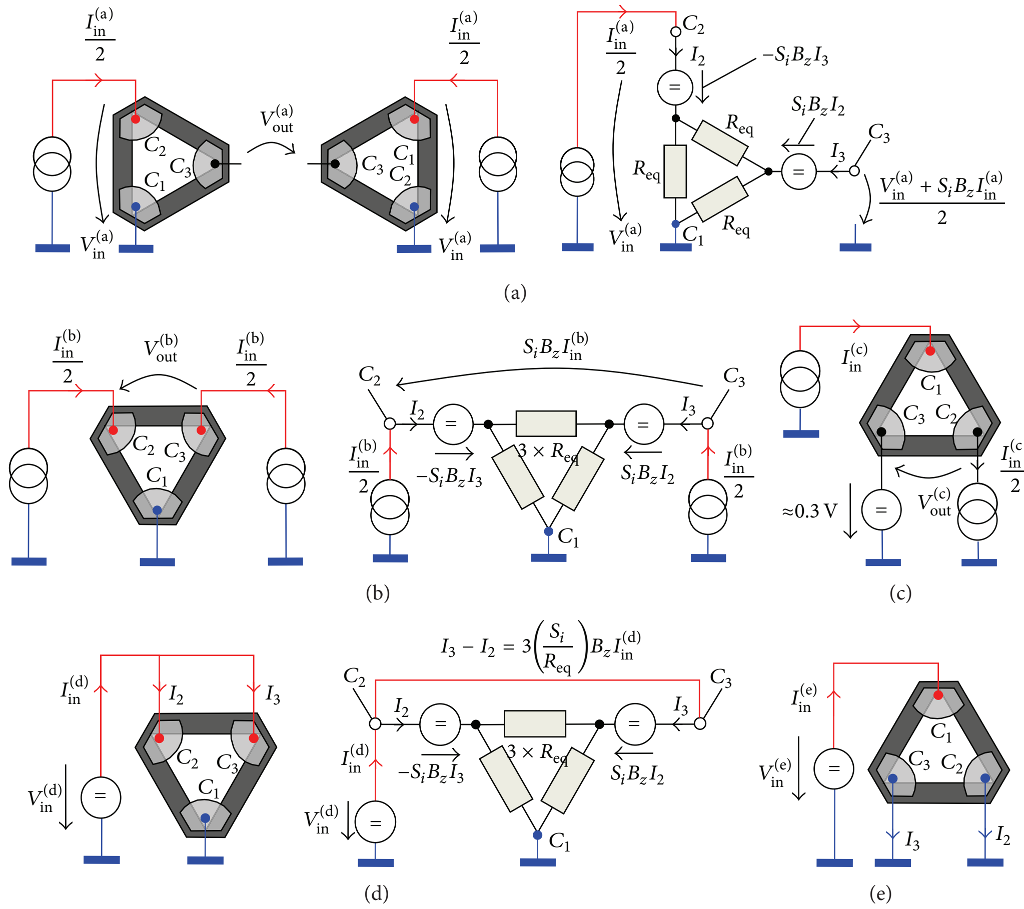

FIGURE 6: Differential operating mode (a) and equivalent circuit model of its left half. (b) Operating mode (b) and equivalent circuit model. (c) Operating mode (c) has inverted current flow polarities of operating mode (b). (d) Operating mode (d) and its equivalent circuit diagram. (e) Operating mode (e) has inverted polarity of supply current from operating mode (d).

the input resistance of the complete device is $R_{\text{in}}^{(a)} = V_{\text{in}}^{(a)}/I_{\text{in}}^{(a)} = 12457.2\,\Omega$. The sheet resistance is $R_S = 1/(t_H\sigma_0) = 16000\,\Omega$ and this gives the effective number of squares $(L/W)_{\text{in}}^{(a)} = R_{\text{in}}^{(a)}/R_S = 0.779$. The output voltage is given by $V_{\text{out}}^{(a)} = S_i B_z I_{\text{in}}^{(a)}$ with the current related magnetic sensitivity

$$S_i = \frac{1}{2}\frac{\mu_H}{\sigma_0}\frac{G_{H0}^{(3C)}}{t_H}, \tag{1}$$

whereby $G_{H0}^{(3C)}$ is the Hall-geometry factor at low magnetic field and factor 1/2 accounts for the fact that the 3C-Hall has only a single output terminal. By splitting apart factors 1/2 and $G_{H0}^{(3C)}$ we make sure that the Hall-geometry factor $G_{H0}^{(3C)}$ accounts only for the short circuiting effects of contacts of finite size; if all contacts become point-sized it holds that $G_{H0}^{(3C)} \to 1$ just like it was originally defined with traditional four-contact Hall plates [10]. A strict derivation of (1) is given in Appendix A.

For the device in Figure 6(a) we get $G_{H0}^{(3C)} = 0.79228$ which gives $S_i = 826.4\,\mathrm{V/A/T}$. The voltage related magnetic sensitivity is defined as $S_u^{(a)} = V_{out}^{(a)}/(B_z V_{in}^{(a)}) = S_i/R_{in}^{(a)}$. For the device in Figure 6(a) we get $S_u^{(a)} = 0.0663\,\mathrm{V/V/T}$. The value for $S_u^{(a)}$ is even 8% larger than the maximum S_u for conventional 4C-HHalls with 90° symmetry, which is $\max S_u^{(4C)} = \mu_H\sqrt{2}/3 = 0.0615\,\mathrm{V/V/T}$ [11]. With Appendix C one finds $\max S_u^{(a)} \cong 0.539\times\mu_H$ for 3C-Halls with 120° symmetry, which is 1.14 times larger than $\max S_u^{(4C)}$.

However, magnetic sensitivity is less important than signal-to-noise ratio, which we derive next. The equivalent resistor network in Figure 6(a) gives $R_{in}^{(a)} = R_{eq}/3$ and $R_{out}^{(a)} = 4R_{eq}/3$, so the output resistance is four times the input resistance. The numbers are $R_{out}^{(a)} = 49828.8\,\Omega$ and $R_{eq} = 37371.6\,\Omega$. The output number of squares is defined as $(L/W)_{out}^{(a)} = R_{out}^{(a)}/R_S$. From the equivalent circuit it follows that $(L/W)_{out}^{(a)} = 4(L/W)_{in}^{(a)}$. Thus, the thermal noise at the output is $V_n^{(a)} = \sqrt{4k_bTR_S(L/W)_{out}^{(a)}\Delta f}$ with Boltzmann's constant k_b, the absolute temperature T, and the effective noise bandwidth Δf. $1/f$-noise is irrelevant, because it is chopped out by the spinning scheme [12]. But in practice the Hall effect device should be optimized to have maximum signal-to-noise ratio, SNR, but at the same time neither the current drain nor the necessary input voltage should be too large. So we do not want to maximize SNR/I_{in} or SNR/V_{in}, but we need maximum SNR while keeping R_{in} constant. In fact at the start of a new sensor system development the circuit design engineers choose the impedance level R_{in} at which they want the circuit to operate, because this defines the current drain and the size of the noise critical transistors of the signal conditioning circuits. To this end we express the signal-to-noise ratio in operating mode (a) in the following way:

$$\mathrm{SNR}^{(a)} = \frac{1}{2}\frac{\mu_H B_z}{\sqrt{4k_bT\Delta f}}\frac{G_{H0}^{(3C)}}{\sqrt{(L/W)_{in}^{(a)}\,(L/W)_{out}^{(a)}}}\frac{V_{in}^{(a)}}{\sqrt{R_{in}^{(a)}}} \tag{2}$$

from which it is evident that we need to maximize the Hall-mobility and the term $G_{H0}^{(3C)}/\sqrt{(L/W)_{in}^{(a)}(L/W)_{out}^{(a)}}$, which depends only on the lateral geometry of the device. The same result is obtained if we maximize the SNR over the square-root of the power dissipated in the Hall effect device $\mathrm{SNR}^{(a)}/\sqrt{V_{in}^{(a)}I_{in}^{(a)}} = \mu_H B_z G_{H0}^{(3C)}/\sqrt{4k_bT(L/W)_{in}^{(a)}(L/W)_{out}^{(a)}\Delta f}$. In practice, saving power in a Hall effect device pays only, if the input resistance of the device is such that the total available supply voltage drops over the device and not over a pass transistor in its bias circuit, and this brings us back to the intuition of the circuit design engineer who chooses the optimum impedance level at the start of the circuit design.

For the device in Figure 6(a) we get $G_{H0}^{(3C)}/\sqrt{(L/W)_{in}^{(a)}(L/W)_{out}^{(a)}} = 0.509$. How does it relate to conventional 4C-Hall plates? Appendix B shows that they have a maximum $G_{H0}^{(4C)}/\sqrt{(L/W)_{in}^{(4C)}(L/W)_{out}^{(4C)}} \le \sqrt{2}/3 = 0.471$, which is achieved for $(L/W)_{in}^{(4C)} = (L/W)_{out}^{(4C)} = \sqrt{2}$. However, in the SNR of the 3C-Hall effect device (in (2)) we had to add the extra factor 1/2, so that the SNR of the device in Figure 6(a) is 0.471/(0.509/2) = 1.85 times smaller than the optimum SNR of 4C-Hall. In Appendix C we investigate the SNR of the symmetrical 3C-Hall for various contact sizes and there we will see that even for optimum symmetrical 3C-Halls the $\mathrm{SNR}^{(a)}$ is ~1.75 times smaller than the SNR for optimum 4C-Halls (under the boundary condition of equal input resistance, see (C.1)). So this is bad news for symmetrical 3C-HHalls and 3C-VHalls in operating mode (a): at the same input resistance they have ~1.75 times smaller SNR; for the same SNR we need to spend ~3.06 times more current. However, in the case of single tub 4C-VHalls it seems impossible to achieve an optimum device, which can be mapped by a conformal transformation onto a 180°-symmetrical 4C-HHall and therefore the single tub 3C-VHalls may still be a viable compromise.

Figure 6(a) also shows an equivalent circuit diagram for the 3C-HHall, which models the output signal at small magnetic field. It holds if the third contact is grounded and it accounts for the symmetry between contacts C_2 and C_3. In the following we show that it may also be used to describe the output signals in other operating modes.

Figure 6(b) shows an operation of a single device, where equal currents are injected into contacts C_2 and C_3, while the third contact C_1 is at ground potential. The output voltage is tapped between the two current input contacts. In this case all three contacts of the device are supply contacts, whereby the two current input contacts also act as sense contacts.

With the parameters from above a numerical simulation gives a voltage difference of $V_{out}^{(b)} = 2.21\,\mathrm{mV}$ at currents of $I_{in}^{(b)}/2 = 53.5\,\mu\mathrm{A}$ in both contacts C_2, C_3, and at Bz = 50 mT. At zero magnetic field the potential at contacts C_2 and C_3 is 1.0 V. Thus, the voltage related magnetic sensitivity is $S_u^{(b)} = 44.2\,\mathrm{mV/V/T}$, which is 1.5 times smaller than $S_u^{(a)}$ in Figure 6(a). The equivalent circuit diagram gives $V_{out}^{(b)} = S_iB_zI_{in}^{(b)}$ which agrees with this result of the numerical simulation. The input resistance $R_{in}^{(b)} = R_{eq}/2$ is 1.5 times larger than that in Figure 6(a). The output resistance $R_{out}^{(b)} = 2R_{eq}/3$ is only half of the output resistance of Figure 6(a). Hence, according to (2) for equal devices at constant supply voltage the SNR of Figure 6(b) is reduced by factor $\sqrt{2}/(3/2) \cong 0.943$ compared to Figure 6(a). However, the supply current is also reduced by factor 1.5 so that the SNR/I_{in} in Figure 6(b) is $\sqrt{2} \cong 1.414$ times larger than that in Figure 6(a). And what is the maximum SNR of Figure 6(b) for a given input resistance? To this end we increase the thickness of the device in operating mode (b) 1.5 times. Then the input resistance of the original thin device in operating mode (a) is equal to the input resistance of the new thick device in operating mode (b). The change of the thickness has no effect on $G_{H0}^{(3C)}/\sqrt{(L/W)_{in}^{(b)}(L/W)_{out}^{(b)}}$, but it decreases the input resistance of mode (b) 1.5 times and so it increases its SNR by $\sqrt{3/2}$. Thus, the SNR of the thick device in mode (b) is factor $\sqrt{2}/\sqrt{3/2} = 2/\sqrt{3} \cong 1.155$ times larger than the SNR

of the thin device in mode (a) with identical input resistance. In other words

$$\max \mathrm{SNR}^{(b)} = \left(\frac{2}{\sqrt{3}}\right) \max \mathrm{SNR}^{(a)} \quad \text{for equal input resistance } R_{in}^{(a)} = R_{in}^{(b)}. \tag{3}$$

Hence, for a given input voltage and for a given input resistance the operating mode (b) can achieve 15.5% higher SNR than operating mode (a). Compared to optimum 4C-HHalls with $(L/W)_{in}^{(4C)} = (L/W)_{out}^{(4C)} = \sqrt{2}$ the maximum SNR of Figure 6(b) at equal input resistance is still ~1.51 times smaller (see Appendices B and C, (B.2), and (C.2)). To make up for this, one has to reduce the input resistance 2.28 times and this increases the current drain by the same factor.

Figure 6(c) shows a current polarity inversion of the operation of Figure 6(b), where current is forced to flow out of two contacts at low potential while the third contact is at high potential.

Figure 6(d) shows the same device being supplied with identical potential at two contacts C_2 and C_3, while the third one is at ground potential. For $V_{in}^{(d)} = 1\,\mathrm{V}$ the numerical simulation gives $I_3 - I_2 = 0.177\,\mu\mathrm{A}$ at Bz = 50 mT. Here the output signal is the difference in currents flowing into both C_2 and C_3. The sum of both currents is $I_{in}^{(d)} = 53.52\,\mu\mathrm{A}$. With the equivalent circuit diagram in Figure 6(d) we obtain $I_3^{(d)} - I_2^{(d)} = 6V_{in}^{(d)} S_i B_z/(R_{eq}^2 + S_i^2 B_z^2) \cong 3I_{in}^{(d)} S_i B_z/R_{eq}$ which matches the result of the numerical simulation. Current consumption and input and output resistance are identical to Figure 6(b). Figure 6(e) shows the polarity inversion of this operation, where the identical potentials at C_2 and C_3 are lower than the supply potential.

4. Iv-Biasing Six-Phase Offset Cancellation Scheme

In this section we discuss an offset cancellation scheme for 3C-Halls: Iv-biasing. Thereby, the device is supplied with *the same input current* in six operating phases and the output voltages of all phases are sensed and processed. For the sake of brevity we explain the principle with asymmetric 3C-VHalls. Obviously, the same procedure may be applied to symmetrical devices and to HHalls, too. In Figures 7(a)–7(f) the left ones show a physical cross section of the device and the circuit parts connected to the device, whereas the right figures show simplified linearized equivalent circuit diagrams to estimate the output signals at zero magnetic field. If a label "+B" is written to a contact this means that the signal at this contact increases with increasing magnetic field whereas "−B" means that it decreases with increasing magnetic field. The magnetic field is supposed to point outside of the drawing plane. In the equivalent circuit diagram R_1 is roughly equal to R_2 due to the symmetry of the device, yet due to tolerances, mechanical stress, and electric nonlinearity of the device there is a mismatch between R_1 and R_2 in the order of $0.1\% \cdots 5\%$. The contacts are labeled 1, 2, and 3 from left to right. Operating phases are labeled $1, 2, \ldots, 6$.

The Iv-biasing scheme applies to the differential operating mode of Figure 6(a). All quantities of the right device are primed whereas the quantities of the left device are unprimed. Two operating phases are shown in Figures 7(a) and 7(b). In phase 1 currents are injected into the left contact of the left device and into the right contact of the right device so that $I_{in}^{(a)} = I_0 + I_0'$. Preferably both currents are identical, yet in practice one has to account for inevitable mismatches between I_0 and I_0'. The center contacts of both devices are grounded and the output voltage V_{ph1} is tapped between the right contact of the left device and the left contact of the right device. In the left device contact C_3 is at the right hand side of the current flow and so its potential decreases with growing magnetic field ("−B"). Conversely, in the right device contact $C_{1'}$ is at the left hand side of the current flow and so its potential increases with growing magnetic field ("+B"). Thereby it is irrelevant if the magnetic sensitivity of both devices is identical or not; only the sign counts, because eventually we aim at adding up all output voltages of all phases constructively in order to have a large overall magnetic sensitivity. We denote this by adding the term $S_1 B$ to the output voltage, whereby 1 denotes phase 1 and $S_1 B$ is supposed to be a positive number. The output signal of phase 1 is the sum of raw offset plus a magnetic field term:

$$V_{ph1} = \frac{I_0' R_1' R_2'}{R_1' + R_2' + R_3'} - \frac{I_0 R_1 R_2}{R_1 + R_2 + R_3} + S_1 B. \tag{4}$$

The raw offset is also called electric raw offset, because it is described by the equivalent electric circuit. This is in contrast to thermoelectric offset terms, which are also present in a real device and which are not described by the equivalent electric circuit. We will come back to thermoelectric offset later.

Figure 7(b) shows operating phase 3 where the roles of current input contacts and voltage output contacts are swapped, whereas the center contacts remain grounded. If the device is asymmetric, the magnetic sensitivity may be different. Therefore we add the positive term $S_3 B$ to the output voltage:

$$V_{ph3} = \frac{I_0 R_1 R_2}{R_1 + R_2 + R_3} - \frac{I_0' R_1' R_2'}{R_1' + R_2' + R_3'} + S_3 B. \tag{5}$$

If the magnetic field vanishes, the output voltages of phases 1 and 3 have equal magnitude but opposite sign! Consequently if we add them up the electric raw offsets of phases 1 and 3 cancel out while the magnetic sensitivities add up: $V_{ph1} + V_{ph3} = (S_1 + S_3)B$. We call these two phases *orthogonal* phases in analogy to conventional 4C-HHalls, where the electric raw offsets of two orthogonal current directions also cancel out. Note that the offset is canceled out even if I_0 and $I_{0'}$ are not equal! In practice, each terminal of the Hall devices is connected to MOS-switches, which have a small but nonnegligible on-resistance. In this case we have to add $R_{2'}^{ds,on} I_{0'} - R_2^{ds,on} I_0$ to V_{ph1}, which comes from the on-resistance of the switch that connects contacts C_2 and $C_{2'}$ to ground. However, the same switch is active in phase 3 and so its contribution is canceled out in the sum of $V_{ph1} + V_{ph3}$. The on-resistance of the switches at the current inputs and voltage outputs is irrelevant.

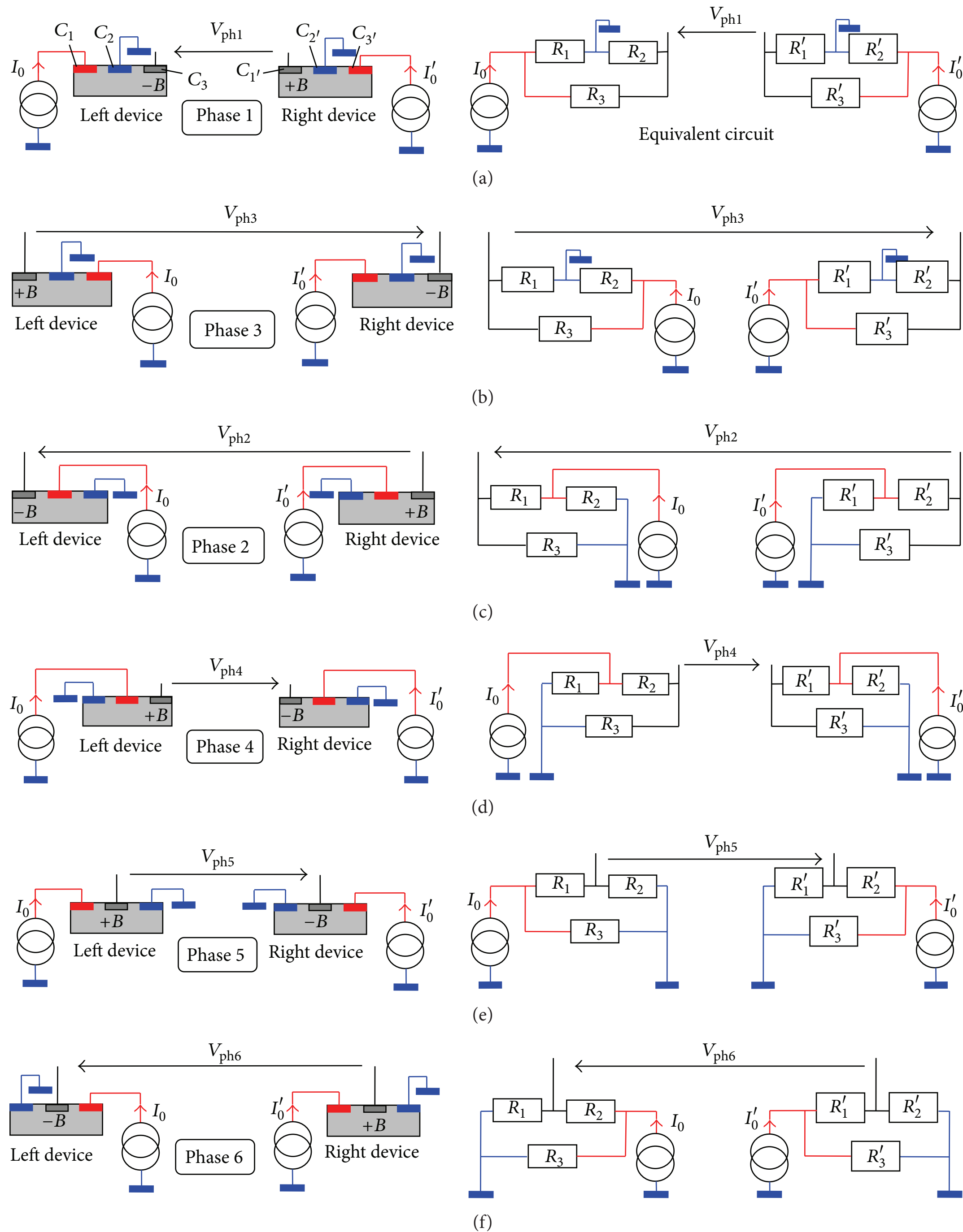

Figure 7: (a) Operating phase 1 of Iv-biasing scheme of differential operating mode according to Figure 6(a). (b) Operating phase 3 of Iv-biasing scheme of differential operating mode according to Figure 6(a). (c) Operating phase 2 of Iv-biasing scheme of differential operating mode according to Figure 6(a). (d) Operating phase 4 of Iv-biasing scheme of differential operating mode according to Figure 6(a). (e) Operating phase 5 of Iv-biasing scheme of differential operating mode according to Figure 6(a). (f) Operating phase 6 of Iv-biasing scheme of differential operating mode according to Figure 6(a).

Basically, the two phases 1 and 3 are enough to cancel out the offset, if the origins of offset were fully described by the equivalent circuit. However, in reality offset also comes from thermoelectric voltages: the output voltage is tapped at a contact, where the n-doped silicon region is in contact with the metal interconnect layer. This pair of different materials adds a small thermoelectric voltage, which depends on the temperature of the contact region and on the difference in Seebeck-coefficients of the involved material partners. Usually, these thermoelectric errors are cancelled out by reversing the polarity of the supply current: if the device is symmetric with respect to the supply current path

a polarity inversion does not change the temperature in the device and so it does not change the thermoelectric voltage at the contacts. However, it changes the sign of the magnetic sensitivity. Thus, if we subtract two output signals from phases with different polarity of supply current, we cancel out thermoelectric voltages and add up the magnetic sensitivities of both phases. Therefore, an efficient offset cancellation scheme must comprise pairs of phases with opposite polarity of supply current. We call the phases of such a pair *inverse* phases. Our phases 1 and 3 were orthogonal, yet they were not inverse! So, we look for additional operating phases, which are inverse to phases 1 and 3. Finally, the complete spinning scheme must consist of a number of phases, where each phase has exactly one orthogonal phase and where each phase has exactly one inverse phase.

Figure 7(c) shows phase 2, which is inverse to phase 3, because it merely reverses the polarity of the supply current. Moreover, Figure 7(d) shows phase 4, which is inverse to phase 1 due to its opposite supply current polarity:

$$V_{\mathrm{ph2}} = \frac{I_0' R_1' R_3'}{R_1' + R_2' + R_3'} - \frac{I_0 R_2 R_3}{R_1 + R_2 + R_3} + S_2 B,$$
$$V_{\mathrm{ph4}} = \frac{I_0 R_1 R_3}{R_1 + R_2 + R_3} - \frac{I_0' R_2' R_3'}{R_1' + R_2' + R_3'} + S_4 B. \quad (6)$$

Unfortunately, phases 2 and 4 are not orthogonal; their electric offsets do not cancel out, if we add the output signals $V_{\mathrm{ph2}} + V_{\mathrm{ph4}}$. So we have to find two phases, which are orthogonal to phases 2 and 4 and at the same time they must be inverse to each other, because phases 1 and 4 are an inverse pair and phases 2 and 3 are also an inverse pair. Phases 5 and 6 in Figures 7(e) and 7(f) fulfill all these requirements: Phase 5 is orthogonal to phase 2, phase 6 is orthogonal to phase 4, and phases 5 and 6 are inverse:

$$V_{\mathrm{ph5}} = \frac{I_0 R_2 R_3}{R_1 + R_2 + R_3} - \frac{I_0' R_1' R_3'}{R_1' + R_2' + R_3'} + S_5 B,$$
$$V_{\mathrm{ph6}} = \frac{I_0' R_2' R_3'}{R_1' + R_2' + R_3'} - \frac{I_0 R_1 R_3}{R_1 + R_2 + R_3} + S_6 B. \quad (7)$$

It holds that $V_{\mathrm{ph2}} + V_{\mathrm{ph5}} = (S_2 + S_5)B$ and $V_{\mathrm{ph4}} + V_{\mathrm{ph6}} = (S_4 + S_6)B$. So the complete spinning scheme uses all six possible combinations of current flow through the device:

$$V_{\mathrm{total}} = V_{\mathrm{ph1}} + V_{\mathrm{ph2}} + V_{\mathrm{ph3}} + V_{\mathrm{ph4}} + V_{\mathrm{ph5}} + V_{\mathrm{ph6}}$$
$$= (S_1 + S_2 + S_3 + S_4 + S_5 + S_6) B. \quad (8)$$

It cancels out electric offset errors and thermoelectric offset errors as long as the device is electrically linear. Electrical linearity means that the equivalent electric circuit consists of resistors, which are constant versus applied potentials. In practice, this is not the case: due to the junction field effect [13] and velocity saturation the resistance values in the equivalent circuit depend on the applied potentials roughly with 10%/V. This means that the resistance values change slightly in different operating phases of the spinning scheme and consequently the offset does not get canceled out perfectly. Moreover, due to this electrical nonlinearity of the device, the current density is increased near contacts at high potential and this leads to an inhomogeneous temperature distribution in the Hall device, which rotates synchronously with the spinning scheme. Therefore the scheme does not cancel out thermoelectric voltages perfectly, which adds another contribution to the so-called residual offset in the total output signal V_{total}.

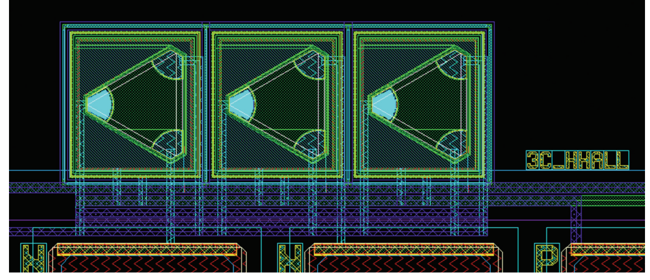

Figure 8: Layout of three devices of type 3C-HHall connected in parallel.

Obviously, the current does not spin around continuously in space like with conventional 4C-HHalls. So the term "spinning" is misleading and the term "contact commutation" is more correct. The essential feature is that each contact acts as positive supply terminal in two phases, as negative supply terminal in two phases, and as sense contact in two phases.

5. Measurement Results

5.1. 120° Symmetric 3C-HHalls. Figure 8 shows the layout of 3C-HHalls, whereby three devices were connected in parallel such that the current flow directions in the left device and in the right device are rotated by ±120° against the current flow direction in the center device. In practice this arrangement acts as a single device with three times larger plate thickness. In the following we treat this arrangement as a single device; for example, by internal resistance $R_{\mathrm{in}}^{(b)}$ we mean the resistance of all three devices in parallel operated in a mode according to Figure 6(b) and by internal resistance $R_{\mathrm{in}}^{(a)}$ we mean the total resistance of two such triples operated in a mode according to Figure 6(a). The doping concentration of the devices was very low: $2E15/\mathrm{cm}^3$ and the thickness was 0.7 μm. The length of the edges of each triangular device was 40 μm and the spacing of the contacts was 20 μm. The contacts had the shape of 60° sectors of circles with 10 μm radius, whereby the centers of the circles coincided with the corners of the triangle. Each device was isolated against its surroundings by a reverse biased pn-junction along the perimeter and at the bottom. At the top there was no pn-junction. Instead, a top metal plate was isolated against the Hall effect region by oxide layers and the top plate was grounded. All samples were made from 750 μm thick silicon chips, glued on small printed circuit boards, wire-bonded, and covered by transparent gel. Measurements were done in a darkened zero-Gauss chamber at room temperature.

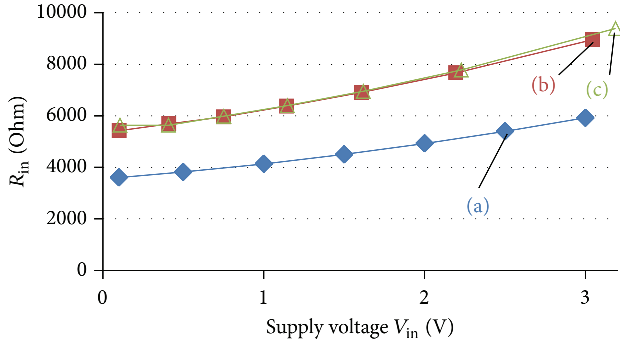

FIGURE 9: Input resistance of the 3C-HHalls of Figure 8 in operating modes (a), (b), and (c) of Figures 6(a), 6(b), and 6(c) measured at room temperature. V_{in} is averaged over all operating phases.

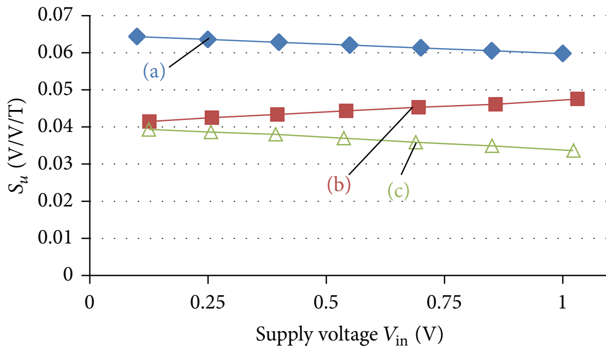

FIGURE 10: Voltage related magnetic sensitivity S_u of the 3C-HHalls of Figure 8 in operating modes (a), (b), and (c) of Figures 6(a), 6(b), and 6(c) measured at room temperature. V_{in} is averaged over all operating phases.

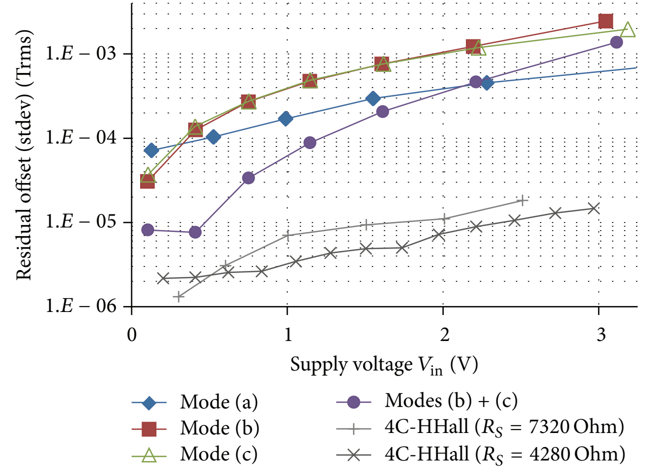

FIGURE 11: Residual offset of the 3C-HHalls of Figure 8 in operating modes (a), (b), and (c) of Figures 6(a), 6(b), and 6(c) measured at room temperature. V_{in} is averaged over all operating phases; "modes (b) + (c)" means that the signals of both operating phases (b) and (c) were summed up. The residual offset of two types of conventional Hall plates with four contacts (4C-HHall) and different sheet resistance R_S is also shown.

The internal resistance versus supply voltage was measured (see Figure 9). The marked nonlinearity of 13.4%/V comes from the junction field effect. The ratio of resistance is 1.505, which is in accordance with the theory of Section 3. This ratio is nearly constant with supply voltage.

The supply voltage related magnetic sensitivity is plotted versus supply voltage in Figure 10. At low supply voltages the ratio of sensitivities is 1.60; according to our theory it should be 1.50. The deviation is 6.7%. The slope versus input voltage is $\partial S_u^{(a)}/\partial V_{in}^{(a)} = -7.8\%/\text{V}$, $\partial S_u^{(b)}/\partial V_{in}^{(b)} = +15.9\%/\text{V}$, and $\partial S_u^{(c)}/\partial V_{in}^{(c)} = -15.9\%/\text{V}$.

The following offset cancellation schemes were investigated: in mode (a) the devices were operated like in Figure 6(a) and the six-phase Iv-biasing as described in the section Iv-biasing was used. When the devices were operated in mode (b) or mode (c) according to Figure 6(b) or Figure 6(c) the offset was cancelled out like this: the devices were operated in three consecutive phases such that output voltages were tapped between contacts C_1-C_2, C_2-C_3, and C_3-C_1; then both current sources were swapped and the three phases were repeated; finally all six output voltages were summed up. The label "modes (b) + (c)" means that the phase signals of both schemes (b) and (c) were added up.

Figure 11 shows measurement results of the residual offset which depends strongly on the supply voltage: at large supply voltage (~3 V) the self-heating as well as the electrical nonlinearity of the device gives a large equivalent residual offset of more than 1 mT. At small supply voltage residual offset below 100 μT is feasible. Modes (b) and (c) have 2⋯3 times larger offset than mode (a), except for very low supply voltage, where mode (a) has the largest offset. It seems to be a disadvantage for the 3C-HHall that in modes (b) and (c) the output contacts are at positive or negative supply rail. On the other hand, the combination "modes (b) + (c)" seems to cancel out a significant systematic offset error in individual modes (b) and (c) so that, finally, the combination "modes (b) + (c)" has a lower offset. Two types of conventional octagonal Hall plates with four contacts and 90° symmetry were also characterized. Their lateral size was 80 μm, and the thickness was 0.9 μm and 1.6 μm, respectively. The doping of the 4C-HHalls was roughly four times larger than the doping of the 3C-HHall. The internal resistance of the 4C-HHalls was 40% larger than their sheet resistance R_S They were operated in a conventional spinning current scheme comprising four phases, where constant current was forced through them and voltage was tapped at their output terminals. Figure 11 shows that the residual offset of these 4C-HHalls was 10⋯30 times smaller. Part of this difference can be explained by the larger doping level and thickness, but a major part seems to come from the lower thermoelectric symmetry of the 3C-HHall: modes (b) and (c) have no pairs of inverse phases and the combination "modes (b) + (c)" has pairs of inverse phases, yet at very different common mode potentials. Note that all devices in Figure 11 are single devices and the offset can be further reduced if a circuit takes the average over output signals of several devices according to the laws of statistics.

5.2. Asymmetric 3C-VHalls. Measurements were carried out on test structures shown in Figure 2. These are 5C-VHalls which we can also operate as 3C-VHalls, if we let the two outer contacts C_1, C_5 float; that is, we simply ignore terminal T_1. The devices are 41.5 μm long and 4.6 μm wide and the Hall effect regions extend 5.5 μm into the substrate. The contacts are 1.1 μm × 4.6 μm and they are spaced apart by 5 μm. The devices were made in BiCMOS technology with a highly conductive n-buried layer at the bottom of a VHall device. The Hall effect region had a doping of about $3E15/\text{cm}^3$, which is way smaller than the doping of the nCMOS-well ($2E17/\text{cm}^3$). The contacts were made of n^+S/D diffusion and nCMOS-well. Along the perimeter of the devices there is a deep trench at ground potential filled with polysilicon and isolated with a thin dielectric layer. The trench simultaneously patterns the Hall effect region and the buried layer. At the top of the device there is a grounded metal plate (not shown in Figure 2), which is isolated from the Hall effect region by oxide layers.

Operation as 5C-VHall Device. Since the 5C-VHall has only four terminals (contacts C_1 and C_5 are connected to the same terminal T_1 (cf. Figure 2)) it can be operated like a conventional 4C-HHall: current flows through the odd terminals and voltage is tapped at the even terminals and vice versa. At room temperature the input resistance at the odd terminals is 4 kOhm and at the even terminals it is 3 kOhm (both at small supply voltages). At larger supply voltages this resistance increases by 8.7%/V due to velocity saturation and charge modulation at the outer surfaces. At 2 V supply the resistance between the odd terminals changes by 4.7% if the polarity of the supply voltage is inverted, which is a clear sign of charge modulation at the trench walls. At small supply voltage the voltage related magnetic sensitivity is 39.5 mV/V/T at the odd terminals and 30.7 mV/V/T at the even terminals. It decreases by 6.3%/V at larger supply voltage. The ratio of input resistance between even and odd terminals is equal to the ratio of voltage related magnetic sensitivities at these terminals, because the current related magnetic sensitivity is the same for even and odd terminals, as was proven in [14]. A conventional spinning scheme of type "Iv-biasing" was carried out: constant current was forced and output voltage was sampled and added up over all four operating phases as described in [1]. Twenty samples were made from 750 μm thick silicon, attached to small printed circuit boards, wire-bonded, covered by transparent gel, and characterized in a darkened zero-Gauss chamber. Figure 12 plots the equivalent residual offset versus supply voltage. Additional test structures were characterized with devices of the same type connected in a forced symmetrization scheme according to Figure 3 and no notable improvement on residual offset was observed (beyond factor two, which is explained by the parallel connection of four devices).

Operation as 3C-VHall Device. The resistance between C_2 and C_4 was 3.8 kOhm. Between C_3 and one of its neighboring contacts (C_2 or C_4) it was 14% smaller. It increased by 10%/V with the supply voltage. In an operation according to Figure 6(a) the voltage related magnetic sensitivity at C_3 was 38 mV/V/T, at C_2 and C_4 it was 14% larger: 43 mV/V/T. We executed the Iv-biasing six-phase offset cancellation scheme and derived the residual offset for 13 samples (see Figure 13). So the spinning scheme basically works.

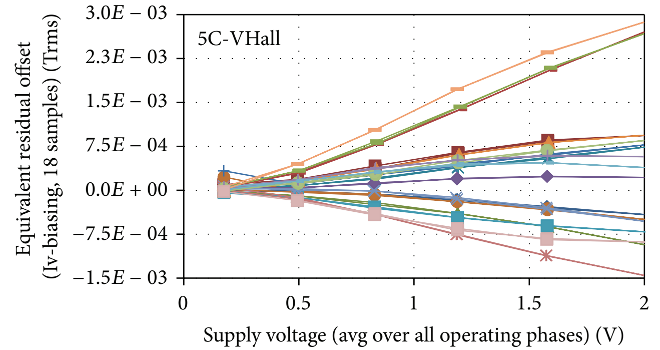

Figure 12: Measured residual offset of 5C-VHalls of Figure 2 operated in conventional spinning current scheme.

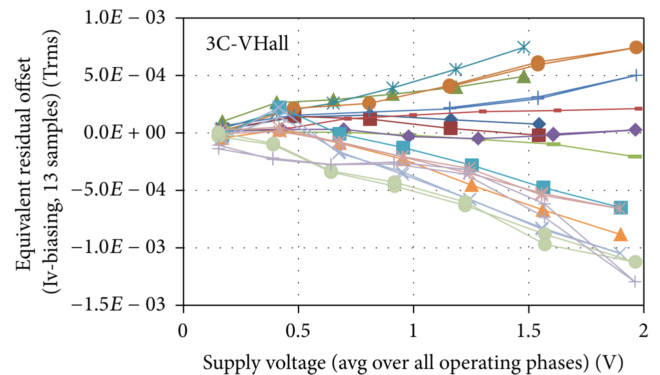

Figure 13: Measured residual offset of 3C-VHalls operated in Iv-biasing six-phase offset cancellation scheme. The devices were actually 5C-VHalls from Figure 2 with the outer contacts C_1, C_5 floating.

Comparison of Figures 12 and 13 shows a smaller offset for the 3C-VHall. This becomes more evident if we plot the standard deviation of both offsets versus supply voltage in Figure 14. For the 5C-VHall it is 200 μTrms at 0.5 V supply and 550 μTrms at 1 V supply. For the 3C-VHall it is 100 μTrms at 0.5 V and 260 μTrms at 1 V supply. So the measurement indicates that the residual offset of the 5C-VHall is twice the residual offset of the 3C-VHall. At 0.55 V supply the ultralow offset VHall in [9] has 50 μTrms offset, yet it is composed of 16 tubs, whereas the 3C-VHall in Figure 14 is only a single tub. A parallel connection of four 3C-VHalls of Figure 14 has the same internal resistance as the ultralow offset VHall in [9] and is expected to have the same offset, namely, 100/sqrt(4) = 50 μTrms. Factor 10 difference in offset errors reported between the ultralow offset VHall and the fully symmetrical VHall in Table 1 of [9] can be explained by the different number of devices (factor 2) and by the different supply voltage: according to Figure 14 the offset at a supply voltage of 2.44 V is roughly 7 times larger than that at 0.55 V. In [9] the doping concentration is higher and so factor 7 may well

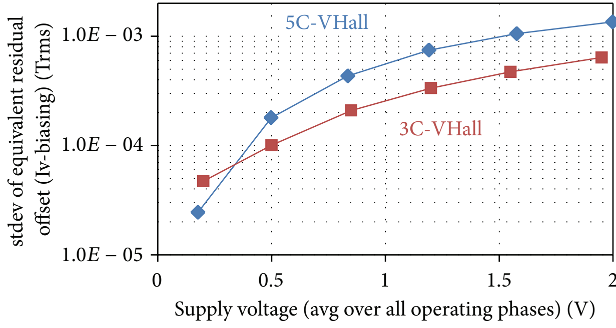

Figure 14: Standard deviation of the residual offsets of Figures 12 and 13.

reduce to a factor of 5. So it seems that both devices in [9] and our 3C-VHall in Figure 14 show similar residual offset errors at low supply voltage.

6. Conclusion

The paper discusses Hall plates (HHalls) and Vertical Hall effect devices (VHalls) with only three contacts. Various geometries with smaller or higher degree of symmetry were shown. Hall sensor devices with single tubs were shown as well as arrangements, where several tubs are connected into a ring circuit. Several operating modes of these devices were discussed and their signal-to-noise ratios were compared. Unfortunately, at given input resistance, the signal-to-noise ratio of 3C-Halls is generally smaller than the SNR of conventional 4C-Halls even though 3C-Halls achieve higher voltage related magnetic sensitivity. The equivalent circuit diagram of 3C-Hall comprises only three resistors and two current controlled voltage sources. Numerical simulations of several operating modes suggest that the equivalent circuit correctly predicts the output signals. An offset cancellation scheme for 3C-Halls was studied. The roles of orthogonal and inverse pairs of operating phases were elucidated. Measurement results on the residual offset of symmetric 3C-HHalls and asymmetric 3C-VHalls show that the offset cancellation schemes also work in practice. The residual offset of 3C-HHalls was found to be larger than that of conventional 4C-HHalls. However, the residual offset of 3C-VHalls was found to be smaller than that of conventional 5C-VHalls. A comparison with [9] indicates that, despite fairly different doping level, technology, layout, and wiring of tubs, in silicon single 3C-VHall devices have 100 μTrms residual offset error at 0.5 V supply.

In general it was found that unconventional devices like the ones with three contacts shed new light on topics like spinning current schemes and signal-to-noise ratio. Further studies of these devices are likely to bring more aspects to our attention, both in theory and in practice; this paper could touch only on the basic topics of unconventional Hall effect devices.

Appendix

A. Asymmetric 3C-Halls with Point-Sized Output Contact

Here we derive the input resistance and the Hall-geometry factor of a 3C-Hall with two arbitrarily large supply contacts and one point-sized sense contact. We apply the method of [14] to the device shown in Figure 15(a). It has the shape of a disc of radius 1 in the z-plane. One supply contact is at ground and it extends over azimuthal coordinates $\psi_1 - \theta_1 < \psi < \psi_1 + \theta_1$. The second supply contact is at potential V_{in} and it extends over azimuthal coordinates $-\psi_2 - \theta_2 < \psi < -\psi_2 + \theta_2$. The sense contact is assumed to be point-sized and located at $\psi = 0$. We transform this device onto a rectangle with the contacts at two opposite edges via a sequence of conformal transformations and then we apply the results of Section 2 of [14].

The bilinear transformation

$$w = \frac{a + bz}{1 + dz} \tag{A.1}$$

has three degrees of freedom a, b, and d which are chosen such as to map the following three pairs of points onto each other:

$$\begin{aligned} Z_1 &= \exp\left(i\left(\psi_1 - \theta_1\right)\right) \longrightarrow W_1 = -1, \\ Z_2 &= \exp\left(i\left(\psi_1 + \theta_1\right)\right) \longrightarrow W_2 = 0, \\ Z_3 &= \exp\left(-i\left(\psi_2 + \theta_2\right)\right) \longrightarrow W_3 = 1. \end{aligned} \tag{A.2}$$

Equation (A.1) maps the interior of the disc in Figure 15(a) onto the upper half of the w-plane in Figure 15(b). Applying (A.1) to the fourth point gives

$$\begin{aligned} Z_4 &= \exp\left(-i\left(\psi_2 - \theta_2\right)\right) \longrightarrow W_4 = w_4 \\ &= \frac{\cos\left(\psi_1 + \psi_2\right) - \cos\left(\theta_1 - \theta_2\right)}{\cos\left(\psi_1 + \psi_2\right) - \cos\left(\theta_1\right)\cos\left(\theta_2\right) + 3\sin\left(\theta_1\right)\sin\left(\theta_2\right)}. \end{aligned} \tag{A.3}$$

A second bilinear transformation maps the w-plane onto the $\bar{t}$-plane

$$\bar{t} = \frac{\bar{a} + \bar{b}w}{1 + \bar{d}w}, \tag{A.4}$$

whereby the following pairs of points are mapped onto each other:

$$\begin{aligned} W_1 &\longrightarrow \overline{T}_1 = -1, \\ W_2 &\longrightarrow \overline{T}_2 = 1, \\ W_3 &\longrightarrow \overline{T}_3 = \frac{1}{p}, \\ W_4 &\longrightarrow \overline{T}_4 = \frac{-1}{p}. \end{aligned} \tag{A.5}$$

These are also just three degrees of freedom, because the parameter p is free and follows from (A.5). With (A.2), (A.4), and (A.5) one obtains

$$\bar{a} = 1, \tag{A.6a}$$

$$\bar{b} = 1 + \sqrt{2\left(1 + \frac{1}{w_4}\right)}, \tag{A.6b}$$

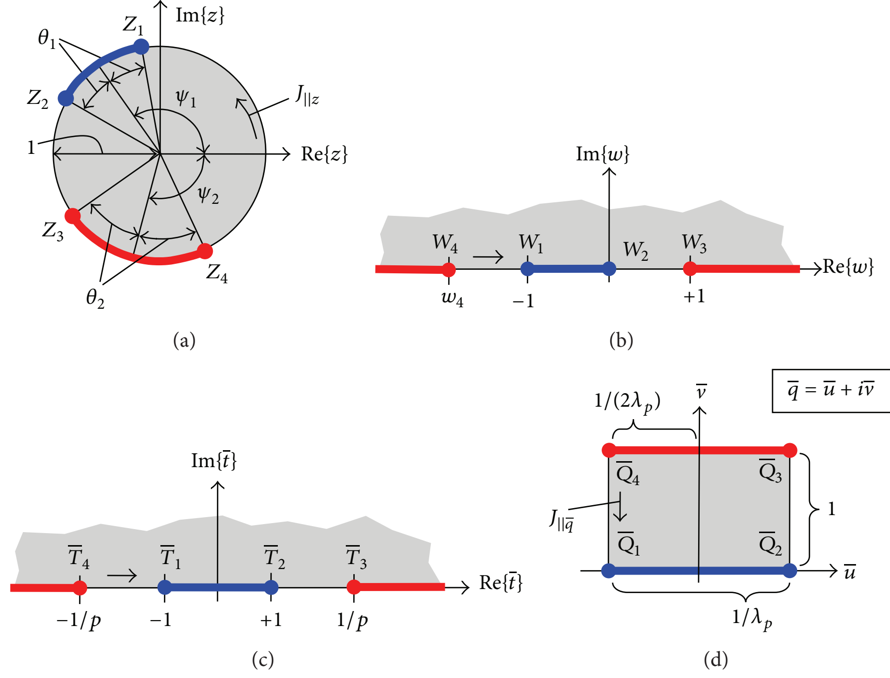

Figure 15: Series of conformal transformations that map a disc of radius 1 with two arbitrarily large supply contacts in the z-plane to a rectangle of λ_p squares in the $\bar{q}$-plane. The contact $\overline{Z_3Z_4}$ is at potential V_{in} and the contact $\overline{Z_1Z_2}$ is at ground potential.

$$\bar{d} = 1 - \sqrt{2\left(1 + \frac{1}{w_4}\right)}, \tag{A.6c}$$

$$p = \frac{w_4 - 1}{1 + w_4\left(3 + 2\sqrt{2\left(1 + 1/w_4\right)}\right)}. \tag{A.6d}$$

Inserting (A.3) into (A.6d) gives p as a function of geometrical parameters $\psi_1, \psi_2, \theta_1, \theta_2$. Finally, a Schwartz-Christoffel transformation

$$\bar{q} = \frac{1}{2\lambda_p K(p)} \int_{\alpha=0}^{\bar{t}} \frac{\mathrm{d}\alpha}{\sqrt{1-\alpha^2}\sqrt{1-p^2\alpha^2}} \tag{A.7}$$

maps the upper half of the $\bar{t}$-plane to the interior of the rectangle in the $\bar{q}$-plane shown in Figure 15(d). $K(p)$ is the complete elliptic integral $\int_0^1 (1-\alpha^2)^{-1/2}(1-p^2\alpha^2)^{-1/2}\mathrm{d}\alpha$. The $\bar{t}$- and $\bar{q}$-planes are similar to Figures 5c and d in [14]. The edge $\overline{\bar{Q}_1\bar{Q}_2}$ is at ground potential and the opposite edge $\overline{\bar{Q}_3\bar{Q}_4}$ is at potential V_{in}. Applying (A.7) to $\overline{\bar{Q}_2\bar{Q}_3}$ gives the resistance between both contacts

$$R_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = R_S\lambda_p \quad \text{with } \lambda_p = \frac{K'(p)}{2K(p)} \tag{A.8}$$

with $K'(p) = K(\sqrt{1-p^2})$.

Since the length $\overline{\bar{Q}_2\bar{Q}_3} = 1$ the electric field in the $\bar{q}$-plane is homogeneous within the rectangle and equal to $-iV_{\text{in}}$. The current density along the boundary is $J_{||\bar{q}} = \sigma_0 V_{\text{in}}$. The situation is the same as in Figure 1 of [14], where we computed the Hall-geometry factor of a rectangular Hall plate with point-sized output contacts. Applying (6) of [14] to our Figure 15(d) gives the Hall potential at small magnetic field (valid in the entire Hall device):

$$\phi_{\bar{q}} = -\mu_{\text{H}} B_z V_{\text{in}} \left\{\bar{u} + \frac{4}{\pi^2\lambda_p} \cdot \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n^2} \frac{\cosh\left(n\pi\lambda_p\left(\bar{v}-1/2\right)\right)}{\cosh\left(n\pi\lambda_p/2\right)} \cdot \cos\left(n\pi\left(\lambda_p\bar{u}\right) + \frac{1}{2}\right)\right\}. \tag{A.9}$$

Along the isolating boundary $\overline{\bar{Q}_4\bar{Q}_1}$ it holds that

$$\bar{u} = \frac{-1}{2\lambda_p},$$
$$\bar{v} = \frac{1}{K'(p)} \int_{\alpha=1}^{-1/\bar{t}'} \frac{\mathrm{d}\alpha}{\sqrt{\alpha^2-1}\sqrt{1-p^2\alpha^2}} \quad \text{with } 1 \le -\bar{t}' \le \frac{1}{p}, \tag{A.10}$$

whereby $\bar{t}'$ denotes the test point, where the Hall potential is evaluated. It is obtained by inserting $z = \exp(i\psi)$ into (A.1) and the result into (A.4):

$$\bar{t}' = \frac{\cos((\psi - 2\psi_1 - \psi_2 - \theta_2)/2) - \cos\theta_1 \cos((\psi + \psi_2 + \theta_2)/2) + p \sin\theta_1 \sin((\psi + \psi_2 + \theta_2)/2)}{p\cos((\psi - 2\psi_1 - \psi_2 - \theta_2)/2) - p\cos\theta_1 \cos((\psi + \psi_2 + \theta_2)/2) + \sin\theta_1 \sin((\psi + \psi_2 + \theta_2)/2)}. \quad \text{(A.11)}$$

Equations (A.9), (A.10), and (A.11) were checked with a numerical simulation on a circular Hall plate with the parameters $\psi_1 = 125^\circ$, $\psi_2 = 105^\circ$, $\theta_1 = 25^\circ$, $\theta_2 = 40^\circ$, $\sigma_0 = 1\,\text{S/m}$, $\mu_H B_z = 0.01$, $t_H = 1\,\text{m}$, and $V_{in} = 1\,\text{V}$. The finite element simulation used a fine mesh of 1.85 million triangular elements and Lagrange multipliers. Figure 16 shows a plot of the Hall potential along the isolating boundary between the two supply contacts. It also gives the difference between FEM-simulation and the analytical calculation according to (A.9). Evidently the matching between both calculation results is better than 0.01% for most parts on the boundary; only in the immediate vicinity of the contacts the meshing was still too coarse and this gave deviations up to 0.2%.

If both supply contacts become point-sized and the sense contact is in the symmetry plane between them we have $\theta_2 = \theta_1 \to 0$, $\psi_2 = \psi_1$, and $\psi = 0$. This gives $\bar{v} = 1/2$ and $\lambda_p \to (2/\pi)\ln((4\sin\psi_1)/\theta_1)$. We insert this and (A.10) into (A.9) and we note that $1/\cosh(n\pi\lambda_p/2) \to 2^{1-2n}(\theta_1/\sin\psi_1)^n$. Equation (A.9) gives the Hall potential at the sense contact $\phi_{\bar{q}} \to \mu_H B_z V_{in}/(2\lambda_p)(1 - 4\theta_1/(\pi^2 \sin\psi_1))$, whereby the current through the device is $V_{in}/(\lambda_p R_S)$. In the discussion of Figure 6(a) we said that the output voltage between both devices was $V_{out} = S_i B_z I_{in}$ and hence the Hall potential of a single device is $V_{out}/2 = S_i B_z I_{in}/2$ with $I_{in}/2$ being the current through the device. Comparison gives $\phi_{\bar{q}} = V_{out}/2$ from which it follows from the current related magnetic sensitivity that

$$S_i = \frac{1}{2}\frac{\mu_H}{\sigma_0}\frac{1}{t_H}\left(1 - \frac{4\theta_1}{\pi^2 \sin\psi_1}\right). \quad \text{(A.12)}$$

Comparison of (A.12) with (1) gives the Hall-geometry factor for small supply contacts and point-sized sense contacts in the symmetry plane between them:

$$G_{H0}^{(3C)} = 1 - \frac{4\theta_1}{\pi^2 \sin\psi_1}. \quad \text{(A.13)}$$

If all three contacts are point-sized the Hall-geometry factor tends to 1 and (A.12) is identical to (1).

B. 4C-Halls with 180° Symmetry

Here we show that conventional 4C-Hall plates have the highest signal-to-noise ratio at given input resistance, if they are 90° symmetric with $(L/W)_{in}^{(4C)} = (L/W)_{out}^{(4C)} = \sqrt{2}$. We start with 4C-Hall plates that have two orthogonal mirror symmetries. As an example such devices may be rectangular with two contacts covering the entire short sides and the other two contacts covering portions of the long sides, whereby the centers of the contacts coincide with the centers of the edges of the rectangle. Equivalent geometries can be obtained by conformal transformation. Such devices were discussed thoroughly in [14]. There equations were given for the Hall-geometry factor (equations (29a–c) in [14]) and input and output resistance (equations (10) and (16) in [14]) at low magnetic field. According to (2) we want to maximize $G_{H0}^{(4C)}/\sqrt{(L/W)_{in}^{(4C)}(L/W)_{out}^{(4C)}}$. Figure 17 shows a plot of this function versus the two degrees of freedom of this device, namely, $(L/W)_{in}^{(4C)}$ and $(L/W)_{out}^{(4C)}$.

From Figure 17 we see that the maximum is achieved for devices with $(L/W)_{in}^{(4C)} = (L/W)_{out}^{(4C)}$; such devices have 90° symmetry. For this kind of symmetry a simple approximate formula is known that expresses the Hall-geometry factor at low magnetic field as a function of squares $\lambda = (L/W)_{in}^{(4C)} = (L/W)_{out}^{(4C)}$ [15]:

$$G_{H0}^{(4C)} \cong \frac{\lambda^2}{\sqrt{\lambda^4 + \lambda^2/2 + 4}}. \quad \text{(B.1)}$$

Equation (B.1) is accurate at $\lambda = 0, \sqrt{2}, \infty$. With (B.1) we can compute $G_{H0}^{(4C)}/\lambda \cong \lambda/\sqrt{\lambda^4 + \lambda^2/2 + 4}$ and look for its maximum, which is at $\lambda = \sqrt{2}$. Luckily, at $\lambda = \sqrt{2}$ (B.1) is accurate and so the result is also accurate, although (B.1) is basically only an approximation. Inserting $\lambda = \sqrt{2}$ into (B.1) gives an upper boundary

$$\max \frac{G_{H0}^{(4C)}}{\sqrt{(L/W)_{in}^{(4C)}(L/W)_{out}^{(4C)}}} = \frac{\sqrt{2}}{3} \cong 0.471 \quad \text{at } \left(\frac{L}{W}\right)_{in}^{(4C)} = \left(\frac{L}{W}\right)_{out}^{(4C)} = \sqrt{2} \quad \text{(B.2)}$$

which cannot be exceeded by any 4C-Hall.

C. Symmetrical 3C-Halls

Here we compute numerically the input resistance and the Hall-geometry factor for symmetrical 3C-Halls which have three contacts of arbitrarily large, equal size and which exhibit 120° symmetry. The finite element models comprised $0.5\cdots1.3$ million elements, whereby the large numbers of elements were used for small contacts. Lagrange multipliers were used. The parameters were $\sigma_0 = 1\,\text{S/m}$, $\mu_H B_z = 0.01$, $t_H = 1\,\text{m}$, and $V_{in} = 1\,\text{V}$. Figure 18 plots the low-field Hall-geometry factor versus number of squares of the input resistance in an operation according to Figure 6(a).

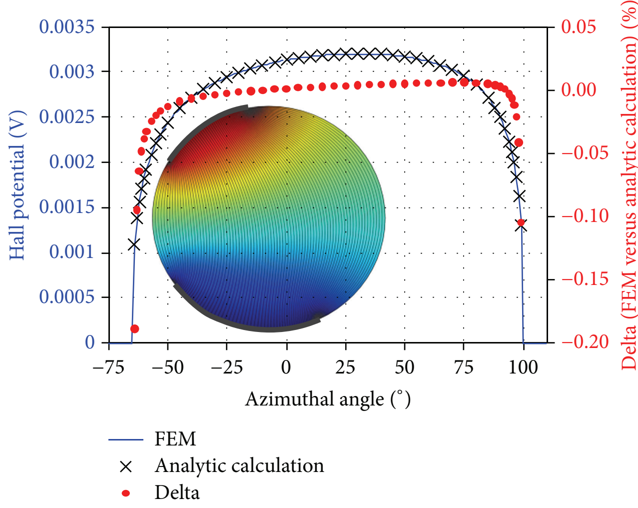

FIGURE 16: Hall potential along the right isolating boundary between the two supply contacts. Comparison of results from a finite element simulation and an analytical calculation after (A.9). The inset shows the geometry with current streamlines and the color coding gives the total potential (where red color denotes 1 V and blue color 0 V). The total potential is the sum of potential at zero magnetic field and the Hall potential.

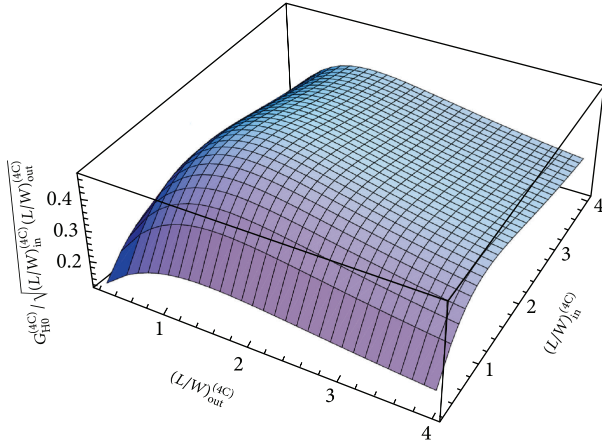

FIGURE 17: The ratio of Hall-geometry factor at small magnetic field over the square-root of product of input and output numbers of squares for all 4C-Halls with two orthogonal mirror symmetries plotted for input and output numbers of squares between 0 and 4. The maximum is in the diagonal $(L/W)_{\text{in}}^{(4C)} = (L/W)_{\text{out}}^{(4C)}$.

The maximum is obtained if each contact extends over 60°. Consider

$$\max \frac{G_{H0}^{(3C)}}{\sqrt{(L/W)_{\text{in}}^{(a)} (L/W)_{\text{out}}^{(a)}}} \approx 0.539$$

$$\text{at } \left(\frac{L}{W}\right)_{\text{in}}^{(a)} = \frac{K\left(\sqrt{2-\sqrt{3}/2}\right)}{K'\left(\sqrt{2-\sqrt{3}/2}\right)} \approx 0.577. \tag{C.1}$$

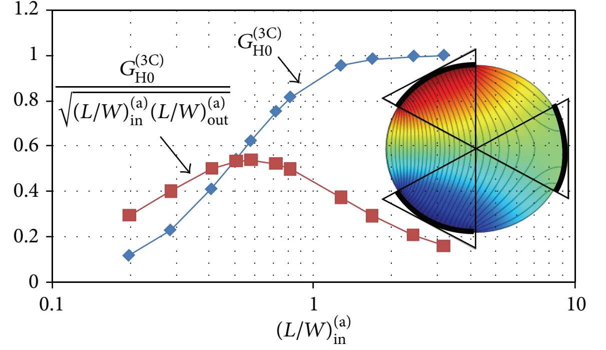

FIGURE 18: The Hall-geometry factor $G_{H0}^{(3C)}$ at small magnetic field and $G_{H0}^{(3C)}/\sqrt{(L/W)_{\text{in}}^{(a)}(L/W)_{\text{out}}^{(a)}}$ versus $(L/W)_{\text{in}}^{(a)}$ for symmetrical 3C-Halls with varying size of contacts. The inset shows the geometry of the circular device with three equal contacts and current streamlines and the color coding denotes total electric potential (whereby red means 1 V and blue means 0 V).

For an operation according to Figure 6(b) the maximum is $2/\sqrt{3}$ times larger:

$$\max \frac{G_{H0}^{(3C)}}{\sqrt{(L/W)_{\text{in}}^{(b)} (L/W)_{\text{out}}^{(b)}}} \approx 0.622$$

$$\text{at } \left(\frac{L}{W}\right)_{\text{in}}^{(b)} = \frac{3K\left(\sqrt{2-\sqrt{3}/2}\right)}{2K'\left(\sqrt{2-\sqrt{3}/2}\right)} \approx 0.866. \tag{C.2}$$

However, the extra factor 1/2 in (1) accounting for the single output contact per Hall tub reduces this large value to 0.311, which is 1.51 times smaller than the maximum value of 4C-Halls (see (B.2)).

Competing Interests

The author declares that there are no competing interests.

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References

[1] U. Ausserlechner, "Limits of offset cancellation by the principle of spinning current Hall probe," in *Proceedings of IEEE Sensors*, vol. 3, pp. 1117–1120, Vienna, Austria, October 2004.

[2] J. H. J. Fluitman, "Hall-effect device with both voltage leads on one side of the conductor," *Journal of Physics E: Scientific Instruments*, vol. 13, no. 7, pp. 783–785, 1980.

[3] R. S. Popovic, "The vertical Hall-effect device," *IEEE Electron Device Letters*, vol. 5, no. 9, pp. 357–358, 1984.

[4] L. Osberger, V. Frick, M. Madec, and L. Hebrard, "High resolution, low offset Vertical Hall device in low-voltage CMOS

technology," in *Proceedings of the 13th IEEE International NEW Circuits and Systems Conference (NEWCAS '15)*, pp. 1–4, Grenoble, France, June 2015.

[5] M. Hackner, R. Ernst, and H.-P. Hohe, "Vertikaler Hall sensor," Patent DE 10150955, 2001.

[6] M. Banjevic, *High bandwidth CMOS magnetic sensors based on the miniaturized circular vertical Hall device [Ph.D. thesis]*, EPFL, Lausanne, Switzerland, 2011.

[7] P. Kejik, S. Reymond, and R. S. Popovic, "Purely CMOS angular position sensor based on a new Hall microchip," in *Proceedings of the 34th Annual Conference of the IEEE Industrial Electronics (IECON '08)*, pp. 1777–1781, IEEE, Orlando, Fla, USA, November 2008.

[8] Patent US 9007060, Electronic device with ring-connected Hall effect regions, U. Ausserlechner, April 2015.

[9] C. Sander, M. C. Vecchi, M. Cornils, and O. Paul, "Ultra-low offset vertical Hall sensor in CMOS technology," *Procedia Engineering*, vol. 87, pp. 732–735, 2014.

[10] H.-J. Lippmann and F. Kuhrt, "Der Geometrieeinfluss auf den Hall-effekt bei rechteckigen Halbleiterplatten," *Zeitschrift für Naturforschung*, vol. 13, pp. 474–483, 1958.

[11] S. Sander, M. Cornils, M. C. Vecchi, and O. Paul, "Sensitivitätsoptimierung von vertikalen Hallsensoren mit drei Kontakten," in *Mikrosystemtechnik Kongress*, pp. 559–562, Aachen, Germany, October 2013.

[12] M. Demierre, *Improvements of CMOS Hall microsystems and application for absolute angular position measurements [Ph.D. thesis]*, Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, 2003.

[13] Ch. Schott and R. S. Popovic, "Linearizing integrated Hall devices," in *Proceedings of the International Conference on Solid-State Sensors and Actuators (Transducers '97)*, pp. 393–396, Chicago, Ill, USA, June 1997.

[14] U. Ausserlechner, "A method to compute the Hall-geometry factor at weak magnetic field in closed analytical form," *Electrical Engineering*, 2015.

[15] U. Ausserlechner, "Closed form expressions for sheet resistance and mobility from Van-der-Pauw measurement on 90° symmetric devices with four arbitrary contacts," *Solid-State Electronics*, vol. 116, pp. 46–55, 2016.

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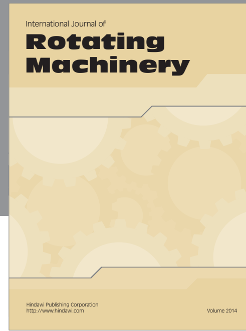
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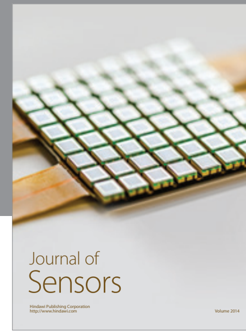
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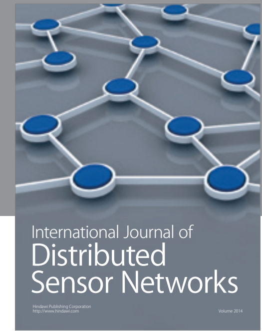
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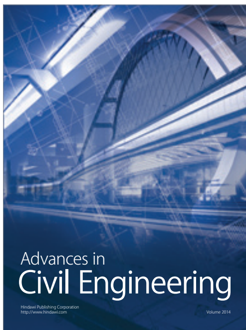
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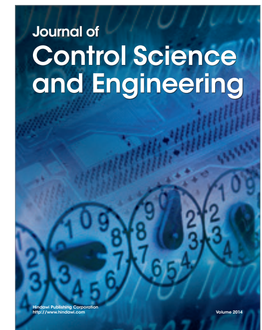
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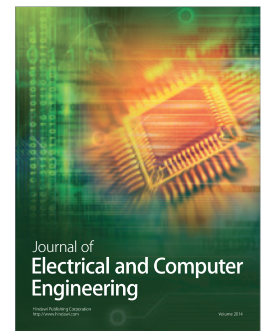
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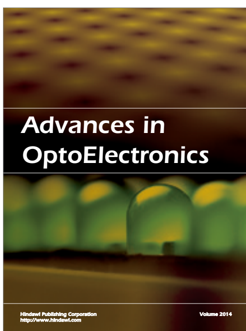
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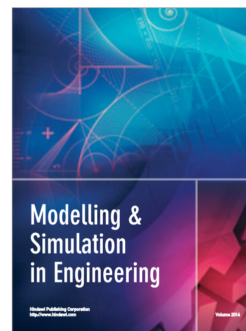
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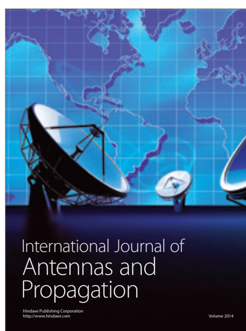
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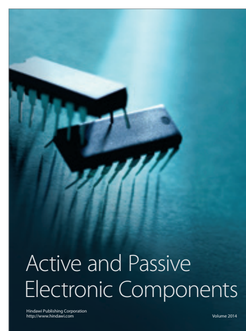
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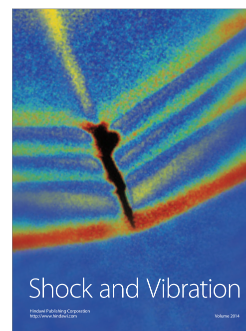
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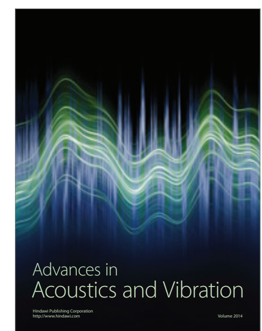
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