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*Research Article*

# Sliding-Mode Control of a Dc/Dc Postfilter for Ripple Reduction and Efficiency Improvement in POL Applications

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This paper proposes an active postfilter based on two Buck converters, connected in parallel, operating in complementary interleaving. In such a configuration the ripple in the load current could be virtually eliminated to improve the power quality in comparison with classical Point-Of-Load (POL) regulators based on a single Buck converter. The postfilter is designed to isolate the load from the main Buck regulator, leading to the proposed three-converter structure named BuckPS. The correct operation of the postfilter is ensured by means of a sliding-mode controller. Finally, the proposed solution significantly reduces the current harmonics injected into the load, and at the same time, it improves the overall electrical efficiency. Such characteristics are demonstrated by means of analytical results and illustrated using numerical results.

## 1. Introduction

The power supplies designed for computers and communications systems must provide sharp requirements: low voltage, high current, and load voltage ripples. Such conditions are imposed to ensure a high performance of the microprocessors, DSP, ASIC, or memory devices [1, 2]. Since the Buck converter provides output voltages lower than its input voltage [3], it is widely adopted in power architectures designed for this kind of electronic equipment [4], named Point-of-Load (POL) regulators. However, the quality of the current and voltage signals generated by a Buck converter is affected by the load, source, or parameters variation, which changes the ripple magnitudes among other problems [5, 6].

Several solutions have been proposed in the literature to improve the quality of the current and voltage generated by a Buck-based POL regulator. In [7], the ripple of a POL converter is reduced by means of a L-C output filter with two stages, which is classically regulated using a controller with two feedback points: the first point sensing the capacitor voltage of the first L-C stage and second point sensing the capacitor voltage of the second L-C stage, that is, the load voltage. In such a solution, the authors demonstrate that a controller with a single feedback point could be used to stabilize the POL converter, but it requires adjusting one L-C filter to cancel out the zeros of the other L-C filter. In any case, the ripple magnitudes depend on the load impedance, which could change depending on the application conditions.

In [8] the performance of Buck-based POL with different current controllers is analyzed, taking into account the bandwidth of the voltage loop and changes in the input voltage. But such a solution does not analyze the ripple behavior with load variations.

A different approach was presented in [9], where a digital controller is used to reduce the load current ripple in a non-isolated POL converter. Such a solution is based on peak current and average current controllers implemented in an FPGA. This controller scheme requires an A/D converter, which increases the system cost in comparison with analog implementations. In the same way, [10] proposes a self-oscillating digital modulator to change instantaneously the dutycycle of the PWM signal driving the converter switch.

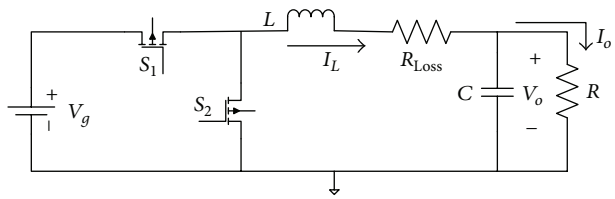


Figure 1: Typical structure of a Buck converter (BuckS).

Thus, it is possible to achieve a sampling frequency of the output voltage, required in the control loop, higher than the switching frequency of the power converter. In this way, a short time response is achieved in the compensation of load variations. But such a solution does not introduce current or voltage ripples analyses.

In [11] a method to design the output filter of a low-voltage/high-current synchronous Buck converter using performance boundary curves is proposed. Such curves constrain the regions in the space of parameters to ensure an acceptable output voltage ripple. But, similar to the previous solutions, the load and source changes that affect the ripple magnitudes are not analyzed.

The previous solutions address the current and voltage ripple limitations by means of passive filters, which are impossible to be modified in operation time. Hence, such solutions are sensible to changes in the load impedance, source voltage, and tolerances of the electronic component parameters. Therefore, this paper proposes a POL based on a synchronous Buck converter operating in cascade with an active postfilter, providing an almost ripple-free current to the load. The postfilter is composed of two parallel-connected Buck converters operating in complementary interleaving [12], and it is regulated using a sliding-mode controller to ensure its correct operation. The proposed POL compensates changes in the load impedance, source voltage, and electronic component parameters. Moreover, the proposed solution improves the electrical efficiency of classical Buck-based POL.

The paper structure is as follows: Section 2 analyzes the Buck converter, introduces the postfilter, and analyzes the proposed POL solution. Then, Section 3 presents the sliding-mode current controller designed to reduce the current and voltage ripples injected to the load. Section 4 illustrates the solution benefits in a realistic scenario by means of numerical results. Finally, conclusions close the work.

## 2. POL Regulator Based on a Postfilter

The proposed step-down POL regulator is based on the classical Buck topology, named BuckS, shown in Figure 1. In such a topology the output voltage ripple directly depends on the output capacitance, which is typically implemented using a large capacitor [13]. Using the classical approach given in [3], the output voltage ripple $\Delta V_o$ in the Buck converter is given in (1), which depends on the inductor peak current ripple $\Delta I_L$. In (1), $T$ represents the switching period, $C$ the output capacitance, $R_{\text{Loss}}$ the aggregated parasitic resistances of the inductor $L$ and the MOSFETs [14], and $D$ the converter duty cycle, while $I_o$ and $V_o$ represent the steady-state load current and voltage, respectively. Since the POL converters must provide reduced voltage ripples to the load [1, 2, 4], $\Delta V_o$ can be reduced by increasing $C$ and $L$ or by reducing $T$ (increasing the switching frequency $F_{\text{sw}}$) and the parasitic losses $R_{\text{Loss}}$. Instead, this paper proposes to use a dc/dc converter to reduce the effective $\Delta I_L$ that reaches the capacitor $C$ to achieve the required small $\Delta V_o$ condition

$$\begin{aligned} \Delta V_o &= \frac{\Delta I_L \cdot T}{8 \cdot C}, \\ \Delta I_L &= \frac{\left(V_o + R_{\text{Loss}} \cdot I_o\right) D' \cdot T}{2 \cdot L}. \end{aligned} \tag{1}$$

Moreover, from the small ripple approximation and volt-second and change balances [3], the steady-state induction current $I_L$, which is equal to the steady-state load current $I_o$, and the voltage conversion ratio are given in (2). In such equations $R$ represents the load impedance at the desired operation condition and $V_g$ represents the power source voltage

$$\begin{aligned} I_L &= \frac{V_o}{R}, \\ \frac{V_o}{V_g} &= \frac{D}{1 + R_{\text{Loss}}/R}. \end{aligned} \tag{2}$$

Finally, the efficiency $\eta$ of the BuckS POL regulator is given in (3). Such efficiency is reduced when the load current increases since the impedance $R$ is reduced. Therefore, the solution proposed in this paper is also intended to improve the overall electrical efficiency. Consider

$$\eta = \frac{1}{1 + R_{\text{Loss}}/R}. \tag{3}$$

In the following subsections the proposed postfilter and POL regulator are introduced, contrasting their performance with the classical BuckS solution.

*2.1. Postfilter Based on Parallel Buck Converters.* Figure 2 presents the proposed postfilter consisting of two Buck converters, operating in complementary interleaving, where the output capacitor is common for both Buck branches. The postfilter main MOSFETs ($S_{1U}$ and $S_{1L}$) are complementary activated to generate complementarily inductor current waveforms on $L_1$ and $L_2$. Such a condition produces the cancelation of the inductor current ripples to provide an almost ripple-free current to the output capacitor $C$, and based on (1), a small voltage ripple is imposed on the load. It must be pointed out that the secondary MOSFETs ($S_{2U}$ and $S_{2L}$) are also complementarily activated with respect to the main MOSFET of each branch.

To ensure the cancelation of the inductor current ripples, both Buck branches must operate in continuous conduction mode (CCM); otherwise if a branch current is zero (in discontinuous conduction mode (DCM)), the other branch

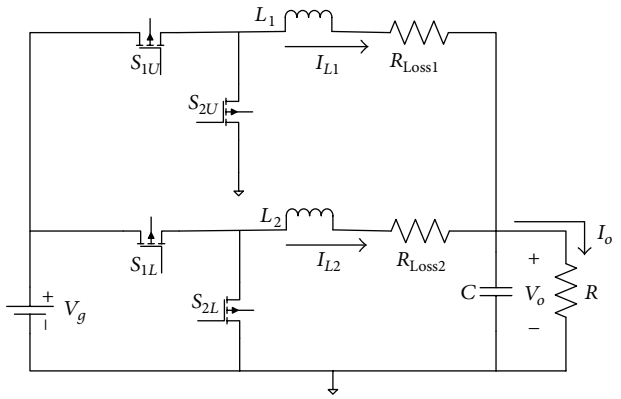


Figure 2: Buck converter in interleaved topology.

ripple is propagated to the output capacitor. From (1), and considering the scheme of Figure 2, where $R_{\text{Loss1}}$ and $R_{\text{Loss2}}$ represent the parasitic resistances in each branch, the CCM on both branches is achieved when the condition given in (4) is fulfilled. Such an expression takes into account the complementary activation of $S_{1U}$ and $S_{1L}$; therefore the first branch has a duty cycle $D$ while the second branch has a complementary duty cycle $D' = 1 - D$. Consider

$$\frac{V_o}{V_g} = \frac{D}{1 + R_{\text{Loss1}}/R} = \frac{D'}{1 + R_{\text{Loss2}}/R}. \tag{4}$$

Solving (4) for $D$, relation (5) is obtained

$$D = \frac{R + R_{\text{Loss1}}}{R_{\text{Loss1}} + 2R + R_{\text{Loss2}}}. \tag{5}$$

Therefore, the symmetrical interleaved Buck converter must be operated at the duty cycle $D$ given in (5) to achieve the desired reduction of the output voltage ripple. Moreover, such a duty cycle imposes the voltage conversion ratio given in

$$\frac{V_o}{V_g} = \frac{DR_{\text{Loss2}} + R_{\text{Loss1}}(1 - D)}{R_{\text{Loss2}} + \left(R_{\text{Loss1}}R_{\text{Loss2}}/R\right) + R_{\text{Loss1}}}. \tag{6}$$

In a practical implementation the inductors $L_1$ and $L_2$ and the MOSFETs could be selected to have similar values and construction characteristics: $L_1 = L_2 = L_f$ and $R_{\text{Loss1}} = R_{\text{Loss2}} = R_{Lf}$. Such a condition is useful to simplify the postfilter design and control since both branches must process the same power. On the basis of such a practical consideration, the required duty cycle given in (5) becomes $D = 0.5$, while the voltage conversion ratio provided by the postfilter becomes

$$\frac{V_o}{V_g} = \frac{1}{2 + \left(R_{Lf}/R\right)}. \tag{7}$$

Moreover, the steady-state currents in each inductor are equal as given in (8), while the steady-state load current is the sum of such currents, that is, the double of a branch current:

$$I_{L1} = I_{L2} = \frac{V_g}{2\left(2R + R_{Lf}\right)}. \tag{8}$$

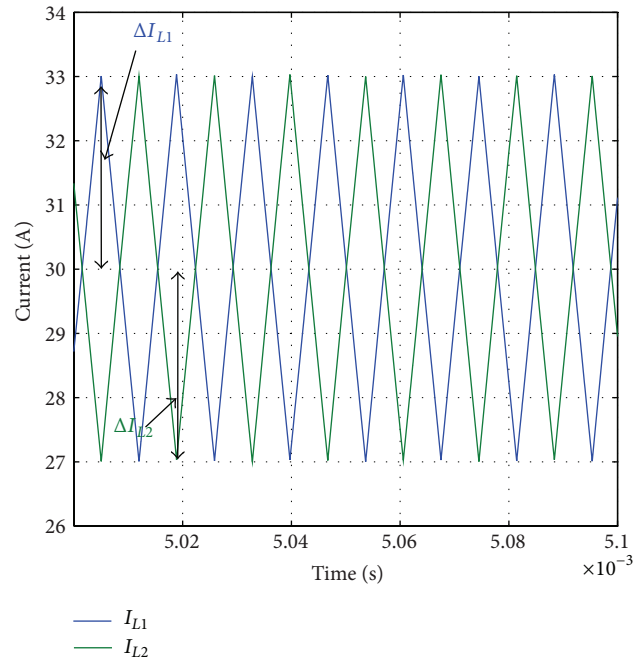


Figure 3: Inductors currents waveform.

In addition, the current ripples in both braches have the same magnitude, while the current ripple injected into the load is near to zero since the postfilter branches operate in complementary mode, which generates opposite slopes for both inductors current as illustrated in Figure 3, where $\Delta I_{L1}$ and $\Delta I_{L2}$ represent the ripple magnitudes for each branch. Therefore, since the current ripple reaching the postfilter output capacitor ($C$ in Figure 2) is near to zero, the output voltage ripple is also near to zero.

To ensure a correct ripple cancelation in the postfilter it is required that both branches exhibit the same average current with opposite instantaneous slopes, and at the same time, it is required that both branches operate in CCM. Such conditions must be ensured despite the load current magnitude or the aging of the components. But, from (5) and (7), it is noted that in all cases the duty cycle and voltage conversion ratio are fixed. Therefore, classical control paradigms based on fixed-frequency drivers, such as the PWM, are not suitable to regulate the postfilter: classical controllers, such as PI, PID, or leadlag, change the duty cycle (using a PWM [3, 15]) to compensate the system perturbations, but because the postfilter requires a fixed duty cycle, it is not possible to regulate it using such type of controllers. For this reason it is necessary to adopt another control paradigm that provides an additional freedom degree. In such a way, this paper proposes to regulate the postfilter using the sliding-mode technique to dynamically change the switching frequency, which according to (1) is given by $f = (V_o + R_{\text{Loss}} \cdot I_o)D'/(2 \cdot L \cdot \Delta I_L)$, to ensure that both branches operate with a fixed maximum difference between their currents, which ensures that both branches exhibit the same duty cycle, average current, and ripple magnitude for any system condition.

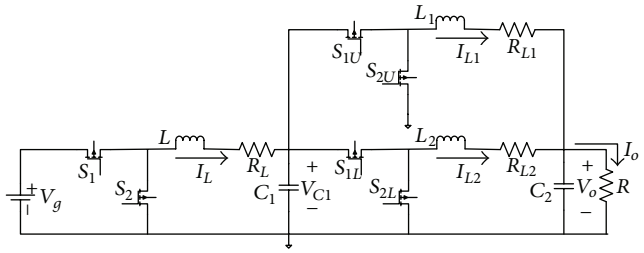


FIGURE 4: Synchronized Buck converter with postfilter in interleaved operation (BuckPS).

Finally, since the postfilter was designed using synchronous Buck converters, the CCM operation is granted.

*2.2. POL Converter.* The main drawback of the postfilter is evident from (5), (6), and (7): the voltage conversion ratio is constant. Therefore, an additional Buck converter is used to regulate the load voltage. Figure 4 presents the proposed POL topology, named BuckPS, obtained from the cascade connection of a Buck converter (interacting with the source) with the postfilter (interacting with the load), where the Buck converter must be independently controlled to regulate the load voltage. Hence, such a Buck converter can be controller using classical approaches based on PWM drivers and PI or PID controllers.

To provide a design criterion, which also ensures a fair comparison with the classical POL based on a Buck converter (BuckS), the inductors of both the postfilter and the Buck converter are considered to be equal; thus $L = L_1 = L_2 = L_f$ and $R_L = R_{L1} = R_{L2} = R_{Lf}$. Then, the voltage conversion ratio of BuckPS is given in (9), where $D_{\mathrm{PS}}$ represents the duty cycle of the Buck converter. Such an equation puts in evidence that the Buck converter could be independently controlled using a classical PWM-based technique:

$$\frac{V_o}{V_g} = \frac{2D_{\mathrm{PS}}R}{4R + 3R_L}. \tag{9}$$

Moreover, the inductor current of the BuckPS first stage, that is, the Buck converter, and the output current are given in (10). Contrasting such results with the BuckS characteristics given in (2), it is recognized that the BuckPS requires three inductors instead of one, but such devices must support the half of the current imposed on the BuckS inductor:

$$\begin{aligned} I_L &= \frac{D_{\mathrm{PS}}V_g}{4R + 3R_L}, \\ I_o &= \frac{2D_{\mathrm{PS}}V_g}{4R + 3R_L}. \end{aligned} \tag{10}$$

An additional condition of the BuckPS solution is extracted from (9): the voltage conversion ratio is always lower than 0.5. This condition is illustrated in Figure 5 considering four cases for $R_L/R = \{0\%, 10\%, 25\%, 35\%\}$. In such an example, for $R_L/R = 10\%$, a $V_o/V_g = 0.25$ is obtained by operating the BuckPS at $D_{\mathrm{PS}} = 0.5375$, while in a BuckS

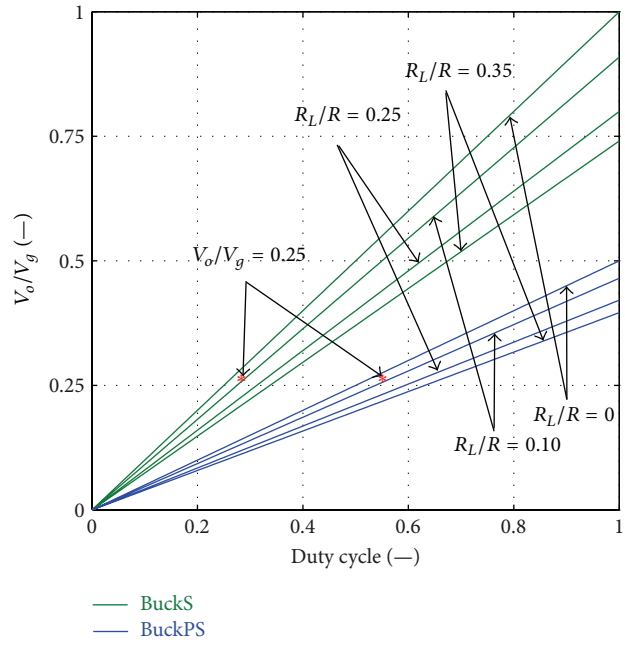


FIGURE 5: Conversion ratio of BuckPS and BuckS.

$D_{\mathrm{S}} = 0.275$ is required to achieve the same voltage conversion ratio. In general, from (2) and (9) it is concluded that the BuckPS always provides lower output voltage than the BuckS for a given duty cycle. Such a condition is also verified in Figure 5. Hence, lower POL voltages can be achieved with the BuckPS by avoiding duty cycle saturations imposed by turn-ON and turn-OFF times of the MOSFETs, which limit the minimum operative duty cycle.

Then, the efficiency of the BuckPS is obtained from (9) and (10):

$$\eta_{\mathrm{BuckPS}} = \frac{4R}{(4R + 3R_L)}. \tag{11}$$

Such an expression shows an efficiency improvement over BuckS (3). Such a condition is because the BuckPS generates currents in each of the three inductors equal to half of the inductor current in the BuckS. Therefore, since the power losses depend on the square of the current, the losses in the BuckPS are lower. To illustrate such an aspect, the resistance relation $k_r$ given in (12) and the efficiency factor $\alpha$ given in (13) have been defined. In particular, $\alpha > 1$ implies an improved efficiency of BuckPS over BuckS, while $\alpha < 1$ implies a reduced efficiency of BuckPS in comparison with BuckS. Consider

$$k_r = \frac{R_L}{R}, \tag{12}$$

$$\alpha = \frac{\eta_{\mathrm{BuckPS}}}{\eta_{\mathrm{BuckS}}} = \frac{4 + 4k_r}{4 + 3k_r}. \tag{13}$$

Since $k_r > 0$ for real values of $R$ and $R_L$, $\alpha > 1$ is always granted in (13), which demonstrates that the proposed BuckPS solution is more efficient than the classical BuckS

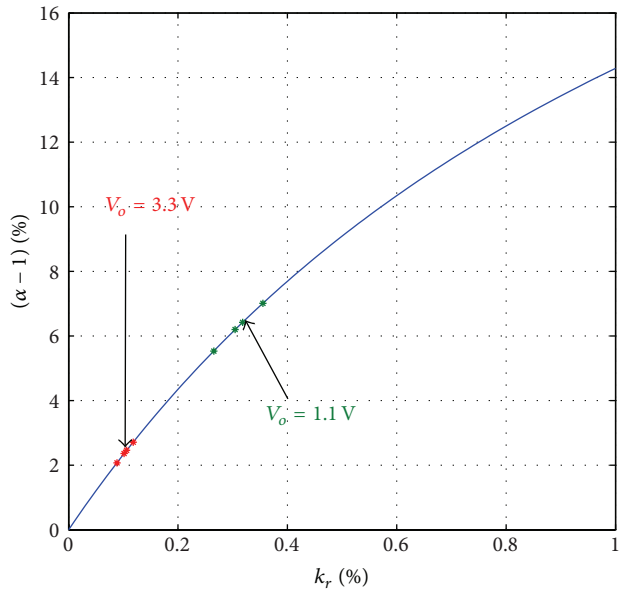


FIGURE 6: Improvement efficiency factor.

TABLE 1: Resistance relation and improvement efficiency factor with commercial elements.

| Load (A) | $R_L$ (mΩ) | $k_r$ (%) | | $\alpha - 1$ (%) | | Cost ($US) |
|---|---|---|---|---|---|---|
| 5 | 18 + 49 | 10.15 | 30.45 | 2.36 | 6.20 | 3.80 |
| 20 | 8.0 + 9.5 | 10.61 | 31.82 | 2.46 | 6.42 | 4.07 |
| 40 | 5.0 + 2.3 | 8.85 | 26.55 | 2.07 | 5.53 | 5.68 |
| 60 | 3.5 + 3.0 | 11.82 | 35.52 | 2.71 | 7.01 | 6.07 |

implementation. Figure 6 presents the efficiency improvement factor $\alpha - 1$, which quantifies the relative efficiency improvement of BuckPS over BuckS, for different values of the resistance relation $k_r$. Such numerical results illustrate the improved efficiency of the BuckPS solution.

Table 1 shows values of the efficiency improvement factor considering commercial elements [16]. The calculations were made for load currents equal to 5 A, 20 A, 40 A, and 60 A, with a ripple current of 10%. Moreover, $R_L$ is calculated by adding the inductor resistance and the ON-resistance of the MOSFETs. Then, $k_r$ and $\alpha - 1$ have two values: the left value corresponds to a load voltage $V_o = 3.3$ V, while the right value corresponds to $V_o = 1.1$ V. In the first case, the efficiency improvement is near to 2.4%, while in the second case the efficiency improvement is between 5% and 7.5%. Therefore, for modern microprocessors requiring very low operation voltages, the proposed BuckPS could provide a significant improvement in the electrical efficiency.

## 3. Sliding-Mode Current Control

The sliding-mode control technique has been extensively used in the literature to regulate power converters due to its robustness and speed [17]. Moreover, sliding-mode controllers have been also used to regulate active filters to improve power quality in AC environments [18]. In the same way, this paper proposes to design a sliding-mode controller to regulate the postfilter, this with aim of ensuring the correct behavior of the system in any operation condition.

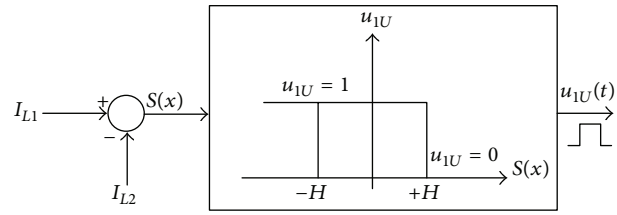


FIGURE 7: Logic scheme of sliding-mode controller.

The controller design requires a state-space model of the POL converter. In such a way, the state-space system that describes the BuckPS dynamic behavior, depending on $u_B$ (driving signal of the first Buck converter) and $u_{1U}$ (driving signal of the postfilter), is given in (14). Such a system considers the states vector $x = [i_L i_{L1} i_{L2} v_{C1} v_{C2}]^T$ and follows the nomenclature defined in Figure 4. Consider

$$\begin{aligned}
\dot{i_L} &= -\frac{R_L i_L}{L} - \frac{v_{C1}}{L} + \frac{V_g u_B}{L},\\
\dot{i_{L1}} &= -\frac{R_{L1} i_{L1}}{L_1} + \frac{v_{C1} u_{1U}}{L_1} - \frac{v_{C2}}{L_1},\\
\dot{i_{L2}} &= -\frac{R_{L2} i_{L2}}{L_2} + \frac{v_{C1}\overline{u_{1U}}}{L_2} - \frac{v_{C2}}{L_2},\\
\dot{v_{C1}} &= \frac{i_L}{C_1} - \frac{i_{L1} u_{1U}}{C_1} - \frac{i_{L2}\overline{u_{1U}}}{C_1},\\
\dot{v_{C2}} &= \frac{i_{L1}}{C_2} + \frac{i_{L2}}{C_2} - \frac{v_{C2}}{(RC_2)}.
\end{aligned} \tag{14}$$

In (14) $\overline{u_{1U}} = 1 - u_{1U}$, where $u_{1U} = 1$ means that MOSFET $S_{1U}$ is turned ON and MOSFET $S_{1L}$ is turned OFF, while $u_{1U} = 0$ means that MOSFET $S_{1U}$ is turned OFF and MOSFET $S_{1L}$ is turned ON.

Following the same approach proposed in [19], a sliding-mode controller was designed to regulate both postfilter inductor currents. The adopted sliding surface, given in (15), is intended to guarantee the same current in both postfilter branches:

$$S(x) = i_{L1} - i_{L2} = 0. \tag{15}$$

But to design a practical realization, the surface must be constrained into a hysteretic band $\pm H(t)$, where the MOSFET commutation is determined by (16): when the difference between the indictor currents is smaller than the lower boundary of the hysteretic band $-H(t)$, $u_{1U}$ must be turned ON (set to 1); while if the difference between the inductor currents is larger than the upper boundary of the hysteretic band $+H(t)$, $u_{1U}$ must be turned OFF (set to 0). Therefore, $H(t)$ defines the steady-state value of the currents ripple. Moreover such surface $S(x) = 0$ imposes the same average value for both currents, which guarantee the correct

operation of the postfilter. Figure 7 presents the logic scheme for both the sliding surface and the hysteretic comparator:

$$\begin{aligned} i_{L1} - i_{L2} &< -H(t), \quad u_{1U} \text{ set to } 1, \\ i_{L1} - i_{L2} &> +H(t), \quad u_{1U} \text{ set to } 0. \end{aligned} \tag{16}$$

The necessary and sufficient conditions for surface reachability are given in [20]

$$\begin{aligned} \lim_{S\to 0^-} \frac{dS(x)}{dt} &> 0 \quad u_{1U} = 1, \\ \lim_{S\to 0^+} \frac{dS(x)}{dt} &< 0 \quad u_{1U} = 0. \end{aligned} \tag{17}$$

The time derivative of the sliding surface, given in (18), is obtained from (15). Then, by introducing the relation (18) in (17) and replacing also the second and third rows of (14) in (17), the expressions for surface reachability given in (19) are obtained

$$\frac{dS(x)}{dt} = \frac{di_{L1}}{dt} - \frac{di_{L2}}{dt}, \tag{18}$$

$$\begin{aligned} \lim_{S\to 0^-} \frac{dS(x)}{dt} &= v_{C2}\left(\frac{1}{L_2} - \frac{1}{L_1}\right) + \left(\frac{R_{L2}}{L_2} i_{L2} - \frac{R_{L1}}{L_1} i_{L1}\right) \\ &\quad + \frac{v_{C1}}{L_1} > 0, \\ \lim_{S\to 0^+} \frac{dS(x)}{dt} &= v_{C2}\left(\frac{1}{L_2} - \frac{1}{L_1}\right) + \left(\frac{R_{L2}}{L_2} i_{L2} - \frac{R_{L1}}{L_1} i_{L1}\right) \\ &\quad - \frac{v_{C1}}{L_1} < 0. \end{aligned} \tag{19}$$

Since for a practical implementation the postfilter inductors are selected equally, $L_f = L_1 = L_2$ and $R_{Lf} = R_{L1} = R_{L2}$, relation (19) is simplified as in (20). In such an expression it is evident that both inequalities are fulfilled, this is because inductors are always positive ($L_f > 0$) and Buck converters provide output voltages with the same polarity of the input voltage ($v_{C1} > 0$). Therefore, the surface reachability of the postfilter controller is always granted

$$\begin{aligned} \lim_{S\to 0^-} \frac{dS(x)}{dt} &= \frac{v_{C1}}{L_f} > 0, \\ \lim_{S\to 0^+} \frac{dS(x)}{dt} &= -\frac{v_{C1}}{L_f} < 0. \end{aligned} \tag{20}$$

The other important aspect in terms of control concerns the local stability, which is verified by using the equivalent control condition given in (21) [19], where $u_{eq}$ represents an equivalent continuous control input that constrains the system evolution into the sliding surface

$$\frac{dS(x)}{dt} = 0, \quad 0 < u_{eq} < 1. \tag{21}$$

From (18) and the second and third rows of (14), in which the control input $u_{1U}$ has been replaced by the equivalent continuous variable $u_{eq}$, the condition given in (21) can be rewritten as in

$$0 < u_{eq} = \frac{R_{L1}L_2 i_{L1} - R_{L2}L_1 i_{L2} + (L_2 - L_1)\, v_{C2} + L_1 v_{C1}}{(L_1 + L_2)\, v_{C1}} < 1. \tag{22}$$

Taking into account that the inductors are selected equally, then (22) becomes

$$0 < R_{Lf} L_f (i_{L1} - i_{L2}) + L_f v_{C1} < 2 L_f v_{C1}. \tag{23}$$

Therefore, the difference between the inductor currents must satisfy (24) to guarantee local stability

$$-\frac{v_{C1}}{R_{Lf}} < i_{L1} - i_{L2} < \frac{v_{C1}}{R_{Lf}} \Longrightarrow |i_{L1} - i_{L2}| < \frac{v_{C1}}{R_{Lf}}. \tag{24}$$

To ensure that relation (24) is fulfilled in any condition, the maximum magnitude of the inductors current difference must be constrained as in

$$\max |i_{L1} - i_{L2}| = \Delta_{\max} < \frac{v_{C1}}{R_{Lf}}. \tag{25}$$

From the second and third rows of (14) with $u_{1U} = 1$ and $\overline{u}_{1U} = 0$, the ripple magnitudes of both postfilter currents, as defined in Figure 3, are given in (26). It is noted that the maximum difference between the inductor currents is constrained by the sum of such ripple magnitudes as in (27):

$$\begin{aligned} \Delta i_{L1} &= \frac{T}{4L_f}\left(-R_{Lf} i_{L1} + v_{C1} - v_{C2}\right), \\ \Delta i_{L2} &= -\frac{T}{4L_f}\left(-R_{Lf} i_{L2} - v_{C2}\right), \end{aligned} \tag{26}$$

$$\begin{aligned} \Delta_{\max} &= \Delta i_{L1} + \Delta i_{L2}, \\ \Delta_{\max} &= \frac{T}{4L_f}\left(-R_{Lf}(i_{L1} - i_{L2}) + v_{C1}\right). \end{aligned} \tag{27}$$

Since the maximum difference between the inductor currents is $\max |i_{L1} - i_{L2}| = \Delta_{\max}$, the second row of (27) must consider $i_{L1} - i_{L2} = \Delta_{\max}$. Therefore, the maximum difference between the inductor currents is given by

$$\Delta_{\max} = \frac{v_{C1}}{(4L_f/T) + R_{Lf}}. \tag{28}$$

The local stability condition of the sliding-mode controller given in (25) is rewritten as in

$$\frac{v_{C1}}{(4L_f/T) + R_{Lf}} < \frac{v_{C1}}{R_{Lf}}. \tag{29}$$

Such an inequality leads to the condition given in (30), which is fulfilled for any operating condition since both the inductance and period are positive quantities. Hence, relation (30) confirms the local stability of the proposed sliding-mode controller:

$$\frac{4L_f}{T} > 0. \tag{30}$$

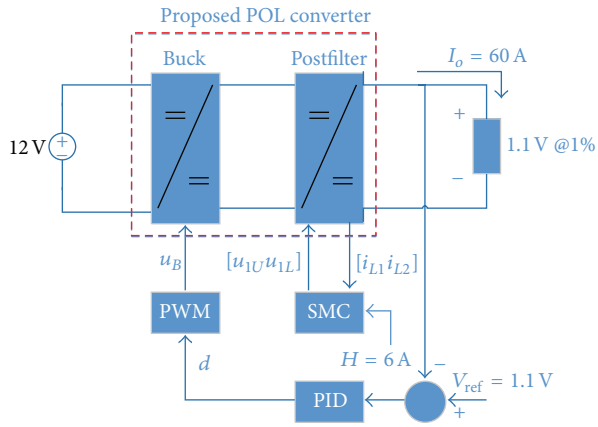


Figure 8: Practical implementation of the proposed Core 2 Duo POL regulator.

Therefore, since surface reachability is granted by (20) and the local stability is granted by (30), the proposed sliding-mode controller always drives the postfilter, from any initial condition, to operate within the space $|i_{L1} - i_{L2}| < H$, which ensures the same average current for both branches and a maximum current difference constrained to $H$. Such characteristics ensure a correct operation of the postfilter.

## 4. Numerical Results

A realistic application was considered to illustrate the operation and advantages of the proposed POL structure by means of numerical results. The example considers a POL regulator designed to supply an Intel Core 2 Duo processor [21, 22], which requires a regulated 1.1 V with 1% voltage ripple and 60 A. Then, the POL converter was designed to provide a maximum voltage ripple equal to 11 mV with a constant current ripple equal to 10% of the maximum load current (6 A). Moreover, the switching frequency was selected equal to 100 kHz for the single Buck converters and near to 100 kHz for the postfilter. Therefore, the inductors were calculated to ensure such current ripple and switching frequencies; hence all the inductors were selected equal to 1.5 $\mu$H. Similarly, the capacitors were calculated to fulfill the desired voltage ripple hence all the capacitors we selected equal to 280 $\mu$F. Moreover, from the last row of Table 1 the parasitic resistance for the single Buck converter and each postfilter branches is extracted, which for all the inductors and MOSFETs are equal to 6.5 m$\Omega$. Finally, the application considers a 12 V battery as the main power source.

Figure 8 shows the practical implementation of the proposed POL regulator to supply the Core 2 Duo processor. Such a scheme shows the two control systems required: the sliding-mode controller to regulate the postfilter, named SMC, and a PID controller acting on the Buck converter to regulate the load voltage.

Figure 9 shows the postfilter operation in two conditions: start-up and load transient. The former one considers the start-up of the POL converter, where the voltage and currents of all the capacitors and inductors are zero. The postfilter time simulation (top-left) shows the satisfactory current ripple cancelation, where the output current Io is almost ripple free. It must be pointed out that in such a figure Io is presented divided by 2 to be in the same scale of the postfilter inductor currents. In addition, the figure also presents, in black traces, the maximum limits of the inductors current difference, which is in agreement with the current ripple condition imposed by the application (6 A). From such a behavior it is noted that, in the start-up condition, the sliding-mode controller successfully guarantees the correct postfilter operation: both inductor currents have the same average current and the same current ripple, which produces a fixed duty cycle equal to 0.5 to ensure the ripple cancelation.

The postfilter phase plane for the start-up operation is also presented at the bottom-left figure, where it is confirmed that the system is into the sliding surface for any steady-state or transient condition.

The same behavior is achieved for a step-down load transient, in which time simulation is presented in the figure at top-right, where a 10% load perturbation was introduced. Similar to the start-up case, in this transient condition the postfilter provides an almost ripple-free load current, while the system is always within the sliding surface (depicted at the bottom-right). Therefore, the simulation in Figure 9 confirms the correct operation of the postfilter and the stability of the sliding-mode controller predicted in (20) and (30) for any operation condition.

Another component to design in the proposed POL solution concerns the load voltage regulator, named PID in Figure 8. To design such a controller, the postfilter is modeled to operate in closed loop with the sliding-mode controller, where both inductor currents are equal and the duty cycle of the prefilter is 0.5. Therefore, the statespace (14) can be simplified as given in (31), where the single control variable is $u_B$:

$$\begin{aligned}
\dot{i_L} &= -\frac{R_L i_L}{L} - \frac{v_{C1}}{L} + \frac{V_g u_B}{L},\\
\dot{i_{Lf}} &= -\frac{R_{Lf} i_{Lf}}{L_f} + \frac{v_{C1}}{(2L_f)} - \frac{v_{C2}}{L_f},\\
\dot{v_{C1}} &= \frac{i_L}{C_1} - \frac{i_{Lf}}{C_1},\\
\dot{v_{C2}} &= \frac{2i_{Lf}}{C_2} - \frac{v_{C2}}{(RC_2)}.
\end{aligned} \tag{31}$$

Then, using the PWM-based averaging technique described in [3, 23], the state-space system in (31) was linearized by replacing $u_B$ with the duty cycle of the Buck converter. Such a system was used to design the PID controller in agreement with the following criteria: closed loop bandwidth equal to 6 kHz, phase margin higher than 60°, and gain margin higher than 6 dB. The design of the controller was performed in SISOTOOL from MATLAB, obtaining the expression given in

$$\text{PID}(s) = 1200\frac{\left(1 + 3.1 \times 10^{-5} s\right)^2}{s}. \tag{32}$$

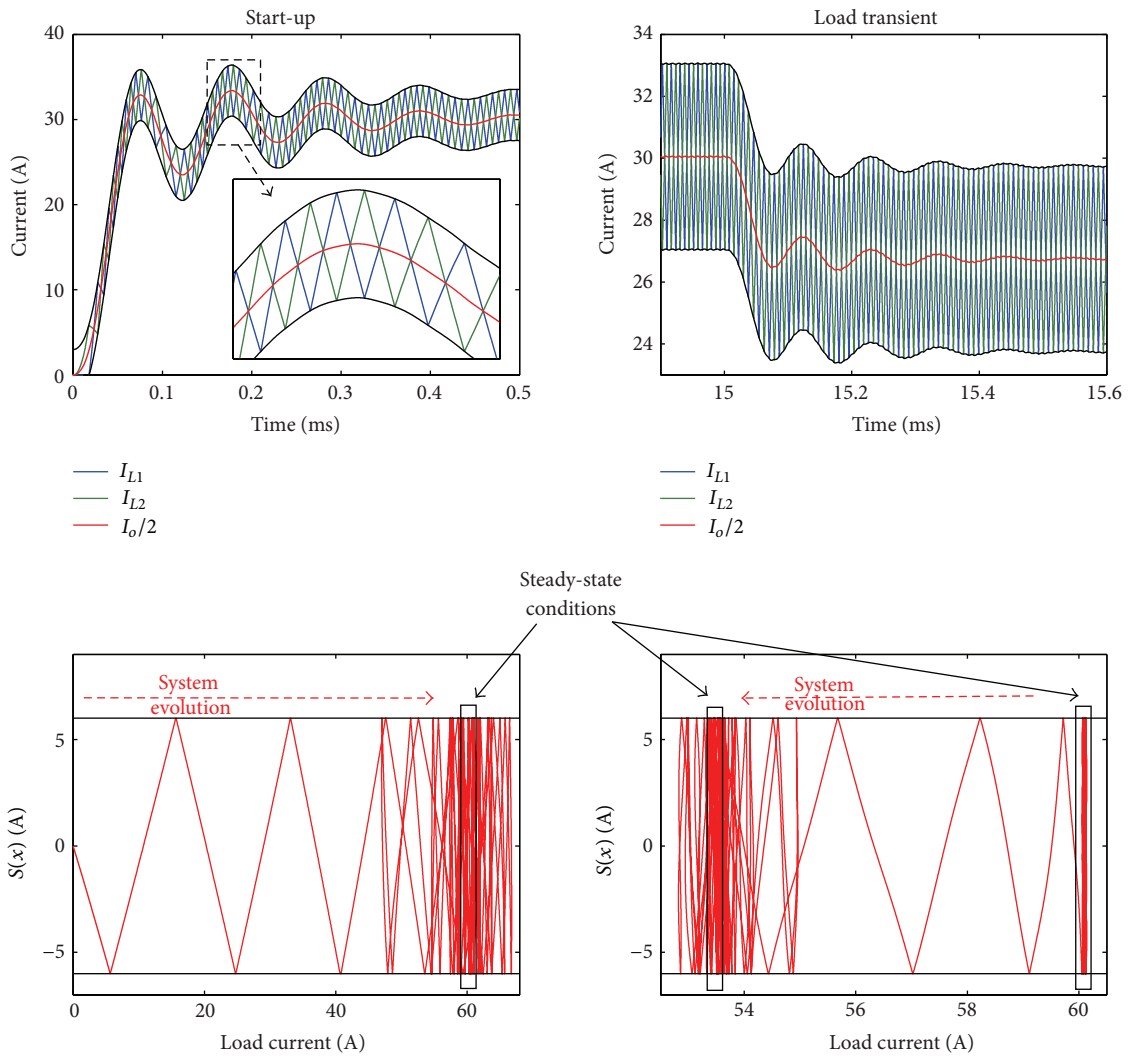


Figure 9: Postfilter simulation: start-up and load transient conditions.

To illustrate the improvement of the proposed POL, a BuckS POL was also designed and simulated. Figure 10 compares the BuckS and BuckPS output voltage ripples, obtaining magnitudes of 3.1% and 0.032%, respectively. Such results put in evidence the large reduction in the voltage ripple provided by the proposed solution, which avoids the requirement of electrolytic capacitances. Similarly, Figure 11 shows the power spectral density (PSD) of the output voltage harmonics for both the BuckS and BuckPS, where a large harmonic component at 100 kHz produced by the BuckS is observed, while the BuckPS exhibits a much attenuated component due to the complementary inductor currents of the postfilter. The simulation also shows that the BuckPS produces a different PSD due to the contribution of both inductor currents, which results in a new harmonic component at 143 kHz. In any case, those results confirm the improvement in the power quality provided to the load by the proposed solution.

To show the overall system performance, Figure 12 shows the dynamic behavior of the BuckPS under a load transient. In such a case, the PID controller must regulate the load voltage while the sliding-mode controller regulates the postfilter. The simulation considers a load current perturbation equal to 10% of the steady-state value (from 60 A to 66 A). The results show the satisfactory compensation of the load voltage provided by the PID controller given in (32). Similarly, Figure 12 also shows the satisfactory regulation of the postfilter inductor currents. Such a correct operation of the sliding-mode controller is also evident from the system evolution reported in the bottom figure, where the system is always constrained with the sliding surface $S(x)$ for any operation condition.

It must be point out that a more complex controller for the Buck converter, such a high-order lead-lag structure, could be used to improve the output voltage dynamics.

## 5. Conclusions

This paper has presented a POL converter based on the cascade connection of an interleaved postfilter with a Buck converter. This solution, named BuckPS, has the aim of

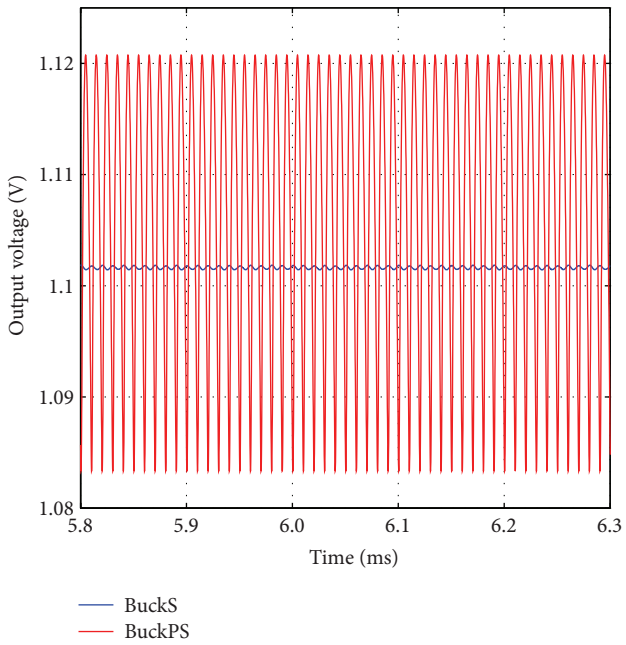


Figure 10: Output voltage ripple comparison between BuckS and BuckPS.

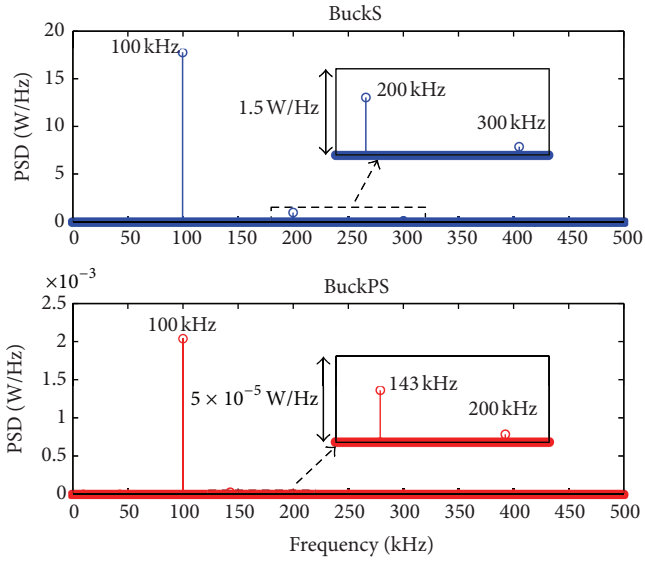


Figure 11: Power spectral density of BuckS and BuckPS.

improving the quality of the power provided to the load, by reducing the output voltage ripple. Moreover, the BuckPS provides an improved efficiency (between the 2.5% and 7.5%) over a classical POL based on a single Buck converter, named BuckS. Similarly, since the BuckPS strongly reduces the output current ripple, its output capacitor could be significantly smaller in comparison with the classical BuckS implementation. This characteristic allows designing the BuckPS without using electrolytic capacitances, which improves the system reliability.

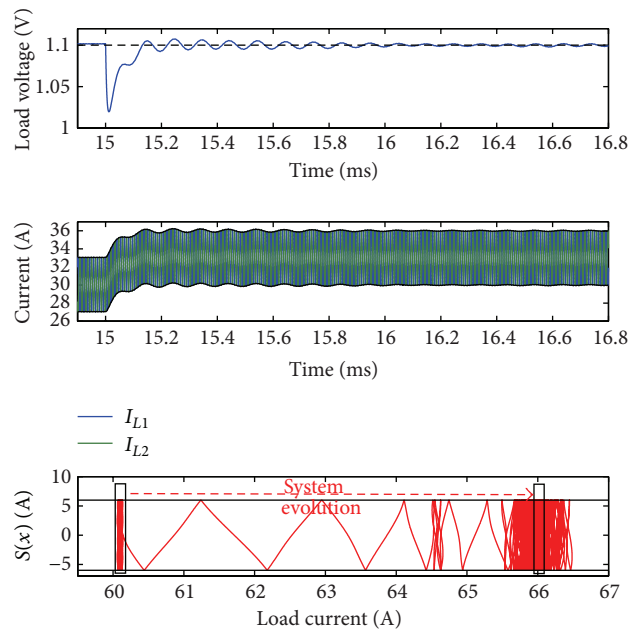


Figure 12: Dynamic behavior of the BuckPS output voltage.

Despite the advantages of the BuckPS structure, it requires more elements and its regulation strategy is more complex in comparison with the BuckS, which could lead to a more costly device. In any case, the elements required by the BuckPS have lower ratings, therefore lower cost, which is especially important for the output capacitor: in BuckS structures a large electrolytic capacitor is required, which increases the system size and cost. Therefore, a comparison between the cost and size of BuckS and BuckPS solutions depends on the specific application conditions.

To illustrate the benefits of the proposed solution, a practical application based on real load requirements was analyzed and simulated. The numerical results of such an example confirm the correctness of the POL converter and the stability of the sliding-mode controller. In the same way, the simulation also puts in evidence the improvement of the proposed BuckPS regulator over a classical BuckS solution.

Finally, this paper describes an analog implementation of the POL controllers. Therefore, a future research may be focused on the digital implementation of the POL control system to provide a more flexible and industrial oriented solution. In such a further work, one of the open problems concerns the fast acquisition of the postfilter currents since the sampling circuit could filter such high-frequency signals. Similarly, the time-delay effect generated by the acquisition and processing circuits could introduce errors in the sliding-mode comparator, degrading the controller accuracy and stability.

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