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Research Article

Semidigital PLL Design for Low-Cost Low-Power Clock Generation

Ni Xu, Woogeun Rhee, and Zhihua Wang

Institute of Microelectronics, Tsinghua University, Beijing 100084, China

Correspondence should be addressed to Woogeun Rhee, wrhee@tsinghua.edu.cn

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This paper describes recent semidigital architectures of the phase-locked loop (PLL) systems for low-cost low-power clock generation. With the absence of the time-to-digital converter (TDC), the semi-digital PLL (SDPLL) enables low-power linear phase detection and does not necessarily require advanced CMOS technology while maintaining a technology scalability feature. Two design examples in 0.18 μm CMOS and 65 nm CMOS are presented with hardware and simulation results, respectively.

1. Introduction

As the system integration complexity increases, robust low-cost frequency generation is highly demanded. Especially, the use of advanced CMOS technologies makes the traditional phase-locked loop (PLL) design challenging as on-chip variability and modeling inaccuracy become severe in deep submicron CMOS. Large loop parameter variation makes it difficult to find the optimum bandwidth for phase noise, spur, and settling time. In addition, analog passive devices become a bottleneck for scalability and integrating the loop filter (LPF) has been a challenging task in the conventional PLL design. Figure 1 depicts an example showing large area contribution of the on-chip loop filter to the PLL. Since the capacitor takes a significant portion of the whole LPF area, the gate leakage current by the on-chip MOS capacitor becomes substantial enough to affect the PLL performance, degrading the static phase error or reference spur performance. As a result, thick-oxide MOSFETs or metal-to-metal capacitors are used for the PLL loop filters at the cost of using an extramask.

2. Design Issues in All-Digital PLL

While integrating a loop filter has been a challenging task in the conventional PLL design, removing the analog loop filter is considered an alternative solution in the recent PLL works [1–13]. However, the all-digital PLL (ADPLL) requires a high-resolution complex time-to-digital converter (TDC) which requires advanced CMOS technology. Use of the bang-bang phase detector (BBPD) relaxes the TDC requirement but suffers from a nonlinear PLL bandwidth control [2]. In this paper, we present recent architectures of hybrid PLL systems which reduce technology dependency.

In the ADPLL design, high resolution of the TDC as shown in Figure 2 is important not only to enhance linearity but also to reduce in-band phase noise of the ADPLL. For the given reference clock frequency F_{REF} and the VCO frequency F_{VCO}, the in-band phase noise L of the ADPLL due to the TDC time resolution Δt_{res} is given by [1]

$$L = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{\mathrm{res}}}{T_{\mathrm{VCO}}}\right)^2 \cdot \frac{1}{F_{\mathrm{REF}}}. \tag{1}$$

The equation implies that finer TDC resolution is required for higher VCO output frequency. In fact, this is analogous to the fact that noise contribution of the phase detector (PD) increases with high division ratio N by the factor of $20 \log N$ in the conventional analog PLL design. Therefore, the ADPLL design also has difficulty in achieving low in-band phase noise performance with high division ratio. Besides, the ADPLL requires advanced CMOS technology for low in-band noise performance based on the above equation, which is different from the analog PLL. In addition to the advanced technology requirement, the TDC is sensitive

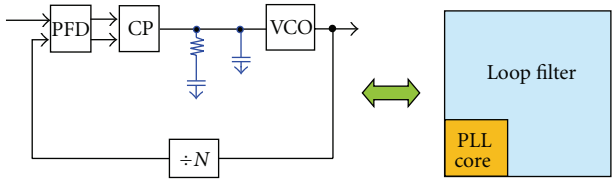


Figure 1: Loop filter area contribution to PLL in advanced CMOS.

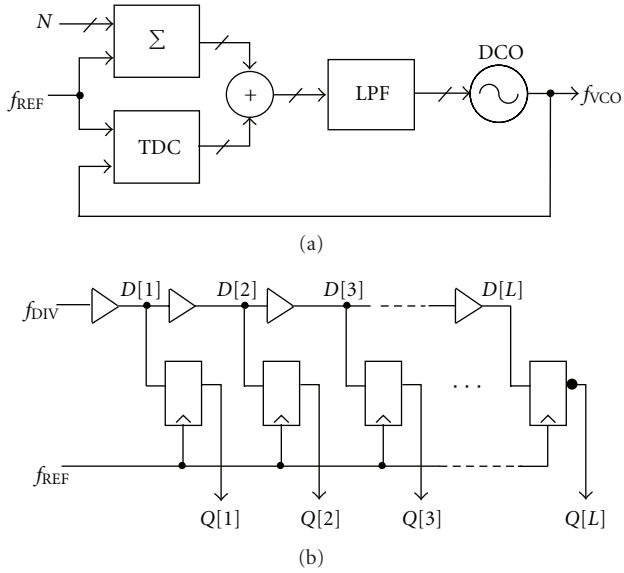


Figure 2: ADPLL with linear TDC [1].

to PVT variation. Typical delay time variation of a single inverter exhibits nearly 50% variation over process and temperature. Such a high sensitivity can cause poor linearity and nonuniform phase detector gain, resulting in widespread spur generation.

Table 1 shows architecture comparison between the ADPLL and the conventional analog PLL which typically consists of the phase-frequency detector (PFD) and the charge pump (CP). The conventional analog PLL suffers from poor scalability and leakage current sensitivity mainly due to the analog loop filter and does not offer good control of loop parameters compared to the ADPLL. On the other hand, the ADPLL features high scalability and reconfigurability with digital implementation but suffers from design complexity and nonlinear loop dynamics. Since the digitally controlled oscillator (DCO) has many switches with parasitic capacitance and the TDC requires fine-timing resolution using an advanced CMOS technology is highly demanded for the high performance ADPLL design.

3. Technology Scalable Semidigital PLL

In this paper, we consider a low-cost TDC-less semidigital PLL architectures [14–17] which do not require a large integration capacitor in the LPF, achieving technology scalability and leakage current immunity like the ADPLL.

Table 1: ADPLL versus conventional PLL.

	ADPLL	Conventional PLL
Power	Fair (depends on tech)	Good
Reconfigurability	Good	Poor
Scalability	Good	Poor
I_{Leak} Immunity	Good	Poor
Linear BW control	Fair	Good
Design complexity	High	Fair
Tech. dependency	High	Fair

3.1. Basic Concept. The type II PLL inherently provides an integral path which tracks frequency offset independently so that, in theory, the static phase error can be zero even with the frequency offset. Figure 3 shows how the type II PLL obtains frequency acquisition without generating a static phase error. As far as phase tracking is concerned, the integral path is a large-signal path while the proportional-gain path is a small-signal path. When the large-signal path slowly tunes the VCO to the desired frequency, the small-signal path does not have to provide additional DC information for frequency acquisition. Therefore, different implementation for each path is possible in the type II PLL design, namely, the integral path in digital and the proportional-gain path in analog.

Figure 4 shows the basic concept of the semi-digital loop control [14], and a linear model is shown in Figure 4(b). Since the control path of the type II PLL can be decomposed into a proportional-gain path and an integration path as discussed, independent implementation is considered for each path. For the proportional-gain path, the conventional analog control is used except the absence of the integrating capacitor. Since the capacitance values for high-order poles are not high, either the MOS capacitor with negligible leakage current or the MIM capacitor can be used. As for the integral path, digital implementation is done with the BBPD and the FSM to compensate for the limited frequency tracking capability of the proportional-gain path. The $\Delta\Sigma$ modulator is used to provide fine frequency resolution as done in the ADPLL. The main purpose of the digital integration path is to provide frequency tracking rather than phase tracking. Accordingly, the time constant of the digital integration path can be much longer than the analog small-signal path, resulting in overdamped loop dynamics. With the overdamped loop dynamics, the PLL bandwidth is linearly controlled by the charge pump current whose value can be digitally programmable in the design. In summary, the proposed hybrid loop control with the analog proportional path and the digital integration path provides linear phase tracking, leakage-insensitive loop filtering, technology scalability, and uniform PD gain capability.

3.2. Architecture Comparison with Other PLLs. For the SDPLL design with an LC VCO, three different topologies can be considered for the analog proportional-gain path as shown in Figure 5. Figure 5(a) is based on the CP PLL topology as already presented previously [14]. Other way

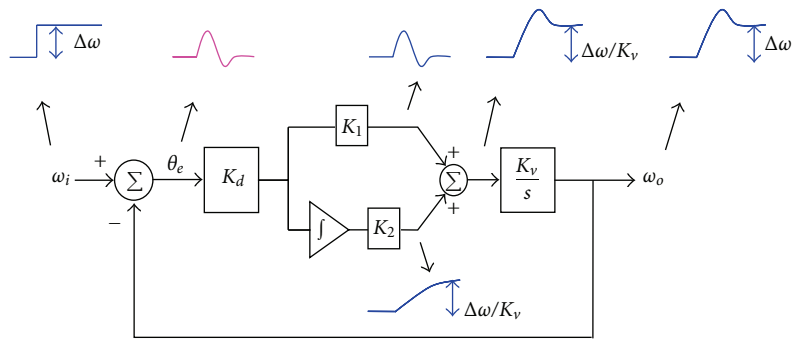
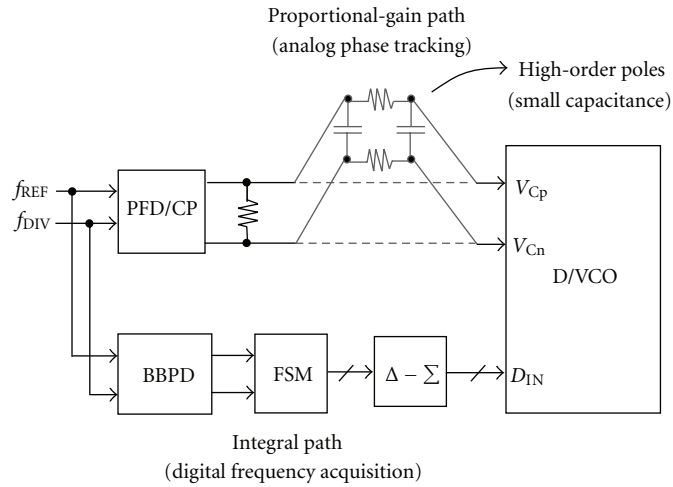
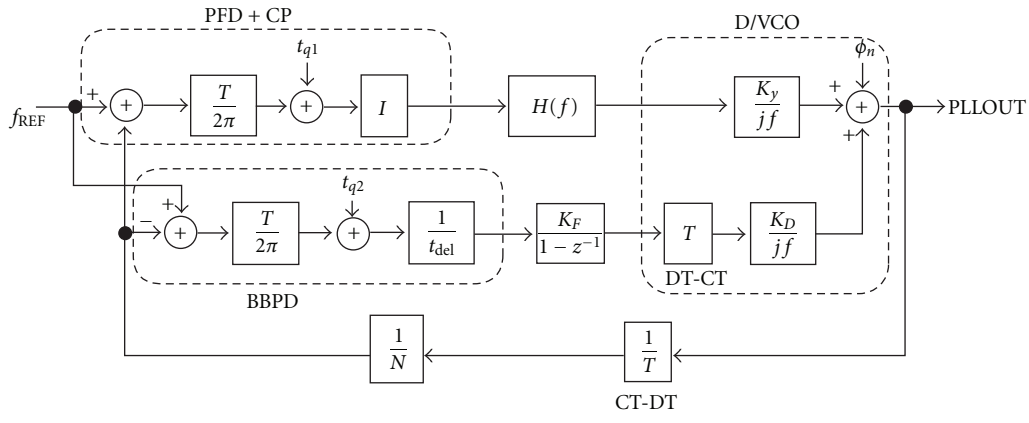


Figure 3: State-variable model of type II PLL.



(a)



(b)

Figure 4: (a) Basic concept and (b) linear model.

is to have the PFD output directly connected to the VCO input [15]. In this case, a linear amplifier (LA) is needed to set the optimum common mode voltage for maximum varactor tuning range. The additional LA degrades VCO noise performance. However, the LA noise contribution can be suppressed by the PLL bandwidth since the LA is placed after the LPF and gets high-pass noise transfer function by the PLL. Without the CP, Figure 5(b) can achieve better in-band phase noise performance. When the PLL bandwidth is narrow and requires good phase noise performance of the VCO, the topology from Figure 5(a) should be chosen. In addition, the phase detector gain can be well regulated over PVT variations if the bias current of the charge pump is generated by an on-chip resistor and a bandgap reference

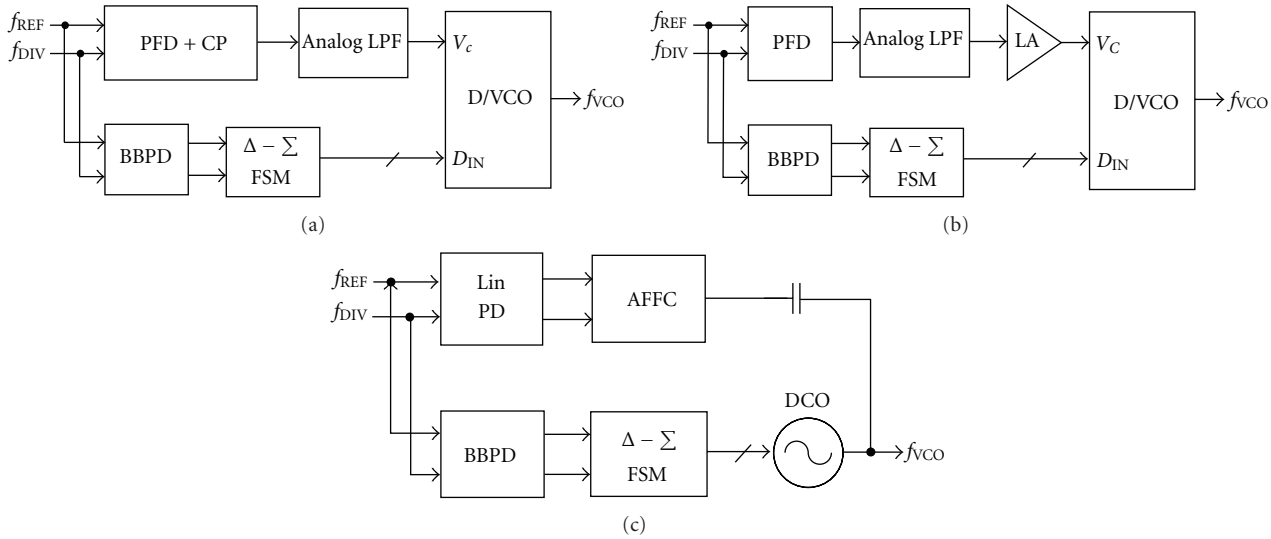


Figure 5: (a) PFD/CP based, (b) PFD/LA based, and (c) AAFC based.

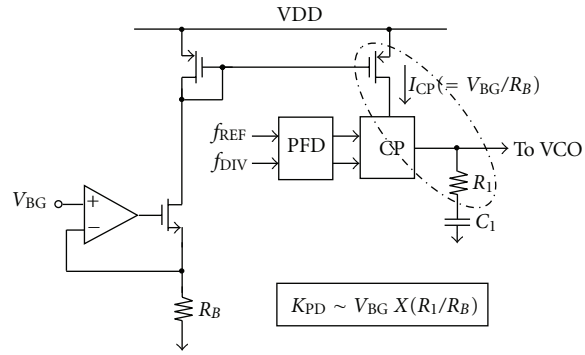


Figure 6: CP biasing for uniform PD gain.

voltage [16], which is illustrated in Figure 6. The last one shown in Figure 5(c) uses analog feed-forward circuits (AFFC) to provide a linear phase modulation path [17]. However, having the AC-coupling path at the VCO output requires more complicated design efforts than employing the dual-control path at the VCO input since dealing with high frequency signals is more difficult. Moreover, the analog RC filter in the AFFC connected to both supply and ground can cause a coupling path to the supply noise.

As depicted in Figure 7, the SDPLL offers moderate performance between the conventional analog PLL and the ADPLL. A mixed-mode loop control with an analog proportional path and a digital integration path offers a leakage-insensitive and technology scalable architecture comparable to the digital PLL, while maintaining low-cost linear phase detection like the analog PLL. The PFD/CP-based proportional-gain path provides linear loop dynamics in which tracking bandwidth is simply set by the PD gain, the passive LPF transfer function, and the analog VCO gain. In addition, with the absence of the linear TDC, power consumption can be reduced and using advanced

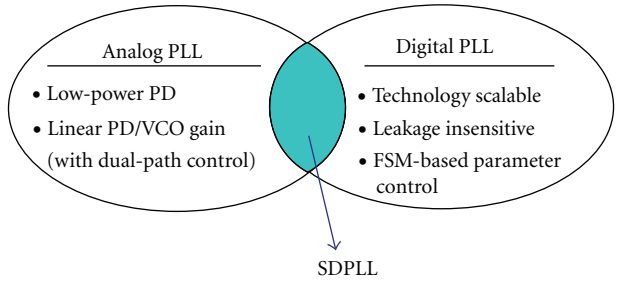


Figure 7: Architecture comparison.

CMOS technology is not a must for achieving good noise performance.

4. Design Examples

In this paper, two SDPLL design examples are presented; one designed in 0.18 μm CMOS for digital clock generation and

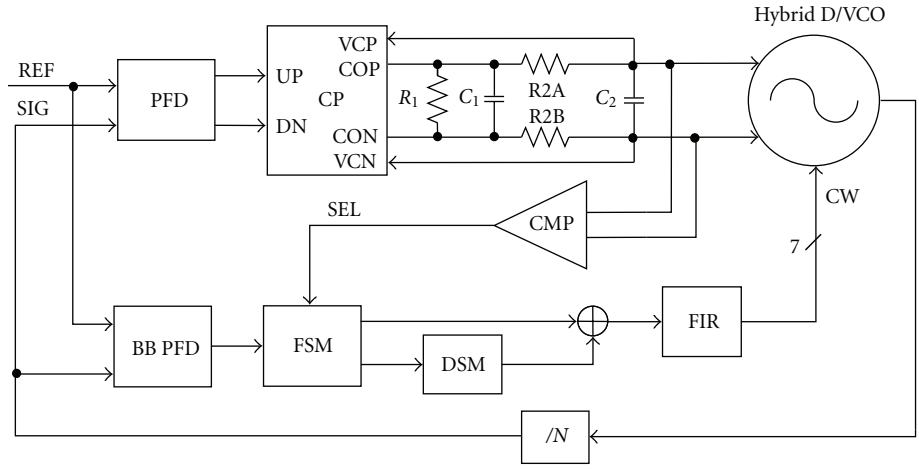


Figure 8: SDPLL block diagram.

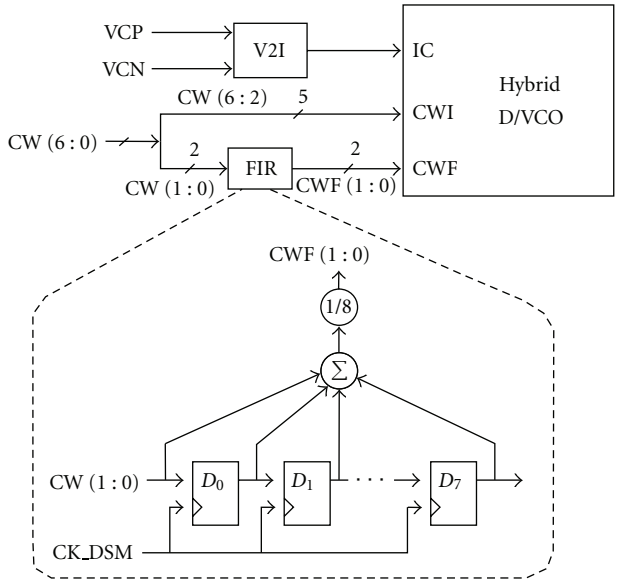


Figure 9: Hybrid D/VCO with embedded FIR filtering.

the other in 65 nm CMOS for wireless applications (Table 2). The former shows that the hybrid loop control is successfully verified in hardware, and the latter shows promising low-power feature of the SDPLL for two-point modulation with a small area comparable to the ADPLL-based modulation.

4.1. 0.18 μm CMOS SDPLL for Digital Clock Generation. Figure 8 shows a block diagram of the SDPLL [14]. To minimize noise coupling, a differential charge pump followed by a differential loop filter is designed in the analog control path. For the 3rd- and 4th-order poles, the MIM capacitor is used to have good isolation from the substrate noise coupling. In the digital integration path, the BBPD is used to provide bi-level information to the 18-bit FSM, where the 7-bit output from the MSB is the integral part and the following 8-bit output is the fractional part. The remaining 3-bit output is used for averaging function. The frequency resolution set by the digital tuning loop is about 2.1 MHz per LSB. Since the digital integration path has slow frequency acquisition, an adaptive bandwidth scheme is designed. For that purpose, a voltage comparator is added to provide transition information to the FSM.

Figure 9 shows the hybrid DCO block diagram with the FIR-based Δ-Σ control, where a 7-bit control input is used. A 2nd-order MASH modulator is used for its simple structure. The 2nd-order MASH modulator has 2-bit output CW (1 : 0), so only the last two bits from the LSB are controlled by the modulator. The 5-bit static input, CW (6 : 2) directly controls the digital input of the hybrid DCO. Since the hybrid DCO has a 5-bit static input and a 2-bit dynamic modulated by the 10-bit modulator, the total frequency resolution of 15 bit is obtained in the digital control path.

Figure 10 shows the behavioral simulation results of the PLL settling behavior, (a) without digital path and (b) with

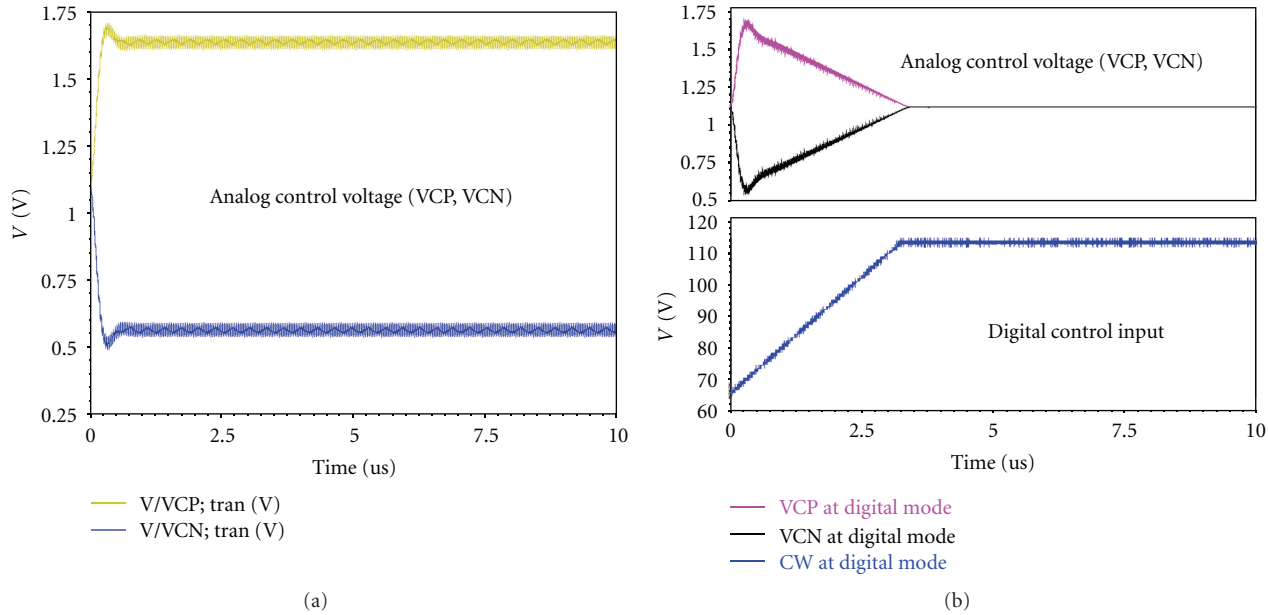


Figure 10: Simulated transient settling voltage: (a) with digital path disabled, and (b) with digital path enabled.

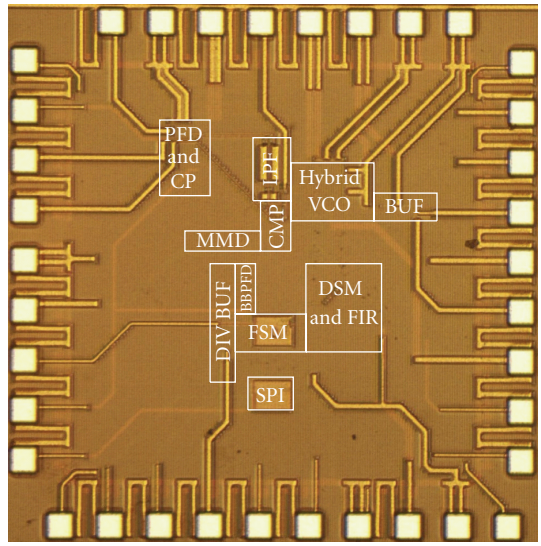


Figure 11: Chip micrograph [14].

digital path. When the digital path is not enabled, frequency acquisition is done only by the proportional-gain path, resulting in an analog type I PLL. As a result, large static phase error is observed when the PLL needs to track the frequency offset. With the digital path enabled, the frequency is tracked by the digital integration path. Consequently, the control voltage is settled within a very small range even with the frequency offset as shown in Figure 10(b), showing that the type II PLL is realized.

Figure 11 shows the micrograph of the test chip fabricated in 0.18 μm CMOS. The active core area is 0.6 mm^2 where only 0.01 mm^2 is occupied by the analog loop filter. Figure 12 shows the measured output spectra at 870 MHz frequency with the reference clock frequency of 30 MHz. The upper plot shows the output spectrum with the digital path disabled. Since the PLL becomes a type I PLL without the digital integration path, a large static phase offset is generated, resulting in the spur level as high as –30 dBc. When the digital integration path is enabled, the reference spur is reduced by more than 20 dB. Also, the DC control voltage range is settled within ±0.02 V when the digital path is enabled. The experimental results prove that the type-II PLL is realized with the hybrid loop control.

Since the phase noise contribution from the analog control path is worse than expected, it is difficult to see the effect of the hybrid FIR filter. Figure 13 shows the phase

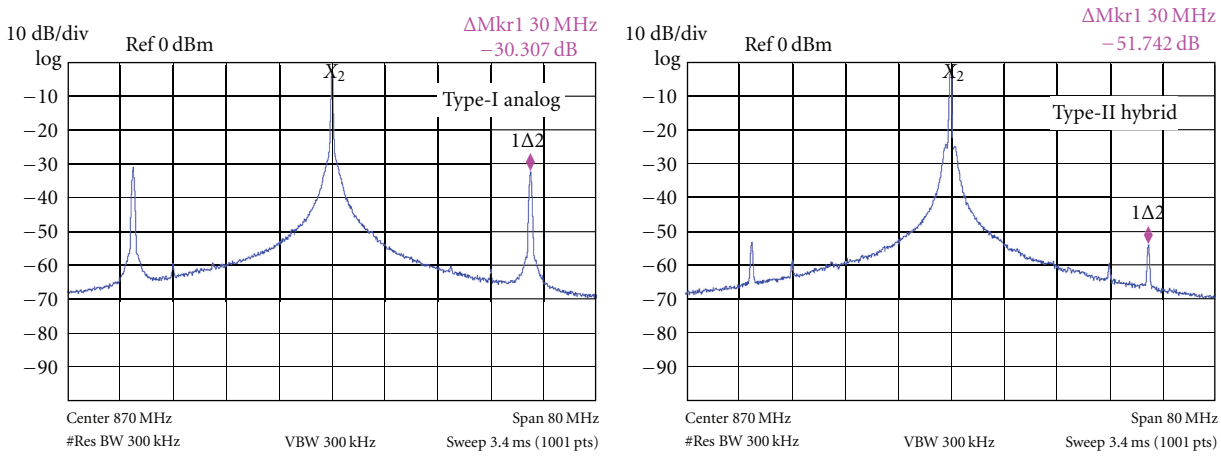


Figure 12: Measured output spectra: (a) with digital path disabled and (b) with digital path enabled.

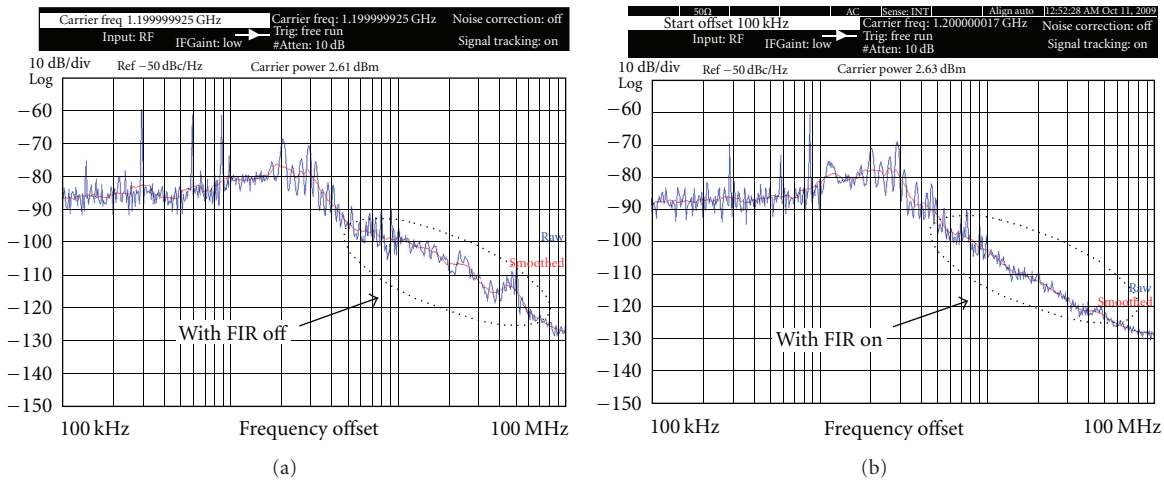


Figure 13: Measured output spectra: (a) with FIR disabled and (b) with FIR enabled.

Table 2: Measured performance summary [14].

Process	0.18 μm CMOS
Supply Voltage	1.8 V for analog, 1.5 V for digital
Power consumption	Total: 16.8 mW (Analog: 11.9 mW, Digital: 4.9 mW)
Occupied area	Active area: ~0.6 mm^2 (LPF < 0.04 mm^2)
VCO tuning range	790–925 MHz
Reference clock	30 MHz
Reference spur	< −52 dBc
Phase noise	< −81 dBc/Hz
Integrated RMS noise	100 kHz~100 MHz: 12.6$^\circ_{\text{rms}}$ 10 MHz~100 MHz: 1.1$^\circ_{\text{rms}}$

noise performance of the SDPLL output from the other test site, in which the hybrid FIR filter embedded in the D/VCO clearly reduces the high-frequency noise caused by the Δ-Σ modulation.

4.2. 65 nm CMOS SDPLL for Two-Point Modulation. The SDPLL architecture can be further extended to accommodate two-point phase modulation for RF transmitter systems, which has been well demonstrated by the ADPLL in the literature [1]. Figure 14 shows a simplified block diagram of the fractional-N SDPLL having the two-point modulation feature for GSM/GPRS applications. Similar to the ADPLL, the DCO gain can be calibrated easily by measuring the frequency step for the 1-LSB change since phase modulation is done in the digital domain with the DCO input control. Also, the group delay mismatch can be controlled to a certain degree by embedding the high-frequency DFFs in the FSM. Since the noise transfer functions of the DCO and the fractional-N divider are still controlled by the PLL loop dynamics, the use of the PFD and the CP offers linear control. Without using the TDC, overall power consumption

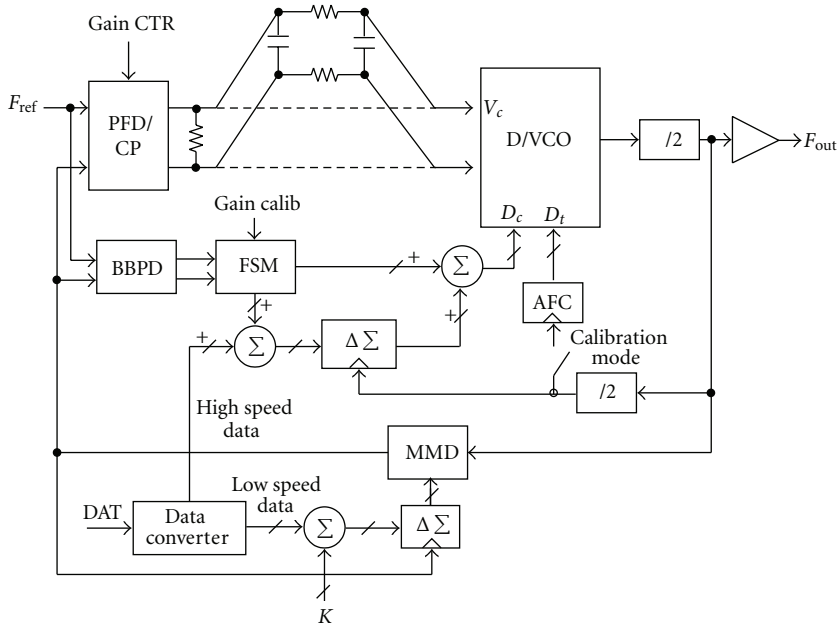


Figure 14: SDPLL with two-point modulation for RF transmitter systems.

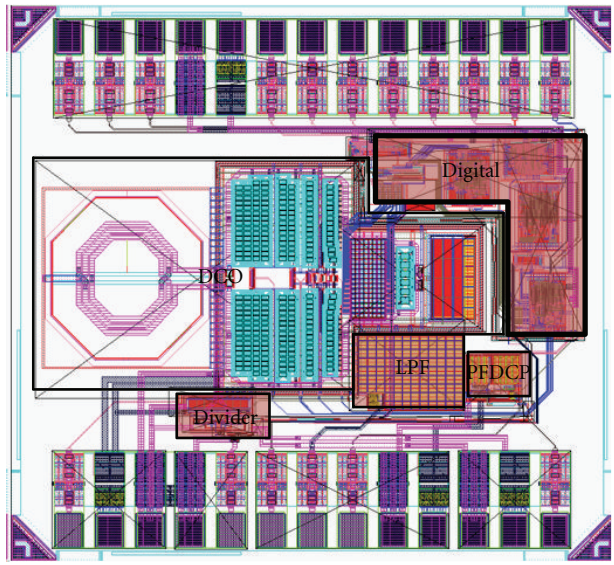


Figure 15: SDPLL layout in 65 nm CMOS (active area: 0.52 mm^2).

of the SDPLL can be further reduced while the total area is comparable to the ADPLL.

Figure 15 shows a layout of the SDPLL in 65 nm CMOS, occupying the active area of only 0.52 mm^2. The active area is much smaller than that of the conventional analog PLL and comparable to that of the ADPLL. Except the ΔΣ modulator and high-frequency control blocks, most digital operations for the two-point modulation are realized by external control with FPGA. Figure 16 shows power consumption analysis of the SDPLL based on postlayout simulation results. The D/VCO consumes nearly 80% of the total power. The power contribution of the PFD and the CP is less than 5% of the total power, showing that the SDPLL can save more power than the ADPLL by not employing the power-hungry TDC.

5. Conclusion

In this paper, some design issues in recent clock generation systems are reviewed and the SDPLL is presented as a low-power technology-friendly architecture. We also show that

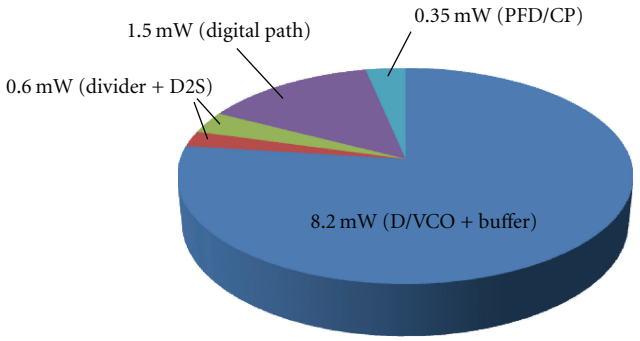


Figure 16: Power consumption analysis.

the SDPLL architecture can be further tailored for various applications without necessarily requiring advanced CMOS technology.

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