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Research Article

A Low-Power and Low-Voltage Power Management Strategy for On-Chip Micro Solar Cells

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Fundamental characteristics of on-chip micro solar cell (MSC) structures were investigated in this study. Several MSC structures using different layers in three different CMOS processes were designed and fabricated. Effects of PN junction structure and process technology on solar cell performance were measured. Parameters for low-power and low-voltage implementation of power management strategy and boost converter based circuits utilizing fractional voltage maximum power point tracking (FVMPPT) algorithm were determined. The FVMPPT algorithm works based on the fraction between the maximum power point operation voltage and the open circuit voltage of the solar cell structure. This ratio is typically between 0.72 and 0.78 for commercially available poly crystalline silicon solar cells that produce several watts of power under typical daylight illumination. Measurements showed that the fractional voltage ratio is much higher and fairly constant between 0.82 and 0.85 for on-chip mono crystalline silicon micro solar cell structures that produce micro watts of power. Mono crystalline silicon solar cell structures were observed to result in better power fill factor (PFF) that is higher than 74% indicating a higher energy harvesting efficiency.

1. Introduction

Sensors that can work in isolated environments for extended duration are demanded by many modern sensor applications. Typically, it is very hard to access these sensors to replace power sources. One example of such sensor applications is implantable biomedical devices such as retinal prosthesis. In such cases accessing the sensor requires surgery. Even very low-power, low-leakage, and energy-efficient systems are limited by the finite energy stored on a battery. Alternative means of powering sensors such as inductive coupling and transmission of power through RF waves are used to overcome limitations of batteries [1–4]. Increasing power transfer efficiency in both methods requires high directivity and large coils/antennas. Moreover, these are not suitable for long range applications [4].

Energy autonomous sensor systems capable of generating their own energy by harvesting ambient energy in the environment to completely eliminate the need for a power source or at least assist it have gained significant interest in recent years. Photovoltaic energy conversion is a viable choice for on-chip energy harvesting due to its high conversion efficiency and compatibility with CMOS manufacturing processes [5, 6]. Fortunately, the level of illumination indoors and outdoors is sufficient for generating micro watts of power if the light energy is harvested efficiently. Furthermore, integrating energy harvesting capability into sensor chip enables reducing the system cost and volume.

Energy harvesters presented are arrays of on-chip micro solar cells (MSCs) composed of PN junction photodiodes that can be built using readily available layers in CMOS processes. Three different MSC structures built with different CMOS layers in three different CMOS manufacturing processes are studied in order to observe the structural and manufacturing effects on the MSC performances.

Power generating PN junction MSCs have voltage-current characteristics varying nonlinearly with load conditions and illumination levels. Therefore, it is necessary to operate the photodiodes at a point that they will deliver the maximum power. This study presents experimental results

showing that a very simple and power efficient method can be employed to operate the on-chip photodiode MSCs at the maximum power point (MPP).

2. Energy Harvesting with On-Chip MSCs

When a photon is absorbed by a semiconductor material, an electron hole pair is generated. The electron and hole eventually recombine unless they are separated. The built-in electric field in the depletion region of PN junctions is used for separating electrons from holes. Drift of photo-generated minority carriers across the depletion region results in a photo generated current flowing from N-region to P-region of the junction. The photo generated current is given by the following [7]:

$$I_{\text{ph}} = A \cdot J_{\text{ph}} = A \cdot \left(q \cdot G \cdot \left(L_{\text{N}} + W_D + L_{\text{P}}\right)\right). \quad (1)$$

Here, A is the junction area, G is the carrier generation rate proportional to illumination level, W_D is depletion layer width, and L_{P} and L_{N} are diffusion lengths of holes and electrons, respectively. Since the electric field is zero outside of the depletion region, only the carriers generated in the depletion region and those carriers that can diffuse to the depletion region are separated by the internal electric field. Therefore, more carriers can be separated in materials with wider depletion regions and longer diffusion lengths.

A net positive charge builds up on the P-region and a net negative charge builds up on the N-region of the photodiode as the photo generated carriers flow across the depletion layer unless an external circuit removes the excess charge. Therefore, the P-region of an illuminated photodiode is at a higher potential than that of the N-region. This potential difference lowers the built-in potential of the PN junction. When potential barrier is lowered, diffusion current flows from P-region to N-region of the junction. This is identical to the diffusion current resulting from an external positive bias. Output current (I_{out}) of a photodiode is the difference between the photo generated current and the forward diode current. I_{out} is given by

$$I_{\text{out}} = I_{\text{ph}} - I_f = I_{\text{ph}} - I_S \cdot \left(e^{V_{\text{out}}/nV_T} - 1\right). \quad (2)$$

Here I_f is the forward current, I_{ph} is the photo generated current, V_{out} is the voltage across the PN junction, V_T is the thermal voltage, n is the diode ideality factor, and I_S is the reverse saturation current of the junction. This equation suggests a first order photodiode model composed of an ideal current source and an ideal diode. Models based on measurements suggest additional shunt and series resistances [8]. Relations derived using this first order equation are accurate enough and added parasitics are ignored in this section for simplicity.

When no external circuit is connected between the terminals of a PN junction photodiode, no net current flows. The forward current due to the potential barrier lowering and photo generated current are equal. The potential difference between the terminals in this condition is known as open circuit voltage (V_{oc}) and can be calculated using (2) for $I_{\text{out}} = 0$ as shown in

$$V_{\text{oc}} = nV_T \cdot \ln\left(\frac{I_{\text{ph}}}{I_S} + 1\right). \quad (3)$$

V_{oc} has a logarithmic dependence on light level unlike linear dependence of photo current (I_{ph}) on light level. Output power is the product of output voltage and current. V_{out} corresponding to maximum power output (V_{MPP}) can be calculated by setting the derivative of power (P_{out}) to zero and is given in

$$V_{\text{MPP}} = nV_T \cdot \left[\ln\left(\frac{I_{\text{ph}}}{I_S} + 1\right) - \ln\left(1 + \frac{V_{\text{MPP}}}{nV_T}\right)\right]. \quad (4)$$

Since I_{ph} is linearly proportional to light level and V_T is proportional to temperature, V_{MPP} depends on light level and temperature. The relation between V_{MPP} and V_{oc} is obtained substituting (3) into (4) and is given in

$$V_{\text{oc}} = V_{\text{MPP}} + nV_T \cdot \left[\ln\left(1 + \frac{V_{\text{MPP}}}{nV_T}\right)\right]. \quad (5)$$

The logarithmic curve defined by (5) is relatively linear when V_{MPP} changes a few hundred millivolts. Since V_{oc} increases less than 100 mV for large changes of illumination, a very linear dependence is expected. Measurements confirm that ratio between V_{oc} and V_{MPP} is fairly constant over a wide range of illumination levels. This observation is the basis of fractional voltage maximum power point tracking (FVMPPT) method proposed for on-chip power management [9].

2.1. On-Chip Micro Solar Cell (MSC) Structures. Several different types of PN junction photodiodes can be built using combinations of P-substrate (P-sub), n+ diffusion (n+ diff), p+ diffusion (p+ diff), P-well, and N-well layers in standard CMOS process. Since P-sub is always connected to ground potential in N-well CMOS processes, junctions built with P-sub are suitable only for generating negative voltages on cathode side of the micro solar cell (MSC) structures.

The three MSC structures investigated in this study are shown in Figure 1. Two of them (MSC1, MSC2) generate positive output voltage while the third one (MSC3) generates negative output voltage. First structure (MSC1) uses p+ diff/N-well junction for energy harvesting. It is built in 0.5 μm 2P3M process. Second structure (MSC2) uses P-well/N-well and P-well/n+ diff junctions in parallel. It is built in a 0.18 μm 1P6M process. Third structure uses P-sub/N-well and p+ diff/N-well junctions in parallel. It is built in 0.35 μm 2P4M process. Inevitable P-sub/N-well junction diode (PD1) in MSC1 and MSC2 is shorted since it cannot be used for energy harvesting in this configuration.

Depletion region width is wider if junctions are built with lightly doped semiconductors. Recombination rate of carriers in a semiconductor increases with increased doping concentration. Therefore, diffusion lengths are longer in lightly doped semiconductors. Substrate and wells have lower doping concentrations compared to diffusion layers.

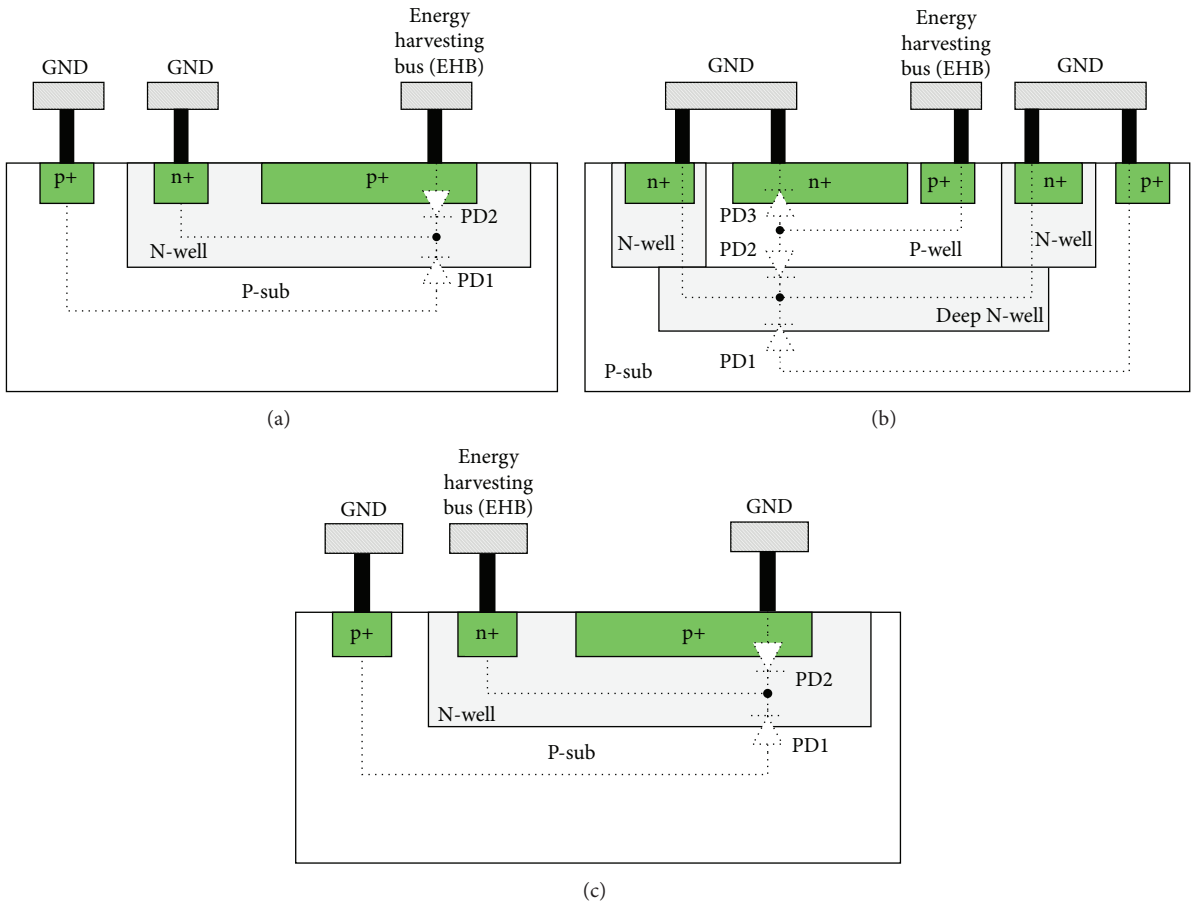

Figure 1: Three on-chip micro solar cell structures (a) MSC1, (b) MSC2, and (c) MSC3.

Moreover, well layers have much deeper sidewalls compared to diffusion layers resulting in larger junction area for same silicon area. Therefore, junctions built with diffusion layers are expected to generate the smallest photo generated current due to high doping concentration on diffusion side and smaller sidewall areas.

Measurements have confirmed that MSC1 using only the shallow diffusion junction for energy harvesting has the lowest energy generating capacity as expected. Even though both MSC2 and MSC3 use a shallow junction in parallel with a deep junction for energy harvesting, MSC3 generates three times larger power than that of the MSC2. P-well/N-well junction generates less current compared to P-sub/N-well junction since isolated P-well region has higher doping compared to substrate region. Moreover, second structure is built in 0.18 μm process. Doping levels are increased as feature size shrinks in CMOS processes [10]. Therefore, depletion region widths and diffusion lengths are shorter in all layers in second structure compared to other structures. This proves that mature processes are more suitable for on-chip solar cell structures. Since shorting parasitic photodiode does not remove the depletion region, parasitic photodiode collects portion of carriers generated in N-well region that could otherwise be collected by the desired photodiodes further reducing the energy generation capacity in MSC1 and MSC2 structures.

3. Low-Power Low-Voltage FVMPPT Circuit

Since on-chip micro solar cells have limited output power, it is important to operate the solar cell at the maximum power point. However, MPPT circuits themselves consume power and power consumption increases with increased tracking circuit complexity. Naturally, it is desired to minimize MPPT circuit power consumption, so that it does not reduce the overall power efficiency of the energy harvesting system. The FVMPPT method can be implemented with very simple circuits while other MPPT methods require complicated sensing and control circuits. Therefore, FVMPPT circuits are the most energy efficient MPPT circuits [11].

MPPT circuits based on FVMPPT method are very simple to implement. The voltage fraction is determined by measurements under various illumination levels. The MPPT circuit adjusts the load to keep the output voltage of solar cell equal to the appropriate predefined fraction of open circuit (V_{oc}). Since the voltage fraction (k_v) changes with illumination and temperature, a predefined k_v value will be

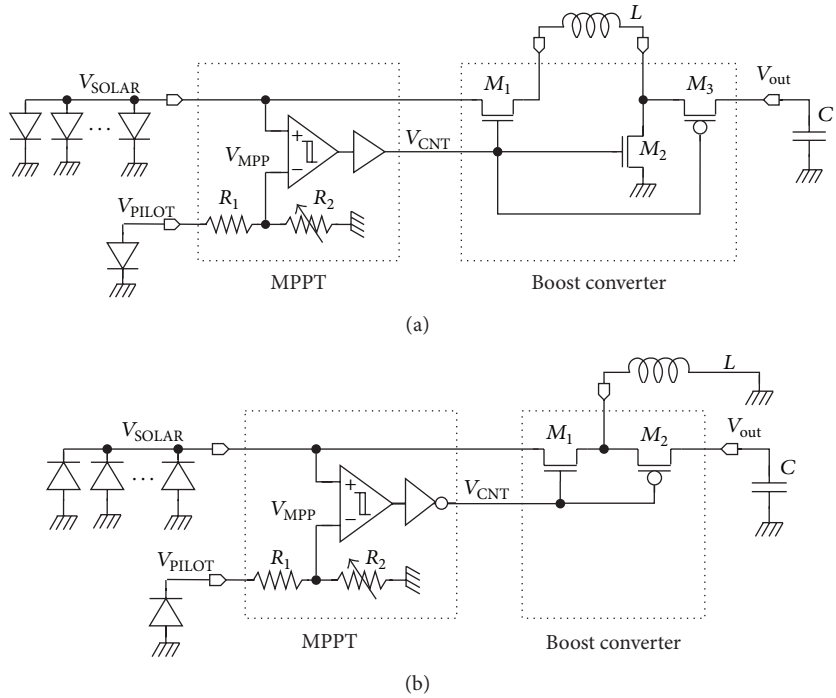

Figure 2: Implementation of self-clocked boost converter integrated with fractional voltage MPPT circuit: (a) noninverting topology, (b) inverting topology.

just an approximation. Thus, FVMPPT circuit is not a true-MPP tracking circuit. The solar cell operating point will miss the MPP slightly when illumination and temperature drift during operation. The solar cell output power will be slightly less than the maximum available.

Measurements have shown that output power is relatively flat in vicinity of maximum power point. Deviation of solar cell output power from the maximum power is less than 5% when k_v values change by 10%. Therefore, output power from a solar cell driven by a FVMPPT circuit will provide more than 95% of maximum power even if predefined k_v was significantly off. Therefore, power loss due to wrong preset k_v is insignificant and using FVMPPT is justified.

3.1. FVMPPT Implementation. MPPT circuits consuming less than 1 mW used to be considered very impressive [12]. Nowadays, advanced CMOS manufacturing processes made it possible to realize MPPT circuits using digital control consuming less than 1 μW [13]. Therefore, relatively complicated MPPT circuits could be integrated with micro solar cell arrays producing only a few microwatts of power. FVMPPT method based MPPT circuits proposed in this work consume very low power and very small silicon area due to its simple circuit topology without complicated digital control circuitry.

The low-power on-chip MPPT circuit proposed in this study is implemented using a pilot solar cell, a comparator, and a 4-bit digitally programmable resistive voltage divider as shown in Figure 2. MPPT and DC-DC converter circuits are integrated together resulting in a very simple overall harvester circuit. Solar cells are connected directly to boost converter input, so additional interface circuits between solar cell and boost converter reducing power efficiency are avoided. Power is dissipated by the low-power comparator and nonzero resistances of inductor and transistors only. Reducing the switch resistances is the key for higher efficiency.

The open circuit voltage (V_{oc}) is generated by a pilot solar cell structure constructed using the same CMOS layers used for building the energy harvesting photodiodes so that pilot cell and energy harvesting photodiodes have the same open circuit voltage. A resistive voltage divider is used for generating the appropriate fraction of pilot cell output voltage (V_{PILOT}). Resistor string is implemented with a very large on-chip resistor string so that the current drawn from the pilot cell is much smaller than the short circuit current of the pilot cells. Ideally, pilot cells should not be loaded so that pilot cell output voltage (V_{PILOT}) is equal to the open circuit voltage. Deviation of V_{PILOT} from V_{oc} is insignificant for small output currents due the logarithmic dependence of photodiode voltage on the output current. Since resistive chain is programmable, resistive division ratio (k_R) can be adjusted to include the deviation of V_{PILOT} from V_{oc}. The required value k_R is given in

$$k_R = k_v \times \frac{V_{oc}}{V_{PILOT}}. \quad (6)$$

The MPPT block comparator continuously monitors whether magnitude of V_{SOLAR} is larger than magnitude of V_{MPP} and generates a control/clock output (V_{CNT}) controlling the boost converter. Comparator functions as an asynchronous control signal generator for the boost converter.

Since boost converter is the load for the solar cell array, comparator controls the amount of current sourced from the solar cell array by controlling the switching speed of the boost converter and forces the solar cells to operate at maximum power point optimizing harvesting efficiency. Boost converter is integrated with the MPPT circuit without any auxiliary circuits in between.

3.2. Boost Converter. Since the output voltage of a solar cell is not sufficient for running analog and digital circuits, DC-DC conversion is necessary for generating the appropriate supply voltage. Boost converters are used for DC-DC conversion of on-chip solar cell outputs in the proposed structures. Noninverting boost converters are used with MSC1 and MSC2 while an inverting boost converter is used with MSC3. When input transistor M1 in both boost converter types is turned on, the solar cell current flows through the off-chip inductor to/from ground. Magnitude of output voltage of solar cell (V_{SOLAR}) drops as the solar cell current increases. When V_{SOLAR} drops one hysteresis voltage below V_{MPP}, the MPPT comparator turns the NMOS switch(es) off and turns the PMOS switch on. When M1 turns off, magnitude of V_{SOLAR} voltage increases towards open circuit voltage. At this moment, the solar cell is disconnected from boost converter and inductor is connected to the storage capacitor. Since the inductor current cannot change instantly, the inductor will go on supplying a decaying current to the storage capacitor. Thus, the solar energy stored in the EMF of the inductor is transferred to large external charge store capacitor. V_{SOLAR} voltage magnitude increases since M1 is off. When it raises one hysteresis voltage above V_{MPP}, the output of MPPT comparator is toggled starting a new cycle. This operation continues indefinitely charging the V_{OUT} node voltage higher with maximum efficiency. The switches in the boost converter are driven by MPPT circuit. This integrated topology requires no clocks to drive the switches, so the circuit ends up being very simple compared to synchronous DC-DC converters.

4. Measurement Results

The three MSC structures investigated in this study were fabricated in three different CMOS processes. MSC1 is fabricated in a 0.5 μm, 2P3M CMOS process. MSC2 is fabricated in a 0.18 μm, 1P6M CMOS process. MSC3 is fabricated in a 0.35 μm, 2P4M CMOS process. Raw measurement data for the 3 different micro solar cell (MSC) structures is shown in Table 1. Output current and voltage of each micro solar cell is measured for a wide range of illumination conditions typically between 1 Klux and 60 KLux. Measurements are normalized for 1 mm^2 solar cell area for comparison purposes.

4.1. Energy Harvesting Measurements. Figure 3 shows the measured generated power per unit area versus illumination level for the three MSCs. Measurements confirm that MSC1 using shallow junctions only has the smallest power generation capacity. MSC2 has 3x to 5x better energy harvesting capability than the MSC1. MSC3 produces much larger power which is 10x to 20x better than the MSC1.

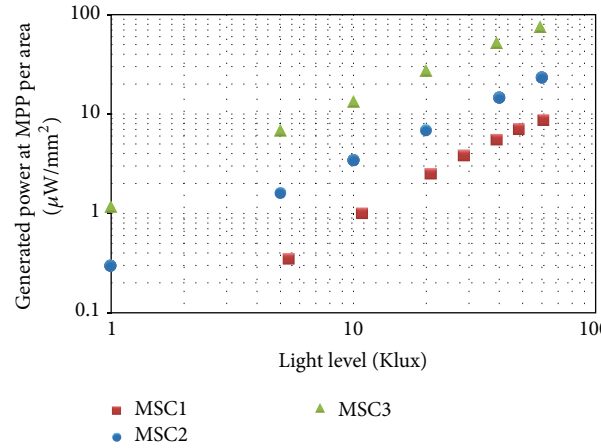

Figure 3: Measured generated power per unit area versus illumination level.

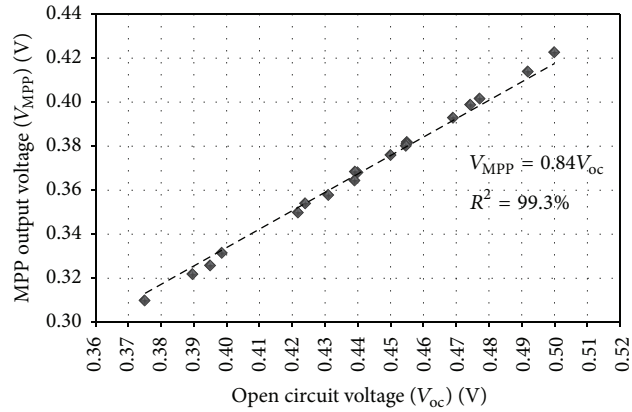

Figure 4: Measured maximum power point voltage versus open circuit voltage.

Power fill factor (PFF) is the ratio of maximum output power to the product of short circuit current and open circuit voltage. PFF is the product of voltage and current fractions. PFF is a measure of how close a solar cell can get to ideal. Therefore, a larger PFF means higher energy conversion efficiency for a solar cell. Since higher voltage fraction leads to higher PFF, on-chip micro solar cells have better energy conversion efficiency than solar cells with smaller k_v. Measured PFF of all 3 MSC structures is larger than 74% for all illumination conditions. A solar cell with k_v value of 0.73 will have PFF less than 0.7 since k_I cannot be 1.

4.2. Voltage Fraction Measurements. Measurements have shown that voltage fraction k_v is fairly constant between 0.82 and 0.85 for varying illumination conditions as shown in Table 1. If MPP output voltages (V_{MPP}) of all three structures at all measured illuminations are plotted against their open circuit output voltages (V_{oc}) and a first order linear regression line is fit, the k_v turns out to be 0.84 with 99.3% accuracy as shown in Figure 4. This observation suggests that if a predefined fixed k_v value of 0.84 is used for a FVMPPT

Table 1: Raw measurement results of the MSCs under different illumination conditions.

Structure	Light (KLux)	V_{oc} (V)	I_{sc} (μA)	V_{MPP} (V)	I_{MPP} (μw)	P_{MPP} (μW)	k_v	k_I	PFF
MSC1	5.4	0.3750	1.194	0.310	1.150	0.356	0.827	0.963	0.796
MSC1	10.8	0.3950	3.084	0.326	3.097	1.010	0.825	1.004	0.829
MSC1	21.0	0.4240	7.716	0.354	7.165	2.536	0.835	0.929	0.775
MSC1	28.6	0.4310	11.574	0.358	10.870	3.892	0.831	0.939	0.780
MSC1	39.1	0.4400	16.498	0.368	15.159	5.579	0.836	0.919	0.769
MSC1	48.1	0.4500	20.760	0.376	19.077	7.173	0.836	0.919	0.768
MSC1	60.7	0.4550	25.274	0.382	23.291	8.897	0.840	0.922	0.774
MSC2	1.0	0.3984	0.988	0.332	0.900	0.298	0.832	0.911	0.758
MSC2	5.0	0.4392	4.894	0.368	4.448	1.639	0.839	0.909	0.763
MSC2	10.0	0.4548	9.841	0.381	8.971	3.420	0.838	0.912	0.764
MSC2	20.0	0.4743	19.848	0.399	17.466	6.966	0.841	0.880	0.740
MSC2	40.0	0.4918	38.821	0.414	35.614	14.742	0.842	0.917	0.772
MSC2	60.0	0.4999	60.623	0.423	55.674	23.529	0.845	0.918	0.776
MSC3	1.0	0.3896	4.008	0.322	3.728	1.200	0.826	0.930	0.768
MSC3	5.0	0.4218	21.434	0.350	19.708	6.896	0.830	0.919	0.763
MSC3	10.0	0.4389	39.596	0.364	36.915	13.454	0.830	0.932	0.774
MSC3	20.0	0.4546	78.005	0.380	72.667	27.628	0.836	0.932	0.779
MSC3	39.0	0.4690	146.191	0.393	135.189	53.137	0.838	0.925	0.775
MSC3	59.0	0.4772	205.513	0.402	188.736	75.796	0.842	0.918	0.773

circuit, it would be accurate enough for a very wide range of illumination conditions. This value would be valid for all three manufacturing processes.

4.3. Fractional Voltage Sensitivity. Measurements have shown that on-chip micro solar cells built in three different CMOS processes all have ratio of output voltage of solar cell to open circuit voltage (V_{out}/V_{oc}) in the range between 0.82 and 0.85. Sensitivity of the harvesting efficiency was measured by setting voltage fraction k_v between 0.74 and 0.88 with 0.2 steps while changing the light level between 1 Klux and 60 Klux. Figure 5 shows sensitivity of power output of MSC structures to variations in V_{out}/V_{oc}. It shows that the energy harvesting efficiency does not suffer drastically for such a wide variation in V_{out}/V_{oc} value and more than 92% of maximum available power is delivered for any illumination condition. These measurements also verify that the simple FVMPPT circuit will harvest maximum power even if preset k_v is set to a wrong value.

Intervals where output power deviates from maximum power point by less than 5% and 10% were also determined for each illumination level. Measurements show that all three structures deliver more than 90% of maximum power as long as k_v is set between 0.72 and 0.90 for all measured illumination levels. Output power is more than 95% of maximum power for all illumination levels when k_v is between 0.76 and 0.88.

4.4. Fractional Voltage Trends. Voltage fractions of the three structures are plotted against open circuit voltage as shown in Figure 6 to see how individual structures behave. MSC1 k_v values have widest spread while MSC2 has the narrowest spread. Measured k_v values increase with illumination as expected. Overall general trend of the k_v with respect to V_{oc} is given in

$$k_v = 0.15 \cdot V_{oc} + 0.77. \quad (7)$$

4.5. Boost Converter Measurements. Boost converter efficiencies and power consumption of harvester circuits are shown in Table 2. Efficiency of boost converter as the ratio of output power to input power and efficiency of harvester considering the power consumption of comparator are provided. Harvester efficiency is calculated using the actual input power. However, since MPPT circuit is not perfect, input power is not equal to maximum available power. Tracking efficiency is the ratio of input power to the maximum power available from solar cell and end to end efficiency is product of tracking efficiency and harvester efficiency. Proposed harvesters can provide more than 50% of the maximum power available from the on-chip solar cells when input power is around 20 μW. 29% end to end efficiency is achieved for only 7.35 μW input power. Satisfactory performance is achieved to prove that this simple harvester structure can be integrated with on-chip solar cells to harvest energy with highest efficiency. However, boost converter efficiency is not as high as recently reported boost converters [13–17]. Boost converter efficiency decreases as input power decreases. Therefore, efficiency of proposed harvesters is expected to be lower than boost converters with larger input power. Efficiency can be increased up to a certain level using larger switches to reduce channel resistances. Since larger switches will have larger parasitic capacitances, power dissipation of comparator will increase proportional to switch size [18]. Transistor sizes and comparator driving capacity should be optimized to achieve maximal efficiency. Moreover, special analog I/O pads should be designed to prevent losses due to leakages and capacitive

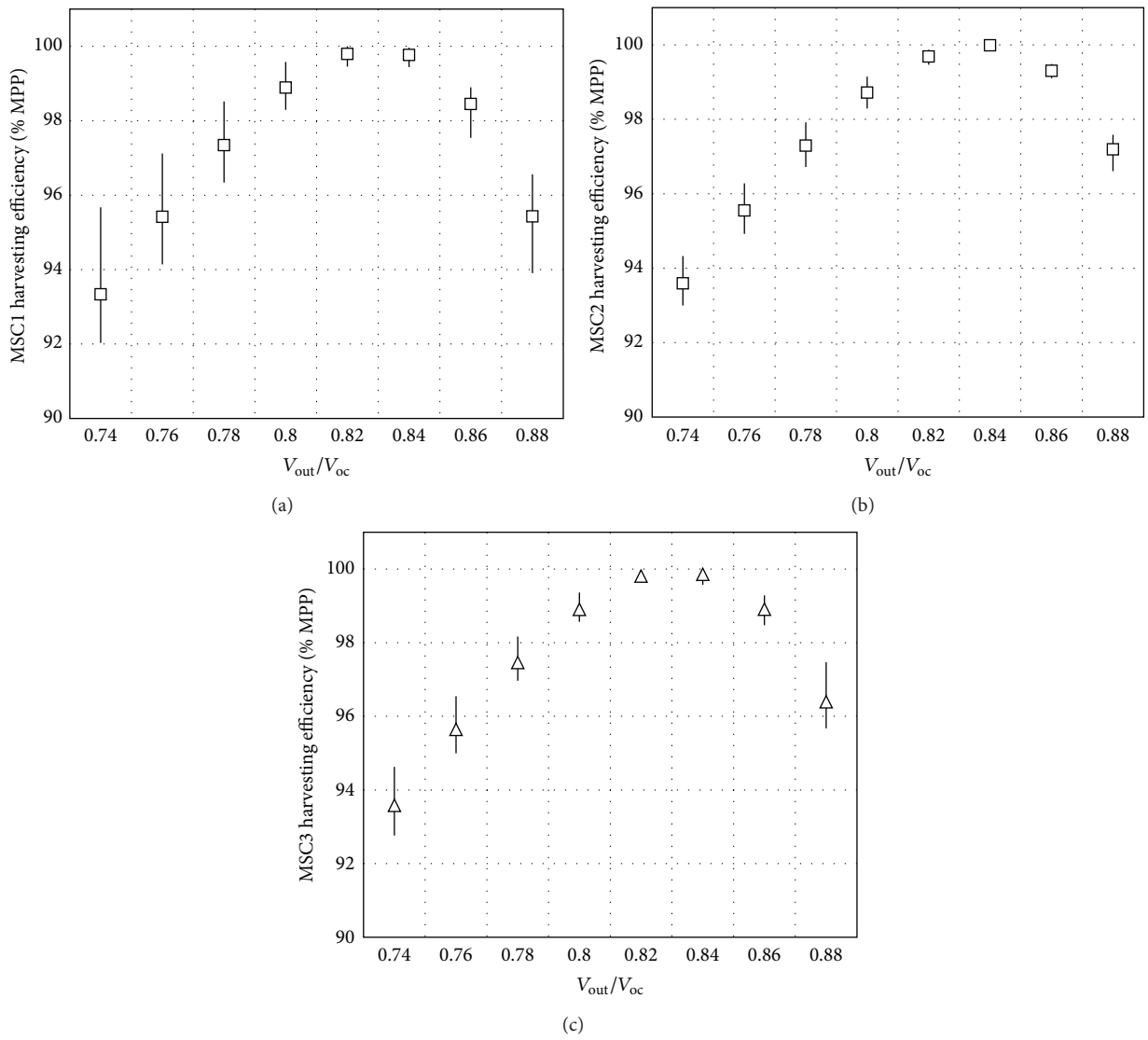

Figure 5: Measured sensitivity of energy harvesting efficiency of MSC structures when ratio of output voltage of solar cell to open circuit voltage (V_{out}/V_{oc}) varies between 0.74 and 0.88, (a) MSC1, (b) MSC2, and (c) MSC3.

loading. Since same channel resistance can be achieved with smaller parasitic capacitances, higher efficiency can be achieved in advanced CMOS processes.

5. Conclusion and Discussions

On-chip micro solar cell (MSC) structures built using available layers in three different CMOS processes were designed and fabricated. The MSC structures were integrated with MPPT and boost converter circuits. Proposed structure is the first DC-DC converter topology with built in MPPT algorithm integrated with on-chip solar cells producing a few microwatts of power. Measurements showed that on-chip solar cells could generate up to 13.5 μW/mm^2 under normal outside daylight illumination condition (10 Klux) and around 1.2 μW/mm^2 under indoor illumination condition (1 Klux).

Effects of PN junction structure and process technology on solar cell performance were characterized. Measurements have shown that ratio of solar cell voltage providing maximum power (V_{MPP}) to open circuit voltage (V_{oc}) is relatively constant despite varying illumination levels and manufacturing processes. Voltage fraction (k_v) is typically between 0.72 and 0.78 for commercially available poly crystalline silicon solar cells that produce several watts of power under typical daylight illumination. Measurements showed that k_v is relatively constant between 0.82 and 0.85 for integrated mono crystalline silicon micro solar cell structures despite varying illumination levels and manufacturing processes. Higher k_v results in a power fill factor (PFF) higher than 74% in monocrystalline solar cells. Higher PFF means monocrystalline solar cells have higher energy harvesting efficiency. Therefore, on-chip energy harvesters with high

Table 2: Comparison of efficiency of proposed boost converters to previously reported boost converter based energy harvesters.

Parameter	Reference [13]	Reference [14]	Reference [15]	Reference [16]	Reference [17]	This work		
						MSC1	MSC2	MSC3
Input voltage range (Volt)	0.33–3.0	0.04–0.30	0.5	0.15–0.75	0.5–2.0	0.30–0.38	0.33–0.42	0.32–0.40
Energy harvesting source type	Photovoltaic	Thermoelectric	Photovoltaic	Photovoltaic	Photovoltaic	Photovoltaic	Photovoltaic	Photovoltaic
Managed power (P_{in}) (μW)	100	4,430	108	1,100	10,000	25.9	23.7	32.8
Boost converter efficiency	61.0%	NA	NA	87.0%	87.0%	59.2%	62.3%	64.5%
Controller power cons. ($P_{control}$) (μW)	NA	0.4	0.41	5.0	2.1	1.35	0.91	1.12
Harvester overall efficiency	NA	83.0%	78.9%	86.5%	87.0%	54.0%	58.4%	61.1%
Tracking efficiency (P_{in}/P_{MPP})	NA	NA	NA	96%	80%	96%	94%	97%
End to end harvesting efficiency	NA	83.0%	78.9%	83.0%	70.0%	51.8%	54.9%	59.2%

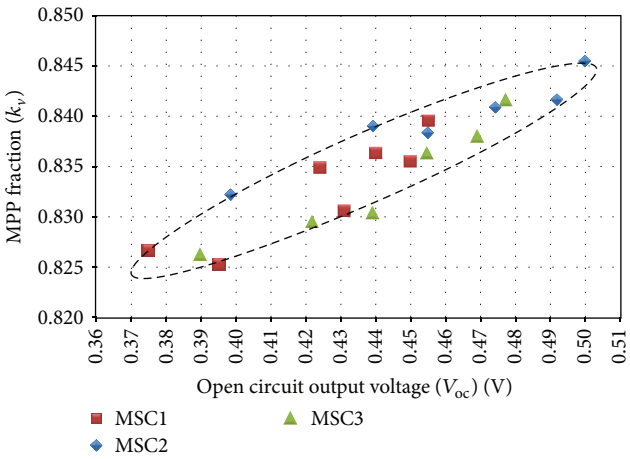

Figure 6: Variation of maximum power point voltage to open circuit voltage ratio (k_v) with open circuit voltage for different structures.

energy conversion efficiency are shown to be a reliable power source for powering on-chip sensors.

Moreover, measurements have shown that output power has relatively low sensitivity for variations in solar cell operating voltages. A preset k_v value provides output power close enough to maximum power even when actual k_v value changes with illumination and temperature.

Fractional voltage maximum power point tracking (FVMPPT) algorithm making use of the relatively constant voltage fraction can be used for harvesting maximum power from solar cells. Designing low-power and low-voltage power management system is possible using FVMPPT algorithm. Power lost by FVMPPT method is insignificant compared to the extra power that will be consumed by more complicated MPPT circuits.

Integrated MPPT-boost converter topology is shown to be very effective with very low power consumption compared to previously reported energy harvester structures. MPPT-boost converter topologies consume only 0.91–1.35 μW power. Boost converter efficiency is around 60% for larger input power.

Conflict of Interests

The authors declare that they have no financial or personal relationships with other people or organizations that can inappropriately influence their work; there are no professional or other personal interests of any nature or kind in any product, service, and/or company that could be construed as influencing the position presented in or the review of the paper.

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