Transmission Line Modeling for the Purpose of Analog Power Flow Computation of Large Scale Power Systems

A Thesis

Submitted to the Faculty

of

Drexel University

by

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in partial fulfillment of the

requirements for the degree

of

Master of Science in Electrical Engineering

July 2005

ACKNOWLEDGMENTS

I would like to acknowledge and thank my advisor, Dr. Chikaodinaka Nwankpa, for all his help and guidance in the research and the development of this thesis. I also thank him for the opportunity to study and conduct research in the Center of Electric Power Engineering (CEPE). The facilities, faculty and students in CEPE all contribute to an environment that is very conducive to learning and conducting research. I am ever grateful for the opportunity to be a part of this organization.

I would also like to thank Dr. Miu, Dr. Halpin and Dr. Nagvajara for serving on my thesis committee. I am appreciative for their expertise, participation in my graduate studies and their time dedicated to reviewing and commenting on this work.

Finally I would like to express gratitude to Jeffrey Yakaski, Anthony Deese, Qingyan Liu and Michael Olaleye for their help and participation in the PowerGrid research project. Their valuable work has assisted me in my research efforts and made much of the work in this thesis possible.

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ABSTRACT

Transmission Line Modeling for the Purpose of Analog Power Flow Computation of Large Scale Power Systems

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This thesis proposes methods for modeling electric power transmission lines for the purpose of analog power flow computation of power system networks. Theoretical and applicable circuit models for analog transmission lines are presented with a focus on power-flow studies which concentrates on the steady state or static behavior of electrical power transmission lines. With this approach the wave propagation and reflection is not as much of a concern as the steady state line voltages and current flows. Because of this lumped circuit equivalent line models are utilized. The primary goal is to develop a computational alternative for power system analysis that overcomes obstacles currently faced by traditional digital computation methods. Analog computation is proving to be a viable alternative and has notable advantages over digital computers. In order to contrive a practical analog emulator precise models for power system components are required. Specifically this thesis develops a realization of an electric power transmission line model for such a purpose.

The transmission line model traditionally utilized in power-flow computation is a lumped parameter pi-model equivalent circuit. In digital computation the shunt elements and sometimes the series resistances are often times neglected in order to simplify the power flow equations and subsequently speed up the calculation times. Prior research in analog computation for power flow analysis also utilized these simplified line models. A fully reconfigurable pi-model is presented here for an analog computation approach. No

components have been neglected resulting in a more accurate line model with fast computation times. The ability to remotely reconfigure each component on the line model makes this model universal. The design could easily be fabricated to an integrated circuit to represent a large scale network and configured to match a real world system. In addition, the model is easily expanded to form a distributed parameter line model by interconnecting multiple components in series. This allows for computational analysis of the power system states throughout the transmission line which is traditionally not done in digital power flow computation due to computational restraints.

1 INTRODUCTION

1.1 OVERVIEW

Analog computation of power systems is a continuing field of research. Among the advantages analog computation possesses over traditional digital methods are physically realizable solutions and much faster computation times. In order to consummate this analog method as a viable tool in power system analysis accurate models of power system components are required. This thesis explores and presents various reconfigurable transmission line models for a specific analog computation methodology.

Currently power-flow computation for large power systems is time intensive. The calculations are non-linear in nature and lengthy iteration schemes are the currently preferred solution. This presents a problem as many assumptions and simplifications are required to solve the equations with digital methods in a timely manner. In addition, expansion of the power grid, increasing necessity and complexity of contingency studies and introduction of economic analyses are demanding further computational burden. Traditional digital methods are too slow to solve the aforementioned demands quickly. This affects the security, reliability and market operation of power systems. Ideally a real-time computation tool, or faster than real-time, is preferable, specifically in market activities and operation. Analog computation provides a viable alternative to traditional approaches to achieve this goal.

Analog power-flow computation has certain inherent advantages over digital computation. Conventional digital methods are expensive and slow in comparison to analog computers. The power-flow solution is obtained almost instantaneously

regardless of the number of components in the network with analog circuits. Analog methods achieve true parallelism in computation, the time to find a solution is independent of network size. Effectively the solution is obtained as quickly as the system stabilizes. Experimentation has shown the ability to calculate solutions even faster than power system phenomena occur in the real world. In prior research, simulation time for a two machine system were typically 10^4 times shorter than the real time simulated phenomena[1]. This is following the approach of modeling generator dynamics for the purpose of transient stability evaluation. Despite that an analog approach is certainly advantageous in some regards there are also barriers in this field and reasons why its use is not widespread today as digital techniques.

The modeling and design of analog components is one obstacle that must be overcome to take advantage of above-mentioned desirable attributes of analog computation. While analog solutions are not as precise as digital methods (measurement errors, noise, etc.) they have the capability to be much more accurate through more detailed modeling in analog hardware. Without clearly defined valid models for power system components this computational method cannot be realized. In addition, these models also must cater towards computational speed. Specifically in power system operation execution of multiple runs and contingencies is required extremely quickly. A priority for these analog models is to yield valid solutions while allowing fast reconfigurability. These problems have been addressed in the design of the transmission line models presented in this thesis. The models were designed based on a previously proposed DC emulation technique of power-flow computation which is reviewed and expanded upon in this thesis. Specifically this work presents a robust analog

transmission line model suitable for the development of a large scale power system emulator.

The work in this thesis is part of ongoing research efforts to develop a Power System on a Chip (PSoC). The vision is to realize this through a Very Large Scale Integrated (VLSI) circuit which is remotely configurable, or reconfigurable, and controllable. A graphical illustration for the development of a PSoC is shown in Figure 1 below[2]. Exploration into Analog Behavior Modeling (ABM), stage I, was conducted by M. Olaleye[2] and the work in this thesis concentrates on stage II and furthering development of the transmission line models for this application. The transmission line models presented here were fully developed in hardware and a prototype power system network was constructed and tested.

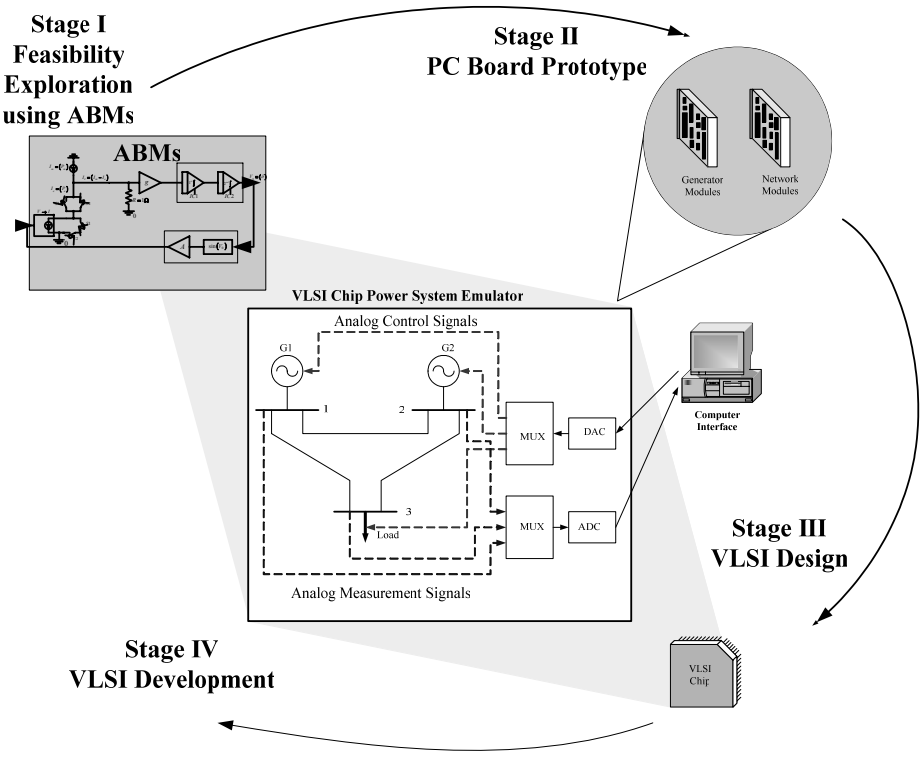

Figure 1: PSoC Development Process

Stage I was a study conducted to analyze the feasibility of analog computation for power system analysis without requiring development and construction of analog circuits and data acquisition. This task was accomplished through software simulation. Stage II encompasses the realization of the power system model in analog circuit form. Stages III and IV move this circuit realization into an end product of a VLSI chip.

The next section details some background, history and renewed interest of analog computational methods. In addition, inherent obstacles and limitations of analog computation are examined along with schemes to try and overcome them.

1.2 BACKGROUND

Analog computation in power systems is certainly not a new endeavor. AC Network Analyzers (NA) were first developed in the 1920's to model and solve problems associated with power distribution systems[3]. These analyzers were essentially miniaturized power systems built with passive components such as resistors, capacitors and inductors. Bell Telephone Laboratories (BTL), Massachusetts Institute of Technology (MIT), and the Office of Naval Research (ONR) all actively developed and researched analog computing applications at some point in time. Development and use of analog computation grew throughout the twentieth century until digital computers came into the mainstream in the 1970's. These digital methods became so popular for good reasons. They were much more precise and were easily programmable in comparison to their analog counterparts. The analog computers at that time required manual configuration of jumpers, potentiometers and other parameters for each computation. This required manual intervention and lengthy setup time for complex problems. Despite

these shortcomings up through the 1960's analog computers were commercially available and considerably successful and efficacious. Some examples of commercial analog computers can be seen in appendix A. Although analog computing lost the commercial war to its digital counterpart there were distinct advantages in the analog world. For example the AC network analyzers used in the 1920's had the capability of real time computation of large power networks. Even the fastest digital computers today cannot claim this capability. This speed is brought about by the ability to have true parallelism in computation and is one of the reasons analog computation is still utilized in some applications today and looks to be in the future. Even recently a fully analog power system emulator, currently the largest in the world, was constructed in 1990 by the Kansai Electric Power Company (KEPCO). This system was constructed with passive elements modeling major components of the power network and consists of 30 generators, 304 transmission lines, 20 loads, HVDC transmission facilities, and static var compensators[4]. This analyzer is based on a real world system and epitomizes some current development for analog computation in the power systems field. In addition, old analog network analyzers no longer in use are being utilized for undergraduate and research efforts in power systems[5].

Current and future development of analog computation looks to take advantage of associated strengths and overcome some of, ideally all, the historically congenital obstacles. Namely some major encumbrances are large size of analog circuits, poor programmability/reconfigurability, and limited computational accuracy and measurement problems. An example of an older computational tool for power systems is shown in Figure 2[6]. This was an analog transmission line model used for computations in relay

studies. This was a very powerful tool for its time but suffered from the drawbacks previously mentioned. New technological developments are showing promise to overcome these hindrances.

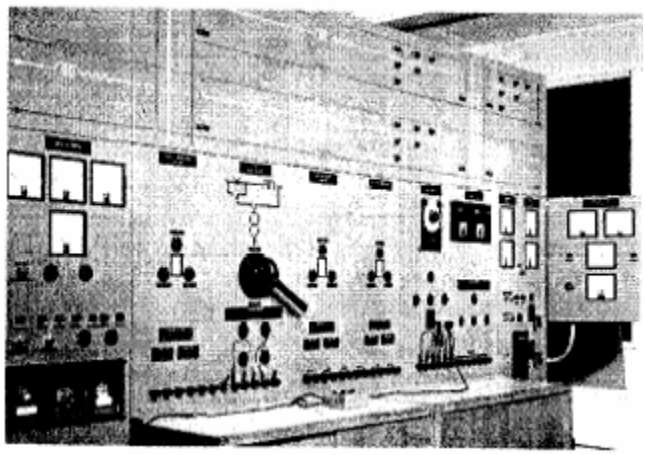

Figure 2: Analog Transmission Line Model Control Panel

One approach deals with hybrid systems. These computational engines utilize both digital and analog components to try and take advantage of both methods. More recently a push is going for computational systems on a chip (SoC) which allows reconfiguration and programmability without the need of manually changing wires or settings. This push for SoC is being done with both analog and digital computational methods. The latter is trying to mimic the main strength of analog computation, true parallel computation.

With the advancement of fabrication technologies digital network analyzers are being researched and developed moving towards real time digital computation[7-10]. These analyzers show promise but are much more complex in comparison to analog network analyzers and still have problems associated with digital computation. The basic

approach to achieve parallel computation in power systems with this method is to associate an independent processor or process with each power system component (transmission lines, generators, loads, etc.). An example of a real time digital analyzer for a transmission line can be seen in [7]. Other methods dedicate a processor to each bus in the power system[9]. In contrast to an analog approach these methods require a vast array of complex devices (processors) to construct and simulate a power system. In addition, these methods are approaching real time by increasing the incremental step size of computation and are not continuous mathematically as analog methods are. Analog approaches have already shown to be much faster than real time computation[1].

Current research in the analog field is pushing towards VLSI implementation of various analog technologies to realize a SoC and is well suited for power system analysis[1, 11-14]. Development in BiCMOS, MOST, BJT and other analog VLSI technologies are paving the way for large scale integration and accuracy for analog designs. Literally thousands of analog components can be fabricated on a wafer the size of a pushpin. In the older network analyzers the components were exceedingly large in comparison to microelectronics. Likewise as the system to be represented by the analyzer grew in size so did the analyzer itself. A realization of large systems with thousands of components is simply not feasible through a NA. VLSI is the solution. Neural network computation methods is a VLSI example being studied[15, 16] along with Evolvable Hardware (EH)[17]. In this thesis modeling of power transmission lines is accomplished with Operational Transconductance Amplifiers (OTAs) which are fundamental building blocks of VLSI circuits. OTA technology specifically lends itself well to fabrication on a large scale and allows for remote reconfiguration via a

controllable bias current allowing remote programmability in a large scale analog emulator for power systems.

1.3 MOTIVATION

The main advantage of analog computational methods is speed through the pure parallelism exhibited. This technology has the potential to create a real-time or faster than real time computation engine for large complex systems, specifically in this case power systems. This can result in better planning and operation which leads to fewer power outages. Power outages are very expensive, specifically for business operations, and current computational methods do not allow full contingency analysis to be conducted during system operation. Faster computational tools can be used during system operation to help eliminate downtime and make the power grid more secure and robust.

For the most part the power grid is extremely reliable. The majority of power outages are alleviated quickly and do not result any major problems. Unfortunately the outages that are not alleviated quickly or easily tend to cause more serious problems, especially economically. In addition, with the interconnection present in the power grid cascading failures are becoming more and more common and at this time are of great concern in planning and operation stages. These failures affect large areas of power transmission and distribution systems and require more time to fix the problems and bring equipment back online. A study published in 2004 by Lawrence Berkeley National Laboratory (Berkeley Labs) estimated that power outages result in monetary losses of eighty billion dollars annually[18] in America. With economic effects of that magnitude

the motivation to push for even higher reliability of electric power is warranted. Some companies are so sensitive to power outages they build and operate their own power generation stations (cogeneration) to supplement utility power and to provide for critical loads in the event of a utility blackout. This is popular in manufacturing facilities where hours of downtime result in millions of dollars in losses of revenue. Table 1[19] details the revenue loss in dollars per hour of operation and per employee-hour for different sectors of the economy.

Table 1: Cost of System Downtime in Different Industries

INDUSTRY SECTOR	REVENUE/HOUR	REVENUE/EMPLOYEE-HOUR
Energy	$2,817,846	$569.20
Telecommunications	2,066,245	186.98
Manufacturing	1,610,654	134.24
Financial institutions	1,495,134	1,079.89
Information technology	1,344,461	184.03
Insurance	1,202,444	370.92
Retail	1,107,274	244.37
Pharmaceuticals	1,082,252	167.53
Banking	996,802	130.52
Food/beverage processing	804,192	153.10
Consumer products	785,719	127.98
Chemicals	704,101	194.53
Transportation	668,586	107.78
Utilities	643,250	380.94
Health care	636,030	142.58
Metals/natural resources	580,588	153.11
Professional services	532,510	99.59
Electronics	477,366	74.48
Construction and engineering	389,601	216.18
Media	340,432	119.74
Hospitality and travel	330,654	38.62
Average	$1,010,536	$205.55

Improving grid reliability makes sense economically. While improving the infrastructure of the power system along with maintenance of the current system yield better reliability the most critical component is in power system operation. This is where faster computation can lead to improved reliability. Power system operators want to economically dispatch electrical energy while allowing for system faults (contingencies) without loss of power to any customers. This particular analysis requires massive computational efforts specifically related to contingency analysis, furthermore, this problem is growing even worse with the trend of deregulation. Prior to deregulation each utility locally operated their power system with minimal or no interaction with other utilities. The analysis was mainly limited to a single utility's power system. Now Regional Transmission Organizations (RTO), such as PJM, operate huge sections of the power grid and are required to run these analyses on systems with tens of thousands of nodes or buses. It is not feasible with current digital computation technology to run all the desired analysis while operating the system. Simplifying assumptions are made along with approximations on failure modes to speed up the processes and meet the demands of power system operation. If real-time computational tools are developed more thorough analyses could be conducted without the need for as many assumptions and shortcuts. Properly applied this increase in system analysis for real-time operations should allow better power system operation and higher reliability.

1.4 PROBLEM STATEMENT

The objective was to expand upon a previously proposed DC emulation power flow technique by developing more detailed transmission line models and also to develop

these line models in low-cost analog hardware. Particularly, the analog hardware should be fast, accurate, remotely reconfigurable, and scalable for large system modeling and have the capability to be easily implemented into a VLSI design.

1.5 ORGANIZATION OF THESIS

The software tools utilized along with the hardware testing environment is outlined in chapter 2. Chapter 3 provides some background theory on power transmission line modeling and Chapter 4 contains an overview of a specific methodology for analog emulation of power systems and the modeling of power system components with emphasis on transmission lines. Specific details of numerous transmission line models for emulation are presented. Chapter 5 introduces the analog circuits and their associated components for the analog emulation line models with the inclusion of software and hardware verification of these circuits. Chapter 6 follows this development with verification and analysis of the analog transmission line models constructed with the analog components introduced in the preceding chapter through software simulation and hardware testing. In conclusion chapter 7 summarizes the work presented in this thesis and the progress made in this research topic with these contributions followed by recommendations for future work.

2 DESIGN AND BENCHMARKING ENVIRONMENT

2.1 OVERVIEW

The work presented in this thesis deals with the formulation and development of transmission line models for the purpose of analog power-flow emulation. During the development of these models numerous hardware (HW) and software (SW) tools were utilized. These tools were used to aid the design process, test the designs against their desired performance, verify the analog circuit functionality and validate the results as applied to power-flow computation. In the development of a hardware prototype representing a network of transmission lines a combination of HW and SW were used for powering, actuating, acquiring data and controlling the associated circuitry. Before the hardware prototype was constructed software tools were used in design, simulation and verification of the line models. More specifically, the circuit design tool PSpice was utilized for software simulations. All emulation results, from both SW simulations and HW testing, were compared directly with commercially available power-flow packages.

2.2 PSPICE

PSpice is a software tool for electronic circuit analysis. It is utilized heavily in the work presented in this thesis. The acronym SPICE refers to Simulation Program for Integrated Circuits Emphasis. This software represents and analyzes circuits through a netlist and component models. A netlist is a text based file which specifies electronic components in the circuit and their interconnections. Each electrical component has an associated PSpice model which mathematically represents its input/output behavior in the

PSpice software along with other information such as pin outs and size of the physical device. With this information mathematical circuit analysis is conducted based on the component models and their interconnections. Specifically, a commercially available product OrCad Capture CIS [20] was used which is published by Cadence. This software package utilizes a PSpice backend for computation and evaluation of circuit behavior via a netlist and also includes a robust graphical user interface.

The interface allows for the construction of circuits by creation of an electrical schematic. The netlist is then automatically produced by the software based on the schematic representation of the circuit. Simulations are conducted and data analyzed by file outputs or graphically through the use of probes. These probes are graphically applied to the circuit schematic and measure the electrical signals and other characteristics which can then be visually plotted. The two basic probes measure current and voltage. In addition, the data from these probes can be processed mathematically to compute other values of interest such as power dissipation or Fourier analysis. Figure 3 shows a PSpice schematic of a simple OTA voltage controlled current source (VCCS). There is a voltage probe on the input of the device and a current probe on the output. The bias current, supplied by current source I1, is the independent variable which controls the gain of the OTA. The output current varies for a fixed input voltage with the bias current. Figure 4 is the plot generated from the probes in the circuit in Figure 3 and is an example of how signals are plotted and can then be analyzed based on probes inserted in the schematic.

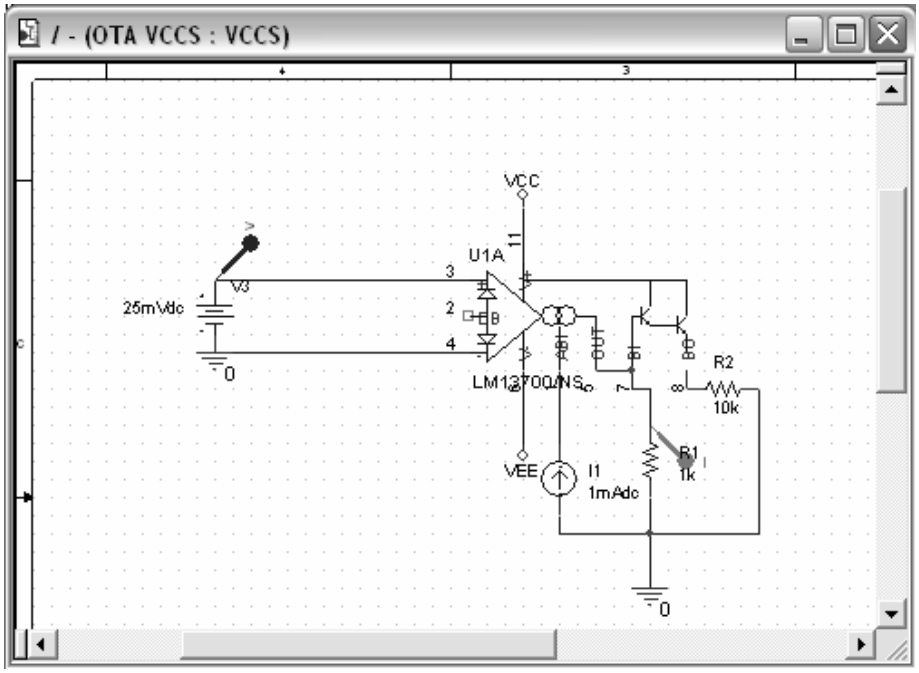

Figure 3: PSpice Electrical Schematic with Voltage and Current Probes

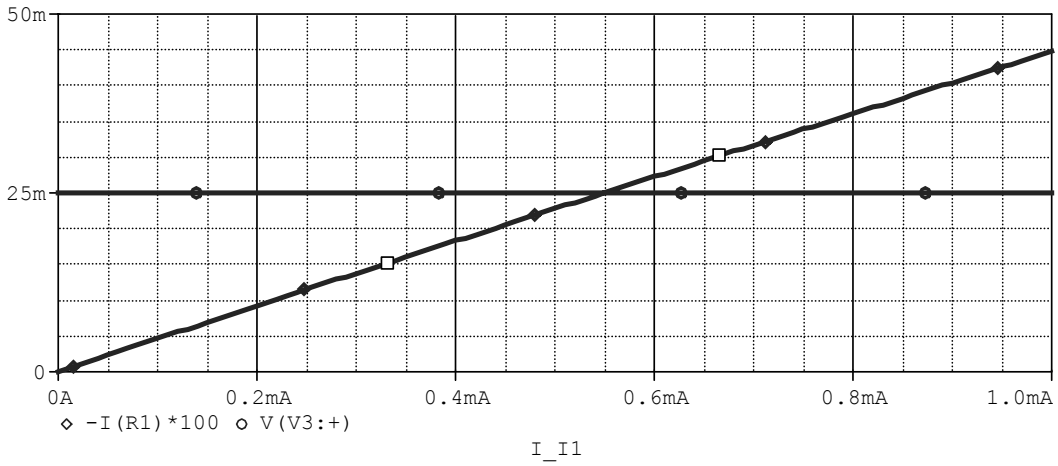

Figure 4: PSpice Plot of Probed Signals vs. Bias Current

PSpice was utilized extensively for the design and verification of the analog transmission line models and analog circuit components in this thesis. This was useful because behavior of the circuits can be tested through the software based circuit models

without the need to construct the circuits in hardware. However these models are approximations of the real device and many components are treated as ideal in the analysis. Assumptions are made to simplify both the models and the computation of their behavior. With this in mind there are inherent differences between the simulation results and the hardware results. This does not invalidate the simulations in anyway but this fact must be recognized when transferring circuits from the simulation environment into hardware. Minor discrepancies in results should be expected and drastic differences can occur if the component models are not an accurate representation of the hardware components. In an attempt to minimize such discrepancies all of the PSpice component models used in this work were obtained directly from the manufacturers of the devices. This was done as an attempt to represent the actual circuit behavior as closely as possible. The hardware prototype was built based off the designs tested through PSpice circuit simulations and include the same electrical components. For comparison to the end application of power-flow both the circuit simulations and hardware results were compared to PowerWorld power-flow solutions [21].

2.3 POWERWORLD

PowerWorld is a visually based software package for power system analysis. More specifically the basic application of this software is to solve static power-flow problems. The power system is represented by a single line graphical diagram consisting of power system components. Figure 5 shows a one line diagram of a six bus power system in PowerWorld. It consists of generators, transmission lines and loads. The parameters of these components are user adjustable and set to represent their real world

counterparts. The dialog box for adjusting transmission line parameters and setting other options is shown in Figure 6. Adjustments and settings can be made for transmission line impedances, power-flow limits and fault parameters. The flow of power through the system is even represented graphically based on the numerical solutions obtained. This can be seen by the green arrows in Figure 5. In addition, this software has other capabilities such as optimal power-flow solvers, economic analysis and area generation control but is utilized in this work only for its static Newton-Raphson power-flow solver. The results of this solver are compared directly to the PSpice and hardware results of the analog line models for validation purposes. Error analysis is conducted on the differences between this power-flow solver and the analog emulation results.

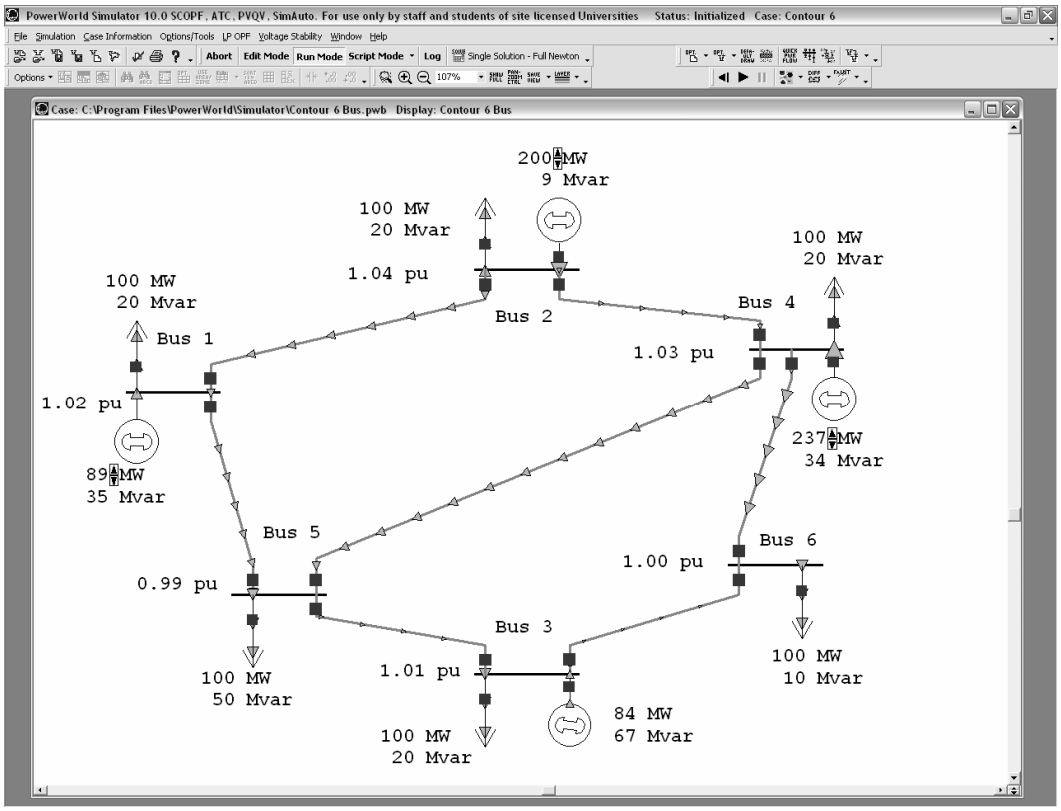

Figure 5: PowerWorld One Line Diagram of a 6 Bus Power System

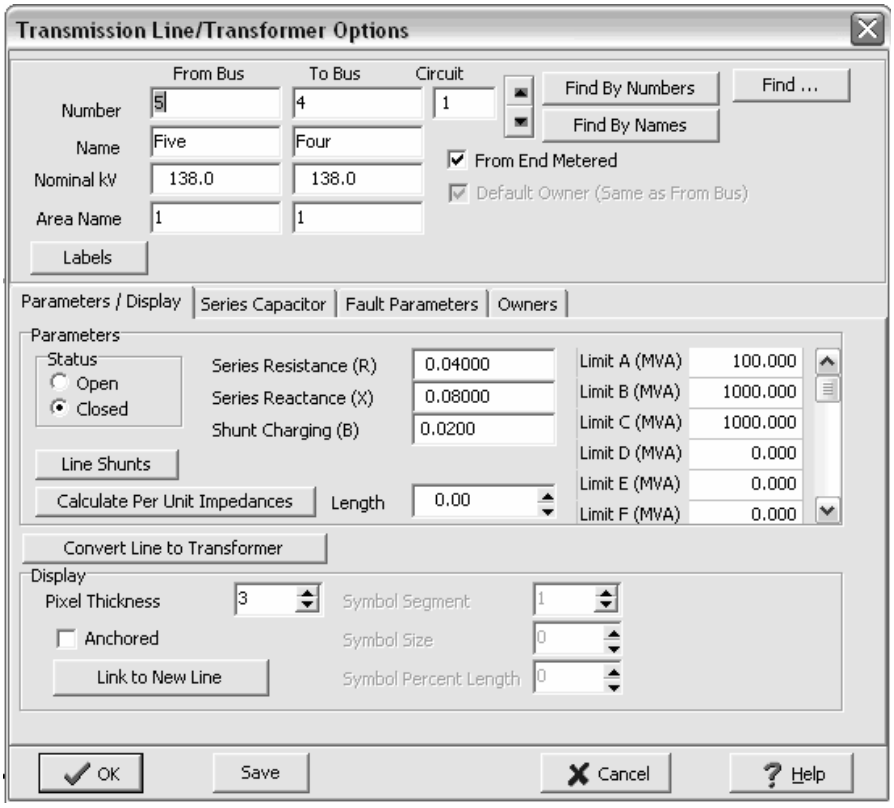

Figure 6: PowerWorld Transmission Line Options

With respect to the main contribution of this work, PowerWorld software was used to construct a three bus power system which was used as a basis of comparison to a three bus analog hardware prototype based on the analog line models derived within this thesis. This three bus system consisted of two generators, three transmission lines and a single load.

2.4 HARDWARE

Hardware tools were utilized for data acquisition, measurement, actuation/configuration, and control of an analog three bus power system prototype.

Oscilloscopes and a National Instruments Data Acquisition (DAQ) card, specifically model # NI PCI-6071E, were used for monitoring and acquiring data from the circuits. DC power supplies and a National Instruments analog output card, model # NI PCI6703, were used for actuation and control of the hardware. Specifically transmission line parameters were set and varied via PC control of the National Instruments analog output card. This control was accomplished through National Instruments LabVIEW[22] software which interfaces with the National Instruments DAQ and analog output cards. The LabVIEW software introduces a graphical programming environment to control power supplies and output cards, in this case an analog output card, and measure data from DAQ cards. Figure 7 details, through a block diagram, the hardware setup for testing of the transmission line prototype. This setup allows remote control, configuration and actuation of the transmission line circuits along with data acquisition from the analog hardware.

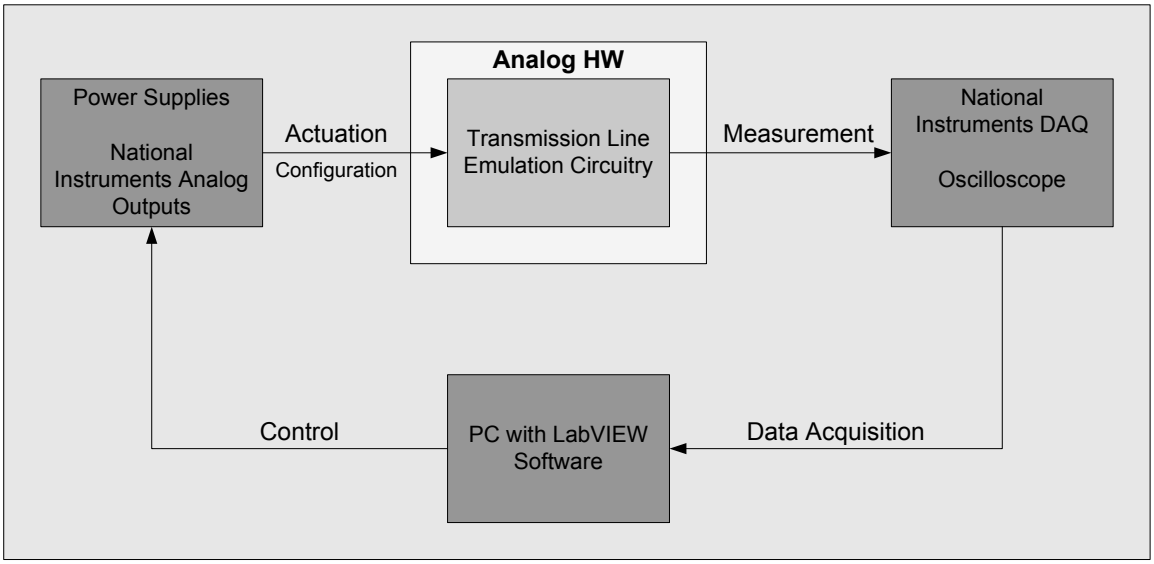

Figure 7: Analog Emulation Hardware Test Setup

3 POWER TRANSMISSION LINE MODELING

3.1 OVERVIEW OF TRANSMISSION LINE MODELING

The transmission line transmits electrical power from one end of the line, sending end, to another, receiving end. A common method of analyzing this behavior is through parameterization and modeling of the transmission lines with passive components. The passive components used in this modeling are resistors, capacitors and inductors. The quantity of these parameters depends mainly on the conductors used in the lines and the physical or geometrical configuration of the lines. The conductors themselves will have certain characteristics such as resistance and reactance both in series from sending to receiving ends of the line and shunt from the line to electrical ground associated with them. In addition, there is inherently mutual inductance, or coupling, of the lines with respect to each other as they are bundled together or placed in close proximity to one another in a multi-phase system. This can all be taken into account through proper analysis and parameterization of the transmission lines. This chapter does not derive the parameterization of the lines but provides an overview of steady state analysis of transmission lines after the line parameters have been obtained.

In this thesis only the sinusoidal steady state of the transmission lines is examined. No dynamic analysis or consideration is taken. The work here is geared mainly towards power-flow studies in which the steady state behavior of the transmission lines is focused on with the dynamics neglected. In a power system the dynamics of generators and loads are much more substantial in both magnitude and time duration and affect the system more than the transmission line dynamics. It is a reasonable assumption to neglect the transmission line dynamics for power-flow studies and generator/load

dynamics should be introduced into power system analysis before the dynamic behavior of transmission lines is considered.

A conventional method of modeling steady state transmission lines is through either distributed or lumped parameterization. The latter is a simplification of the former. The next sections detail the derivation of the distributed line model and the methodology and justification of lumped parameter equivalent models. Most of this information was gathered from[23, 24].

3.2 DISTRIBUTED TRANSMISSION LINE PARAMETERS

The distributed transmission line model gains its name from 'distributing' the parameters of the line equally through the line. The parameters are quantified per unit length and are additive in nature as the length of the line increases. This is effective for wave propagation analysis along the line as well as at the terminals of the line. Specifically for a power transmission line the voltage and current behavior along the line is of interest. Power transmitted through the line as well as losses can be observed and determined from these quantities. A diagram for a segment of a distributed transmission line is shown in Figure 8 [24]. The line model segment consists of a series impedance and a shunt admittance. The overall distributed transmission line model consists of a summation of these line segments.

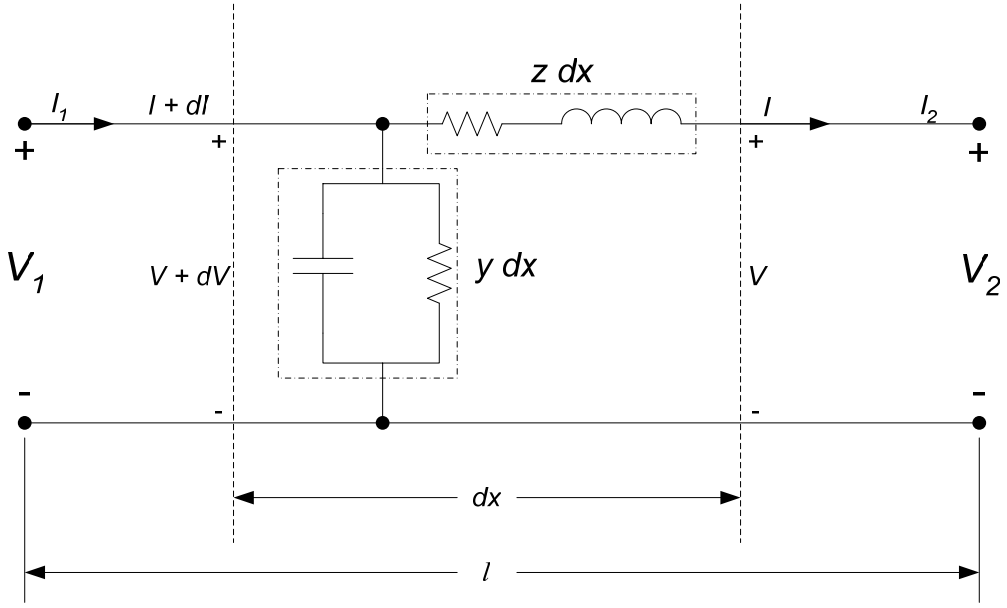

Figure 8: Distributed Parameter Transmission Line Model

The series impedance of the line is represented by a resistance in series with an inductance. This is quantified per unit length as follows:

$$z = r + j\omega l \tag{3.1}$$

The series resistance r and the series inductance l are quantified respectively as ohms per unit length and henrys per unit length. The term ω represents the operational angular frequency of the AC power system in radians per second. The resulting impedance of the inductor is therefore dependant on the operational frequency of the system. In this thesis lower case letters will be used for distributed parameters and upper case letters for lumped parameters. The shunt elements of the line model consist of a capacitance and a resistance in parallel with each other. The admittance of this shunt element is quantified by:

$$y = g + j\omega c \tag{3.2}$$

The capacitor admittance is also dependant on the system operational frequency.

As shown in Figure 8, the length of the whole line is denoted by l and the length of the differential segment by dx. The series impedance across a segment is zdx and the shunt segment ydx. V_1 and I_1 denote the voltage and current at the sending end, $x = 0$, and V_2 and I_2 at the receiving end, $x = l$. A voltage drop dV appears across the series element of the line and a current dI flows through the shunt element. Two first-order differential equations (3.3) quantify the voltage drop and current loss of the line[24].

$$\begin{aligned} \frac{dV}{dx} &= zI \\ \frac{dI}{dx} &= yV \end{aligned} \tag{3.3}$$

This same behavior can also be represented by a single second-order linear equation in terms of either current or voltage:

$$\frac{d^2V}{dx^2} = yzV = \gamma^2 V \tag{3.4}$$

$$\frac{d^2I}{dx^2} = yzI = \gamma^2 I \tag{3.5}$$

The term γ is called the propagation constant. Solving the differential equations yields the following solutions [24]:

$$\begin{aligned} V &= V_2 \cosh(\gamma x) + Z_c I_2 \sinh(\gamma x) \\ I &= I_2 \cosh(\gamma x) + \frac{V_2}{Z_c} \sinh(\gamma x) \end{aligned} \tag{3.6}$$

These equations yield the voltage and current at any point along the transmission line designated by x. The term Z_c is referred to as the characteristic impedance of the line and is computed by:

$$Z_c = \sqrt{z / y} \tag{3.7}$$

The terminal voltages and currents are usually of more interest and can be computed by setting $x = l$:

$$\begin{aligned} V_1 &= V_2 \cosh(\gamma l) + Z_c I_2 \sinh(\gamma l) \\ I_1 &= I_2 \cosh(\gamma l) + \frac{V_2}{Z_c} \sinh(\gamma l) \end{aligned} \tag{3.8}$$

The lumped parameter model is a simplification of the distributed model and was developed to model only the terminal relationships at the sending end and receiving end of the transmission lines. It was derived from (3.8) but contains no information of voltage and current as they propagate down the line. Voltage and current information at

any point along the line can be useful but where it is not required the simplified lumped models are adequate.

3.3 LUMPED TRANSMISSION LINE PARAMETERS

Traditionally in power flow analysis the voltages and currents at the line terminals are the values of more interest as compared to points along the transmission line. Historically the wave propagation on the lines is neglected and a simplified lumped parameter model is implemented for power flow. To develop the lumped model equation (3.8) can be put in the following form [24]:

$$\begin{aligned} V_1 &= AV_2 + BI_2 \\ I_1 &= CV_2 + DI_2 \end{aligned} \tag{3.9}$$

where:

$$\begin{aligned} A &= \cosh(\gamma l) \\ B &= Z_c \sinh(\gamma l) \\ C &= \frac{1}{Z_c}\sinh(\gamma l) \\ D &= \cosh(\gamma l) \end{aligned} \tag{3.10}$$

The lumped transmission line model holds the appropriate terminal behavior in equation (3.9) with lumped circuit elements. A π-equivalent circuit for this purpose is shown in Figure 9.

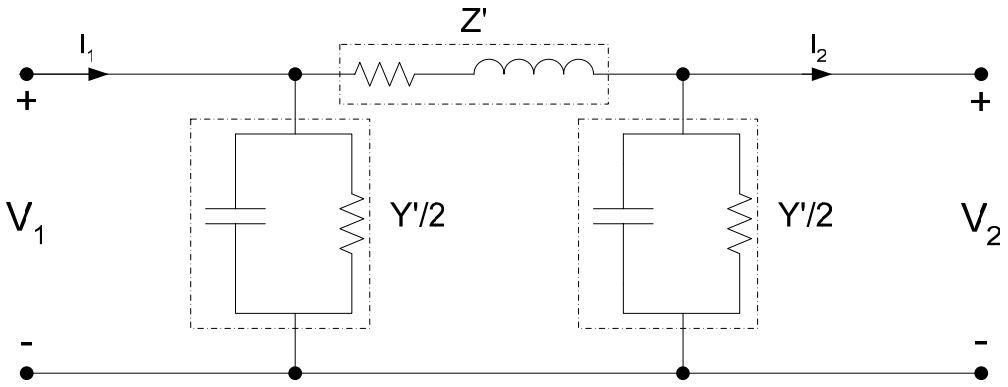

Figure 9: Lumped Parameter Π-Equivalent Transmission Line

Passive elements model the series and shunt elements in this model. The effects of the distribution of impedance across the line are lumped together in quantities of ohms. They are related to the length of the line but are not in terms of unit length. By appropriately picking the values of Z' and $Y'/2$ the same terminal behavior of the distributed line is held. Utilization of Kirchoff's voltage (KVL) and current (KCL) laws to the lumped parameter circuit in Figure 9 yield the following results [24]:

$$\begin{aligned} V_1 &= V_2 + Z'\left(I_2 + \frac{Y'}{2}V_2\right) \\ &= \left(1 + \frac{Z'Y'}{2}\right)V_2 + Z'I_2 \end{aligned} \tag{3.11}$$

$$\begin{aligned} I_1 &= \frac{Y'}{2}V_1 + \frac{Y'}{2}V_2 + I_2 \\ &= Y'\left(1 + \frac{Z'Y'}{4}\right)V_2 + \left(1 + \frac{Z'Y'}{2}\right)I_2 \end{aligned} \tag{3.12}$$

Comparing (3.11) and (3.12) to (3.9) allows the quantification of the A, B, C, and D parameters for the lumped equivalent circuit.

$$
\begin{aligned}
A &= 1+\frac{Z'Y'}{2} \\
B &= Z' \\
C &= Y'\left(1+\frac{Z'Y'}{4}\right) \\
D &= 1+\frac{Z'Y'}{2}
\end{aligned}
\tag{3.13}
$$

Solving for the components Z' and $\frac{Y'}{2}$ in Figure 9 yields:

$$Z' = Z_c \sinh\left(\gamma l\right) \tag{3.14}$$

$$\frac{Y'}{2} = \frac{1}{Z_c}\tanh\left(\frac{\gamma l}{2}\right) \tag{3.15}$$

The formulation here allows the quantification of parameters in a lumped π-equivalent circuit with respect to the length, characteristic impedance and the propagation constant of the line. Resistors, capacitors and inductors for the lumped model are sized by (3.14) and (3.15). From there circuit analysis on the resultant RLC circuit will maintain the appropriate terminal behavior. In a similar manner a T equivalent circuit could be constructed with two series impedance elements and one shunt impedance element. This is simply a transformation of the π model which holds the same terminal relationship. For shorter length transmission lines this derivation may be simplified.

For lines that are not particularly long $|\gamma l| \ll 1$. If this is the case small angle approximations can be made to (3.14) and (3.15) to simplify the computation without

substantial loss in computational accuracy. The next section deals with this simplification along with the omission of certain passive elements to simplify the lumped model even further.

3.4 LUMPED PARAMETER TRANSMISSION LINE MODELS

The prior sections introduced both distributed and lumped parameter transmission line modeling. Specifically the lumped parameter model was a π-equivalent circuit which incorporates shunt resistive and capacitive elements along with series resistive and inductive elements. Certain simplifying assumptions can be made to this lumped equivalent circuit based on the length of the transmission line. Four different line models are presented here based on the transmission line length. As the lines become shorter certain parameters have a minimal effect on the terminal voltages and currents of the line and can then be neglected.

For a *long transmission line* $\left(l > 150 \text{ miles}\right)$ no approximations should be made. The circuit elements for a π-equivalent circuit should be computed by (3.14) and (3.15). For this π-equivalent circuit the characteristic impedance and propagation constant are computed as follows:

$$\begin{aligned}\gamma &= \sqrt{yz} = \sqrt{\left(g + j\omega c\right)\left(r + j\omega l\right)} \\ &= \sqrt{gr - \omega^2 cl + j\left(\omega cr + \omega gl\right)}\end{aligned} \tag{3.16}$$

$$Z_c = \sqrt{\frac{z}{y}} = \sqrt{\frac{r + j\omega l}{g + j\omega c}} \tag{3.17}$$

With γ and Z_c the complex values of $Z'$and $Y'/2$ are computed. The RLC circuit elements are then sized for the equivalent circuit in Figure 10. This representation will be referred to as the *long transmission line* model.

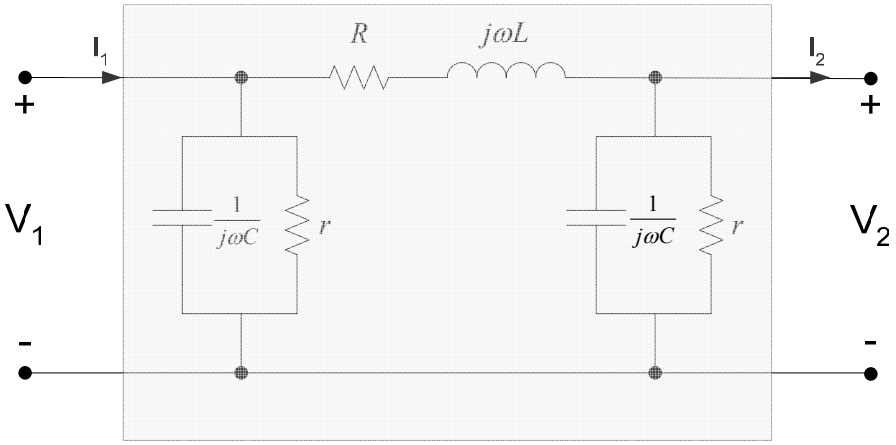

Figure 10: Long Transmission Line Model

where:

$$Z' = R + j\omega L \tag{3.18}$$

$$\frac{Y'}{2} = \frac{1}{r} + j\omega C \tag{3.19}$$

Note that "r" in (3.19) is a lumped parameter. It is in lower case here to differentiate it from the series resistive element. This shunt resistive element can be neglected if a transmission line is less than 150 miles in length. This is defined as a *medium length transmission line*.

The resistive shunt current flow on a transmission line is usually very small and is proportional to the terminal voltage magnitude. This element's contribution is only

significant in longer high voltage transmission lines. For medium length lines this component is neglected with little discrepancy in calculated results. If the shunt resistance of the line is neglected the lumped equivalent circuit will yield the form in Figure 11.

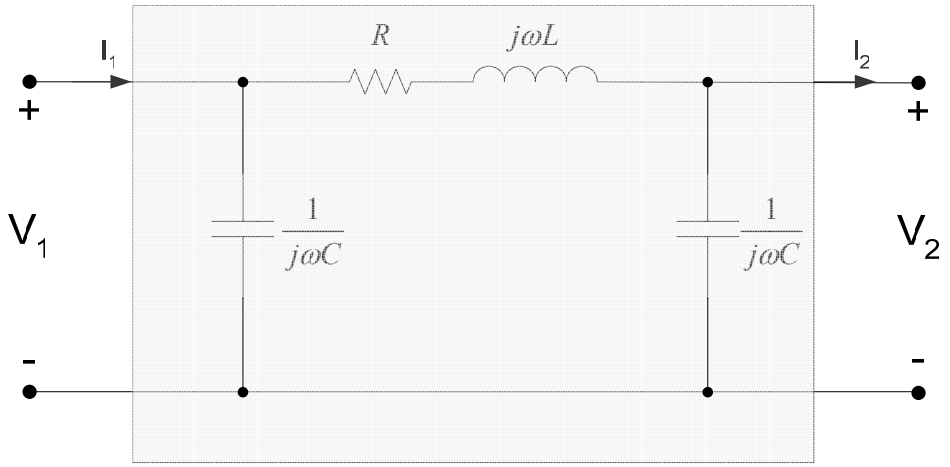

Figure 11: Medium Length Transmission Line Model

Further approximations are also made for this model. No longer are the propagation constant and characteristic impedances used to calculate the RLC elements in the lumped circuit. The following approximations are made:

$$Z' \approx Z = zl = R + j\omega L \tag{3.20}$$

$$\frac{Y'}{2} \approx \frac{Y}{2} = yl = -j\omega C \tag{3.21}$$

This is simpler than the long line model computation. The elements in this model can be quantified by the line length and parameters in per unit length. No hyperbolic functions

are necessary. Next further approximations are made for short transmission line. A short transmission line is defined as a line less than 50 miles in length.

For short transmission lines all the shunt elements are neglected. The argument for this is that the shunt charging due to the shunt capacitance is negligible for short transmission lines and eliminating them from the modeling results in little inaccuracy. Two short transmission line models are represented here. One is referred to as a *short lossy transmission line* and the other *short lossless transmission line*. The lossy model incorporates both the series resistor and inductor components shown in Figure 12. The term lossy is formulated from the presence of I^2R real power losses in the model. Small angle approximations are again used and the components in this model are quantified by equation (3.20).

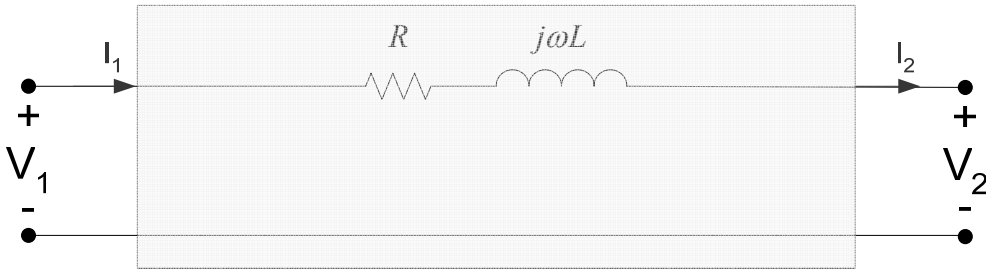

Figure 12: Short Lossy Transmission Line Model

The fourth and final lumped line model considered here is the short lossless line model. This is the simplest representation of a power transmission line and is often used in distribution system line modeling and for very short lines. This is also fairly popular in power flow solvers in order to simplify and speed up calculations. This model is

simply a series inductive element shown in Figure 13. The absence of the series resistor, and real power losses, is why the model is called lossless.

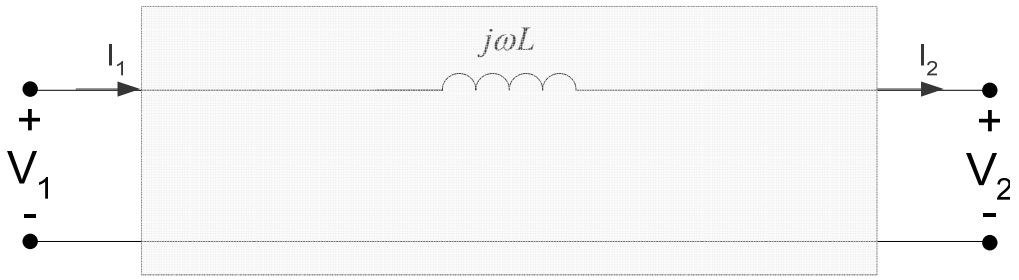

Figure 13: Short Lossless Transmission Line Model

The inductor in this model is sized by the following equation:

$$Z = j\omega L \tag{3.22}$$

Four lumped line models have been presented, specifically long, medium, short lossy and short lossless models. Care must be taken when to incorporate which model in calculations to prevent large errors in the results. Guidelines have been given in [24] with respect to the transmission line length. This is summarized in Table 2 and each line type is labeled by a letter. Intuition indicates that the short lossless line model should only be used in lines much less than 50 miles in length.

Table 2: Details on Lumped Line Models

Line Model	Transmission Line Length	Appropriate Lumped Model	Assumptions Made
A	$l \ll 50$ miles	Short Lossless	-all shunt element neglected -series resistance neglected $Z' \approx Z$
B	$l < 50$ miles	Short Lossy	-all shunt elements neglected $Z' \approx Z$
C	$50 \le l < 150$ miles	Medium Line	-shunt resistor neglected $Z' \approx Z$ $\frac{Y'}{2} \approx \frac{Y}{2}$
D	$l \ge 150$ miles	Long Line	None

The four lumped line models presented here are the basis for the analog transmission line modeling for power flow in this thesis. Analog circuit equivalents to the four models derived are developed and tested for the analog power flow emulation. Chapter 4 details this analog power flow method and the modeling of power system components with emphasis on the transmission lines for this application.

4 ANALOG EMULATION OF A POWER SYSTEM

4.1 INTRODUCTION

In this chapter the analog DC emulation power flow methodology is examined. The fundamental theory behind this computational approach is presented along with a characterization of the power system model employed in this emulation environment. Each power system component is identified separately in this context. The mathematical models are presented with emphasis on application to this particular emulation scheme. This DC emulation approach is utilized here but other methods have been investigated.

There are various approaches for analog computation of power systems that have been introduced over the years. Three different methods have been outlined in [12, 13], functional analog computation, DC emulation and AC emulation of the power system. More specifically, functional analog computation is similar to the old generic analog mathematical computation methods but with one key difference. It is specialized specifically to power system problems. It consists of analog computation blocks based on electrical equations. These are pieced together in a manner to solve the desired problem. In the DC emulation technique, which is utilized here, the states of the power system network are represented by DC voltages and currents in equivalent DC networks. The elements in the network are inherently frequency independent. This is discussed in more detail later. The latter approach, AC emulation, is analogous with both the old and new AC network analyzers. The emulation of the system is done in pure AC and the elements are all frequency dependant. "The main difference between the AC and DC emulation approaches is the fact that in the AC approach the computation is performed instantaneously, whereas in the DC approach it is only the signals' envelopes which are

being computed."[13] These represent three different approaches to the same problem and encompass many things in common with each other.

The prevalent common theme in the aforementioned emulation techniques is the necessity to model power system components. Whether it is an analog computation element, a DC network, or an AC network there requires behavioral representation of the real world power system components. The results of the subsequent computation will only be as precise as the system models and definitions. For the DC emulation method used here the classical power system model is utilized which contains three main components: generators, transmission lines and loads.

4.2 ANALOG POWER SYSTEM DC EMULATION METHODOLOGY

The power system network in the DC emulation technique is represented in rectangular coordinates. The power system parameters are separated into real and imaginary components and the states, voltages and currents, are also separated into real and imaginary components which are represented by DC voltage and current levels. With this method only the magnitude of the signals requires to be measured and phase can be computed later. This permits the use of DC. The power system emulation network consists of generators, transmission lines and loads and is shown in Figure 14.

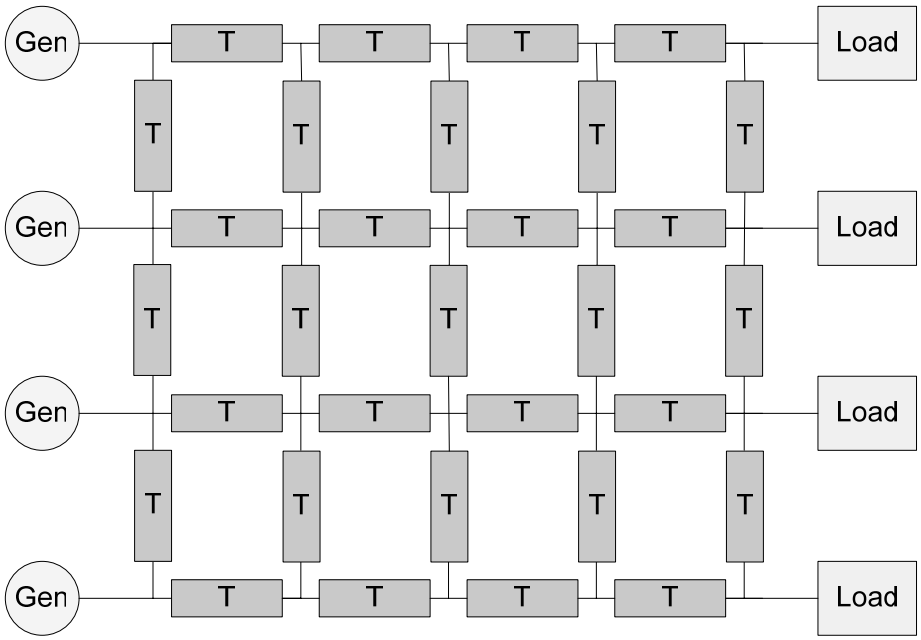

Figure 14: Power System Emulation Network

Any number of transmission lines, loads and generators can be combined together to represent a power system. Switches, relays, transformers and other power system components are not modeled here but are topics of future research. The fundamental components for power generation, transmission and consumption were analyzed here.

Power system computation in many digital applications is conducted in polar coordinates. This system details the magnitude and the angle of power system states and parameters. In the analog DC emulation technique the computation in the network is performed exclusively in rectangular (Cartesian) coordinates. All power system parameters and values are represented in rectangular and/or converted from polar form to rectangular form when necessary for application in the emulator. Figure 15 is a comparison of polar and rectangular representation of a vector V on a complex plane.

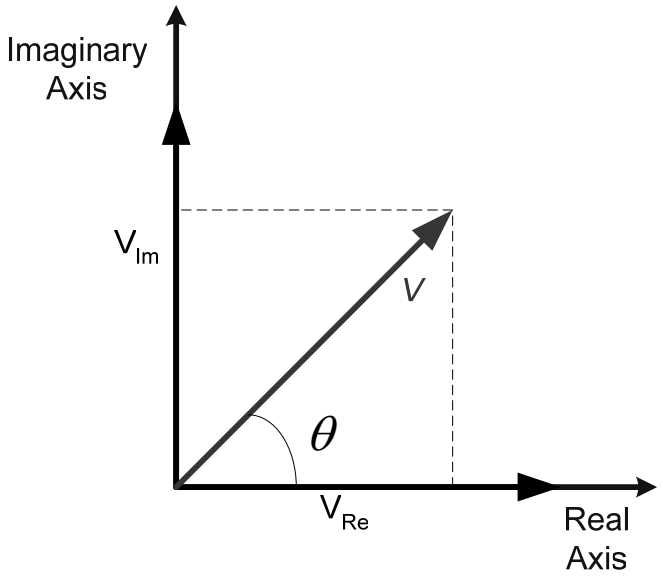

Figure 15: Polar and Rectangular Coordinate Comparison

The polar form representation contains two components, a vector magnitude and phase. It can be represented in the following manner:

$$V = |V| \angle \theta \tag{4.1}$$

The Cartesian coordinate representation consists of two magnitudes. One is purely real and lies on the real axis and the other is purely imaginary and lies on the imaginary axis. This representation is related to the magnitude and phase by (4.2) where V_{Re} and V_{Im} are the real and imaginary vector components respectively.

$$V = V_{\mathrm{Re}} + jV_{\mathrm{Im}} = |V|\cos(\theta) + j|V|\sin(\theta) \tag{4.2}$$

The rectangular form can easily be transformed into polar form by (4.3). Note that the sign of the quotient of V_{Im} and V_{Re} dictates what quadrant θ lies. If the quotient is positive θ is located in the first quadrant and if negative θ lies in the fourth quadrant.

$$\begin{aligned} |V| &= \sqrt{V_{\text{Re}}^2 + V_{\text{Im}}^2} \\ \theta &= \tan^{-1}\left(\frac{V_{\text{Im}}}{V_{\text{Re}}}\right) \end{aligned} \tag{4.3}$$

The specifics of the previously proposed DC emulation method were first introduced in [12] and highlighted and expanded upon here. The method roots itself in solving the network matrix equation in rectangular coordinates. This equation simply relates the current flow in the network to a voltage applied to the admittance of the network:

$$[I] = [Y] \cdot [V] \tag{4.4}$$

The admittance matrix, $[Y]$, is a nodal admittance matrix based on the power system topology and impedances of the transmission lines. Note that this is not a Y_{bus} matrix and ground is considered a node in the construction of this matrix. With this in mind for an n-bus system this matrix would be $(n+1)$ by $(n+1)$ square. $[I]$ is an $(n+1)$ vector of the currents entering the network nodes and $[V]$ is an $(n+1)$ vector of the nodal voltages of the network. The multiplication of a complex admittance and a complex voltage in rectangular coordinates yields:

$$\begin{aligned} Y \cdot V = I_{\mathrm{Re}} + jI_{\mathrm{Im}} &= \left(Y_{\mathrm{Re}} + jY_{\mathrm{Im}}\right)\cdot\left(V_{\mathrm{Re}} + jV_{\mathrm{Im}}\right) \\ &= Y_{\mathrm{Re}}V_{\mathrm{Re}} + jY_{\mathrm{Re}}V_{\mathrm{Im}} + jY_{\mathrm{Im}}V_{\mathrm{Re}} - Y_{\mathrm{Im}}V_{\mathrm{Im}} \\ &= \left(Y_{\mathrm{Re}}V_{\mathrm{Re}} - Y_{\mathrm{Im}}V_{\mathrm{Im}}\right) \quad \{\text{real current}\} \\ &\quad + j\left(Y_{\mathrm{Im}}V_{\mathrm{Re}} + Y_{\mathrm{Im}}V_{\mathrm{Re}}\right) \quad \{\text{imaginary current}\} \end{aligned} \tag{4.5}$$

The real and imaginary components in (4.5) are labeled. For this case, with complex network impedances, there are a total of four current components. Each one is an admittance magnitude multiplied by a voltage magnitude. This behavior is identical to the resultant current flow based on a voltage drop across a resistor. This is how the DC emulation is conducted. Resistive networks represent the admittances and a voltage is applied to induce current flow. With four DC networks, one for each of the components in (4.5), the network equation can be solved. The solution to the power flow problem is specifically the voltages and currents flowing in these DC networks. This information needs to be extracted, or measured, from the analog circuits. Specifically the four networks are defined as follows:

$$\begin{aligned} I_{\mathrm{Re}} + jI_{\mathrm{Im}} = {} & Y_{\mathrm{Re}}V_{\mathrm{Re}} && \text{network 1} \\ & - Y_{\mathrm{Im}}V_{\mathrm{Im}} && \text{network 2} \\ & + jY_{\mathrm{Im}}V_{\mathrm{Re}} && \text{network 3} \\ & + jY_{\mathrm{Re}}V_{\mathrm{Im}} && \text{network 4} \end{aligned} \tag{4.6}$$

From a circuit viewpoint all the nodal voltages can be measured directly in rectangular coordinates, one imaginary voltage magnitude and one real voltage magnitude. Obtaining the rectangular current magnitudes is not as straight forward. Four

currents must be measured and added together to obtain the branch current flow or injections in rectangular coordinates. Specifically the summation of currents in networks one and two equal the real current value and the summation of currents in networks three and four equate to the imaginary current component. More generally for any size system the current at a node i, such as a generator injection into the network, can be computed by:

$$\begin{aligned} I_{Gi} = & \sum_{j=1}^{n+1} \mathrm{Re}\{Y_{ij}\} \cdot \mathrm{Re}\{V_j\} \quad \text{network 1} \\ & -\sum_{j=1}^{n+1} \mathrm{Im}\{Y_{ij}\} \cdot \mathrm{Im}\{V_j\} \quad \text{network 2} \\ & +j\sum_{j=1}^{n+1} \mathrm{Im}\{Y_{ij}\} \cdot \mathrm{Re}\{V_j\} \quad \text{network 3} \\ & +j\sum_{j=1}^{n+1} \mathrm{Re}\{Y_{ij}\} \cdot \mathrm{Im}\{V_j\} \quad \text{network 4} \end{aligned} \tag{4.7}$$

where $\mathrm{Re}\{Y_{ij}\}$ and $\mathrm{Im}\{Y_{ij}\}$ are the real and imaginary network admittances between nodes i and j, and $\mathrm{Re}\{V_j\}$ and $\mathrm{Im}\{V_j\}$ represent the real and imaginary voltage magnitudes at bus j respectively. The formulation in (4.7) is for an n bus system with $(n+1)$ nodes with the inclusion of ground as a node.

The key to implementing this emulation technique is to develop accurate representation of the power system components to operate in the DC networks. The generators are modeled as PV buses and provide current injections and voltages at the generator buses, the transmission lines are passive resistive networks corresponding to

the line impedances and the loads are modeled as current injections or sinks as necessary. The next section delves into the details of each power system emulation component.

4.3 POWER SYSTEM EMULATION COMPONENTS

This section outlines the three main power system components utilized in the DC emulation of power-flow. These components are representative of the classic power system model containing generators, loads and transmission lines. Each component is catered towards operation in rectangular coordinates and ideally a final circuit design would be easily scaled towards VLSI technology. Realistically a large scale implementation would be a system on a chip (SOC) application. Furthermore, the components should act as computational 'modules' and allow configuration to suit specific parameters of real world power systems. For example a generator module should be able to computationally represent any kind of generator, whether it is a nuclear plant or a smaller coal burning generating station.

4.3.1 GENERATORS

The generator is modeled as a constant voltage source behind internal impedance. This is sometimes referred to as the classical generator model shown in Figure 16 [25]. For the application in DC emulation the generator maintains a PV bus behavior. The real power output, P, and the generator terminal voltage, V, are specified and maintained by the model.

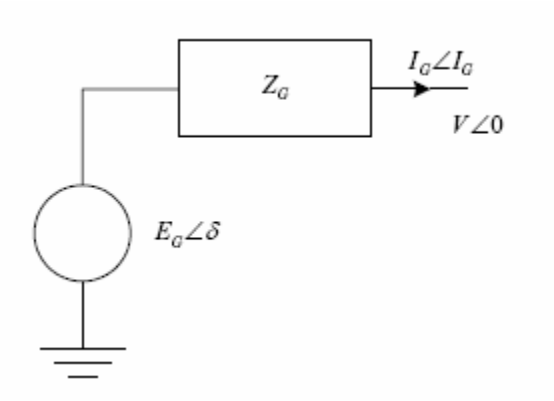

Figure 16: Classical Generator Model

The swing equation is solved to match the electrical power output of the generator with the specified mechanical input:

$$M\ddot{\delta} + D\dot{\delta} + P_e(\delta) = P_m \tag{4.8}$$

where M is the generator inertia coefficient and D is the damping coefficient of the generator. If damping is neglected solving (4.8) for the power angle results in the double integral shown in (4.9).

$$\delta = \frac{1}{M}\int\int\left(P_m - P_e(\delta)\right)dtdt \tag{4.9}$$

With the solution of the power angle and a specified generator voltage magnitude the voltages to be applied to the networks can be determined in a similar manner as equation (4.2):

$$\begin{aligned} V_{\mathrm{Re}} &= |V|\cos(\delta) \\ V_{\mathrm{Im}} &= |V|\sin(\delta) \end{aligned} \tag{4.10}$$

Figure 17 illustrates a block diagram detailing how equations (4.9) and (4.10) are solved in analog hardware [2]. The current flowing out of the generator is measured and used to calculate the electrical power output of the generator. A more generic form of the real power injected by a generator into bus i:

$$P_{e_i} = \mathrm{Re}\left\{E_i \cdot I_i^*\right\} \tag{4.11}$$

The difference between the computed electrical power output of the generator and the specified mechanical power input is integrated to solve for the power angle and the appropriate voltages are applied to the DC emulation networks. The actual solution for the terminal voltage in this model is obtained in polar form and is then converted into rectangular components via sine and cosine shaper circuits to interface with the DC networks. The swing equation of this model is an example of a functional analog computation block.

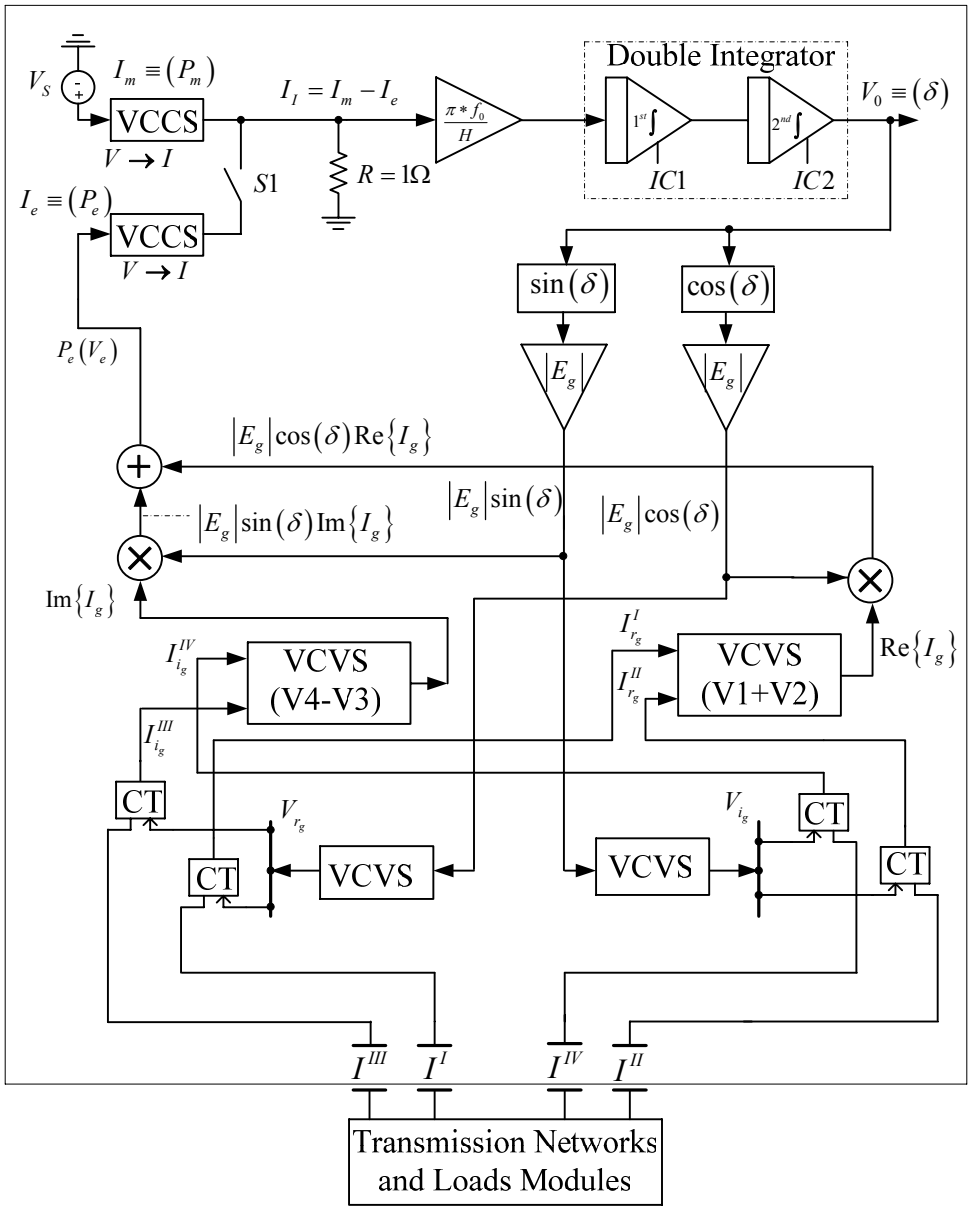

Figure 17: Analog Generator Module for DC Emulation

4.3.2 TRANSMISSION LINES

The transmission line components in this emulation scheme are purely resistive and the sizing of the imaginary resistor values is dependant upon operating frequency. By modeling the imaginary impedances as fixed resistances the operational frequency of

the power system is assumed to be constant. With the automatic generation control systems implemented today this is a reasonable assumption. The variance in operating frequency is quite minimal. Depending on the transmission line model being used, refer to Table 2 for the four lumped parameter line types, the modeling of the resistor networks for the line changes. The sizing of resistors for the four models, lossless (A) and lossy short (B), medium (C) and long length (D) lines are presented here which are analogous to the lumped parameter transmission line models presented in chapter 3. The topology of the DC emulation networks for a three bus balanced power system is also illustrated for the various line models. The simplest case of the short lossless transmission line is examined first.

The *short lossless transmission line* (A) consists of only a series inductance as outlined in Figure 13. There is only one component and it is imaginary. The admittance Y_{ij} comes from row i and column j term in the admittance matrix from equation (4.4).

$$Y_{ij} = \frac{1}{j\omega L_{ij}} = \frac{1}{X_{Lij}} \tag{4.12}$$

Separating the line reactance between two terminals i and j into real and imaginary components is trivial. There is no real component. The appropriate resistor is sized as follows:

$$R_{\mathrm{Im}(ij)} = \frac{1}{\mathrm{Im}\{Y_{ij}\}} = X_{Lij} \tag{4.13}$$

The result of the simplified line model and (4.13) indicates that only two DC resistive networks are required for this simplified transmission line. Networks one and four from equation (4.7) are no longer necessary. In addition, if the whole network is lossless this also simplifies the current measurements and feedback required for the generator model by cutting measurements in half and eliminating the summation of current components to find the real and imaginary parts of the currents. Figure 18 shows the DC network topology for a single short lossless transmission line. The interconnection of resistors resembling this line can create any size lossless network model.

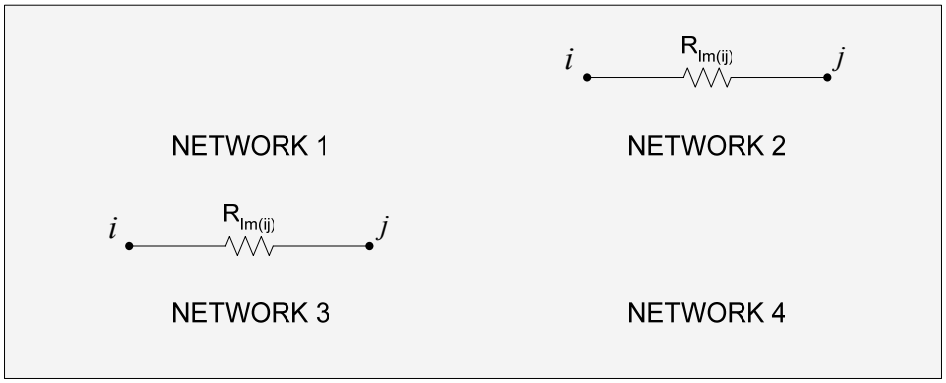

Figure 18: Resistor Networks for a Short Lossless Transmission Line

The *lossy short transmission line* (B) requires four DC networks as do the medium and long line models. They all have complex line impedances. The lossy short line depicted in Figure 12 has a series resistance and inductance. The admittance of this segment is:

$$Y_{ij} = \frac{1}{R_{ij} + j\omega L_{ij}} = \frac{1}{R_{ij} + X_{Lij}} \tag{4.14}$$

Separating this series impedance between two terminals i and j into real and imaginary components yields the following results [12]:

$$\begin{aligned} R_{\mathrm{Re}(ij)} &= \frac{1}{\mathrm{Re}\{Y_{ij}\}} = \frac{R_{ij}^2 + X_{Lij}^2}{R_{ij}} \\ R_{\mathrm{Im}(ij)} &= \frac{1}{\mathrm{Im}\{Y_{ij}\}} = \frac{R_{ij}^2 + X_{Lij}^2}{X_{Lij}} \end{aligned} \tag{4.15}$$

The resistor sizing for each network is dependant on both the resistance and reactance of the line. Note that the computation of the imaginary resistor value is quite different here than it was in equation (4.13). Figure 19 shows the DC network topology for a single short lossy transmission line.

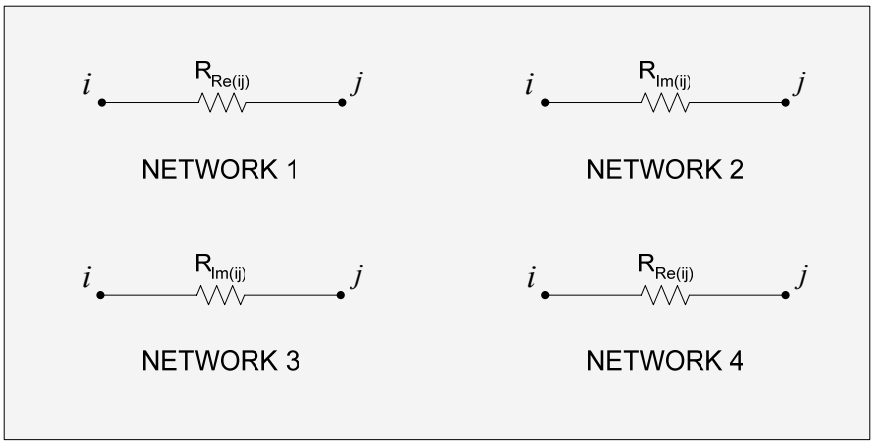

Figure 19: Resistor Networks for a Short Lossy Transmission Line

The *medium length transmission line* (C) model adds shunt capacitive elements as shown in Figure 11. The shunt elements are viewed as additional branches in the network. These branched extend from the line terminals, or bus, to ground. For notation purposes ground is labeled as node k. The formulation of the series elements remains the same as in equation (4.15). The admittance between the line terminals and ground is governed by:

$$Y_{ik} = Y_{jk} = \frac{Y_C}{2} = \frac{1}{-2X_C} \tag{4.16}$$

The sizing of the resistive element for the DC emulation networks is as follows for the shunt capacitor:

$$R_{\mathrm{Im}(jk,ik)} = \frac{1}{\mathrm{Im}\left\{Y_{jk,ik}\right\}} = -2X_C \tag{4.17}$$

Similar to the lossless case there is no real resistive component for the DC networks. This indicates that the shunt resistors are only added to the DC networks representative of imaginary admittances. There is an interesting problem associated with the solution above. Due to the nature of capacitive reactance the quantity in (4.17) is a negative. A negative resistor is required to properly emulate the shunt capacitive effects of transmission lines in this DC emulation scheme.

$$\frac{1}{Y_C} = -jX_C = -j\frac{1}{\omega C} \tag{4.18}$$

Figure 20 shows the DC network topology for a single medium length transmission line.

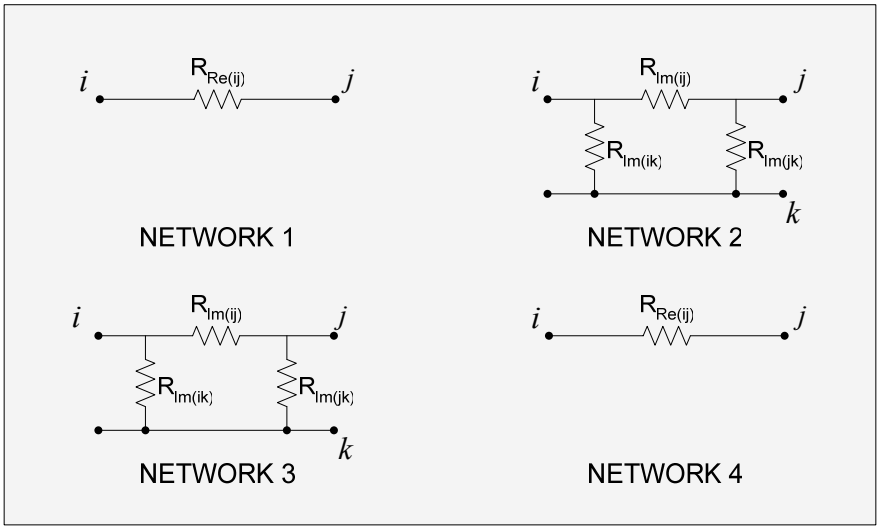

Figure 20: Resistor Networks for a Medium Length Transmission Line

For the *long transmission line* (D) in Figure 10 a shunt resistive element is added in parallel with the shunt capacitor. The formulation of the series and shunt elements both change in this line model. The approximations taken for the other line models, $Z' \approx Z$ and $\frac{Y'}{2} \approx \frac{Y}{2}$, are not sufficient for the long line model as mentioned prior, see Table 2. The values computed from (3.14) and (3.15) should be used to determine Y_{ij} and the shunt elements Y_{ik} and Y_{jk} respectively. Once this is accomplished the resistors for the series line elements for DC emulation can be solved for by (4.15). As for the shunt elements the shunt admittance is now complex:

$$Y_{ik} = Y_{jk} = \frac{Y'}{2} = \frac{1}{2r} - j\frac{1}{2X_C} \tag{4.19}$$

The sizing of the resistive elements for the DC emulation networks is as follows for the shunt capacitor and resistor:

$$\begin{aligned} R_{\mathrm{Re}(jk,ik)} &= \frac{1}{\mathrm{Re}\{Y_{jk,ik}\}} = 2r \\ R_{\mathrm{Im}(jk,ik)} &= \frac{1}{\mathrm{Im}\{Y_{jk,ik}\}} = -2X_C \end{aligned} \tag{4.20}$$

A negative resistance is still required in the shunt capacitor representation. This behavior remains unchanged from the medium length model. Figure 21 shows the DC network topology for a single long length transmission line.

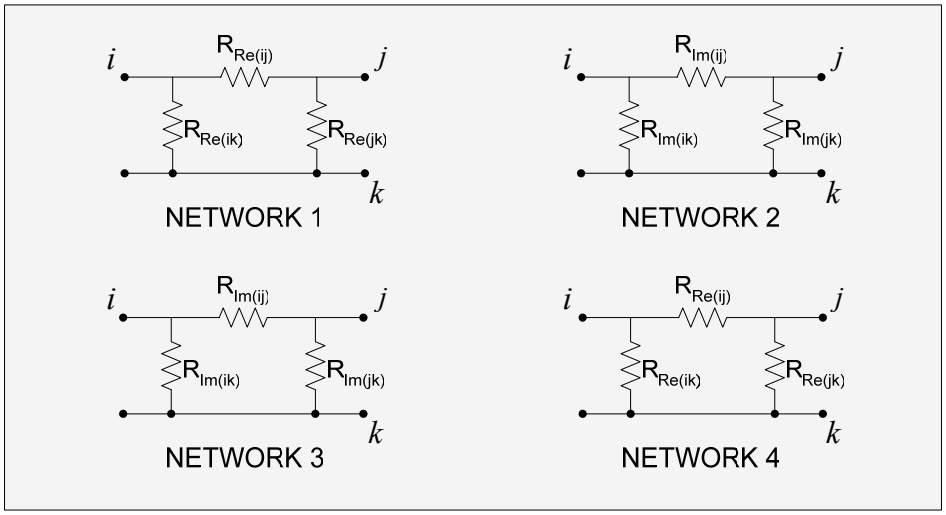

Figure 21: Resistor Networks for a Long Transmission Line Model

The four static lumped parameter transmission line models in chapter 3 have been transferred into the DC emulation approach and circuit topologies presented. In a power system there are multiple transmission lines of different lengths and parameters which interconnect generators and loads. For example Figure 22 is a single line diagram of a three bus power system. It consists of two generators, three transmission lines and a single load. The hardware prototype development was based on this three bus power system. The three transmission lines are labeled A, B and C.

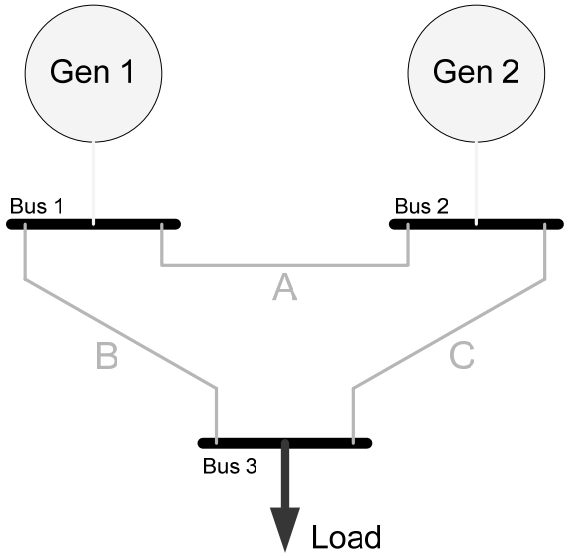

Figure 22: Single Line Diagram of a Three Bus Power System

The following figures show the DC emulation network topologies of the three bus system for the four different transmission line models presented. Generator one is the slack bus generator which is simply a voltage source. The complex voltages applied at the slack bus are determined by the reference angle and the specified voltage magnitude of that generator with equation (4.2). Generator 2 is a generator based on the swing

equation model in Figure 17. In steady-state it behaves as a voltage source and is drawn as such in the below figures. The modeling of the load is mentioned in the next section. These diagrams are indicative of how a power system network is constructed in this DC emulation.

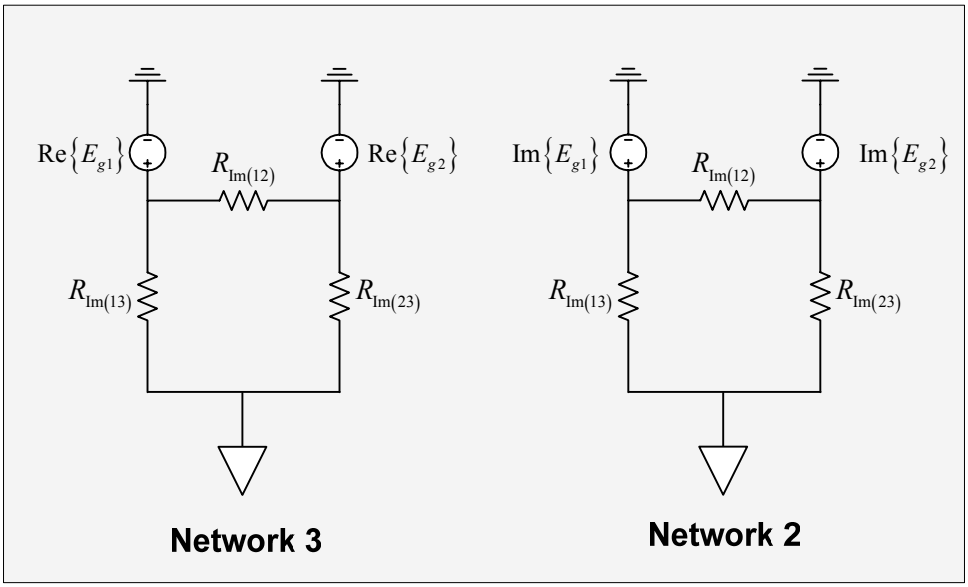

Figure 23: Three Bus DC Emulation Topology with Short Lossless Transmission Line Model

The real and imaginary slack bus generator voltages are labeled $\mathrm{Re}\{E_{g1}\}$ and $\mathrm{Im}\{E_{g1}\}$ respectively. The swing equation generator at bus two follows a similar naming convention with the subscript of 2. The resistors for the lines are labeled as imaginary with a subscript indication what buses the lines interconnect. Figure 24 shows the emulation circuits for the lossy transmission lines. Two more networks are added for this model.

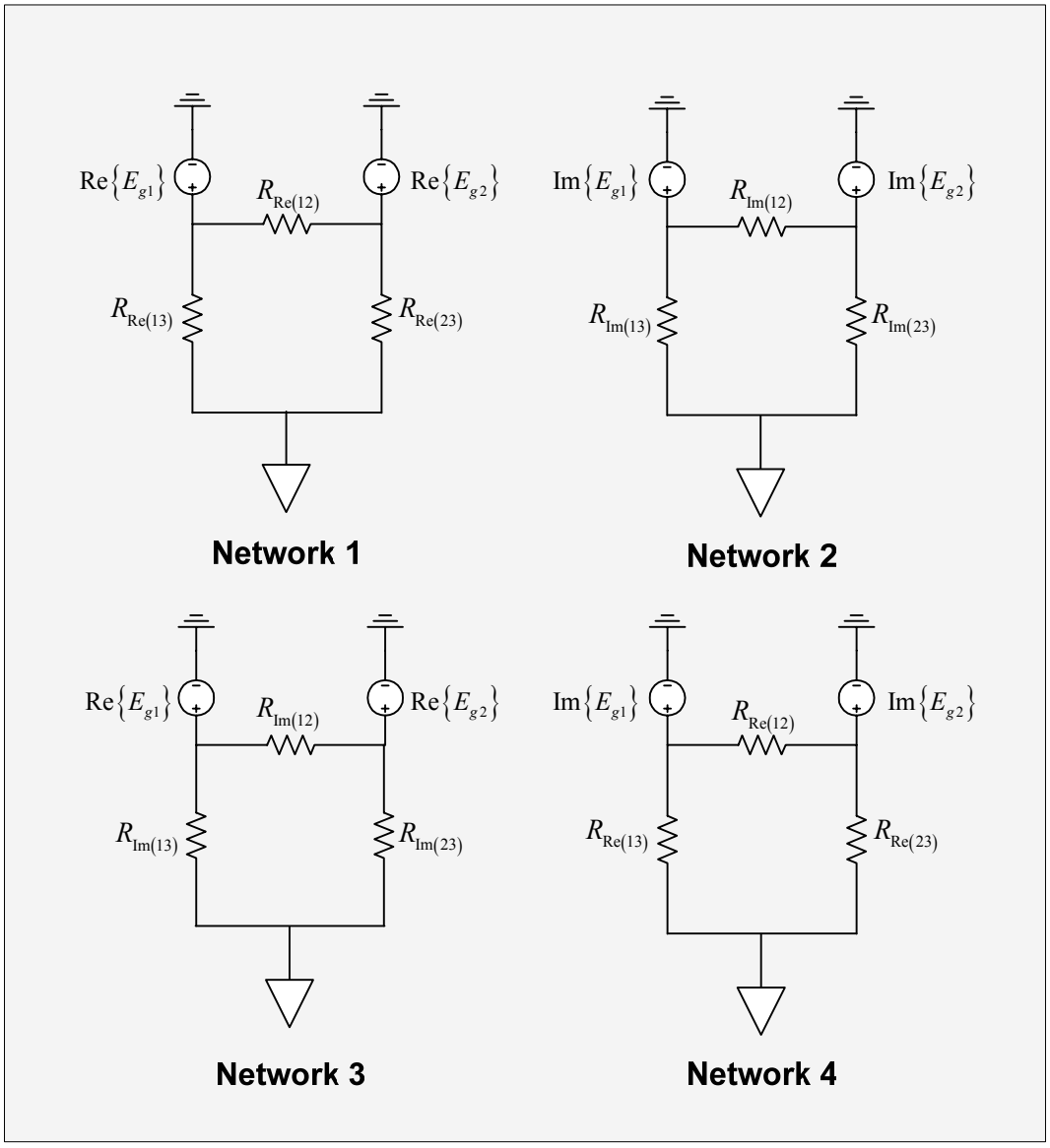

Figure 24: Three Bus DC Emulation Topology with Short Lossy Transmission Line Model

The next two figures show the medium and long length transmission lines respectively. Resistors are added from each line terminal to ground for the shunt elements in the line models. The inclusion of the shunt capacitors requires resistors for

the imaginary networks and the shunt resistance adds resistors to the real DC emulation networks. For ease in understanding the figures instead of labeling the individual resistors the networks are indicated as real or imaginary resistive networks in the DC emulation scheme.

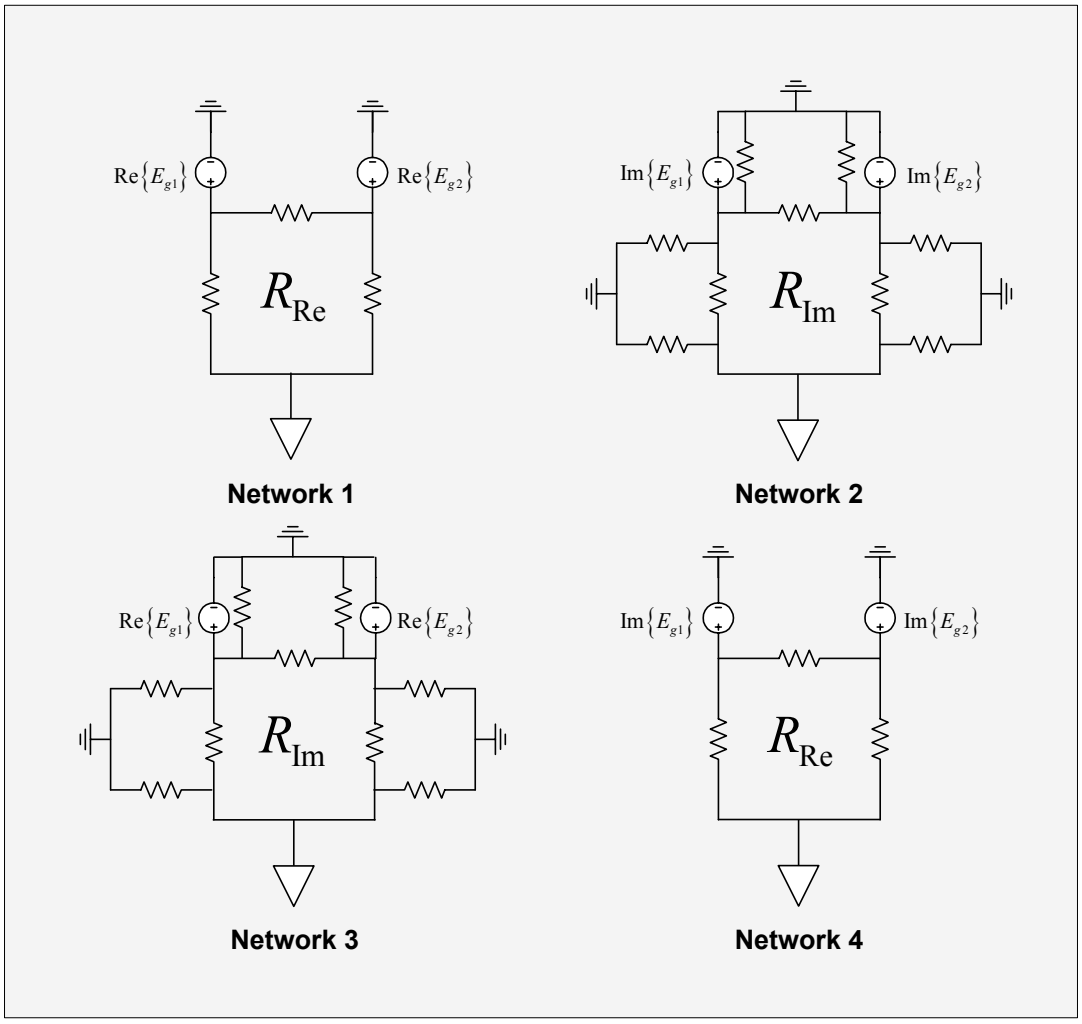

Figure 25: Three Bus DC Emulation Topology with Medium Length Transmission Line Model

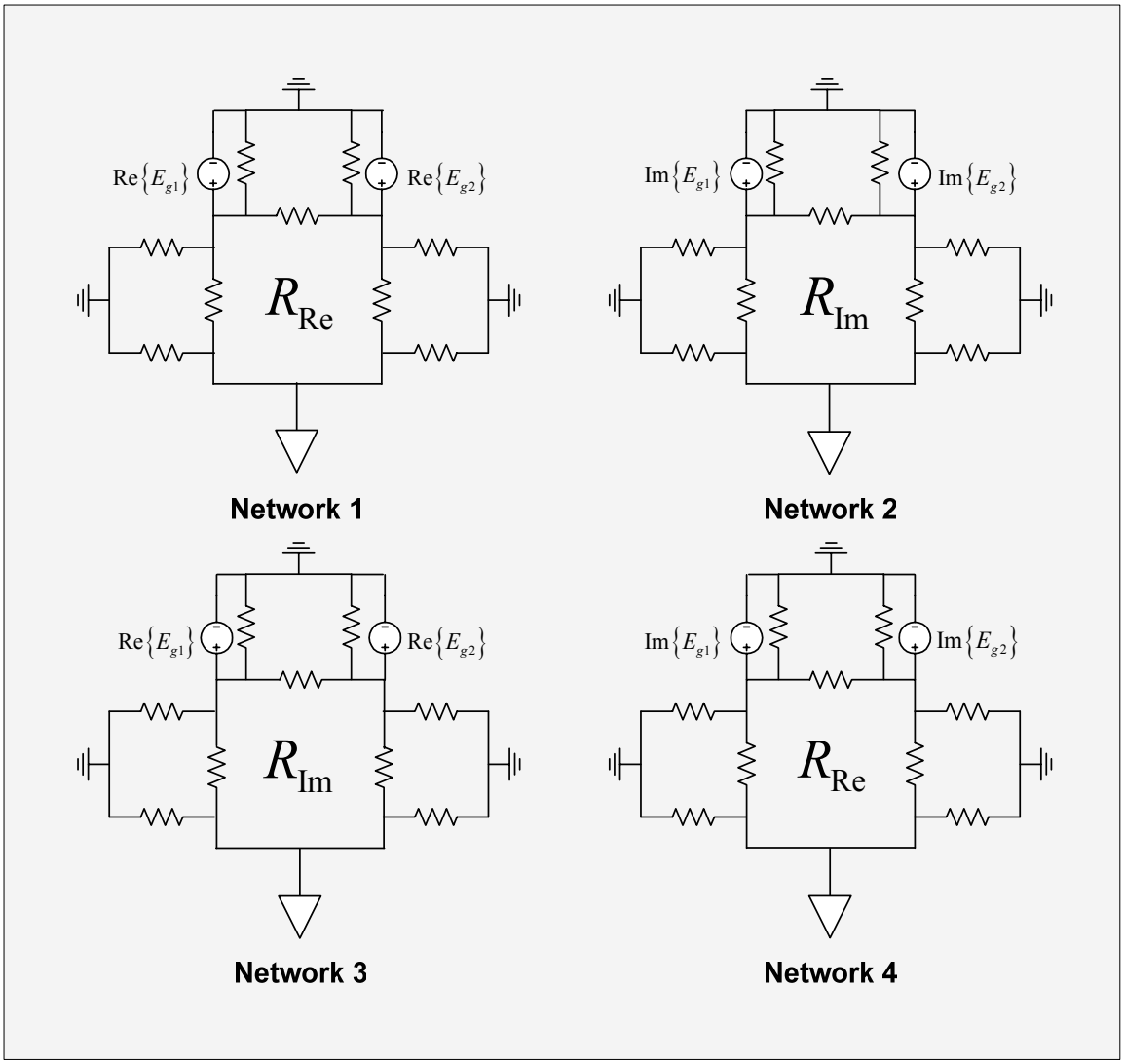

Figure 26: Three Bus DC Emulation Topology with Long Length Transmission Line Model

The four transmission line models for DC emulation outlined in this section are based on the lumped equivalent line models and are comprised of two basic building blocks. These blocks are positive and negative resistors. In chapter 5 these building blocks are developed in analog circuits with reconfigurability for altering the line parameters through a change in the resistance. Distributed line models for this analog

approach can also be realized in a similar manner with these building blocks. For example, with the lossy line model instead of a single resistor modeling a component of the line in each emulation network, a distributed model is constructed by placing many resistors in series with the sum of these resistances being equal to the desired resistance for the line model. Effectively, the parameters of the transmission line are distributed throughout these multiple resistors. The states of the power system, voltages and currents, can then be measured at intervals along the transmission line model in analog hardware. These intervals are finite in size depending on how many resistors are used to model each line segment and furthermore this approach is applicable to all the emulation line models presented. This is analogous to Figure 8 where each resistor creates a segment of the line dx.

4.3.3 LOADS

The main purpose of the loads is to sink or source current as necessary from the DC networks. The basic model that is in development for this analog power-flow method is a static ZIP load model. A ZIP load model is a linear combination of constant impedance (Z) constant current (I) and constant power (P) load. The following equations express the power consumed for each load type. The values of Z_{Load}, I_{Load} and S_{Load} are specified for the load and S_Z, S_I and S_P represent the complex power of each load type Z, I, and P respectively.

$$S_P = S_{Load} \tag{4.21}$$

$$S_I = V_{Load} \cdot I_{Load}^* \tag{4.22}$$

$$S_Z = \frac{V_{Load}^2}{Z_{Load}^*} \tag{4.23}$$

The combination load including all three elements can be expressed as follows where k_i is a weighting coefficient for each load type:

$$S_{ZIP} = k_1 \cdot S_P + k_2 \cdot S_I + k_3 \cdot S_Z \tag{4.24}$$

The only load type used in this thesis is the constant current type. The circuit realization of this load model is based off of OTAs as is the transmission line circuits which are developed in the next chapter.

5 METHODOLOGY AND DEVELOPMENT OF ANALOG TRANSMISSION LINE BULDING BLOCKS

5.1 INTRODUCTION

Chapter 4 outlined multiple transmission line models for use in the DC emulation technique for power flow analysis. To be precise the transmission lines are represented by resistive networks analogous to the real world transmission line parameters. With the aim to take advantage of the associated strengths of this analog method the hardware model was designed to have certain characteristics such as remote high speed reconfigurability, high accuracy, low-cost and VLSI capability for large scale integration. This cannot be obtained with a simple network of resistors. A network of resistors, or potentiometers, would require manual intervention to configure and alter the emulator for a given power-flow computation. In addition, there is a requirement for negative resistance when modeling shunt capacitive elements of the transmission lines. This chapter outlines a hardware design using active devices that achieves the aforementioned goals. The circuits constructed are remotely reconfigurable variable positive and negative resistive circuits which are the building blocks necessary to construct the analog line models discussed in chapter 4. Specifically, the active device utilized is an operational transconductance amplifier.

5.2 CHARACTERIZATION OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is the fundamental building block for the hardware realization of the transmission line models. This section first characterizes the ideal behavior of an OTA and then the non-linear and non-ideal characteristics such as offsets and saturation are examined. Furthermore methods for correcting some of these undesirable traits are pointed out.

The OTA is classified as an operational amplifier although it differs from the traditional operational amplifier, or op-amp. Usually when referring to an op-amp it is with regards to a voltage controlled voltage source (VCVS). Essentially this is a voltage amplifier. The input and the outputs are both voltages and ideally the open-loop gain is infinite. An OTA in contrast is a voltage controlled current source (VCCS). The input is still a voltage but the output is a current. The transfer function is dependant upon the OTAs transconductance gain (g_m) which is finite and controllable via an external bias current. This bias current is the key element which allows for reconfiguration and remote control of the line models.

A diagram of an ideal OTA is shown in Figure 27. The amplifier has a differential voltage input v_{in} and a current output i_o proportional to the device transconductance gain.

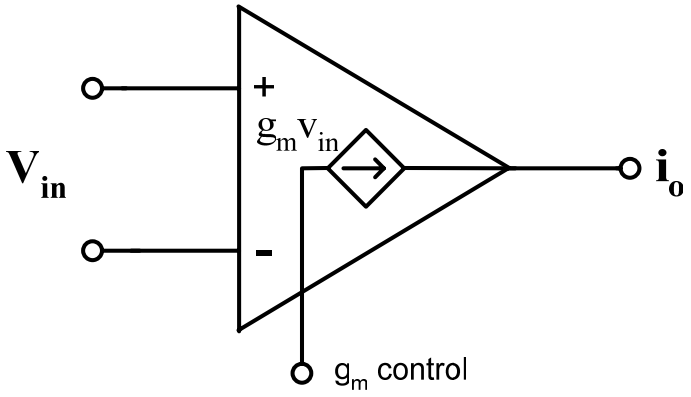

Figure 27: Ideal OTA

For an ideal OTA the output current is characterized by:

$$i_o = g_m v_{in} \tag{5.1}$$

The transconductance gain of the OTA is established by an applied biasing current (i_{abc}). To accurately control this device it is necessary to explicitly and accurately define g_m in relation to the biasing current. When doing so it turns out that the gain of the device is highly nonlinear. For numerous applications the gain is linearized around an operating point. For example for OTA-C filters, which are active filters with a remotely controllable cut-off frequency, the inaccuracies induced by assuming a linear gain do not drastically alter the cut-off frequency which is gain controlled. For the LM13700 OTA the following approximation is recommended by the manufacturer [26]:

$$g_m \approx 19.2 \cdot i_{abc} \tag{5.2}$$

Due to the precision required for computation applications this approximation is not sufficient. Large errors can result if it is used. A more accurate nonlinear definition of the transconductance gain of a basic bipolar OTA is quantified by [27]:

$$g_m = \frac{i_{abc}}{2 \cdot V_T} \cdot \sec h^2 \left(\frac{V_{in}}{2 \cdot V_T} \right) \tag{5.3}$$

In actuality the transconductance gain is not only a function of the bias current as the approximation in (5.2) states. It is also directly related to the thermal voltage$\left(V_T\right)$, which will aberrate with temperature change, and the differential input voltage to the device which can change during operation. In addition, by the nature of the hyperbolic secant function, the gain will saturate very quickly for a relatively small magnitude input voltage. This is one of the more important device limitations. The input voltage must be very small, in the mV range, to avoid large deviation or saturation of the device gain. This is one aspect of this device which has limited its applications in industry. Newer off the shelf OTAs, for example the National Semiconductor LM13700, improve the linearity of the device by incorporating linearizing diodes at the input of the device. The gain for an OTA with linearizing diodes can be approximated by (5.4) for a differential input voltage in the range of ±50 mV,

$$g_m \approx \frac{i_{abc}}{2 \cdot V_T} \cdot \sec h^2 \left(\frac{V_{in} \cdot D}{2 \cdot V_T} \right) \tag{5.4}$$

where $V_T = 26mV$ (room temperature) and D is a diode linearization constant.

The diodes help smooth the response of the gain but the magnitude of the input differential voltage is still extremely limited. In quantitative terms the gain drops off about 6% with an input of 25mV with the linearizing diodes and 20% without. Figure 28 shows the effects of the linearizing diodes on the gain factor, C, of the OTA with respect to the differential input voltage. The gain factor is defined in (5.5). The linearization (5.3) led to a gain factor of 19.2 as mentioned prior.

$$g_m = C \cdot i_{abc} \tag{5.5}$$

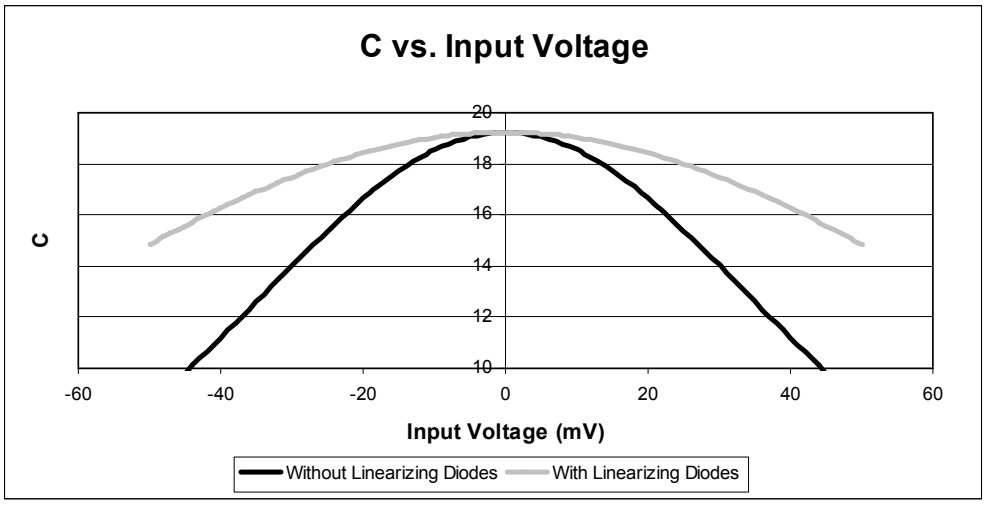

Figure 28: Effect of OTA Gain Factor with Linearizing Diodes

From the plots in Figure 28 it is very evident that the assumption made in (5.2) is a poor one for input voltage that deviate even slightly from zero volts. In addition, the effects of the linearizing diodes are pretty evident. The input voltage range can be larger for a given roll off in gain. This input voltage limitation can be improved further through

proper use of feedback similarly used in traditional op-amps. Also a CMOS design using a 2-MOSFET linear transresistor in a feedback loop has shown excellent linearity over a wide input voltage range [28]. Specifically, simulation results show total harmonic distortion of less than one percent for inputs within 8 volts peak to peak.

Another complication mentioned is that the OTA gain is inversely proportional to absolute temperature. This needs to be compensated to achieve high accuracy in large VLSI based systems where temperature differences across the chip are expected. A method is shown in [29] which alters the gain (bias current) of the OTA in direct proportion to the absolute temperature. Experimental results indicate a reduction of temperature sensitivity of more than 100 times [29]. One final characteristic of the OTA that needs to be addressed is the offsets of the device.

The transfer function in equation (5.1) is for an ideal OTA which assumes there is no offset present. In the actual OTA there are offsets. Specifically there is an offset present at the output of the device. The offset current present at the output is almost entirely caused by the internal offset voltage of the OTA. This can be modeled in a similar manner as offset voltages of traditional op-amps. Specifically a voltage source, v_{off}, applied to the input of the device is amplified to the output producing the offset current, i_{offset}. This offset can be quantified by the following equation:

$$i_{offset} = v_{off} \cdot \sec h^2 \left(\frac{v_{in}}{2 \cdot V_T} \right) \tag{5.6}$$

A compensator could be constructed to eliminate the effects of this offset although it is probably more suitable to incorporate this into fabrication through a custom designed OTA. This problem is identical to the one present with traditional op-amps but the popular method of compensation, an external trimming resistor, is insufficient for this OTA based circuit. This solution is inadequate with reconfigurability. The effects of this offset voltage are proportional to the gain of the OTA and changes as the line model parameters are changed. Trimming can only accomplish precise offset cancellation for a single gain setting. A different approach is required.

A method for eliminating an OTA input offset voltage has been proposed in [30]. This method is suitable for fabrication and quantifies and minimizes the offset for any gain configuration. An offset rejection of 40dB was achieved in simulation [30]. In general the OTA and the aforementioned methods for minimizing offset and gain dependence on temperature are fairly simple circuits and well suited to large scale VLSI integration.

The basic OTA lends itself well to fabrication due to the simplicity of the device. The central building blocks of an OTA are bipolar junction transistors (BJT) and a simple OTA can be constructed with only nine transistors. The internal structure of the LM3080 OTA is shown in Figure 29. Essentially there are four main components of the circuit, a differential pair of BJTs for the input voltage and four current mirrors. Due to its versatility the OTA is one of the most important building blocks of analog VLSI circuits [31] and can be highly accurate if used properly. With current fabrication technology tens of thousands of OTAs can be fabricated into a single VLSI design for a large scale power system emulator.

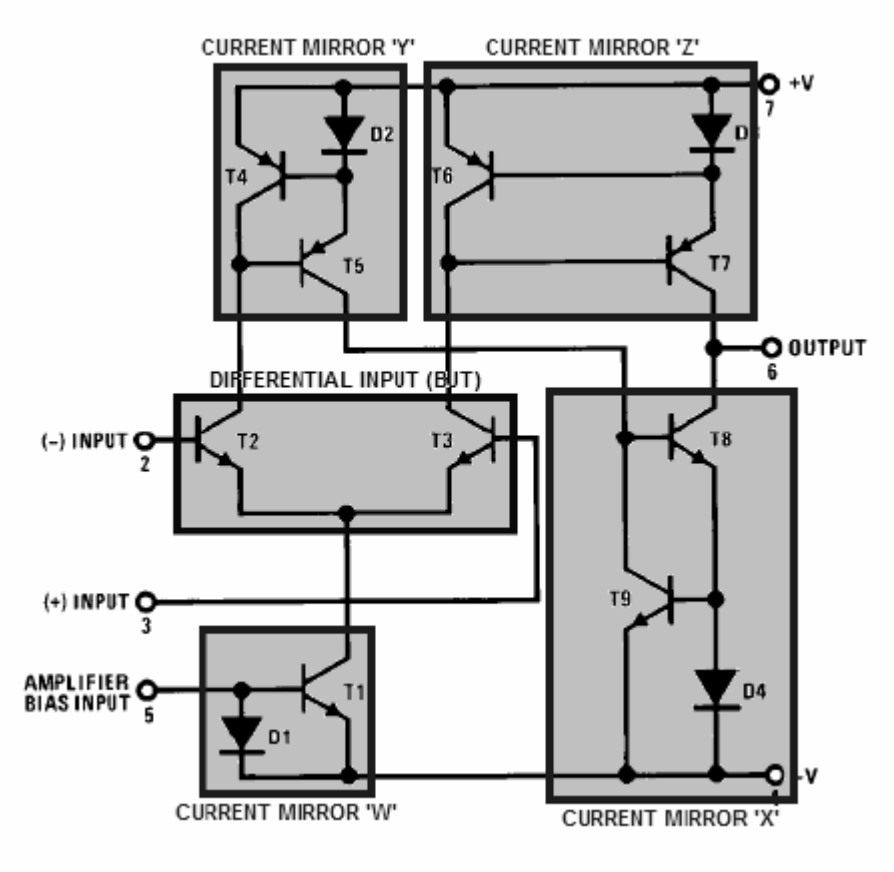

Figure 29: Internal Structure of LM3080 OTA

In general, the OTA is a device that can accomplish the antecedent goals for the emulation hardware. Specifically reconfiguration of the hardware through transconductance gain and easy implementation into large scale integrated circuits. In addition, through methods mentioned the OTA gain dependence on temperature, limited input voltage magnitude, and output current offsets can be alleviated. This is essential for large scale emulators. The best approach would be through a custom OTA design for VLSI implementation catered towards the application of analog computation. This will yield a device that is very accurate and suitable for power-flow emulation. The next

sections detail the application of OTAs to construct the variable resistive circuits necessary for the emulation of power transmission lines.

5.3 POSITIVE OTA VARIABLE RESISTOR

This section deals with the development of an OTA based positive resistive circuit in which the resistance is controlled via the OTA gain. The evaluation of resistance seen by these circuits is defined and the variable resistor circuit is logically developed. First a single ended open loop OTA variable resistor is examined and then feedback is added to attenuate the input voltage allowing a larger swing on the input. Finally a double ended OTA variable resistor circuit is developed with feedback to allow bi-directional current flow which is necessary in the DC emulation scheme.

The VCCS operation of the OTA naturally lends itself to an application of a variable resistor. A simple OTA based variable resistor is shown in Figure 30.

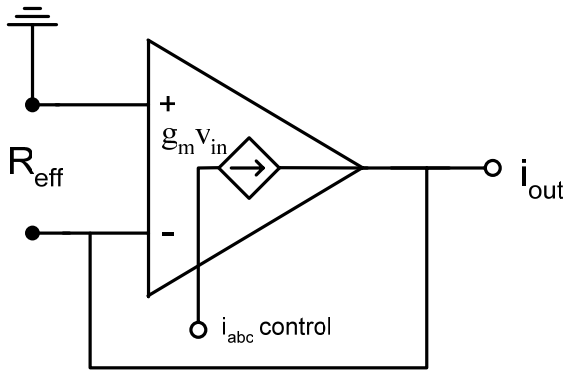

Figure 30: Basic OTA Variable Resistor

In the development and testing of the variable resistance circuits the resistance seen across the devices was defined as the "effective resistance" and designated by R_{eff}. For the simple open loop OTA configuration in Figure 30 the effective resistance is defined by the input voltage and output current relationship:

$$R_{eff} = \frac{v_{in}}{i_0} = \frac{v_{in}}{v_{in} \cdot g_m} = \frac{1}{g_m} \tag{5.7}$$

Using this configuration would be the simplest implementation although it is inadequate for this application. The circuit will show signs of saturation as the input voltage exceeds 25 mV. Furthermore the limitation of ± 25mV at the input would be burdensome in system configuration and measurement. With the introduction of feedback this problem can be alleviated. Figure 31 shows a schematic of a single ended variable resistor circuit based on the LM13700 OTA which includes a buffered voltage output used here. A voltage applied at the V_1 terminal produces an input voltage to the negative input terminal of the OTA. This in turn is multiplied by the transconductance gain producing an output current. The end result is an effective impedance present at the V_1 terminal which is controllable by the sizing of the resistors R and R_A, along with the gain of the OTA.

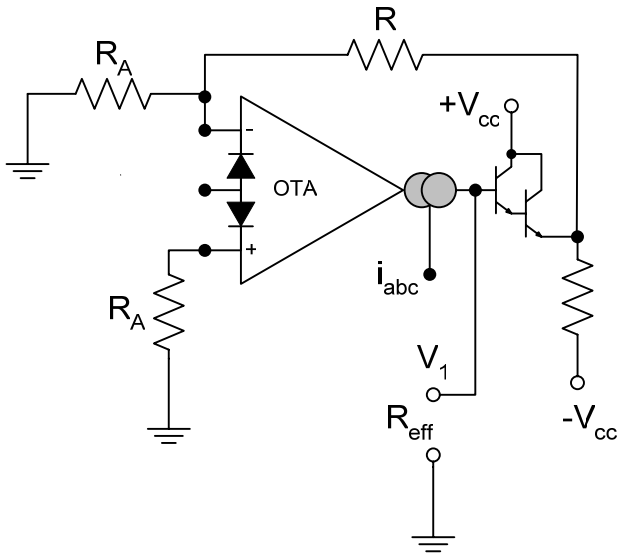

Figure 31: Single Ended Variable Resistor with Extended Input Range

The effective resistance is quantified in a similar manner as in (5.7). The input voltage V_1 is attenuated by the two resistors to provide an input voltage to the terminal of the OTA:

$$v_{in} = -V_1 \cdot \frac{R_a}{R + R_a} \tag{5.8}$$

The output current of the OTA is given by:

$$i_o = -V_1 \cdot \frac{g_m \cdot R_a}{R + R_a} \tag{5.9}$$

Note that the output current of the OTA is negative. This indicates the current is flowing into the output terminal of the OTA or in other words the circuit is loading the voltage

source V1. The effective resistance seen at the V_1 terminal is then defined as the input voltage divided the current flowing into the OTA:

$$R_{eff} = \frac{V_1}{-i_0} = \frac{R + R_a}{R_a \cdot g_m} \tag{5.10}$$

This circuit allows further configuration of the effective resistance through sizing of the resistors and also incorporates feedback of the input voltage to widen up the input voltage range while operating in a linear fashion. The only problem is that this is a single ended device and the input is referenced to the supply ground. For application in the DC emulation network this is not sufficient for the transmission line models. The lines, and subsequent resistors, are interconnected in a grid by nodes and these nodes are not tied to ground. This circuit would be useful for a constant impedance load model for this DC emulation network but the line resistors require a double ended circuit. This was incorporated by introducing a modification to this design.

The proposed OTA based variable resistor is shown in Figure 32 [26]. The inputs are floating with respect to the power supply and similar feedback is incorporated to extend the linear operating range of the circuit. Note how the input of the OTA on the left is the inverse of the OTA on the right. This allows for the outputs of the two OTAs to mimic a 'flow' of current through the circuit in a similar manner as a passive device would conduct current. The current flowing into the V_1 terminal is equal to the current flowing out of the V_2 terminal. The circuit is completely symmetric and has the same

behavior regardless of which direction the current is flowing. Due to the symmetry the effective resistance can be defined by analyzing one of the OTAs in the circuit.

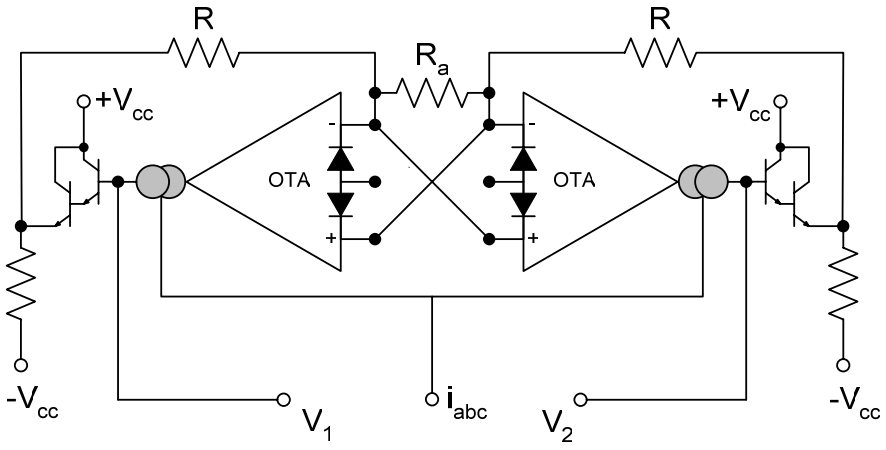

Figure 32: OTA Based Floating Variable Positive Resistor

The input voltage $V_1 - V_2$ is attenuated by the three resistors to provide an input voltage to the terminal of the OTA on the right side:

$$v_{in} = (V_1 - V_2) \cdot \frac{R_a}{2R + R_a} \tag{5.11}$$

The output current of the OTA is:

$$i_o = (V_1 - V_2) \cdot \frac{g_m \cdot R_a}{2R + R_a} \tag{5.12}$$

The effective resistance seen at the terminals is then defined as:

$$R_{eff} = \frac{(V_1 - V_2)}{i_0} = \frac{2R + R_a}{R_a \cdot g_m} \tag{5.13}$$

This variable resistance circuit has three terminals similar to a potentiometer. The two inputs, V_1 and V_2, mimic terminals of a resistor and the biasing current used to control the effective resistance of the model similar to the wiper on a potentiometer. The terminal relationship to a potentiometer is shown in Figure 23.

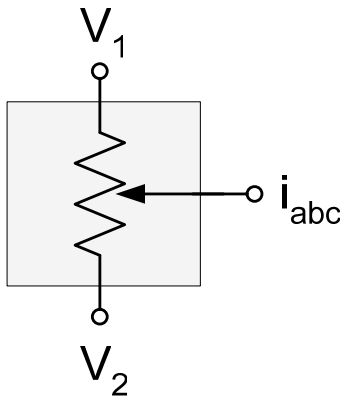

Figure 33: Potentiometer Relationship to OTA Variable Resistor Circuit

The effective resistance of the double ended OTA variable resistor in terms of the terminal voltages and current through the device is defined as:

$$R_{eff} = \frac{(V_1 - V_2)}{I_{12}} = \frac{V_{line}}{I_{line}} \tag{5.14}$$

where I_{12} is the current flowing from V_1 to V_2.

The terms V_{Line} and I_{Line} are used from here on to represent the voltage across the variable resistor terminals and the current through the device. In the emulation environment the line voltage will either be the real or imaginary component of the line voltage of the power system and the line current will be one of the components of the line currents in equation (4.7).

The circuit in Figure 32 is the variable positive resistor used for the analog emulation of a power system in this thesis. The effective resistance has been defined and can be set by the sizing of resistors and setting of the bias current. This circuit design addresses the main design requirements mentioned prior and with appropriate resistors and control over transconductance gain a very large range of effective resistance and line voltage is obtainable. The overall limitations of the circuit are mostly related to properties of OTA. The limitations, operation and controllability of this design were analyzed through PSpice simulations and hardware testing.

5.3.1 SIMULATION RESULTS

A LM13700 dual OTA that the double ended variable resistor circuit is based on was used for the simulations in PSpice. The PSpice model was obtained directly from the manufacturer to ensure accuracy. Various simulations were conducted to validate and characterize the variable resistor circuit in such respects as controllability, resistance variance and circuit limitations.

The first simulation dealt with controlling the circuit through the bias current. Applying a current source is not as simple and easily controllable in comparison to a

voltage source. The simulation using the circuit in Figure 34 uses a voltage source, V_{abc}, behind impedance, R_{abc}, to drive the bias current.

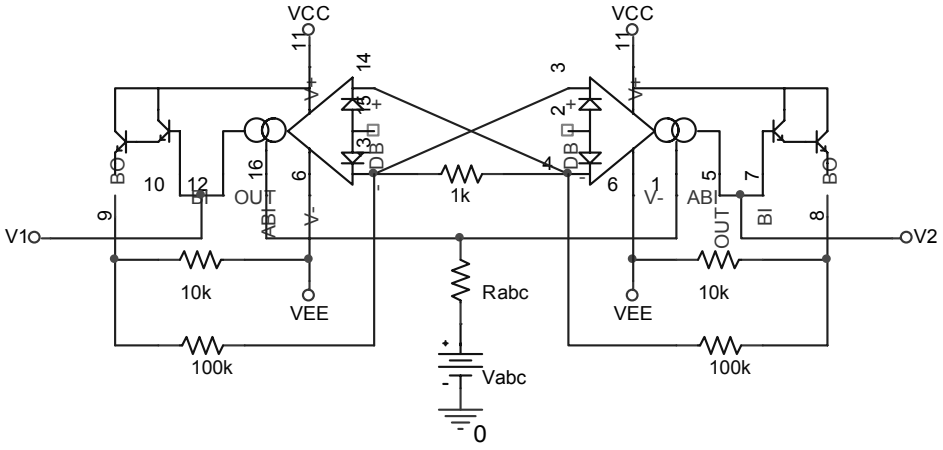

Figure 34: PSpice Schematic for OTA Based Variable Positive Resistor

A voltage sweep was performed on V_{abc} and the corresponding bias current produced was measured. The relationship between bias voltage and i_{abc} is differentiable until i_{abc} approached zero as shown in Figure 35. From these results the following relationship between V_{abc}, R_{abc} and i_{abc} was established:

$$i_{abc} = \frac{1}{2} \cdot \left(\frac{V_{abc} + 13.56}{R_{abc}} \right) \tag{5.15}$$

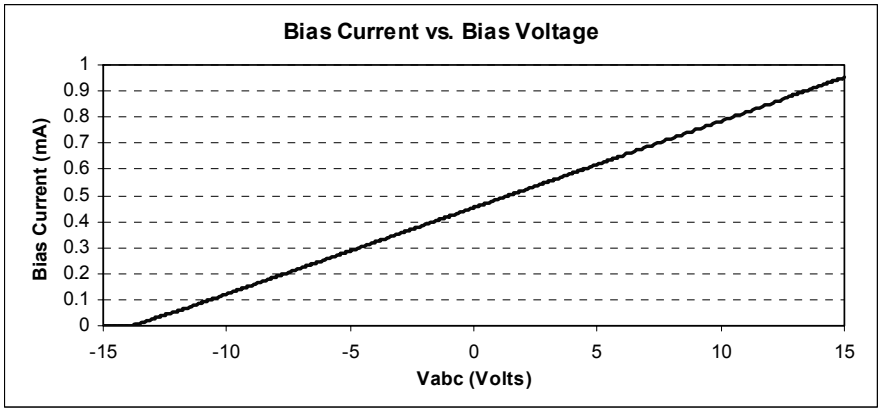

Figure 35: Bias Current versus Bias Voltage

The approximation in equation (5.15) is close to the simulation results deviating only as the bias current becomes very close to zero. This is due to a non-linear roll-off of the bias current when compared to the bias voltage applied. Reasonable accuracy is obtained from -13 volt to +15 volt bias voltage. The upper limit is due to device limitations. The next simulation analyzed the change in effective resistance with the transconductance gain. This is what allows remote control and configuration of line parameters.

A simulation was conducted where V_{abc} was varied to change the effective resistance while holding the line voltage constant. Figure 36 shows simulation and theoretical results from (5.13). The effective resistance was computed from the simulation results using (5.14). These results show the controllability of resistance through the bias current over a wide range. More specifically, the effective resistance can be varied over two orders of magnitude.

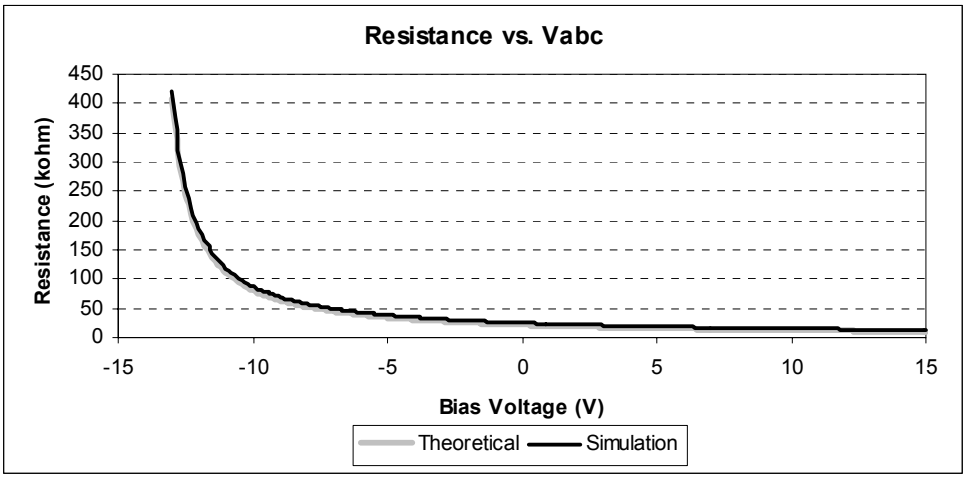

Figure 36: Simulated and Theoretical Effective Resistance vs. Bias Voltage

The simulation results are fairly close to the theoretical with most of the error coming from the internal OTA offset voltage and a voltage offset present in the buffered output of the LM13700 OTA.

More simulations were run to analyze the consistency of the resistance. While maintaining a constant bias current, or effective resistance, the circuit was subjected to varying line voltages. Figure 37 shows results from multiple sweeps of the line voltage with different bias currents. The plot shows line current vs. line voltage. The slope of this plot is the effective resistance of the circuit. For an ideal resistor the slope of the resulting line should be constant.

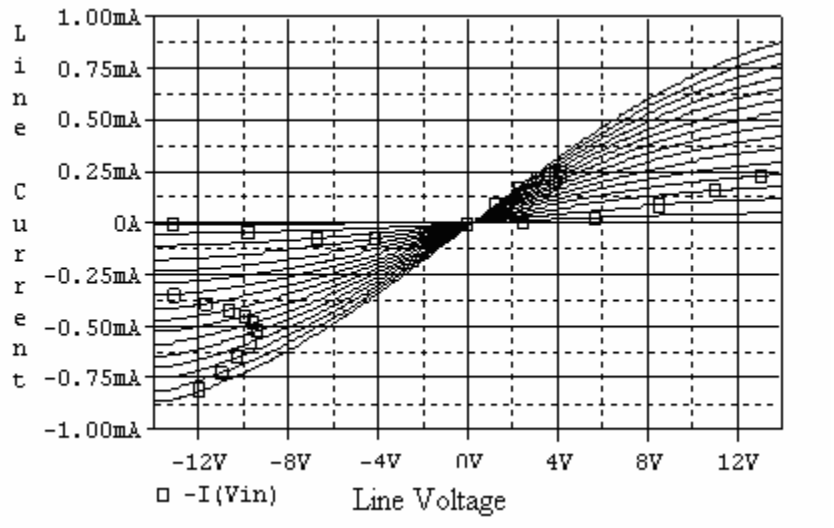

Figure 37: SW Line Current vs. Line Voltage

As seen from the above plot when the line voltage is between approximately ± 4 volts the slope, or effective resistance, remains constant. Beyond that the gain of the OTA begins to saturate. Figure 38 shows the same plot zoomed in on the linear range.

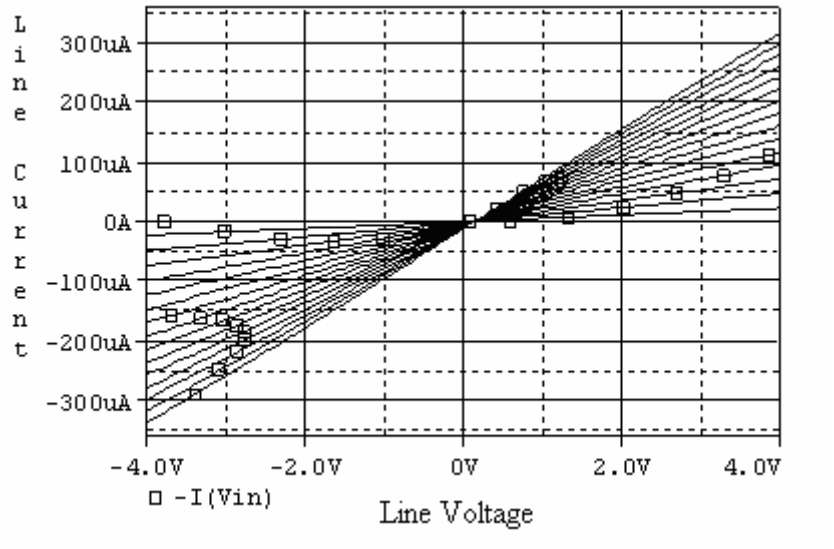

Figure 38: SW Line Current vs. Line Voltage (Linear Region)

The saturation of the circuit is dependant on two factors, the bias current and the throughput current. The effective resistance has a variance of less than ±1% with throughput current 30% or less of the bias current. Complete saturation occurs when the throughput current is equal to the bias current. Further examination of Figure 38 reveals an offset in the circuit behavior. The current is nonzero when the line voltage is zero. The magnitude of this offset is quantified by equation (5.6). This behavior is problematic as the effective resistance of the circuit governed by ohms law becomes nonlinear. The computation of the effective resistance from the simulation results is shown in Figure 39 and exhibits anomalous behavior as the line voltage approaches zero.

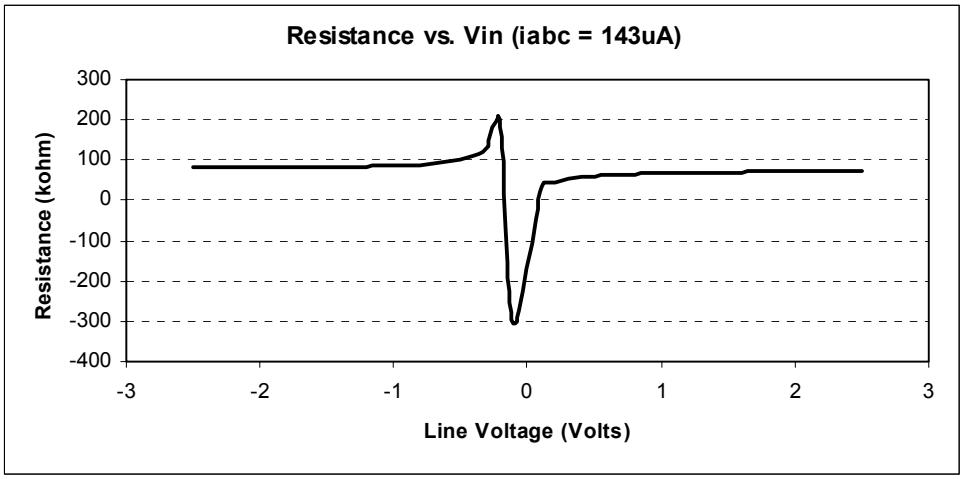

Figure 39: Effective Resistance from PSpice Simulation

Ideally the effective resistance would be constant throughout a wide line voltage applied to the circuit. The only way to achieve this, or come close to achieving this, is to eliminate the offset current present in the circuit. A method for eliminating this offset was mentioned earlier and with the recognition of this sufficient offset cancellation the

data was corrected mathematically in a manner representing the elimination of the offset quantified by (5.6) to analyze the circuit performance with offset compensation. The corresponding results are much better. Figure 40 shows effective resistance versus line voltage for various bias current settings corrected for the offset. The asymptotic behavior is eliminated and the resistance exhibits a variance of approximately 1% with a line voltage magnitude of 2.5 volts or less.

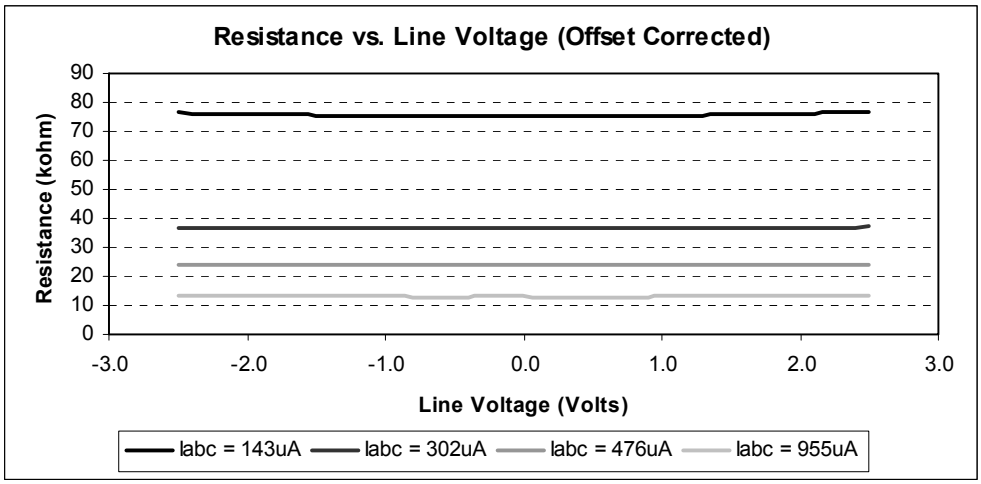

Figure 40: SW Effective Resistance vs. Line Voltage

Overall the simulation results verify the circuit functionality as a controllable variable resistor. The circuit was also constructed in hardware and tested.

5.3.2 HARDWARE RESULTS

The OTA based variable positive resistor was constructed in hardware using the LM13700 OTA and tested. The hardware tests run were similar to the PSpice simulations for comparison. Figure 41 shows the effective resistance of the circuit,

which was calculated from measurements, versus the bias voltage from both the hardware test and software simulation. The hardware exhibits similar controllable resistance as the software simulations with only slight deviation from simulation results. Analysis shows the offset voltage present in hardware is slightly higher, and subsequently closer to the data sheet specifications, than the PSpice model resulting in this discrepancy.

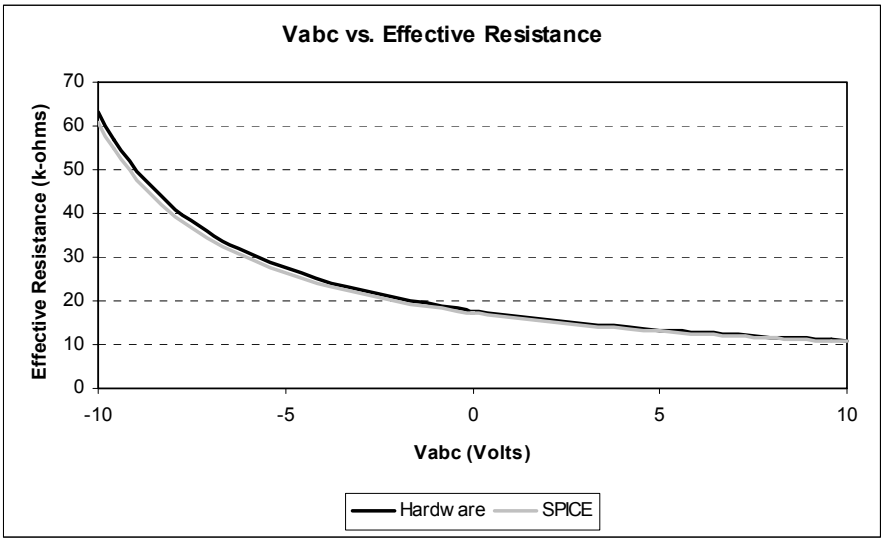

Figure 41: Hardware and PSpice Effective Resistance vs. Bias Voltage

Multiple hardware tests were conducted to analyze the saturation effects of the circuit. The circuit was configured with a constant bias current and subjected to a varying line voltage. Figure 42 plots the line current versus the line voltage from these tests for eight different effective resistance configurations. The slope of the plots is indicative of the effective resistance and is constant for a limited line voltage range before saturation effects are noticeable. This is very similar to the simulations results. Approximately the same variance of less than ± 1% for line currents at 30% or less of bias current was exhibited in hardware. Figure 43 shows line current and the linear trend

line of this line current plotted against line voltage. This is indicative of how linear the response is and how it deviates only slightly in this range. This linearity is exhibited in the effective resistance of the circuit.

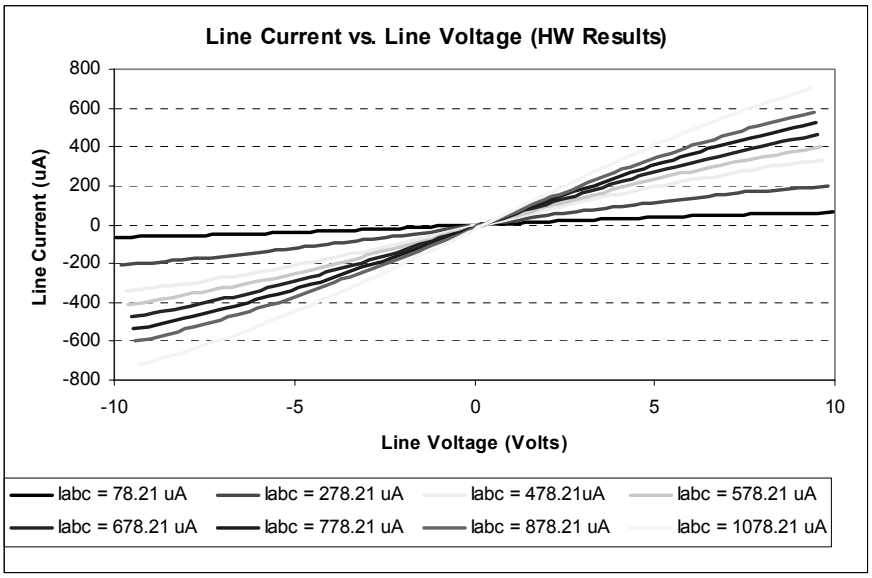

Figure 42: HW Line Current vs. Line Voltage for Various Bias Currents

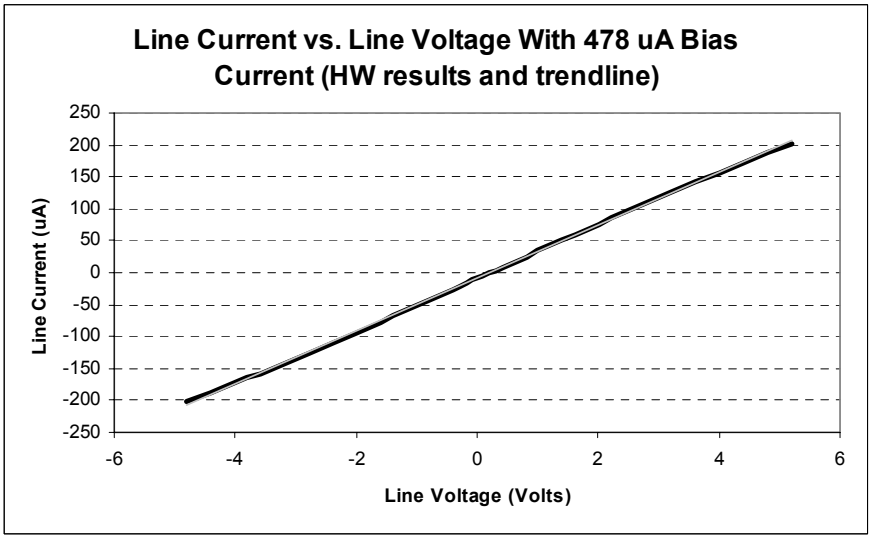

Figure 43: HW Line Current Linearity

The effective resistance is plotted against line voltage in Figure 44. With the line voltage range between ± 2.5 volts the variance of the effective resistance was less than 1%. This is an accurate range for operation of this model in this configuration. The line model becomes less accurate and saturation effects become more severe, as the line current magnitude approaches the bias current magnitude. From the software and hardware results the linear range for this model, defined by < 1% variance of effective resistance, is quantified by the following relationship:

$$i_{line} \leq 0.3 \cdot i_{abc} \tag{5.16}$$

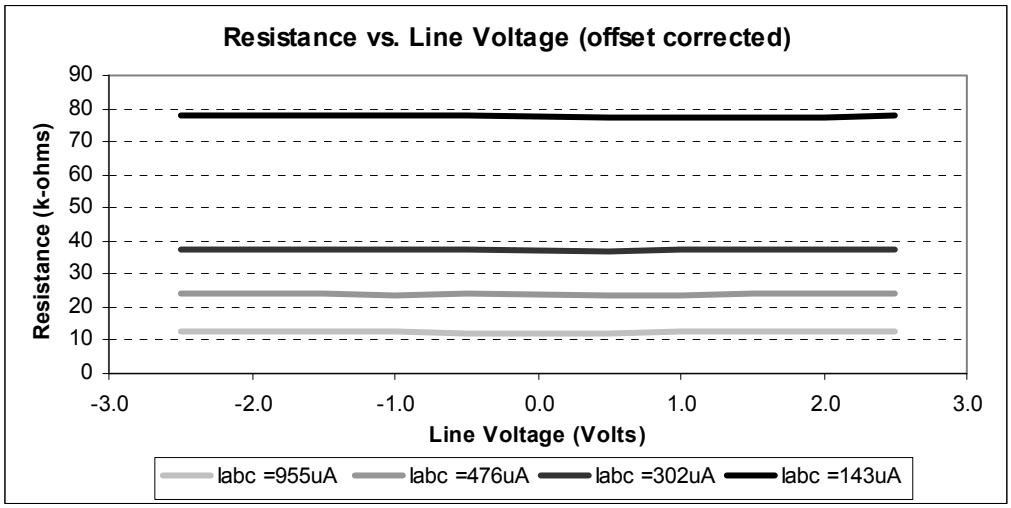

Figure 44: Hardware Effective Resistance vs. Line Voltage

Within device limitations the line voltage can be any magnitude so long as the relationship in (5.16) holds is maintained. This is advantageous as the linear operating voltage range has been significantly increased from a basic open loop OTA with the use

of feedback. This will allow easy measurement of the bus voltages in an emulation network. Overall the results from both simulation and hardware were very similar and verify the operation, control and linear operating conditions of this OTA based variable positive resistor. The next section deals the negative resistance circuit.

5.4 NEGATIVE OTA VARIABLE RESISTOR

A variable negative resistance circuit is required to properly emulate and allow reconfiguration for the shunt capacitive element in the line models. The same basic approach was taken as with the OTA based variable positive resistor circuit. Altering the feedback to the double ended variable positive resistor produces the input and output characteristics of a negative resistor. This circuit is shown in Figure 45. The derivation of the circuit behavior is conducted in the same manner as before.

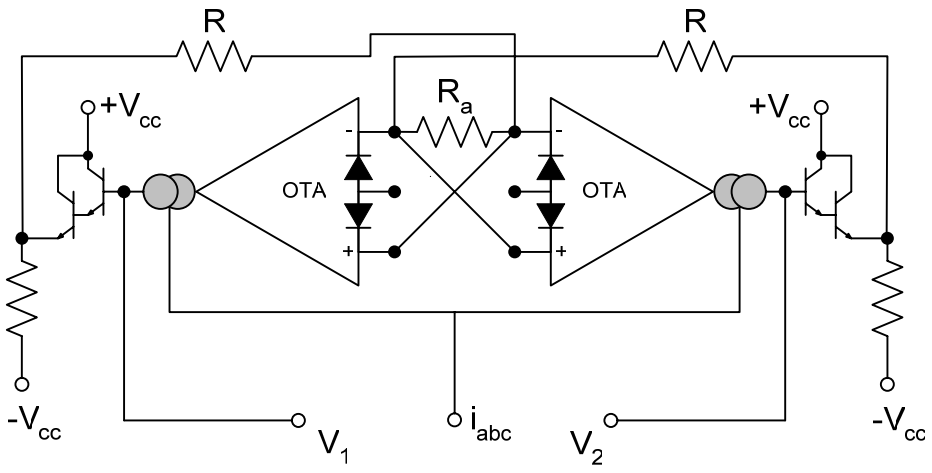

Figure 45: Double Ended OTA Variable Negative Resistor

This circuit is symmetrical just like the variable positive resistor. The behavior is examined by looking at one of the OTAs recognizing that the second has the inverse behavior. The input voltage $V_1 - V_2$ is attenuated by the resistors to provide an input voltage to the terminal of the OTA on the right side:

$$v_{in} = -(V_1 - V_2) \cdot \frac{R_a}{2R + R_a} \tag{5.17}$$

The negative sign is a result of the change of polarity at the input of the OTA as compared to the positive resistor circuit. The output current of the OTA is governed by:

$$i_o = -(V_1 - V_2) \cdot \frac{g_m \cdot R_a}{2R + R_a} \tag{5.18}$$

The effective resistance seen at the terminals is defined as:

$$R_{eff} = \frac{(V_1 - V_2)}{i_0} = -\frac{2R + R_a}{R_a \cdot g_m} \tag{5.19}$$

This circuit behaves in the same manner as the variable positive resistor with a change in the direction of the current flow with respect to the voltage applied. This effectively creates a negative resistance behavior at the terminals of the circuit. The design was verified through simulation and hardware testing utilizing the same LM13700 OTA.

5.4.1 SIMULATION RESULTS

Three simulation tests were run on the OTA based variable negative resistor circuit and were similar to the tests performed on the variable positive resistance circuit. The first simulation varied the bias current with a fixed line voltage to evaluate the controllability of effective resistance of the circuit. This was compared with the theoretical value in (5.19). The second simulation swept the line voltage across a wide range while holding the bias current constant to evaluate the saturation effects of the circuit and the final test evaluated the consistency of the effective resistance of the circuit while varying the line voltage. The circuit used for the simulations is shown in Figure 46.

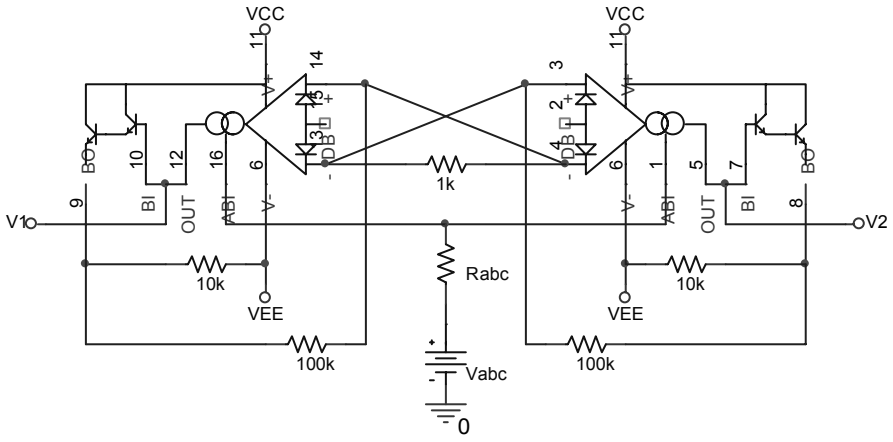

Figure 46: PSpice Schematic for OTA Based Variable Negative Resistor

The bias current was controlled via a bias voltage and bias resistor and is governed by equation (5.15). Figure 47 plots the effective resistance from both simulation results and theoretical computation for a fixed line voltage. This verifies the negative resistance behavior and shows controllability of negative resistance over a wide

range. The simulation results are fairly close to the theoretical with most of the error coming from the internal OTA offset voltage and a voltage offset present in the buffered output of the LM13700 OTA.

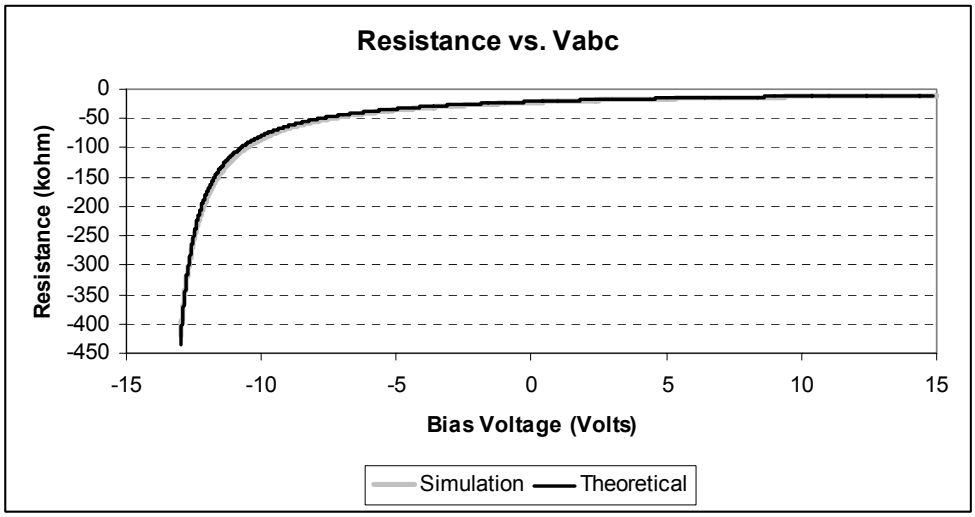

Figure 47: Simulated and Theoretical Effective Resistance vs. Bias Voltage

More simulations were run to analyze the consistency of the effective resistance. While maintaining a constant bias current the circuit was subjected to varying line voltages and the line current measured. Figure 48 shows results from multiple sweeps of the line voltage with different bias currents. The plot shows line current vs. line voltage and the slope of the plot is indicative of the effective resistance. For an ideal resistor the slope of the resulting line should be constant.

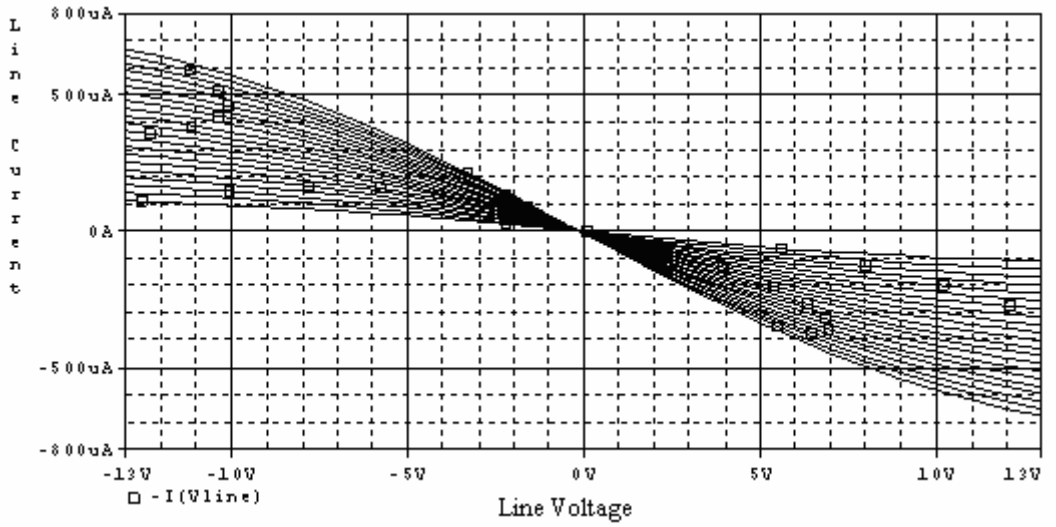

Figure 48: SW Line Current vs. Line Voltage

The effects of OTA saturation on the effective resistance, slope of the line, in the above plot can be clearly seen. The effective resistance changes as the OTA begins to saturate. The effective resistance is fairly linear in the range of ± 4 volts. This range is shown in Figure 49.

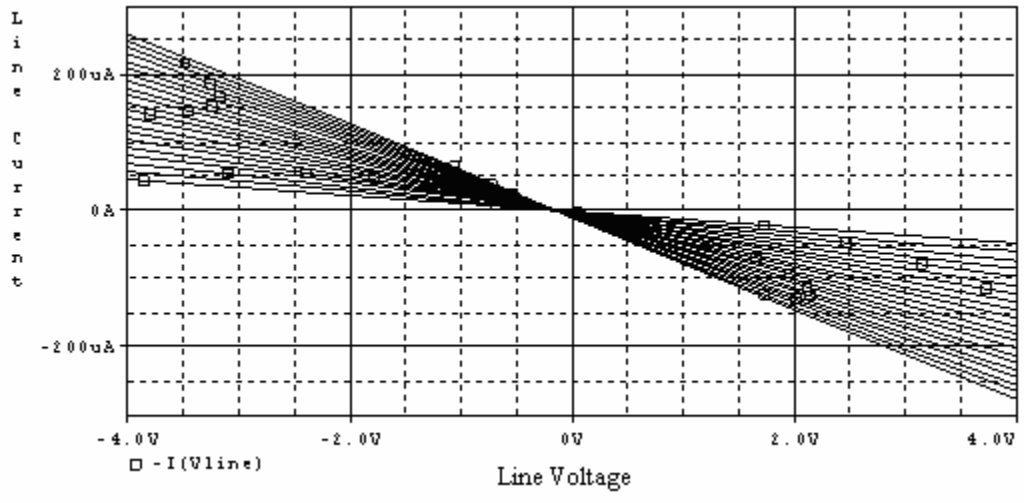

Figure 49: SW Line Current vs. Line Voltage (Linear Region)

The saturation effects for this negative resistor circuit are identical to those seen in the positive OTA resistor. In addition, the same offset from the OTA is present and can be seen in Figure 49 with non-zero line current with zero voltage applied. This is expected as the design of the circuits is so similar and utilizes the same OTA. The following figure plots the offset corrected effective resistance versus line voltage for various i_{abc} and yields good results. The effective resistance does not deviate much with an input voltage between ±2.5 volts.

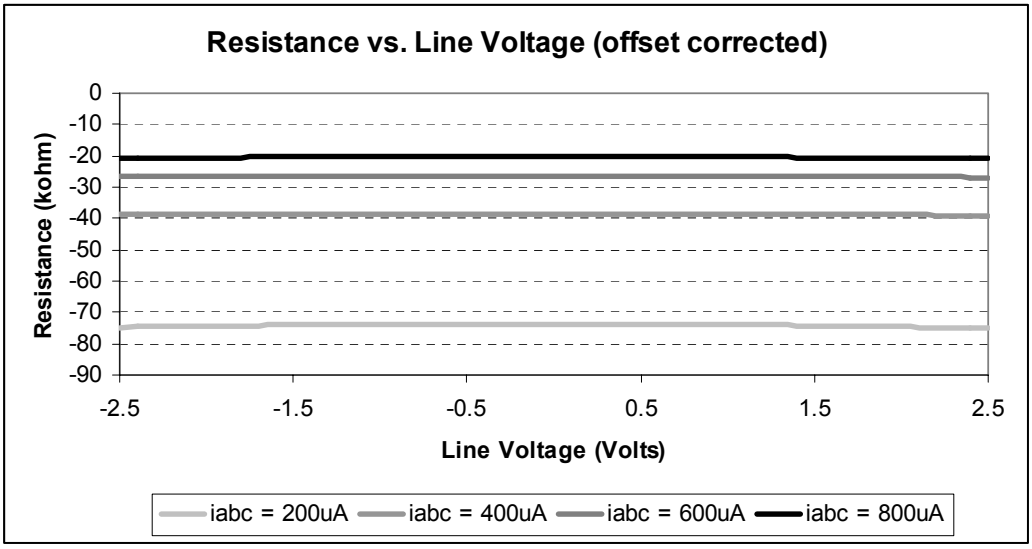

Figure 50: SW Effective Resistance vs. Line Voltage

These simulation results verify the circuit functionality as a controllable variable negative resistor. The circuit was also constructed in hardware and tested in a similar manner.

5.4.2 HARDWARE RESULTS

The OTA based variable negative resistor was also constructed in hardware using the LM13700 OTA and tested. The tests conducted were similar to the PSpice simulations and used for comparison and verification of the circuit performance. In the first test the effective resistance of the circuit was calculated from measurements while varying the bias voltage and holding the line voltage constant. The hardware exhibits similar controllable negative resistance as the software simulations with only slight deviation from simulation results as shown in Figure 51.

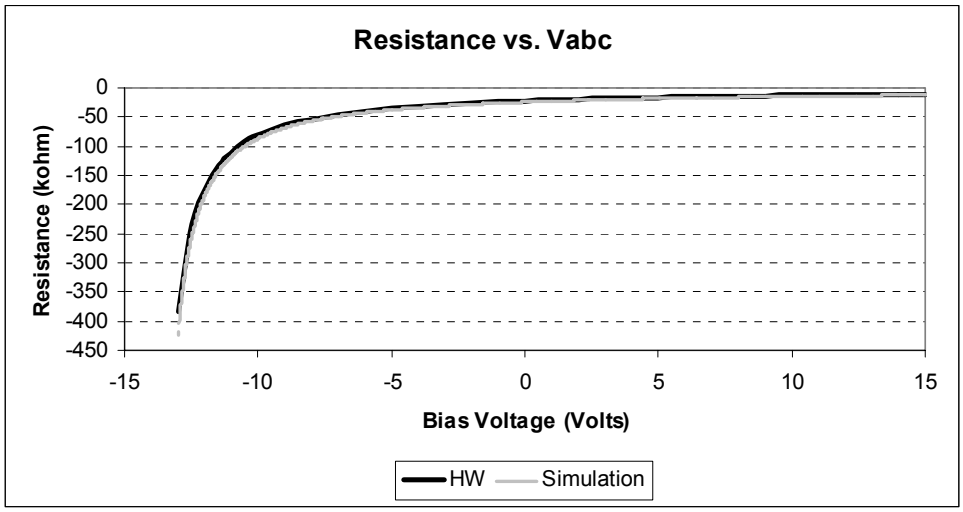

Figure 51: Hardware and PSpice Effective Resistance vs. Bias Voltage

In the next test the bias current was held constant as the line voltage was varied and the line current measured. The slope of the line current versus line voltage plot is the resultant effective resistance of the circuit. Ideally the slope would be constant but the OTA saturation effects limit the linear range. Figure 52 shows the results of this test for five different bias currents and a line voltage sweep from -10 volts to +10 volts. The

circuit is behaving as a negative resistor. With a negative voltage applied the current is positive and with a positive voltage applied the current is negative. The saturation effects are quite noticeable as the line voltage increases but for a limited voltage region the circuit exhibits good linearity of effective resistance. Figure 53 shows the same plot but zoomed into a smaller voltage range which maintains a fairly linear response, or a constant effective resistance.

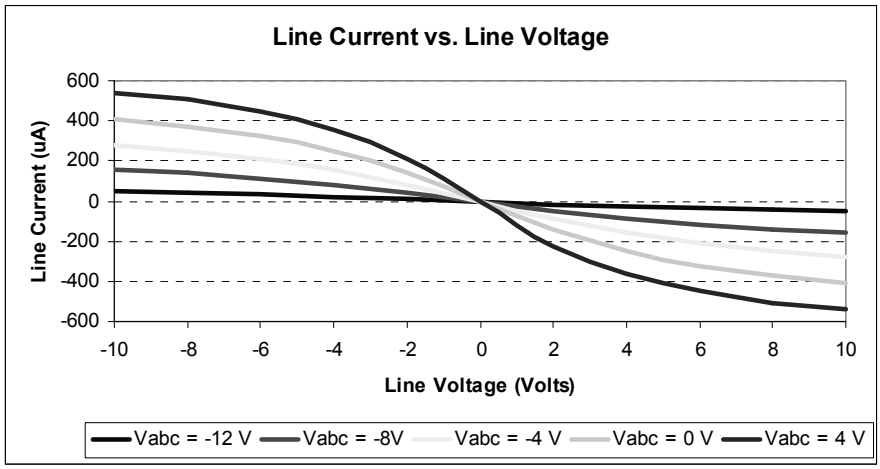

Figure 52: HW Line Current vs. Line Voltage for Various Bias Voltages

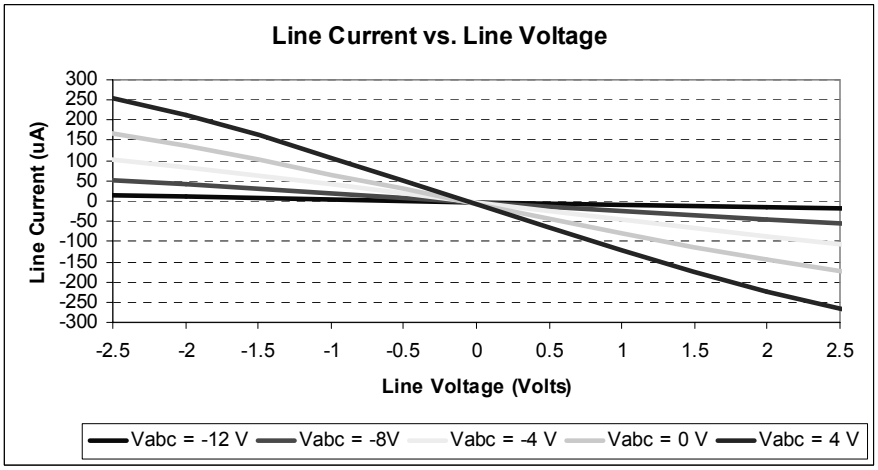

Figure 53: HW Line Current vs. Line Voltage (Linear Region)

Figure 54 plots the measured effective resistance in hardware against the line voltage applied to the circuit. The resistance remains fairly constant with a slight decrease as the line voltage is increased. This follows from the behavior seen in Figure 52 with the slope, or effective resistance, decreasing as the OTAs begin to saturate.

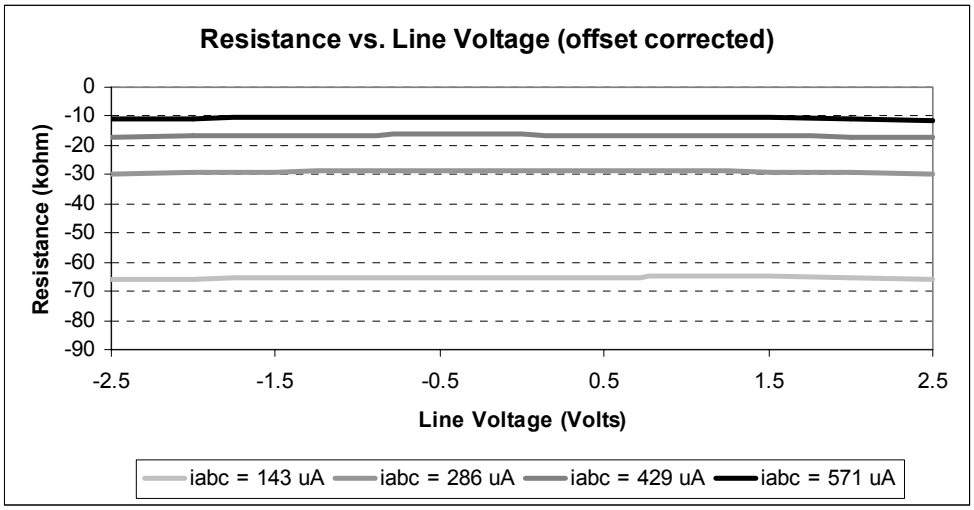

Figure 54: Hardware Effective Resistance vs. Line Voltage

Remotely reconfigurable OTA based variable positive and negative resistance circuits have been developed and verified through software simulations and hardware testing. These are the building blocks necessary to construct the transmission line models for the DC emulation approach presented in chapter 4. The primary concern when configuring these circuit is to ensure the effective resistance is set properly and that the line current is small enough that the circuit does not exhibit saturation effects. The following chapter utilizes these OTA circuits to construct transmission lines for computation of power-flow using the DC emulation scheme. The results are compared to PowerWorld for verification.

6 VERIFICATION OF ANALOG LINE MODELS

6.1 OVERVIEW

This chapter presents test results which verify the application of the analog transmission line models presented in this thesis in power flow computation. This was consummated through hardware testing, software simulation and the evaluation of the subsequent results. For hardware testing purposes a three bus power system network was constructed consisting of the OTA based transmission line circuits presented in chapter 5. Refer to Figure 22 for a one line diagram of a three bus power system. Software simulations were conducted with PSpice with the OTA based circuits. For the tests presented here the real world transmission line parameters, system voltages, currents, and power for that matter, were all required to be scaled according to the limitations of the analog hardware. The devices would saturate or become damaged during emulation if the scaling is not applied properly. Multiple emulation tests were performed in software and hardware and the results are tabulated in this chapter. More specifically test results for the lossless, lossy and pi transmission line models are included. For comparison and error analysis results were compared to the solutions obtained by PowerWorld.

The test results are broken up into two sections. The first section tests the transmission line models in emulation circuitry. The second section connects the analog transmission line emulation circuits, or network module, to the analog load circuitry, or load module.

6.2 PARAMETER SCALING

Through the testing and analysis of the OTA based variable resistor circuits it was recognized that the desirable constant effective resistance is only obtainable within certain limited operating ranges. Specifically the input voltage needs to be within device limitations and the line current proportional to the bias current as shown in equation (5.16). For the test cases presented in this thesis the line parameters were scaled from PowerWorld values such that for the given power flow cases the hardware was within the defined linear operating range. A more specific and robust parameter scaling method would ensure that maximum line currents (failure point of the lines) are scaled within the linear range of the analog circuits. This would ensure a fairly linear effective resistance in the line models for any currents that could be seen in the real world power system.

PowerWorld executes power flow in per unit quantities. For simpler comparison the emulation parameters are scaled directly from the per-unit normalized values in PowerWorld. The data from emulation can then be easily extrapolated to real world values by the analog hardware scaling factors and the base values associated with the per-unit normalization. The voltage, current and impedance from per-unit values are scaled to emulation hardware values by the following scaling factors:

$$\begin{aligned} V_{HW} &= V_{p.u.} \cdot V_k \\ Z_{HW} &= Z_{p.u.} \cdot Z_k \\ I_{HW} &= I_{p.u.} \cdot I_k = I_{p.u.} \cdot \left(\frac{V_k}{Z_k} \right) \end{aligned} \tag{6.1}$$

where the subscript “HW” indicates analog hardware values, the subscript “p.u.” per-unit values and the subscript “k” scaling factors.

Three scaling factors are detailed above but only two are necessary to convert the per-unit power system values to analog hardware values. In this thesis the two scaling factor chosen are V_k and Z_k. The scaling factor I_k is derived from V_k and Z_k.

6.3 PROTOTYPE NETWORK MODULE

A prototype network module consisting of OTA based variable resistor circuits was built in hardware. This board was designed to emulate a three bus power system for the lossless and lossy transmission line models. It consists of four three bus networks. Two of the networks are used for the lossless lines and all four for the lossy line model as outlined in chapter 4. In addition the board can also emulate a single shunt element transmission line. Figure 55 shows the layout of the prototype network module.

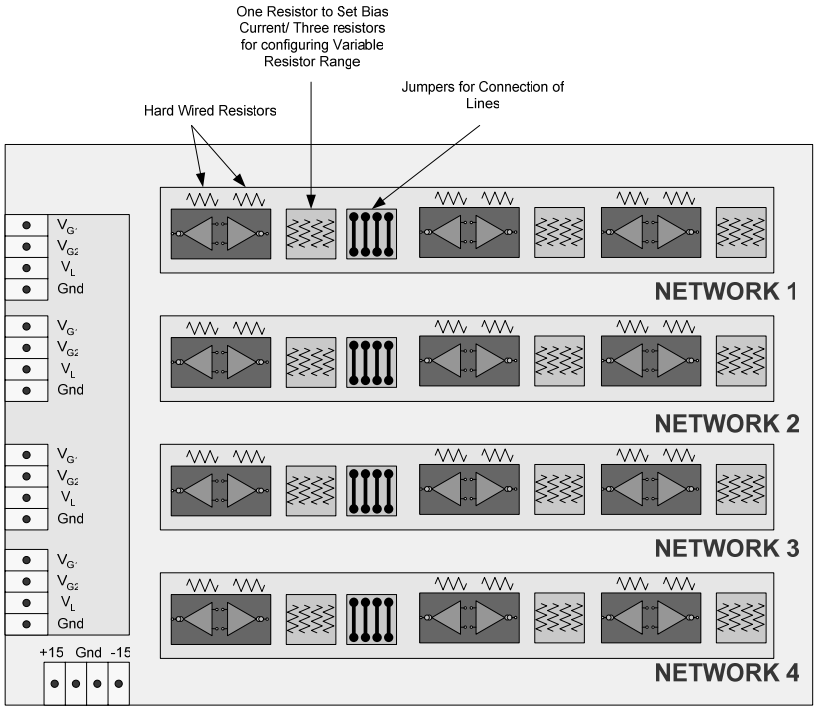

Figure 55: Network Module Layout

The board consists of twelve OTA based variable resistor circuits making up the four DC emulation networks. Each network represents an emulation circuit for a three bus power system (three transmission lines). There are jumpers which allow different connections of the lines or the removal of a line (line failure contingency). Furthermore each transmission line circuit is reconfigurable by resistors in an 8-pin DIP socket and the biasing current. The resistors which can be interchanged are the three resistors in the feedback loop and the bias resistor. For simpler control the bias resistor is tied to the +15 volt supply. In this configuration the bias current is set by the bias resistor value. Another option is to use an external voltage source for remote control of line parameters.

Both methods were utilized in this work and a National Instruments analog output card interfaced with LabVIEW was used for the remote control of line parameters.

The layout and connections for a single emulation network on the prototype board in relation to a three bus power system is shown in Figure 56.

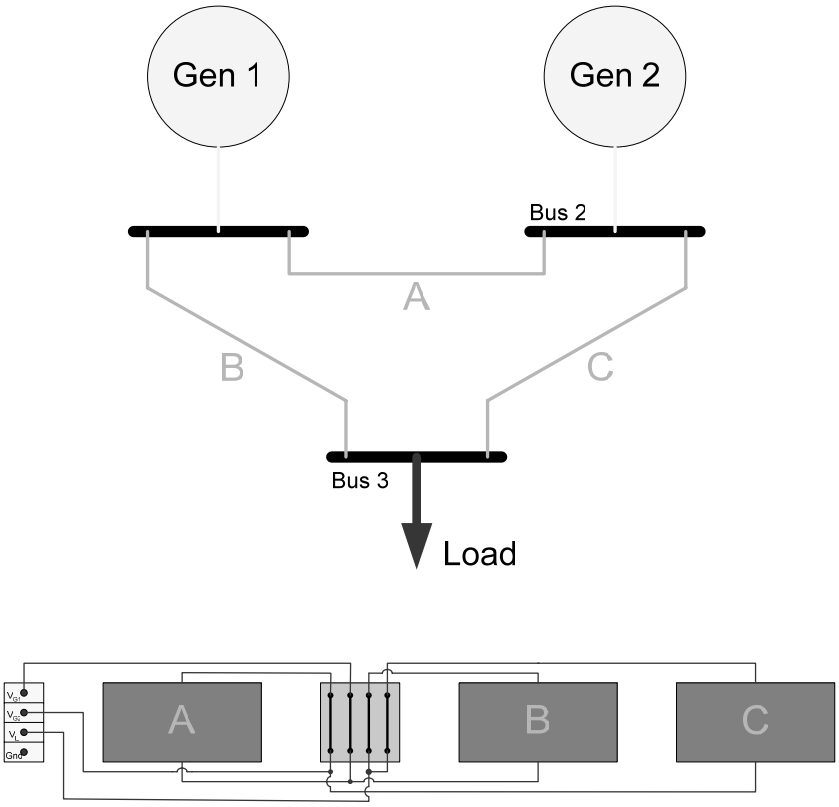

Figure 56: Emulation Network and a Three Bus Power System

A picture of the actual prototype is shown in Figure 57 with the DC emulation networks and transmission lines labeled.

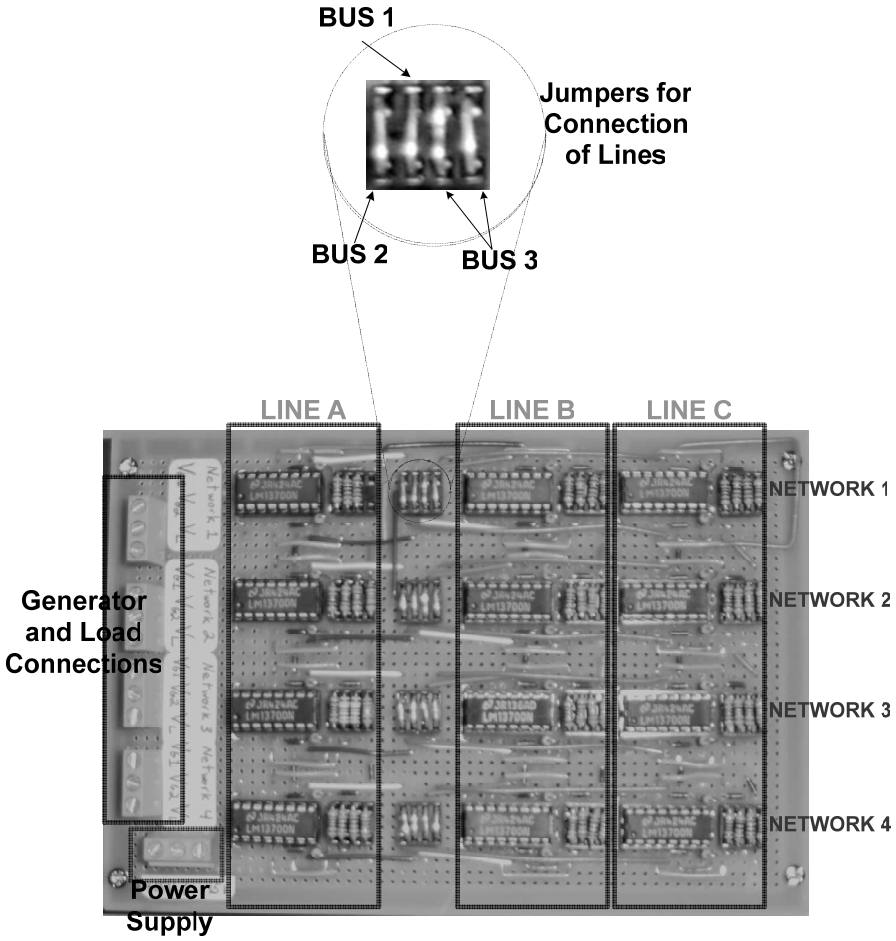

Figure 57: Prototype Network Module

6.4 NETWORK MODULE TESTING

This section tabulates results from tests performed on the network module. For these tests the generators and loads were modeled as DC voltage sources. The appropriate values for these sources were obtained from the simulations conducted in PowerWorld along with the analog hardware scaling factors. The effective resistance values for the network module were determined based on the line impedances in PowerWorld, the analog hardware scaling factors, and the equations in chapter four pertaining to whichever analog line model is utilized in emulation. Ideally with the

appropriate bus voltages applied to a properly configured network module the line currents and currents injected into the network should be equivalent to those computed with PowerWorld.

The current was measured in hardware via current sensing resistors and instrumentation amplifiers. The circuit for a single current measurement is shown in Figure 58.

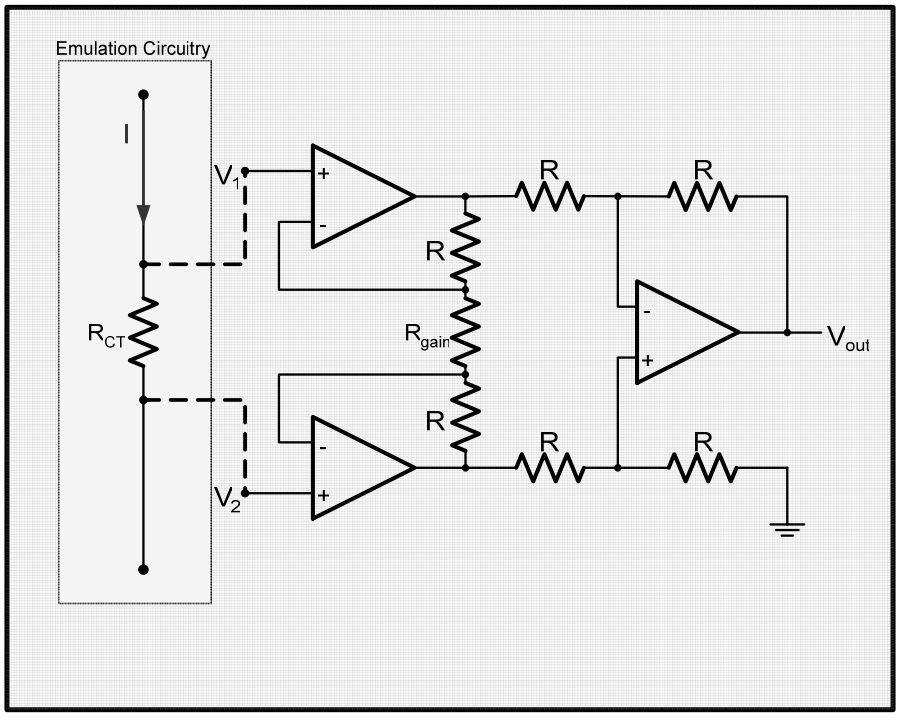

Figure 58: Current Measurement Circuit

The current sensing resistor, R_{CT}, is placed in series with a component in the emulation hardware and the voltage across this resistor, which is proportional to the current through the emulation component, is sensed by a differential amplifier and

conditioned into a single ended output for data acquisition. The following equation relates the output, V_{out}, to the current flow:

$$V_1 - V_2 = I \cdot R_{CT}$$
$$V_{out} = I \cdot R_{CT}\left(1 + \frac{2R}{R_{gain}}\right) \tag{6.2}$$

The circuit consists of two amplifier stages. The gain of the differential amplifier stage is set by the values of R and R_{gain} while the second stage is a unity gain amplifier which converts the differential voltage to a voltage with respect to ground. The input impedance to the primary stage is very high in order to mitigate any current draw from the emulation circuitry which would lead to errors in computation. In addition, the current sensing resistors are lumped into the effective resistance of the line models as shown in Figure 59. This alleviates any issues of altering the resistance of the circuit with the current sensing resistors.

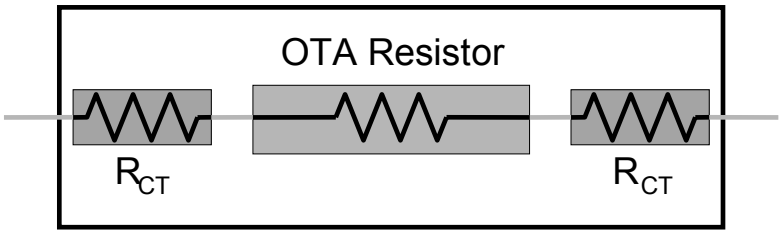

Figure 59: OTA Variable Resistor with Current Sensing Resistors

The resistance of R_{CT} is two to three orders of magnitude less than the effective resistance of the OTA circuit. This ensures the effective resistance of the circuit is still

controllable over a wide range via the bias current. The effective resistance of this OTA circuit with the additional current sensing resistors is governed by:

$$R_{eff} = 2 \cdot R_{CT} + R_{OTA} \tag{6.3}$$

where R_{OTA} is the effective resistance of just the OTA circuit.

The next few sections present results for the testing of the network module with different analog line models.

6.4.1 LOSSLESS LINE MODEL

Hardware results for lossless transmission line models are presented in the appendix.

6.4.2 LOSSY LINE MODEL

The network module was configured for a three bus lossy power system and tested. For the testing of the lossy transmission line network the effective resistance was set using LabVIEW software user interface and a National Instruments analog output card. Two cases were setup and run in both PowerWorld and the analog emulator. In each of these cases the transmission lines remained unchanged but the states of the power system were different. One example is outlined in this section and the results of the second case are located in the appendices. Bus one in the three bus system was modeled as the slack bus, the generator on bus two was modeled as a PV bus and the load on bus

three was modeled as a PQ bus. The PowerWorld system with results for this case is shown in Figure 60.

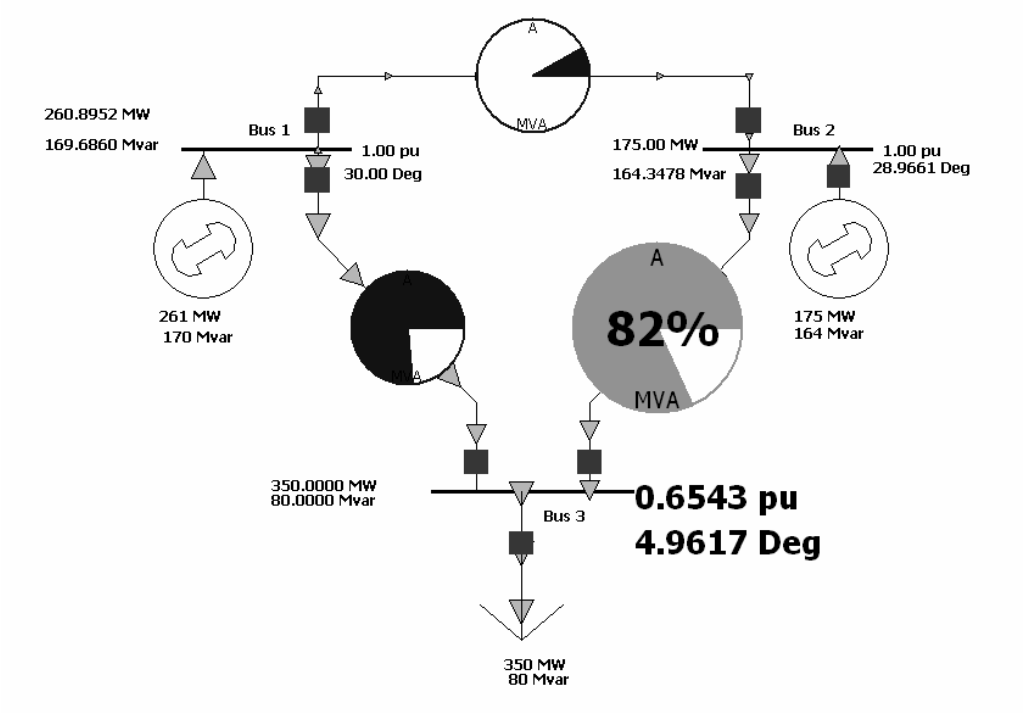

Figure 60: PowerWorld Simulation Results with Lossy Lines

Table 3 details the power system parameters results from the PowerWorld simulation:

Table 3: Simulation Details for Lossy Network

PowerWorld Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8660	0.5000	V p.u.
Bus 2 Voltage	0.8749	0.4843	V p.u.
Bus 3 Voltage	0.6518	0.0566	V p.u.
Generator 1	260.90	169.69	MW/MVAR
Generator 2	175.00	164.35	MW/MVAR
Load	350	80	MW/MVAR
T Line A	0.02	0.22	ohms p.u.
T Line B	0.06	0.15	ohms p.u.
T Line C	0.05	0.19	ohms p.u.

The scaling factors for the analog emulation were chosen as follows: $V_k = 2$, $Z_k = 16000$, and $I_k = 0.000125$. Using these scaling factors, PowerWorld parameters and equation (4.15) the analog transmission lines were configured as per Table 4. For example the effective resistance for the real component of line A was computed with equations (4.15) and (6.1) as follows:

$$R_{\mathrm{Re}(12)} = \frac{R_{12}^2 + X_{L12}^2}{R_{12}} \cdot Z_k = \frac{(0.02)^2 + (0.22)^2}{0.02} \cdot 16000 = 39040 \tag{6.4}$$

The other resistors were sized in a similar manner. The scaling factors were chosen in a manner to keep the OTA circuits operating in a fairly linear manner as discussed before.

Table 4: Emulation Parameters for Lossy Transmission Lines

Line Configuration						
Real Networks						
Line	Reff	Iabc(uA)	Rabc	Vabc	R	Ra
A	39k	188.9	10k	-9.78	71.5k	1k
B	7k	828.3	10k	3.01	47.5k	1k
C	12.4k	681.4	10k	0.07	71.5k	1k
Imaginary Networks						
Line	Reff	Iabc(uA)	Rabc	Vabc	R	Ra
A	3.5k	969.3	10k	5.83	14.7k	500
B	2.8k	843.6	10k	3.31	10k	500
C	3.3k	731.6	10k	1.07	10k	500

Table 5 details the emulation bus voltages determined by scaling factor V_k and PowerWorld results:

Table 5: Emulation Bus Voltages for Lossy Transmission Line Test

Emulation Bus Voltages		
Bus	Real	Imaginary
1	1.73	1.00
2	1.75	0.97
3	1.30	0.11

The emulation hardware was configured, bus voltages applied and line currents measured and tabulated in Table 6 and Table 7.

Table 6: Emulated Line Currents for Lossy 3 Bus Network

Hardware Results								
	Actual Line Current (uA)				Line Current Offset (uA)			
Line	Network 1	Network 2	Network 3	Network 4	Network 1	Network 2	Network 3	Network 4
A	-1	6	-7	0	-1	-3	-3	-1
B	68	320	156	133	5	5	5	5
C	43	266	143	76	6	6	6	6

Table 7: Offset Corrected Emulation Line Currents

Emulation Results (offset corrected)					
Line	I Real (uA)	I Imag (uA)	Device	Real	Imaginary
A	9	5	Gen 1	387	-18
B	378	-23	Gen 2	288	-72
C	297	-67	Load	675	-90

The offset corrected results converted into per-unit values via the scaling factors are compared directly to the PowerWorld results in Table 8. The results are good and show marked improvement over the results for the lossy line model cases. This improvement is attributed to the more precise control of line parameters through LabVIEW and analog power supplies. The difference in the magnitude of the currents is not more than 4 hundredths of a volt and the phase angle is typically within half a degree

with the exception of the line A current. The phase angle is off because the line current in the analog hardware is proportional to the error seen in the measurement circuitry.

Table 8: Error Analysis on Emulation Results for 3 Bus Lossy Network

PowerWorld and Analog Emulation Comparison (A p.u.)						
	PowerWorld Current		Analog HW Current		Difference	
	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase
Line A	0.08	34.68	0.08	23.96	0.00	10.71
Line B	3.05	-3.98	3.03	-3.48	0.02	0.50
Line C	2.46	-12.80	2.44	-12.71	0.02	0.09
Generator 1	3.11	-3.04	3.10	-2.81	0.01	0.23
Generator 2	2.40	-14.24	2.37	-13.85	0.03	0.39
Load	5.49	-7.91	5.45	-7.59	0.04	0.32

The results from the second 3 bus case with lossy transmission lines are located in the appendix. The next section includes hardware results for the full pi transmission line model.

6.4.3 PI LINE MODEL

For the testing of the full pi transmission line model the prototype board was used to test a single line segment in hardware. This required all twelve OTA variable resistor circuits on the prototype board to emulate this single line. For a three bus power system PSpice was used to simulate the full pi transmission line model. The simulation results are located in the appendices.

For the single pi line test voltage sources were attached at both ends of the line and currents through the shunt and series elements were measured. The diagram below shows the test configuration for one of the four DC emulation networks.

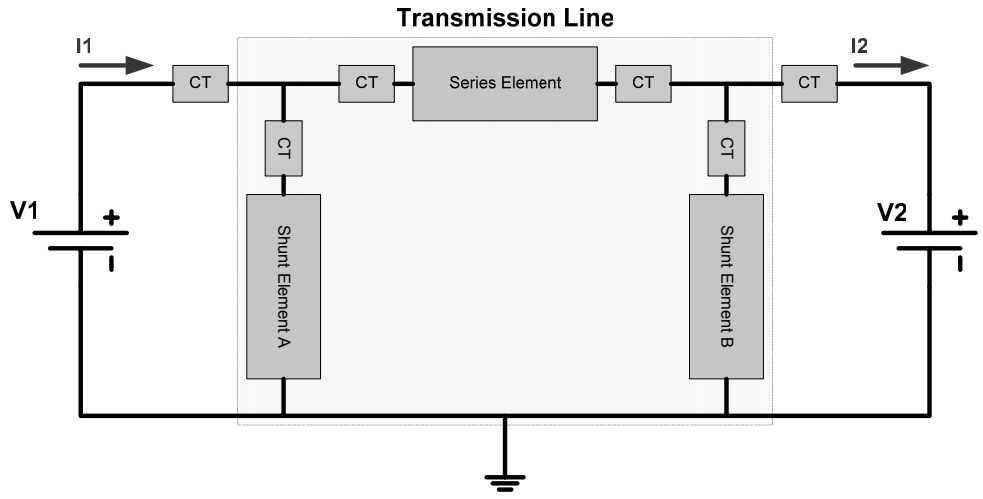

Figure 61: Single Pi Transmission Line HW Test Setup

The power system parameters for the transmission line and terminal voltages are outline in Table 9. The analog hardware was configured based on this data, the emulation scaling factors, and equations (4.15) and (4.20). Details on the OTA circuit configuration are given in Table 10 and Table 11. The scaling factors V_k and Z_k were chosen as 2 and 14000 respectively to keep the OTA circuit operating in the linear region during emulation.

Table 9: Power System Parameters for Pi Line HW Test

Power System Parameters				
		Real	Imag	
V1		1	0	V p.u.
V2		0.708205	-0.19932	V p.u.
Pi Line	series	0.06	0.15	ohms p.u.
	shunt	50	5	ohms p.u.

Table 10: Pi Line Emulation Parameters

Network Parameters (ohms)			
		Real	Imag
Pi Line	series	6090	2436
	shunt	700000	-70000

Table 11: Emulation Parameters for Pi Transmission Line

Emulation Configuration								
			R	Ra	Ibias(uA)	Vbias	Rabc	
Pi Line	series	real	23.75k	1k	454	-6.79	7.48k	Network 4
			31.6k		621	-4.26	7.48k	Network 1
		imag	7.5k	1k	401	-7.56	7.48k	Network 2
					425	-7.23	7.48k	Network 3
	shunt	real	1000k	1k	515	-3.33	4.99k	Network 4
			1000k	1k	182	-10	4.99k	Network 1
		imag	200k	1k	700	0.386	4.99k	Network 2
			143k	1k	263	-8.39	4.99k	Network 3

The results from the emulation of the pi line are detailed below. The offset corrected results from the hardware were compared to Ybus computed results. The terminal voltages are known and the Ybus was constructed based on the transmission line parameters.

$$\begin{bmatrix} I_1 \\ -I_2 \end{bmatrix} = \left[Y_{BUS} \right] \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{6.5}$$

Table 12: Emulated Line Currents for Pi Transmission Line

Emulation Results (uA)							
Network Currents (Network 1)				Network Currents (Network 3)			
	Offset	Measured	Corrected		Offset	Measured	Corrected
series	3	100	97	series	3	242	239
shunt A	2	5	3	shunt A	-2	-31	-29
shunt B	2	4	2	shunt B	-2	-22	-20
Network Currents (Network 2)				Network Currents (Network 4)			
	Offset	Measured	Corrected		Offset	Measured	Corrected
series	2	168	166	series	3	70	67
shunt A	6	6	0	shunt A	-4	-4	0
shunt B	4	15	11	shunt B	-4	-5	-1

The line currents measured in the four networks were converted into rectangular coordinates using equation (4.6) , converted to per unit by the analog scaling factors and then compared directly to the Ybus results. Table 14 details the magnitudes and phase results from the Ybus method and DC networks in per unit and degrees respectively.

Table 13: Ybus and Emulation Current Injections

	DC Network (scaled uA)		DC Network (p.u.)		Ybus Method (p.u.)	
	Real	Imag	Real	Imag	Real	Imag
I1	266	143	1.86	-1.00	1.84	-1.02
I2	250	191	1.75	-1.34	1.76	-1.36

Table 14: Emulation Error for Pi Transmission Line HW Test

	DC Network		Ybus Method		Difference	
	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase
I1	2.11	-28.26	2.10	-29.02	0.01	0.76
I2	2.20	-37.38	2.22	-37.59	0.02	0.21

The offset corrected results from emulation are very close to the Ybus computed valued. The difference in magnitude and phase are both small. Overall the full pi transmission line model for DC emulation functions well in hardware. The following section includes emulation circuitry of the loads in emulation.

6.5 NETWORK AND LOAD EMULATOR TESTING

The prior tests concentrated on testing the transmission lines independently. This section takes this a step further by incorporating analog emulation hardware modeling the loads. The tests were conducted using the network module and an OTA based constant current load module. The generators are represented by DC voltage sources as before.

For testing the network and load modules all parameters were set according to the PowerWorld system parameters and analog emulation scaling factors. Lossless transmission line models and OTA based constant current load models were used. The appropriate generator voltages were applied to the network and the load bus voltage measured and compared with the results from PowerWorld.

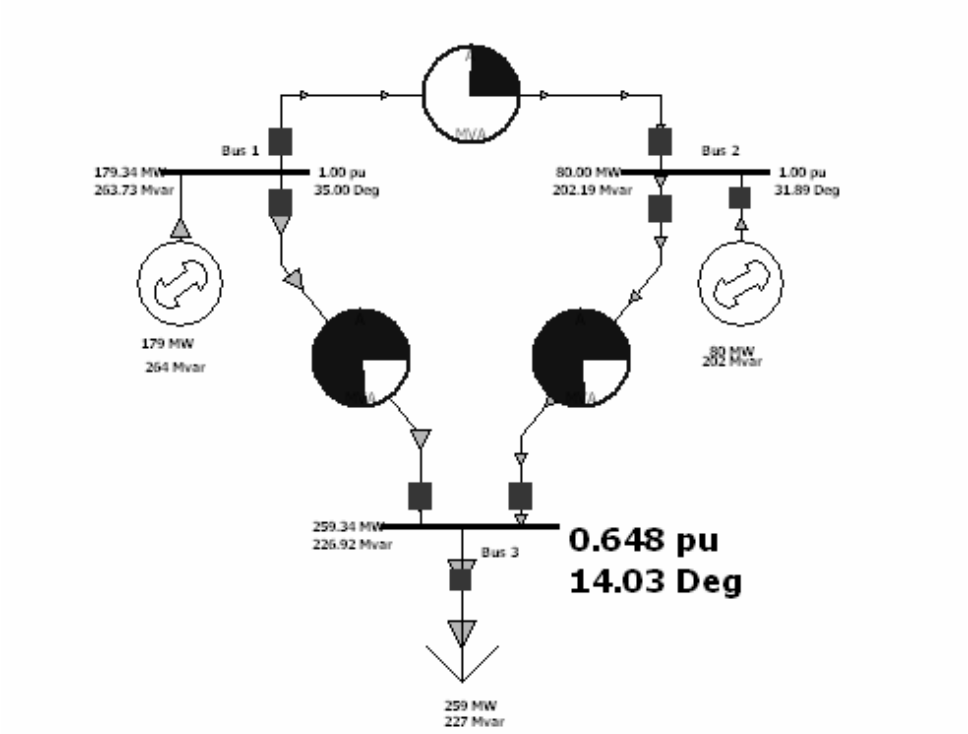

Figure 62: PowerWorld Results for Network and Load Module Emulation

Table 15: PowerWorld Parameters and Results

PowerWorld Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8192	0.5736	V p.u.
Bus 2 Voltage	0.8491	0.5283	V p.u.
Bus 3 Voltage	0.6287	0.1571	V p.u.
Generator 1	179.34	263.73	MW/MVAR
Generator 2	80	202.19	MW/MVAR
Load	400	350	MW/MVAR
T Line A	0	0.22	ohms p.u.
T Line B	0	0.15	ohms p.u.
T Line C	0	0.19	ohms p.u.

The same transmission line configuration that was used is detailed in Table 20 in the appendices. Table 16 and Table 17 outline the emulation parameters, results and error analysis.

Table 16: Emulation Parameters and Results

Emulation Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	1.6383	1.1472	V
Bus 2 Voltage	1.6981	1.0566	V
Bus 3 Voltage	1.2573	0.3142	V
T Line A	0	22	kohms
T Line B	0	15	kohms
T Line C	0	19	kohms
I load	94.6	48.6	uA
Vload (measured)	1.290	0.330	V

Table 17: Error Analysis on Emulation with Network and Load Modules

PowerWorld and Analog HW Load Voltage Comparison (p.u.)			
	Analog HW	PowerWorld	Difference
Real	0.645	0.629	0.016
Imaginary	0.165	0.157	0.008
Magnitude	0.666	0.648	0.018
Phase (degrees)	14.349	14.030	0.319

The emulation results are very close to the PowerWorld results. Component tolerances and OTA nonlinearities are introducing most of the error seen here. The results from two more cases with the same transmission line configuration are located in the appendix.

Taken as a whole the test results presented in this chapter verify the functionality and reconfigurability of the transmission line models presented in this thesis. All of the results, while they do contain errors, are relatively close to the expected power flow results. With further development the computational accuracy of these circuits could be improved to yield even better results.

7 CONCLUSIONS AND FUTURE WORK

7.1 CONCLUSIONS

This thesis provided an overview of static lumped parameter power transmission line modeling and applied these models to a previously proposed analog power flow technique. Essentially four different line models were outlined for DC emulation: lossless short line, lossy short line, medium line and long line models. In addition, OTA based reconfigurable analog hardware realizations for all four of these transmission line models were developed, presented and verified through testing.

Simulation and hardware results verified all of the analog designs, clearly defined linear operating ranges and examined the deficiencies of current off the shelf OTAs while pointing out methods of compensation. A power system network hardware prototype was constructed with off the shelf electronic components based on the proposed analog line models and the resultant power flow results compared favorably to those from commercially available software. Furthermore the OTA based circuits are fairly simple, contain basic components such as bipolar junction transistors and resistors, and are universally applicable to all the emulation line models. These properties are extremely advantageous for VLSI fabrication of a large scale power system emulator. Thousands of the OTA based building blocks for the analog transmission line models (variable positive and negative resistance circuits) can be fabricated onto a single chip and remotely configured to construct the desired transmission line model and set the associated line parameters. VLSI fabrication can also encompass distributed transmission line modeling for this application.

Historically lumped parameter modeling is used for its simplicity and accurate terminal behavior but no information on the system states is available along the transmission line. A distributed parameter transmission line models the voltage and current throughout the transmission line in finite intervals. From the analog models proposed in this thesis a distributed parameter line model is easily incorporated by connecting multiple segments in series to produce a model for a single transmission line. The terminals of each line segment are representative of the transmission line behavior at a finite interval along the line. This information can be extracted from the emulator through measurement and could lead to further, more refined, analysis of transmission line behavior in a large complex power system networks. Specifically in a VLSI implementation this is very feasible due to the number of line model segments that can be fabricated in a single chip.

7.2 SUMMARY OF RESEARCH CONTRIBUTIONS

The work presented in this thesis is a continuation of research in the field of analog computation for power systems. More specifically this work is an expansion on a previously proposed DC emulation technique for power flow computation. The following contributions to this research topic have been made:

- Development of a simple, low-cost, reconfigurable analog hardware representation of analog transmission line networks for DC emulation.
- Development of an analog transmission line model incorporating shunt elements and distributed parameters.

- Verification of the DC emulation power flow technique in fully reconfigurable analog hardware suitable for VLSI implementation.

7.3 FUTURE WORK

Logically the next step for this work would be a VLSI implementation of the transmission line models to construct a large power system network in analog hardware. This would require a custom VLSI design and fabrication of the chip. Furthermore control and parameter scaling schemes would need to be refined for larger scale networks. More research can also be conducted towards the modeling of other power system components. In this thesis the network model comprises transmission lines only. Switches, circuit breakers, transformers and other power system components can be modeled and included in this network. In fact, if the additional components are modeled as impedances the techniques utilized here for modeling the transmission line elements can be used for the other components. For example, a basic transformer model consists of series and shunt inductive and resistive elements. This could easily be implemented into the DC emulation network with the analog hardware presented in this thesis. In addition, the dynamics of the network could also be implemented in analog hardware.

In this thesis only the static behavior of the transmission lines were examined. The dynamics of the lines could also be incorporated, although for power flow applications the dynamics of the generators, and to a lesser extent, the loads are much more influential than those resulting from the transmission lines.

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APPENDIX A: EXAMPLES OF COMMERCIAL ANALOG COMPUTERS

This section provides some pictorial examples of analog computer systems which were once commercially available. All pictures obtained from the Analog Computer Museum and history center[32].

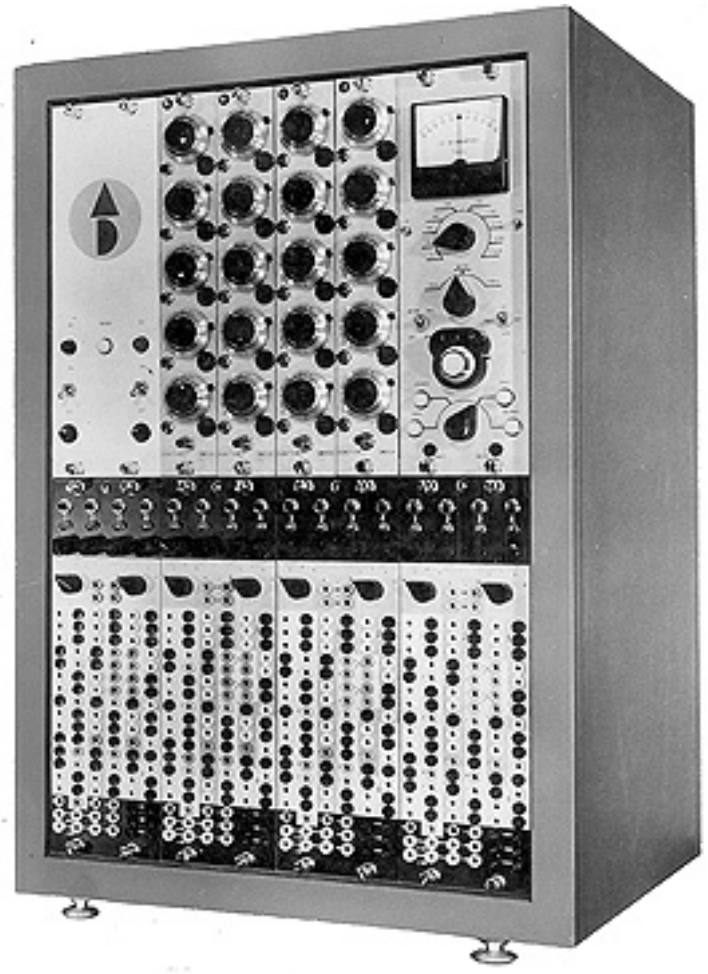

Figure 63: Applied Dynamics Model # AD-1-16

The computer in Figure 63 is a vacuum tube based analog computer built by Applied Dynamics and introduced commercially in 1960. It had an operating range of ± volts DC and consisted of 16 amplifiers.

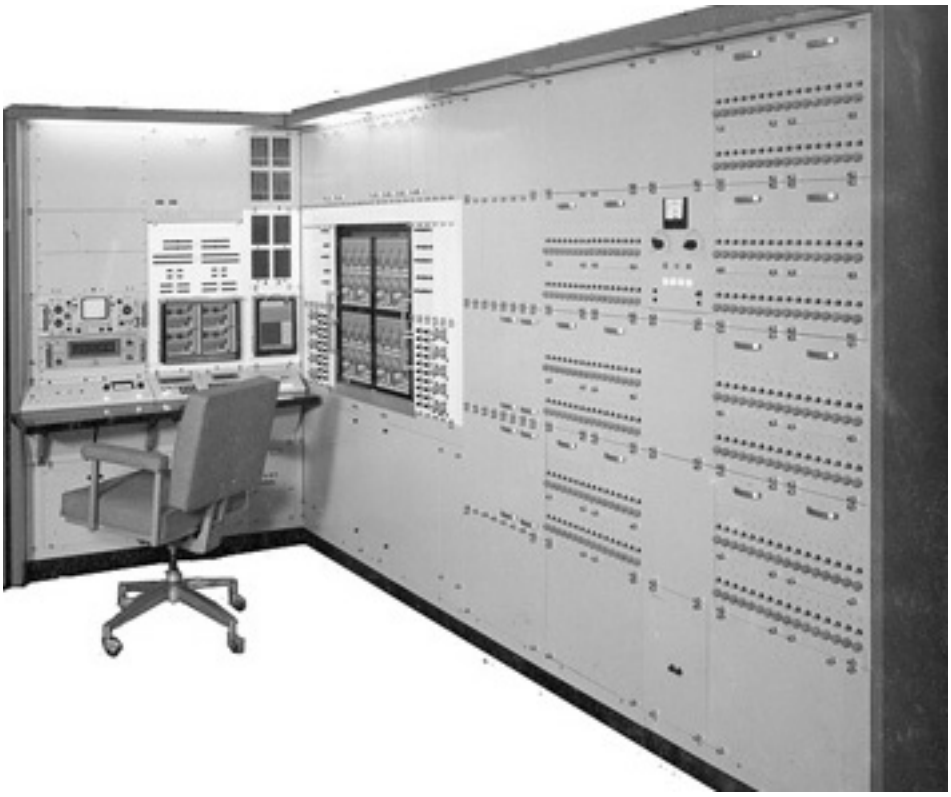

Figure 64: Applied Dynamics Model # AD-256

The computing system shown in Figure 64 was introduced in 1964 and was much larger and more advanced than their vacuum tube based models. Transistors were utilized instead of the larger more expensive tubes. The operational range was maintained at ±100 volts DC with 256 amplifiers. More specifically the unit consisted of 48 integrators, 80 summers, 128 inverters and 200 coefficient potentiometers.

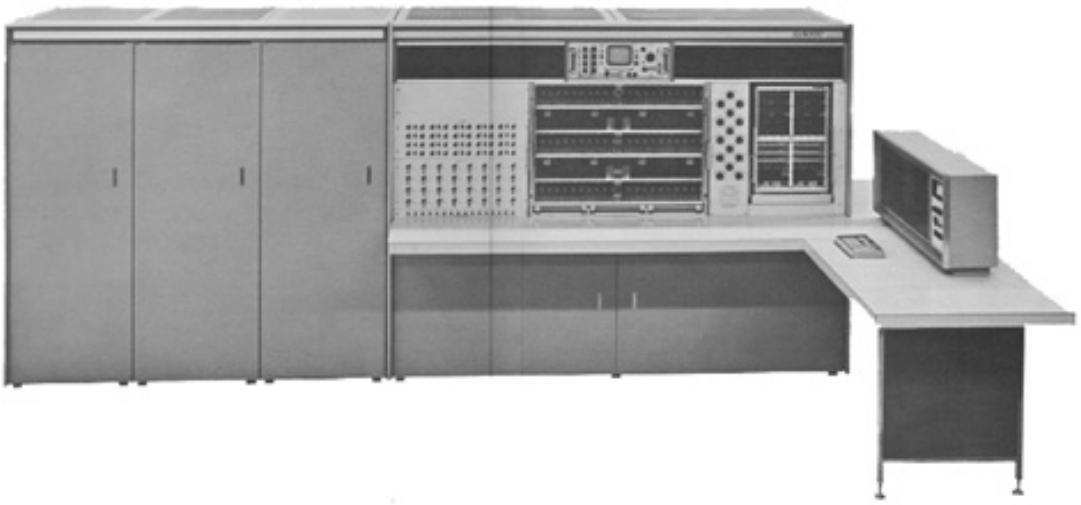

Figure 65: Comcor Incorporated Model # Ci 5000

Figure 65 is another transistor based analog computer introduced by Comcor Inc. This unit had 376 amplifiers and an operational range of ± 100 volts DC. This is an example of one of the more advanced commercial analog computers. Towards the late 1960's and 1970's the development of commercially available analog computers dropped off drastically in favor of digital micro-processor based computers.

APPENDIX B: EMULATION RESULTS FOR 3 BUS LOSSLESS TRANSMISSION LINE NETWORK

The network module was configured for a three bus lossless power system and tested. For the tests outlined in this section the effective resistance was set using bias resistors, R_{abc}, tied to the positive supply on the prototype board. Three tests were run and the results from these different power system operating points are presented here. The same scaling factors and transmission line configurations were used in all these cases.

Case 1:

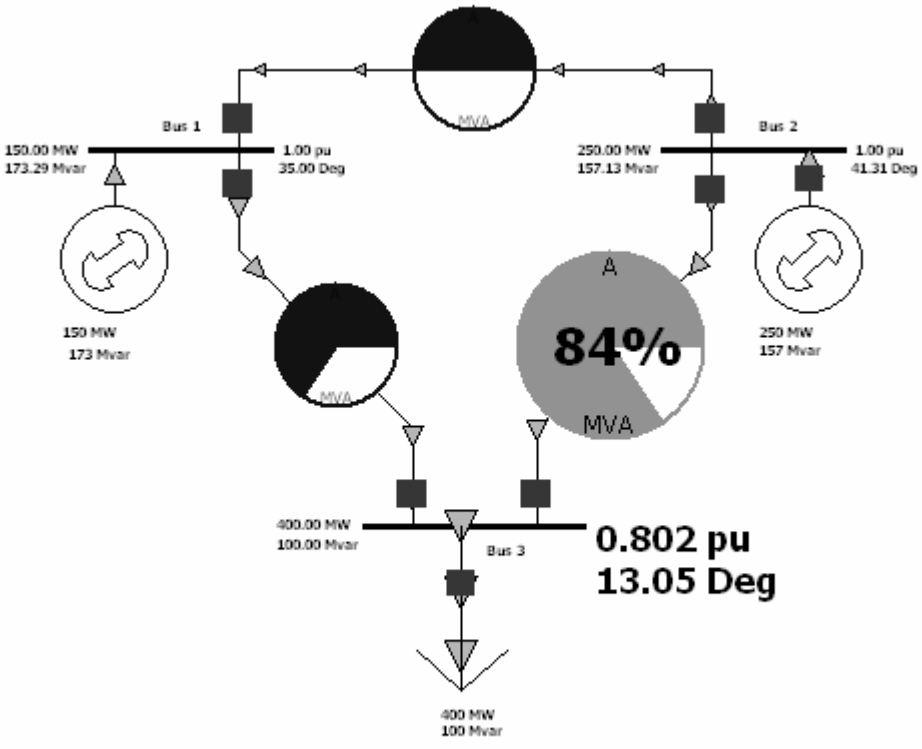

Figure 66: PowerWorld Simulation Results with Lossless Lines

Table 18: Simulation Results for Lossless Network

PowerWorld Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8192	0.5736	V p.u.
Bus 2 Voltage	0.7511	0.6601	V p.u.
Bus 3 Voltage	0.7813	0.1811	V p.u.
Generator 1	150	173.29	MW/MVAR
Generator 2	250	157.13	MW/MVAR
Load	400	100	MW/MVAR
Transmission Line A	0	0.22	ohms p.u.
Transmission Line B	0	0.15	ohms p.u.
Transmission Line C	0	0.19	ohms p.u.

The scaling factors for the analog emulation were chosen as follows:

Table 19: Scaling Factors for Lossless Network Testing

Scaling Factors	
Vk	2
Zk	100000
Ik	0.00002

Table 20: Emulation Parameters for Lossless Transmission Lines

Line	Reff	Iabc(uA)	Rabc at 15V (kohm)	Rabc in HW	R	Ra
A	22k	262	54.50	52.3k	81.5k	1k
B	15k	724	19.72	19.6k	71.5k	1k
C	19k	601	23.76	23.7k	81.5k	1k

Table 21: Emulation Bus Voltages for Lossless Transmission Line Test

Bus	Real	Imaginary
1	1.64	1.15
2	1.50	1.32
3	1.56	0.36

Table 22: Emulated Line Currents for Lossless 3 Bus Network

Hardware Results						
	Actual Line Current (uA)		Line Current Offset (uA)		Offset Corrected Line Current(uA)	
Line	Real	Imaginary	Real	Imaginary	Real	Imaginary
A	-6	4	2	-2	-8	6
B	57	2	5	-1	52	3
C	57	-6	5	-3	52	-3

Table 23: Emulated Current Injections for Lossless 3 Bus Network

Hardware Generator/Load Currents (uA)		
Device	Real	Imaginary
Gen 1	44	9
Gen 2	60	-9
Load	104	0

Table 24: Error Analysis on Emulation Results for 3 Bus Lossless Network

PowerWorld and Analog Emulation Comparison (A p.u.)						
	PowerWorld Current		Analog HW Current		Difference	
	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase
Line A	0.50	-38.15	0.50	-36.87	0.00	1.28
Line B	2.63	5.51	2.60	3.30	0.02	2.21
Line C	2.53	-3.60	2.60	-3.30	0.08	0.30
Generator 1	2.29	14.18	2.25	11.56	0.05	2.62
Generator 2	2.95	-9.12	3.03	-8.53	0.08	0.59
Load	5.14	1.05	5.20	0.00	0.06	1.05

Case 2:

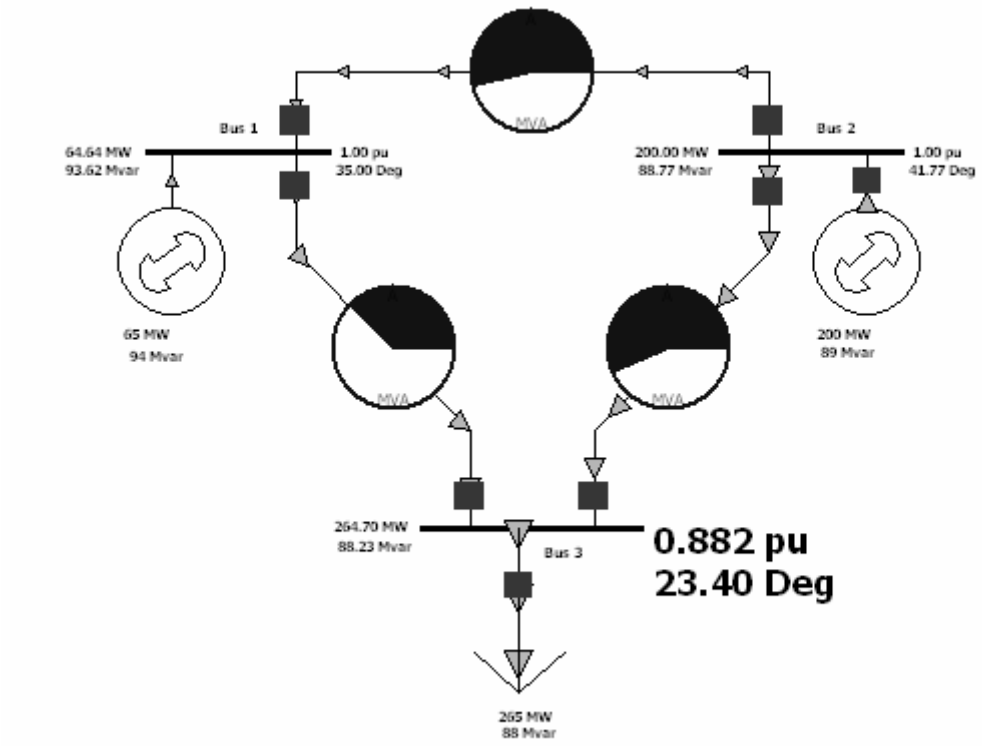

Figure 67: PowerWorld Simulation Results with Lossless Lines

Table 25: Simulation Results for Lossless Network

PowerWorld Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8192	0.5736	V p.u.
Bus 2 Voltage	0.7458	0.6661	V p.u.
Bus 3 Voltage	0.8095	0.3503	V p.u.
Generator 1	64.64	93.62	MW/MVAR
Generator 2	200	88.77	MW/MVAR
Load	265	88	MW/MVAR
T Line A	0	0.22	ohms p.u.
T Line B	0	0.15	ohms p.u.
T Line C	0	0.19	ohms p.u.

Table 26: Emulation Bus Voltages for Lossless Transmission Line Test

Bus	Real	Imaginary
1	1.64	1.15
2	1.49	1.33
3	1.62	0.70

Table 27: Emulated Line Currents for Lossless 3 Bus Network

Hardware Results						
	Actual Line Current (uA)		Line Current Offset (uA)		Offset Corrected Line Current(uA)	
Line	Real	Imaginary	Real	Imaginary	Real	Imaginary
A	-6	4	2	-2	-8	6
B	35	1	5	-1	30	2
C	38	-9	5	-3	33	-6

Table 28: Emulated Current Injections for Lossless 3 Bus Network

Hardware Generator/Load Currents (uA)		
Device	Real	Imaginary
Gen 1	22	8
Gen 2	38	-12
Load	63	-4

Table 29: Error Analysis on Emulation Results for 3 Bus Lossless Network

PowerWorld and Analog Emulation Comparison (A p.u.)						
	PowerWorld Current		Analog HW Current		Difference	
	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase
Line A	0.54	-38.38	0.50	-36.87	0.04	1.51
Line B	1.49	2.49	1.50	3.81	0.01	1.33
Line C	1.70	-11.39	1.68	-10.30	0.02	1.09
Generator 1	1.14	20.44	1.17	19.98	0.03	0.45
Generator 2	2.19	-17.78	1.99	-17.53	0.20	0.26
Load	3.16	-4.90	3.16	-3.63	0.01	1.27

Case 3:

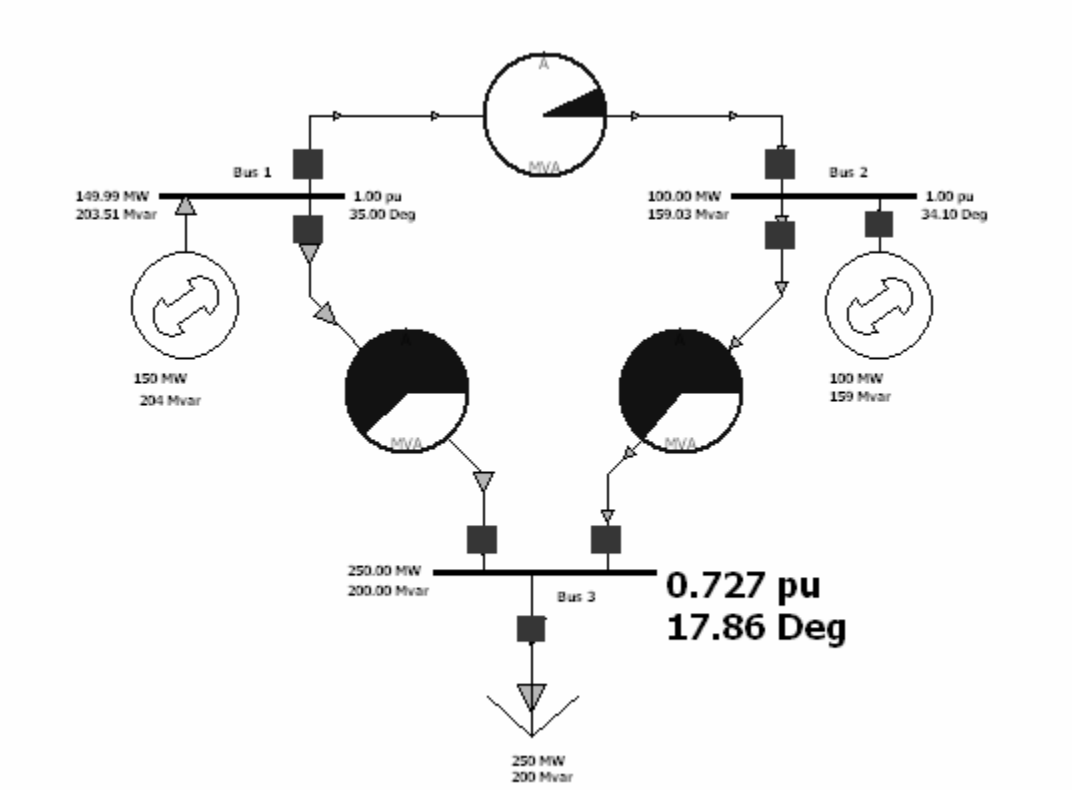

Figure 68: PowerWorld Simulation Results with Lossless Lines

Table 30: Simulation Results for Lossless Network

PowerWorld Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8192	0.5736	V p.u.
Bus 2 Voltage	0.8281	0.5606	V p.u.
Bus 3 Voltage	0.6920	0.2230	V p.u.
Generator 1	149.99	203.51	MW/MVAR
Generator 2	100	159.03	MW/MVAR
Load	250	200	MW/MVAR
Transmission Line A	0	0.22	ohms p.u.
Transmission Line B	0	0.15	ohms p.u.
Transmission Line C	0	0.19	ohms p.u.

Table 31: Emulation Bus Voltages for Lossless Transmission Line Test

Bus	Real	Imaginary
1	1.64	1.15
2	1.66	1.12
3	1.38	0.45

Table 32: Emulated Line Currents for Lossless 3 Bus Network

Hardware Results						
	Actual Line Current (uA)		Line Current Offset (uA)		Offset Corrected Line Current(uA)	
Line	Real	Imaginary	Real	Imaginary	Real	Imaginary
A	3	-4	2	-2	1	-2
B	52	16	5	-1	47	17
C	40	12	5	-3	35	15

Table 33: Emulated Current Injections for Lossless 3 Bus Network

Hardware Generator/Load Currents		
Device	Real	Imaginary
Gen 1	48	15
Gen 2	34	17
Load	82	32

Table 34: Error Analysis on Emulation Results for 3 Bus Lossless Network

PowerWorld and Analog Emulation Comparison (A p.u.)						
	PowerWorld Current		Analog HW Current		Difference	
	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase
Line A	0.07	-34.55	0.11	-63.43	0.04	28.88
Line B	2.49	19.94	2.50	19.89	0.01	0.05
Line C	1.92	21.95	1.90	23.20	0.01	1.25
Generator 1	2.53	18.62	2.51	17.35	0.01	1.27
Generator 2	1.88	23.77	1.90	26.57	0.02	2.80
Load	4.40	20.81	4.40	21.32	0.00	0.50

APPENDIX C: EMULATION RESULTS FOR 3 BUS LOSSY TRANSMISSION LINE NETWORK

Emulation results for an additional case with the lossy transmission line network are presented here. The same scaling factors and transmission line configuration used in chapter 6 for the lossy network were used in this case.

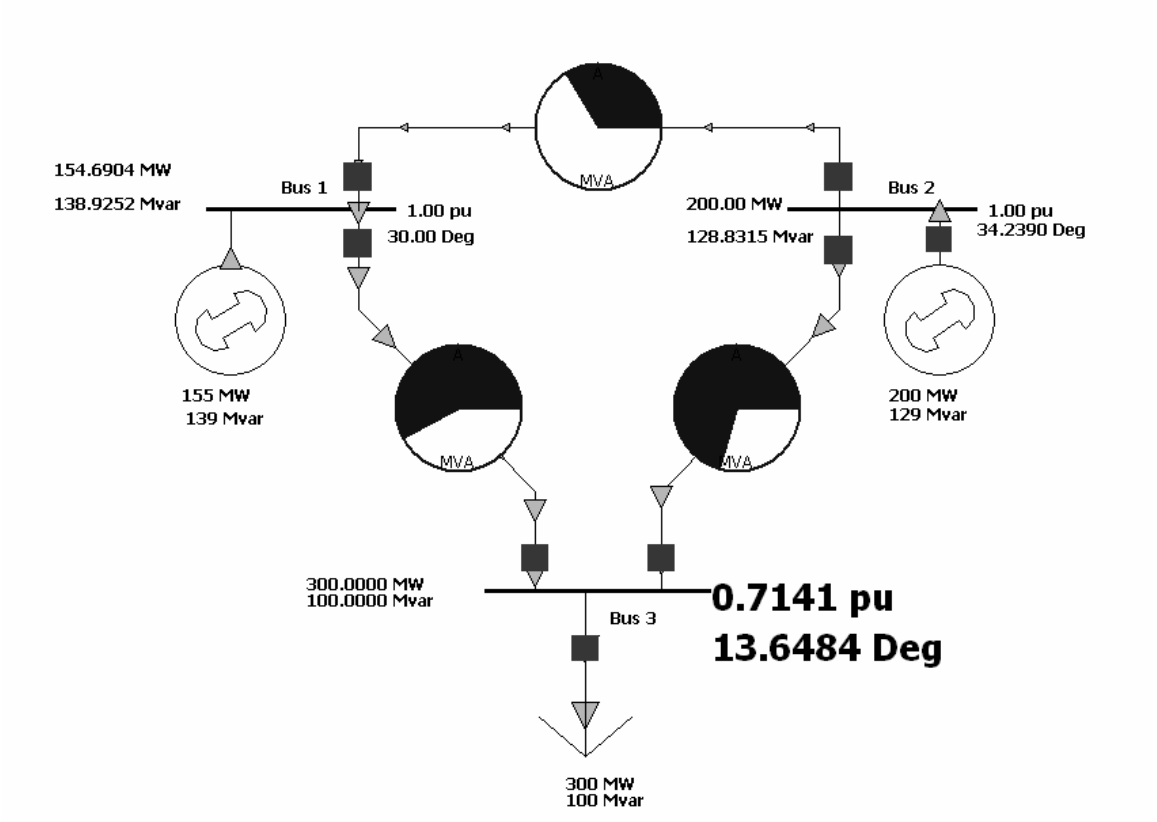

Figure 69: PowerWorld Simulation Results with Lossy Lines

Table 35: Simulation Results for Lossy Network

PowerWorld Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8660	0.5000	V p.u.
Bus 2 Voltage	0.8267	0.5626	V p.u.
Bus 3 Voltage	0.6939	0.1685	V p.u.
Generator 1	154.69	138.93	MW/MVAR
Generator 2	200.00	128.83	MW/MVAR
Load	300	100	MW/MVAR
T Line A	0.02	0.22	ohms p.u.
T Line B	0.06	0.15	ohms p.u.
T Line C	0.05	0.19	ohms p.u.

Table 36: Emulated Line Currents for Lossy 3 Bus Network

Hardware Results								
	Actual Line Current (uA)				Line Current Offset (uA)			
Line	Network 1	Network 2	Network 3	Network 4	Network 1	Network 2	Network 3	Network 4
A	1	-39	20	-4	-1	-3	-3	-1
B	55	239	127	102	5	5	5	5
C	28	244	87	70	6	6	6	6

Table 37: Offset Corrected Emulation Results for Lossy 3 Bus Network

Emulation Results (offset corrected in uA)					
Line	I Real	I Imaginary	Device	I Real	I Imaginary
A	-34	-26	Gen 1	250	-51
B	284	-25	Gen 2	294	9
C	260	-17	Load	544	-42

Table 38: Error Analysis on Emulation Results for 3 Bus Lossy Network

PowerWorld and Analog Emulation Comparison (A p.u.)						
	PowerWorld Current		Analog HW Current		Difference	
	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase
Line A	0.33	37.31	0.34	37.41	0.01	0.09
Line B	2.31	-5.63	2.28	-5.03	0.03	0.60
Line C	2.12	-3.87	2.08	-3.74	0.03	0.13
Generator 1	2.08	-11.93	2.04	-11.53	0.04	0.40
Generator 2	2.38	1.45	2.35	1.75	0.03	0.31
Load	4.43	-4.79	4.36	-4.41	0.06	0.38

APPENDIX D: PSPICE SIMULATION OF THREE BUS POWER SYSTEM EMULATION WITH PI LINE MODELS

The emulator configuration and results for a PSpice simulation of power flow emulation for a three bus power system utilizing the full pi analog transmission line model is presented here. Error analysis was conducted on the emulation results with respect to PowerWorld results.

Table 39: Power World Simulation Results for Three Bus System with Pi Lines

PowerWorld Results				
		Real	Imag	
Gen1 V		1	0	V p.u.
Gen2 V		0.997	0.075	V p.u.
Load V		0.708	-0.199	V p.u.
Line A	series	0.02	0.22	ohms p.u.
	shunt	100	10	ohms p.u.
Line B	series	0.06	0.15	ohms p.u.
	shunt	50	5	ohms p.u.
Line C	series	0.05	0.19	ohms p.u.
	shunt	66.67	6.67	ohms p.u.

Table 40: Emulation Scaling Factors

Scaling Factors	
Vk	2
Ik	0.000143
Zk	14000

Table 41: DC Emulation Network Parameters

DC Emulation				
DC Emulation Network Parameters				
		Real	Imag	
Line A	series	17080	1552.727	ohms
	shunt	700000	-70000	
Line B	series	3045	1218	
	shunt	350000	-35000	
Line C	series	5404	1422.105	
	shunt	466666.2	-46666.2	

Table 42: Emulation Line Configuration for Pi Transmission Lines

Emulation HW Configuration					
			R	Ra	Ibias(uA)
LineA	series	real	4.6k	500	63.2125
		imag	4.6k	500	745.6
	shunt	real	200k	500	49.4697
		imag	100k	1k	155.851
Line B	series	real	4.6k	500	366.35
		imag	4.6k	500	971.8
	shunt	real	200k	500	107.981
		imag	100k	1k	319.899
Line C	series	real	4.6k	500	203.05
		imag	4.6k	500	820.117
	shunt	real	200k	500	78.6062
		imag	100k	1k	236.556

Table 43: Error Analysis on Emulation Results for 3 Bus Pi Line Network

	Scaled OTA Network (A p.u.)		PowerWorld (A p.u.)		Difference	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
Load Current	4.35	-35.81	4.27	-36.28	0.08	0.46
Gen 1 Current	1.84	-33.04	1.79	-32.47	0.05	0.57
Gen 2 Current	2.26	-20.45	2.20	-20.55	0.06	0.10

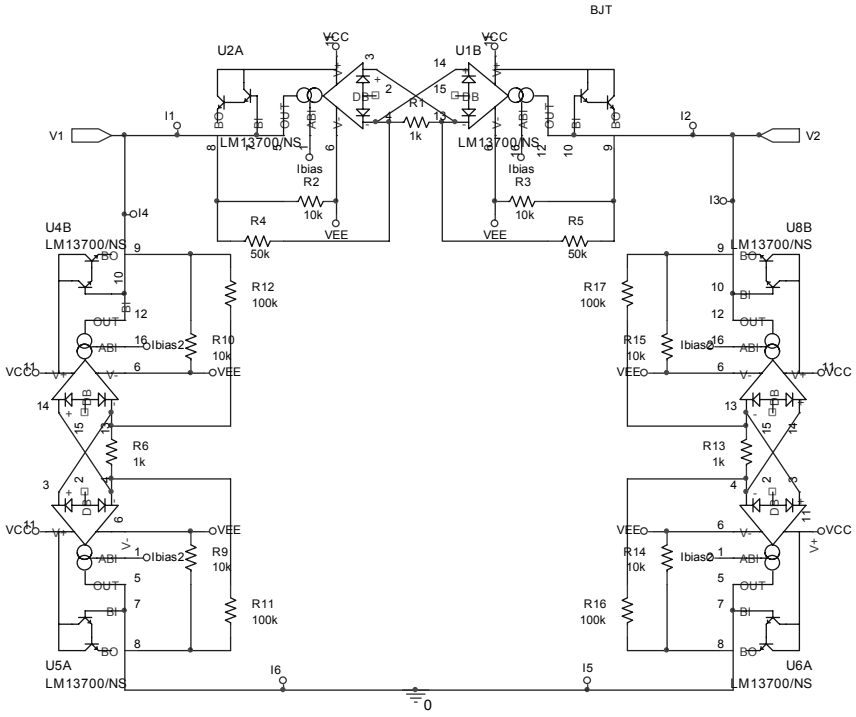

Figure 70: PSpice Schematic for a Single Pi Line DC Emulation Network

For the simulation a single pi line segment shown in Figure 70 was condensed into a hierarchal block. This block essentially compresses the circuit into a box with input and output terminals and makes it simpler to construct complex circuits for simulation through the graphical user interface in OrCad. The next figure shows the full three bus system emulator built from these hierarchal blocks.

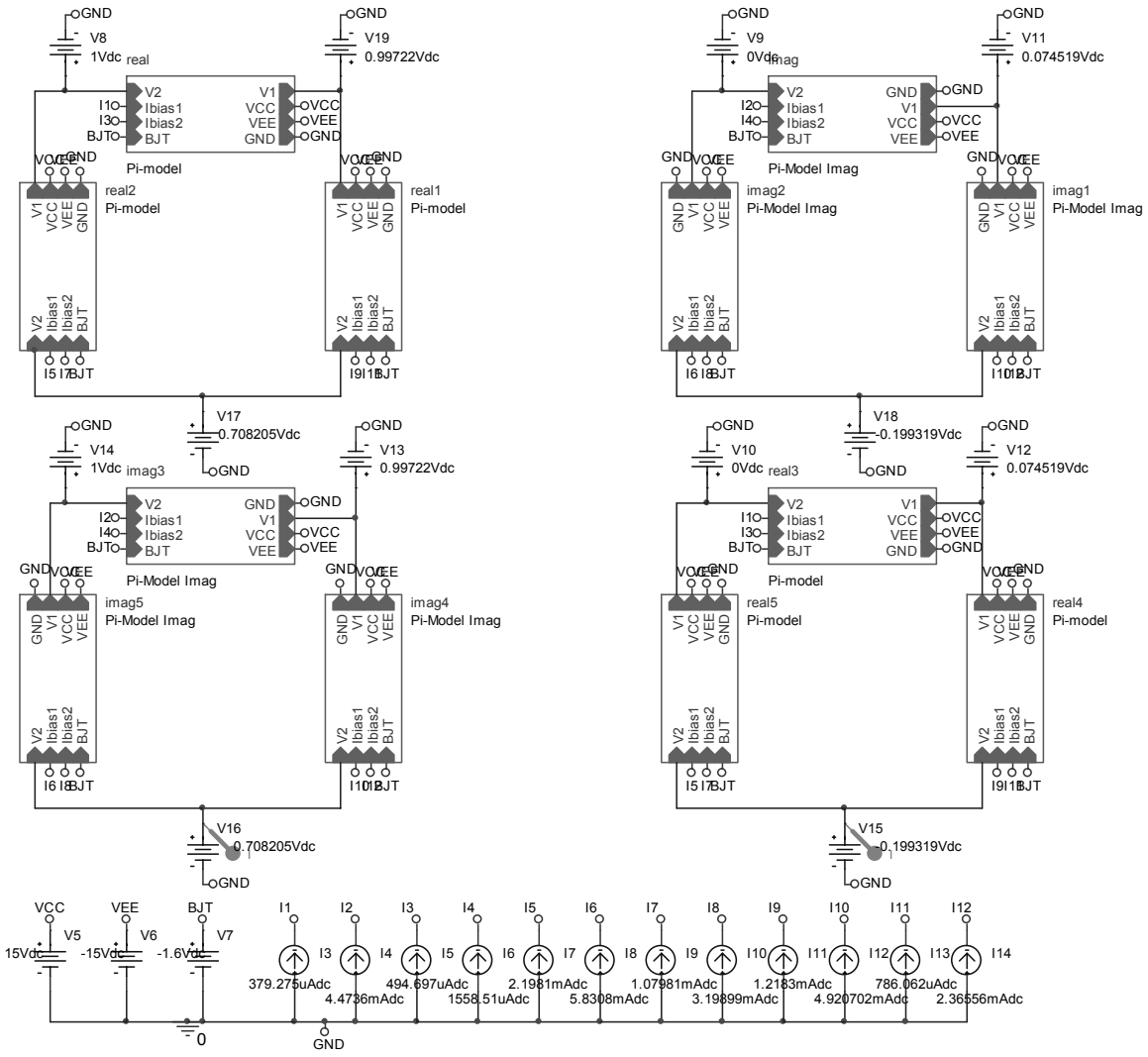

Figure 71: PSpice Schematic for Three Bus Simulation with Hierarchal Blocks

The following plots are taken from measurements in the PSpice simulations. They are measurements of the generator and load currents in the emulation.

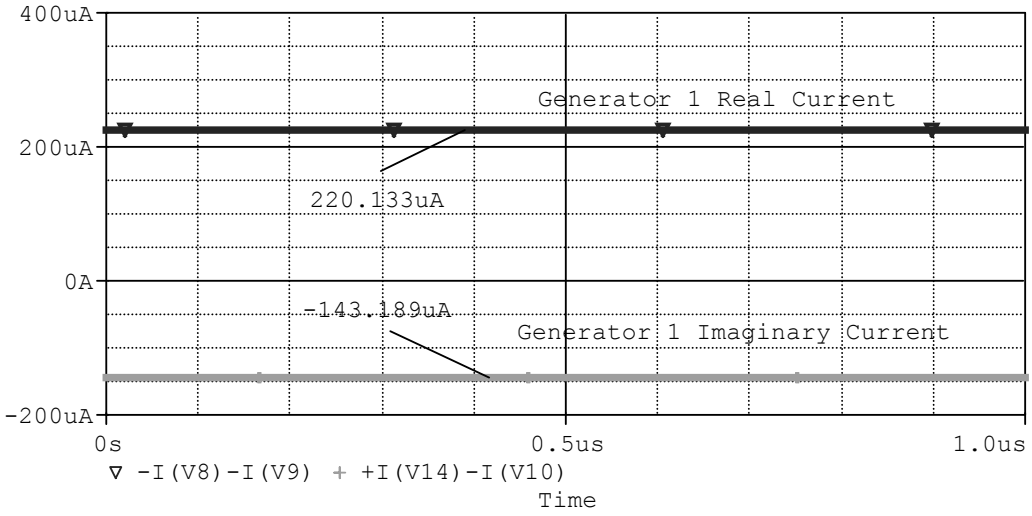

Figure 72: Simulation Results for Generator 1 Current for 3 Bus Pi Line Network

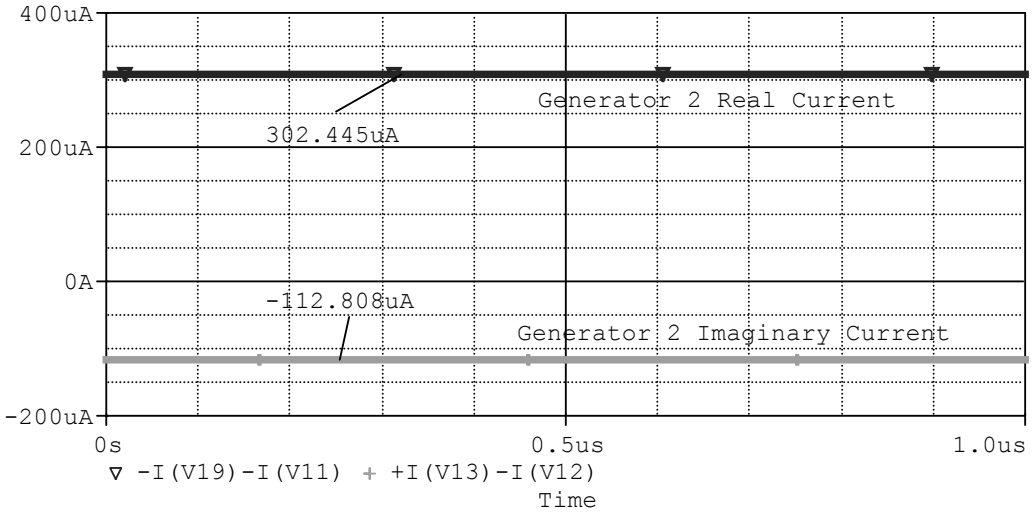

Figure 73: Simulation Results for Generator 2 Current for 3 Bus Pi Line Network

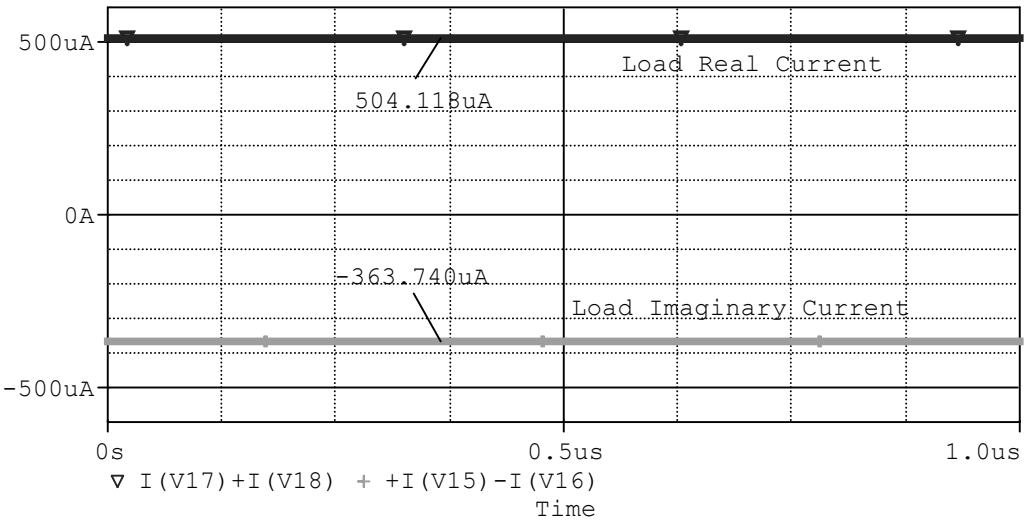

Figure 74: Simulation Results for Load Current for 3 Bus Pi Line Network

APPENDIX E: EMULATION RESULTS FOR NETWORK AND LOAD MODULE

Tabulated here are the PowerWorld simulation results and the analog emulation results for a three bus emulation system. The load and transmission lines are OTA based emulation circuits and the generators are voltage sources. Results from two cases are presented. The same scaling factors and transmission line configurations in chapter 6 for the network and load module testing were used in these cases

Case 1:

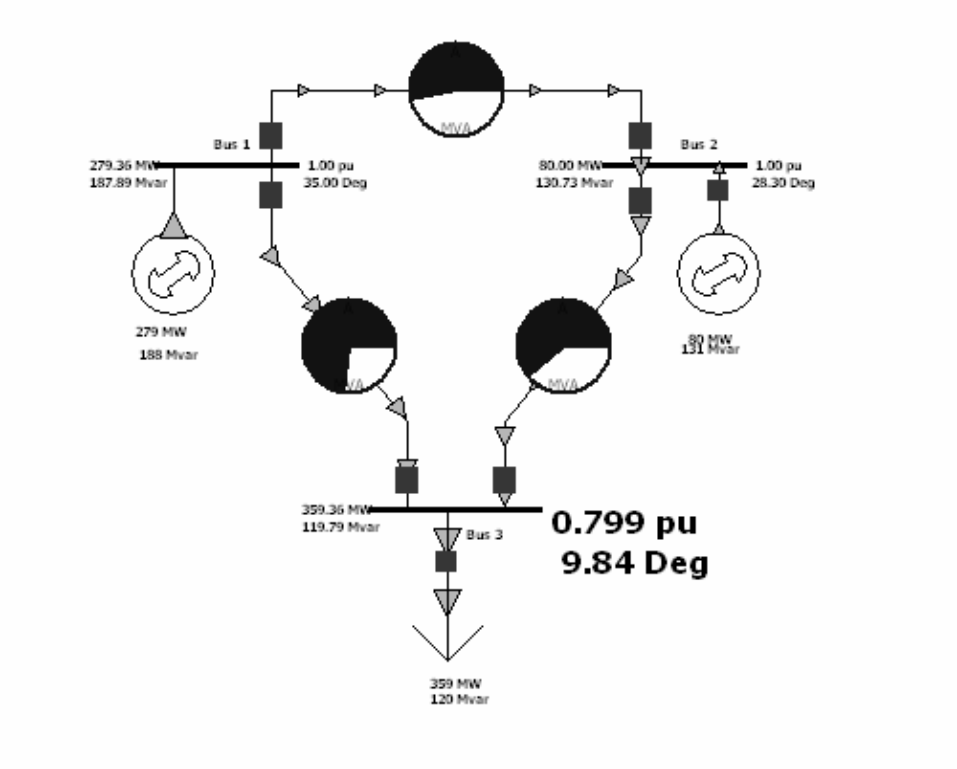

Figure 75: PowerWorld Results for Network and Load Module Emulation

Table 44: PowerWorld Parameters and Results

PowerWorld Paramters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8192	0.5736	V p.u.
Bus 2 Voltage	0.8805	0.4741	V p.u.
Bus 3 Voltage	0.7872	0.1365	V p.u.
Generator 1	279.36	187.89	MW/MVAR
Generator 2	80.00	130.73	MW/MVAR
Load	450	150	MW/MVAR
T Line A	0	0.22	ohms p.u.
T Line B	0	0.15	ohms p.u.
T Line C	0	0.19	ohms p.u.

Table 45: Emulation Parameters and Results

Emulation Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	1.6383	1.1472	V
Bus 2 Voltage	1.7610	0.9482	V
Bus 3 Voltage	1.5745	0.2731	V
T Line A	0	22	kohms
T Line B	0	15	kohms
T Line C	0	19	kohms
I load	93	14	uA
Vload (measured)	1.599	0.340	V

Table 46: Error Analysis on Emulation with Network and Load Modules

PowerWorld and Analog HW Load Voltage Comparison (p.u.)			
	Analog HW	PowerWorld	Difference
Real	0.800	0.787	0.012
Imaginary	0.170	0.137	0.033
Magnitude	0.817	0.799	0.018
Phase (degrees)	12.004	9.840	2.164

Case 2:

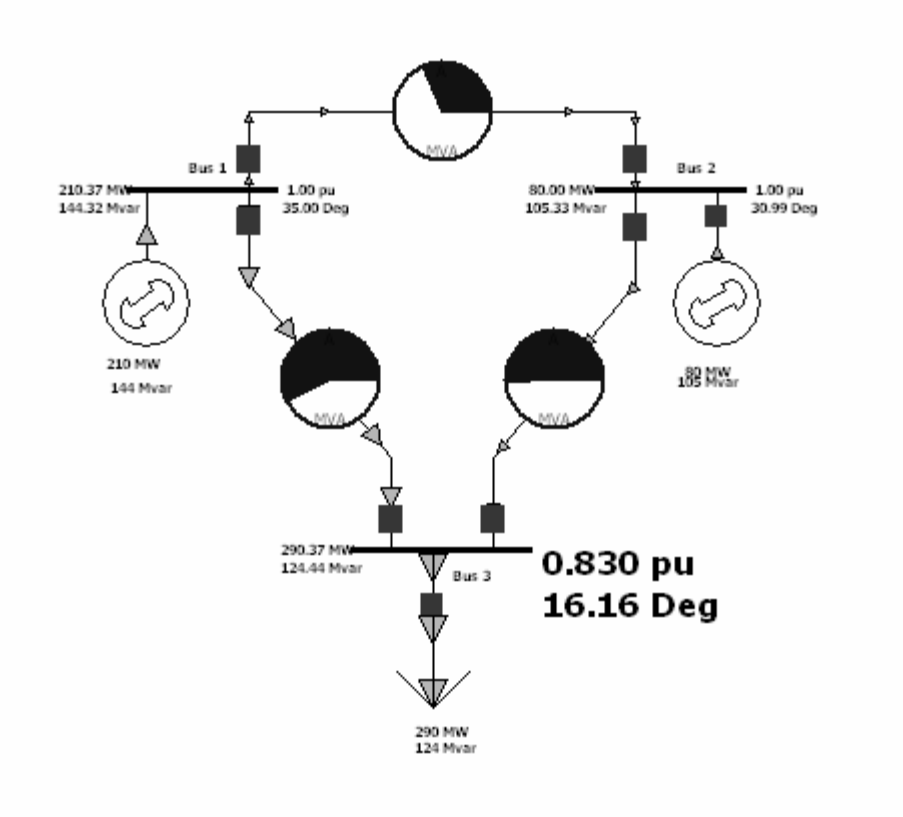

Figure 76: PowerWorld Results for Network and Load Module Emulation

Table 47: PowerWorld Parameters and Results

PowerWorld Paramters and Results			
	Real	Imaginary	
Bus 1 Voltage	0.8192	0.5736	V p.u.
Bus 2 Voltage	0.8573	0.5149	V p.u.
Bus 3 Voltage	0.7972	0.2310	V p.u.
Generator 1	210.37	144.32	MW/MVAR
Generator 2	80.00	105.33	MW/MVAR
Load	350	150	MW/MVAR
T Line A	0	0.22	ohms p.u.
T Line B	0	0.15	ohms p.u.
T Line C	0	0.19	ohms p.u.

Table 48: Emulation Parameters and Results

Emulation Parameters and Results			
	Real	Imaginary	
Bus 1 Voltage	1.6383	1.1472	V
Bus 2 Voltage	1.7145	1.0298	V
Bus 3 Voltage	1.5944	0.4620	V
T Line A	0	22	kohms
T Line B	0	15	kohms
T Line C	0	19	kohms
I load	75.5	9	uA
Vload (measured)	1.612	0.520	V

Table 49: Error Analysis on Emulation with Network and Load Modules

PowerWorld and Analog HW Load Voltage Comparison (p.u.)			
	Analog HW	PowerWorld	Difference
Real	0.806	0.797	0.009
Imaginary	0.260	0.231	0.029
Magnitude	0.847	0.830	0.017
Phase (degrees)	17.879	16.160	1.719