Efficient Acoustic Feature Computation Using FPGAs

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Abstract

Many recent advances in music information retrieval (MIR) have been data-driven. Widespread performance evaluations on common data sets, like the annual MIREX events, have been instrumental in advancing the field. Such endeavors incur large computational costs and could potentially benefit from faster calculation of acoustic features. Traditional cluster-based solutions are expensive and space- and power-inefficient. The massively parallel architecture of the field programmable gate array (FPGA) makes it possible to design lower-cost, application-specific chips rivaling cluster speed for large-scale acoustic feature computation. Such devices also show potential for implementations of MIR systems on embedded devices where hardware acceleration is a necessity. We present a prototype Xilinx System Generator (XSG) library for acoustic feature calculation. We use a genre classification task to compare the performance of simulated hardware features to those computed using standard methods. Finally, we discuss ongoing efforts toward a working hardware design.

Acoustic Feature Specification

Features computed included mel-frequency cepstral coefficients (MFCCs) and spectral shape features (centroid, flux, rolloff).

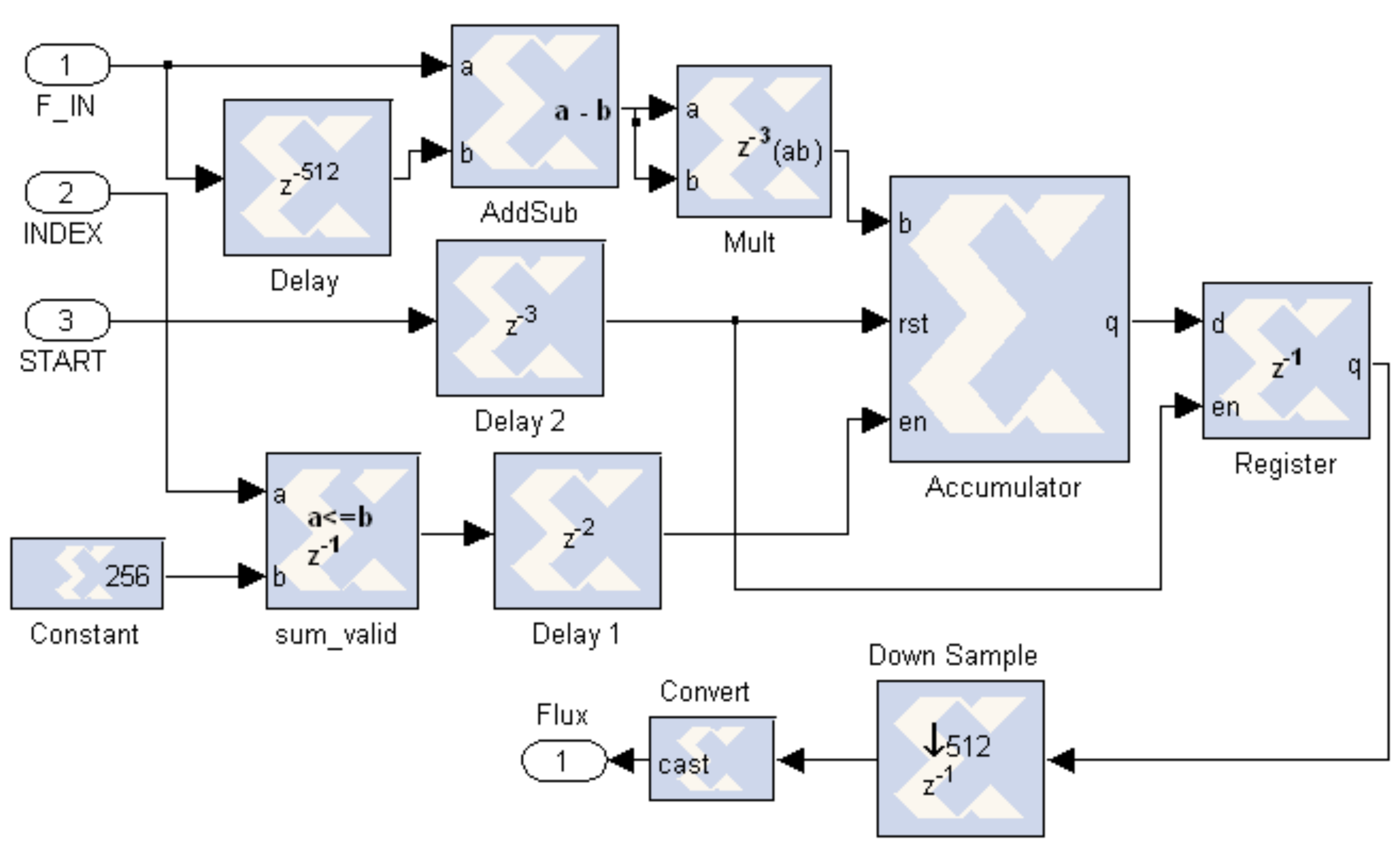

Figure 1 - Example Xilinx System Generator implementation of spectral flux in Simulink

Speed Experiments

- Single FFT performance on 30 sec clips, ~23ms frames (1292 total).
- Feature performance using 6 parallel computation engines, ~23 ms frames.

Toolkit	Computation Time
M2K	0.483
MATLAB	0.364
FPGA	0.033

Table 1 - Comparison of feature computation times for 30 second clips between hardware and software.

Feature	First frame (μs)	Three secs (ms)	Thirty secs (ms)
S. Shape	25.6	0.576	5.536
MFCC	32	0.582	5.542

Table 2 - Performance of feature extraction on simulated hardware.

Classification Experiment

To verify the classification accuracy of the resulting fixed-point features in MIR, we calculate mel-frequency cepstral coefficients (MFCCs) and spectral shape features (centroid, flux, and rolloff) using XSG bit-accurate simulation. Features are verified through a six-class genre classification task: 100 examples per class, split 80:20 (training:testing).

Classifier Feature Set	CART	J48	LDA	Linear SMO
M2K	**36.43%**	**36.79%**	35.7%	45.36%
MATLAB	34.24%	35.15%	37.16%	46.63%
FPGA	34.24%	34.97%	**37.89%**	**49%**

Table 3 - Artist-filtered classification results.

Work in Progress

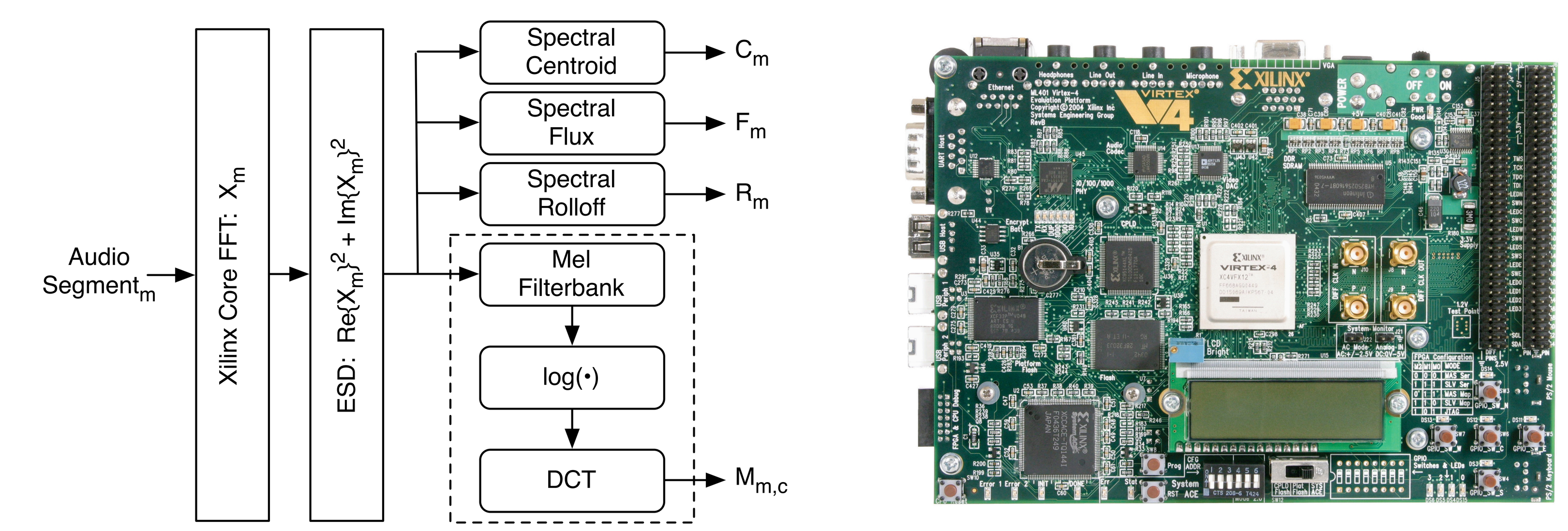

Figure 2 - Block diagram of hardware implementation of audio feature computation (left), image of FPGA board (right).

- A working hardware prototype is in development. XSG designs, built graphically in Simulink, are exported as HDL to the Xilinx Embedded Development Kit (EDK).
- An on-board PowerPC (PPC-405) processor handles PC-to-board TCP/IP communication over ethernet, allowing the FPGA to access data through shared memory registers.
- Ongoing issues include:
  - Reconciling the speeds of shared memory read/write operations, FPGA computations, and TCP/IP communication with the host PC.
  - TCP/IP communication introduces "spikes" in the data upon return to the host PC. The source of the spikes is under investigation. Some potential causes include indexing discrepancies between MATLAB scripts running on the host PC and C programs running on the PPC-405.

References

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[2] J.S. Downie. The music information retrieval evaluation exchange (2005–2007): A window into music information retrieval research. *Acoustical Science and Technology,* 29(4):247–255, 2008.

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