Power System Security Assessment through Analog Computation

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ABSTRACT

Power System Security Assessment through Analog Computation
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This dissertation proposes a methodology for power system security assessment through analog computation. By exploiting the strengths of analog computation a more robust security assessment can be performed as compared to traditional methods. Security assessment is currently performed by power system operators utilizing digital computers and determines the power system structure, states and level of security based on telemetered data and knowledge of the system. Ideally this process would occur in real time but due to the limitations of digital computers and telemetry systems the security assessment is currently conducted at periodic intervals of ten to fifteen minutes. This process requires a tremendous amount of computation for large systems. In order to provide updated assessment at such time intervals, not even in real time, numerous assumptions and simplifications of the power system models and analyses are required to simplify and speed up the digital computations. Due to its inherent speed and computational efficiency analog computation is proving to be a viable alternative.

Analog computation by definition is continuous in time and embodies an entirely different paradigm to computing as compared to discrete time methods. Security assessment for digital computers consists of topology estimations, state estimation and contingency analysis. The theory and practical approaches to these tasks through digital, discrete time, computational methods are fairly mature at this point in time but do not translate directly to analog computation. A robust analog computation engine along with corresponding computational theory is required in order to make use of analog methods for power system security assessment. This dissertation provides the relevant theory, hardware realization and application of an analog computer for power system security assessment.

1 INTRODUCTION

1.1 OVERVIEW

Analog computation of power systems is a continuing field of research. Among the advantages analog computation possesses over traditional digital methods are physically realizable solutions and much faster and more efficient computation. In prior research, simulation time for a two machine system were typically 10^4 times shorter than the real time phenomena [1]. In order to consummate this analog method as a viable tool in power system analysis accurate models of power system components and pertinent analog computational theory are requisite. This dissertation explores analog computational theory and the development of an analog computer for the purpose of power system security assessment. The focus here is on power system security assessment. However, the analog computer presented here is capable of conducting other power system analyses. It could be generalized as a solver of ordinary differential equations (ODEs). This introductory chapter covers background information on power system security assessment, the problem statement, analog/digital computation methods in power systems, and their associated strengths and weaknesses. Motivation for this research is also addressed.

1.2 BACKGROUND

Ideally the power system will always be operated in a safe and secure manner while providing electrical power to meet the current demand. In practice this is not possible, but generally speaking the system can be operated in a reasonably secure manner. In a paper detailing an adaptive control system [2], T. E. DyLiacco developed a methodology to define the power system operating state and appropriate control actions based on the determined state. DyLiacco defined three states: preventive, emergency and restorative. Control objectives were defined based on which state the system is in.

"In the preventive state, the generation-transmission system is being operated so that the demands of all customers are satisfied at standard frequency and at desired operating voltages" [2]. The term preventive was used to indicate that the system should be controlled in a defensive manner to prepare for and contend with disturbances from the current state such that the system maintains normal operation. The emergency operating state is defined when an overload is occurring, frequency is deviating unacceptably from nominal, or the voltage profile is beyond tolerable specifications. The desired control action is to mitigate the detected problem in the system while maintaining the maximum, ideally all, of the system load. "The restorative operating state is that condition when service to some customer loads has been lost" [2]. The control action at this point is to restore power supply to all customers and restore the system to the preventive state. An operating state strategy is depicted visually in Figure 1 [2]. The arrows designate transitions from one state to another. Solid arrows are indicative of desired control actions while dashed arrows show unintentional state transitions.

It is desirable to keep the system in preventive state at all times. If unexpected outages or failures of the equipment occur then the system could transition to emergency or restorative state. At this point control actions will be taken to move the system to a more desirable operating state. In general, the main objective is to serve as much load as possible. With this in mind, in some circumstances it may be desirable to take the system to emergency state while still maintaining all system load, or to the restorative state in a controlled manner to minimize the loss of load (e.g. load shedding). Determining the state of the system and appropriate control action can be accomplished through observation and detailed analysis of the system. A more generalized term encompassing this analysis and control determination is power system security.

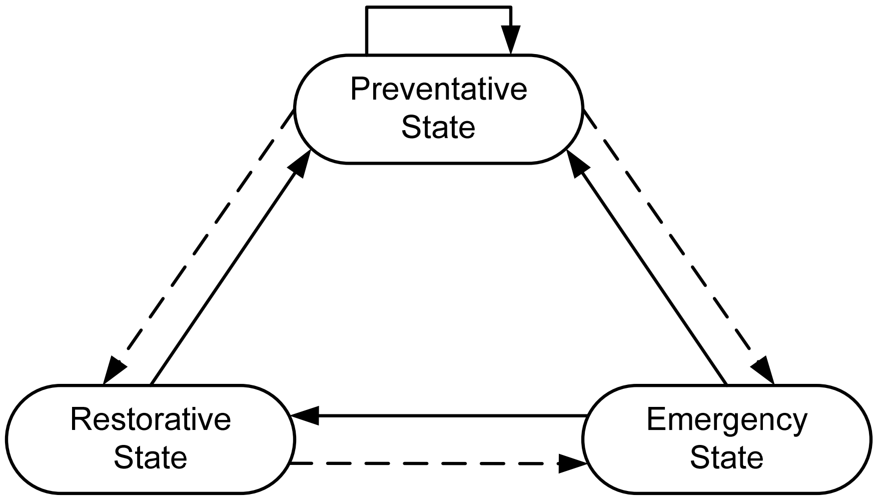


Figure 1: Operating State Strategy

A.J. Wood and B.F. Wollenberg define power system security by three main points [3]:

1. System Monitoring
2. Contingency Analysis
3. Security Constrained Optimal Power Flow (SCOPF)

System monitoring consists of acquiring real time measurements and data from the system along with analysis of this data. Data such as bus voltages, transmission line currents and power flows, circuit breaker status, transformer tap settings and load and generation levels are measured. Typical analyses of this data consist of topology estimation, state estimation and system limitation checks.

Contingency analysis is a process in which the effect of a component failure in the system is analyzed. For example, to investigate the effects of a transmission line loss a simulation is run on the system at its current state without the transmission line. Analysis of the resulting simulation provides insight to the system response to such a line loss. This is typically conducted for numerous failures to identify dangerous scenarios which would result in system limit violations or blackouts. This analysis helps determine which state the power system would move to in the event of a component failure or multiple failures. SCOPF is a tool that attempts to keep the system operating in the preventative state.

A security constrained optimal power flow is a process which incorporates contingency analysis, optimal power flow and economic dispatch. The end result, or goal, of SCOPF is to specify how the system should be operated in the most economical manner (minimizing cost) while not violating any constraints during contingencies. In other words, allow the system to remain in the preventive state in the event of contingencies. Power system security assessment as presented in this dissertation is defined as a subset of power system security. More specifically, it consists of system monitoring and contingency analysis.

Presently security assessment of the power system is conducted via digital computers. Digital computers are also utilized for most other power system analyses that require computation. This was not always the case. Historically, analog computation was prevalent in power systems as well as other fields. Before the advent of low cost and highly programmable digital computers almost all computationally intense problems were performed in analog form. The following sections provide an overview of analog and digital computation in power systems as well as a comparison between the two methods.

1.2.1 COMPARISON OF ANALOG AND DIGITAL COMPUTATION

Currently digital computers, mainly due to the low cost and ease of use, dominate computation. Although through advancements in circuit technology analog computers are gaining attention once again. The main reason for this is that in certain applications analog computation is desirable due to inherent strengths in the methodology. The main difference between analog and digital computation is that analog computation is continuous in time while digital computation is discretized. Due to the discrete nature and architecture of digital computers they rely on a clock, with a finite rate, and memory whose quantity and bandwidth are also finite. In direct comparison an analog computer, or machine, inherently has memory embedded in the system where required. This results in no corresponding memory bandwidth limitation. In addition, the continuous nature is equivalent to an infinite clock rate. Further analysis has been conducted regarding the relative strengths and weaknesses of both approaches to computation. These are listed in Table 1.

Table 1: Strengths and Weaknesses of Analog and Digital Computation

	Digital Computation	Analog Computation
Strengths	Highly programmable	Computation can be performed faster or slower than real time
	Low cost	Computation time independent of system size and model complexity
	Ease of use	High Efficiency
	Precise solutions	Numerically stable
	Robust computation theory already exists	Extremely proficient at computing non-linear systems
Weaknesses	Computation time dependant on system size/number of variables	Calibration required
	Discretization of models required	Historically not easily programmable
	Simplification of models required to speed up computation	Measurement is required to obtain solutions
	Numerical instability and convergence problems	Expensive and typically not easy to use
	Slow computation of non-linear systems	Very little existing computational theory

A stark contrast between digital and analog computation methods can be seen from Table 1. Digital methods are very sophisticated, and the technology mature. Due to these factors the technology exhibits low cost, high programmability and easy operation. In addition, they are very precise in contrast to analog methods. The digital methods run into problems specifically with large non-linear systems. These systems require time intensive iterative computation methods such as Newton-Raphson or Gauss-Seidel. Inherently many of these methods also result in numerical instability. In these instances no solution can be obtained. In addition, the discretization and simplification of the models can lead to, albeit precise, inaccurate results. With current state of the art technology the analysis of large scale non-linear systems with these digital methods is not feasible. In contrast analog methods can overcome some of these deficiencies.

Analog methods inherently exhibit true parallel computation resulting in computation time independent of system size and model complexity. Non-linear models are easily implemented and computed without numerical stability issues. The presence of any instability in analog computation is inherently instability of the system being studied. Theoretically utilizing analog, a vastly complex non-linear system of an arbitrary size can be computed in real-time, or even faster than real-time. However, certain weaknesses of analog computation have prevented such an implementation in the past. Analog components require constant calibration and historically programming was very time consuming and required manual intervention (e.g. manual adjustment of jumper and potentiometer settings). This has hindered online applications of analog computers. Most realizations have been limited to offline studies. In addition, analog computers are traditionally expensive to implement and a measurement system is also required to extract solutions. Due to these limitations digital computers have been chosen widely in favor of analog counterparts. However, there has consistently been a niche where analog machines are utilized because of their inherent strengths. Recent advancements in technology and analog computing techniques have begun to alleviate many of the disadvantages and make the method feasible for more applications.

The main advantage of analog computation can be summed up by computational efficiency. Computational efficiency can be quantified by time, space and energy. A.H. Kramer provides insight into computational efficiency [4]. He states “This added efficiency [in analog computation] may be expressed in terms of computational density: by providing an implementation that is more than an order of magnitude more dense than a digital implementation, analog techniques may allow for realization on a single chip what requires an entire board using digital techniques" [4]. This assertion alludes to the physical size of the hardware although it is applicable to energy efficiency and computation time as well. Kramer concludes in the article that "Analog implementations have higher design complexity and scale less easily than mainstream digital techniques, so they must offer a one to two order of magnitude efficiency gain over competing digital technologies to maintain a niche" [4]. Through time scaling techniques [5-7] it is clearly seen that a significant computation time advantage can be had utilizing analog methods. This is specifically true in cases where digital methods cannot feasible compute in real time, for example analysis of large non-linear systems. Very high energy efficiency has also been shown in analog hardware in comparison to traditional digital approaches [8]. In addition, with the advent of very-large-scale integration (VLSI) technology the spatial efficiency of analog computers is comparable to digital computers. While for general purpose computing it would be very inefficient to utilize an analog computer it would be tremendously beneficial to make use of analog computers in specific applications where they exhibit a large gain in efficiency over digital methods. Both analog and digital computers have been utilized in power systems and analog methods have historically been implemented when they were more efficient.

1.2.2 ANALOG COMPUTATION IN POWER SYSTEMS

Analog computation in power systems is certainly not a new endeavor. It is also used in a limited capacity today. In the late 1800's during the construction of his first electric power transmission network Thomas Edison commissioned the design and manufacture of an analog computer [9]. He oversaw the development of a miniaturized version of a power network by Francis R. Upton, Charles L. Clarke, and Samuel D. Mott that was employed as a computer for the actual network. This was for a direct current (DC) system. Alternating Current (AC) Network Analyzers (NA) were first developed in the 1920's to model and solve problems associated with power distribution systems [10]. They were later applied to transmission systems. These analyzers were essentially miniaturized power systems built with passive components such as resistors, capacitors and inductors. Bell Telephone Laboratories (BTL), Massachusetts Institute of Technology (MIT), and the Office of Naval Research (ONR) all actively developed and researched analog computing applications at some point in time. Development and use of analog computation grew throughout the twentieth century. Power system analyses were conducted exclusively in analog until digital computers came into the mainstream in the 1970's. In a short period of time digital methods overtook almost all analog computers for power system studies. They were much more precise and were easily programmable in comparison to their analog counterparts. The analog computers at that time required manual configuration of jumpers, potentiometers and other parameters for each computation. This required manual intervention and lengthy setup time for complex problems. Despite these shortcomings up through the 1960's analog computers were commercially available and considerably successful and efficacious. Many examples of these machines can be seen in [11]. Despite the fact that analog computing lost the commercial war to its digital counterpart there were still niche applications in power systems.

In 1990 the Kansai Electric Power Company (KEPCO) constructed a fully analog power system emulator. It is currently one of the largest in the world. This system was constructed with passive elements modeling major components of the power network. The emulator consists of 30 generators, 304 transmission lines, 20 loads, HVDC transmission facilities, and static var compensators [12]. This analyzer is based on a real world system and epitomizes some recent development for analog computation in the power systems field. One major application of this, and other NAs still in use, is for relay testing and coordination. These analyzers were built to operate in real time and provide an excellent test bed for relay systems. In addition, old analog network analyzers no longer in use are being utilized for undergraduate and research efforts in power systems [13].

Current and future development of analog computation looks to take advantage of associated strengths and overcome if not all then some of the historically congenital obstacles. Namely some major encumbrances are the large size of analog circuits, poor programmability/reconfigurability, and limited computational precision and measurement problems. An example of an older computational tool for power systems is shown in Figure 2 [14]. The figure shows the control panel for an analog transmission line simulator used for testing relays. This was a very powerful tool for its time but suffered from the drawbacks previously mentioned. New technological developments and research are making analog computation a more attractive and viable alternative.

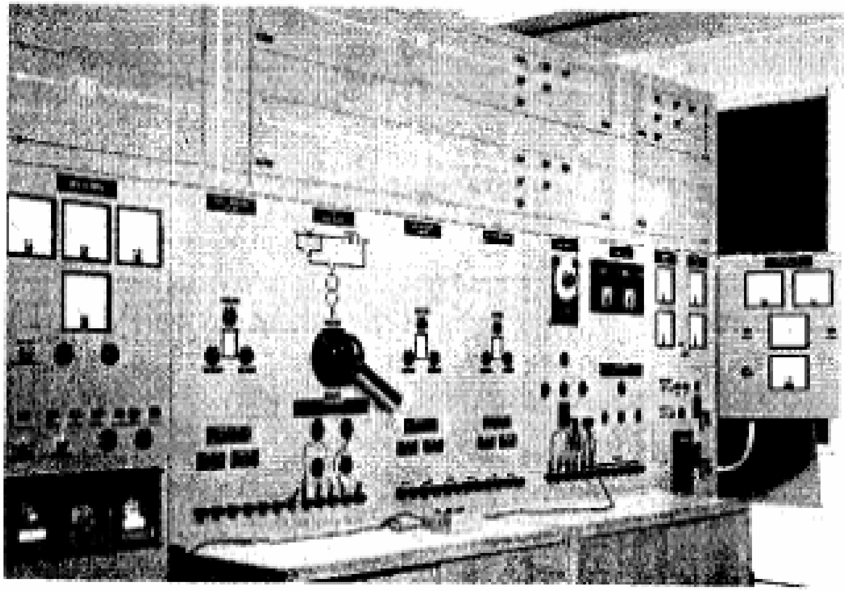


Figure 2: Analog Transmission Line Model Control Panel [14]

Recently, there has been a major thrust toward computational systems on a chip (SoC). These systems can allow for reconfiguration and programmability without the need of manually changing wires or settings. This push for SoC is being done with both analog and digital computational methods. Some examples are Field Programmable Gate Arrays (FPGA) and Field Programmable Analog Arrays (FPAA) [15].

Current research in the analog field is pushing towards VLSI implementation of various analog technologies to realize a SoC. This technology is well suited for power system analysis [1, 16-19]. Development in complimentary metal-oxide-semiconductor (CMOS) technology, the integration of bipolar junction transistors into CMOS technology (BiCMOS) and advancement of other analog VLSI technologies are paving the way for large-scale integration and accuracy for analog designs. Literally thousands of analog components can be fabricated on a wafer the size of a pushpin. In the older network analyzers the components were exceedingly large in comparison to microelectronics. As the system to be represented by the analyzer grew in size so did the analyzer itself. A realization of large systems with thousands of components is simply not feasible through a traditional NA. VLSI is the solution. Neural network computation methods is a VLSI example being studied [16, 17] along with Evolvable Hardware (EH) [18]. In this thesis, the main analog components for modeling of power systems in analog hardware are Operational Transconductance Amplifiers (OTAs). OTAs are fundamental building blocks of VLSI circuits. OTA technology specifically lends itself well to fabrication on a large scale and allows for remote reconfiguration via a controllable gain. This technology is paving the way toward programmability in a large-scale analog emulator for power systems.

1.2.3 DIGITAL COMPUTATION IN POWER SYSTEMS

Initially digital computers were limited to offline studies and simulated power system phenomena much slower than real time. Despite this limitation they became immensely popular due to easy use, programming and automation. As the technology matured and became more powerful, research into digital network analyzers began [23-26]. These efforts were moving towards real time digital computation. This has resulted in the release of commercial real time simulators by RTDS Technologies [19] and HyperSim [20] by Hydro-Quebec. These analyzers are essentially a collection of processors in parallel. They show promise but are arguably more complex in comparison to analog network analyzers and still have problems associated with digital computation.

The basic approach to achieve parallel computation in power systems with this method is to associate an independent processor or process with each power system component (transmission lines, generators, loads, etc.) or a set of components. Other methods dedicate a processor to each bus in the power system [21]. In contrast to an analog approach these digital methods require a vast array of complex devices (processors) sharing resources (memory) to construct and simulate a power system. In addition, these methods are approaching and/or reaching real time by increasing the incremental step size of computation and are not continuous mathematically as analog methods are. Currently available real time simulators are extremely expensive even for small system simulation. With current technology this approach is not viable for an online application, such as power system assessment, for a large system.

1.3 MOTIVATION

An overview of power system operation is shown in Figure 3. This is a closed loop process with human (system operators) intervention. The process is commonly referred to as Supervisory Control and Data Acquisition (SCADA). The system operators dispatch generation, control circuit breakers and switches based on detailed system information. This detailed information is provided through system measurement and analysis which is currently done through digital computers. Due to limitations of digital computers the information provided is typically incomplete (e.g. limited contingency analysis) and sometimes in the worst case absent all together (e.g. state estimator fails to converge). The failure of a state estimator was a leading cause of the August 2003 blackout in North America [22]. Based on the findings in this report it is evident that if better information is provided to system operators the system can be controlled in a more secure and efficient manner. Due to high computation efficiency an analog method could provide more robust power system security analysis hence providing system operators with better information. A more ambitious possibility would be to utilize an analog computer as a closed loop observer/controller for the power system.

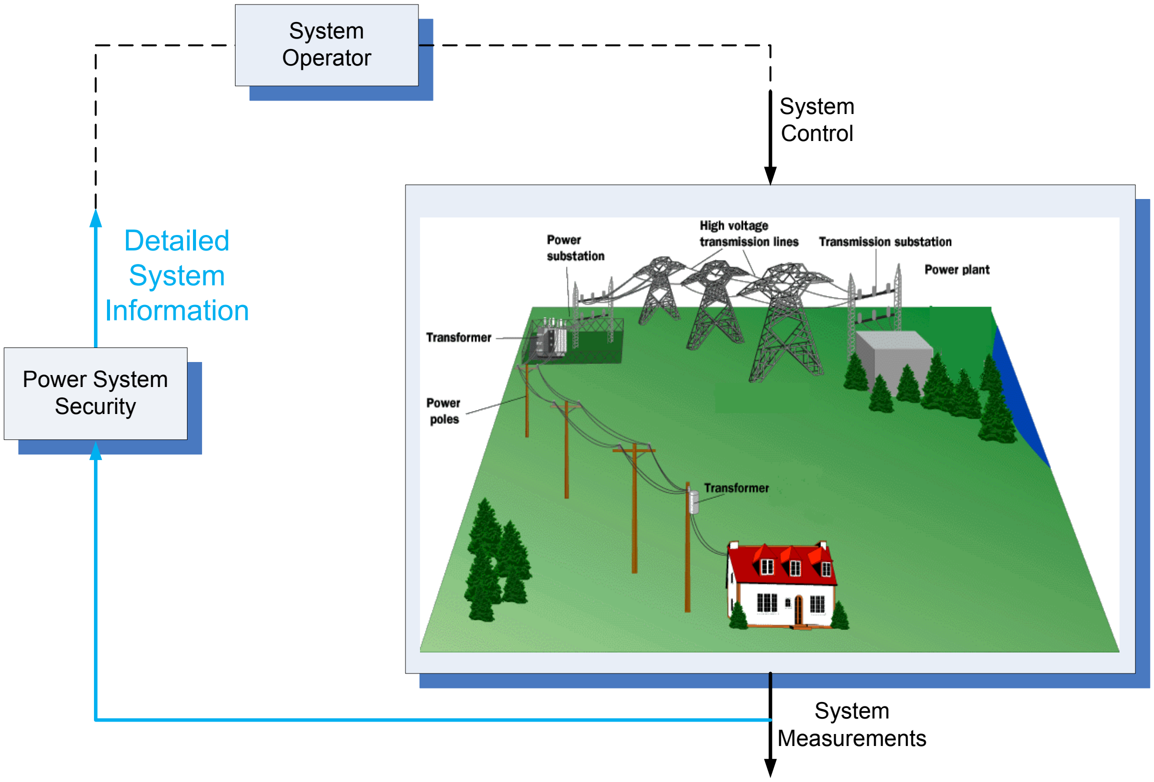
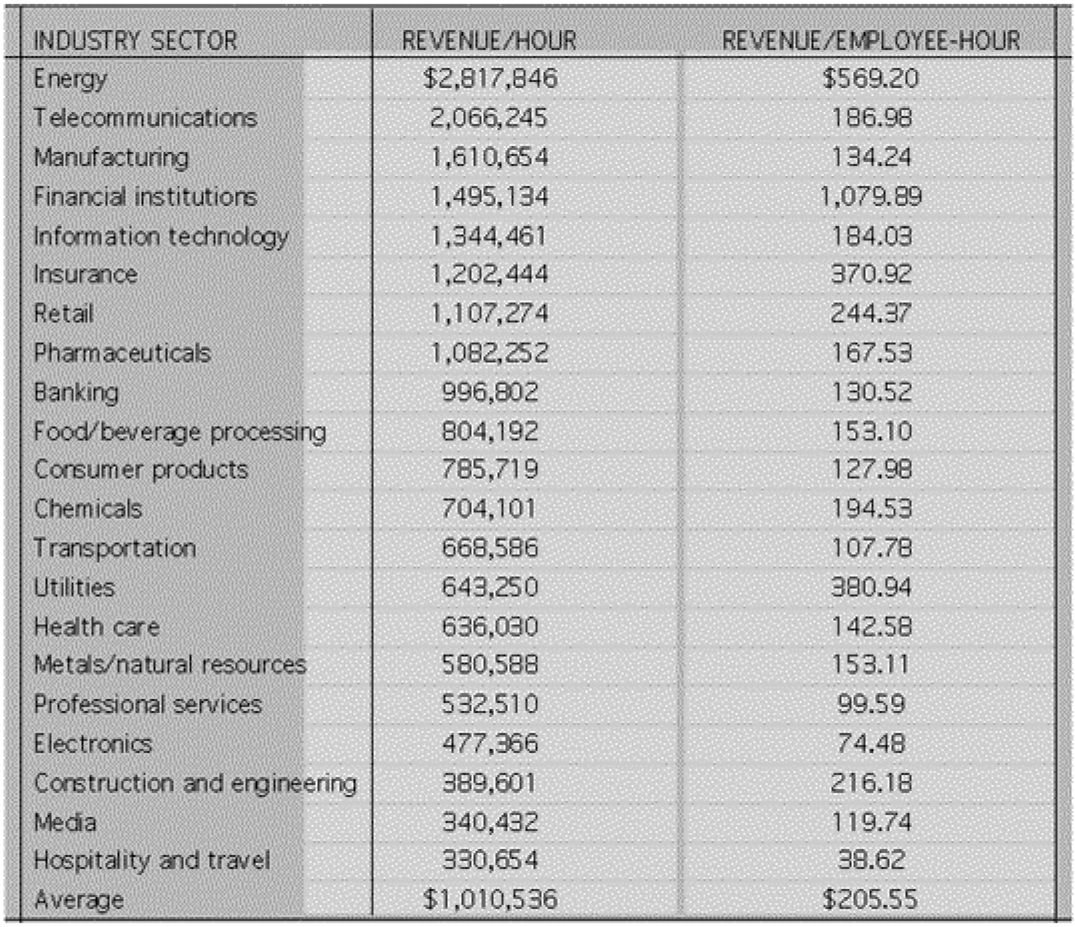


Figure 3: Power System Operation Overview

Presently digital computers analyze the power system security through state estimation, contingency analysis and SCOPF. Ideally state estimation would be conducted in real time and a thorough contingency analysis, including dynamic stability, be performed. Current digital computer technology cannot achieve this. State estimation is not done in real time; limited contingencies are studied and are restricted to static analysis. No online dynamic stability analysis is performed. Analog computation could potentially achieve the desired analyses and increase the reliability and security of the power system.

For the most part the power grid is extremely reliable. The majority of power outages are alleviated quickly and do not result in any major problems. Unfortunately the outages that are not alleviated quickly or easily tend to cause more serious problems especially economically. In addition, with the interconnection present in the power grid cascading failures are becoming more and more common and are of great concern in planning and operation stages. These failures affect large areas of power transmission and distribution systems and require significant time to fix the problems and bring equipment back online. A study published in 2004 by Lawrence Berkeley National Laboratory (Berkeley Labs) estimated that power outages result in monetary losses of eighty billion dollars annually [23] in America. With economic effects of that magnitude the motivation to push for even higher reliability of electric power is warranted. Some companies are so sensitive to power outages they build and operate their own power generation stations (cogeneration) to supplement utility power and to provide for critical loads in the event of a utility blackout. This is popular in manufacturing facilities where hours of downtime result in millions of dollars in losses of revenue. Table 2 [24] details the revenue loss in dollars per hour of operation and per employee-hour for different sectors of the economy.

Table 2: Cost of System Downtime in Different Industries



INDUSTRY SECTOR	REVENUE/HOUR	REVENUE/EMPLOYEE-HOUR
Energy	$2,817,846	$569.20
Telecommunications	2,066,245	186.98
Manufacturing	1,610,654	134.24
Financial institutions	1,495,134	1,079.89
Information technology	1,344,461	184.03
Insurance	1,202,444	370.92
Retail	1,107,274	244.37
Pharmaceuticals	1,082,252	167.53
Banking	996,802	130.52
Food/beverage processing	804,192	153.10
Consumer products	785,719	127.98
Chemicals	704,101	194.53
Transportation	668,586	107.78
Utilities	643,250	380.94
Health care	636,030	142.58
Metals/natural resources	580,588	153.11
Professional services	532,510	99.59
Electronics	477,366	74.48
Construction and engineering	389,601	216.18
Media	340,432	119.74
Hospitality and travel	330,654	38.62
Average	$1,010,536	$205.55

Improving grid reliability makes sense economically. Better reliability can be achieved by improving the infrastructure of the power system along with maintenance of the current system. The most critical component is in power system operation. This is where faster computation can lead to improved reliability. Power system operators want to economically dispatch electrical energy while allowing for system faults (contingencies) without loss of power to customers. This particular analysis requires massive computational efforts specifically related to contingency analysis and dynamic stability. Furthermore, this problem is growing even worse with the trend of deregulation. Prior to deregulation each utility locally operated their power system with minimal or no interaction with other utilities. The analysis was mainly limited to a single utility's power system. Now Regional Transmission Organizations (RTO), such as PJM, operate huge sections of the power grid and are required to run these analyses on systems with tens of thousands of nodes or buses. It is not feasible with current digital computation technology to run all the desired analysis while operating the system. Simplifying assumptions are made along with approximations on failure modes to speed up the processes and meet the demands of power system operation. If real-time computational tools are developed more thorough analyses could be conducted without the need for as many assumptions and shortcuts. Properly applied this increase in system analysis for real-time operations would allow better power system operation and higher reliability.

1.4 PROBLEM STATEMENT

The objective of this work is to develop necessary analog computation theory and methodology to utilize an analog computer for power system security assessment. In addition, for benchmarking and proof of concept, an analog emulator is designed and prototyped. Particularly it is desirable that the analog hardware be fast, accurate, remotely reconfigurable, and scalable for large system modeling and have the capability to be implemented into a VLSI design. These characteristics are necessary for an online application such as security assessment. Listed here are the main deliverables of this work:

1. Analog computation theory and methodology for power system security assessment
2. Power system models and hardware for analog computation
3. Computational algorithms and software for running the proposed analog computer

1.5 ORGANIZATION OF DISSERTATION

Information and theory for current methods of power system security assessment are provided in chapter two. Chapter three details the proposed method of analog power system security assessment and associated analog computation theory. Chapter four covers the methodology, power system models, and hardware of an analog power system emulator. Chapter five encompasses the proposed methodology for analog power system security assessment. Examples, results and analysis are presented in chapter six. In conclusion chapter seven summarizes the work presented in this dissertation and highlights the major contributions. In addition, future research paths are discussed.

2 POWER SYSTEM SECURITY ASSESSMENT

2.1 OVERVIEW

This chapter provides an overview on power system security assessment. Included is a summary of the theory and implementation of digital methods. The power system models, measurement models, computation methods, and limitations are presented. The modeling and theoretical information was gathered from [3, 25, 26]. A diagram detailing the current process of power system security is shown in Figure 4 [25].

Power system security is divided into three distinct tasks. Specifically these tasks are network model building (system monitoring), contingency analysis and secure optimal dispatch of generation. The inputs to this process are measurements acquired from the system. From these measurements, and knowledge of the power system structure, the current status of the system, both structurally (breaker/switch status, component status, etc.) and electrically (voltages, currents, power flows), is estimated. The estimation process consists of several subtasks.

In order to accurately estimate the electrical status of the system the physical structure, or topology, of the system must be known, the measurement data must be accurate, and the states to be estimated must be observable. The topology processor models the structure of the system based on knowledge of the system and measurement data. For example, if a line power flow is measured to be zero it could be reasonable to assume the line is not in service and eliminate it from the topology of the system. However, this line could still be in service and simply not transmitting any power based on the current operating point of the system. The topology processor needs to decide whether or not this line, and other components, is in service or not. In addition, there are external systems which are interconnected to the system being operated. These must also be accounted for in the topology processor. Typically information from external systems such as parameters and structure are not easily obtained. The external system is often modeled through an equivalent circuit at the bus, which interconnects the two systems. Once the topology is known the states (voltages) of the system can be estimated.

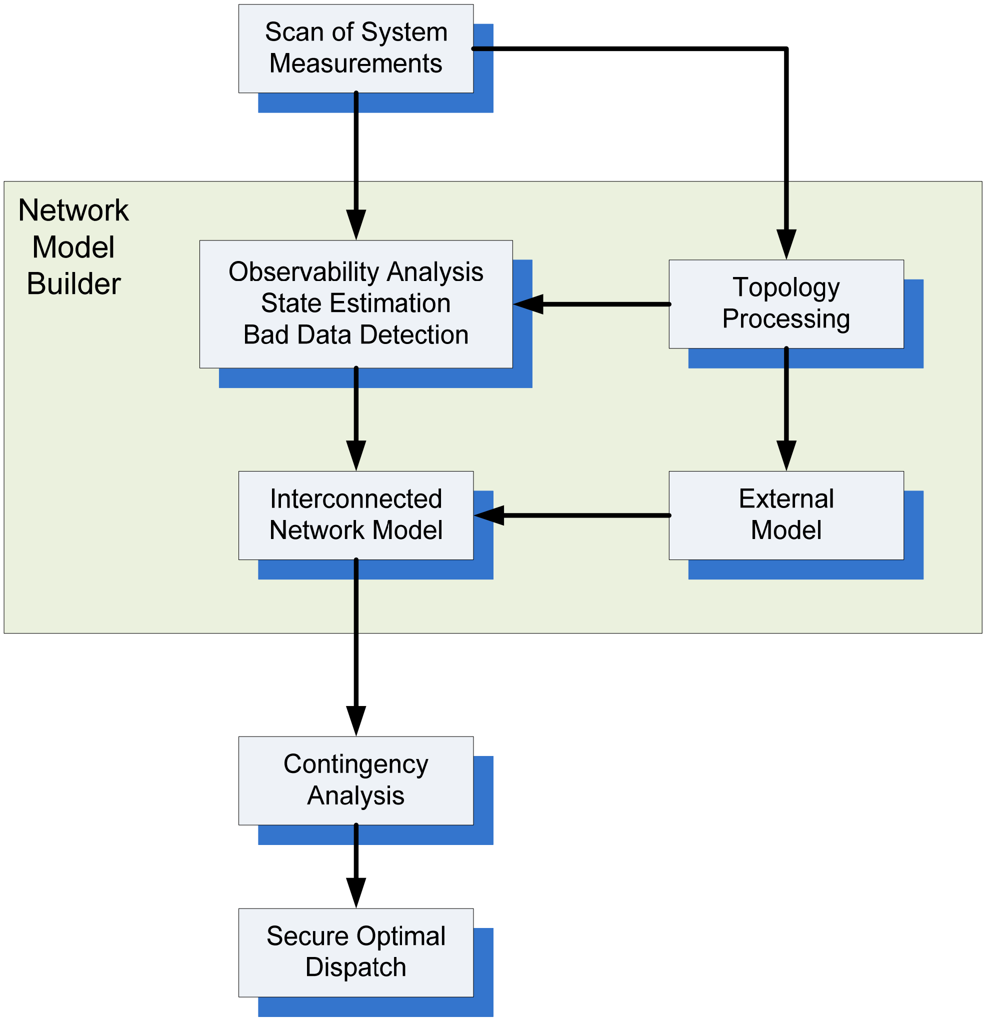

Scan of System Measurements
Network Model Builder
Observability Analysis State Estimation Bad Data Detection
Topology Processing
Interconnected Network Model
External Model
Contingency Analysis
Secure Optimal Dispatch

Figure 4: Power System Security Diagram

Before the states are estimated the system is first checked for observability. If all states are observable, the state estimator provides an estimate of the system states. Bad data is detected through post processing of the state estimator output. If bad data is detected it is removed and the state estimator is run again. Once a good estimate is found contingency analysis and secure optimal dispatch are conducted. This overall process requires tremendous computational power for a large nonlinear system and has certain limitations due to the current methods and technology.

2.2 DIGITAL METHODOLOGY

The power system is inherently non-linear and solution routines require iterative numerical methods. This results in an exponential increase in computation time as the system being analyzed increases in size. In addition, numerical instability can also arise. Much research has been conducted to decrease the computation time necessary to conduct power system security assessment. This includes, but is not limited to, limiting the number of cases being studied, decreasing the size of the system being examined and linearization/simplification of system models. Linearization of the power system models in particular results in a drastic increase in computation time but the accuracy of the results is insufficient for the purpose of security assessment. For example, the DC load flow methodology does not provide information on bus voltage magnitudes which is an important metric in evaluating system security.

2.2.1 POWER SYSTEM MODELS

Power system models can be separated into two classes, specifically dynamic and steady-state. Power system dynamics are typically modeled by non-linear ordinary differential equations (ODEs). Traditional digital methods for solving such equations, for example Euler's method, discretize the process and solve the equations for numerous points in time. The solution is then an estimate of the trajectory, or response of the system variables. Due to the nature of digital computation the step size of these solutions methods is finite. This is generally perceived as an approximate solution with errors and potential numerical instability. As step size decreases more accurate results can be obtained. However, a smaller step size increases computation time. With these techniques, current digital methods are not fast enough to perform dynamic analysis of large systems online. In order to speed up power system assessment a steady-state model of the power system is used for most analyses. In particular, power flow analysis is predominating in the security assessment procedure.

The basic power system model for power flow analysis is broken up into two main parts, the power system network and the power injections into the network. The network consists of transmission lines and transformers while the power injections are generators (positive injection of power) and loads (negative injection of power/power consumption). To further simplify analysis the system is often modeled with one phase instead of three. The assumption is that the system is balanced, or near balanced, across all three phases. A one line diagram of a five bus power system is shown in Figure 5 which is indicative of the single phase model of the power system. The generators are modeled as power injections, S_{Gi}, where i is the bus number where the generator is injecting power. In a similar fashion the loads are modeled as power injections S_{Di}. The lines connecting the buses are indicative of transmission lines or transformers.

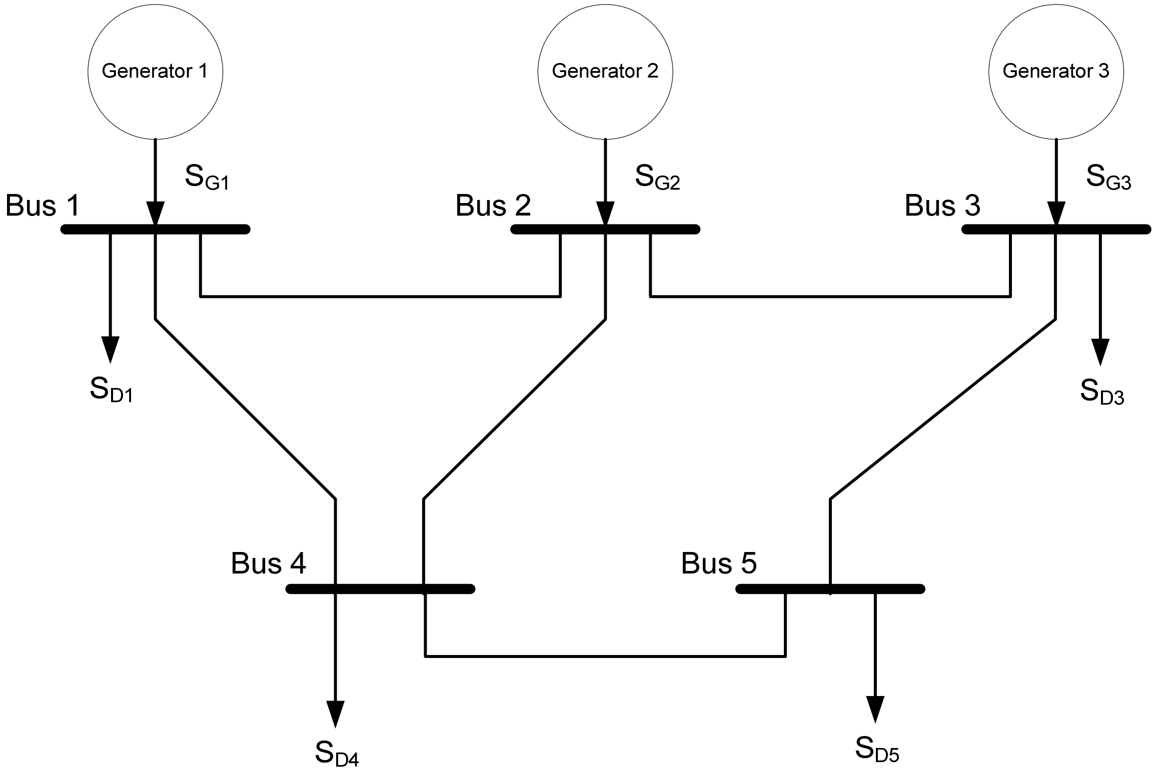


Figure 5: Five Bus Power System

The network of transmission lines and transformers transmit electrical power through the power system. A common method of analyzing the steady-state behavior of the network is through parameterization and modeling of the lines and transformers. Typically, each component of the network is modeled as a two-port network of passive components. The passive components used in this modeling approach are resistors, capacitors and inductors. The quantity of these parameters depends mainly on the conductors used and the physical or geometrical configuration of the lines and transformers. The conductors themselves will have certain characteristics, such as series resistance and reactance and shunt impedances from the terminals to electrical ground. In addition, there is inherently mutual inductance, or coupling, of the lines with respect to each other and in the transformers between the cores as they are bundled together or placed in close proximity to one another in a multi-phase system. With the power system normalized to a per-unit system both transformers and transmission lines can be modeled as impedances between two buses as shown in Figure 6. By modeling the network as an interconnection of impedance elements a bus admittance matrix can be used to characterize the behavior of the nodal voltages and currents of the system.

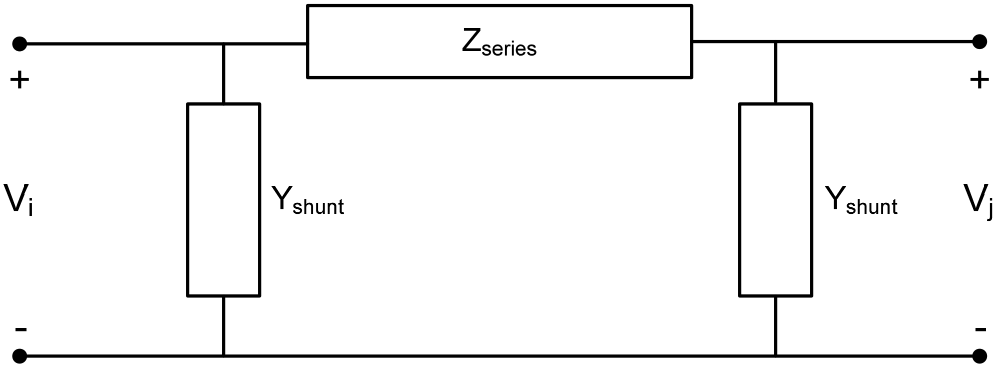


Figure 6: Equivalent Circuit for Transmission Line/Transformer

The nodal currents are related to the nodal voltages through the bus admittance matrix as follows:

$$\mathbf{I} = \mathbf{Y}_{\mathbf{bus}}\mathbf{V} \tag{2.1}$$

where for an n bus power system:

$\mathbf{I} \triangleq$ n x 1 vector of injected node currents

$\mathbf{Y}_{\text{bus}} \triangleq$ n x n bus admittance matrix

$\mathbf{V} \triangleq$ n x 1 vector of node voltages

The power system network can also be modeled as an impedance matrix (inverse of the admittance matrix). However, for most analyses the $\mathbf{Y}_{\text{bus}}$ representation is used. For details in building admittance and impedance matrices refer to [26].

Generators and loads are modeled as power injections into the network. Generally speaking generators are modeled as PV buses. More specifically they maintain constant power injection (P) and constant bus voltage magnitude (V). Assuming a generator has not reached its reactive power limits this is a fairly accurate model for steady-state analysis. Underlying assumptions are that there is sufficient regulation of the electrical power output and voltage magnitude through the mechanical input power (prime mover), and terminal voltage through the exciter. The Loads on the other hand are modeled as PQ buses indicating constant real (P) and reactive (Q) power. Numerically the analysis is usually conducted in polar coordinates. Each voltage and current is represented by a magnitude and a phase. The phase in particular requires a reference point. Usually one bus in the system is defined as the reference, or slack, bus. This bus is modeled as a voltage source with a known voltage magnitude and phase. Power flow methods are formulated based on this model or slight variations. The basic power flow problem is defined as the determination of system voltages and currents based on known power injections. For further details on power flow and iteration schemes, such as Newton-Raphson and Gauss-Seidel, refer to chapter 10 in [26]. The other class of power system modeling comprises dynamic models.

There exist many rich models for dynamic analysis of power systems. These models incorporate machine dynamics for generators and motor loads along with electro-magnetic dynamics for the network. Typically system dynamics are completely neglected for static security assessment. When system dynamics are incorporated for dynamic security assessment the electromagnetic and load dynamics are generally neglected to speed up computation. Only generator dynamics are included in the system model. The generator dynamics are modeled using the swing equation relating mechanical power input from the prime mover, P_M, to the electrical power output P_e:

$$M\ddot{\delta}+D\dot{\delta}+P_e\left(\delta\right)=P_M \tag{2.2}$$

where:

$\delta \triangleq$ phase angle of the internal generator voltage

$M \triangleq$ generator inertial coefficient

$D \triangleq$ generator damping coefficient

The resulting model of the power system consists of dynamic power injections from the generators dictated by equation (2.2) and steady-state line and load models as previously outlined. The measurement equipment embedded in the system is also modeled.

2.2.2 MEASUREMENT MODELS

Limited sets of measurements from the power system are provided to the system operators. Economically it is not feasible to measure every state in the system so a state estimator is used to estimate all the states of the system based on the system structure and measurements. The measurements obtained are inherently noisy and contain errors. Some measurements may contain very large errors if there is a problem with the sensor itself. The presence of error in measurement will naturally result in errors in state estimation. To mitigate the effects of measurement error, a detailed model of measurements, including error, are required. This section provides an overview of a measurement model which is utilized in state estimation.

Measurements obtained from the power system can be categorized as one of two types, measurement of an electrical quantity or the status of a switching element. The latter is discrete in nature, while the former is continuous. The status of a switching element is simply modeled as on or off. Errors in switch status measurement are also discrete. An error would be reporting incorrectly the status of the switch. For example, a measurement indicating a switch is open when in the system it is actually closed. Continuous quantities require a more advanced measurement model that accounts for uncertainty.

A continuous measurement will never be precise and will always contain some error. The concept of "random measurement error" has been used to formulate a detailed measurement model [3]. Assuming the measurement device provides a reading that is close to the true value and contains some unknown error the following model has been derived:

$$z^{meas} = z^{true} + \eta \tag{2.3}$$

where:

$z^{meas} \triangleq$ value of the measurement received from a measurement device

$z^{true} \triangleq$ unknown true value of the quantity being measured

$\eta \triangleq$ random measurement error

The random measurement error, η, represents the uncertainty present in measurement. Typically, it is assumed that there is no bias present in the measurement. With this assumption the probability density function (PDF) of η can be chosen as a Gaussian, or normal distribution with a zero mean:

$$PDF\left(\eta\right)=\frac{1}{\sigma\sqrt{2\pi}}e^{-\left(\frac{\eta^2}{2\sigma^2}\right)} \tag{2.4}$$

where σ is defined as the standard deviation and σ^2 the variance of η. With these parameters the model can be tuned to the specific measurement device. For example, a device which has a large measurement error will have a relatively large standard deviation as compared to a very accurate measurement device. This PDF is depicted graphically in Figure 7. Other PDFs could be chosen to model the uncertain measurement error but "normal distribution is commonly used for modeling measurement error since it is the distribution that will result when many factors contribute to the overall error." [3] Another factor which is important when conducting security assessment is the structure of the power system. The structure is determined through topology processing.

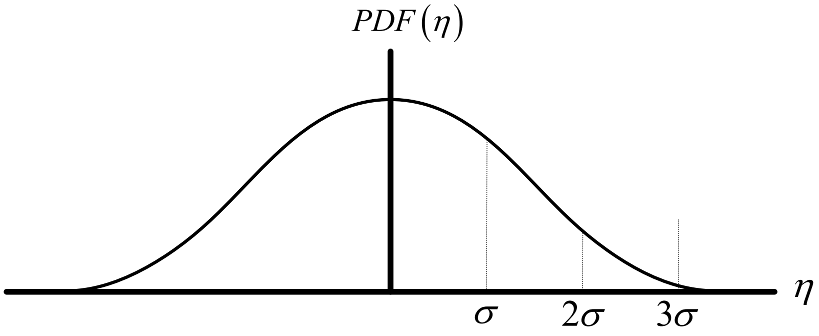


Figure 7: Gaussian Probability Density Function

2.2.3 TOPOLOGY PROCESSING

Topology processing is a procedure for determining the structure of the power system. This process determines the connectivity of the network (location of transmission lines, loads, generators, etc.), meter locations, and the status of switches and circuit breakers. Correct determination of topology is critical to other tasks in power system security assessment. Inherently if the topology of the power system is incorrectly identified, all further analysis based on the topology is flawed. For example, an accurate state estimate may never be found as topology errors can appear as measurement errors in post processing of state estimation. In addition, contingency analysis specifically examines the system response to a list of topology changes. With an incorrect initial topology the pre contingency and post contingency topologies will be incorrect resulting in erroneous solutions.

Topology processing is a difficult task due to the complex structure of an interconnected power system. Figure 5 is a simplified one line electrical diagram of the physical structure of the power system. This simplified diagram, with the addition of meter types and locations, is the output of the topology processor. In order to determine the topology, and the corresponding one-line diagram, a more detailed bus-section/switching device view of the system is required as proposed in [27]. An example of such a model is shown in Figure 8.

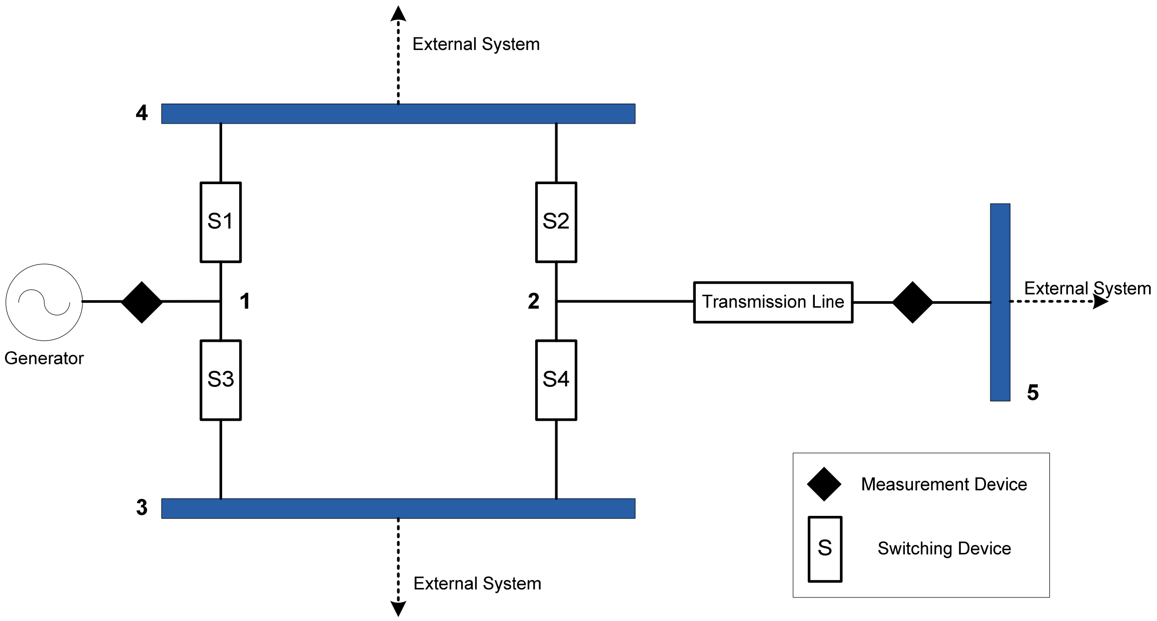


Figure 8: Bus-Section/Switching Device Power System Example

This example system consists of five nodes (numbered on through five), two measurement devices, four switching devices (numbered S1 through S4) which represent physical switches or circuit breakers, along with a generator and transmission line. Physically the number of possible switch states is 2^n where n is defined as the number of switches. For this example there are 2^4, or 16, potential physical configurations. The possible electrical configurations of the system are a subset of the physical configurations. For example, if all switches are closed the electrical configuration would result in a two bus system as shown in Figure 9. Through inspection it can be determined that if any three switches are closed the same two bus electrical configuration would result. Examining all sixteen switching states yields twelve potential electrical configurations. Graph theory can be utilized to determine how many unique electrical configurations exist for a given bus-section/switching device structure.

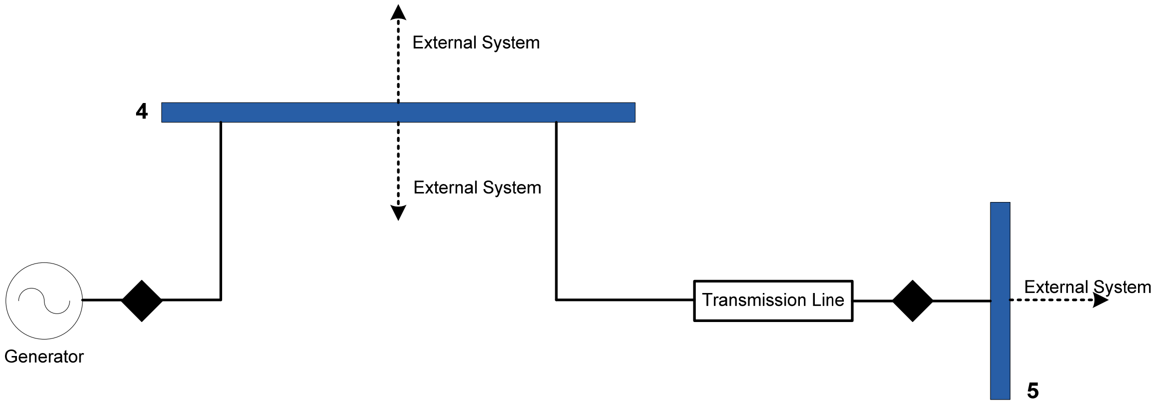


Figure 9: Electrical Configuration

The power system topology is determined based on the known bus-section/switching device diagram and system measurements. The topology is not always easily determined. In certain cases insufficient measurements can result in multiple potential topologies. In addition, erroneous data could lead to incorrect identification of topology. Data is preprocessed and checked for consistency to help correctly determine the topology. Basic tests on the data include verification of operating limits, checking for non-zero flows in open switches and for non-zero voltage difference across closed switches. These tests can help identify erroneous or inconsistent data and lead to more accurate topology processing. State estimation is performed after the topology is determined.

2.2.4 STATE ESTIMATION

The purpose of state estimation is to approximate the state variables of the system based on measurements. In power systems the state variable are usually defined as the magnitude and phase of nodal voltages. This is a statistical process due to the nature of the measurements. There are numerous statistical criteria that could be applied such as maximum likelihood, weighted-least-squares (WLS) or minimum variance. WLS is one of the more common criteria and is presented here. This derivation was obtained from [3].

The WLS state estimation problem is formulated as a minimization "of the sum of the squares of the difference between each measured value and the true value being measured (expressed as a function of our unknown parameter)" [3]. The difference of squares is "weighted" based on the measurement accuracy. More specifically they are weighted by the variance of the meter error. The minimization expression when estimating a single parameter is:

$$\min_{x} J(x) = \sum_{i=1}^{N_m} \frac{\left(z_i^{meas} - f_i(x)\right)^2}{\sigma_i^2} \tag{2.5}$$

where

$f_i \triangleq$ function relating the state to the ith measurement

$\sigma_i^2 \triangleq$ variance of the ith measurement

$J(x) \triangleq$ measurement residual

$N_m \triangleq$ number of independent measurements

$z_i^{meas} \triangleq$ ith measured quantity

This formulation is easily expanded for estimating any number of states. For estimating N$_s$ states with N$_m$ measurements:

$$\min_x J\left(x_1, x_2, \ldots, x_{N_s}\right) = \sum_{i=1}^{N_m} \frac{\left(z_i^{meas} - f_i\left(x_1, x_2, \ldots, x_{N_s}\right)\right)^2}{\sigma_i^2} \tag{2.6}$$

This can be written in the following form

$$\min_x J\left(x\right) = \left[\mathbf{z}^{\mathbf{meas}} - \mathbf{f}\left(\mathbf{x}\right)\right]\left[R^{-1}\right]\left[\mathbf{z}^{\mathbf{meas}} - \mathbf{f}\left(\mathbf{x}\right)\right] \tag{2.7}$$

where $\mathbf{z}^{\mathbf{meas}}$ is defined as the measurement vector:

$$\mathbf{z}^{\mathbf{meas}} = \begin{bmatrix} z_1^{meas} \\ z_2^{meas} \\ \vdots \\ z_{N_m}^{meas} \end{bmatrix} \tag{2.8}$$

$\mathbf{f}\left(\mathbf{x}\right)$ is defined as the function vector relating states to measurements:

$$\mathbf{f}\left(\mathbf{x}\right) = \begin{bmatrix} f_1\left(\mathbf{x}\right) \\ f_2\left(\mathbf{x}\right) \\ \vdots \\ f_{N_m}\left(\mathbf{x}\right) \end{bmatrix} \tag{2.9}$$

and $\left[R\right]$ as a diagonal matrix called the covariance matrix of measurement errors:

$$\left[R\right]=\begin{bmatrix}\sigma_1^2 & & & \\ & \sigma_2^2 & & \\ & & \ddots & \\ & & & \sigma_{N_m}^2\end{bmatrix} \tag{2.10}$$

If $\mathbf{f}\left(\mathbf{x}\right)$ is linear it can be put in the form $\mathbf{f}\left(\mathbf{x}\right)=\left[H\right]\mathbf{x}$ where $\left[H\right]$ is an N$_m$ by N$_s$ matrix containing the coefficients of the functions $f_i\left(\mathbf{x}\right)$. In linear form equation (2.7) can be solved directly for the estimate of the states. The states resulting in the minimum $J\left(x\right)$ can be found by setting the gradient of the residual equal to zero and solving for the states. Expanding equation (2.7) and taking the gradient yields:

$$\nabla J\left(\mathbf{x}\right)=-2\left[H\right]^T\left[R^{-1}\right]\mathbf{z}^{\mathbf{meas}}+2\left[H\right]^T\left[R^{-1}\right]\left[H\right]\mathbf{x} \tag{2.11}$$

With $\nabla J\left(\mathbf{x}\right)=0$ the estimates states $\mathbf{x}^{\mathbf{est}}$ can be solved for by:

$$\mathbf{x}^{\mathbf{est}}=\left[\left[H\right]^T\left[R^{-1}\right]\left[H\right]\right]^{-1}\left[H\right]^T\left[R^{-1}\right]\mathbf{z}^{\mathbf{meas}} \tag{2.12}$$

It is clear that in order to solve equation (2.12) that the inverse of $\left[[H]^T\left[R^{-1}\right][H]\right]$ must exist. The inverse exists if the states being estimated are observable. If the states are not observable a singularity will be present and the state estimate cannot be found. In practical terms, so long as there are a sufficient number of non-redundant measurements observability will be maintained. If observability of the system cannot be maintained a subset of the system can still be estimated. Those states that are unobservable need to be removed from estimation procedure. Often times if there are not sufficient measurements pseudo-measurements can be implemented to gain observability. A pseudo-measurement is an unmeasured value determined based on knowledge of the system. For example, the generator power output is typically maintained very close to the dispatched value. Assuming this generator is operating properly the real power injection can be used as a pseudo-measurement in the state estimator without measurement. Typically in power systems the state estimation problem is overdetermined. More specifically the number of measurements is greater than the number of states being estimated $\left(N_m > N_s\right)$. This allows for a better and more robust estimate as compared to completely determined or underdetermined cases.

A closed form solution for estimation only exists for linear systems, or more specifically when the functions $\mathbf{f}\left(\mathbf{x}\right)$ are linear. For AC power systems the functions $f_i\left(x_1, x_2, ..., x_{N_s}\right)$ are based on the nonlinear power flow equations:

$$\begin{aligned} P_i &= \sum_{k=1}^{n} |V_i||V_k|\left(G_{ik}\cos\theta_{ik} + B_{ik}\sin\theta_{ik}\right) \\ Q_i &= \sum_{k=1}^{n} |V_i||V_k|\left(G_{ik}\sin\theta_{ik} - B_{ik}\cos\theta_{ik}\right) \end{aligned} \tag{2.13}$$

$J(\mathbf{x})$ terms for real and reactive power flows across a transmission line from bus i to bus j would then be:

$$\frac{\left\{\mathbf{MW}_{\mathbf{ij}}^{\mathbf{meas}} - \left[|E_i|^2 G_{ij} + |E_i||E_j|\left(\cos\left(\theta_i - \theta_j\right)G_{ij} + \sin\left(\theta_i - \theta_j\right)B_{ij}\right)\right]\right\}^2}{\sigma_{\mathbf{MW}_{ij}}^2} \tag{2.14}$$

and

$$\frac{\left\{\mathbf{MVAR}_{\mathbf{ij}}^{\mathbf{meas}} - \left[-|E_i|^2 B_{ij} + |E_i||E_j|\left(\sin\left(\theta_i - \theta_j\right)G_{ij} - \cos\left(\theta_i - \theta_j\right)B_{ij}\right)\right]\right\}}{\sigma_{\mathbf{MVAR}_{ij}}^2} \tag{2.15}$$

Due to the nonlinear nature of $J(\mathbf{x})$ a closed form solution to equation (2.6) does not exist. To solve this equation iterative approaches, such as Newton's method, are required. The process is similar to that of solving AC power flow. Initial conditions are specified for $\mathbf{x}^{\mathbf{est}}$ and updated each iteration until it converges to a feasible solution that satisfies $\nabla J(\mathbf{x}) = 0$. The gradient of $J(\mathbf{x})$ is:

$$\nabla J(\mathbf{x}) = \begin{bmatrix} \frac{\partial J(\mathbf{x})}{\partial x_1} \\ \frac{\partial J(\mathbf{x})}{\partial x_2} \\ \vdots \\ \frac{\partial J(\mathbf{x})}{\partial x_{N_s}} \end{bmatrix} = -2 \begin{bmatrix} \frac{\partial f_1(\mathbf{x})}{\partial x_1} & \frac{\partial f_2(\mathbf{x})}{\partial x_1} & \cdots & \frac{\partial f_{N_m}(\mathbf{x})}{\partial x_1} \\ \frac{\partial f_1(\mathbf{x})}{\partial x_2} & \frac{\partial f_2(\mathbf{x})}{\partial x_2} & & \vdots \\ \vdots & & \ddots & \\ \frac{\partial f_1(\mathbf{x})}{\partial x_{N_s}} & & \cdots & \frac{\partial f_{N_m}(\mathbf{x})}{\partial x_{N_s}} \end{bmatrix} \begin{bmatrix} \frac{1}{\sigma_1^2} & & & \\ & \frac{1}{\sigma_2^2} & & \\ & & \ddots & \\ & & & \frac{1}{\sigma_{N_m}^2} \end{bmatrix} \begin{bmatrix} z_1^{meas} - f_1(\mathbf{x}) \\ z_2^{meas} - f_2(\mathbf{x}) \\ \vdots \\ z_{N_m}^{meas} - f_{N_m}(\mathbf{x}) \end{bmatrix} \tag{2.16}$$

The Jacobian of $\mathbf{f}(\mathbf{x})$ is defined as:

$$\frac{\partial \mathbf{f}(\mathbf{x})}{\partial \mathbf{x}} = [H] = \begin{bmatrix} \frac{\partial f_1(\mathbf{x})}{\partial x_1} & \frac{\partial f_1(\mathbf{x})}{\partial x_2} & \cdots & \frac{\partial f_1(\mathbf{x})}{\partial x_{N_s}} \\ \frac{\partial f_2(\mathbf{x})}{\partial x_1} & \frac{\partial f_2(\mathbf{x})}{\partial x_2} & & \vdots \\ \vdots & & \ddots & \\ \frac{\partial f_{N_m}(\mathbf{x})}{\partial x_1} & & \cdots & \frac{\partial f_{N_m}(\mathbf{x})}{\partial x_{N_s}} \end{bmatrix} \tag{2.17}$$

equation (2.16) can then be written as:

$$\nabla J(\mathbf{x}) = -2[H]^T[R]^{-1}\begin{bmatrix} z_1^{meas} - f_1(\mathbf{x}) \\ z_2^{meas} - f_2(\mathbf{x}) \\ \vdots \\ z_{N_m}^{meas} - f_{N_m}(\mathbf{x}) \end{bmatrix} \tag{2.18}$$

This form is analogous to equation (2.11) and can be solved by using an iterative method. The state estimation procedure as shown here assumes that the system topology is correct and that the measurement data is good. If this is not the case the resulting estimate will be poor. Post processing of the state estimation result can provide insight and determine if bad data is present or topology errors exist.

A simple check for measurement accuracy is to examine the residual of each state based on the estimate as shown in equation (2.19). If the measurement z_i^{meas} is bad the resulting residual, $J(x_i)$, will be large. A hypothesis testing approach can be applied to detect the presence of a bad measurement. Topology errors will also cause large residuals and can be incorrectly identified as bad measurements using this technique. It is difficult to discern between bad data and topology errors without adjusting the topology, re-estimating the states, and processing the results again. It would be advantageous to have a technique which can easily identify the source of the error.

$$J(x_i) = \frac{\left(z_i^{meas} - f_i\left(\mathbf{x}^{\mathbf{est}}\right)\right)^2}{\sigma_i^2} \tag{2.19}$$

2.2.5 CONTINGENCY ANALYSIS

Contingency analysis analyzes the power system response to an outage of a component or multiple components. Typically an outage of a single device per contingency is investigated. This is commonly referred to as 'n-1' contingency analysis where the system consists of n devices and analysis is performed with the loss of one device. Contingencies consisting of multiple outages can be handled in a similar fashion but the discussion here is limited to n-1 contingency analysis. Due to the number of simulations required for n-2 contingency analysis it is hardly ever conducted during system operation. Sometimes a select few multiple outage contingencies are examined, but not a full analysis. A flowchart for a typical contingency analysis procedure is outlined in Figure 10.

The initialized system model is obtained from the topology processor and state estimator. This initialized system is simulated numerous times for the loss of any single generator or any single line. The results of each contingency are analyzed for stability and line flows/voltage levels are checked against predefined limits for violations. If any violations or instabilities are present they are flagged and further analyzed during SCOPF. Contingency analysis is historically broken up into two distinct types. Dynamic contingency analysis, commonly referred to as Dynamic Security Assessment (DSA), and steady-state contingency analysis.

It is desirable to simulate a detailed power system model in the time domain for each contingency. This provides the best and most accurate information concerning system stability. However, due to computational constraints this cannot be performed during system operation. Much research has been conducted to develop methods for contingency analysis suitable for real time [28-32]. Numerous methods have been developed to allow for faster computation. Popular techniques are outlined below:

1. Run a limited number of selected important contingencies [28-30]
2. Utilize faster, non-time domain dynamic simulation techniques (e.g. Energy function methods) [31]
3. Utilize steady-state simulation techniques and neglect dynamic stability [28, 29]
4. Run time domain simulations on a subset of the whole system or for a short time frame [30]

Contingency selection, or screening, is a technique which attempts to identify contingencies that are most threatening to system operation and only conduct analysis on this limited set of cases. Inherently this is a subset of all system contingencies. If this subset can be identified with a degree of accuracy then only a small number of actual contingencies are required to be computed for security purposes. This results in a substantial savings of computation.

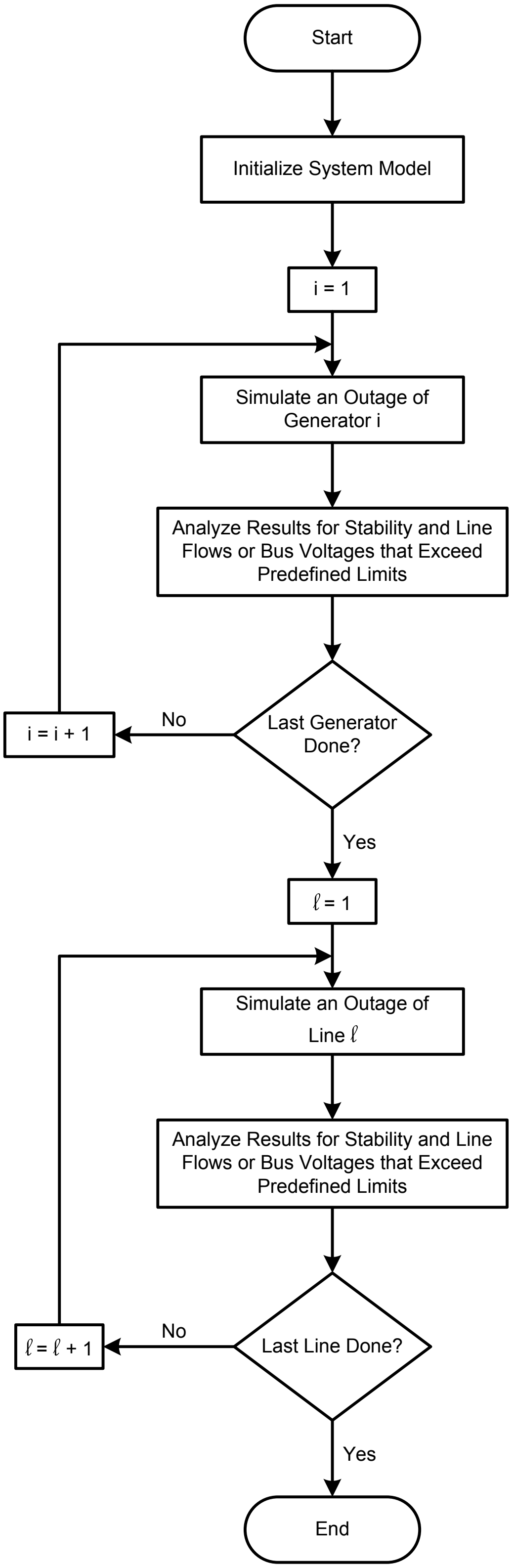

Start
Initialize System Model
i = 1
Simulate an Outage of Generator i
Analyze Results for Stability and Line Flows or Bus Voltages that Exceed Predefined Limits
Last Generator Done?
No
i = i + 1
Yes
ℓ = 1
Simulate an Outage of Line ℓ
Analyze Results for Stability and Line Flows or Bus Voltages that Exceed Predefined Limits
Last Line Done?
No
ℓ = ℓ + 1
Yes
End

Figure 10: Contingency Analysis Procedure

The basic premise of contingency selection is to perform some quick, approximate, analyses for each contingency and rank them according to severity. Performance indices (PI) have been introduced for this purpose. An overload performance index is defined as follows [3]:

$$PI = \sum_{\substack{\textbf{all branches} \\ \ell}} \left(\frac{P_{flow\,\ell}}{P_{\max}^{\ell}} \right)^{2n} \tag{2.20}$$

where

$P_{flow\,\ell} \triangleq$ power flow on line ℓ

$P_{\max}^{\ell} \triangleq$ maximum power flow on line ℓ

$n \triangleq$ parameter for the performance index

The PI is computed for each contingency and the contingencies are ranked based on this index. The power flow on each line can be approximated quickly by either linearized DC power flow or by a single iteration of an AC power flow method. Once the contingencies are ranked a decision needs to be made on which contingencies are further analyzed. Those contingencies with a relatively high PI will be run but it is a cost benefit decision to determine the cutoff point where cases are no longer simulated. Many other performance indices can be formulated and defined. For example, bus voltage magnitude could be incorporated into the index although this would require AC analysis. Through contingency selection computation time is substantially reduced. However, important contingencies could inadvertently be filtered out based on the definition and robustness of the performance index, and the quality of the fast approximate analysis performed to quantify the index. In practice this screening technique is utilized heavily in both dynamic and steady-state contingency analysis.

Steady-state contingency analysis performs all computation using a steady-state model of the power system. All dynamics are neglected. A basic approach is to incorporate the contingency into the power system model and perform a power flow. The result is then analyzed for limit violations. A full AC power flow technique is preferable although DC power flow and linear sensitivity techniques based on partial derivatives are often used to speed up computation. This steady-state analysis provides little information on power system stability. Low voltage magnitude results from an AC power flow are indicative of voltage stability problems but further analysis is required verify system stability.

The main objective for dynamic contingency analysis is to determine if the system maintains stability for a given disturbance, or contingency. A power system stability definition has been proposed as "the ability of an electric power system, for a given initial operating condition, to regain a state of operating equilibrium after being subjected to a physical disturbance, with most system variables bounded so that practically the entire system remains intact" [33]. The most accurate way to determine stability is to perform a full time domain simulation on the system. For dynamic contingency analysis it is not feasible to conduct a full time domain simulation of a large system. Specific tools have been developed in order to speed up this process. These tools analyze subsets of the overall problem of dynamic stability.

Dynamic stability of power systems has been recently defined with three forms of stability [33]:

1. **Rotor Angle Stability (Transient Stability)**: refers to the ability of synchronous machines of an interconnected power system to remain in synchronism after being subjected to a disturbance.
2. **Voltage Stability**: refers to the ability of a power system to maintain steady voltages at all buses in the system after being subjected to a disturbance from a given initial operating condition.
3. **Frequency Stability**: refers to the ability of a power system to maintain steady frequency following a severe system upset resulting in a significant imbalance between generation and load.

This classification is a subset of the broad problem of power system stability. State of the art tools for fast dynamic contingency analysis examine transient stability and voltage stability. Frequency stability is usually not examined during operation. For small disturbances a linearized analysis through eigenvalues and eigenvectors of the system yield approximate results very quickly. This analysis is sufficient for small disturbances but inaccurate for larger disturbances. For large disturbances energy function techniques have been proposed [31] with some success. However, the energy methods are limited to single swing analysis and do not always correctly determine the stability of the system. As for voltage stability techniques, the fast approximate methods utilize quasi-dynamic time domain simulations.

2.2.6 COMPUTATIONAL PROCEDURE AND LIMITATIONS

As outlined in this chapter the overall computational procedure for power system security assessment consists of topology estimation, state estimation and contingency analysis. This process requires numerous calculations which increase in number as the system being studied increases in size. In addition, the computation time for each calculation increases with system size. For example, the solution time of the Newton-Raphson algorithm is a quadratic function of system size. The computation time is so significant due to the nonlinear nature of power systems. Listed below are some specific limitations of state of the art methods of power system security assessment:

1. Iterative solution methods are required.
2. Numerical instability exists in solution methods.
3. Simplified power system models are required in many analyses.
4. Limited number and types of analyses are performed due to time constraints.
5. Many solutions are approximated with linearized/fast solution methods.

Despite these limitations the operation of the power system remains fairly secure and the reliability very high. This is generally achieved by operating the power system in a conservative manner. With this in mind, there is much room for improvement in security assessment. Many of the existing limitations can be overcome by a drastic increase in computational resources. There is a great deal of research and development of large parallel processing and cluster computing systems to yield more computational power. However, for operation and security of large power systems (thousands of buses) this is simply not economically feasible to implement such a system at this time. In addition, numerical stability issues will remain. Another approach, which is proposed and investigated in this dissertation, is to apply a different computational methodology to the problem. The next chapter provides an overview of the theory and methodology pertaining to the application of analog computers to power system security assessment.

3 ANALOG METHOD FOR POWER SYSTEM SECURITY ASSESSMENT

This chapter provides an overview of the proposed approach to power system security assessment by means of analog computation. A summary of theory and progression of analog computation is included. Some of the concepts for analog computation are similar to those of digital methods, for example, the requirements of initial conditions for integration. Other concepts are unique to analog methods. New analog computation concepts necessary for this work are clearly defined and explained in this chapter. In conclusion, the necessary requirements, both theoretical and computational, to implement an analog approach to power system security assessment are identified.

3.1 ANALOG COMPUTATION THEORY

Historically analog computation has been limited mostly to offline applications in power systems. Generally speaking, with the exception of analog controllers, analog computation has never been utilized as an online tool. However, new advancements and research are indicating it is possible to apply analog methods in online applications. Specifically, advancements in microelectronics, such as remote control, reconfigurability, and VLSI, are paving the way for future analog computation applications. However, unlike digital computation, analog methods do not have the benefit of mature computational theory.

In the infancy of computation theory, long before digital computers, Alan Turing and Alonzo Church provided some basic theoretical framework. Turing went so far as to clearly define an abstraction of a computer called a "Turing machine" which was used heavily in his efforts in computation. Turing's work paved the way for subsequent computation techniques and theories.

A Turing machine is purely conceptual. There have been many examples and refinements over time but the machine was never meant to be constructed, or for that matter viewed as a practical computational tool. In retrospect, the basic Turing machine is essentially a finite state machine operating in a sequential manner. Turing's main purpose for the machine was thought experiments. These thought experiments allowed for the development and refinement of rich computation theory.

Turing published much of his work on computation in a publication titled "On Computable Numbers, with an Application to the Entscheidungsproblem." [34] Turing deduced that "Logical computing machines (i.e. Turing machines) can do anything that could be described as rule of thumb or purely mechanical" [35]. In related work, Church developed a definition to ascertain the computability of a function. He defined a function as "effectively calculable" if there is an effective method for calculating the values of the function. This led to a combined Church-Turing theory. This theory states that if an algorithm exists then an equivalent Turing machine for this algorithm also exists. In other words any problem in which a solution method can be defined recursively through an algorithm is intrinsically computable. With this theory, in addition to the development of computers, it can be deduced that a computer can be constructed to solve any effectively calculable function. In the work presented here an analog computer has been constructed to emulate the behavior of a power system.

Emulation is defined as "When one system performs in exactly the same way as another, though perhaps not at the same speed" [36]. The emulator developed here represents a large jump from the thought experiment Turing machines. Due to inherent differences, and the application to power system security assessment, some new terms and theory are introduced for analog computation and system emulation. The first definition deals specifically with computability in analog computers:

Analog Computable: A function, or set of functions is analog computable if for a given set of input(s) an analog method can provide a correct output.

This is a more general definition, which is applicable to any function and any form of analog computation. For example, this can be applied to a mechanical differential analyzer, a general purpose analog computer, or an analog emulator as in this work. Generally speaking, this definition states that for a predefined function, or set of functions, and given input(s), the value(s) of the function(s) can be provided by the analog method only if the problem is analog computable. In other words a set of m functions with n inputs as shown in equation (3.1) is analog computable if it can be evaluated and solved with an analog method. The correct output is defined as an output of the analog method that satisfies the defined function(s) based on the input(s). An answer, or correct output, can be unique in the case of many-to-one or one-to-one functions or multiple solutions can exist for multiple-valued functions. Computability does not depend upon or require a unique solution.

$$\begin{gathered} f_1\left(x_1, x_2, \ldots, x_n\right) \\ f_2\left(x_1, x_2, \ldots, x_n\right) \\ \vdots \\ f_m\left(x_1, x_2, \ldots, x_n\right) \end{gathered} \tag{3.1}$$

Analog computability can be determined for any arbitrary set of functions and inputs for any analog method. The evaluation of computability is deterministic. The problem is either computable or not computable. Specifically in this research the focus is on analog computation of power systems. The following lemmas clarify the concept of analog computability as applied to power system analysis.

Power system analysis is traditionally separated into static, or steady-state, and dynamic analyses. Static analysis provides information at an equilibrium point of the system. More specifically, it is assumed that the states of the system are not changing with time and averaged values of states are used. Root-mean-square values of voltages and currents are used in power system analysis. Dynamic analysis provides information on the behavior of the power system over an interval of time where the states are changing. The following two lemmas elucidate computability for power systems in both static and dynamic cases respectively.

Lemma 1: Analog computability in a steady-state sense is determined based on the static functions modeling the power system and the set of inputs to the analog computer.

The functions that model the power system are derived from the power system structure, parameters, and component models. For example, for an n bus AC power system the current injections can be modeled as a function of bus voltages:

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1n} \\ y_{21} & y_{22} & & \vdots \\ \vdots & & \ddots & \\ y_{n1} & & \cdots & y_{nn} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = f\left(v_1, v_2, \ldots, v_n\right) \tag{3.2}$$

where

$i_i \triangleq$ the complex current injection into bus i

$v_i \triangleq$ the complex voltage at bus i

$y_{ij} \triangleq$ the complex element of the Ybus matrix in row i, column j

Generally speaking the power system states are known if all voltage and current injections are known. In this formulation the power system is computable if all n bus voltages (2n inputs as these voltages are complex) are provided as an input to an analog method that has an output proportional to the function $f\left(v_1, v_2, \ldots, v_n\right)$. More specifically, the output of the analog method should be linearly proportional based on the time and magnitude scaling, if present, between power system values and analog method values. However, this formulation of steady-state computability of the power system is not unique. The following representation is equivalent to equation (3.2) and computable if all the current injections are provided as an input to an analog method that has an output linearly proportional to $f\left(i_1, i_2, ..., i_n\right)$:

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} y_{11} \; y_{12} & \cdots & y_{1n} \\ y_{21} \; y_{22} & & \vdots \\ \vdots & \ddots & \\ y_{n1} & \cdots & y_{nn} \end{bmatrix}^{-1} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} = f\left(i_1, i_2, ..., i_n\right) \tag{3.3}$$

Another formulation of power system steady-state behavior is to relate current injections to power injections into the system:

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix}^* = \begin{bmatrix} v_{11} \; v_{12} & \cdots & v_{1n} \\ v_{21} \; v_{22} & & \vdots \\ \vdots & \ddots & \\ v_{n1} & \cdots & v_{nn} \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_n \end{bmatrix} = f\left(s_1, s_2, ..., s_n\right) \tag{3.4}$$

where

$s_i \triangleq$ power injection into bus i

$v_{ij} \triangleq$ element of the bus voltage matrix in row i, column j

The bus voltage matrix is defined based on the complex power flowing through a branch of the power system network:

$$S_{ij} = V_{ij} I_{ij}^* \tag{3.5}$$

where

$S_{ij} \triangleq$ the power flowing from bus i to bus j

$V_{ij} = V_i - V_j$

$I_{ij} \triangleq$ the current flowing from bus i to bus j

and the power flows through branches are related to power injections by:

$$S_i = \sum_{j=1}^{n} S_{ij} \tag{3.6}$$

The bus voltage matrix can be constructed based on the following rules. For off diagonal entries:

$$v_{ij} = \begin{cases} \dfrac{-1}{V_{ij}} & \textbf{if} \;\; y_{ij} \neq 0 \\ 0 & \textbf{if} \;\; y_{ij} = 0 \end{cases} \tag{3.7}$$

For diagonal entries:

$$v_{ij} = \sum \frac{1}{V_{ij}} \quad \textbf{for all } V_{ij} \textbf{ where } \; y_{ij} \neq 0 \tag{3.8}$$

Equation (3.4) expresses current injections into the power system as a function of power injection. This formulation is analogous to the traditional power flow problem. Traditionally, the power flow problem is defined as solving for voltages based on power injections. However, solving for currents is analogous to solving for voltages as previously shown in equations (3.2) and (3.3). Similar to power flow equation (3.4) is computable in a digital sense. An iterative approach such as Newton-Raphson could be used to solve the equation. The problem is computable in an analog sense if all the power injections are provided as an input to an analog method that has an output proportional to $f\left(s_1, s_2, ..., s_n\right)$. A more general computability formulation for steady-state power system analysis can be formulated if the analog method for computation is more clearly defined.

If an analog method that behaves, or has the same functional behavior, like the power system network exists, then question of computability can be determined by analyzing the following more general representation of a power system:

$$\begin{bmatrix} i_1 \\ \vdots \\ i_m \\ i_{m+1} \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} Y_1 & V_1 \\ Y_2 & V_2 \end{bmatrix} \begin{bmatrix} v_1 \\ \vdots \\ v_m \\ s_1 \\ \vdots \\ s_q \end{bmatrix} = f\left(V, S\right) \tag{3.9}$$

This representation handles the relationship of current to both voltages and power injections. Computability for an n bus system requires a total of n voltages and power injections as inputs $\left(m+q=n\right)$. Another specification for computability is that there exists only one input per bus. In other words, either a voltage or power injection at each bus is required as an input. This equation reduces to equation (3.2) if the only inputs are voltages and equation (3.4) if the only inputs are power injections. An analogous form of this equation can also be written in which current and power injections are inputs and bus voltages the output. It is also common in power system analysis to have inputs that are only a component of the bus voltage or power injection. For example, a generator bus is often modeled as a PV bus in which the voltage magnitude and real power injection are specified. This type of input can be handled with the following representation of the power system where the inputs are m bus voltage magnitudes, r bus voltage angles, p real power injections, and q reactive power injections:

$$[I]=\left[Y_{|V|}\ Y_{\theta}\ V_{P}\ V_{Q}\right]\begin{bmatrix}|V|\\ \theta\\ P\\ Q\end{bmatrix}=f\left(V,S\right) \tag{3.10}$$

where

$|V|\triangleq$ an m x 1 vector of bus voltage magnitudes

$\theta\triangleq$ an r x 1 vector of bus voltage angles

$P\triangleq$ a p x 1 vector of real power injections

$Q\triangleq$ a q x 1 vector of reactive power injections

$Y_{|V|}\triangleq$ an n x m matrix relating current injections to bus voltage magnitudes

$Y_\theta \triangleq$ an n x r matrix relating current injections to bus voltage angles

$V_P \triangleq$ an n x p matrix relating current injections to real power injections

$V_Q \triangleq$ an n x q matrix relating current injections to reactive power injections

Computability in the steady-state sense is achieved if:

$$m + r + p + q = 2n \tag{3.11}$$

It is clear that the set of inputs to yield computability is not unique. Many different sets of inputs can be defined which result in computability. The next lemma deals with analog computability for dynamic cases.

Lemma 2: Analog computability in a dynamic sense is determined based on the differential equations modeling the power system and the set of inputs to the analog computer. An nth order system that can be represented in canonical form is computable in an analog sense if and only if a computable set of n first order differential equations can be obtained.

Power system dynamics are typically modeled by non-linear ordinary differential equations (ODEs). Traditional digital methods provide approximate solutions with errors and potential numerical instability. Computability becomes hard to identify when approximate solutions are obtained. The following are questions often linked with digital computability: How much numerical error is required before the solution is deemed incorrect, and hence incomputable? How do you insure the instability of a system during simulation is not due to numerical instability? Intrinsically analog techniques integrate continuously and do not have this particular problem. This is analogous to an infinitely small step size in digital methods.

Analog computability can be determined by simply analyzing the differential equations and inputs to the system. For example, a second order generator model has been shown in equation (2.2). This equation can be solved by analog methods by direct integration (in this case D=0):

$$\delta = \frac{1}{M}\int\int\left(P_M - P_E\left(\delta\right)\right)dtdt \tag{3.12}$$

This is computable in an analog sense if the initial conditions, P_M, and $P_E\left(\delta\right)$ are specified and the analog method can operate based on these inputs and functions. The initial conditions requirement is the same for digital methods. The form of the analog method is shown in Figure 11. This is a double integrator circuit with feedback for $P_E\left(\delta\right)$, an input for P_M, and the capability of setting initial conditions on the output of the integrators. This circuit will naturally solve for the dynamic response of the generator angle by direct integration. This is a major advantage over the discretized nature of digital integration techniques. Analog integration experiences no numerical instability. However, in practice analog techniques do have some unique limitations.

Most limitations of analog techniques are due to non-ideal behavior of analog hardware. In certain instances this can cause the emulator to behave differently than the system being emulated. For example, if the slew rate of the emulator is less than the rate of change of the system variables then the result of integrating equation (3.12) in the emulation hardware will be different than the actual system. The variables in emulation will not change as quickly as the real world system if the slew rate is not as fast as the system being emulated. In addition, in steady-state saturation of components in the emulator could yield incorrect results. In practice, the following are additional questions that must be addressed when determining analog computability: How do you insure the instability of a system during emulation is not due to saturation or failure of analog devices? How much measurement error is required before the answers obtained are deemed incorrect or inaccurate? These questions must be addressed in the design and operation of the analog emulator. More specifically, through proper scaling of the system into analog hardware many of the issues can be resolved. More details are provided concerning the specific emulator in this work in chapter four.

The power system consists of numerous generators and other dynamic components. All of these dynamics can be modeled by a set of differential equations. Computability for this system model is achieved if computability for all the differential equations holds. Generally speaking if an nth order system can be represented in canonical form, the system can be represented by n 1st order differential equations. The power system models used in this work can be represented in such a canonical form. As a direct result, computability of the system can be determined by analyzing computability of each first order differential equation individually. If each first order differential equation is computable then the nth order system is computable through equivalency to the n first order differential equations. Likewise, if the nth order system is computable it is equivalent to a system of n first order differential equations which is by equivalency also computable. Larger order equations must be examined to determine computability for systems that cannot be reduced to canonical form.

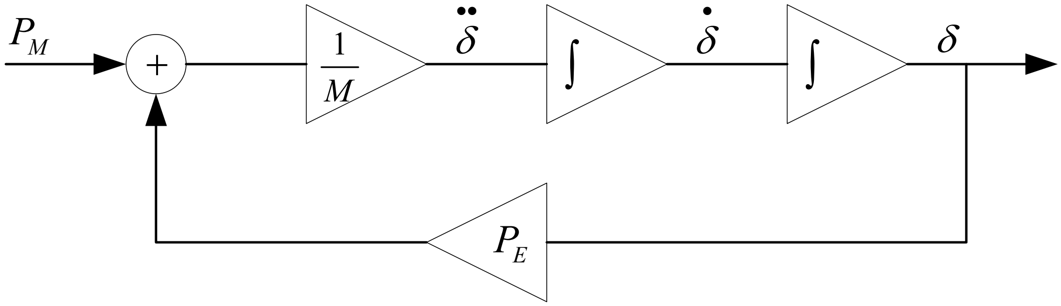


Figure 11: Block Diagram of Analog Method to Compute Swing Equation

Lemmas 1 and 2 dealt with steady-state and dynamic computability of power systems. Often times these two concepts are analyzed concurrently. One method in power systems is to model machines dynamically and the network statically. This is done by setting algebraic constraints (based on the network model) on the differential equations. Analog computability for such a method can be determined by analyzing computability in the steady-state sense for static models and the dynamic sense for dynamic models. Computability in both the static sense and dynamic sense is required for such analysis. If the algebraic constraints are not computable then the constraints on the differential equations will yield an incorrect steady-state result in the analog computer. This incorrect result yields an incorrect answer to the algebraically constrained differential equations which negates computability. The lack of dynamic computability will affect static computability in the same fashion. In summary, in order to compute algebraically constrained differential equations by an analog method steady-state and dynamic analog computability are required. This relates directly to power systems as these types of equations are often used to represent the system.

The concept of analog computability in power systems was examined through a definition of analog computability and associated lemmas. These lemmas described the requirements for analog computability. Essentially, for analog computability, an analog method must provide a correct response of the defined function based on the input(s). The inputs and/or functions are arbitrary in this definition. Power system emulation, or more generally system emulation, is examined next. Emulation was previously defined as "When one system performs in exactly the same way as another, though perhaps not at the same speed." A more specific term for this work, system emulation, is now defined as follows:

System Emulation: The process of emulating the behavior of a system at a specified point in time at equilibrium or for a specified interval of time.

It is clear that in order to emulate a power system, or any system for that matter, with an analog method that computability is required. However, computability alone is not necessarily sufficient in order to emulate the behavior of a given system. Theorem 1 outlines the necessary requirements for system emulation through analog computation.

Theorem 1: System emulation can be performed by an analog method if and only if all the following criteria are met:

1. A correctly defined functional description of the system is known.
2. Correctly defined input(s) to the system are known.
3. The system is computable in the analog sense.

The requirements for system emulation are much stricter than those for analog computability. Analog computability is based upon an arbitrary set of inputs and functions. Depending on the particular problem, the inputs may or may not be arbitrary. For example, if the objective is to emulate the behavior of the power system in real time the inputs to the emulator are required to match the real world system in real time. In addition, the functional behavior of the emulator must also match the real world system. If the system is computable, and the inputs are correct, the emulator will output the result dictated by the functional description of the system. However, the analog computer may not behave like the system being emulated if the functional description of the system is not adequate. If it is assumed that the functional description, or model, of the system is correct, and the inputs are known, or specified, then determining if system emulation is possible reduces to determining computability. However, for some applications these assumptions will result in large deviations between the emulator behavior and the actual system. The result in these cases is an emulator that is not behaving like the system being emulated. Generally speaking system emulation is dealing with a specific real world system. To get an analog emulator to behave exactly like, or close enough within specified tolerances, the real system, the models and inputs to the system are not arbitrary. As a result, the question of correctly modeling the system and determining the inputs is not necessarily deterministic.

Models can be developed, verified, and analyzed for accuracy. Strictly speaking a model will never be perfect but it can be justified based on testing, benchmarking and validation. In order to emulate a system the model has to be deemed acceptable, or in other words correctly defined. The inputs to the system must also be correctly defined in order to emulate a system.

In many applications the inputs to the system are not explicitly known. For example, in power system state estimation the inputs are measurements with noise and errors. This noise can be modeled and accounted for. Errors can be detected and eliminated from the analysis. The result is that the inputs are estimates of the actual system values. For the purpose of analog computation, these estimates can be accepted as correctly defined inputs in cases where the inputs are not explicitly known. This approach is used in this work for power system security assessment with analog methods. The inputs to the emulator are estimated from measurement and system data. Details on the determination of these inputs are in chapter five. In addition, due to the uncertain nature of analog computation, the system emulation process is not deterministic. This is in contrast to digital emulators.

Throughout the development of digital computers many processors, microprocessors and different computing architectures have been created. Often times compatibility issues arise when a software package or process is ported to a different architecture. One way to deal with these incompatibilities is to emulate the older architecture on the newer architecture. This can be a deterministic process because the architectures operate within a strictly defined framework. For example, the instruction set of a processor is specifically defined. Any processor can be made to operate just like another processor if the full instruction set can be performed or emulated.

With this overview Theorem 1 can be proven:

Assuming that the system can be emulated the three requirements are verified by contradiction:

1. If the system model is incorrect the result obtained from the analog method will deviate from the system behavior. This contradicts the assumption that the system can be emulated.
2. If the inputs to the analog computer are not correct the results obtained from the analog method will deviate from the system behavior. This contradicts the assumption that the system can be emulated.
3. If analog computability is not maintained the results obtained from the analog method will deviate from the system behavior. This contradicts the assumption that the system can be emulated.

Conversely, assuming that the three conditions are true it is shown that a system can be emulated:

1. Based on the definition of system emulation the analog method must reproduce the behavior of the system
2. The behavior of a generic system can be described as shown in equation (3.1). This is replicated here:

$$\begin{gathered} f_1\left(x_1, x_2, \ldots, x_n\right) \\ f_2\left(x_1, x_2, \ldots, x_n\right) \\ \vdots \\ f_m\left(x_1, x_2, \ldots, x_n\right) \end{gathered}$$

3. The system consists of m functions , $\left(f_1(\cdot), f_2(\cdot), \cdots\cdots, f_m(\cdot)\right)$, and n inputs, $\left(x_1, x_2, \cdots\cdots, x_n\right)$.
4. Assuming a correctly defined function of the system is known an analog method can correctly evaluate the functions describing the system.
5. Assuming the inputs are correctly defined they can be applied to the analog method.
6. Assuming the system is computable, the analog method will evaluate the functions and provide the correct output for the correct inputs.
7. The analog method will then behave exactly like the definition of the system satisfying system emulation requirements..

Theorem 1 states that the inputs to the emulator must be correct in order to emulate the system. This is a general requirement. This requirement for steady-state and dynamic system emulation is refined by the next two theorems. These theorems focus on the input requirements. It is assumed that the models are correct and the system is analog computable:

Theorem 2: If a set of inputs for an analog computer are correctly defined for a specified equilibrium point then the system can be emulated in a steady-state sense at the specified equilibrium point.

This theorem is proven by contradiction:

1. Assume the system cannot be emulated in a steady-state sense.
2. It is assumed that the functional description of the system is correctly defined.
3. It is assumed that the system is analog computable in the steady-state sense (lemma 1).
4. From theorem 1 the system is emulatable if the correct values of inputs are known.
5. By definition of steady-state analysis the only values of inputs required are those at the specified equilibrium point.
6. The system is emulatable in steady-state since the inputs are known at the equilibrium point.

7. This contradicts the assumption that the system is not emulatable in steady-state sense.

Steady-state analysis by its nature assumes that the states of the system are not changing in time. In other words there is no dynamic behavior in the system. In reality this is not the case. The system is always evolving and moving dynamically. One way to view steady-state analysis is assuming the system is in equilibrium. For a specified moment in time the system states can be analyzed and are not in motion. In order to emulate a system for a moment in time the inputs must be synchronized. The inputs must all be correct or known for the same instant in time. If the inputs are not synchronized then the output will not represent what the system did or is doing at that moment in time. This result is particularly important in power system analysis which relies on telemetered data. In order to properly emulate the behavior of the system at a point in time the data must be synchronized, or at the very least very near synchronous with some level of tolerance that can be deemed acceptable. Theorem 3 deals with system emulation in the dynamic sense.

Theorem 3: If a set of inputs for an analog computer are correctly defined for a specified interval in time then the system can be emulated in a dynamic sense for the specified interval of time.

This theorem is a natural extension of theorem 2. It is proven by contradiction:

1. Assume the system cannot be emulated in a dynamic sense for an arbitrary time interval: $t_0 \le t \le t_0 + \tau$ for $\tau \ne 0$.

2. It is assumed that the functional description of the system is defined correctly.

3. It is assumed that the system is analog computable in the dynamic sense (lemma 2).

4. From theorem 1 the system is emulatable if the correct values of inputs are known for the time interval $t_0 \le t \le t_0 + \tau$ for $\tau \ne 0$.

5. By definition of dynamic analysis the values of inputs required are across the specified time interval.

6. The system is emulatable in the dynamic sense across the time interval since the inputs are known across this interval.

7. This contradicts the assumption that the system is not emulatable in a dynamic sense.

This result is important to analysis of power system dynamics. To accurately emulate the dynamics of the system information on inputs to the system over the entire interval of time to be analyzed is required. Theorems 2 and 3 focused on the inputs applied to the emulator. It was assumed that the functional description of the system was correct and that the system was computable. In a similar fashion, the requirements for a functional description of the system and analog computability could be defined and proven.

Within this framework a system emulation process has been defined. In order to properly emulate the system the procedure for system emulation must evaluate computability and whether or not the system is emulatable. A general process of system emulation was derived from these results. This process is shown as a flowchart in Figure 12.

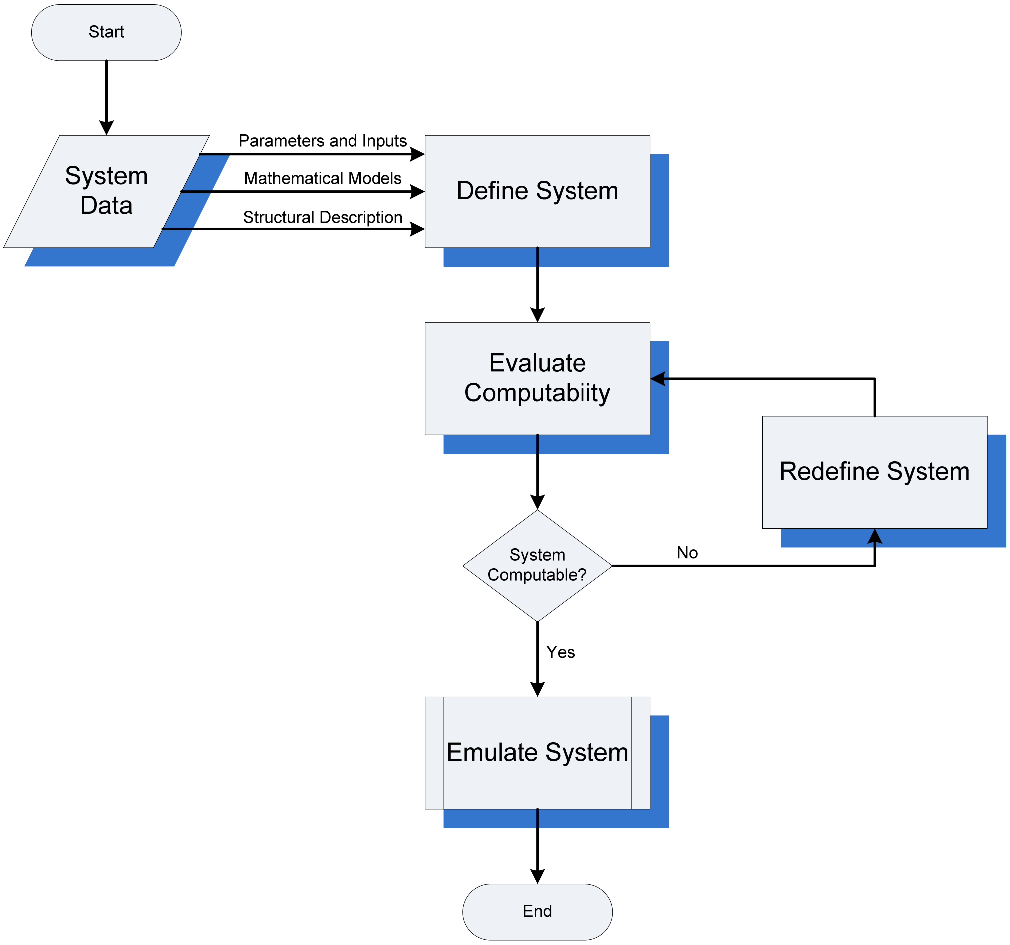


Figure 12: Generic System Emulation Process

In order to emulate a system, it is first defined. This definition is formulated from system data. This system data consists of system parameters, models, known data, measured data, system structure, etc. Computability can then be determined through analysis of this system definition and the desired outputs from the emulator. With a correct definition of the system and appropriate inputs, the system can be emulated if it is computable. If it is not computable then the system must be redefined in order to emulate it. For example, if not enough inputs are known the system can not be emulated. However, with the provided inputs a subsystem may exist that is computable and emulatable. Another important factor in this analog computation theory is the physical limitations of the analog emulator or method.

Emulation can be performed by a variety of different methods such as a mechanical process, electrical process, etc. The domain (temporal) and range (spatial) of operation are finite for all methods. This finite nature results in some restrictions to computation. If the system is emulated in the time domain then the limitations consist of slew rate of the analog hardware and reasonable time to solution. The slew rate of the analog hardware must be greater than or equal to the system being emulated. If not the emulator response will be slower and different than the system being emulated. The analog method must also yield a solution in a reasonable time. Emulation of slowly occurring phenomena in real time may result in long computation time. For example, it would take approximately 75 years to emulate one period of Halley's Comet in real time. The typical solution to this problem is to incorporate time scaling factors in the emulator. The process can be emulated along the same range but at a fraction of the time period. The behavior can then be solved for and monitored in a reasonable fashion. A similar scaling process can allow for proper handling of a system's range in emulation.

The range of the analog hardware is finite. This is due to device limitations, saturation effects, etc. For example, if emulating an electric transmission system which operates at 765kV it would be unreasonable to emulate this within the same range with a

CMOS circuit. It is not physically possible to maintain or create 765kV in such a device. However, a magnitude scaling factor can be introduced to scale the range of the real world system to a level appropriate for the emulator. For example, one volt in the CMOS circuit could be equivalent to the nominal 765kV level of the transmission system. A similar, although different, process is used for per unit normalization of power systems.

It is clear that the physical limitations of the analog hardware could result in incorrect results in emulation. In fact, the analog emulator could even be destroyed if the limits of the devices are surpassed during emulation. Theorem 4 addresses the physical limitations of an emulator and how these limitations pertain to system emulation. It is assumed that the requirements of theorem 1 are satisfied.

Theorem 4: If there exists a linearly scaled one-to-one mapping between the system being emulated and the emulator then a system can be emulated.

This theorem is proven through contradiction:

1. Assume that the system cannot be emulated.
2. A linearly scaled one-to-one mapping between a generic system and a generic emulator can be defined as follows:

$$f\left(x_{sys}, t_{sys}\right) = g\left(\alpha \cdot x_{emul}, \frac{t_{emul}}{\tau}\right) \tag{3.13}$$

for all x in the range of $f\left(x,t\right)$ and all t in the domain of $f\left(x,t\right)$.

where

$x_{sys} \triangleq$ a vector of states of the system to be emulated

$t_{sys} \triangleq$ time of the system to be emulated

$f\left(x_{sys}, t_{sys}\right) \triangleq$ functional description of the system to be emulated

$\alpha \triangleq$ a row vector scaling the states of system into the range of emulator

$\tau \triangleq$ a scalar time scaling factor that scales the system domain into the emulator domain

$x_{emul} \triangleq$ a vector of states of the emulator

$t_{emul} \triangleq$ time of the emulator

$g\left(x_{emul}, t_{emul}\right) \triangleq$ functional description of the emulator

3. It is assumed the requirements of theorem 1 are satisfied.
4. By definition of emulation an emulator defined by equation (3.13) will emulate the system.
5. This contradicts the assumption that the system is not emulatable.

The emulation process presented here is distinctly different than well established simulation techniques. Well established simulation techniques determine the behavior of the system through a process which does not function like the system being simulated. For example, a numerical simulation can integrate functions using a trapezoidal rule and provide an output of the results. This method is numerically based and at no point mimics the behavior of the system being simulated. However, the output, assuming the correctness of the model and numerical solution technique, will be the same as the actual system. Computation time for simulation and emulation also differ.

The computation time for digital techniques is clearly defined. This time is based on the frequency of the system clock and how many clock cycles it takes to complete the simulation. Many factors, including finite memory and latency, effect simulation time of digital methods. The process of analog emulation is much different. A clear definition for analog computation time is required. In comparison to digital techniques an analog emulator operates as if there is an infinite clock rate with no memory limits or latency. These properties are what allow for very fast computation. However, there are other limiting factors that must be accounted for when defining computation time.

Assuming the system can be emulated, the process of emulation comprises three steps as shown in Figure 13. The emulator must first be configured and initialized based on system inputs and parameters. At this point emulation begins through actuation of the emulator. Lastly, data must be extracted from the system to provide results. The overall computation time is defined as the summation of time spent on these three steps:

$$t_{comp} = t_{conf} + t_{emul} + t_{acq} \tag{3.14}$$

where

$t_{conf} \triangleq$ time required to configure and initialize the emulator.

$t_{emul} \triangleq$ time required to emulate the system.

$t_{acq} \triangleq$ time required to acquire the desired data from the emulator

$t_{comp} \triangleq$ total computation time

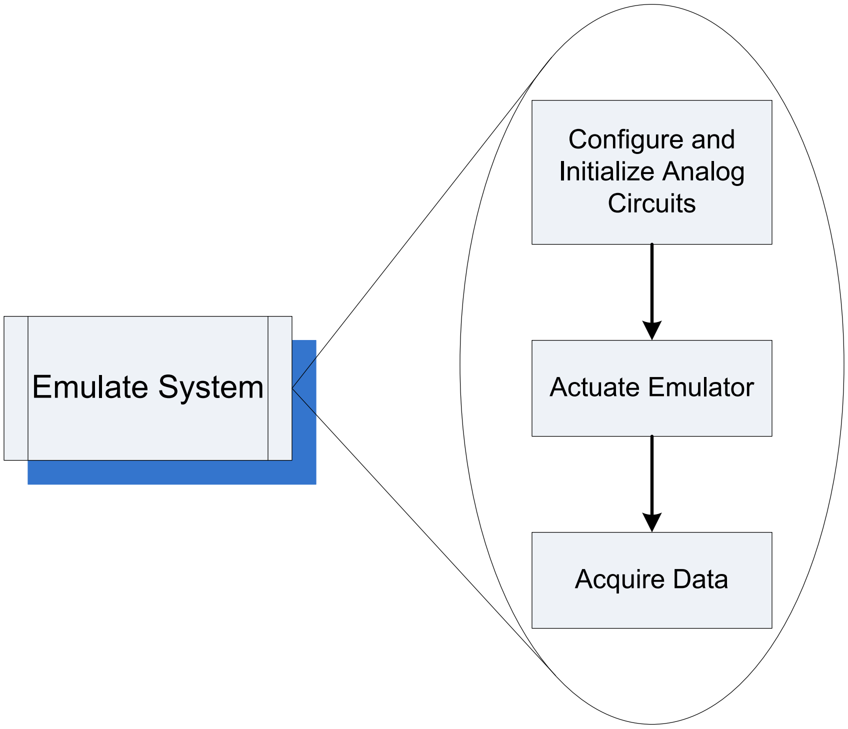


Figure 13: Emulation Steps

For an online application, such as power system security assessment the computation time, or emulation time, of the analog emulator, t_{emul}, should be able to be comparable if not faster than the time required for an equivalent digital technique. If this is not the case there is not much merit in implementing an analog system. The next section provides an overview of the proposed analog emulation approach to power system security assessment and highlights requirements for viability as an online tool.

3.2 ANALOG METHOD FOR SECURITY ASSESSMENT

The digital method for power system security assessment consists of building a network model and conducting contingency analysis as shown in Figure 4. A similar process for analog power system security assessment is shown in Figure 14. This process consists of emulating the power system based on telemetry, knowledge of the system and contingency/stability analysis.

The process of system emulation in steady-state produces a similar result to the network builder but is performed in a different manner. The network builder consists of a topology estimator and a state estimator. The network builder also handles bad data detection. The steady-state system emulation process configures and runs the emulator such that it is operating in the same fashion as the real power system based on the scan of system measurements. In order to accurately emulate the system in steady-state the requirements of theorems 1, 2 and 4 must be satisfied. The measurements should be time-stamped so they may be synchronized. When the system emulation is complete it essentially represents the operating point of the power system at the time when the system telemetry was acquired. This operating point is then used as initial conditions for contingency and stability analysis. This process is run via dynamic system emulation.

Similar to state estimation, performing security assessment via an analog method is not deterministic. Once the system is declared computable the steady-state system emulation process determines the correct structure of the power system, identifies and eliminates bad data, and configures the emulator based on the statistical properties of the measurements. The correct functional description of the system and inputs to the emulator are determined by quantifying the probability that the emulation state is correct based on the available information. Different inputs and/or topologies can be examined and correctness quantified through probability theory. Correct steady-state system emulation is defined as the configuration with the highest probability of being correct.

Contingencies to be emulated dynamically are defined beforehand and run once the system is emulated in the steady-state.

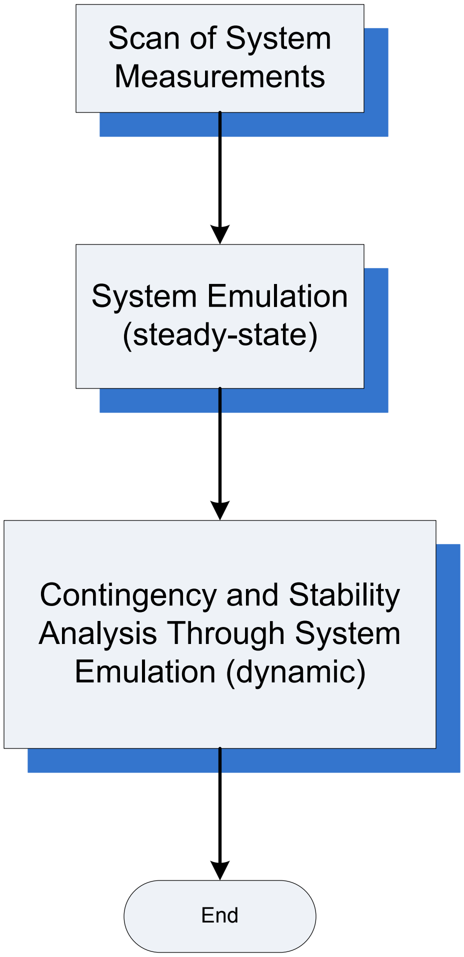

Scan of System Measurements
System Emulation (steady-state)
Contingency and Stability Analysis Through System Emulation (dynamic)
End

Figure 14: Analog Power System Security Assessment

In order to accurately emulate the system dynamics the requirements of theorems 1, 3 and 4 must be satisfied. The contingency and stability analysis is performed on the emulator by perturbing or making changes to the system. Lines, generators and loads can be removed to represent the loss of a component. The emulator will respond in a similar manner as the system being studied. Results are obtained by simply observing the behavior of the emulator. Information concerning stability and limit violations can be extracted through measurements from the emulator. In addition, due to the fact that system dynamics are represented in the emulator, transient stability analysis is performed on the selected contingencies. Analysis of faults and the response of the system can also be investigated. In addition, through various perturbations and monitoring the stability of the emulator the boundaries of stability for the system can be found for a given operating point. This method has some distinctive advantages over the traditional digital approach.

The advantages of this analog approach include very fast contingency/stability analysis through emulation. The emulator is modeled in the time domain hence the output is equivalent to a full time domain simulation. Through the application of time scaling the dynamics of the system are emulated much faster than real time. This enables the analog approach to run large sets of contingencies very quickly. In addition, transient stability is determined for each contingency. The approach also does not exhibit numerical instability.

The emulator will always converge to a solution and emulate the system so long as it can be emulated. Even if a non-computable or non-emulatable system is emulated a result will still be found, albeit incorrect. Evaluating if a system is emulatable will ensure that the solution the emulator is providing is indeed correct. If a system is not emulatable a subsystem may exist that is emulatable. This is in contrast to the digital approach which exhibits convergence issues and can fail to estimate states in the event that observability is not maintained. These advantages exhibit an improvement over the traditional approaches. However, there are also limitations to this proposed technique.

One particular limitation is the requirement of measurements. Results cannot be obtained unless they are measured or observed from the emulator. The measurement process increases computation time. In addition, measurement techniques inherently affect the system and will thus introduce some error into the results. Noise and other parasitic effects also contribute to errors. Due to these limitations the analog method will not have a comparable precision to digital techniques. However, by incorporating better models, at no cost to computation time, a more accurate, albeit not as precise as digital methods, representation of the system can be achieved through analog emulation. As a result, more accurate solutions can be obtained from this method. With these limitations in mind requirements for an analog emulator for the purpose of security assessment are defined.

3.3 REQUIREMENTS FOR ANALOG SECURITY ASSESSMENT

The aforementioned lemmas and theorems provided insight into analog computability and system emulation with analog computers. The theorems were generalized for applicability to a nonspecific analog computer. The proposed process of power system security assessment through analog computation was then developed from the theorems. Based on this proposed method for security assessment and practical implications of an online tool, the requirements for an analog emulator are enumerated below:

1. A detailed power system model
2. Emulation theory and methodology
3. A fast and accurate power system emulator

For an analog method to be viable the power system model and emulation methodology should be at least as detailed as current digital methods. In addition, the computation time should be comparable or faster than digital methods. The results should also exhibit similar, if not better, accuracy than current methods. The following chapter provides details on the power system emulator.

4 ANALOG POWER SYSTEM EMULATOR

This chapter provides detailed information on the power system emulator design and operation. More specifically, the focus is placed on the modeling of a power system in analog form and the methodology of analog computation. These items addresses the functional description requirement for system emulation in theorem 1 and functional relationship, or mapping, between the emulator and the power system outlined in theorem 4. Chapter five covers the additional requirements necessary for power system security assessment. First an overview of the emulator structure and functionality is provided. This is followed by details on the emulation methodology and power system models. Next the associated hardware, scaling and software of the emulator are presented.

4.1 POWER SYSTEM EMULATOR

The power system emulator consists of both analog and digital components. A diagram of the emulator is shown in Figure 15. The emulation is conducted via analog hardware and a digital computer interfaces with the analog hardware. The digital computer is used primarily for data acquisition and control of the emulation hardware.

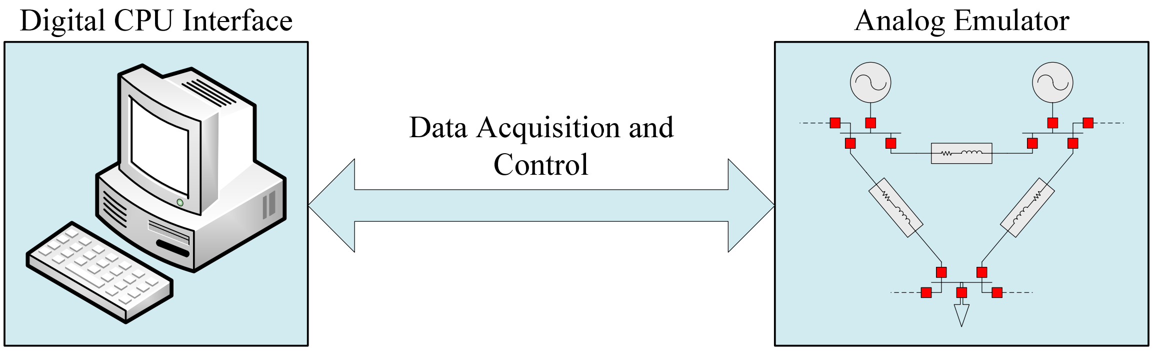


Figure 15: Power System Emulator Diagram

The control of the emulator consists of two main stages: configuration, reconfiguration and actuation. The emulator parameters are first configured, or reconfigured if changes are required for subsequent computation, and then when all parameters have been set the computation is actuated. During actuation the integrators are turned on and the response of the emulator provides the solution. For a given system the configuration is only required once and henceforth multiple computations can be conducted with minimal reconfiguration of the system. For example, the line parameters once set will not need to be changed every time a power flow case is run. Line or generator outages can be emulated by simply turning off the specified line(s) or generator(s) and leaving the rest of the system alone.

The control of the analog hardware is handled via a digital computer. An illustration showing the control method and interaction between the digital and analog hardware is shown in Figure 16. It is shown that the digital computer feeds data into an analog-to-digital (D/A) converter, which is then routed into a de-multiplexer (DEMUX) to the analog components of the emulator for configuration. For a single D/A converter and DEMUX combination, this is a serial process. The computer provides a single signal to configure a device and the DEMUX is controlled directly by the computer to select which analog device to configure. The DEMUX latches the outputs to maintain the proper configuration as it cycles through the devices. Multiple D/A converters and de-multiplexers can be implemented in parallel to speed up this process. The actuation of the analog hardware is accomplished through a digital signal that turns on the integrators. In summary there are three sets of digital signals. The digital signals feeding into the D/A converter specify parameters and values for the analog hardware. The digital

DEMUX control specifies where the current analog control signal is to be routed. The digital control of integrators goes directly to the analog emulator to turn integrators on, off, and sets initial conditions. The system has the capability of individually actuating each component if required. The data acquisition is also handled via a digital computer.

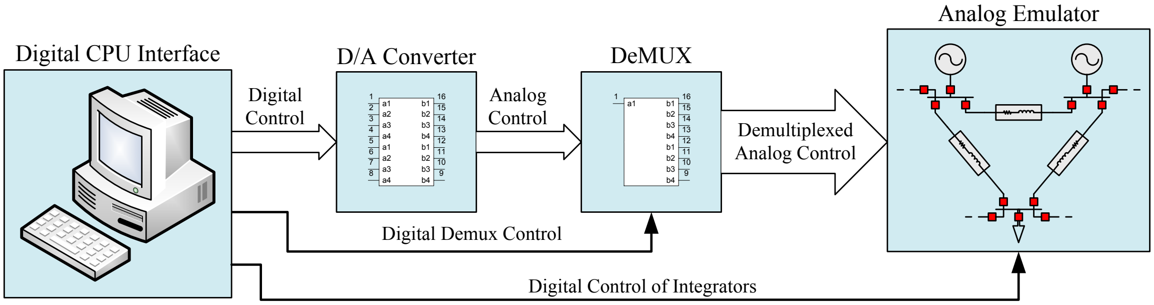


Figure 16: Emulator Control

The data acquisition scheme is shown in Figure 17. The analog data acquisition hardware provides conditioned signals from the analog emulation hardware for measurement via the digital computer. The conditioned signals are routed through an analog multiplexer before the analog-to-digital (A/D) conversion takes place. This process can be sped up via incorporating parallel combinations of D/A converters and multiplexers. Most of the time required for computation is spent acquiring data. This could potentially create a bottleneck on computation time for large systems.

It has been shown that as system size increases the emulation time remains the same [37]. No discernable increase in emulation time is exhibited. However, both the data acquisition and configuration time will increase linearly with system size. This increase in time can be mitigated though additional data acquisition hardware. For example, assuming sufficient memory bandwidth, doubling the number of A/D converters, and subsequently operating them in parallel, will cut acquisition time in half. Another method for saving time is to only acquire data that is necessary for each computation. For some analyses very little data is actually required. For example, when conducting contingency analysis a digital flag can be used in hardware to indicate a system violation (e.g. over current, under voltage, etc.). Data acquisition is then conducted only when this digital flag indicates a violation; otherwise the system is operating within predefined limits.

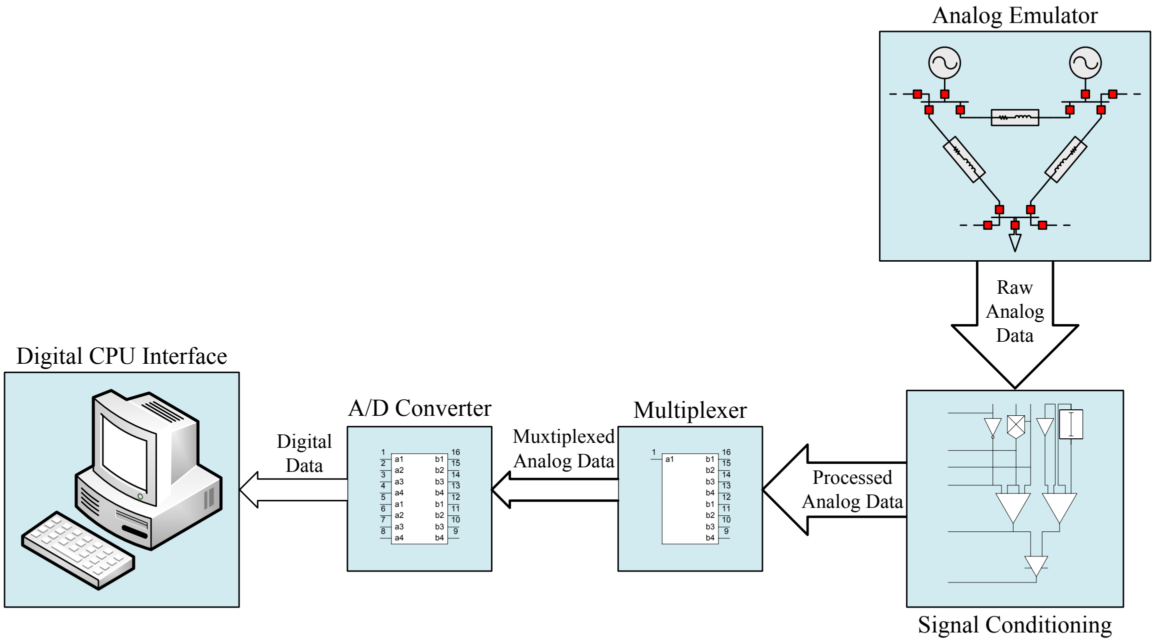


Figure 17: Emulator Data Acquisition

4.2 EMULATION METHODOLOGY AND MODELING

There are numerous different approaches to modeling and emulating a power system. Historically, the behavior of power systems was emulated using AC techniques. For example, transient network analyzers built the AC power system on a small scale and operated the miniaturized model in the same fashion as the real power system. In this work a DC emulation approach is utilized.

4.2.1 DC EMULATION

Power system computation in many digital applications is conducted in polar coordinates. The power system states are represented by a magnitude and angle. In the analog DC emulation technique used in this work, the computation in the network is performed exclusively in rectangular (Cartesian) coordinates. All power system parameters and values are represented in rectangular and/or converted from polar form to rectangular form when necessary for application in the emulator. Figure 18 is a comparison of polar and rectangular representation of a vector $\mathbf{V}$ on a complex plane.

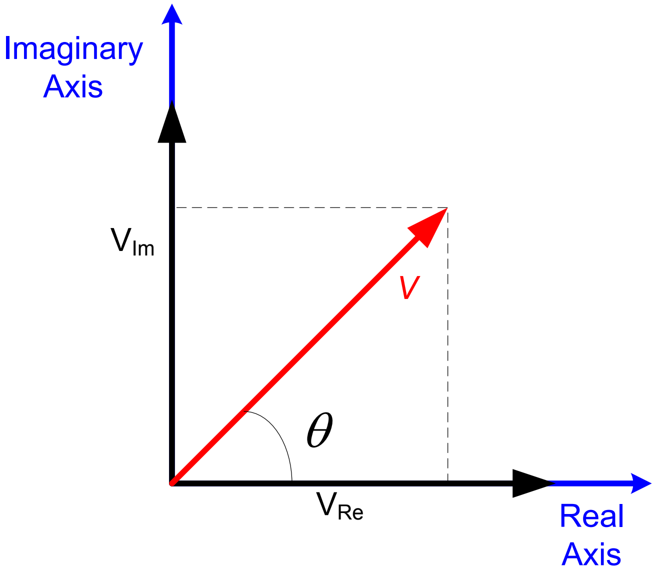


Figure 18: Polar and Rectangular Coordinate Comparison

The polar form representation contains two components, a vector magnitude and phase. It can be represented in the following manner:

$$\mathbf{V} = |V| \angle \theta \tag{4.1}$$

where

$\mathbf{V} \triangleq$ complex voltage

$|V| \triangleq$ magnitude of the complex voltage $\mathbf{V}$

$\theta \triangleq$ phase of the complex voltage $\mathbf{V}$

The Cartesian coordinate representation consists of two magnitudes. One is purely real and lies on the real axis and the other is purely imaginary and lies on the imaginary axis. This representation is related to the magnitude and phase by equation (4.2) where V_{Re} and V_{Im} are the real and imaginary vector components respectively.

$$\mathbf{V} = V_{\text{Re}} + jV_{\text{Im}} = |V|\cos(\theta) + j|V|\sin(\theta) \tag{4.2}$$

The rectangular form can easily be transformed into polar form by equation (4.3). Note that the sign of the quotient of V_{Im} and V_{Re} dictates what quadrant θ lies.

$$\begin{aligned} |V| &= \sqrt{V_{\text{Re}}^2 + V_{\text{Im}}^2} \\ \theta &= \tan^{-1}\left(\frac{V_{\text{Im}}}{V_{\text{Re}}}\right) \end{aligned} \tag{4.3}$$

The specifics of the previously proposed DC emulation method were first introduced in [38] and highlighted and expanded upon here. The method roots itself in solving the network matrix equation in rectangular coordinates. This equation relates the current flowing through a network of impedances to a voltage applied to the network:

$$[I]=[Y]\cdot[V] \tag{4.4}$$

The admittance matrix, $[Y]$, is a nodal admittance matrix based on the power system topology and impedances of the power system network. Solving equation (4.4) in rectangular coordinates with a complex admittance and a complex voltage yields:

$$\begin{aligned} Y\cdot V &= I_{\mathrm{Re}}+jI_{\mathrm{Im}}=\left(Y_{\mathrm{Re}}+jY_{\mathrm{Im}}\right)\cdot\left(V_{\mathrm{Re}}+jV_{\mathrm{Im}}\right)\\ &= Y_{\mathrm{Re}}V_{\mathrm{Re}}+jY_{\mathrm{Re}}V_{\mathrm{Im}}+jY_{\mathrm{Im}}V_{\mathrm{Re}}-Y_{\mathrm{Im}}V_{\mathrm{Im}}\\ &= \left(Y_{\mathrm{Re}}V_{\mathrm{Re}}-Y_{\mathrm{Im}}V_{\mathrm{Im}}\right)\quad \{\text{real current}\}\\ &\quad +j\left(Y_{\mathrm{Im}}V_{\mathrm{Re}}+Y_{\mathrm{Re}}V_{\mathrm{Im}}\right)\quad \{\text{imaginary current}\} \end{aligned} \tag{4.5}$$

The real and imaginary components in equation (4.5) are labeled with subscripts Re and Im respectively. For this case, considering complex network impedances, there are a total of four current components. Each current component is computed by multiplying an admittance magnitude by a voltage magnitude. This calculation is identical to the resultant current flow based on a voltage drop across a resistor. This is how DC emulation is conducted. Resistive networks represent the admittances and DC voltages are applied to the resistive networks to induce current flow. Utilizing four DC networks, one for each of the components in equation (4.5), the network equation can be solved. The solution is specifically the voltages and currents flowing in these DC networks. This information needs to be extracted, or measured, from the analog circuits. The four networks are defined as follows:

$$\begin{aligned} I_{\mathrm{Re}} + jI_{\mathrm{Im}} = & \; Y_{\mathrm{Re}}V_{\mathrm{Re}} && \text{network 1} \\ & - Y_{\mathrm{Im}}V_{\mathrm{Im}} && \text{network 2} \\ & + jY_{\mathrm{Im}}V_{\mathrm{Re}} && \text{network 3} \\ & + jY_{\mathrm{Re}}V_{\mathrm{Im}} && \text{network 4} \end{aligned} \tag{4.6}$$

These four emulation networks and their associated current components are depicted graphically in Figure 19 as four DC resistive networks.

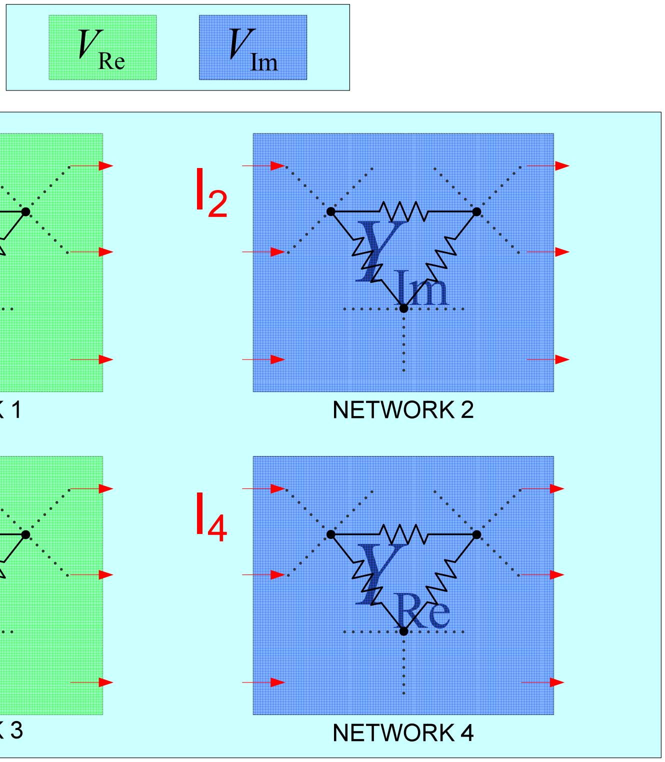


Figure 19: DC Emulation Networks

From a circuit viewpoint all the nodal voltages can be measured directly in rectangular coordinates, one imaginary voltage magnitude and one real voltage magnitude. Obtaining the rectangular current magnitudes is not as straight forward. Four currents must be measured and added together to obtain the branch current flow or injections in rectangular coordinates. Specifically the summation of currents in networks one and two equal the real current value and the summation of currents in networks three and four equate to the imaginary current component. More generally for any size system the current at a node i, such as a generator injection into the network, can be computed by:

$$\begin{aligned} I_{Gi} &= \sum_{j=1}^{n+1} \operatorname{Re}\left\{Y_{ij}\right\} \cdot \operatorname{Re}\left\{V_j\right\} \quad \text{network 1} \\ &- \sum_{j=1}^{n+1} \operatorname{Im}\left\{Y_{ij}\right\} \cdot \operatorname{Im}\left\{V_j\right\} \quad \text{network 2} \\ &+ j\sum_{j=1}^{n+1} \operatorname{Im}\left\{Y_{ij}\right\} \cdot \operatorname{Re}\left\{V_j\right\} \quad \text{network 3} \\ &+ j\sum_{j=1}^{n+1} \operatorname{Re}\left\{Y_{ij}\right\} \cdot \operatorname{Im}\left\{V_j\right\} \quad \text{network 4} \end{aligned} \tag{4.7}$$

where $\operatorname{Re}\left\{Y_{ij}\right\}$ and $\operatorname{Im}\left\{Y_{ij}\right\}$ are the real and imaginary network admittances between nodes i and j, and $\operatorname{Re}\left\{V_j\right\}$ and $\operatorname{Im}\left\{V_j\right\}$ represent the real and imaginary voltage magnitudes at bus j respectively. The formulation in equation (4.7) is for an n bus system with $(n+1)$ nodes with the inclusion of ground as a node. The key to implementing this emulation technique is to develop accurate representation of the power system components to operate in the DC networks. The next section delves into the details of the power system model used in DC emulation.

4.2.2 POWER SYSTEM MODEL

A component based modeling approach was taken for the power system emulator. This model comprises of an interconnection of generators, transmission lines, transformers and loads. An example of such an interconnection is shown in Figure 20. The system is modeled in per unit utilizing per phase analysis. This framework assumes balanced system operation. Mathematically speaking the power system is modeled as a system of algebraically constrained ordinary differential equations (ODEs):

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{f}\left(\mathbf{x}(t),\mathbf{u}\right) \\ \mathbf{g}\left(\mathbf{x}(t),\mathbf{u}\right) &= 0 \end{aligned} \tag{4.8}$$

where

$\mathbf{x} \triangleq$ set of the state variables of the system

$\mathbf{u} \triangleq$ set of system parameters and inputs

$\mathbf{f} \triangleq$ set of ordinary differential equations

$\mathbf{g} \triangleq$ set of algebraic constraints

The power system network is represented as a set of algebraic constraints. This network, consisting of lines and transformers, is modeled with impedances. Electromagnetic transients are not incorporated into this model. The power injections, generators and loads, into the network are modeled dynamically. They are represented by a set of nonlinear ODEs. More specifically, a state space averaging technique is used to model the dynamics of the system.

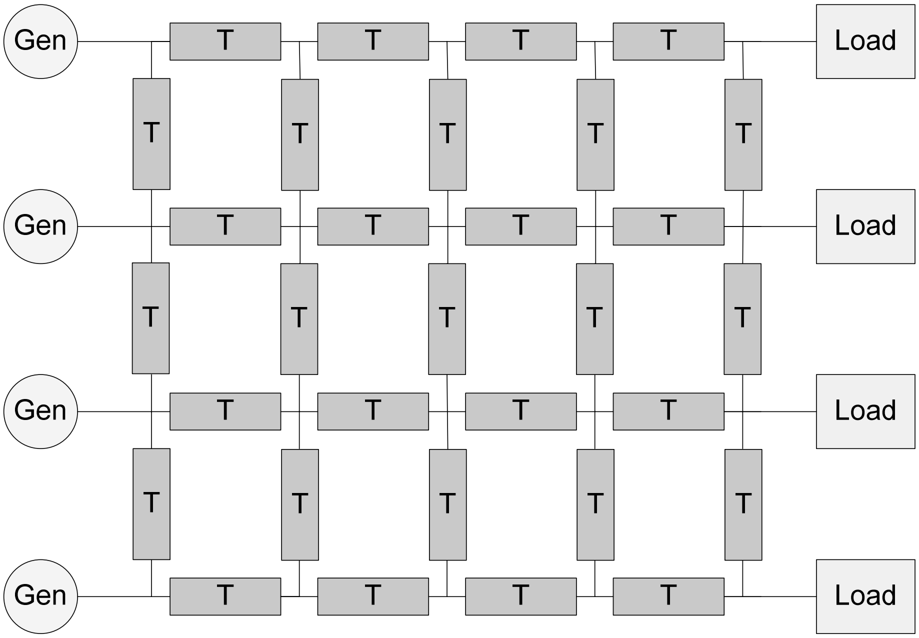


Figure 20: Power System Emulation Network

There has been extensive development of state space averaging, or dynamic phasor, techniques in power system analysis [39-41]. The method has been applied primarily to machines and power electronic converters. In the application here it is used to model the dynamics of generation and load. “The generalized averaging method is based on the fact that the waveform $x(\bullet)$ can be approximated on the interval $(t-T,t]$ to arbitrary accuracy with a Fourier series representation of the form [39]:”

$$x\left(t-T+s\right)=\sum_{k}\left\langle x\right\rangle_{k}\left(t\right)e^{jk\omega_{s}\left(t-T+s\right)} \tag{4.9}$$

where the summation is performed over all integers k, $\omega_s = \frac{2\pi}{T}$, $s \in \left(0,T\right]$, and $\left\langle x\right\rangle_{k}\left(t\right)$ are the complex Fourier coefficients of $x\left(\bullet\right)$. Each Fourier coefficient can be defined by [39]:

$$\left\langle x\right\rangle_{k}\left(t\right)=\frac{1}{T}\int_{0}^{T}x\left(t-T+s\right)e^{-jk\omega_{s}\left(t-T+s\right)}ds \tag{4.10}$$

Differentiating equation (4.10) with respect to time yields [39]:

$$\frac{d}{dt}\left\langle x\right\rangle_{k}\left(t\right)=\left\langle\frac{d}{dt}x\right\rangle_{k}\left(t\right)-jk\omega_{s}\left\langle x\right\rangle_{k}\left(t\right) \tag{4.11}$$

The ordinary differential equations which model the load and generator dynamics in this work are based on phasor dynamics of the form in equation (4.11). This expression is an approximation and assumes that ω_s is time invariant. It has been shown that this approximation also holds for slowly varying ω_s [39]. In this work it is assumed that the frequency is dominated by the fundamental component (60 Hz) and that this frequency is maintained fairly constant. These assumptions allow for using only one Fourier component, and thus one differential equation, for each state variable.

The generator is modeled as a constant voltage source, E_G, behind internal impedance, Z_G. This is sometimes referred to as the classical generator model shown in Figure 21 [42]. For the application in DC emulation the generator maintains a PV bus behavior in steady-state. The mechanical power input, P_m, and the generator terminal voltage, V, are specified as inputs. The dynamics of the generators are modeled via the swing equation.

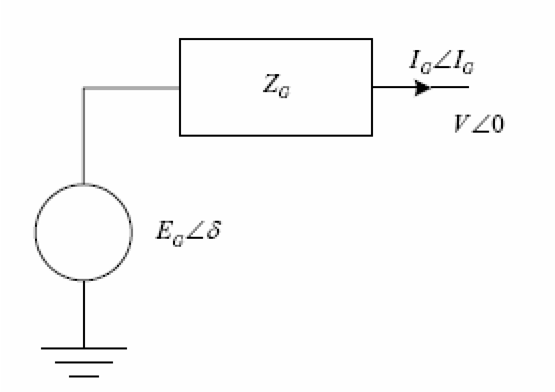


Figure 21: Classical Generator Model

The swing equation quantifies swings in the power angle δ during a transient:

$$M\ddot{\delta}+D\dot{\delta}+P_e(\delta)=P_m \tag{4.12}$$

where

$M \triangleq$ generator inertia coefficient

$D \triangleq$ damping coefficient of the generator

$P_e(\delta) \triangleq$ electrical real power output of the generator

$P_m \triangleq$ mechanical input power from the prime mover

A transient occurs when there is a difference between electrical power output and mechanical power input to the machine. In steady-state $\left(\ddot{\delta} = \dot{\delta} = 0\right)$ the electrical power output is equal to the specified mechanical input power. If damping is neglected solving equation (4.12) for the power angle results in the double integral shown in equation (4.13):

$$\delta = \frac{1}{M}\int\int\left(P_m - P_e\left(\delta\right)\right)dtdt \tag{4.13}$$

With the solution of the power angle and a specified generator voltage magnitude the voltages applied to the DC emulation networks is determined in a similar manner as equation (4.2):

$$\begin{aligned} V_{\mathrm{Re}} &= \left|V\right|\cos\left(\delta\right) \\ V_{\mathrm{Im}} &= \left|V\right|\sin\left(\delta\right) \end{aligned} \tag{4.14}$$

The load is represented in a similar fashion as the generators.

The load dynamic behavior is described by a decoupled exponential recovery model based on the operation of induction motors [43, 44]. Within this model, bus voltage magnitude and angle are expressed as functions of complex power flow, complex power injection, and time:

$$\begin{aligned}\frac{d|V|}{dt} &= -\frac{1}{K_Q}\left(Q_L - Q_e\left(|V|,\theta\right)\right)\\ \frac{d\theta}{dt} &= -\frac{1}{K_P}\left(P_L - P_e\left(|V|,\theta\right)\right)\end{aligned} \tag{4.15}$$

where

$|V| \triangleq$ load voltage magnitude

$|\theta| \triangleq$ load phase angle

$Q_L \triangleq$ specified load reactive power

$Q_e\left(|V|,\theta\right) \triangleq$ reactive power injection into network

$K_Q \triangleq$ voltage magnitude time constant

$P_L \triangleq$ specified load real power

$P_e\left(|V|,\theta\right) \triangleq$real power injection into network

$K_P \triangleq$ phase angle time constant

For the aggregate load model, however, injection may be dependent on several factors including the current injection or load impedance at a given operating point. The electrical power injection, S_e, into a bus *i* as defined by the popular ZIP model, is shown in [45]:

$$S_e = P_e + jQ_e = S_i + V_i\left(I_i\right)^* - \left|V_i\right|^2\left(Y_i\right)^* \tag{4.16}$$

where

$S_i \triangleq$ load power injection at bus i

$I_i \triangleq$ load current injection at bus i

$Y_i \triangleq$ load impedance at bus i

The power system network model consists of an interconnection of transformers and transmission lines represented by complex impedances. The transmission line portrayal is based on the pi equivalent model shown in Figure 22. In order to translate this model into the DC emulation scheme the line parameters are separated into real and imaginary components. This yields the resistor values for the DC emulation networks. The series resistive elements are determined by:

$$\begin{aligned} R_{\mathrm{Re}(ij)} &= \frac{1}{\mathrm{Re}\left\{Y_{ij}\right\}} = \frac{R_{ij}^2 + X_{Lij}^2}{R_{ij}} \\ R_{\mathrm{Im}(ij)} &= \frac{1}{\mathrm{Im}\left\{Y_{ij}\right\}} = \frac{R_{ij}^2 + X_{Lij}^2}{X_{Lij}} \end{aligned} \tag{4.17}$$

where

$Y_{ij} \triangleq$ transmission line series admittance

$R_{ij} \triangleq$ transmission line series resistance

$X_{Lij} \triangleq$ transmission line series reactance

The shunt resistive elements are determined by:

$$
\begin{aligned}
R_{\mathrm{Re}(ik)} &= R_{\mathrm{Re}(jk)} = \frac{1}{\mathrm{Re}\left\{Y_{jk,ik}\right\}} = r_{jk} \\
R_{\mathrm{Im}(ik)} &= R_{\mathrm{Im}(jk)} = \frac{1}{\mathrm{Im}\left\{Y_{jk,ik}\right\}} = \frac{-1}{\omega C_{jk}} = -X_{C_{jk}}
\end{aligned}
\tag{4.18}
$$

where

$Y_{jk,ik} \triangleq$ transmission line shunt admittance

$r_{jk} \triangleq$ transmission line shunt resistance

$X_{C_{jk}} \triangleq$ transmission line shunt reactance

The emulation networks can be constructed based on the line parameters and equations (4.17) and (4.18). The topology of each DC network will mimic the topology of the power system. For example, for the pi model shown here the analogous section DC emulation network will have a pi form. For a network of many transmission lines the required resistance values and network topology are developed in the same fashion. Simplified impedance based line models are incorporated following the same approach.

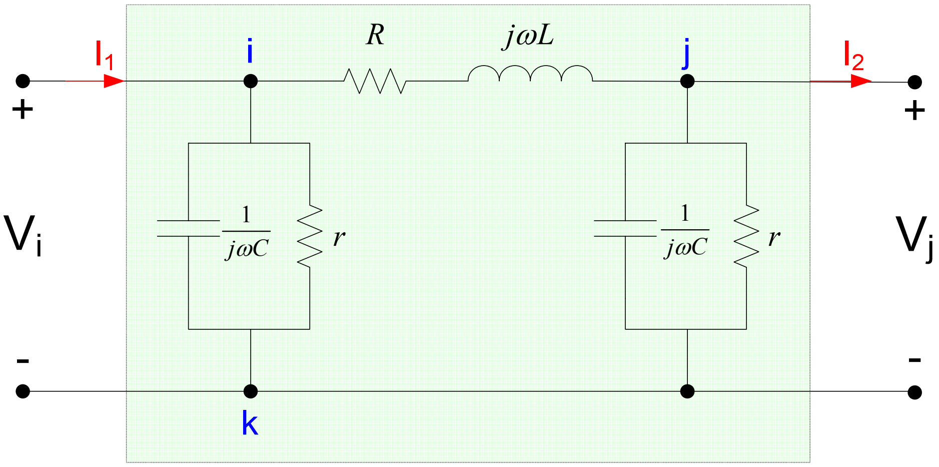


Figure 22: Pi Equivalent Transmission Line Model

There are two types of transformers modeled for the emulator. Tap changing and non tap changing. The tap changing transformer model is shown in Figure 23. It consists of an ideal transformer with a turns ratio of t and a series impedance $R + jX$. Developing equations for the voltages and currents in the circuit yields the following [46]:

$$\begin{bmatrix} I_i \\ I_j \end{bmatrix} = \begin{bmatrix} |t|^2 Y & -t^* Y \\ -tY & Y \end{bmatrix} \begin{bmatrix} V_i \\ V_j \end{bmatrix} \tag{4.19}$$

A pi equivalent circuit can be developed for this transformer from (4.19) so long as the tap setting t does not have a phase shift. If a phase shift is present the off diagonal entries become unequal and an equivalent circuit will no longer be realizable. The pi equivalent model of the transformer is shown in Figure 24. For a transformer without a tap changer (t=1 in a per unit normalized system), the shunt element are removed and the equivalent model is simply a series impedance.

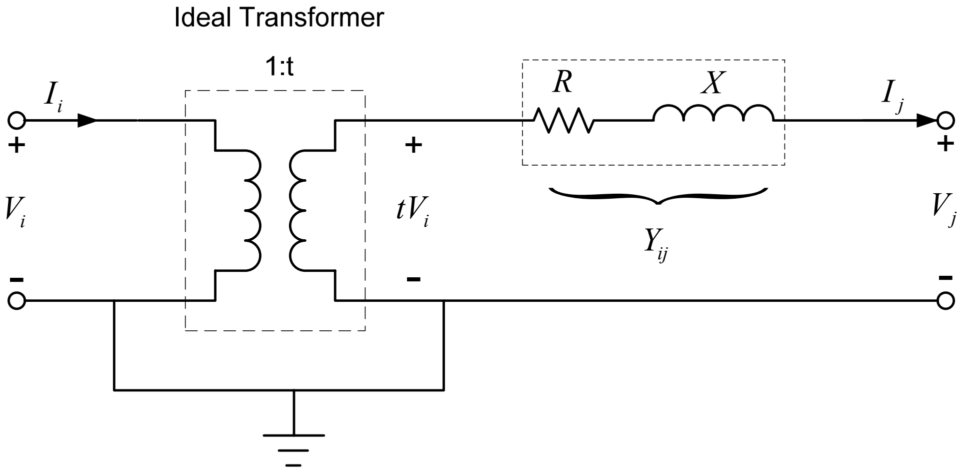


Figure 23: Tap Changing Transformer Model

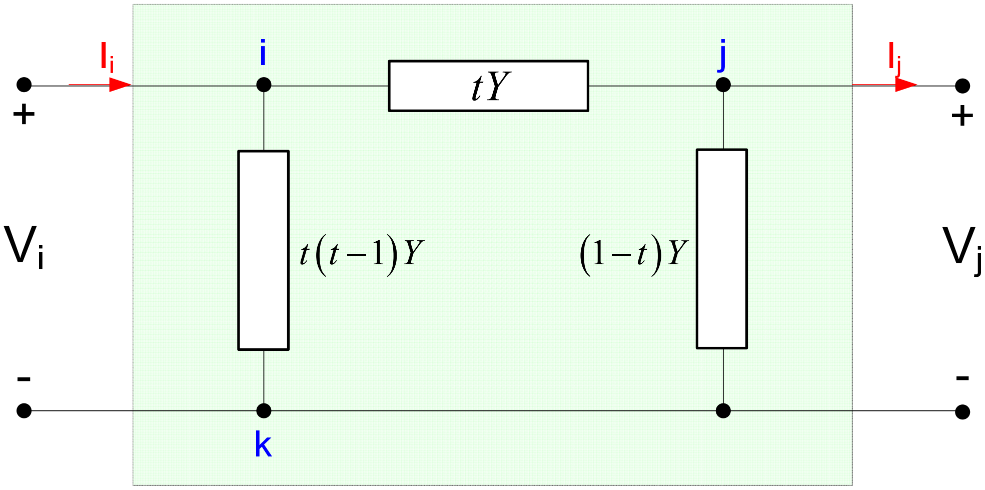


Figure 24: Pi Equivalent Tap Changing Transformer Model

The resistor values for the DC emulation networks can be determined by the following equations for the tap changing transformer:

$$\begin{aligned} R_{\mathrm{Re}(ij)} &= \frac{1}{\mathrm{Re}\left\{tY_{ij}\right\}} = \frac{1}{t}\left(\frac{R_{ij}^2 + X_{Lij}^2}{R_{ij}}\right) \\ R_{\mathrm{Im}(ij)} &= \frac{1}{\mathrm{Im}\left\{tY_{ij}\right\}} = \frac{1}{t}\left(\frac{R_{ij}^2 + X_{Lij}^2}{X_{Lij}}\right) \end{aligned} \tag{4.20}$$

$$\begin{aligned} R_{\mathrm{Re}(ik)} &= \frac{1}{\mathrm{Re}\left\{t\left(t-1\right)Y_{ik}\right\}} = \frac{1}{t\left(t-1\right)}\left(\frac{R_{ij}^2 + X_{Lij}^2}{R_{ij}}\right) \\ R_{\mathrm{Im}(ik)} &= \frac{1}{\mathrm{Im}\left\{t\left(t-1\right)Y_{ik}\right\}} = \frac{1}{t\left(t-1\right)}\left(\frac{R_{ij}^2 + X_{Lij}^2}{X_{Lij}}\right) \end{aligned} \tag{4.21}$$

$$\begin{aligned} R_{\mathrm{Re}(jk)} &= \frac{1}{\mathrm{Re}\left\{\left(1-t\right)Y_{ik}\right\}} = \frac{1}{\left(1-t\right)}\left(\frac{R_{ij}^2 + X_{Lij}^2}{R_{ij}}\right) \\ R_{\mathrm{Im}(jk)} &= \frac{1}{\mathrm{Im}\left\{\left(1-t\right)Y_{ik}\right\}} = \frac{1}{\left(1-t\right)}\left(\frac{R_{ij}^2 + X_{Lij}^2}{X_{Lij}}\right) \end{aligned} \tag{4.22}$$

The network components in this emulation scheme are purely resistive and the sizing of the resistor values is dependant upon operating frequency. By modeling the emulation networks with fixed resistances the operational frequency of the power system is assumed to be constant. With the automatic generation control systems implemented today this is a reasonable assumption. The variance in operating frequency is quite minimal. Faults and circuit breakers are also modeled within this framework.

Any balanced fault can easily be translated into the emulation approach so long as it is modeled with impedances. A similar derivation as previously shown will allow for determination of appropriate resistance values for the DC emulation networks. Circuit breakers are modeled as ideal switches. They are either on or off. This behavior of the circuit breakers is handled directly via the hardware realization of the power system network. No additional components or switches are required in the emulation networks.

4.3 ANALOG HARDWARE

The analog hardware was designed to accurately represent the power system based on the aforementioned models and also to allow for remote control and configuration. The control of the hardware was achieved through the use of operational transconductance amplifiers (OTAs). The OTA is the fundamental building block of the power system emulator.

The OTA is classified as an operational amplifier although it differs from the traditional operational amplifier, or op-amp. Usually when referring to an op-amp it is with regards to a voltage controlled voltage source (VCVS). Essentially this is a voltage amplifier. The input and the outputs are both voltages and ideally the open-loop gain is infinite. An OTA in contrast is a voltage controlled current source (VCCS). The input is a voltage and the output is a current. The transfer function is dependant upon the OTAs transconductance gain $\left(g_m\right)$ which is finite and controllable via an external bias current $\left(i_{abc}\right)$. This bias current is the key element which allows for reconfiguration and remote control of the emulator.

A diagram of an ideal OTA is shown in Figure 25. The amplifier has a differential voltage input v_{in} and a current output i_o proportional to the device transconductance gain.

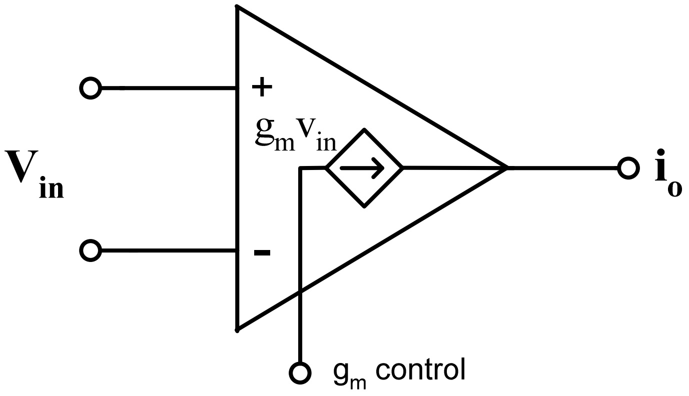


Figure 25: Ideal OTA

For an ideal OTA the output current is a linear function of the input voltage and transconductance gain:

$$i_o = g_m v_{in} \tag{4.23}$$

While the transconductance gain is a function of a biasing current i_{abc}:

$$g_m = f\left(i_{abc}\right) \tag{4.24}$$

However, the basic circuit design of the OTA is highly nonlinear. The nonlinearity of the OTA and how it relates to analog computation has been dealt with in prior publications [42, 47, 48]. It has been shown that through proper scaling the OTA can operate in a linear fashion, albeit within a limited range. In addition, numerous circuit designs have developed highly linear OTAs [49-52]. However, these circuits were not implemented in this work as the hardware designs were restricted to commercially available parts.

A block diagram of the analog hardware for a generator is shown in Figure 26 [53]. The difference between the computed electrical power output of the generator and the specified mechanical power input is integrated to solve for the power angle and the appropriate voltages are applied to the DC emulation networks. The solution for the terminal voltage in this model is obtained in polar form and is then converted into rectangular components via sine and cosine shaper circuits in order to interface with the DC networks.

The analog hardware consists of reconfigurable OTA based integrators to compute the swing equation, reconfigurable voltage sources to specify P_m and $|E|$, analog adders, multipliers and current sensors to compute P_e as shown in equation (4.25). The hardware also incorporates voltage controlled current sources (VCCS), voltage controlled voltage sources (VCVS) and current controlled voltage sources (CCVS) to condition the signals as necessary. In addition, integration can be remotely controlled to on/off states and initial conditions can be set and applied to the integrators. Details on these circuits can be seen in [54].

$$
\begin{aligned}
\mathrm{Re}\{S\} &= \mathrm{Re}\{V \cdot I^*\} \\
P_e &= E_{\mathrm{Re}} \cdot I_{\mathrm{Re}} + E_{\mathrm{Im}} \cdot I_{\mathrm{Im}} \\
P_e &= |E| \cdot \cos\delta \cdot I_{\mathrm{Re}} + |E| \cdot \sin\delta \cdot I_{\mathrm{Im}}
\end{aligned}
\tag{4.25}
$$

The process of computation consists of initializing the integrators with initial conditions, applying voltages to the DC emulation networks and then turning on integration. Ground faults can be created at the generator terminal via the switch shown in the diagram. By opening the switch the electrical power in the feedback loop goes to zero simulating a ground fault at the generator terminal. The construction of the load circuit was conducted using similar components.

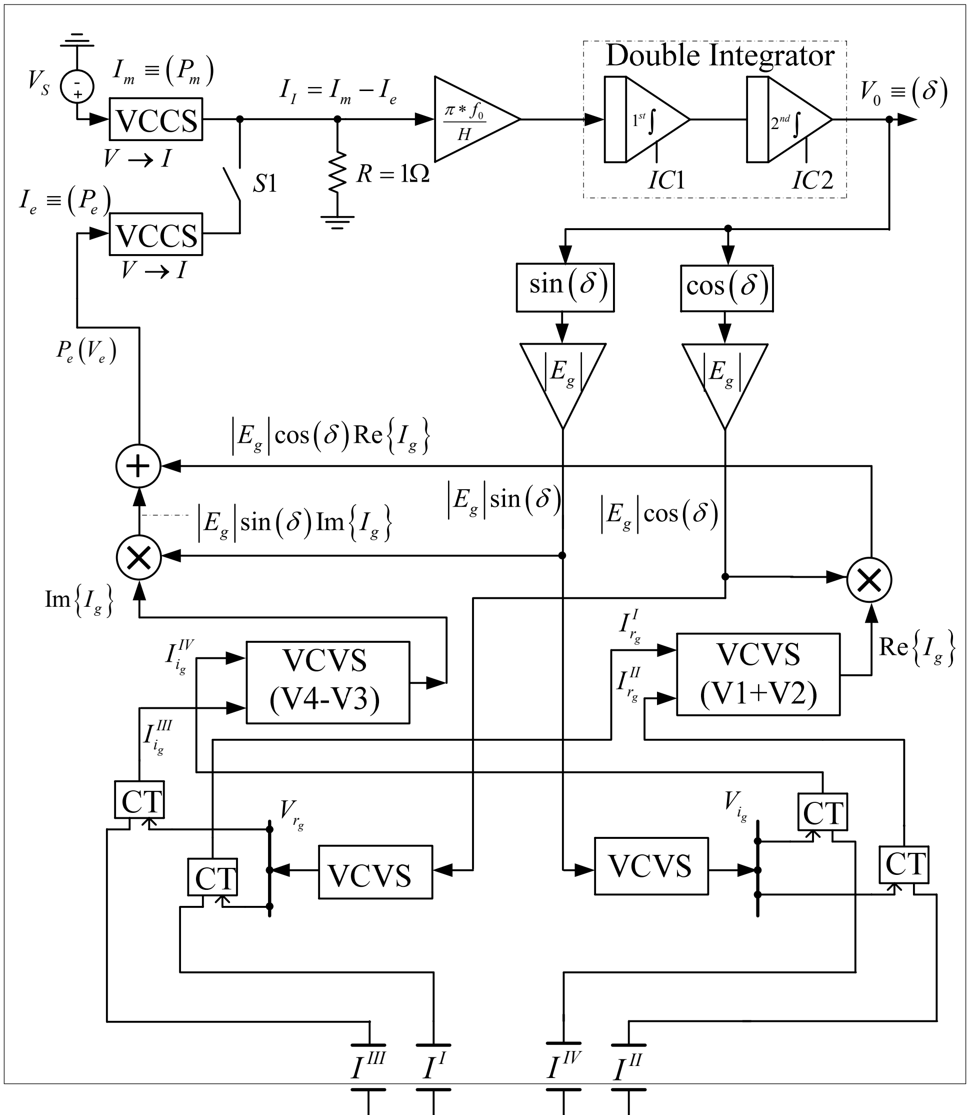


Figure 26: Analog Generator Module for DC Emulation

A block diagram of the load emulation hardware is shown in Figure 27. It is a compilation of four sub-circuits, of which the first is the network interface. The second sub-circuit utilizes the current flows and load bus voltage supplied by the interface to calculate the complex power flow leaving the load bus as dictated by:

$$\begin{aligned} S_i = V_i I_i^* = \left(V_{i\mathrm{Re}} + jV_{i\mathrm{Im}}\right)\left(I_{i\mathrm{Re}} - jI_{i\mathrm{Im}}\right) = \ldots \\ \ldots = \underbrace{\left(V_{i\mathrm{Re}} I_{i\mathrm{Re}} + V_{i\mathrm{Im}} I_{i\mathrm{Im}}\right)}_{P_i} + j\underbrace{\left(V_{i\mathrm{Im}} I_{i\mathrm{Re}} - V_{i\mathrm{Re}} jI_{i\mathrm{Im}}\right)}_{Q_i} \end{aligned} \qquad (4.26)$$

The third sub-circuit utilizes this power flow in conjunction with the user defined power injection to update the voltage at the load bus, through integration as defined in equation (4.15). The fourth sub-circuit takes this updated voltage and, using a set of cosine and sine shapers, converts it from a polar to a rectangular form, as required by the network interface.

The load hardware allows for the remote configuration of integration parameters and gains, as well as load parameters based on the ZIP model in equation (4.16). The load circuitry can also be turned on and off remotely. Initial conditions can be specified and integration can be controlled remotely. The hardware design for the power system network was different than the load and generator. The design consisted of a network of resistive elements.

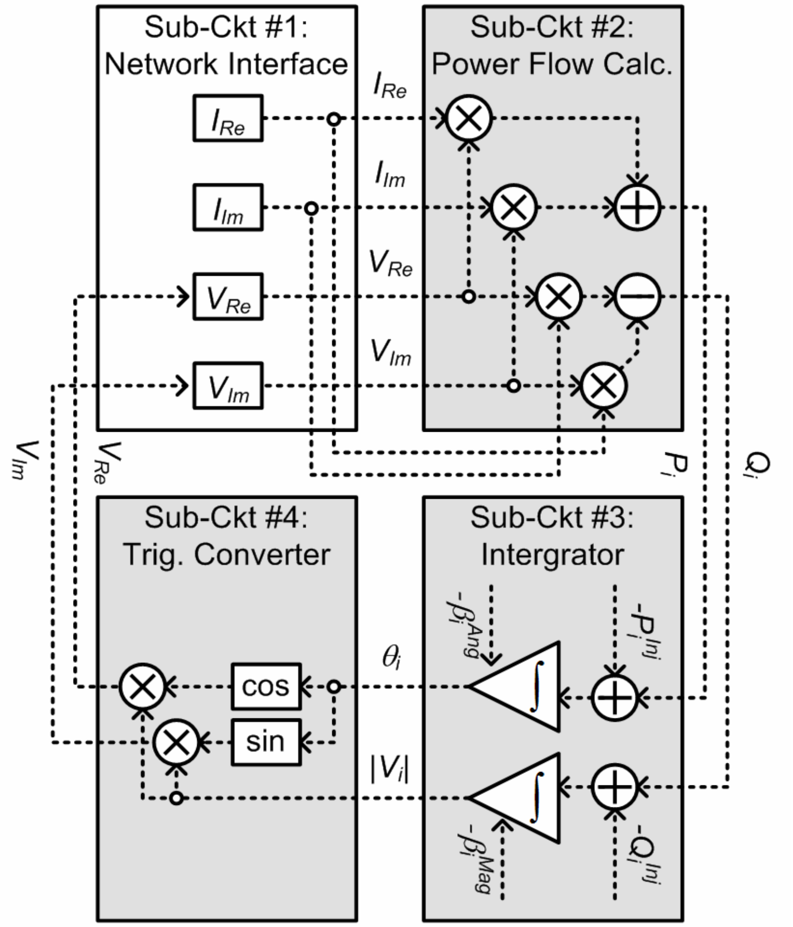


Figure 27: Analog Load Module for DC Emulation

In circuit form a network of resistors, or potentiometers, would require manual intervention to configure and alter the emulator for a given computation. There is also a requirement for negative resistance when modeling shunt capacitive elements of the transmission lines. A hardware design with active devices that achieves remote reconfigurability and negative resistance has been developed. The circuits are OTA-based reconfigurable variable positive and negative resistive circuits.

A double ended OTA variable resistor [55] is shown in Figure 28. This circuit behaves like a potentiometer. The controllable bias current is analogous to the wiper terminal.

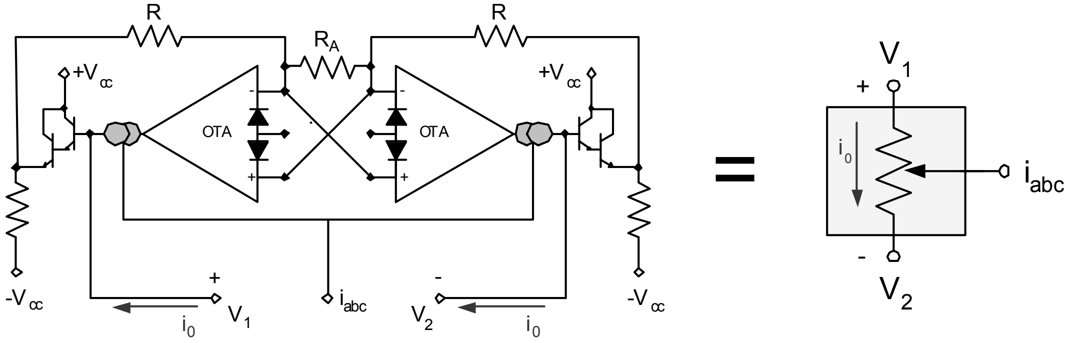


Figure 28: OTA Variable Resistor Circuit

The effective resistance of this circuit (R_{eff}), which is the resistance seen between the terminals V_1 and V_2 is determined by:

$$R_{eff} = \frac{(V_1 - V_2)}{i_0} = \frac{2R + R_a}{R_a \cdot g_m} \tag{4.27}$$

A negative resistance circuit was developed with the same design by switching the polarity of the OTA inputs, which results in reversing the current flow. The power system network is represented in hardware by constructing the four DC emulation networks with these variable resistive circuits. The network parameters are fully controllable and reconfigurable via the transconductance gain of the OTAs. Line outages and circuit breaker openings can also be represented by setting the bias current to zero for all OTAs representing the line out of service. Additional hardware was incorporated into the emulator for data acquisition and control.

Analog isolation and signal conditioning was provided between the emulation hardware and the digital computer/analog to digital converters. All control signals are conditioned and isolated. This was to ensure no disturbances or failures in the analog hardware could adversely affect the digital hardware. In addition, measurement and signal conditioning hardware was included within the emulator to process data before data acquisition. For current measurement instrumentation amplifiers measure and conditioned voltages across current sensing resistors embedded in the emulation networks. These current sensing resistors are lumped within the network model as to not induce error into the emulation. Instrumentation amplifiers were also used to condition voltages measurements before analog to digital conversion. Other parameters such as electrical power injections, power angles, and other state variables are also conditioned in the analog hardware.

The complete power system emulator is shown in Figure 29. A National Instruments PXI chassis is used. This chassis includes a fully integrated digital computer including CPU, graphics card, PXI slots, SCXI slots, USB ports, etc. A keyboard, mouse and monitor are attached directly to this chassis. This allows for user interface and software development. Data acquisition and control hardware were incorporated via the PXI interface. PXI is an open industry standard developed for instrumentation. It is similar to PCI architecture but includes some additions specifically for instrumentation. In this work analog-to-digital converters, digital-to-analog converters, and digital counters/timers are attached via the PXI slots. This hardware is connected via cabling in front of the chassis directly to the analog emulation hardware. The analog emulation hardware was developed in modular fashion to interface with the PXI chassis.

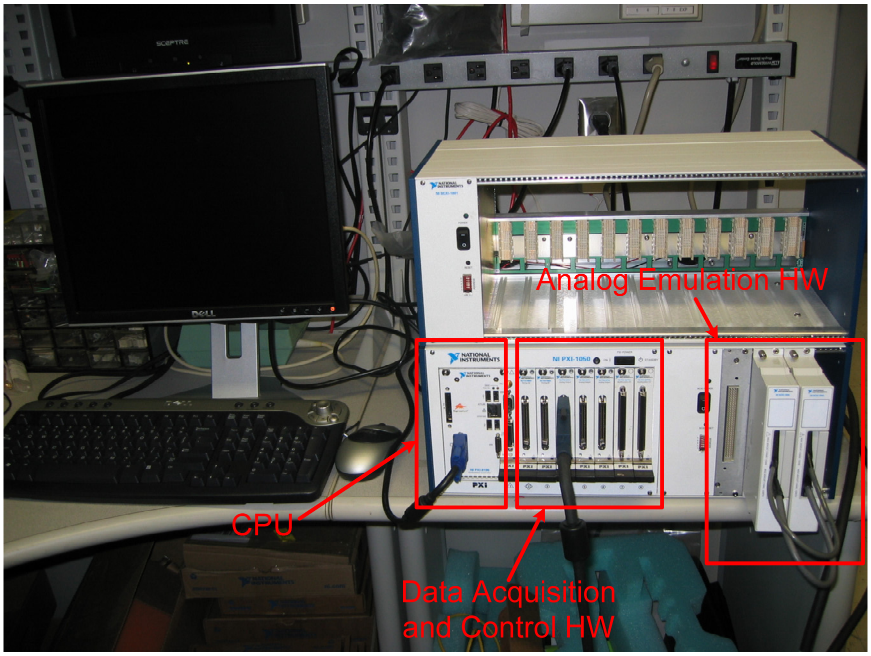


Figure 29: Complete Power System Emulator

Modules for the analog emulator were designed to interface with the SCXI slots in the chassis. The generator module is shown in Figure 30. This module emulates one generator. The analog isolation module, load emulation module, and network emulation module are shown in Figure 31. The load module emulates a single load and the network module consists of twelve variable resistance circuits. These variable resistive circuits can be configured to be either positive or negative resistance and interconnected in any fashion. These modules slide directly into the SCXI slots and have three connectors.

Each module has a 24 pin connector to that receive unregulated power from the chassis. Onboard power supplies regulate and supply the required power for each module. A 50 pin connector provides interface to all data acquisition and control circuitry via a backplane in the PXI chassis. The interconnection of emulation modules is accomplished via a 96 pin connector. The emulation system as shown in Figure 29 emulates a three bus power system. This system consists of three transmission lines, two generators and a single load. In this configuration there still exist twelve additional SCXI slots for expansion. The software for the emulator was developed to control the three bus system. However, the software was designed in a modular fashion which allows for interface to a larger system.

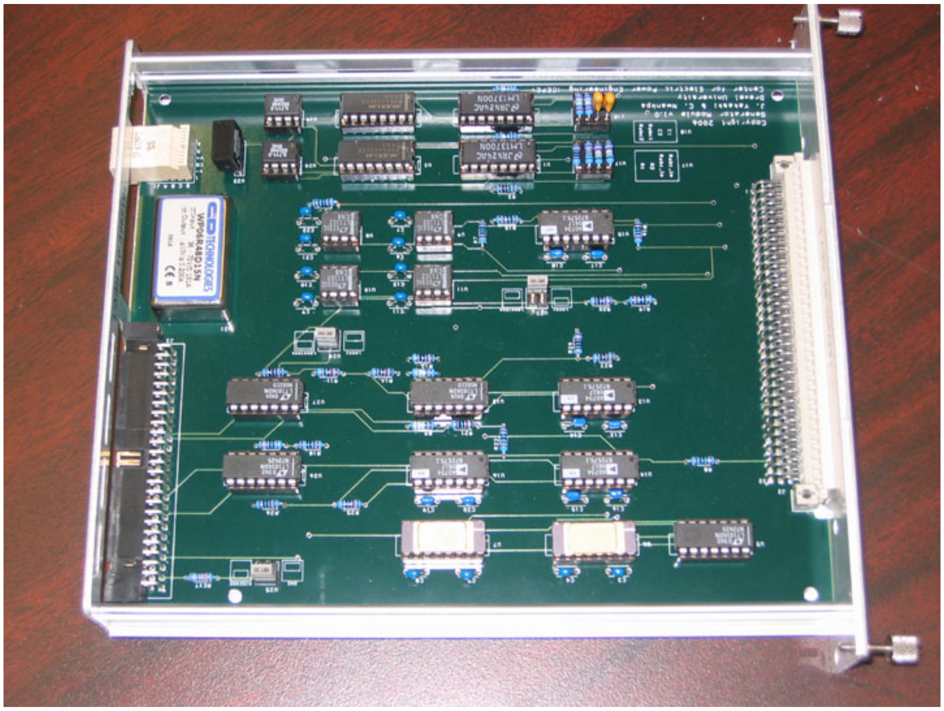


Figure 30: Generator Module

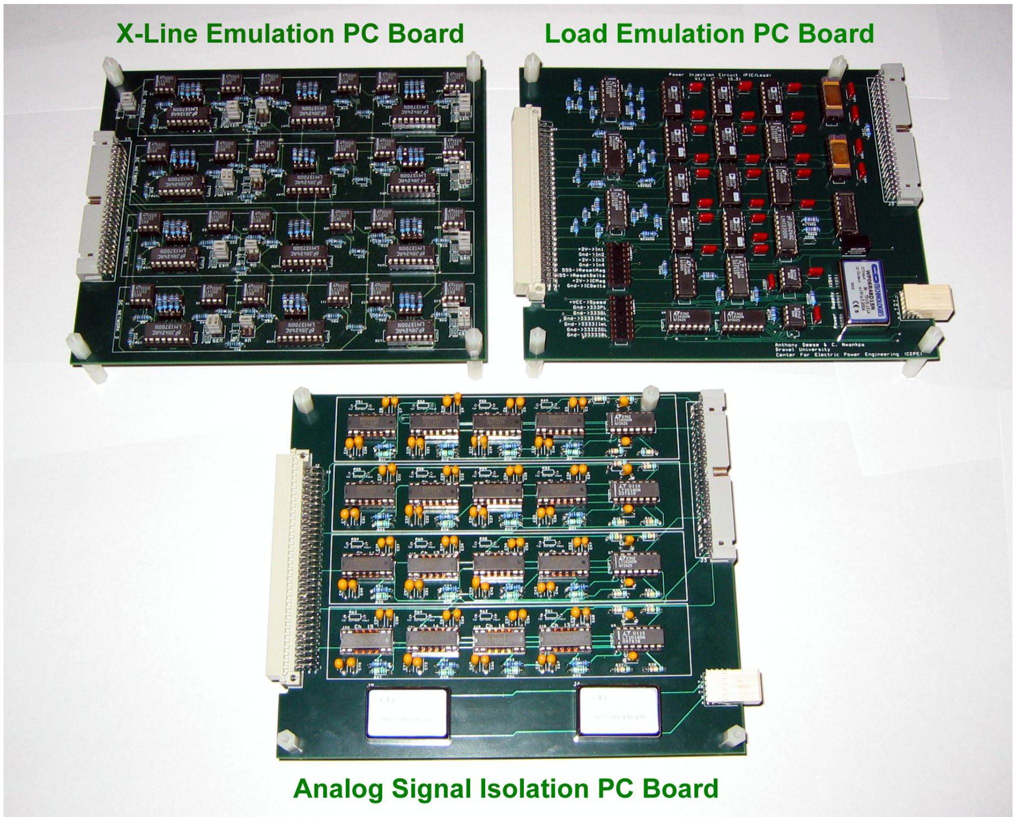


Figure 31: Network, Load, and Isolation Modules

4.4 SCALING POWER SYSTEM PARAMETERS FOR EMULATION

Scaling of parameters is an essential part of the analog computation and system emulation processes. The scaling requirements for system emulation detailed in theorem 4 are satisfied by the scaling process presented here. System parameters must be scaled and configured (historically manually) in relation to the real world system it is representing. In the scaling process the limitations of the hardware, namely linearity and stress, are addressed. The hardware must be configured to allow proper emulation of the system without violating the constraints of the circuitry.

Historically the components of analog computers (resistors, op-amps, etc.) are highly linear in a large operating range, specifically, levels of 10 or 100V. In the DC emulation hardware the levels are much lower due to nonlinear devices. For example, the linear operating range of a BJT based operational transconductance amplifier (OTA) is ±25mV [56] and ±1mA [55]. Signal fidelity must also be maintained to ensure measurability of the solutions, which are analog voltages and currents. Most literature on the subject of scaling [5-7, 57, 58] separates scaling into two main components: time and magnitude.

Time scaling allows analog computers to calculate in real time and faster or slower than real time. Magnitude scaling is defined as "the process through which a linear relationship is established between the voltage at any reference node and the variable represented by it" [6]. Magnitude scaling factors are utilized to scale the parameters (line impedance, power injections, etc.) to appropriate levels which the analog hardware can represent. For example, the analogous resistance values in the DC emulation networks must fall within a range achievable via the OTA based resistor circuits. Magnitude scaling is typically performed in a linear fashion as follows:

$$X_{PS} = x_{HW} \cdot X_b \tag{4.28}$$

where

$X_{PS} \triangleq$ physical quantity related to the power system

$x_{HW} \triangleq$ analogous physical quantity in the emulator

$X_b \triangleq$ magnitude scaling factor

Time scaling is conducted in a similar linear fashion. Generally speaking the relationship between the time of the power system under study and the analog emulation can be represented by:

$$t_{HW} = \frac{t_{PS}}{\tau} \tag{4.29}$$

where

$t_{PS} \triangleq$ power system time

$t_{HW} \triangleq$ analogous time in the emulator

$\tau \triangleq$ time scaling factor

For $\tau \geq 1$ the emulator will run faster than the real phenomena being emulated. A value of $\tau \leq 1$ will result in emulation slower than real time and $\tau = 1$ will result in real time computation. For power system analysis it is desirable to speed up the computation as much as possible but there are limitations to doing so.

The main limiting factors to time scaling are the analog hardware itself and the data acquisition. The analog hardware is comprised of many active and passive electronic elements and has associated frequency responses. Generally the responses will drop off once the frequency increases beyond a certain level. In order for accurate emulation the transients being emulated must be below these frequencies. In addition, the sampling frequency for data acquisition must be higher than the frequency of the fastest transient to be emulated.

The scaling process traditionally involved a trial and error approach. "Rough estimation of maximum values and fine tuning gains for small/large values" [58] until the analog computer is within operating regions (i.e. no overloads) and acceptable noise levels for measurement. In the past "a large simulator is often setup in a number of stages" [58]. The scaling approached formulated for this work involves linear scaling of magnitude and time and has been automated to allow for fast configuration of the emulator.

One application of this emulator is transient stability analysis. With trial and error methods, it is not possible to ensure operation within linear regions. The approach taken here is to ensure all stable cases fall within linear regions. If this is accomplished saturation of the electronic devices may be used as an indicator for instability. In the scaling process used in this work a one-to-one mapping of the power system states and parameters to the analog hardware states and parameters is developed. This mapping is constrained based on the analog hardware limitations and measurement requirements. The power system states and parameters are quantified and described using intervals. For example an interval for a generator voltage magnitude $\widetilde{V}_G$ is defined as:

$$\left[V_G\right] = \left[\underline{V_G}, \overline{V_G}\right] := \left\{\widetilde{V}_G \in \mathbb{R} \mid \underline{V_G} \le \widetilde{V}_G \le \overline{V_G}\right\} \tag{4.30}$$

where

$\left[V_G\right] \triangleq$ interval of $\widetilde{V}_G$

$\overline{V_G} \triangleq$ supremum of $\widetilde{V}_G$

$\underline{V_G} \triangleq$ infimum of $\widetilde{V}_G$

The intervals for all power system parameters (e.g. moment of inertia, line impedances, etc) can be determined from power system data. Determining the intervals for power system states (e.g. voltages, currents, etc.) requires further analysis. In this approach a linearized analysis of the power system dynamics is utilized to estimate the intervals of the power system states. Refer to [48] for further details. The intervals describing the analog hardware are determined based on properties of the hardware. With these intervals the scaling process was defined as follows:

$$\begin{aligned}&\text{Determine } \tilde{K} \text{ and } \tau \text{ such that:}\\ &\tilde{K} \cdot [PS] \subseteq [HW]\\ &\tau \leq \tau_{\max}\\ &\tilde{K} \subseteq [K]\\ &M_{SNR} \geq SNR_{\min}\end{aligned} \tag{4.31}$$

where

$\tilde{K} \triangleq$ row vector containing all magnitude scaling factors

$[PS] \triangleq$ vector of power system state and parameter intervals

$[HW] \triangleq$ vector of analog hardware state and parameter intervals

$\tau_{\max} \triangleq$ maximum speedup factor of analog hardware

$[K] \triangleq$ vector of analog hardware gain intervals

$M_{SNR} \triangleq$ vector of signal-to-noise ratios of emulator measurements

$SNR_{\min} \triangleq$ minimum required signal to noise ratio

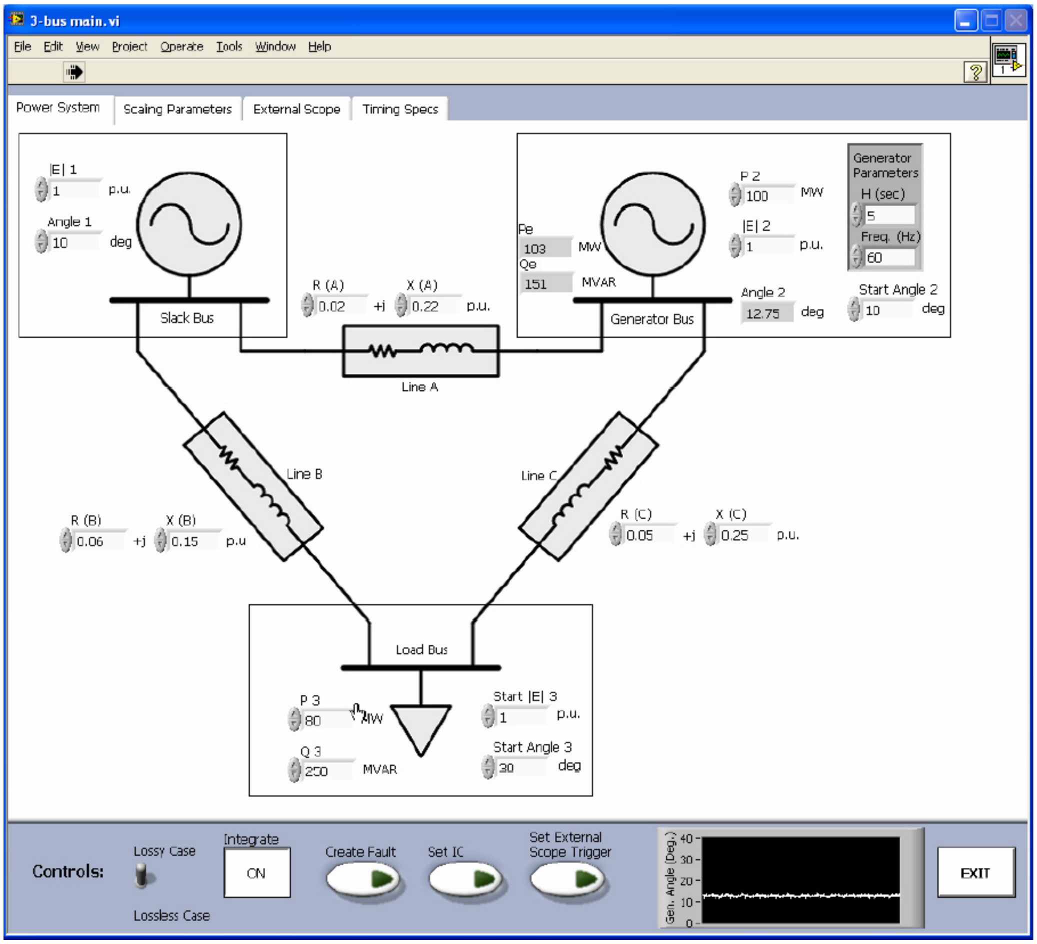
The result of this scaling process is the determination of the time and magnitude scaling factors such that the analog hardware can properly emulate the system. More specifically, a linearly scaled mapping is created between the power system and the power system emulator. This behavior satisfies the requirements for system emulation in theorem 4. The emulator is configured based on one single time scaling factor. All dynamics are scaled identically in time. This is necessary to properly emulate the system. The time scaling factor is constrained to a maximum value determined by the operation of the analog hardware. The magnitude scaling factors are constrained based on the limitations of analog hardware. For example, the OTA gain while controllable has a finite interval on which it can be adjusted. This interval results in an associated interval for the scaling factor which maps a network impedance to the variable resistor circuit. Determination of the power system state intervals and signal-to-noise ratio of measurements requires running a linearized analysis of the power system for predetermined cases. If the set of predetermined cases is insufficient, or the resulting errors from the linearized analysis grow large the results from this scaling process will not be precise. Generally speaking the system is scaled in a conservative manner to try and accommodate any such errors.

It should be noted that the scaling process is defined based on a few hard constraints. With this definition a feasible solution space may not exist. In the event this occurs the constraints can be made to be soft by incorporating penalty factors for constraint violation. This will ensure a solution can be found. The quality of this solution can be post processed to determine feasibility. In addition, the scaling process can be defined as an optimization problem. The power consumption of analog hardware could be minimized, signal-to-noise ratio maximized, or optimized to other objectives. The strength of the scaling approach presented here as compared to historical scaling methods is that it is flexible and can be automated via software for an arbitrarily sized system.

4.5 SOFTWARE FOR DATA ACQUISITION AND CONTROL

An overview has been provided on the hardware configuration, control and data acquisition of the power system emulator. This section details the functionality of the software interface. The software interface is where the end user operates the emulator. This software was developed with National Instruments LabVIEW [59].

The main panel of the interface for the three bus power system emulator which has been constructed is shown in Figure 32. From this main panel the system topology can be seen which consists of three transmission lines, two generators (one slack) and a single load. Basic operation of the emulator is conducted via this interface. System parameters are entered and can be adjusted in real time during emulation. Data is also acquired and displayed during emulation.



|E| 1 1 p.u.

Angle 1 10 deg

R (A) 0.02 +j X (A) 0.22 p.u.

Pe 103 MW

Qe 151 MVAR

P 2 100 MW

|E| 2 1 p.u.

Angle 2 12.75 deg

H (sec) 5

Freq. (Hz) 60

Start Angle 2 10 deg

R (B) 0.06 +j X (B) 0.15 p.u

R (C) 0.05 +j X (C) 0.25 p.u.

P 3 80 MW

Q 3 250 MVAR

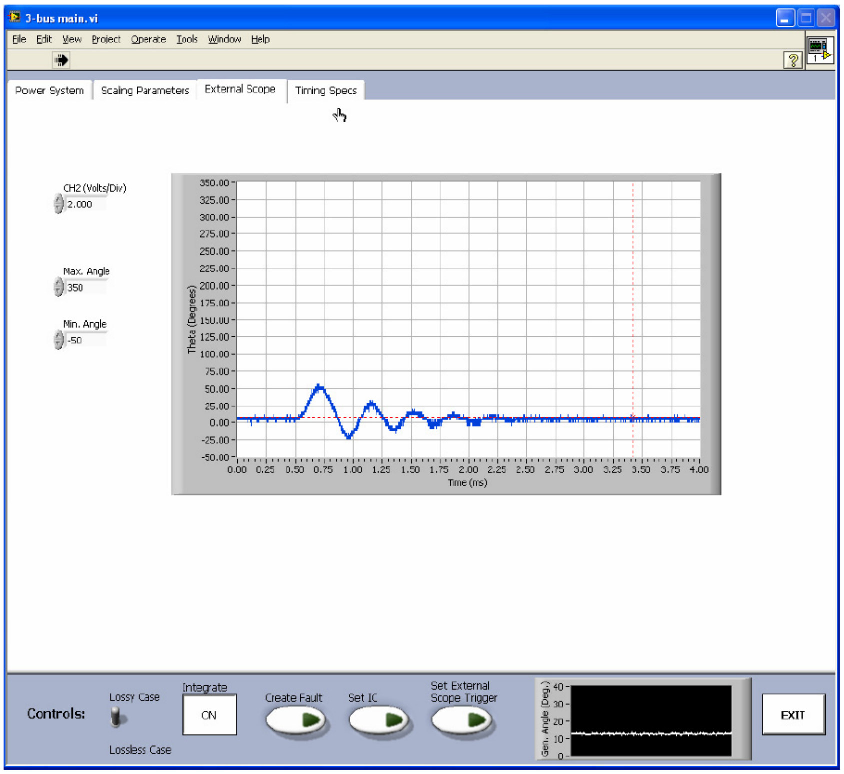
Start |E| 3 1 p.u.

Start Angle 3 30 deg

Figure 32: Emulator Graphical User Interface

Scaling and power system parameters are entered into the software interface. For the generator user input information is real power output in MW, voltage magnitude in per unit, system frequency in Hz, generator moment of inertia and initial condition for the generator angle. The boxes labeled Pe, Qe and angle 2 are measured values from the emulator. For the generator these are real and reactive power output and generator angle, respectively. In a similar manner system parameters are entered and data acquired for the load and transmission lines. The control panel at the bottom of the screen allows the user to control emulator actuation (turn the emulator on and off), set initial conditions on integrators, and also create system faults. The type of fault, duration of the fault and the clearing time of the fault can all be specified and controlled. Waveforms from the emulator can also be captured and displayed via the user interface as shown in Figure 33. Specifically this screen capture shows the generator angle response to a ground fault at the generator terminal.

The functionality explained thus far allows for the user to run and control the emulator manually. The software can also run in batch mode. For example, a set of predefined cases can be entered into the software and run in succession automatically. The cases could include different faults, contingencies, or even different system topologies. The user can also specify what data to acquire for each case.


CH2 (Volts/Div) 2.000

Max. Angle 350

Min. Angle -50

Integrate ON

Figure 33: Waveform Acquisition Screen

This chapter has provided detailed information on the power system emulator design and operation. This emulator is the analog computer in which the proposed method power system security assessment is performed. With the analog computer clearly defined the generalized theorems from chapter three can be applied specifically to the security assessment process and this analog computer. The following chapter provides an overview of performing security assessment with this analog computer.

5 ANALOG POWER SYSTEM SECURITY ASSESSMENT

This chapter provides details of the proposed method for analog power system security assessment. The goal is to first emulate the power system in steady-state by satisfying the requirements of theorems 1 and 2. Steady-state system emulation is based on power system information (mathematical models, system structure, and parameters) and a set of measured data. Dynamic contingency and stability analysis is then conducted once the system is emulated in the steady-state sense. This is accomplished by satisfying the requirements of theorems 1, 2, and 3. The result is a detailed analysis of the system security at the current operating point of the system.

5.1 STEADY-STATE POWER SYSTEM EMULATION

The formulation of steady-state power system emulation presented here assumes that the mathematical models and parameters of the system are known and correct. The model of the power system presented in chapter four is deemed acceptable for this application. As a result of this, and theorems 1 and 2, the steady-state system emulation problem is formulated in two parts. Namely, determining the correct power system topology and estimating the inputs to the emulator. By doing so, all the requirements for steady-state system emulation are satisfied. In this case the inputs are determined from measurements, or a subset of the measurements, taken from the power system and associated statistical information. The power system can be emulated in steady-state by identifying the correct topology and applying the estimated inputs to the emulator. While this formulation assumes the parameters are known it should be noted that in most applications these parameters are not explicitly known. Parameter estimation is required.

Parameter estimation utilizing analog techniques is left for future work. The next section addresses topology identification.

5.1.1 TOPOLOGY IDENTIFICATION

The process for determining the power system topology is shown in Figure 34. First the power system structure is modeled as a graph. Graph theory is utilized to identify potential topologies of the power system. Unlikely topologies can be discarded and not examined. For example, a topology in which no transmission lines are present need not be examined. Potential topologies are then tested with the analog emulator and measurement data. A performance index is defined and used to quantify, based on probability and measurement statistics, how well a particular topology matches the power system measurement data. Poor performance indexes are indicative of bad data and/or incorrect topologies. Bad data is identified and removed from the process. Once bad data is removed the correct topology is chosen as the one with the best performance index.

The process begins by defining the system as a bus section/switching device structure. An example of this system representation is shown in Figure 35. Based on the status of the switching devices and power system components numerous different topologies can be realized. The number of possible topologies can be large but is inherently finite. All the possible configurations can be identified and represented using graph theory.

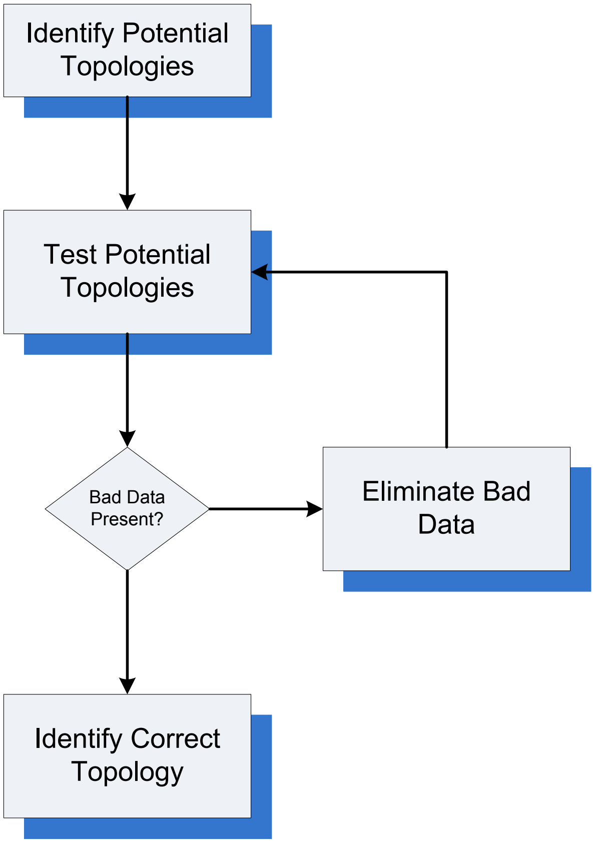

Identify Potential Topologies
Test Potential Topologies
Bad Data Present?
Eliminate Bad Data
Identify Correct Topology

Figure 34: Topology Determination Process

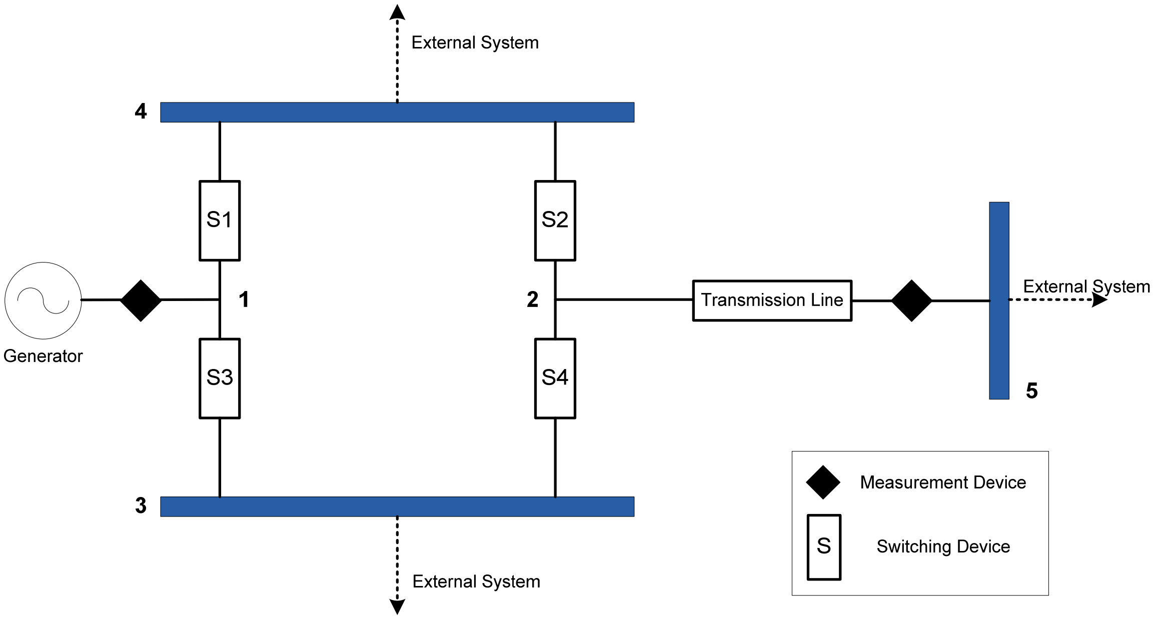


Figure 35: Bus-Section/Switching Device Power System Example

A graph, G, is defined by a set of vertices and a set of edges as follows [60]:

$$G = (V, E) \tag{5.1}$$

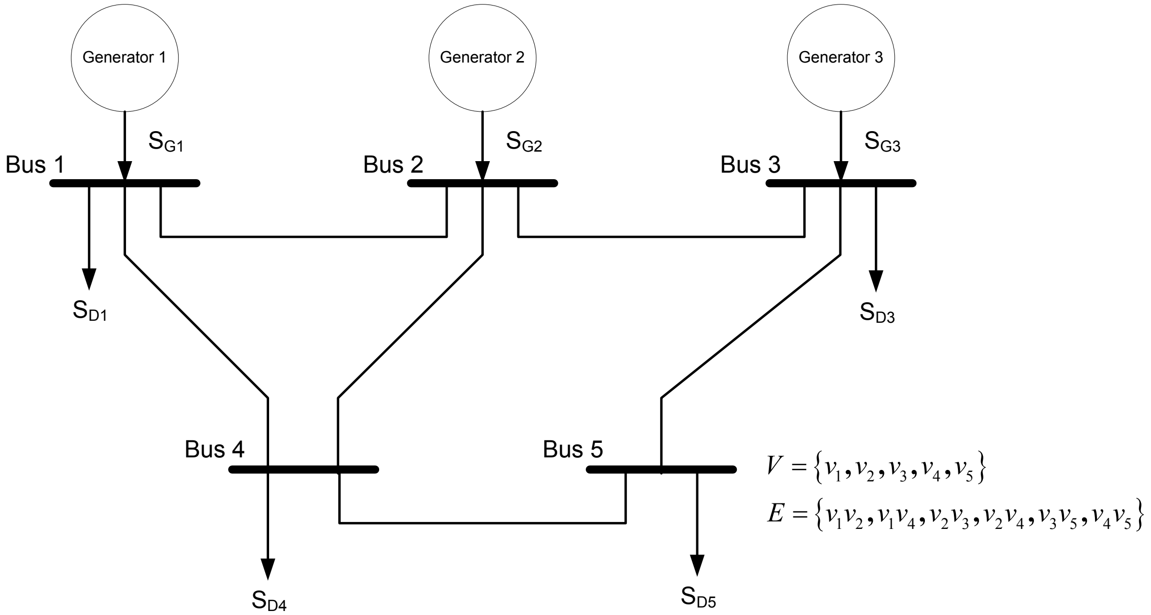
where V is a set of vertices, or nodes:

$$V = \{v_1, v_2, ..., v_n\} \tag{5.2}$$

and E is defined as a set of edges, or lines, which link the vertices:

$$E = \{v_1 v_2, v_2 v_{3,...}\} \tag{5.3}$$

A power system is easily represented as a graph from a one-line diagram. For example, a five bus system and the associated graph are shown in Figure 36. Each bus is defined as a vertex and each transmission line or transformer connecting two buses is defines as an edge. Buses one through five are denoted in graph form as the set of vertices $V = \{v_1, v_2, v_3, v_4, v_5\}$. The lines connecting the buses are denoted in graph form as the set of edges $E = \{v_1 v_2, v_1 v_4, v_2 v_3, v_2 v_4, v_3 v_4, v_3 v_5, v_4 v_5\}$. For example, the line connecting buses one and two is denoted by edge $v_1 v_2$.



$$V = \{v_1, v_2, v_3, v_4, v_5\}$$
$$E = \{v_1v_2, v_1v_4, v_2v_3, v_2v_4, v_3v_5, v_4v_5\}$$

Figure 36: Graph Definition for Five Bus System

Many different topologies can be formed for this five bus system. Four examples of connected topologies are shown in Figure 37. The graphs are connected if a path exists connecting every distinct pair of vertices. Topology I corresponds to the system shown in Figure 36. Topology II would represent the same system if the line between buses two and four were removed or taken out of service. During operation the power system is typically connected. It is designed and operated as an interconnected system. However, in certain situations islanding can occur. Examples of such situations are blackouts or a loss of a transmission line interconnecting two parts of the power system. In the absence of a large failure the system will typically remain connected. As a result, in this work all connected topologies are identified as potential topologies. The potential topologies of the power system are then a small, connected, subset of all possible topologies.

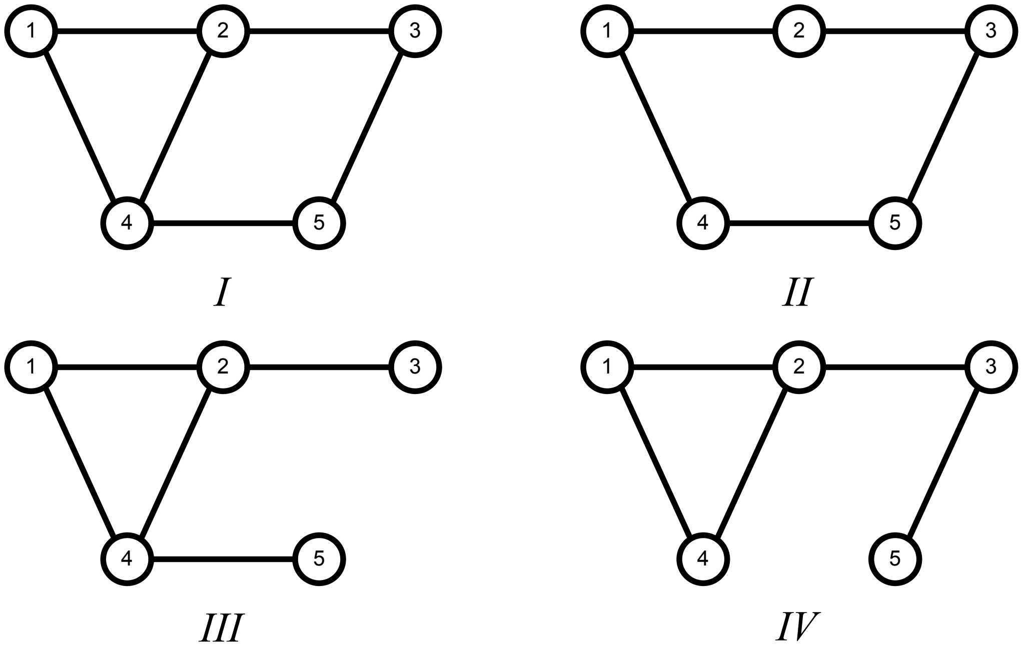


Figure 37: Potential Topologies for Five Bus System in Graph Form

Analyzing connectedness on all possible subgraphs of the power system graph identifies the set of potential topologies. There exist numerous techniques for analyzing connectedness. Some examples are depth-first-search (DFS) [61], breadth-first search (BFS) [62] or Floyd-Warshall algorithm [61]. BFS and DFS are search techniques which traverse the graph from a specified root node. The Floyd-Warshall algorithm defines shortest paths between nodes in the graph. This is performed via dynamic programming. Specifically, the Floyd-Warshall algorithm is designed for use on weighted directed graphs. In this application the graph is neither directed, nor weighted and connectivity determination does not require the determination of the shortest path. A modified Floyd-Warshall algorithm was used here to determine connectedness. This algorithm was chosen because it is well documented and relatively simple to implement as compared to other methods.

The modified Floyd-Warshall algorithm that was implemented is detailed in [61]. The algorithm accepts the power system graph in the form of an adjacency matrix as an input and computes the transitive closure of the graph. The transitive closure determines if a node can be reached from another node by traversing the edges of a graph. This is determined for all nodes in the graph. In an unconnected graph there is no method to traverse from some nodes to others. This information is obtained from the transitive closure. Connectivity of a given topology is obtained by analyzing the output of this algorithm. The power system graph used for this test contains all possible vertices and edges representing power system components. This graph is defined as:

$$G_{PS} = \{V_{PS}, E_{PS}\} \tag{5.4}$$

where

$G_{PS} \triangleq$ a graph representing the power system containing all possible edges and vertices

$V_{PS} \triangleq$ a set of all possible vertices of the power system

$E_{PS} \triangleq$ a set of all possible edges of the power system

By definition the actual topology of the power system at any point in time is a subset of this graph. Depending on the bus section/switching device structure of the system nodes can be created or eliminated based on the status of switches. Due to this G_{PS} is most likely not unique if it is formed directly from a one-line diagram of the power system. A unique G_{PS} can be defined for any system based on the bus section/switching device diagram and including the switches as edges in the graph. In a subgraph of G_{PS} the presence of an edge representing a switch indicates the switch is closed and an absence of this edge indicates an open switch.

A G_{PS} representing a power system structure can be said to consist of n vertices and m edges. The number of subgraphs of G_{PS}, or possible topologies of the power system, is then 2^m. The modified Floyd-Warshall algorithm is performed on all 2^m subgraphs to identify connectedness. The algorithm can also identify the number of islands present in unconnected graphs. For an unconnected graph the algorithm will output subsets of nodes that exhibit finite costs to reach each other. Each one of these subsets is an island.

This algorithm is performed using a digital computer. While this algorithm, or others, could have been implemented with analog techniques this was not examined in this work. The time complexity of the process is proportional to the number of vertices in the graph. More specifically, the algorithm will complete in a finite number of operations proportional to the number of vertices of the graph. This particular algorithm is proportional to the number of vertices due to the nature of transitive closure. Each vertex of the graph must be examined to determine transitive closure. For large power systems where many graphs need to be analyzed this can be a time consuming process. However, it is only required to be performed once for a given power system to identify all potential topologies. Only when a structural change to the system occurs (e.g. a construction of a new transmission line) is it required to run this algorithm again. Once all potential topologies are identified the emulator is utilized to test these topologies and identify the correct one.

Each potential topology is tested by the analog emulator. Steady-state analog computability is required for each test as outlined in lemma 1. Each topology is assigned a performance index based on the test results. This index is indicative of the likelihood that the topology is correct. This process requires redundant measurement data and analog computability for every topology/measurement set to be tested. For this work, the power system model for the emulator consists of power injections (generators and loads) and the power system network. The measurements are assumed to be one of six types, real power injection (P), reactive power injection (Q), bus voltage magnitude $(|V|)$, bus voltage angle θ_V, injected current magnitude $(|I|)$, or injected current phase θ_I. Other measurements and/or models for the power system can be used but the formulation for computability will be slightly different.

From lemma 1, a given topology is computable in DC emulation if the network currents can be emulated correctly based on the inputs to the emulator. In other words $[I]=[Y][V]$ must be solvable based on the inputs. The measurement data from the power system is used directly as inputs to the analog emulator. For example, if all the measurements are voltages, then all bus voltage angles and magnitudes must be measured in order for a given topology to be computable. The computability formulation can be stated in a more precise form similar to those shown in chapter 3.

Any potential topology can be viewed as a network with n nodes which requires a minimum of $2n$ measurements to be computable. At each node there are a total of six variables: complex power injection (P,Q), voltage $(|V|,\theta_V)$, and complex current injection $(|I|,\theta_I)$. Figure 38 shows a generic node, or bus, in the power system. The node is shown as bus *i* and has a power injection and a connection to the network. Of the six variables only two are required to be specified. The other four can be solved for by the emulator. For example, if the power injection is a PQ load connected to the network the load circuit applies the applicable voltage to satisfy the specified PQ and resulting current flow in the network. Essentially the network is solving for the current variables and the load is solving for the voltage variables. So long as any two variables are measured at every bus the potential topology is analog computable by this emulator in the *steady-state* sense. Every computable topology can be tested and assigned a performance index.

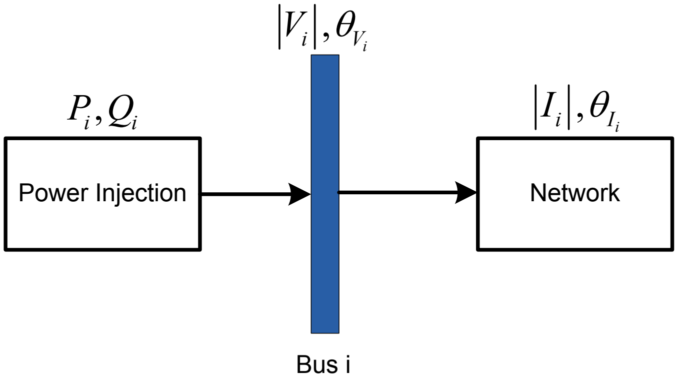


Figure 38: Power System Bus

It is assumed redundant data exists in order to test a topology. Multiple computable sets of inputs to the emulator exist with redundant measurement data. The computability requirements and the number of measurements available determine how many computable sets exist. For a given topology where k is defined as the number of measurements and $2n$ the number of measurements required for computability. The degree of redundancy (DoR) is defined as:

$$DoR = k - 2n \tag{5.5}$$

If

$DoR \leq 0$ topology is not computable

$DoR = 0$ topology computable with one set of inputs

$DoR \geq 0$ topology computable with multiple sets of inputs

With redundant data the number of computable sets (ComputSets) of data can be determined by:

$$ComputSets = C_{2n}^{k} = \begin{pmatrix} k \\ 2n \end{pmatrix} = \frac{k!}{(2n)!(k-2n)!} \tag{5.6}$$

A test can be conducted for each one of these combinations, or a subset of these combinations, in order to calculate the performance index of each topology. For testing purposes the following assumptions are made:

1. The inputs to the emulator are correct.
2. The variances of the power system measurements are known.

3. The variances of the emulator measurements are known.
4. All measurements are normally distributed.
5. The random errors in measurement are statistically independent variables.

Taking one computable set of data and applying it to the input of the emulator conducts the test. This will bring the emulator to a steady-state operating point based on the data from the computable set. Measurements are then taken from the emulator at this operating point. Specifically, these measurements are taken at the points where redundant data that is not in the computable set exists. The performance index is calculated by comparing this measured data from the emulator to the measured data from the power system. The procedure is similar to the process used in detection theory.

Ideally if the inputs to the emulator are correct, all power system measurements correct, and the topology correct, then the measurement from the emulator would precisely match the measurement from the power system. However, due to errors and noise in both the power system and emulator measurements this will not be the case. As long as these measurement errors are relatively small they will only cause slight differences between the power system measurement and emulator measurement. Bad data and topological errors will yield very large deviations in these two measurements. This property allows for detection and elimination of bad data. The performance index is designed and calculated based on these properties. For each redundant measurement not in the computable set the probability of the measurement being correct for the given topology and emulator inputs can be quantified. This is shown graphically in Figure 39.

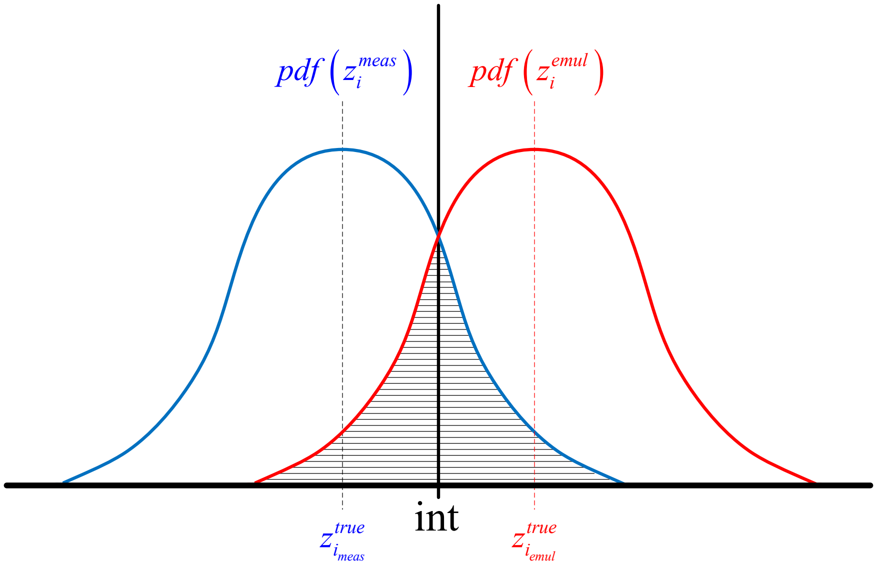


Figure 39: Likelihood Test

The probability of measurement z_i^{meas} from the power system being correct is quantified by the overlap of the probability density functions of the measurement z_i^{meas} and the measurement of the same point from the emulator z_i^{emul}. The probability density function of the power system measurement is:

$$pdf\left(z_i^{meas}\right)=\frac{1}{\sigma_i^{meas}\sqrt{2\pi}}e^{\frac{\left(z_{i_{meas}}^{true}-z_i^{meas}\right)^2}{2\sigma_i^{meas^2}}} \tag{5.7}$$

and the probability density function of the emulator measurement is:

$$pdf\left(z_i^{emul}\right)=\frac{1}{\sigma_i^{emul}\sqrt{2\pi}}e^{\frac{\left(z_{i_{emul}}^{true}-z_i^{emul}\right)^2}{2\sigma_i^{emul^2}}} \tag{5.8}$$

The probability of the power system measurement being correct, $P\left(z_i^{meas}\right)$, is quantified by the shaded region in Figure 39. This area can be computed numerically by:

$$P\left(z_i^{meas}\right)=\begin{cases}\int\limits_{-\infty}^{\text{int}} pdf\left(z_i^{emul}\right)dz+\int\limits_{\text{int}}^{\infty} pdf\left(z_i^{meas}\right)dz & \text{for } z_i^{emul}\geq z_i^{meas}\\ \int\limits_{-\infty}^{\text{int}} pdf\left(z_i^{meas}\right)dz+\int\limits_{\text{int}}^{\infty} pdf\left(z_i^{emul}\right)dz & \text{for } z_i^{emul}< z_i^{meas}\end{cases} \tag{5.9}$$

This probability is computed for each redundant measurement. From these probabilities the probability of all measurements being correct for a given computable set m is computed by a weighted average of the individual probabilities:

$$P\left(m\right)=\frac{1}{\sum\limits_{i=1}^{DoR}\frac{1}{\sigma_i^{meas}}}\cdot\sum_{i=1}^{DoR}\frac{1}{\sigma_i^{meas}}P\left(z_i^{meas}\right) \tag{5.10}$$

Each individual probability is weighted with the variance of the measurements. This allows for more accurate measurements to have more impact on the probability. $P\left(m\right)$ is computed for each computable set of data for the topology. The performance index for a given topology is based on these probabilities. Numerous different performance indices could be defined. The performance index used in this work is as follows:

$$PI = \sum_{m=1}^{n_{cs}} \frac{1}{P(m)} \tag{5.11}$$

where

$n_{cs} \triangleq$ the number of computable sets used in testing a topology

With this performance index a low probability will result in a large PI. Topologies with very large PI are discarded as incorrect. A low PI is indicative of a topology that closely matches the acquired data from the power system. A PI is computed for each potential topology. The correct topology is chosen as the one that exhibits the lowest performance index. This procedure is shown as a block diagram in Figure 40.

This process identifies the topologies through testing. Topological errors will come through the process as a high PI. However, bad data measured from the power system will also result in a high PI. It is essential to distinguish where the error is coming from, either topological or measurement error. This process is well suited for identifying the source of errors. For a given measurement analyzing $P\left(z_i^{meas}\right)$ will provide information on measurement and/or topology errors:

- If $P\left(z_i^{meas}\right)$ is consistently low for all topologies tested then the measurement data is most likely bad.
- If $P\left(z_i^{meas}\right)$ is low for one, or multiple similar topologies then this error is most likely due to errors in those topologies.

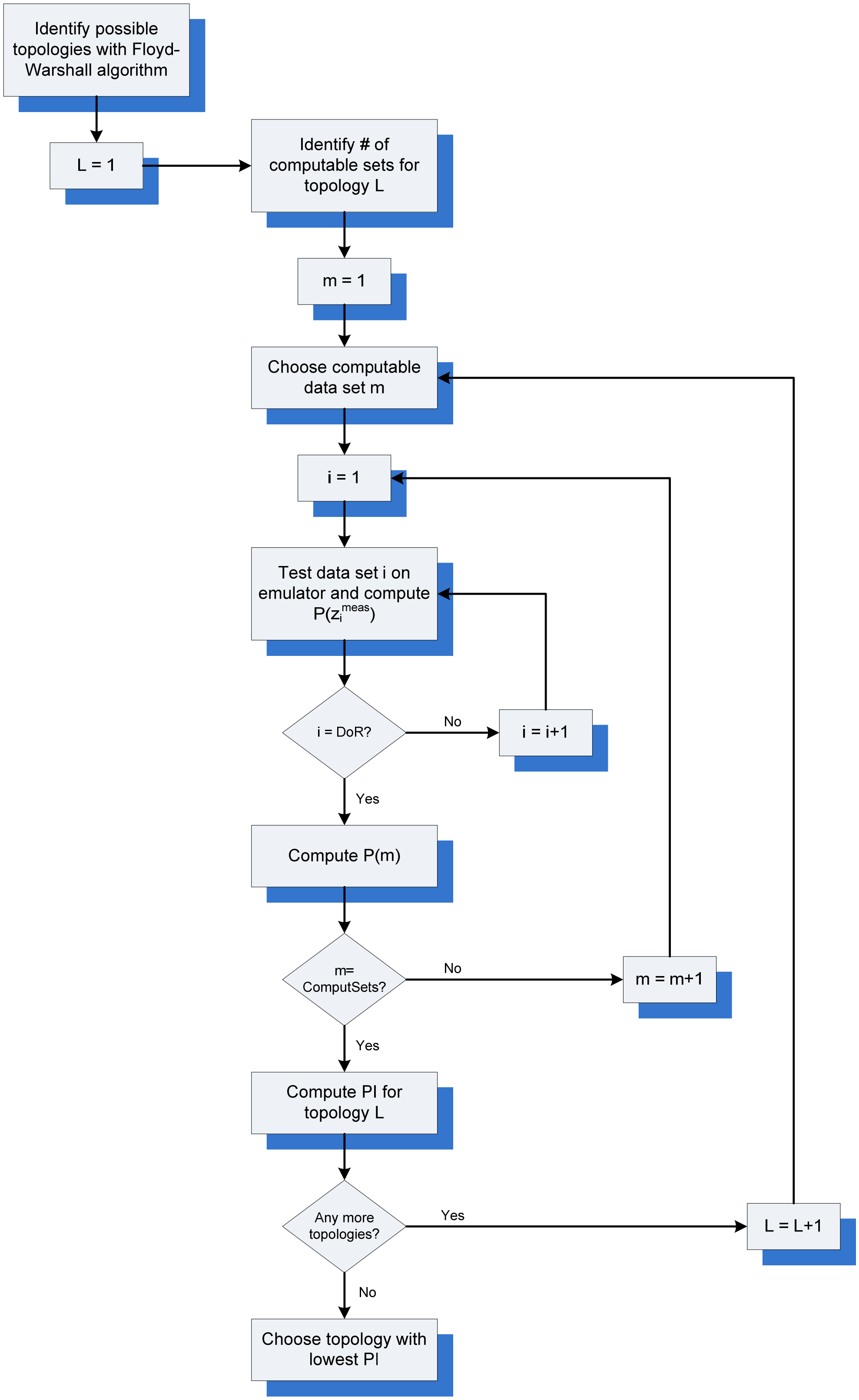

Identify possible topologies with Floyd-Warshall algorithm
L = 1
Identify # of computable sets for topology L
m = 1
Choose computable data set m
i = 1
Test data set i on emulator and compute P(z$_i^{meas}$)
i = DoR?
No
i = i+1
Yes
Compute P(m)
m= ComputSets?
No
m = m+1
Yes
Compute PI for topology L
Any more topologies?
Yes
L = L+1
No
Choose topology with lowest PI

Figure 40: Topology Testing Procedure

In the event of topological errors those topologies are thrown out as incorrect with a high PI. In the case of measurement errors the performance indices are recalculated excluding any data related to the bad measurement data. Input identification is performed once the correct topology is identified.

5.1.2 INPUT IDENTIFICATION

Given a set of good data and the correct topology, the power system can be emulated in steady-state by identifying the correct inputs to the emulator. From theorem 1, two out of the three requirements have been met. The system is analog computable (this was a requirement for topology identification) and the functional description of the system is known (correct topology and correct functional description from accepted models). Once the correct inputs are identified the system can be emulated in steady-state. In this case the inputs are not explicitly known. As a result, an estimate of the actual inputs derived from measurements from the system is assumed to be the correct input to the analog computer. The basic approach taken here is to adjust the inputs in a method to achieve the highest probability that the inputs are correct for a given topology. The computable set of inputs from the topology identification process that yields the highest $P(m)$ is taken as a starting point for input identification. From this point the inputs are adjusted in order to achieve the highest probability.

The probability for input identification is slightly different than in topology identification. Specifically the difference is that more individual probabilities are required to compute $P(m)$. Since the emulator inputs will be altered to estimate the power system inputs the emulator inputs should also be used when computing $P(m)$. The computation is carried out as follows for n measurements:

$$P(m)=\frac{1}{\sum_{i=1}^{n}\frac{1}{\sigma_i}}\cdot\sum_{i=1}^{n}\frac{1}{\sigma_i}P\left(z_i^{meas}\right) \tag{5.12}$$

To save time in computing this probability for a given set of inputs, the inputs can be taken as pseudo measurements and not explicitly measured from the emulator. Doing this assumes that the inputs are being applied to the emulator correctly. With this method only the redundant data is required to be measured from the emulator. Numerous techniques could be utilized in adjusting the inputs to maximize $P(m)$.

One approach to find a high $P(m)$ is to perform Monte Carlo style emulations. Many different sets of inputs can be randomly generated and applied to the emulator. The probability is computed for each set. The set of inputs that yield the highest probability will then be chosen as the correct set of inputs. A good estimate of the inputs can be found by performing numerous emulations. However, as the number of emulation runs increases so does the computation time necessary to emulate the power system. A different approach could yield a good estimate of the system inputs in a shorter time frame. One such approach is to use heuristics to alter the inputs towards values that achieve a higher probability.

The basic idea in utilizing heuristics is to alter the inputs in a direction that raises $P(m)$. For example, if a measurement of real power injection in the emulator is lower than the analogous power system measurement altering an input to the emulator could raise the power injection and hence raise $P(m)$. More specifically, if the voltage angle at the injection point is an input to the emulator it could be changed to raise the real power injection. In a similar fashion voltage magnitudes could be raised to increase reactive power injections. Conversely, if power injections are inputs to the emulator, real power inputs can be changed to change voltage angles and reactive power injections changed to change voltage magnitudes. A generalized iterative scheme for adjusting an emulator with n inputs is as follows:

$$\mathbf{x}^{i+1} = \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix}^{i+1} = \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix}^{i} + \alpha [D] \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \vdots \\ \sigma_n \end{bmatrix} = \mathbf{x}^i + \alpha [D] \sigma \tag{5.13}$$

where

$\mathbf{x}^i \triangleq$ the input vector at step *i*

$\mathbf{x}^{i+1} \triangleq$ the input vector at step *i*+1

$\alpha \triangleq$ a scalar parameter dictating how much to adjust the input vector

$\sigma \triangleq$ a vector weighting input adjustments based on measurement standard deviations

$[D] \triangleq$ diagonal direction matrix dictating which direction to adjust inputs

This scheme can be run numerous times to achieve different operating points in the emulator and different probabilities $P(m)$. The changes in inputs are weighted based on the standard deviation of the power system measurements. This is done because inputs with larger standard deviations can be changed more with less effect on $P(m)$ in comparison to more accurate measurements with small standard deviations. The scaling factor α is a parameter specified which dictates how large of a step from the prior iteration should be taken. If the step is too large the process will take the emulator to an operating point far from the actual power system operating point. If α is too small it will take many steps to improve $P(m)$. Heuristics are utilized to determine the direction matrix D.

The direction matrix is a diagonal matrix. This assumes that the covariance between any two measurements is zero. If measurement covariance is modeled this matrix will not be diagonal. The non-zero off diagonal entries will be proportional to the measurement covariances. The diagonal entries in the direction matrix are either one, negative one, or zero. The values are determined based on heuristics. For example, if the input is a real power injection and heuristics dictate this should be raised to improve $P(m)$ then the corresponding entry in the D matrix is one. A positive value dictates that input should be increased from the previous value. The value should be negative one if the input should be decreased. If it is determined that a change in the input will not improve $P(m)$ then the entry should be zero. This heuristic evaluation is required for all emulator inputs. It should be noted that the process in equation (5.13) does not converge to a maximum. It is designed to find a high quality solution in a faster manner than a

Monte Carlo type method. It should be run until a relatively close match between the emulator and the power system measurements is found. In addition, noise in the analog emulator will affect this process.

Noise on the emulator inputs and noise in the emulator measurements will limit the precision of the analog solution. As a result there will be a minimum value of α for which the emulator can produce a discernibly different solution from the prior iteration. This minimum value will depend on the noise in analog hardware and the sensitivity of any given measurement to the inputs being changed each iteration. It is not a straightforward process to define a minimum α as it will vary on a case-by-case basis. However, it is easy to identify if a given α value is too low during emulation. If a noticeable change in the measurements, and likewise $P(m)$, is not observed from one iteration to the next the value chosen for α is too small. The value should be increased before another iteration is made. In addition, if the emulator is providing very noisy measurements, data can be sampled multiple times to gain confidence in the results. Inherently this will result in additional computation time. An example of the input identification process is demonstrated on a small two bus example.

The example two bus system is shown in Figure 41. It consists of a generator, a lossless transmission line, and a load. The true values and measured values are also shown. The real power injection from the generator, P_1, load bus voltage magnitude, $|V_2|$, and load bus voltage angle, θ_2, are measured. Bus 1 is designated as the slack bus. The power transfer across a short lossy transmission line is dictated by the following equation:

$$P_1 = \frac{|E_1||E_2|}{X_L}\mathbf{sin}\left(\theta_{12}\right) \tag{5.14}$$

where $\theta_{12} = \theta_1 - \theta_2 = -\theta_2$.

Given equation (5.14) and the known slack bus values, two measurements are required as inputs to compute the function. The degree of redundancy is one. With three measurements this yields three different computable sets. These three computable sets were used and the $P(m)$ calculated for each set of data. For this example the emulator solution is assumed to be equivalent to equation (5.14). The results are tabulated in Table 3.

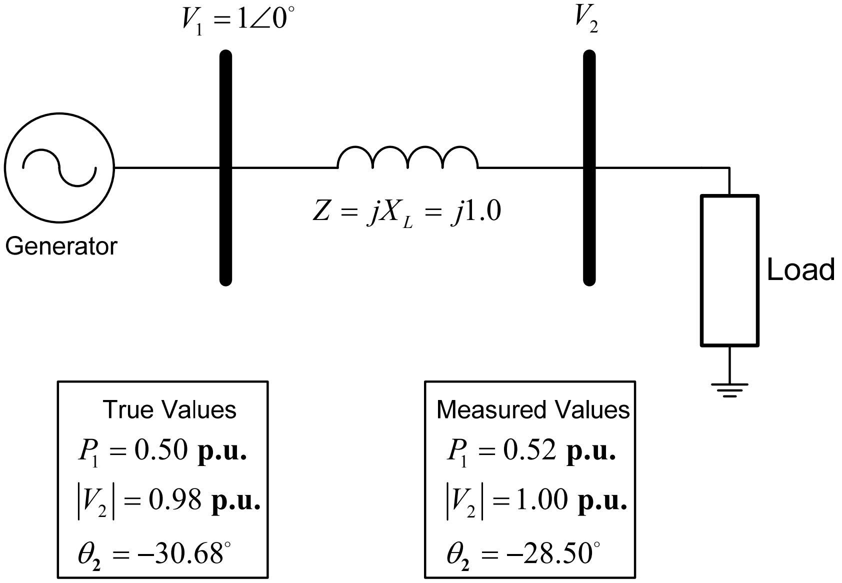


Figure 41: Two Bus Input Identification Example

Table 3: Results of Three Computable Sets

Inputs to Emulator	Emulator Solution	P(m)	Heuristic
P_1 , $\lvert V_2\rvert$	$\theta_2 = -31.332^\circ$	0.504	lower P, raise V
P_1 , θ_2	$\lvert V_2\rvert = 1.09$	0.527	raise angle, lower P
$\lvert V_2\rvert$, θ_2	$P_1 = 0.477$	0.762	raise angle

$P(m)$ was computed for each computable set as per equation (5.12). For this example, $\sigma_P = \sigma_V = 0.1$ and $\sigma_\theta = 3.0$ for both the power system and emulator measurements. The third case provided the best result while the first and second had relatively lower $P(m)$ values. The final column of the table details the heuristics for the given computable set to raise $P(m)$. The last computable set was taken as the starting point for adjusting the inputs to find the best estimate of the system operating point.

From the emulator solution of case 3 the power injected into bus one from the generator is 0.477 per unit. This is lower than the measured value of 0.52 per unit. In order to raise this power injection, and hence raise $P(m)$, the voltage magnitude at bus two could be raised and/or the angle at bus 2 changed. Changing the voltage angle will result in raising the power injection more than voltage magnitude based on the standard deviations of the measurements and equation (5.14). The angle was changed in steps and the results are tabulated in

Table 4. For this example $\alpha = 0.1$ and only the angle was adjusted. It can be seen from the results that a fairly high quality solution was obtained at step 28. $P(m)$ was

computed to be 0.984 for a $P_1 = 0.52$, $|V_2| = 1.0$, and $\theta_2 = -31.3^\circ$ These values are close to the true values and a significant improvement over the measured values. This example is a basic case in which only one input was changed to achieve good results. These results could be improved further by adjusting the other inputs. For larger cases changes to more than one input are required to find a high quality solution.

Table 4: Input Identification Results for 2 Bus System

Step	$\lvert V_2 \rvert$	θ_2	P_2	**P(m)**
0	1	-28.5	-0.477	0.769
1	1	-28.6	-0.479	0.779
2	1	-28.7	-0.480	0.783
3	1	-28.8	-0.482	0.795
4	1	-28.9	-0.483	0.799
5	1	-29.0	-0.485	0.809
6	1	-29.1	-0.486	0.813
7	1	-29.2	-0.488	0.823
8	1	-29.3	-0.489	0.828
9	1	-29.4	-0.491	0.838
10	1	-29.5	-0.492	0.842
11	1	-29.6	-0.494	0.852
12	1	-29.7	-0.495	0.857
13	1	-29.8	-0.497	0.867
14	1	-29.9	-0.498	0.872
15	1	-30.0	-0.500	0.883
16	1	-30.1	-0.502	0.893
17	1	-30.2	-0.503	0.898
18	1	-30.3	-0.505	0.908
19	1	-30.4	-0.506	0.913
20	1	-30.5	-0.508	0.923
21	1	-30.6	-0.509	0.928
22	1	-30.7	-0.511	0.938
23	1	-30.8	-0.512	0.943
24	1	-30.9	-0.514	0.953
25	1	-31.0	-0.515	0.958
26	1	-31.1	-0.517	0.969
27	1	-31.2	-0.518	0.974
28	**1**	-31.3	**-0.520**	**0.984**
29	1	-31.4	-0.521	0.978
30	1	-31.5	-0.522	0.972
31	1	-31.6	-0.524	0.961
32	1	-31.7	-0.525	0.955
33	1	-31.8	-0.527	0.944
34	1	-31.9	-0.528	0.938
35	1	-32.0	-0.530	0.927

Generally speaking the set of inputs with the highest $P(m)$ during this process is chosen as the correct set of inputs for steady-state power system emulation. A decision is required as to when the inputs are sufficient or of a high enough quality. Defining a threshold for $P(m)$ could handle this determination. Once this threshold is reached the current inputs are selected as the estimates for steady-state emulation. At this point the topology and inputs have been identified. The emulator is configured based on this information and steady-state power system emulation is achieved as per theorem 1. The emulator is functioning at an estimated operating point based on the measurements from the power system. Contingency and stability analyses are performed at this operating point.

5.2 CONTINGENCY AND STABILITY ANALYSIS

The contingency and stability analysis procedure in analog form is similar to the digital contingency method outlined in Figure 42. The main difference is that the analog hardware provides a time domain representation of the system and measurements are required in order to analyze the performance of the system for each contingency. Due to the time domain representation of the system, faults can be emulated and transient stability determined. The procedure for analog contingency and stability analysis is shown in Figure 43.

In order to perform dynamic system emulation the requirements in theorems 1 and 3 must be satisfied. The inputs to the emulator over the time interval to be emulated need to be specified for each contingency emulated. The stead-state emulation point is used as initial conditions to all integrators. Specifics on the contingencies to be analyzed and inputs to be changed are defined by the user. These inputs are relatively arbitrary and can be defined as correct inputs for satisfying theorems 1 and 3.

The power system is first emulated in steady-state. At this point a contingency or fault is selected and the system is actuated to emulate the power system. Actuation is handled by turning on the integrators with a digital signal. Measurements are then taken and data analyzed to determine if the system is stable and within operating limitations. All contingencies and faults specified are run in a serial manner until all cases have been emulated. The process of emulating all of these contingencies is quite fast. For n-1 contingencies only two changes must be made to the emulator for each case. For example, if line outages are being studied going from one contingency to the next the line, which was just analyzed, must be added back to the system and another removed when running the next contingency. Similarly faults are also emulated very fast. The type of fault and fault time duration are specified and the emulator will emulate faster than real time based on the time scaling factor. Data Acquisition requires the most time.

In digital simulations all of the data is explicitly known and can be easily analyzed. Utilizing this analog technique data must be measured before analysis is possible. Measuring all the data from the emulator for each case is simply not feasible. This would slow down the computation process tremendously. However, for contingency and stability analysis many cases do not need to be analyzed. Namely, cases in which the system is stable and operating within predefined limits do not require extensive analysis. The approach taken here is to utilize analog hardware to analyze stability and system operating limits. Small sets of signals can be used to indicate if the system is stable or operating out of limits. More specifically, digital flags are used to indicate the status of the power system.

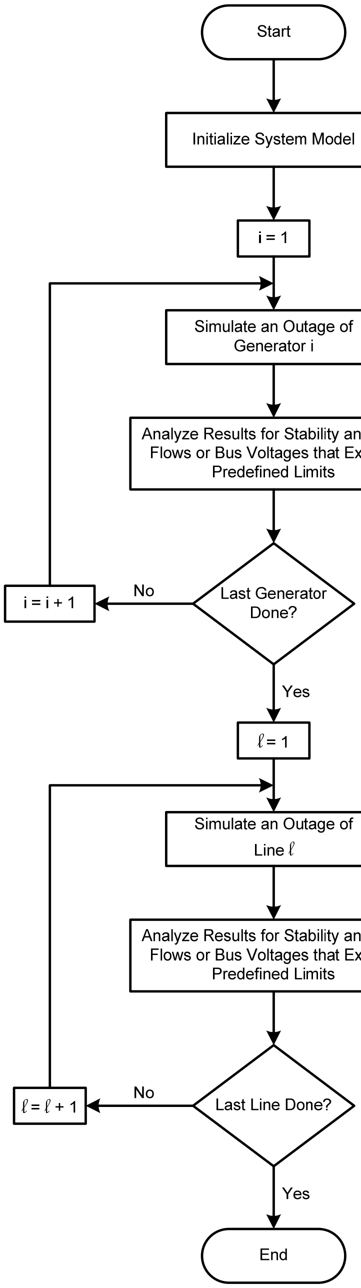

Start
Initialize System Model
i = 1
Simulate an Outage of Generator i
Analyze Results for Stability and Line Flows or Bus Voltages that Exceed Predefined Limits
Last Generator Done?
No
i = i + 1
Yes
ℓ = 1
Simulate an Outage of Line ℓ
Analyze Results for Stability and Line Flows or Bus Voltages that Exceed Predefined Limits
Last Line Done?
No
ℓ = ℓ + 1
Yes
End

Figure 42: Digital Contingency Analysis Procedure

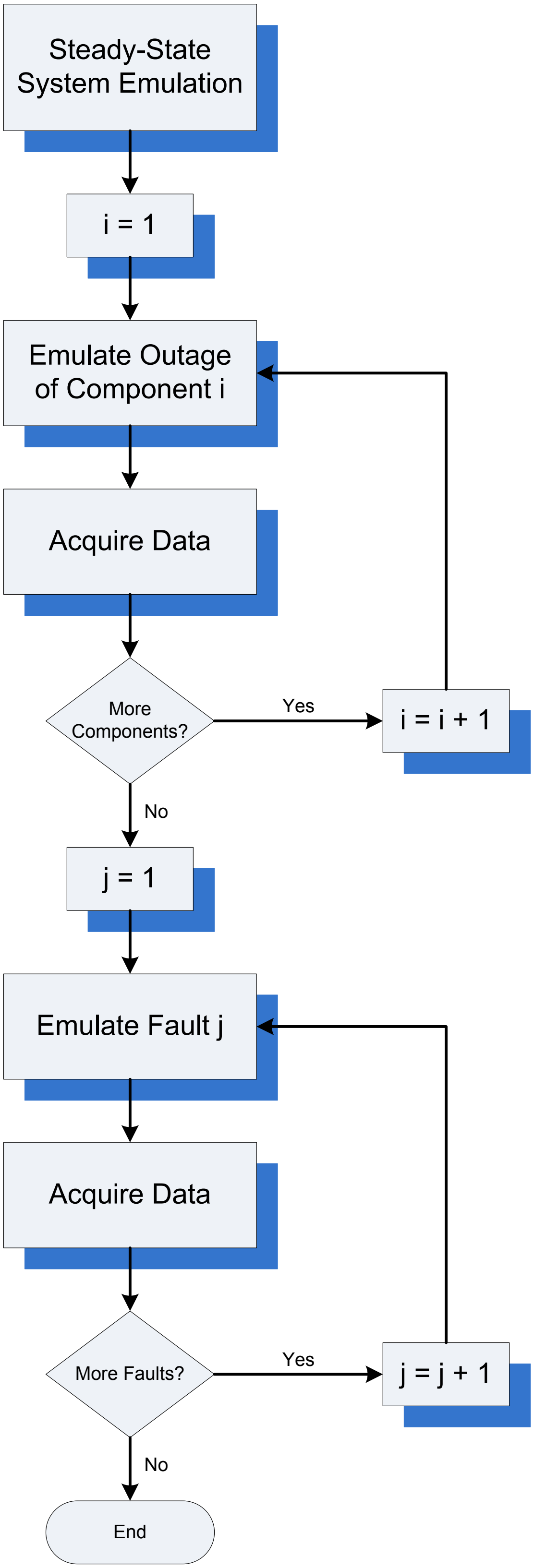


Figure 43: Analog Contingency and Stability Analysis Procedure

The digital flags are set by using comparators to compare the value in the emulator to a predetermined limit. If the limit is surpassed the comparator output will be set to one. If the limit is not exceeded the output will be zero. One comparator, or set of comparators, is used to indicate stability. Due to the nature of the analog hardware the devices will saturate when instability occurs. For example, if a generator loses synchronism with the grid the angle will grow large and saturate the output of the integrator. A similar behavior is exhibited in the loads. The operating region of integrator outputs can be divided into two parts as shown in Figure 44. There is the normal operating region and a saturated region. Through appropriate scaling of the power system into the analog hardware the devices will only hit the saturation region when exhibiting instability. A schematic for a comparator setup analyzing stability for a set of two generators is shown in Figure 45. With this circuit stability for the set of generators can be determined for each contingency by simply measuring one digital signal. If either generator goes unstable a comparator will output a one to the input of the OR gate. The OR gate will then output a one indicating that they system is unstable for the given case. The same circuit topology can be used to monitor line current flows. A similar comparator circuit can be used for monitoring voltage magnitudes as shown in Figure 46.

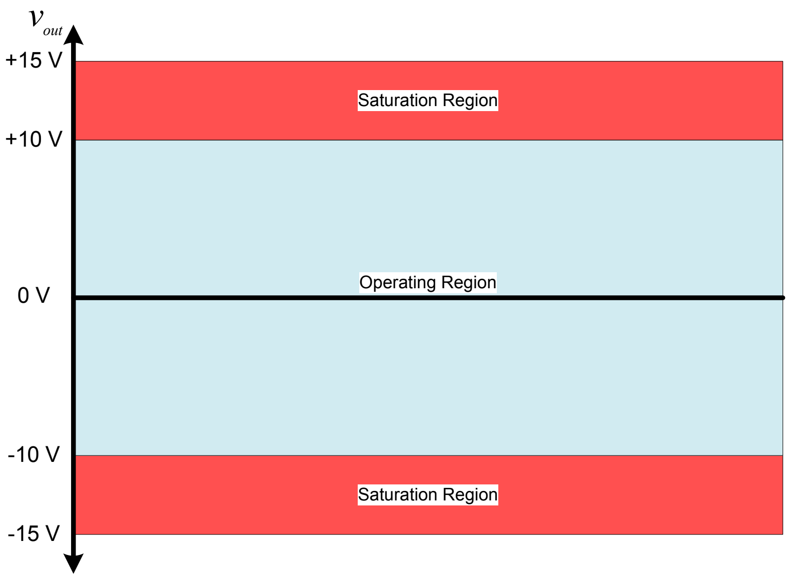


Figure 44: Operating Regions for Second Order Generator Analog Hardware

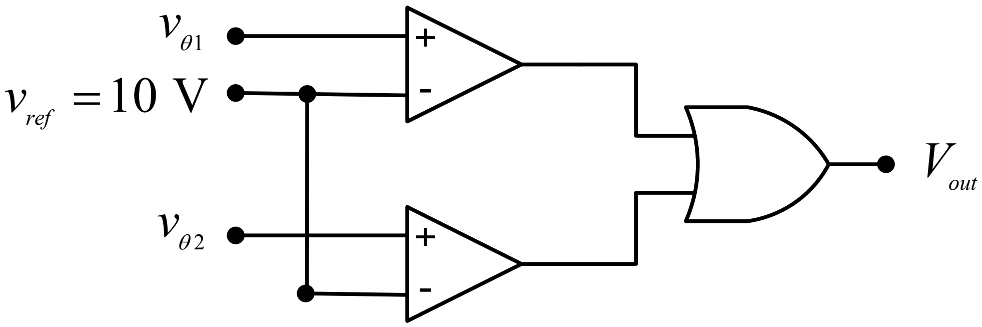


Figure 45: Comparator Circuit

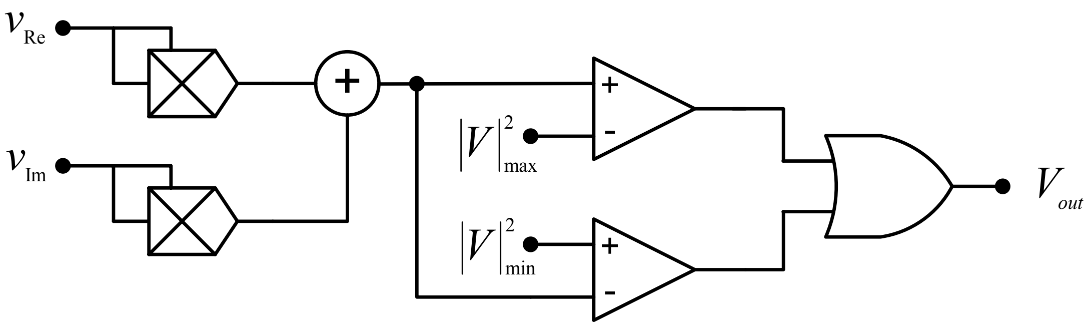


Figure 46: Voltage Magnitude Monitoring Circuit

For the monitoring of voltage magnitude the square of the voltage magnitude can be computed by the following:

$$|V|^2 = v_{Re}^2 + v_{\mathrm{Im}}^2 \tag{5.15}$$

This computation can be done in analog hardware with two multipliers and an adder. It is simpler to compute the magnitude squared as compared to the magnitude. A square root operation is not required. The bus voltage magnitude squared is then compared to both the minimum and maximum values that are predetermined. The circuit will output a one if the voltage is out of range and a zero if the voltage is in range. Many voltage magnitudes can be monitored with one digital flag by chaining the circuits together with multiple OR gates.

For each case emulated only these digital flags require measurement to determine the severity of the case. Cases resulting in overloads or instability can be quickly identified with this technique. Additional measurements can then be taken to further analyze only the dangerous cases. This process results in significant savings in computation time as minimal measurement is required for most contingencies.

5.3 COMPUTATION TIME

The procedure for analog power system security assessment consists of many steps and each must be accounted for to accurately assess computation time. As previously defined the overall computation time consists of the time it takes to configure the emulator, emulate the system, and acquire necessary data. These times are dependent on many factors.

System emulation time is independent of system size. However, configuration and data acquisition are inherently a function of system size. Computation time is also highly dependent on the system architecture. Specifically computation time is dependent on how many A/D and D/A converters are running in parallel, and how many channels the multiplexers and demultiplexers have. In addition, the number of potential topologies and degree of redundancy of data will effect how many cases are to be studied. Likewise the number of contingencies to be computed will alter the computation time. With this in mind the determination of computation time for the presented security assessment procedure is derived in a generic fashion. This derivation is applicable to a variety of cases and hardware configurations.

Computation time is found by assessing the time taken to perform specific operations and enumerating how many times each operation is conducted while performing security assessment. The operations are defined as the time to make one data acquisition $\left(t_{acq1}\right)$, time to configure one device or input $\left(t_{conf1}\right)$, and the time to perform one emulation $\left(t_{emul1}\right)$. For an emulator with one A/D converter it can only acquire one piece of data at a time. If an emulator consists of multiple A/D converters operating in parallel, it can acquire multiple points of data in this time. For simplicity the derivation here enumerates the number of operations required assuming one A/D converter. This value will have to be scaled appropriately for the architecture of the emulator. In a similar fashion multiple devices could be configured with parallel D/A converters. Computation time required for topology identification, input identification, and contingency/stability analysis are enumerated independently here. Total computation time for security assessment is the sum of the time taken for these three processes.

Topology Identification

The process of topology identification requires numerous different configurations of the power system. These configurations consist of different topologies and different inputs to each topology based on the computable sets of data available. The total configuration time for the topology identification process can be quantified by:

$$t_{conf} = n_{comp} \cdot t_{conf1} + \sum_{i=1}^{n_{top}-1} \left(\alpha_i \cdot m_i + \beta_i \right) t_{conf1} \tag{5.16}$$

where

$n_{comp} \triangleq$ the number of components that require configuration for the first topology

$n_{top} \triangleq$ the number of topologies to be tested

$m_i \triangleq$ the number of computable sets of data for topology *i*

$\alpha_i \triangleq$ the number of operations required to configure inputs from one computable set to another

$\beta_i \triangleq$ the number of operations required to configure topology *i* from topology *i-1*

During the topology identification process the system must be emulated for each computable set present for each topology tested. The time for emulation is quantified by:

$$t_{emul} = \sum_{i=1}^{n_{top}} \left(m_i \right) t_{emul1} \tag{5.17}$$

Data must also be acquired for each of these emulations. Specifically the redundant data must be acquired from the emulator. The data acquisition time is quantified by:

$$t_{acq} = \sum_{i=1}^{n_{top}} \left(m_i \cdot DoR_i \right) t_{acq1} \tag{5.18}$$

where

$DoR_i \triangleq$ the degree of redundancy of topology *i*

There are a few places where this process can be optimized to reduce computation time. During configuration the order in which topologies are tested can be arranged such that minimal amount of operations are required to go from one topology to the next. In addition, it may not be necessary to test all computable sets or acquire all the redundant data to eliminate a potential topology. For example, if only a few data sets are run on a given topology but exhibit very poor performance this topology could be eliminated with no further computation. Figure 47 shows the relationship between the number of computable sets tested and the number of computation operations required for a nine bus power system.

For this example, the nine bus test system consists of nine transmission lines, three loads, and three generators. There are a total of seven potential topologies to be tested and a degree of redundancy on data of one, resulting in ten computable sets. It can be seen that the computation operations required increases linearly with the number of computable sets to be tested. Computation operations are defined as the summation of configuration, emulation, and acquisition operations required. Actual computation time will be a linear combination of configuration, emulation, and acquisition operations. By reducing the number of computable sets to be tested, the overall computation time for topology identification decreases proportionally. The next step of the security assessment is input identification.

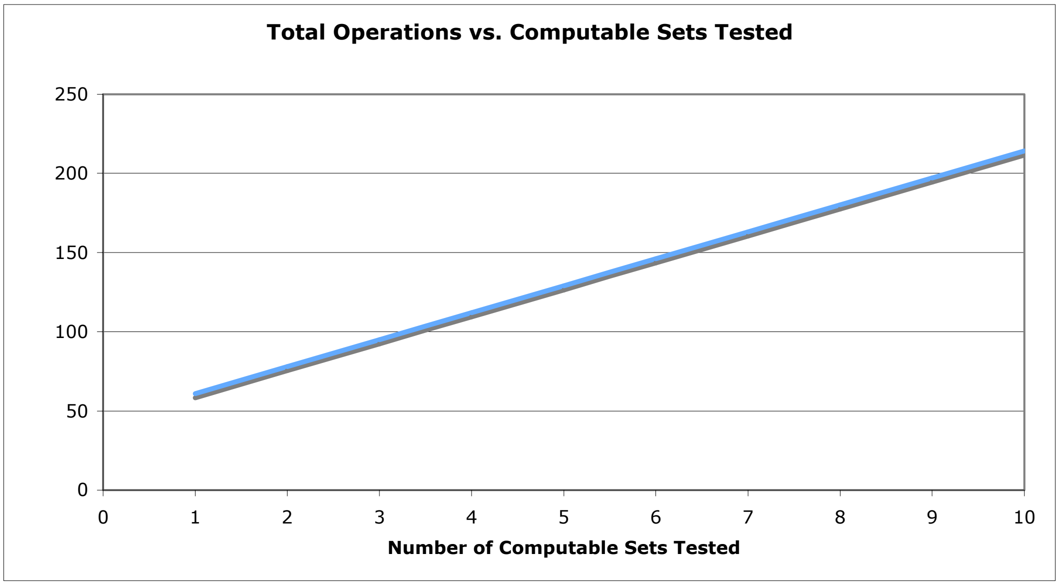


Figure 47: Computation Operations for Topology Identification

Input Identification

The input identification does not require as much configuration as the topology identification. The chosen topology must be reconfigured in the emulator. After this is done the only changes in configuration are the changing of the inputs at each iteration. This configuration time can be quantified by:

$$t_{conf} = \left(n_{reconf} + n_{input} \cdot k\right) \cdot t_{conf1} \tag{5.19}$$

where

$n_{reconf} \triangleq$ the number of operations required to reconfigure the emulator from last tested topology to topology chosen as correct

$n_{input} \triangleq$ the number of inputs to be adjusted for each iteration

$k \triangleq$ the number of iterations in the input identification procedure

The time for emulation is directly proportional to the number if iterations taken:

$$t_{emul} = k \cdot t_{emul1} \tag{5.20}$$

The data acquisition time for input identification is proportional to the number of iterations and degree of redundancy for the chosen topology:

$$t_{acq} = DoR \cdot k \cdot t_{acq1} \tag{5.21}$$

The process of input identification can be sped up by finding a high quality solution in as few iterations as possible. Figure 48 shows the number of computation operations required in relation to the number of iterations performed for input identification. This was determined based on the same nine bus example system used previously. The computation operations required increases linearly with the number of iterations performed. The final part of the security assessment procedure is contingency and stability analysis.

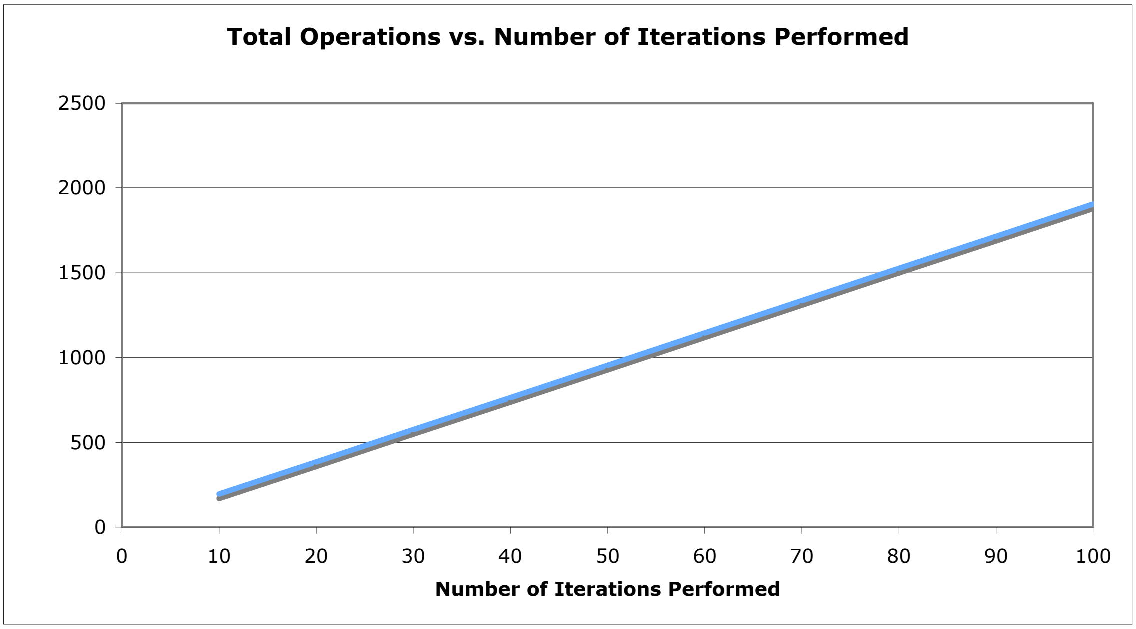


Figure 48: Computation Operations for Input Identification

Contingency and Stability Analysis

The configuration time for the contingency and stability analysis is solely dependent on how many contingencies and faults are to be emulated. No initial configuration is necessary as the system is emulated in the steady-state once input identification is finished. For n-1 contingencies $2n-1$ configurations are required. The initial contingency will require one operation, for example removing a line, while subsequent contingencies will require two operations. The first operation is to restore the component from the prior contingency and the second is to remove the component for the next contingency. When emulating faults one configuration is required per case to configure the faulted condition. The configuration time is quantified as follows:

$$t_{conf} = \left(2n-1\right)\cdot t_{conf1} + n_{fault}\cdot t_{conf1} \tag{5.22}$$

where

$n \triangleq$ the number of contingencies to be emulated

$n_{fault} \triangleq$ the number of faults to be emulated

Emulation time is directly proportional to the number of contingencies and faults emulated:

$$t_{emul} = \left(n + n_{fault}\right)\cdot t_{emul1} \tag{5.23}$$

Data acquisition time is dependent on how many cases to be emulated and how many cases are deemed dangerous and require acquiring more data from the emulator. The data acquisition time is enumerated by:

$$t_{acq} = \left(n + n_{fault}\right)\left(n_{dig} + 2n_{bus}\rho\right) \cdot t_{acq1} \tag{5.24}$$

where

$n_{dig} \triangleq$ the number of digital flags measured per case

$n_{bus} \triangleq$ the number of buses in the power system

$\rho \triangleq$ a number between zero and 1 indicating how many cases are dangerous and require further data acquisition

For $\rho = 1$ all of the cases are dangerous and require data acquisition beyond the digital flags. For $0 < \rho < 1$ only a portion of the cases require further data acquisition. $2n_{bus}$ measurements are required to provide all the states of the power system for a given case. For example, measuring the real and imaginary bus voltages are each bus will provide all the necessary information from the emulator for further analysis. With this information line flows, power injections, etc. can be analyzed.

The computation time required for data acquisition can be reduced if fewer contingencies and/or faults are analyzed and if less information is acquired for the dangerous cases. For example, if a generator exhibits instability for a given case the system operator may not be interested in the profile of the entire system. Acquiring data from the general area where the generator is located may be sufficient to analyze the case.

Figure 49 shows the computation operations required for contingency analysis in relation to the number of contingencies run on the nine bus system. It can be seen that the computation operations increases linearly with the number of contingencies performed. A similar behavior is seen for stability analysis. Figure 50 shows the computation operations required for stability analysis in relation to the number of faults performed. This plot assumes that 10% of the cases are dangerous and require data acquisition beyond the digital flags. The acquisition time changes linearly as the number of dangerous cases changes. The next chapter provides simulation and hardware results that validate this power system security assessment method.

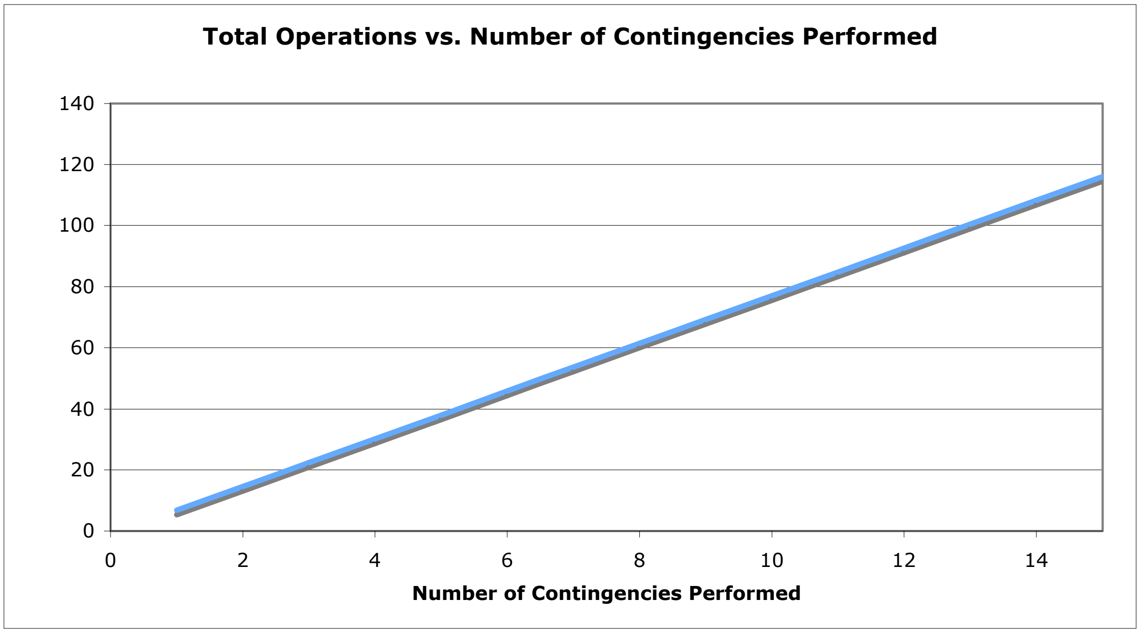


Figure 49: Computation Operations for Contingency Analysis

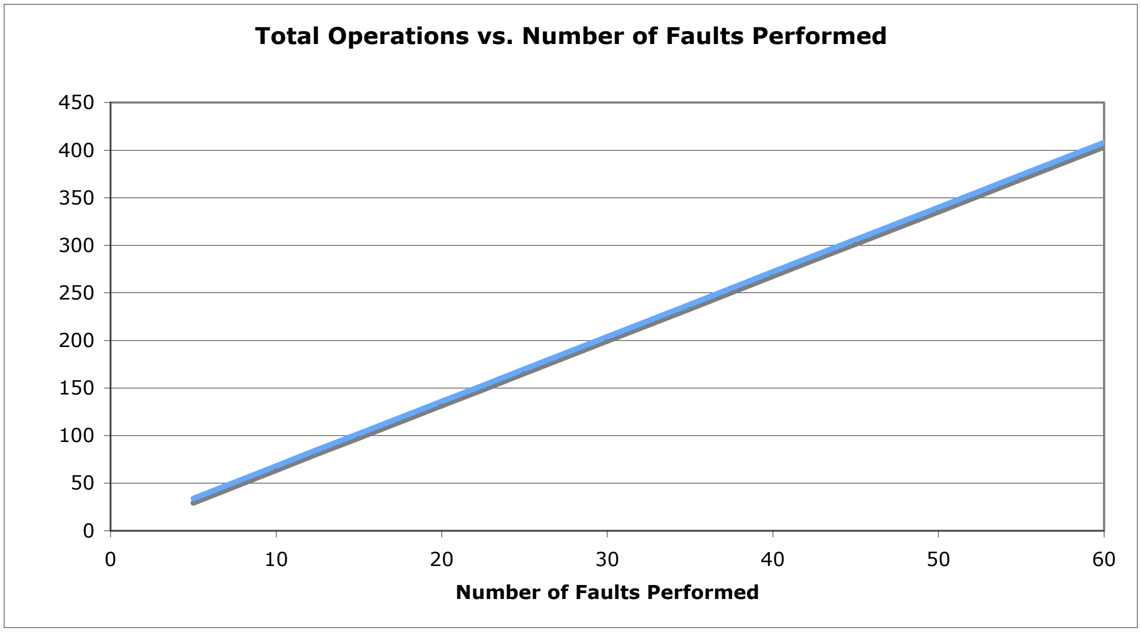


Figure 50: Computation Operations for Stability Analysis

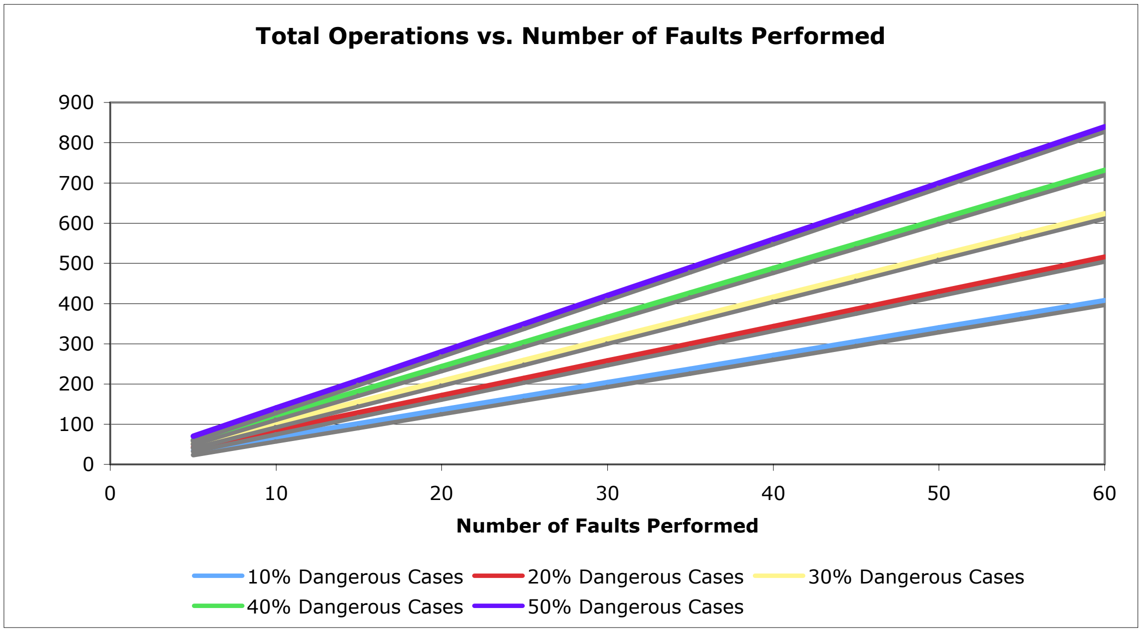


Figure 51: Computation Operations for Various Dangerous Cases

6 EXAMPLES, RESULTS, AND ANALYSIS

6.1 INTRODUCTION

This chapter provides results that verify the proposed method of power system security assessment. Topology identification, including bad data detection and identification, is presented. This is followed by input identification and then contingency and stability analysis. The presented results were obtained through either software simulation of the analog emulator or directly from the prototype power system emulator.

Prior work has shown that the DC emulation method (assuming ideal hardware) is equivalent to AC power flow results for steady-state analysis [63]. With this in mind a digital AC power flow solver was utilized for simulations of cases where steady-state results are required. More specifically, Matpower 3.2 was used [64] in conjunction with MATLAB R2007b [65]. Analog behavior modeling was utilized for simulating the dynamic behavior of the emulator. This technique has been used extensively in the design and benchmarking of the emulator models and techniques [53, 66]. This simulation technique provides emulation results assuming ideal hardware. Based on hardware testing the emulator prototype results are typically within 5% of digital power flow solvers. The errors are due to non-ideal hardware components, noise, and measurement error.

The analog security assessment method was applied to two sample power systems. The first test system is a three bus power system and the second is a nine bus power system. One line diagrams are used to represent these test systems. As stated previously, switches and breakers can be represented in a one line diagram as a line with low or no impedance. The presence of the line in the topology represents a closed switch or breaker, the absence an opened switch or breaker. The three bus power system results are presented next.

6.2 THREE BUS POWER SYSTEM TEST CASE

The one line diagram of the three bus power system is shown in Figure 52. This system consists of two generator buses, one that is a slack bus, a load bus and three transmission lines. The system parameters and base case power flow results can be seen in the appendix. The system parameters are enumerated in Table 29 and the power flow results in Table 33 located in the appendix. The base case results represent the "true" values of the system for these examples.

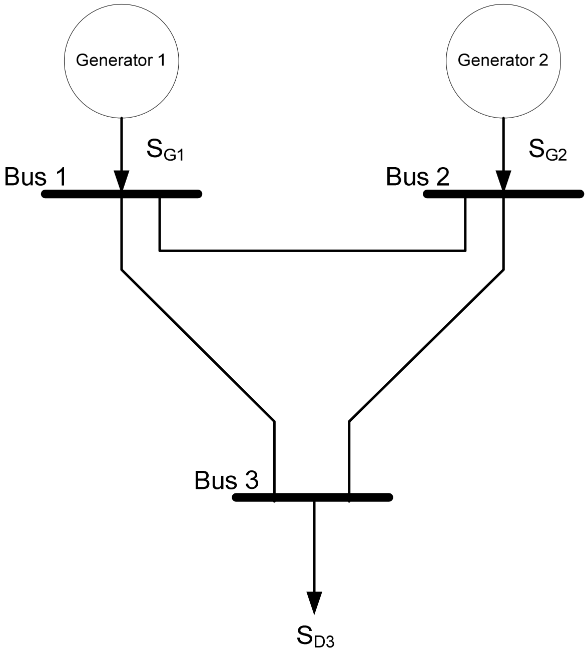
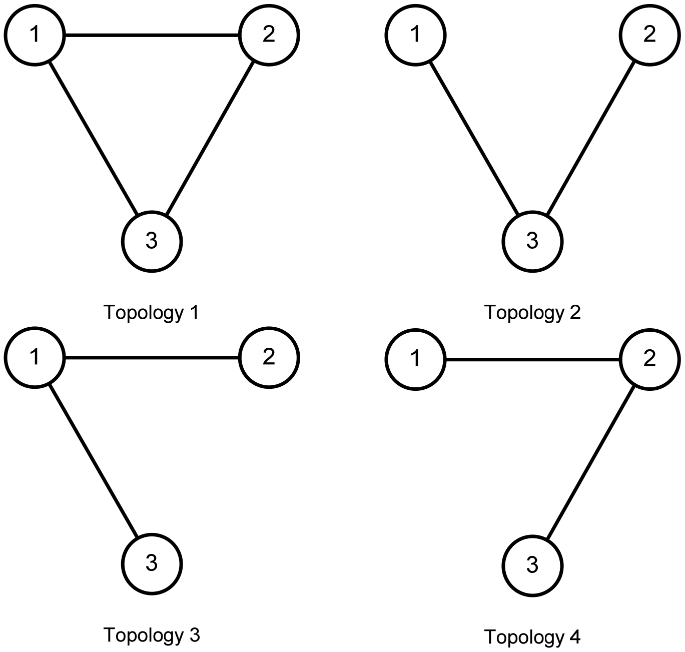


Figure 52: One Line Diagram of Three Bus Power System

The first step of the security assessment procedure is to identify the correct topology. The potential topologies for this system are defined as those topologies that represent a connected power system. The modified Floyd-Warshall algorithm was run on the three bus system graph to identify these topologies. The system graph consists of three vertices and three edges:

$$\begin{aligned} V_{3bus} &= \left\{ v_1, v_2, v_3 \right\} \\ E_{3bus} &= \left\{ v_1 v_2, v_1 v_3, v_2 v_3 \right\} \end{aligned} \tag{6.1}$$

The algorithm identified four potential topologies. These topologies are shown in Figure 53. These topologies were tested with measurement data to determine which topology is correct.



Topology 1

Topology 2

Topology 3

Topology 4

Figure 53: Potential Connected Topologies for Three Bus Power System

All four potential topologies consist of three nodes, or vertices. As a direct result, the topologies have the same requirements for computability. Six inputs are necessary to satisfy steady-state computability requirements for each test. The inputs for testing are obtained from pseudo measurements and measurement data. Measurement data was simulated by adding normally distributed random noise with a given standard deviation to the true values of the system. Table 5 enumerates the true values, measured values and standard deviations of the measurements. For this example it is assumed that the standard deviation of power system measurements and emulation measurements are the same. Real power injections and bus voltage magnitudes are measured for buses one and two. Reactive power injection and bus voltage angle are measured at bus three. The slack bus voltage magnitude is taken as a pseudo measurement and set to one per unit. In addition, the slack bus is taken as the reference point and the voltage angle is set to zero degrees.

With the slack bus angle specified and used as an input to the emulator, only five measurements are required for computability. Six measurements are randomly generated and there is one pseudo measurement for a total of seven. This results in a degree of redundancy of two. Redundant data is only available at bus three resulting in six computable sets of data $\left(C_2^4 = 6\right)$. To keep computation time low it is desirable to test a small subset of all computable sets and still correctly identify the system topology.

The simulation results for this system show that only two of the six computable sets need to be tested in order to accurately identify the correct topology. The correct topology from the base case is topology one in Figure 53. The two test cases used are detailed in Table 6. The inputs on the two generation buses remain constant and the inputs for the load bus are varied from case one to case two. In case one the load is modeled as a PV bus. Q_3 and θ_3 are measured during the test. For the second case the load bus is modeled as a PQ bus. $|V_3|$ and θ_3 are measured.

Table 5: True and Measured Values for Three Bus Example

	True Value	Measured Value		σ
P2	1.630	1.6640	p.u.	0.05
|V2|	1.000	0.9862	p.u.	0.05
P3	2.000	2.0495	p.u.	0.05
Q3	0.750	0.7609	p.u.	0.05
|V3|	0.909	1.0022	p.u.	0.05
θ3	-6.466	-6.7273	degrees	0.50

Table 6: Test Cases for Three Bus Example

Case	Inputs	Measurements
1	|V1|, θ1, P2, |V2|, P3, |V3|	Q3, θ3
2	|V1|, θ1, P2, |V2|, P3, Q3	|V3|, θ3

The simulations results for the four topologies and two cases are enumerated in Table 7. The probability $P(m)$ was computed for each case and the performance index PI computed for each topology. Topology one was chosen correctly as the topology with the lowest PI. Topologies three and four resulted in significantly high performance indices while topology two was closer in performance to topology one. If only one of these cases were run for this example the technique would have still correctly identified topology one as the correct topology. However, the performance indices would have been closer between topologies. Generally speaking, the more cases performed the more discrepancies can be seen between the topologies. This approach to topology selection can also identify bad data.

Table 7: Topology Identification Results for Three Bus Example

Topology	Case 1			Case 2			
	P(m1)	**Q3**	**θ3**	**P(m2)**	**|V3|**	**θ3**	**PI**
1	0.0592	-0.4909	-6.4090	0.2393	0.901	-6.722	21
2	0.0160	-0.5907	-3.0710	0.1054	0.890	-2.867	72
3	0.0001	-0.4898	-14.5590	0.0073	0.814	-16.903	7447
4	0.0000	-0.7431	-30.1980	0.0000	1.358	170.310	> 10E6

For this next example, topology identification for the three bus system was simulated with the presence of bad data. This bad data was specifically a measurement of reactive power at bus three equal to zero $\left(Q_3 = 0\right)$. This can occur in a situation where the meter is not reporting data or if the measurement was missed. The same two cases were simulated for all four topologies with this bad data. The results are listed in Table 8. Bad data is likely to not match any of the topologies and result in a low $P\left(z_i^{meas}\right)$. For this example, bad data was correctly detected by observing that $P\left(z_i^{meas}\right)$ for Q_3 was consistently low across all topologies. $P\left(z_i^{meas}\right)$ is approximately zero for the Q_3 measurement across all four topologies. PI was recalculated once the bad data was identified and removed. PI calculations are shown for good data and bad data. It is interesting to note that regardless of bad data the method identified the correct topology. This can be expected so long as the majority of data is good and all the data used as inputs for a given test case are good. More specifically, there must be enough good data to maintain an adequate degree of redundancy. This allows for a sufficient number of computations to identify the correct topology. For a given power system a minimum DoR could be defined which is necessary for topology identification. This minimum DoR will be specific to the system and set of measurements. Additional examples of topology identification in the presence of bad data are shown in the appendix. This technique easily identifies and eliminates bad data and correctly identifies the topology. In some cases the correct topology is identified with the presence of bad data. Further investigation is required to analyze the robustness of the technique with bad data. Inherently there are some limitations and aspects to consider for bad data detection with this technique.

First and foremost, to correctly identify bad data it must be one of the measurements for a given topology test. To scan all measurements for bad data it is required to select the test cases appropriately. In addition, once bad data is identified and removed the degree of redundancy and number of computable sets decreases. If the current topology identification problem has a low DoR and bad data exists it may be difficult to identify the correct topology. One topology identification test has been presented in detail and properly identified the correct topology. To analyze the robustness and repeatability of this topology identification procedure, one hundred topology identification tests were performed on the three bus system with randomly generated measurement data for each case.

Table 8: Three Bus Topology Identification Results in the Presence of Bad Data (Q3=0)

Topology	**Case 1**			**Case 2**				
	P(m1)	**Q3**	**θ3**	**P(m2)**	**|V3|**	**θ3**	**PI (bad data)**	**PI (good data)**
1	0.0590	-0.4909	-6.4060	0.6179	0.965	-6.494	18.56	3.16
2	0.0000	-0.5907	-3.0680	0.4730	0.957	-2.962	> 10E6	> 10E6
3	0.0000	-0.4898	-14.5530	0.3523	0.939	-15.186	> 10E6	> 10E6
4	0.0000	-0.7431	-30.1980	0.0074	0.815	-35.482	> 10E6	> 10E6

Measurement data was randomly generated for each of the one hundred tests performed. This data can be seen in Table 39 located in the appendix. The same standard deviations and test cases were utilized when performing these tests. The results of the simulations are enumerated in Table 40. The correct topology was identified in 80% of the cases. Topology two was incorrectly chosen six times and topology three was incorrectly identified as the topology 14 times. However, in most of these cases when a topology is chosen incorrectly there are multiple topologies with very low performance indices. This is indicative that the results may be questionable. One way to improve the results is to run more test cases on computable sets of data. A quicker technique that requires no further testing was found while scanning for bad data.

For this example the $P(m)$ for reactive power on bus three was consistently low for all 100 runs. This is picked up by the algorithm as the presence of bad data. While there is not bad data present in these cases these results show that the reactive power injection at this bus is very sensitive to other factors. This comes through in the results as a very low $P(m)$. Since this $P(m)$ is very low for all cases it can be disregarded as bad data or an unreliable result. This data was removed and the performance indices recalculated for all 100 runs. These filtered results are shown in Table 41. Topology one was selected as the correct topology for 100% of the runs. In addition, there was a minimum of an order of magnitude difference between the performance index of topology one and any other topology performance index. This technique has worked well for this three bus case in these simulation results. However, these simulation results do not factor in the presence of noise at the inputs of the emulator or noise on the measurements from the emulator. The power system measurements are taken explicitly as inputs to the simulation and the power flow results are taken as measurements from the simulation. The next examples examine the effects of both input noise and measurement noise from the emulator.

The same tests were performed again on the three bus system for 100 runs. In these tests randomly generated noise was added to the inputs of the emulator (power flow simulator). The noise had a zero mean and standard deviation of 0.05 for voltage (in per unit) and power (in per unit) measurements and 0.5 for angle measurements in degrees. These simulations analyze the robustness of the technique in the presence of noise on the emulator inputs. The results are enumerated in Table 42. In the presence of this noise the correct topology was identified in 98% of the cases. In the two cases where topology one was not chosen the performance indices of multiple topologies were very low. Due to the nature of the performance index a large discrepancy between indices from the correct topology and an incorrect topology is expected. With this property instances where multiple topologies exhibit low performance indices, or indices that are relatively close to each other, can be labeled as suspect, or questionable. Some more simulations were performed to analyze this property.

Two more sets of 100 simulations were performed. More specifically, the two test cases were tested separately with randomly generated input noise. The results for case one is shown in Table 43 and case two in Table 44. These results show the performance indices for each of the 100 simulations. These tables are located in the appendices. The results of these tests and the original test with both cases are tabulated in Table 9.

As stated previously, when both test cases were run the correct topology was identified 98% of the time. For the cases where topology one was not chosen, the PI for topology one was low and very close to the PI of the topology that was selected. When both test cases were run only 4% of the results were questionable (multiple PI within an order of magnitude). In addition, all of the incorrectly identified topology tests were identified as questionable. When only analyzing one case the topology identification process did not perform as well.

When only test case two was performed the process correctly identified the topology in 97% of the tests. However, 62% of the results were flagged as questionable. When examining only test case one the correct topology was identified in 78% of the tests while only 6% of the results were questionable. This performance will vary from system to system and case by case. However, more test cases will generally result in more reliable topology identification and less questionable results. In addition, by identifying questionable results a user can determine if more test cases are required to gain confidence in the results. Overall the performance of the topology identification technique improves when more cases are analyzed and is robust enough to handle noise on the input to the emulator. Another set of runs were simulated to analyze the effect of emulation measurement noise.

Table 9: Topology Identification Results for Three Bus System

Cases Run	Topology Identification		
	Correct	Incorrect	Questionable
1,2	98%	2%	4%
1	78%	22%	6%
2	97%	3%	62%

In prior simulation results the value achieved from the power flow solver was used as the measurement value from the emulator. In other words emulator measurement noise is neglected. The last set of 100 simulations for the three bus system incorporated both input noise and outputs noise of the emulator. It was assumed that the noise on the input is uncorrelated to the noise on the output. In physical terms this assumes that errors on the input are caused solely by the actuation circuitry and the measurement error is due to measurement circuitry. Random noise was added to the power flow results to simulate measurement error. The noise added had a zero mean and standard deviations of 0.05 for voltages and power and 0.5 for angles. The results for these simulations are shown in Table 45. The correct topology was chosen for all 100 runs. In addition, no cases were flagged as questionable. The technique has exhibited strong performance in the presence of noise.

Once the correct topology of a power system is chosen, two out of the three requirements for steady-state system emulation in theorem 1 are satisfied. The functional description of the system is known from the topology and component models. In addition, the requirement of computability in steady-state has already been satisfied during the topology identification process. Determining the correct inputs is all that remains. The inputs to the emulator are determined through the input identification process. This process is presented next. It is assumed that the measurement data provided is synchronized. In application, the telemetered data should be time stamped to allow for this synchronization.

For the three bus system, topology one and case two were taken as the starting point for input identification. This test case exhibited the highest $P(m)$. $P(m)$ was computed as 0.8577 for this case. Two different methods were utilized to determine the inputs to the emulator. The first was a Monte Carlo type process the second was the heuristic process described in chapter 5. For the Monte Carlo process the inputs were randomly generated by adding normally distributed noise to the inputs from case two. Five hundred runs were conducted with varying standard deviations for the random noise. The standard deviations were varied from 0.5 to 0.0001. The best results were obtained with $\sigma_P = \sigma_Q = \sigma_V = 0.001$. $P(m)$ was improved to 0.8636 from the starting point. Heuristics were used as a different approach to identifying the inputs.

The largest discrepancy from case two results and the measurements was with bus three voltage. That resulted in the smallest $P(z_i)$. In order to improve the results it would be desirable to increase this voltage. In order to do this the load reactive power Q_3 could be lowered, the bus voltage V_2 could be raised, and the load real power P_3 could be lowered. Specifically for this example alpha was chosen as 0.001 and the direction matrix entries for V_2 was one and negative one for Q_3 and P_3. In less than ten iterations $P(m)$ was improved to a level slightly better than that achieved with the Monte Carlo method. The results are detailed in Table 10.

Table 10: Input Identification Results for Three Bus System

	Inputs						Measurements		
	V1	θ1	V2	P2	P3	Q3	V3	θ3	P(m)
Starting Point	1.000	0.000	0.9862	1.6640	2.0495	0.7610	0.9010	-6.7220	0.8577
Monte Carlo	1.000	0.000	0.9864	1.6644	2.0495	0.7606	0.9027	-6.7147	0.8636
Heuristics	1.000	0.000	0.9863	1.6640	2.0494	0.7610	0.9010	-6.7225	0.8648

The inputs were not changed that drastically from the starting point. The starting already represented a decent estimate of the power system for this case. For benchmarking purposes the results obtained here were compared to that of a weighted-least-squares method of state estimation as outlined in chapter 2. POWERGEN software [3] was utilized to perform state estimation on the three bus system. The simulated results of the analog method are compared to the WLS state estimation results and the true values in Table 11. For the most part the results are pretty comparable. However, with the proposed analog technique the reactive power injections at bus one and bus two were much closer to the true values as compared to the WLS estimation procedure. Table 12 shows a comparison of the measurement residuals computed for the WLS estimation and the analog methods. The overall residuals were fairly close to one another. The main difference between the techniques was seen on the residual for bus three voltage magnitude. The analog techniques exhibited a higher residual than the WLS method. However, the analog techniques provided a bus voltage magnitude closer to the true value. The inputs identified are taken as the correct inputs to the power system emulator. All the requirements for steady-state system emulation from theorems 1 and 2 have been satisfied. The next step is to emulate the power system in steady-state and perform contingency and stability analysis.

Table 11: Input Estimation Results Comparison for Three Bus System

	Monte Carlo	Heuristic	WLS	True Value
$\lvert V1 \rvert$	1.0000	1.0000	1.0000	1.0000
θ1	0.0000	0.0000	0.0000	0.0000
$\lvert V2 \rvert$	0.9864	0.9863	1.0237	1.0000
θ2	6.4765	6.4690	6.2020	6.4690
$\lvert V3 \rvert$	0.9027	0.9010	0.9186	0.9090
θ3	-6.7147	-6.7225	-6.5810	-6.4660
P1	0.4179	0.4200	0.4352	0.4200
Q1	0.7910	0.7900	0.6052	0.7900
P2	1.6644	1.6640	1.6637	1.6300
Q2	0.4653	0.4640	0.6598	0.4640
P3	2.0495	2.0494	2.0477	2.0000
Q3	0.7606	0.7610	0.7535	0.7500
P(m)	0.8636	0.8648	x	x

Table 12: Measurement Residual Comparison for Three Bus System

	Monte Carlo	Heuristic	WLS
P2	0.0001	0.0000	0.0000
$\lvert V2 \rvert$	0.0000	0.0000	0.5625
P3	0.0000	0.0000	0.0013
Q3	0.0000	0.0000	0.0219
$\lvert V3 \rvert$	3.9617	4.0966	2.7956
θ3	0.0006	0.0001	0.0856
J(x)	3.9624	4.0967	3.4669

The contingency and stability analysis process was verified by simulating the analog emulator in PSpice and comparing the results to numerical integration methods. In order to satisfy the requirements for dynamic system emulation, as outlined in theorems 1 and 3, the steady-state emulation operating point is taken as initial conditions. The other inputs to the emulator are dictated by the contingency to be tested. In addition, the time duration to be emulated is specified as the time it takes for the emulator to converge to a solution or exhibit instability. These components satisfy the requirement for correct inputs to the emulator for dynamic system emulation. The functional description and computability requirements have already been satisfied.

The integration results were obtained using the true values of the system. When compared to the emulation results, this comparison will show how close the results from the proposed analog method will match computations based on the actual system states. Contingency and stability analysis was performed for the loss of each transmission line (one at a time). In addition, stability analysis was conducted on a ground fault at bus two. The purpose of this analysis was to identify the critical clearing time of the fault in order to maintain system stability.

The first contingency was performed on transmission line one. This transmission line connects buses one and two. The system was stable for this contingency for both the emulator simulation and integration results. The steady-state values are enumerated in Table 13 for the emulator results and Table 14 for the integration results. The emulation results are very close to the integration results. The voltage magnitudes are within 0.01 per unit, angles within 0.4 degrees, real power values within 0.034 per unit, and reactive power values within 0.077 per unit. The system dynamics were also very comparable.

The generator angle swing for both techniques is plotted for comparison in Figure 54. The response obtained from the security assessment approach is tracks the true value very closely. In addition, the load dynamics are also compared. The load voltage magnitude is shown in Figure 55 and the load voltage angle in Figure 56. Qualitatively the security assessment results match the true value results. Quantitatively there is some difference due to the steady-state emulation values differing from the true values. This slight deviation was expected and the results are comparable. Contingencies were also performed on the other two lines. The contingency for line two resulted in instability. Results for the line three contingency are similar and can be seen in the appendix. Next, a fault was simulated at bus two.

Table 13: Three Bus System Analog Security Assessment Results for Line One Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.458	0.876	0.000	0.000
2	0.986	16.956	1.664	0.618	0.000	0.000
3	0.890	-3.030	0.000	0.000	2.050	0.761

Table 14: Three Bus System Numerical Integration Results for Line One Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.438	0.799	0.000	0.000
2	1.000	16.583	1.630	0.631	0.000	0.000
3	0.900	-2.737	0.000	0.000	2.000	0.750

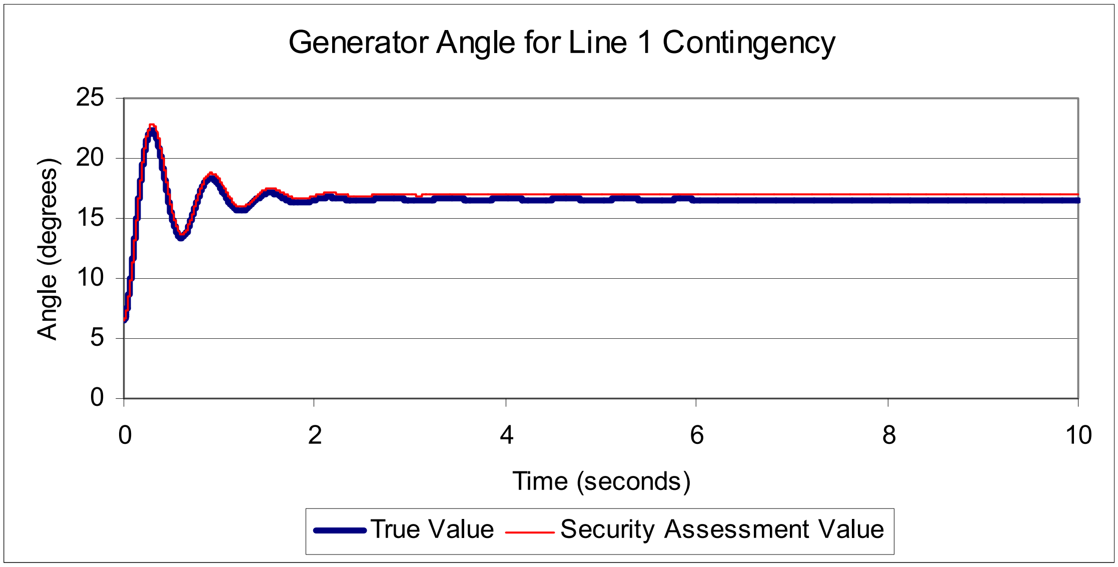


Figure 54: Three Bus System Generator Two Angle for Line One Contingency

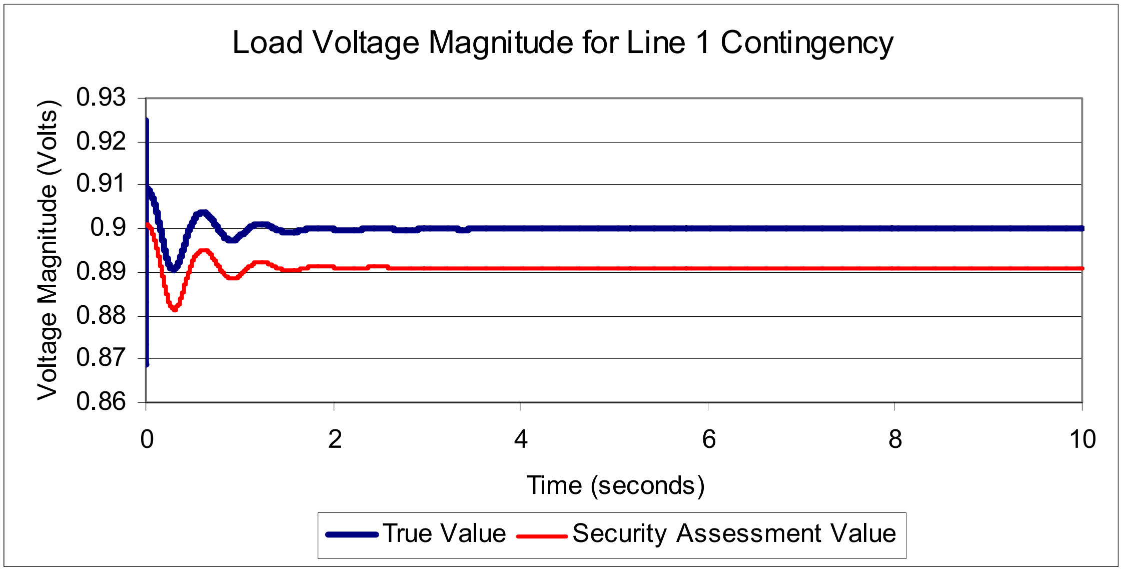


Figure 55: Three Bus System Load Voltage Magnitude for Line One Contingency

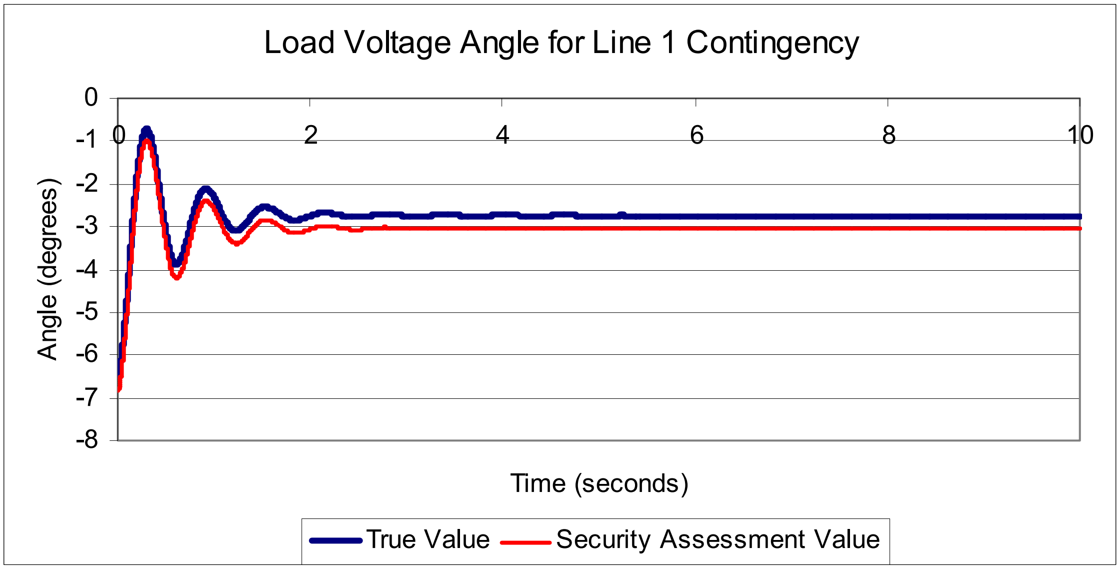


Figure 56: Three Bus System Load Voltage Angle for Line One Contingency

A three phase ground fault at the generator terminals was simulated. Multiple fault durations were analyzed in order to find the instability point of the system for such a fault. The instability point was defined as the minimum fault time duration which resulted in system instability. This point is often referred to as critical clearing time. The fault must be cleared from the system before this time in order to maintain stability. This clearing time was determined to be 208 ms for the true values of the system and 204 ms for the analog emulator results. The slight difference is due to the different initial conditions and inputs to the system. The response of the system in emulation, for both unstable and stable cases, is very close to the true values. Figure 57 shows the generator angle results for the fault duration equal to the critical clearing time. The next example tests the proposed method of security assessment on the prototype power system emulator.

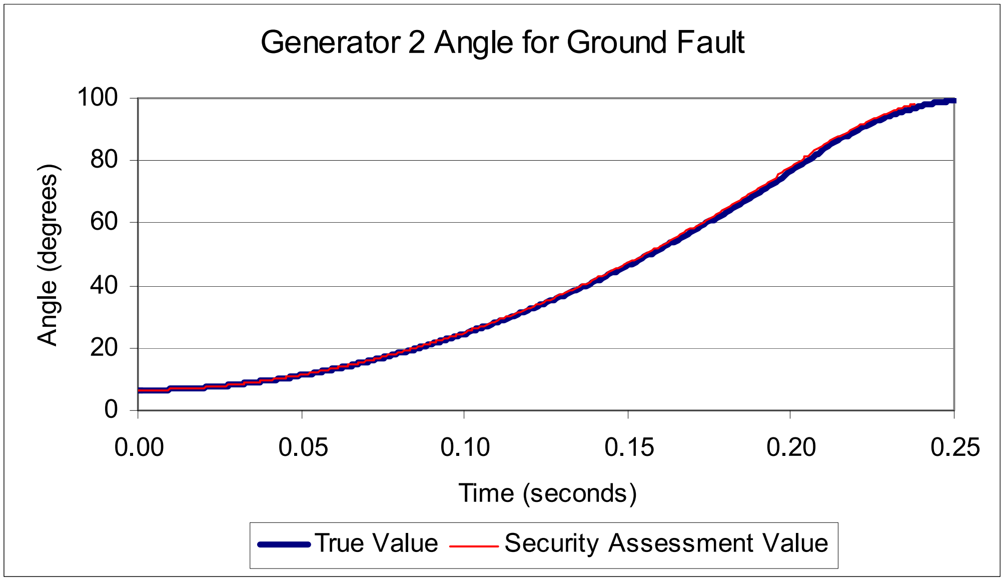


Figure 57: Three Bus System Generator Angle for Ground Fault

A three bus power system was constructed and tested in hardware to verify the proposed method for power system security assessment. Two examples of security assessment in hardware are presented here. The two examples are similar to the prior simulation example and satisfy the requirement for steady-state and dynamic system emulation in the same fashion. For the first example, the system parameters are enumerated in Table 30 and the base case power flow results in Table 34. Both tables are located in the appendix. For the purpose of topology identification the same four topologies were tested using the same two test cases outlined previously. In a similar fashion random measurement data was generated by adding zero mean random noise to the true values obtained from the base case load flow. The true and measured values are enumerated in Table 15.

Table 15: True and Measured Values for Three Bus System I Hardware Testing

	True Value	Measured Value		σ
P2	2.000	2.0164	p.u.	0.05
|V2|	1.050	1.0563	p.u.	0.05
P3	2.500	2.4907	p.u.	0.05
Q3	1.000	1.0363	p.u.	0.05
|V3|	0.875	0.8577	p.u.	0.05
θ3	-10.230	-9.6345	degrees	0.50

The emulator was run for all topologies and test cases. The results are tabulated in Table 16. Topology one exhibited the lowest performance index and was selected correctly as the topology of the power system. A performance index could not be computed for topologies three or four. These topologies exhibited instability during testing. An equilibrium point could not be achieved for either of the two test cases. This behavior is indicative of the topologies not matching the power system data. As a result these topologies were discarded as incorrect. In addition, topology identification was performed in the presence of bad data.

Table 16: Topology Identification Results for Three Bus System I in Hardware

Topology	Case 1			Case 2			
	P(m1)	Q3	θ3	P(m2)	|V3|	θ3	PI
1	0.6077	1.0700	-10.3900	0.8906	0.864	-10.130	2.77
2	0.0384	0.8900	-4.1200	0.6720	0.834	-3.740	27.55
3	x	x	x	x	x	x	x
4	x	x	x	x	x	x	x

For the purpose of performing topology identification in the presence of bad data the reactive power injection measurement at bus three was set to zero. The topology tests were preformed with this bad data. The results are shown in Table 17. The bad data was easily identified and removed. For test case one, topologies three and four exhibited instability. In test case two these topologies were stable. However, the results deviated from the measurement substantially resulting in very high performance indices. In addition, topology two had very high performance indices with or without the bad data. Topology one was easily selected as the correct topology, even with the bad data present. Similar results were obtained with bad data for θ_3. Next, input identification and contingency analysis were performed on topology one.

Table 17: Topology Identification Results for Three Bus System I in Hardware with Bad Measurement Data

Topology	Case 1			Case 2				
	P(m1)	Q3	θ3	P(m2)	|V3|	θ3	PI (bad data	PI (good data)
1	0.0259	1.3000	-10.8700	0.8906	0.983	-8.710	39.67	4.63
2	0.0000	1.1600	-3.7000	0.6720	0.965	-3.420	> 10E6	> 10E6
3	x	x	x	0.3588	0.918	-24.110	> 10E6	> 10E6
4	x	x	x	0.5739	0.892	-40.430	> 10E6	> 10E6

Test case two exhibited the highest $P(m)$ for topology one during topology identification. This was used as the starting point for input identification. Different direction matrices and values of α were tested. However, no discernable increase in $P(m)$ was obtained during this process. This is due mainly to the presence of noise in the emulator. From the simulation results an increase in $P(m)$ was only seen very close to the starting point. The result from the best test case in the topology identification process is taken as the operating point of the power system. It has been shown in simulations that the inputs change very little in obtaining a larger $P(m)$. Within hardware limitations this is the best result obtained for this case and is a close approximation of the system states.

The results are compared with the true values and values obtained from WLS in Table 18. The results obtained from the analog technique are fairly close to the true values and comparable to the WLS method. A residual comparison between the analog method and WLS is shown in Table 19. The analog technique exhibited a slightly lower residual than the digital WLS technique. Contingency analysis was then performed using the operating point achieved from the identified inputs as initial conditions.

Table 18: Input Estimation Results Comparison for Three Bus System I in Hardware

	Emulation	WLS	True Value
|V1|	1.0000	1.0000	1.0000
θ1	0.0000	0.0000	0.0000
|V2|	1.0563	1.0493	1.0500
θ2	6.2200	6.3540	6.1800
|V3|	0.8640	0.8699	0.8750
θ3	-10.130	-10.154	-10.230
P2	2.0164	2.0165	2.0000
Q2	1.3500	1.2561	1.3100
P3	2.4907	2.4911	2.5000
Q3	1.0363	1.0377	1.0000
P(m)	0.974	x	x

Table 19: Measurement Residual Comparison for Three Bus System I in Hardware

	Emulation	WLS
P2	0.0000	0.0000
|V2|	0.0000	0.0196
P3	0.0000	0.0001
Q3	0.0000	0.0008
|V3|	0.0159	0.0595
θ3	0.9821	1.0795
J(x)	0.9980	1.1595

Contingencies were performed on each transmission line of the three bus system. The generator and load responses were monitored to evaluate the stability and security of the system. The system maintained stability for the line one contingency. The response of the generator angle is plotted and compared to numerical integration results in Figure 58. The analog hardware was running at approximately 2500 times faster than real time. The x-axis on the plots were scaled appropriately for comparison purposes. The hardware results exhibit some offset errors, but overall track the integration results closely. Contingencies on transmission lines two and three resulted in instability. The response of the generator angle for a line two contingency is shown in Figure 59. The generator quickly loses stability. In the case of the line three contingency the generator maintained stability. However, the load went unstable and exhibited voltage collapse. These results are plotted in Figure 60. Overall the results obtained from the emulator are similar to those achieved by simulation of the emulator and validate the proposed method of security assessment. One final example is presented to show a specific case where multiple topologies can perform similarly in the topology identification process.

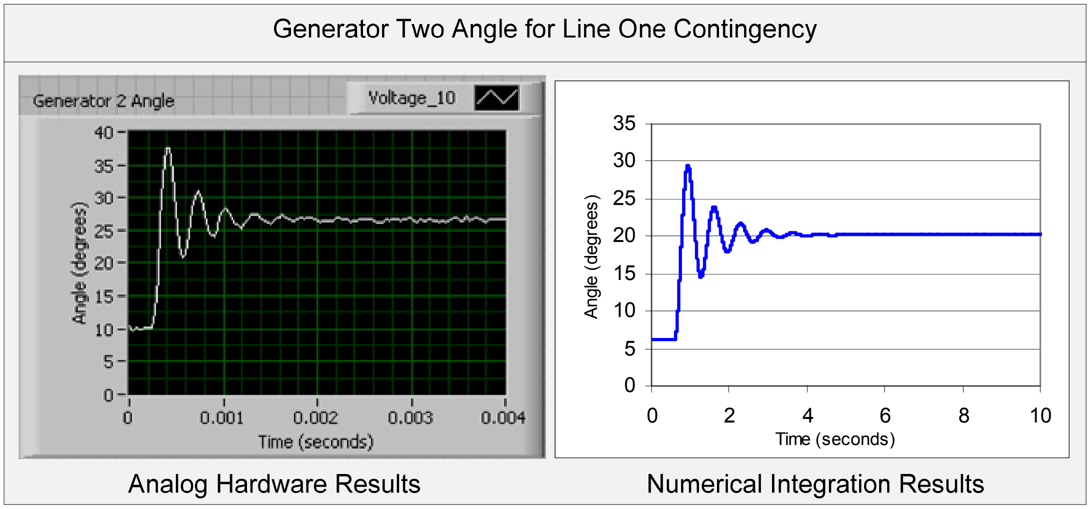


Figure 58: Three Bus System I in Hardware Generator Angle for Line One Contingency

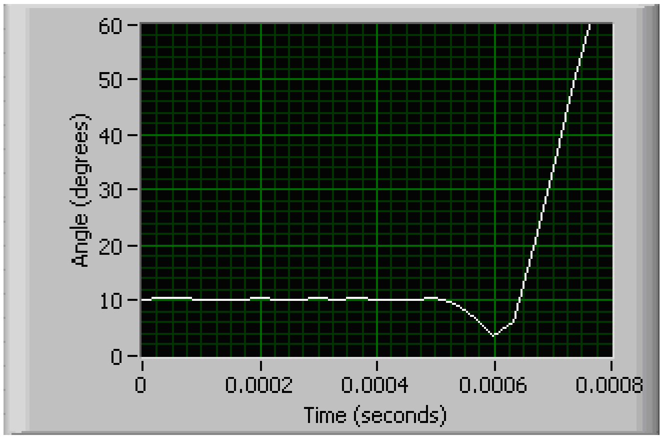
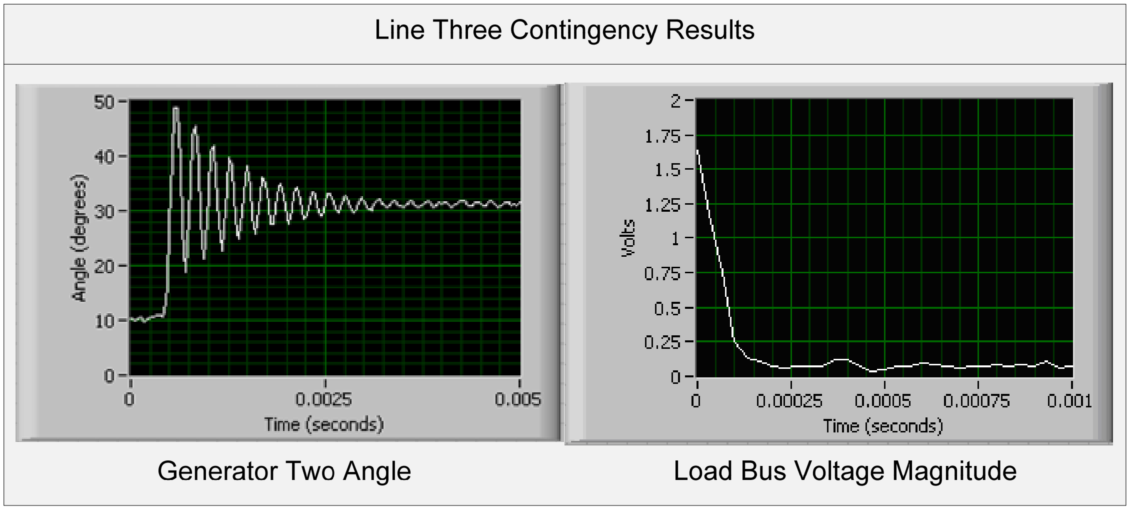


Figure 59: Three Bus System I in Hardware Generator Angle for Line Two Contingency



Line Three Contingency Results

Generator Two Angle

Load Bus Voltage Magnitude

Figure 60: Three Bus System I in Hardware Line Three Contingency Results

The topology testing and identification process essentially tests multiple topologies and compares their associated electrical characteristics to the data obtained from the power system. The topology which behaves, electrically speaking, most like the real power system is chosen as the correct topology. The process has been shown to be robust in selecting the correct topology. However, when two or more topologies exhibit similar electrical performance it can be hard to discern between the two with this technique. One such example, as shown here, would be when a transmission line is very lightly loaded.

The topology identification process was performed with the analog emulator for a case with a very lightly loaded transmission line. The same three bus system was tested. The transmission line connecting buses one and two is the lightly loaded line. The parameters of the system can be seen in Table 31 and the base case load flow in Table 35.

The same testing process was performed for identifying the system topology. Table 20 enumerated the true and measured values of the system. The results from the topology testing are shown in Table 21. Topologies three and four were easily discarded with extremely large performance indices. However, topologies one and two both performed very well and a correct topology cannot be easily identified. Electrically speaking topologies one and two are very similar. More testing could be performed to try and clearly discern which topology is correct. Another approach would be to perform contingency and stability analysis on both topologies and act accordingly based on the results. The assumption would be that the system is in one of these topological states.

Table 20: True and Measured Values for Three Bus System II Hardware Testing

	True Value	Measured Value		σ
P2	1.000	0.9287	p.u.	0.05
|V2|	1.000	1.0234	p.u.	0.05
P3	1.500	1.4819	p.u.	0.05
Q3	0.500	0.4508	p.u.	0.05
|V3|	0.899	0.9084	p.u.	0.05
θ3	-6.012	-6.2386	degrees	0.50

Table 21: Topology Identification Results for Three Bus System II in Hardware

Topology	**Case 1**			**Case 2**			
	P(m1)	**Q3**	**θ3**	**P(m2)**	**|V3|**	**θ3**	**PI**
1	0.5364	0.4040	-6.4100	0.8543	0.922	-6.320	3.03
2	0.4913	0.4030	-5.6400	0.7992	0.922	-5.510	3.29
3	0.0000	0.0150	-14.7300	0.2231	0.826	-13.920	> 10E6
4	0.0000	0.0120	-31.6200	0.0832	0.789	-31.570	> 10E6

This last example has identified one shortcoming of the proposed method of topology identification. However, multiple topology identifications were performed for different loading conditions and different measurement variances and generally speaking the proposed technique performed well. Even with fairly large power system measurement errors. In addition, it was noted that the analog technique performed especially well in moderate to heavily loaded conditions. This behavior is due primarily to the dynamic emulation of the system. In heavily loaded cases some topologies actually exhibited instability. Assuming the actual power system is at a stable operating point these topologies can be discarded as incorrect topologies. In the next section simulation results for security assessment are presented for a nine bus power system.

6.3 NINE BUS POWER SYSTEM TEST CASE

The next example system used was a nine bus system. Security assessment simulation results for the nine bus system are presented here. The system consists of three generators, three loads, and nine transmission lines. The one line diagram for the system is shown in Figure 61. The system parameters are shown in Table 32 and the base case power flow results shown in Table 35. These tables are located in the appendix. The base case results are taken as the true values of the system and the configuration in Figure 61 as the correct topology. For topology identification the potential topologies were first identified.

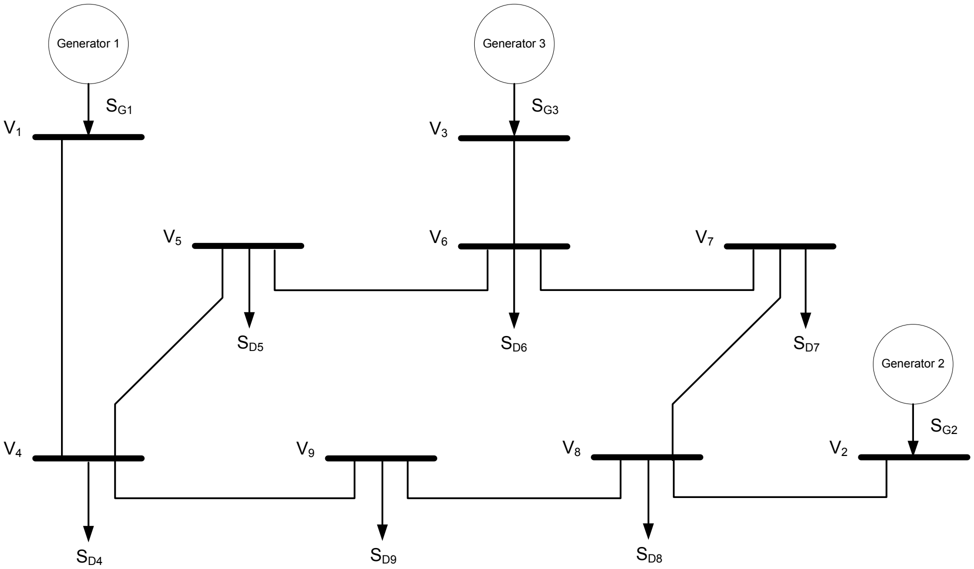


Figure 61: One Line Diagram of Nine Bus Power System

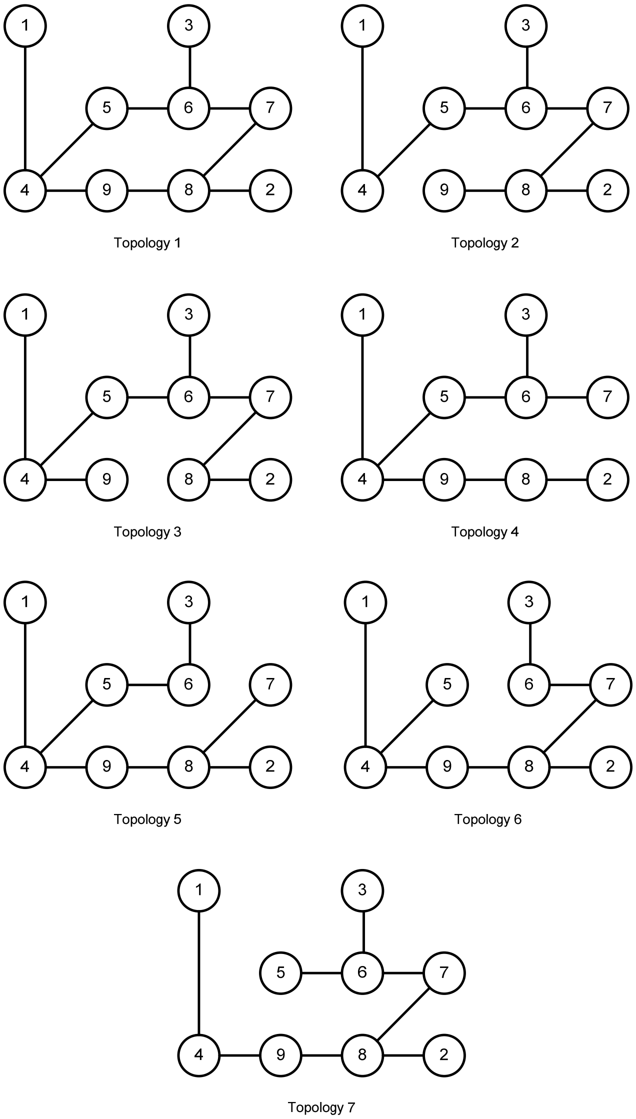
The Floyd-Warshall algorithm was run on the nine bus system graph. The system graph consists of nine vertices and nine edges:

$$\begin{aligned} V_{9bus} &= \left\{ v_1, v_2, v_3, v_4, v_5, v_6, v_7, v_8, v_9 \right\} \\ E_{9bus} &= \left\{ v_1v_4, v_2v_8, v_3v_6, v_4v_5, v_4v_9, v_5v_6, v_6v_7, v_7v_8, v_8v_9 \right\} \end{aligned} \tag{6.2}$$

The algorithm identified seven potential topologies as shown in Figure 62. All seven topologies consist of nine nodes. As a direct result, the topologies have the same requirements for computability. Eighteen inputs will be required to satisfy steady-state computability requirements for each test. The inputs for testing are obtained from pseudo measurements and measurement data. These topologies were tested to determine which topology is correct.

Measurement data was simulated by adding normally distributed random noise with a given standard deviation to the true values of the system. Table 22 enumerates the true values, measured values, and standard deviations of the measurements. For this test case the standard deviations of the emulator measurements are the same as the power system measurements. The slack bus voltage magnitude is taken as a pseudo measurement and set to one per unit. In addition, the slack bus is taken as the reference point and the voltage angle is specified as zero degrees. Pseudo measurements are taken as $P = Q = 0$ for power injections at buses without any generation or load. Computability is determined based on the available measurements.

For this system eighteen inputs are required for computability for all connected topologies. In this example, 23 total measurements are available resulting in a degree of redundancy of six. Redundant measurements are present at buses five, seven, and nine. The result is a total of 216 computable sets of data. Similar to the previous example, it is not necessary to use all of these sets to determine the correct topology and desirable to test as few sets as possible to keep computation time low. For this example seven sets of computable data were used to identify the topology. The seven test cases are detailed in Table 23.



Topology 1

Topology 2

Topology 3

Topology 4

Topology 5

Topology 6

Topology 7

Figure 62: Potential Topologies for Nine Bus System

Table 22: True and Measured Values for Nine Bus Example

	True Value	Measured Value		σ
P2	1.6300	1.63294411	p.u.	0.01
|V2|	1.0000	1.00125332	p.u.	0.01
P3	0.8500	0.85714325	p.u.	0.01
|V3|	1.0000	0.98853529	p.u.	0.01
P5	0.9000	0.91254001	p.u.	0.01
θ5	-4.0170	-4.00826804	degrees	0.05
|V5|	0.9750	0.97827292	p.u.	0.01
Q5	0.3000	0.28406270	p.u.	0.01
P7	1.0000	0.99600114	p.u.	0.01
θ7	0.6220	0.73115929	degrees	0.05
|V7|	0.9860	0.98011683	p.u.	0.01
Q7	0.3500	0.35689997	p.u.	0.01
P9	1.2500	1.26290250	p.u.	0.01
θ9	-4.3500	-4.34703593	degrees	0.05
|V9|	0.9580	0.96866768	p.u.	0.01
Q9	0.5000	0.50668601	p.u.	0.01

Table 23: Test Cases for Nine Bus Example

Case	Inputs	Measurements
1	|V1|, θ1, P2, |V2|, P3, |V3|, P5, Q5, P7, Q7, P9, Q9	|V5|, θ5, |V7| ,θ7, |V9|, θ9
2	|V1|, θ1, P2, |V2|, P3, |V3|, P5, Q5, P7, Q7, P9, |V9|	|V5|, θ5, |V7|, θ7, Q9, θ9
3	|V1|, θ1, P2, |V2|, P3, |V3|, P5, Q5, P7, |V7|, P9, Q9	|V5|, θ5, Q7, θ7, |V9|, θ9
4	|V1|, θ1, P2, |V2|, P3, |V3|, P5, Q5, P7, |V7|, P9, |V9|	|V5|, θ5, Q7, θ7, Q9, θ9
5	|V1|, θ1, P2, |V2|, P3, |V3|, P5, |V5|, P7, Q7, P9, Q9	Q5, θ5, |V7|, θ7, |V9|, θ9
6	|V1|, θ1, P2, |V2|, P3, |V3|, P5, |V5|, P7, Q7, P9, |V9|	Q5, θ5, |V7|, θ7, Q9, θ9
7	|V1|, θ1, P2, |V2|, P3, |V3|, P5, |V5|, P7, |V7|, P9, Q9	Q5, θ5, Q7, θ7, |V9|, θ9

The simulation results for the seven topologies and 7 test cases are enumerated in Table 24. For each test case noise was simulated for the emulator inputs and emulator measurements by adding normally distributed, zero mean, random noise to the inputs and outputs of the simulation. The probability $P(m)$ was computed for each test case and the performance index PI computed for each topology. Topologies two through seven were dismissed with high performance indices and topology one was chosen correctly as the power system topology. Similar to the three bus test case the topology was correctly identified in the presence of noise. $P(m)$ for topology one was consistently the highest or close to the highest in all test cases. For this example seven test cases were run. However, good results can be obtained by running as few as four. To test the robustness of this technique multiple topology identification tests were simulated on randomly generated sets of data.

Table 24: Topology Identification Results for Nine Bus Example

Topology	P(m1)	P(m2)	P(m3)	P(m4)	P(m5)	P(m6)	P(m7)	PI
1	0.749	0.562	0.758	0.274	0.538	0.357	0.058	30
2	0.272	0.570	0.240	0.257	0.234	0.299	0.001	1192
3	0.148	0.150	0.000	0.003	0.176	0.204	0.000	> 10E6
4	0.210	0.210	0.208	0.294	0.002	0.000	0.000	> 10E6
5	0.211	0.277	0.405	0.264	0.197	0.001	0.000	> 10E6
6	0.148	0.152	0.000	0.003	0.303	0.207	0.000	> 10E6
7	0.348	0.148	0.200	0.000	0.346	0.241	0.011	> 10E6

One hundred topology identification simulations were performed on the nine bus system. The measurement data was randomly generated for one hundred tests with $\sigma_P = \sigma_{|V|} = 0.005$ and $\sigma_\theta = 0.05$. The emulation measurements were modeled with the same standard deviations. The topology identification results are shown in Table 48. The correct topology was selected for 99% of the cases. The one case where the incorrect topology was selected was flagged as questionable. In addition, these same one hundred cases were performed with varying the standard deviation of the emulator measurements. The technique was relatively robust and correctly identified the topology over 95% of the time with standard deviations as large as $\sigma_P = \sigma_{|V|} = 0.1$ and $\sigma_\theta = 0.5$ for emulator measurements.

Simulations were also conducted modeling the noise present in the emulator by adding random noise to the emulator inputs and outputs during simulation. These results are tabulated in Table 49 where the emulation measurements had the same standard deviations as the power system measurements. In these simulations the correct topology was selected for 99% of the cases. The only case that the incorrect topology was identified was flagged as questionable. These results are similar to those shown in the three bus example and further exhibit the robustness of the technique in the presence of noise in the analog emulator. The results are more dependent upon the quality of measurements from the power system.

Another set of one hundred cases were simulated with random measurement data from the power system. In these cases the standard deviations of the power system measurements where $\sigma_P = \sigma_{|V|} = 0.05$ and $\sigma_\theta = 0.5$. The results for topology identification are shown in Table 50. These simulations incorporated emulator measurement noise with the standard deviation of emulator measurements equal to the power system measurements. With the larger error in power system measurements the correct topology was identified in 84% of the cases. Eleven out of the sixteen incorrect cases were labeled as suspect. As an end result in five of these one hundred cases the incorrect topology would have been selected. Additional simulations were conducted with varying emulator measurement noise and similar results were obtained. Input identification was performed next.

Topology one was selected as the correct topology. With the topology identified, two out of the three requirements for steady-state system emulation in theorem 1 are satisfied. Determining the correct inputs will satisfy the remaining condition. Case three was used as the starting point for the input identification process. This test case was chosen because it exhibited the highest $P(m)$ during topology identification. Similar to the previous example, two methods were utilized to determine the inputs to the emulator. The first was a Monte Carlo type process and the second was the heuristic process. Five hundred runs were conducted for the Monte Carlo analysis and twenty steps were performed for the heuristic process. The generation of inputs for the Monte Carlo analysis was the same as before. Random noise was added to the starting point inputs with standard deviations of $\sigma_P = \sigma_Q = \sigma_V = 0.001$. The twenty steps of the heuristic process are detailed in Table 51. The results obtained from these steps are enumerated in Table 52. These tables are located in the appendices. The inputs identified by these methods are shown in Table 25. The true values and values obtained with a WLS state estimator are also included for comparison purposes.

Both the heuristic and Monte Carlo approaches showed improvement over the starting point $\left(P(m) = 0.9052\right)$. The Monte Carlo only showed marginal improvement while the heuristic approach achieved a better solution in far fewer steps. In addition, the results of both methods compared favorably to the WLS method and were close to the true values of the system. Generally speaking, the results from the proposed approach are closer to the true system values than the WLS state estimator. In particular, reactive power injections at generation buses and bus voltage angles for the proposed method are closer to the true values than the WLS estimator. Table 26 shows a comparison in measurement residuals for the WLS estimator and the two analog techniques. Both analog methods exhibited lower total residuals as compared to the WLS method. With the topology chosen and the inputs identified the emulator can emulate the power system in steady-state and perform contingency and stability analysis. All the requirements from theorems 1 and 2 have been satisfied.

Table 25: Input Estimation Results Comparison for Nine Bus System

	Monte Carlo	**Heuristic**	**WLS**	**True Value**
|V1|	1.0000	1.0000	1.0000	1.0000
θ1	0.0000	0.0000	0.0000	0.0000
|V2|	0.9960	1.0013	1.0047	1.0000
θ2	9.7658	9.7342	9.6290	9.6690
|V3|	0.9881	0.9885	0.9908	1.0000
θ3	4.9881	4.9774	4.9140	4.7710
|V4|	0.9852	0.9854	0.9865	0.9870
θ4	-2.4510	-2.4473	-2.4500	-2.4070
|V5|	0.9718	0.9721	0.9738	0.9750
θ5	-4.0857	-4.0875	-4.0950	-4.0170
|V6|	0.9948	0.9953	0.9977	1.0030
θ6	2.0580	2.0511	2.0020	1.9260
|V7|	0.9801	0.9809	0.9837	0.9860
θ7	0.7026	0.6994	0.6510	0.6220
|V8|	0.9933	0.9945	0.9974	0.9960
θ8	3.8641	3.8513	3.7840	3.7990
|V9|	0.9547	0.9552	0.9572	0.9580
θ9	-4.4266	-4.4134	-4.4210	-4.3500
P1	0.7314	0.7305	0.7320	0.7195
Q1	0.2734	0.2692	0.2512	0.2407
P2	1.6336	1.6329	1.6328	1.6300
Q2	0.1846	0.1923	0.1992	0.1446
P3	0.8574	0.8571	0.8570	0.8500
Q3	-0.0907	-0.0925	-0.0939	-0.0365
P4	0.0000	0.0000	0.0000	0.0000
Q4	0.0000	0.0000	0.0000	0.0000
P5	0.9112	0.9125	0.9124	0.9000
Q5	0.2845	0.2849	0.2834	0.3000
P6	0.0000	0.0000	0.0000	0.0000
Q6	0.0000	0.0000	0.0000	0.0000
P7	0.9960	0.9952	0.9962	1.0000
Q7	0.3541	0.3566	0.3569	0.3500
P8	0.0000	0.0000	0.0000	0.0000
Q8	0.0000	0.0000	0.0000	0.0000
P9	1.2643	1.2621	1.2627	1.2500
Q9	0.5056	0.5075	0.5055	0.5000
P(m)	0.9067	0.9192	x	x

Table 26: Measurement Residual Comparison for Nine Bus System

	Monte Carlo	Heuristic	WLS
P2	0.0042	0.0000	0.0002
|V2|	0.2760	0.0000	0.1188
P3	0.5523	0.5103	0.4900
|V3|	0.0019	0.0000	0.0513
P5	0.0167	0.0000	0.0002
θ5	2.3983	2.5121	3.0090
|V5|	0.4190	0.3824	0.2001
Q5	0.0019	0.0064	0.0044
P7	0.0000	0.0064	0.0004
θ7	0.3263	0.4038	2.5702
|V7|	0.0000	0.0064	0.1284
Q7	0.0787	0.0011	0.0000
P9	0.0204	0.0064	0.0004
θ9	2.5322	1.7617	2.1883
|V9|	1.9510	1.8138	1.3151
Q9	0.0122	0.0064	0.0141
J(x)	8.5909	7.4172	10.0907

The contingency and stability analysis process was tested in a similar fashion as the three bus system. In order to satisfy the requirements for dynamic system emulation, as outlined in theorems 1 and 3, the steady-state emulation operating point is taken as initial conditions. The other inputs to the emulator are dictated by the contingency to be tested. In addition, the time duration to be emulated is specified as the time it takes for the emulator to converge to a solution or exhibit instability. These components satisfy the requirement for correct inputs to the emulator for dynamic system emulation. The functional description and computability requirements have already been satisfied.

Contingency and stability analysis were performed for the loss of transmission lines. In addition, stability analysis was conducted on ground faults at buses two and three. The contingency on transmission line number nine is presented here.

Transmission line nine connects buses nine and four. The system maintained stability with the loss of this line. The steady-state results are enumerated in Table 27 for the emulator results and Table 28 for the integration results. The voltage magnitudes are within 0.016 per unit, angles within 0.95 degrees, real power values within 0.018 per unit, and reactive power values within 0.070 per unit. The analog security assessment method also correctly identified a low bus voltage magnitude on bus nine. The system dynamics were also very comparable.

Table 27: Nine Bus System Analog Security Assessment Results for Line Nine Contingency

Bus #	**Voltage**		**Generation**		**Load**	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.795	0.050	0.000	0.000
2	0.996	-1.764	1.634	0.859	0.000	0.000
3	0.988	-2.627	0.855	0.076	0.000	0.000
4	0.998	-2.631	0.000	0.000	0.000	0.000
5	0.979	-6.834	0.000	0.000	0.911	0.285
6	0.985	-5.567	0.000	0.000	0.000	0.000
7	0.948	-9.854	0.000	0.000	0.996	0.354
8	0.948	-8.566	0.000	0.000	0.000	0.000
9	0.778	-23.521	0.000	0.000	1.264	0.506

Table 28: Nine Bus System Numerical Integration Results for Line Nine Contingency (True Values)

Bus #	**Voltage**		**Generation**		**Load**	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.777	0.024	0.000	0.000
2	1.000	-1.505	1.630	0.790	0.000	0.000
3	1.000	-2.464	0.850	0.111	0.000	0.000
4	1.000	-2.566	0.000	0.000	0.000	0.000
5	0.983	-6.670	0.000	0.000	0.900	0.300
6	0.995	-5.427	0.000	0.000	0.000	0.000
7	0.958	-9.550	0.000	0.000	1.000	0.350
8	0.956	-8.205	0.000	0.000	0.000	0.000
9	0.794	-22.569	0.000	0.000	1.250	0.500

The generators swings were plotted for both the emulator and integration techniques for comparison. The swing of generator two angle is shown in Figure 63 and generator three angle in Figure 64. The analog techniques results are very comparable to the true values. A closer look at the initial swings for generator two is shown in Figure 65 and generator three in Figure 66. Contingencies for the other lines showed similar results. These results are tabulated in the appendix. Two faults were then simulated for stability analysis.

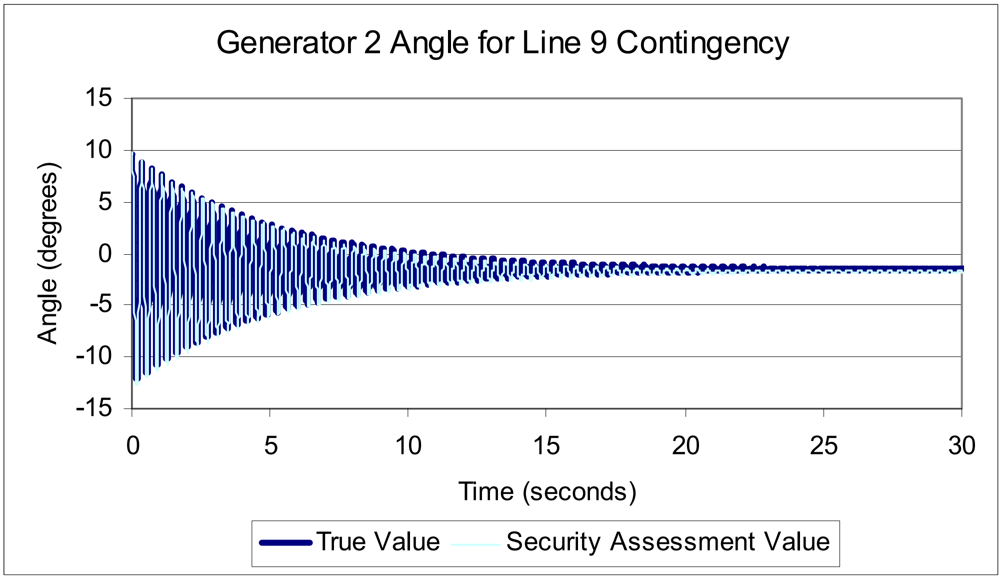


Figure 63: Nine Bus System Generator Two Angle for Line Nine Contingency

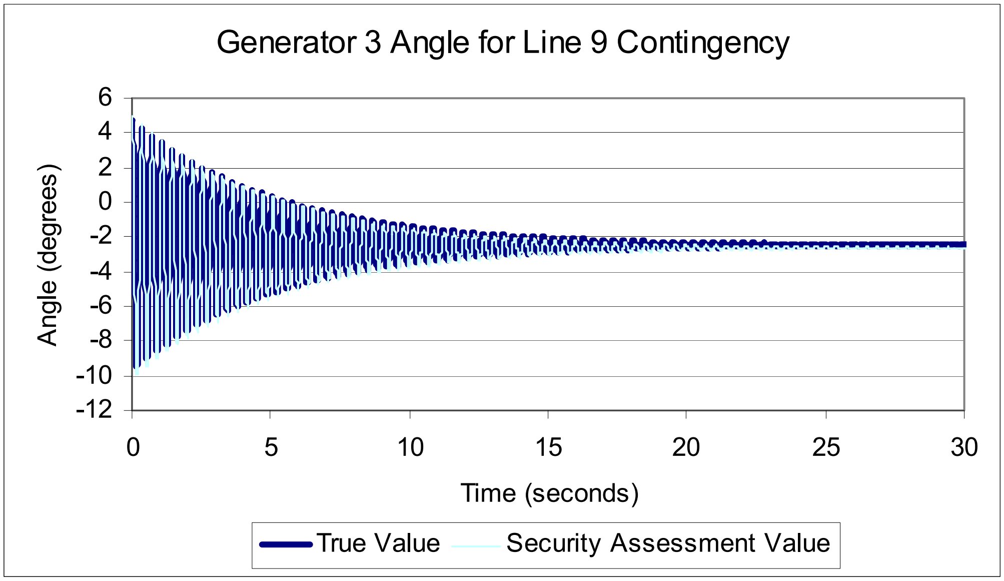


Figure 64: Nine Bus System Generator Three Angle for Line Nine Contingency

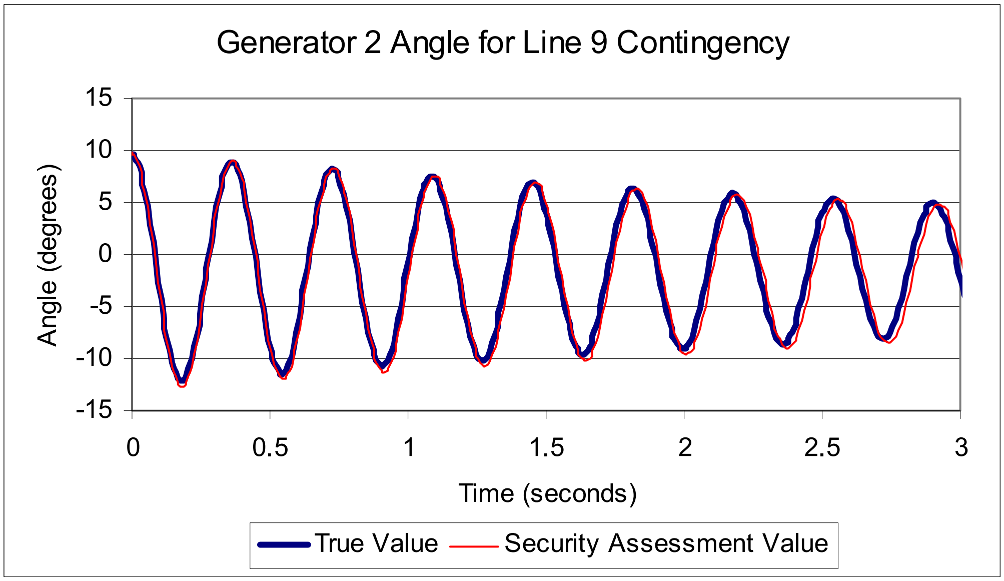


Figure 65: Nine Bus System Generator Two Angle Initial Swings for Line Nine Contingency

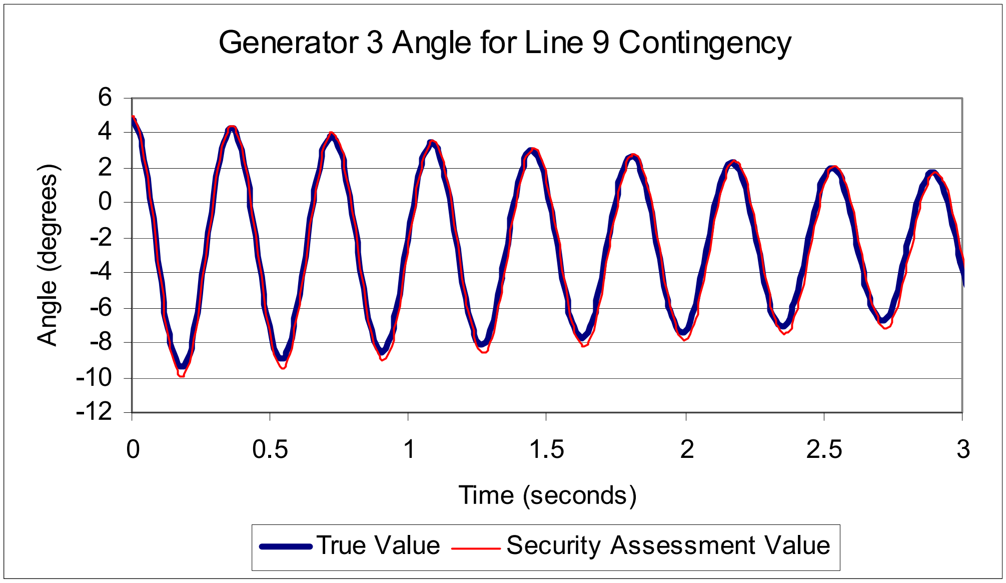


Figure 66: Nine Bus System Generator Three Angle Initial Swings for Line Nine Contingency

Analysis of three phase ground faults on bus two and bus three were performed. The faults were analyzed separately. In once case a fault was introduced on bus two and in another the fault on bus three. Many fault durations were analyzed to determine the critical clearing time of each fault. For the fault on bus two the clearing time was determined to be 384 ms for the true values of the system and 382 ms for the emulator results. The response of the system in emulation, for both unstable and stable cases, is very close to the true values. Figure 67 shows the generator angle results for the fault duration equal to the critical clearing time. For the fault on bus three the clearing time was determined to be 252 ms for the true values and 251 ms for the emulator. The generator response for the fault at bus three with a duration equal to the critical clearing time is shown in Figure 68. The emulator results closely match the true values.

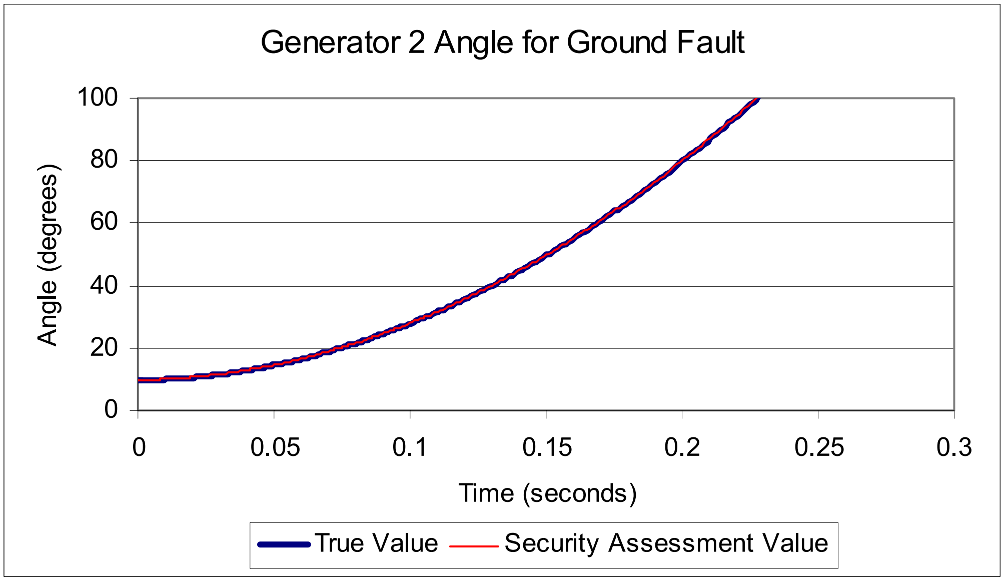


Figure 67: Nine Bus System Generator Two Angle for Ground Fault at Bus Two

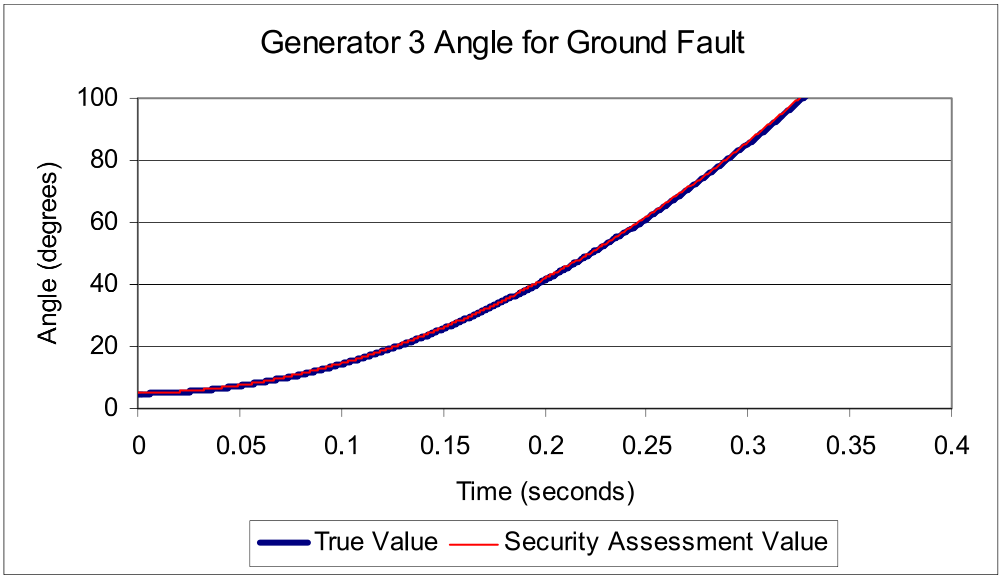


Figure 68: Nine Bus System Generator Three Angle for Ground Fault at Bus Three

7 CONCLUSIONS AND FUTURE WORK

7.1 CONCLUSIONS

This dissertation provided an overview of current methods for power system security assessment and presented an alternative method utilizing analog computation. The framework for the analog method, including relevant computation theory, methodology, hardware, and software, was developed and presented. The proposed method of security assessment was verified through simulation and hardware testing. The performance of this new method was verified through benchmarking against current methods.

The proposed method of power system security assessment has shown good results and exhibits certain advantages over traditional techniques. Namely, errors due to topology and measurement errors can be identified and eliminated simultaneously in the topology identification step. In addition, the process of identifying the correct topology also produces a decent estimate of the system operating state. In addition, during contingency analysis a full dynamic analysis of the system is performed much faster than real time. This provides system stability information not found in state of the art online techniques. The proposed analog technique also always converges to a solution. The same cannot be said for traditional numeric techniques. Computation time for the proposed method was defined explicitly and will be directly related to the structure of the emulation hardware for actuation and data acquisition.

Historically analog computation was limited due to configuration and data acquisition times. In addition, noise and measurement accuracy further limited analog techniques. The work presented here advanced analog computation techniques and mitigated many of the prior limitations. The configuration and acquisition of data was fully automated via a software interface. This allows for much faster operation of the analog computer. In addition, a scaling technique has been presented that is automated via software. The software interface also allows for automatic calibration of the analog hardware which can help offset errors due to non-ideal analog hardware. These advancements move forward the concept of analog computation as a security assessment tool.

The proposed security assessment process was separated into a few parts. Specifically the parts are topology identification, input identification, and contingency/stability analysis. The topology identification technique has been shown to be very robust in the presence of noise in the analog emulator and measurement errors. This allows for accurate topology identification in a realistic application. Input identification and contingency/stability analysis, while quantitatively limited to the hardware performance, qualitatively perform very well. The result is a fully analog technique capable of performing security assessment. In addition, this analog method, or portions of this proposed method, could also be used in conjunction with traditional digital methods to improve current security assessment routines. For example, the analog tools could be utilized as a contingency screener for digital techniques and/or a fast stability analyzer.

7.2 SUMMARY OF RESEARCH CONTRIBUTIONS

The work presented in this dissertation is a continuation of research in the field of analog computation and application in power system analysis. The following contributions to this research topic have been made:

- Development of relevant and necessary analog computation theory on computability, system emulation, and computation time. Specifically, computability and system emulation in both the steady-state and dynamic sense have been addressed.
- Further development of an analog computational methodology for power system analysis (DC Emulation).
- Development of power system models and appropriate analog hardware for the computation technique.
- Development of algorithms, interface to analog hardware, and software for operating the analog emulator.

7.3 FUTURE WORK

There is still much work necessary before implementing this approach as an online tool for power system analysis. Firstly, state of the art analog hardware and fabrication techniques need to be analyzed to determine the feasibility of constructing a large scale emulator. Size, cost, and computation time need to be addressed for specific hardware architectures. Many of these issues can be addressed through the construction of a large scale prototype.

A logical approach would be to fabricate a larger prototype, of the range of hundreds of buses, on a single VLSI chip. Data acquisition and control methods could be implemented on the same chip or a separate chip interfacing with the analog hardware. In addition, the potential of running many of these chips in parallel to realize an even larger power system emulator should be examined. Many of the aforementioned issues could be addressed at least partly in the process of building such a prototype. Further work could also be carried out on the presented technique for power system security assessment.

There is much room for optimization in the proposed technique for power system security assessment. The steps and algorithms for topology identification, input identification, and contingency/stability analysis could be refined for both performance and computation time. The result would be faster and more accurate security assessment. In addition, the issue of parameter estimation was not examined in this work. In order to provide a more robust technique of security assessment this should be addressed in future work.

While the majority of this work focused primarily on analog computation it should be noted that it is not practical to implement a purely analog method. The presented technique took advantage of digital technology to control the analog hardware, acquire data, and some post processing of the results. However, the core computation of the power system was performed in analog hardware. This synergy between analog and digital technology is driving the renewed interest in analog computation.

Improvements to power system security assessment could be seen by only implementing some of the presented analog methods to augment the current digital methods. Specifically, the presented technique for topology identification handles and eliminates topological and measurement errors concurrently. State of the art digital methods cannot accomplish this. In addition, faster than real time dynamic emulation, independent of system size, is possible with the presented analog techniques. State of the art digital methods simply cannot perform this type of dynamic simulation in a timely fashion. Implementation of these two aspects alone would yield tremendous improvement in power system security assessment.

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APPENDIX A: EXAMPLE POWER SYSTEM DATA

Table 29: Three Bus Power System Bus Type and Parameters

Three Bus System								
Bus	Bus Type		Transmission Lines					
1	slack		Line	From Bus	To Bus	R	X	B
2	PV		1	1	2	0.022	0.220	0.000
3	PQ		2	1	3	0.012	0.120	0.000
			3	2	3	0.019	0.190	0.000

Table 30: Three Bus Power System I Bus Type and Parameters for Hardware Testing

Three Bus System								
Bus	Bus Type		Transmission Lines					
1	slack		Line	From Bus	To Bus	R	X	B
2	PV		1	1	2	0.020	0.220	0.000
3	PQ		2	1	3	0.015	0.150	0.000
			3	2	3	0.019	0.190	0.000

Table 31: Three Bus Power System II Bus Type and Parameters for Hardware Testing

Three Bus System								
Bus	Bus Type		Transmission Lines					
1	slack		Line	From Bus	To Bus	R	X	B
2	PV		1	1	2	0.020	0.220	0.000
3	PQ		2	1	3	0.060	0.150	0.000
			3	2	3	0.050	0.190	0.000

Table 32: Nine Bus Power System Bus Type and Parameters

Nine Bus System								
Bus	Bus Type		Transmission Lines					
1	slack		Line	From Bus	To Bus	R	X	B
2	PV		1	1	4	0.0000	0.0576	0.0000
3	PV		2	4	5	0.0170	0.0920	0.1580
4	PQ		3	5	6	0.0390	0.1700	0.3580
5	PQ		4	3	6	0.0000	0.0586	0.0000
6	PQ		5	6	7	0.0119	0.1008	0.2090
7	PQ		6	7	8	0.0085	0.0720	0.1490
8	PQ		7	8	2	0.0000	0.0625	0.0000
9	PQ		8	8	9	0.0320	0.1610	0.3060
			9	9	4	0.0100	0.0850	0.1760

Table 33: Three Bus System Base Case Power Flow

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.420	0.790	0.000	0.000
2	1.000	6.469	1.630	0.464	0.000	0.000
3	0.909	-6.466	0.000	0.000	2.000	0.750

Table 34: Three Bus System I Base Case Power Flow for Hardware Testing

Bus #	**Voltage**		**Generation**		**Load**	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.590	0.666	0.000	0.000
2	1.050	6.180	2.000	1.310	0.000	0.000
3	0.875	-10.230	0.000	0.000	2.500	1.000

Table 35: Three Bus System II Base Case Power Flow for Hardware Testing

Bus #	**Voltage**		**Generation**		**Load**	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.586	0.414	0.000	0.000
2	1.000	2.528	1.000	0.359	0.000	0.000
3	0.899	-6.012	0.000	0.000	1.500	0.500

Table 36: Nine Bus System Base Case Power Flow

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.720	0.241	0.000	0.000
2	1.000	9.669	1.630	0.145	0.000	0.000
3	1.000	4.771	0.850	-0.037	0.000	0.000
4	0.987	-2.407	0.000	0.000	0.000	0.000
5	0.975	-4.017	0.000	0.000	0.900	0.300
6	1.003	1.926	0.000	0.000	0.000	0.000
7	0.986	0.622	0.000	0.000	1.000	0.350
8	0.996	3.799	0.000	0.000	0.000	0.000
9	0.958	-4.350	0.000	0.000	1.250	0.500

APPENDIX B: DATA AND RESULTS FOR SECURITY ASSESSMENT EXAMPLES

Table 37: Three Bus Topology Identification Results in the Presence of Bad Data (θ3=0)

Topology	Case 1			Case 2				
	P(m1)	Q3	θ3	P(m2)	|V3|	θ3	PI (bad data)	PI (good data)
1	0.0000	-0.4909	-6.4060	0.1490	0.965	-6.494	> 10E6	6.10
2	0.0000	-0.5907	-3.0680	0.1054	0.957	-2.962	> 10E6	8.62
3	0.0000	-0.4898	-14.5530	0.0073	0.939	-15.186	> 10E6	124.90
4	0.0000	-0.7431	-30.1980	0.0000	0.815	-35.482	> 10E6	980136.94

Table 38: Three Bus Topology Identification Results in the Presence of Bad Data (V3=0.75)

Topology	Case 1			Case 2				
	P(m1)	Q3	θ3	P(m2)	|V3|	θ3	PI (bad data)	PI (good data)
1	0.0134	2.1032	-7.7530	0.0958	0.965	-6.494	85.35	75.91
2	0.0000	1.9695	-2.9900	0.0069	0.957	-2.962	> 10E6	> 10E6
3	0.0001	1.0473	-18.1300	0.0968	0.939	-15.186	17155.75	> 10E6
4	0.0000	0.1537	-38.2970	0.0000	0.815	-35.482	> 10E6	> 10E6

Table 39: Randomly Generated Measurement Data for Three Bus Power System

Randomly Generated Measurement Data

Case	V2	θ2	V3	θ3	P1	Q1	P2	Q2	P3	Q3
1	0.986	6.368	1.002	-6.727	0.379	0.808	1.664	0.541	2.050	0.761
2	0.998	6.963	0.879	-5.728	0.379	0.822	1.565	0.421	1.976	0.761
3	0.979	6.725	0.849	-6.514	0.442	0.775	1.622	0.473	2.021	0.834
4	0.932	6.651	0.881	-6.988	0.455	0.814	1.620	0.445	1.956	0.658
5	0.979	6.557	0.920	-7.086	0.455	0.811	1.703	0.438	2.000	0.724
6	1.025	7.855	0.901	-6.251	0.322	0.763	1.536	0.459	1.934	0.716
7	1.047	7.244	0.930	-6.746	0.429	0.751	1.583	0.394	1.905	0.747
8	1.000	6.479	0.881	-5.523	0.409	0.719	1.615	0.436	1.994	0.730
9	0.978	5.695	0.904	-6.012	0.538	0.816	1.651	0.517	2.021	0.815
10	0.967	6.089	0.879	-6.060	0.423	0.698	1.721	0.497	1.923	0.731
11	0.995	6.638	0.961	-7.168	0.368	0.758	1.639	0.531	2.097	0.787
12	0.995	6.069	0.934	-5.847	0.485	0.776	1.641	0.496	1.973	0.761
13	0.969	7.142	0.958	-7.655	0.365	0.774	1.529	0.542	2.012	0.782
14	1.085	6.832	0.949	-6.164	0.417	0.735	1.737	0.396	2.023	0.770
15	1.073	6.218	0.919	-6.089	0.373	0.821	1.718	0.468	2.130	0.716
16	1.014	6.012	0.811	-6.625	0.449	0.831	1.546	0.368	1.978	0.752
17	1.009	6.943	0.883	-7.024	0.340	0.849	1.654	0.546	1.977	0.800
18	1.001	5.664	0.971	-6.124	0.381	0.817	1.737	0.482	2.012	0.814
19	0.972	6.847	0.863	-5.780	0.432	0.796	1.649	0.460	1.971	0.773
20	0.965	6.873	0.858	-5.819	0.421	0.801	1.716	0.360	2.006	0.696
21	0.980	6.267	0.913	-6.684	0.392	0.834	1.589	0.451	2.025	0.710
22	1.008	7.759	0.844	-5.954	0.459	0.748	1.601	0.467	1.999	0.746
23	0.977	6.516	0.923	-6.006	0.446	0.802	1.560	0.512	2.080	0.678
24	1.004	6.047	0.881	-6.480	0.358	0.827	1.633	0.471	2.080	0.711
25	0.992	6.626	0.980	-6.302	0.444	0.810	1.626	0.530	2.049	0.836
26	1.037	6.579	0.975	-6.151	0.365	0.768	1.594	0.482	1.975	0.645
27	0.984	7.820	0.827	-6.734	0.447	0.865	1.607	0.439	2.062	0.752
28	1.015	7.008	0.947	-7.126	0.395	0.818	1.532	0.426	1.878	0.717
29	0.971	4.932	0.987	-6.670	0.491	0.722	1.675	0.491	1.977	0.872
30	1.002	6.739	0.943	-6.761	0.407	0.866	1.680	0.479	1.959	0.725
31	0.996	6.844	0.819	-5.859	0.417	0.770	1.660	0.496	2.051	0.797
32	0.965	6.172	0.896	-5.845	0.343	0.771	1.644	0.505	1.951	0.745
33	1.019	6.417	0.874	-6.659	0.421	0.858	1.651	0.467	2.015	0.774
34	1.076	6.627	0.949	-6.176	0.509	0.743	1.584	0.483	2.045	0.758
35	0.969	6.874	1.005	-6.268	0.377	0.912	1.588	0.478	2.041	0.811
36	0.911	6.499	0.871	-7.311	0.475	0.863	1.642	0.409	2.121	0.730
37	1.066	6.630	0.885	-6.428	0.415	0.861	1.665	0.482	1.970	0.707
38	0.959	5.831	0.995	-6.415	0.380	0.727	1.692	0.540	2.089	0.782
39	1.063	5.594	0.908	-5.232	0.387	0.803	1.611	0.530	1.967	0.753
40	1.054	6.537	0.908	-6.935	0.346	0.808	1.654	0.480	1.906	0.784
41	1.006	6.559	0.879	-6.984	0.405	0.863	1.720	0.397	2.019	0.749
42	0.950	5.967	0.923	-6.321	0.408	0.779	1.675	0.432	1.991	0.786
43	0.998	6.454	0.890	-6.743	0.467	0.724	1.615	0.334	2.039	0.780
44	0.997	6.510	0.821	-7.357	0.387	0.858	1.737	0.472	1.915	0.764
45	1.009	5.550	0.834	-6.056	0.408	0.708	1.614	0.424	2.035	0.748
46	0.949	6.519	0.903	-6.121	0.514	0.806	1.625	0.466	1.969	0.663
47	1.019	6.495	0.885	-6.344	0.456	0.798	1.637	0.414	2.065	0.810
48	1.019	6.038	0.847	-5.145	0.375	0.729	1.645	0.427	1.943	0.679
49	0.925	6.426	0.908	-6.639	0.469	0.822	1.776	0.402	2.008	0.789
50	1.084	6.869	0.953	-6.578	0.435	0.764	1.622	0.459	2.050	0.772
51	0.988	5.886	0.947	-5.884	0.369	0.875	1.605	0.473	2.018	0.738
52	0.999	6.778	1.002	-6.425	0.500	0.771	1.565	0.428	1.972	0.781
53	0.945	5.092	0.922	-6.895	0.477	0.775	1.688	0.516	2.106	0.717
54	0.980	6.277	0.933	-6.244	0.439	0.845	1.673	0.405	2.020	0.721
55	1.003	6.204	0.936	-6.125	0.447	0.764	1.564	0.433	1.972	0.754
56	1.000	6.424	0.896	-6.903	0.441	0.783	1.657	0.508	1.937	0.793
57	0.963	6.314	0.833	-6.053	0.389	0.838	1.729	0.479	1.980	0.779
58	1.001	6.385	0.875	-6.961	0.418	0.826	1.616	0.393	2.023	0.805
59	1.050	6.507	0.816	-6.773	0.478	0.761	1.617	0.464	1.998	0.725
60	1.036	6.902	1.031	-6.411	0.421	0.839	1.630	0.534	2.088	0.794
61	1.010	6.122	0.910	-7.019	0.515	0.782	1.593	0.414	2.045	0.772
62	0.995	7.243	0.917	-6.064	0.334	0.799	1.606	0.427	1.893	0.659
63	0.941	6.092	0.956	-6.557	0.417	0.835	1.703	0.408	2.091	0.758
64	1.033	6.296	0.896	-6.788	0.375	0.826	1.630	0.323	1.993	0.779
65	0.971	6.652	0.882	-6.177	0.322	0.816	1.710	0.501	2.028	0.709
66	0.976	5.593	0.863	-6.005	0.422	0.811	1.660	0.560	2.036	0.634
67	0.977	6.155	0.960	-6.711	0.400	0.860	1.644	0.558	1.960	0.722
68	0.929	6.091	0.917	-6.277	0.429	0.760	1.580	0.523	2.119	0.863
69	1.025	6.409	0.909	-6.682	0.410	0.839	1.653	0.396	2.014	0.882
70	0.896	6.068	0.886	-6.369	0.464	0.710	1.614	0.429	1.963	0.769
71	1.033	7.031	0.958	-7.124	0.419	0.797	1.750	0.509	2.004	0.768
72	0.981	7.112	0.937	-6.556	0.418	0.887	1.695	0.446	1.984	0.754
73	0.863	6.201	1.019	-6.769	0.492	0.850	1.667	0.458	1.998	0.700
74	1.043	7.505	0.879	-6.173	0.496	0.897	1.593	0.387	1.989	0.775
75	0.929	7.041	0.958	-6.220	0.483	0.820	1.653	0.393	1.954	0.678
76	0.989	6.310	0.941	-6.447	0.419	0.812	1.604	0.411	1.998	0.725
77	0.952	6.393	0.993	-5.688	0.367	0.795	1.643	0.576	2.016	0.850
78	1.072	6.432	0.891	-6.855	0.407	0.769	1.701	0.422	2.008	0.748
79	1.044	6.266	0.778	-6.950	0.448	0.828	1.601	0.522	1.985	0.750
80	1.007	5.561	0.770	-6.335	0.426	0.807	1.608	0.464	1.990	0.752
81	0.960	6.158	0.980	-7.508	0.422	0.789	1.602	0.406	2.005	0.774
82	0.954	6.470	0.941	-7.250	0.455	0.839	1.626	0.462	2.015	0.717
83	0.984	5.909	0.982	-6.261	0.477	0.819	1.584	0.549	1.999	0.712
84	1.032	6.661	0.879	-6.673	0.476	0.755	1.612	0.555	1.918	0.764
85	1.065	6.700	0.973	-6.944	0.480	0.770	1.600	0.556	1.952	0.730
86	1.015	6.860	0.929	-6.629	0.401	0.775	1.544	0.461	2.011	0.859
87	0.946	6.179	0.815	-6.007	0.393	0.760	1.631	0.477	2.037	0.742
88	1.003	5.605	0.945	-6.448	0.411	0.749	1.679	0.375	1.998	0.795
89	0.980	5.915	0.997	-6.826	0.409	0.819	1.639	0.439	2.060	0.744
90	0.934	5.928	0.917	-7.199	0.454	0.808	1.660	0.468	2.054	0.717
91	1.001	6.815	0.875	-6.488	0.343	0.736	1.619	0.380	1.915	0.745
92	1.037	6.267	0.952	-4.794	0.451	0.854	1.593	0.516	1.969	0.771
93	0.994	6.979	0.996	-5.972	0.399	0.773	1.587	0.425	2.073	0.805
94	1.031	7.580	0.844	-5.881	0.361	0.762	1.689	0.475	2.038	0.708
95	1.130	6.123	0.830	-6.771	0.439	0.854	1.600	0.576	1.999	0.787
96	0.942	6.812	0.946	-6.209	0.505	0.756	1.801	0.444	2.060	0.765
97	1.039	6.303	1.014	-6.272	0.387	0.787	1.651	0.460	2.039	0.743
98	0.998	6.627	1.008	-6.789	0.436	0.870	1.581	0.407	1.926	0.702
99	0.908	5.698	0.897	-5.866	0.418	0.763	1.627	0.577	2.011	0.759
100	0.881	5.453	0.970	-6.648	0.388	0.779	1.639	0.509	1.938	0.756

Table 40: Topology Identification Results for Three Bus System

Case	Performance Indices				Correct	Topology 1		Topology2		Topology 3		Topology 4	
	PI top 1	PI top 2	PI top 3	PI top 4	Topology	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)
1	21	>10E6	>10E6	>10E6	1	0.059	0.240	0.000	0.106	0.000	0.007	0.000	0.000
2	58	435	333400	>10E6	1	0.018	0.645	0.002	0.697	0.000	0.370	0.000	0.000
3	22	181060	1502	>10E6	1	0.049	0.578	0.000	0.589	0.001	0.464	0.000	0.000
4	5	3	838	>10E6	2	0.283	0.874	0.445	0.860	0.001	0.532	0.000	0.000
5	40	375710	>10E6	>10E6	1	0.026	0.757	0.000	0.612	0.000	0.174	0.000	0.002
6	14	137	>10E6	>10E6	1	0.082	0.759	0.007	0.735	0.000	0.302	0.000	0.000
7	3	4	>10E6	>10E6	1	0.618	0.903	0.382	0.857	0.000	0.137	0.000	0.000
8	87	532	185970	>10E6	1	0.012	0.624	0.002	0.701	0.000	0.397	0.000	0.036
9	9	1184	>10E6	>10E6	1	0.122	0.831	0.001	0.691	0.000	0.154	0.000	0.000
10	14	3	9523	>10E6	2	0.080	0.789	0.457	0.863	0.000	0.449	0.000	0.000
11	19	>10E6	>10E6	>10E6	1	0.058	0.458	0.000	0.303	0.000	0.028	0.000	0.000
12	19	4608800	>10E6	>10E6	1	0.057	0.694	0.000	0.544	0.000	0.100	0.000	0.000
13	62	>10E6	>10E6	>10E6	1	0.017	0.357	0.000	0.284	0.000	0.038	0.000	0.000
14	3	35	>10E6	>10E6	1	0.517	0.946	0.030	0.776	0.000	0.059	0.000	0.000
15	39	56	>10E6	>10E6	1	0.026	0.718	0.018	0.759	0.000	0.135	0.000	0.000
16	26	7362200	4	>10E6	3	0.047	0.211	0.000	0.151	0.391	0.797	0.000	0.000
17	33	64	>10E6	>10E6	1	0.031	0.671	0.016	0.749	0.000	0.291	0.000	0.014
18	15	>10E6	>10E6	>10E6	1	0.082	0.388	0.000	0.248	0.000	0.019	0.000	0.000
19	36	399	1400	>10E6	1	0.029	0.628	0.003	0.702	0.001	0.493	0.000	0.000
20	37	7819	37	>10E6	3	0.028	0.561	0.000	0.645	0.028	0.638	0.000	0.000
21	6	249	>10E6	>10E6	1	0.211	0.894	0.004	0.726	0.000	0.201	0.000	0.000
22	57	584100	14	>10E6	3	0.019	0.335	0.000	0.359	0.082	0.687	0.000	0.380
23	78	3949	>10E6	>10E6	1	0.013	0.728	0.000	0.640	0.000	0.167	0.000	0.000
24	29	1601	360120	>10E6	1	0.037	0.642	0.001	0.681	0.000	0.379	0.000	0.000
25	19	654080	>10E6	>10E6	1	0.066	0.259	0.000	0.179	0.000	0.010	0.000	0.000
26	13	2241900	>10E6	>10E6	1	0.089	0.607	0.000	0.472	0.000	0.055	0.000	0.144
27	34	4267200	4	>10E6	3	0.033	0.344	0.000	0.328	0.369	0.793	0.000	0.000
28	136	>10E6	>10E6	>10E6	1	0.007	0.670	0.000	0.595	0.000	0.115	0.000	0.009
29	35	>10E6	>10E6	>10E6	1	0.033	0.197	0.000	0.097	0.000	0.008	0.000	0.000
30	44	>10E6	>10E6	>10E6	1	0.024	0.642	0.000	0.521	0.000	0.098	0.000	0.058
31	186	350770	4	>10E6	3	0.005	0.253	0.000	0.278	0.365	0.790	0.000	0.000
32	2	20	>10E6	>10E6	1	0.873	0.953	0.054	0.781	0.000	0.304	0.000	0.000
33	13	227610	344450	>10E6	1	0.087	0.580	0.000	0.603	0.000	0.371	0.000	0.005
34	5	33	>10E6	>10E6	1	0.263	0.883	0.031	0.776	0.000	0.059	0.000	0.000
35	25	104390	>10E6	>10E6	1	0.058	0.122	0.000	0.075	0.000	0.005	0.000	0.542
36	3	38	77992	>10E6	1	0.661	0.944	0.027	0.753	0.000	0.395	0.000	0.000
37	17	>10E6	63260	>10E6	1	0.068	0.429	0.000	0.439	0.000	0.406	0.000	0.000
38	20	2545300	>10E6	>10E6	1	0.071	0.160	0.000	0.082	0.000	0.009	0.000	0.000
39	75	2091	>10E6	>10E6	1	0.014	0.634	0.000	0.682	0.000	0.210	0.000	0.000
40	108	58	>10E6	>10E6	2	0.009	0.680	0.018	0.756	0.000	0.205	0.000	0.000
41	26	558	297650	>10E6	1	0.040	0.621	0.002	0.697	0.000	0.363	0.000	0.000
42	13	>10E6	>10E6	>10E6	1	0.090	0.606	0.000	0.418	0.000	0.113	0.000	0.000
43	11	4	>10E6	>10E6	2	0.105	0.845	0.352	0.849	0.000	0.258	0.000	0.008
44	177	>10E6	3	>10E6	3	0.006	0.204	0.000	0.270	0.730	0.874	0.000	0.000
45	83	303290	6	>10E6	3	0.013	0.281	0.000	0.291	0.224	0.750	0.000	0.000
46	5	338	9228700	>10E6	1	0.259	0.888	0.003	0.718	0.000	0.348	0.000	0.000
47	28	91	>10E6	>10E6	1	0.038	0.695	0.011	0.736	0.000	0.231	0.000	0.000
48	122	528840	3	>10E6	3	0.008	0.267	0.000	0.313	0.454	0.822	0.000	0.002
49	21	>10E6	>10E6	>10E6	1	0.051	0.609	0.000	0.413	0.000	0.175	0.000	0.000
50	6	90	>10E6	>10E6	1	0.204	0.904	0.011	0.751	0.000	0.047	0.000	0.000
51	33	121230	>10E6	>10E6	1	0.033	0.527	0.000	0.437	0.000	0.073	0.000	0.000
52	18	2707000	>10E6	>10E6	1	0.072	0.251	0.000	0.144	0.000	0.008	0.000	0.000
53	14	>10E6	>10E6	>10E6	1	0.082	0.616	0.000	0.442	0.000	0.144	0.000	0.000
54	15	>10E6	>10E6	>10E6	1	0.074	0.669	0.000	0.514	0.000	0.114	0.000	0.000
55	17	772750	>10E6	>10E6	1	0.064	0.721	0.000	0.583	0.000	0.097	0.000	0.000
56	10	2	>10E6	>10E6	2	0.114	0.821	0.899	0.908	0.000	0.243	0.000	0.000
57	22	>10E6	6	>10E6	3	0.050	0.470	0.000	0.498	0.207	0.744	0.000	0.119
58	15	367	2821200	>10E6	1	0.074	0.677	0.003	0.706	0.000	0.324	0.000	0.002
59	20	>10E6	4	>10E6	3	0.076	0.138	0.000	0.118	0.440	0.814	0.000	0.000
60	20	162030	>10E6	>10E6	1	0.075	0.153	0.000	0.092	0.000	0.001	0.000	0.682
61	2	5	>10E6	>10E6	1	0.854	0.969	0.260	0.837	0.000	0.165	0.000	0.000
62	2	9	>10E6	>10E6	1	0.907	0.974	0.137	0.818	0.000	0.296	0.000	0.000
63	17	>10E6	>10E6	>10E6	1	0.073	0.299	0.000	0.199	0.000	0.040	0.000	0.000
64	19	97	>10E6	>10E6	1	0.056	0.698	0.011	0.737	0.000	0.235	0.000	0.000
65	17	3	167550	>10E6	2	0.063	0.801	0.446	0.861	0.000	0.398	0.000	0.000
66	50	968560	19	>10E6	3	0.021	0.512	0.000	0.579	0.057	0.682	0.000	0.764
67	32	>10E6	>10E6	>10E6	1	0.033	0.437	0.000	0.305	0.000	0.061	0.000	0.000
68	110	6876	>10E6	>10E6	1	0.009	0.430	0.000	0.338	0.000	0.066	0.000	0.000
69	2	10	>10E6	>10E6	1	0.910	0.971	0.112	0.807	0.000	0.101	0.000	0.000
70	16	>10E6	>10E6	>10E6	1	0.070	0.724	0.000	0.532	0.000	0.326	0.000	0.000
71	119	>10E6	>10E6	>10E6	1	0.009	0.580	0.000	0.463	0.000	0.042	0.000	0.000
72	22	>10E6	>10E6	>10E6	1	0.049	0.612	0.000	0.456	0.000	0.092	0.000	0.244
73	30	>10E6	>10E6	>10E6	1	0.051	0.097	0.000	0.009	0.000	0.008	0.000	0.000
74	21	2469200	1583800	>10E6	1	0.051	0.531	0.000	0.518	0.000	0.344	0.000	0.016
75	15	>10E6	>10E6	>10E6	1	0.079	0.366	0.000	0.207	0.000	0.081	0.000	0.000
76	13	>10E6	>10E6	>10E6	1	0.090	0.657	0.000	0.490	0.000	0.099	0.000	0.124
77	41	88602	>10E6	>10E6	1	0.031	0.109	0.000	0.066	0.000	0.006	0.000	0.000
78	28	>10E6	>10E6	>10E6	1	0.039	0.462	0.000	0.516	0.000	0.292	0.000	0.000
79	30	>10E6	328	>10E6	1	0.068	0.066	0.000	0.038	0.003	0.487	0.000	0.000
80	71	9972400	1197	>10E6	1	0.016	0.125	0.000	0.054	0.001	0.431	0.000	0.000
81	91	>10E6	>10E6	>10E6	1	0.012	0.210	0.000	0.139	0.000	0.018	0.000	0.000
82	37	>10E6	>10E6	>10E6	1	0.028	0.483	0.000	0.371	0.000	0.099	0.000	0.000
83	16	771880	>10E6	>10E6	1	0.077	0.317	0.000	0.208	0.000	0.028	0.000	0.008
84	28	>10E6	109000	>10E6	1	0.038	0.512	0.000	0.552	0.000	0.410	0.000	0.000
85	63	>10E6	>10E6	>10E6	1	0.016	0.615	0.000	0.533	0.000	0.043	0.000	0.000
86	13	237870	>10E6	>10E6	1	0.086	0.758	0.000	0.614	0.000	0.062	0.000	0.000
87	164	503360	3	>10E6	3	0.006	0.313	0.000	0.376	0.695	0.866	0.000	0.000
88	17	>10E6	>10E6	>10E6	1	0.065	0.614	0.000	0.456	0.000	0.055	0.000	0.382
89	20	>10E6	>10E6	>10E6	1	0.064	0.239	0.000	0.123	0.000	0.010	0.000	0.000
90	21	>10E6	>10E6	>10E6	1	0.051	0.623	0.000	0.458	0.000	0.166	0.000	0.000
91	20	18365	4804	>10E6	1	0.055	0.593	0.000	0.637	0.000	0.472	0.000	0.000
92	234	1920	>10E6	>10E6	1	0.004	0.641	0.001	0.569	0.000	0.056	0.000	0.000
93	47	7642	>10E6	>10E6	1	0.025	0.171	0.000	0.133	0.000	0.006	0.000	0.000
94	61	3364500	8	>10E6	3	0.017	0.269	0.000	0.294	0.150	0.726	0.000	0.000
95	22	>10E6	6	89522	3	0.086	0.093	0.000	0.066	0.212	0.745	0.314	0.000
96	15	>10E6	>10E6	>10E6	1	0.082	0.381	0.000	0.223	0.000	0.054	0.000	0.000
97	15	1708500	>10E6	>10E6	1	0.091	0.279	0.000	0.162	0.000	0.005	0.000	0.000
98	53	>10E6	>10E6	>10E6	1	0.021	0.215	0.000	0.136	0.000	0.016	0.000	0.000
99	55	481180	>10E6	>10E6	1	0.019	0.627	0.000	0.491	0.000	0.241	0.000	0.000
100	29	>10E6	>10E6	>10E6	1	0.042	0.180	0.000	0.063	0.000	0.036	0.000	0.000

Table 41: Topology Identification Results for Three Bus System Filtered Results

Case	Performance Indices				Correct	Topology 1		Topology2		Topology 3		Topology 4	
	PI top 1	PI top 2	PI top 3	PI top 4	Topology	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)
1	6	4227884	>10E6	>10E6	1	0.653	0.241	0.000	0.106	0.000	0.007	0.000	0.000
2	7	8241	>10E6	>10E6	1	0.195	0.645	0.000	0.697	0.000	0.370	0.000	0.000
3	4	2404768	>10E6	>10E6	1	0.544	0.578	0.000	0.589	0.000	0.464	0.000	0.000
4	3	>10E6	>10E6	>10E6	1	0.455	0.874	0.000	0.861	0.000	0.532	0.000	0.000
5	6	>10E6	>10E6	>10E6	1	0.236	0.757	0.000	0.612	0.000	0.174	0.000	0.000
6	2	421603	>10E6	>10E6	1	0.896	0.759	0.000	0.735	0.000	0.302	0.000	0.000
7	5	>10E6	>10E6	>10E6	1	0.238	0.903	0.000	0.858	0.000	0.137	0.000	0.000
8	9	9341	>10E6	>10E6	1	0.129	0.625	0.000	0.701	0.000	0.398	0.000	0.000
9	4	245306	>10E6	>10E6	1	0.415	0.831	0.000	0.691	0.000	0.154	0.000	0.000
10	2	>10E6	>10E6	>10E6	1	0.823	0.789	0.000	0.863	0.000	0.450	0.000	0.000
11	4	5354729	>10E6	>10E6	1	0.636	0.458	0.000	0.303	0.000	0.028	0.000	0.000
12	3	431248	>10E6	>10E6	1	0.621	0.694	0.000	0.544	0.000	0.100	0.000	0.000
13	8	>10E6	>10E6	>10E6	1	0.185	0.357	0.000	0.284	0.000	0.039	0.000	0.000
14	2	>10E6	>10E6	>10E6	1	0.871	0.946	0.000	0.776	0.000	0.059	0.000	0.000
15	5	32477	>10E6	>10E6	1	0.287	0.718	0.000	0.759	0.000	0.135	0.000	0.000
16	7	669301	>10E6	>10E6	1	0.518	0.211	0.000	0.151	0.000	0.797	0.000	0.001
17	4	>10E6	>10E6	>10E6	1	0.344	0.671	0.000	0.749	0.000	0.292	0.000	0.000
18	4	>10E6	>10E6	>10E6	1	0.899	0.388	0.000	0.248	0.000	0.019	0.000	0.001
19	5	954008	>10E6	>10E6	1	0.322	0.628	0.000	0.702	0.000	0.493	0.000	0.000
20	5	6717661	>10E6	>10E6	1	0.309	0.561	0.000	0.645	0.000	0.638	0.000	0.000
21	2	907401	>10E6	>10E6	1	0.921	0.894	0.000	0.726	0.000	0.201	0.000	0.000
22	8	53102	>10E6	>10E6	1	0.205	0.335	0.000	0.359	0.000	0.687	0.000	0.753
23	10	393	>10E6	>10E6	1	0.111	0.728	0.003	0.640	0.000	0.167	0.000	0.084
24	4	115521	>10E6	>10E6	1	0.407	0.642	0.000	0.681	0.000	0.379	0.000	0.000
25	5	59467	>10E6	>10E6	1	0.726	0.259	0.000	0.179	0.000	0.010	0.000	0.000
26	3	203812	>10E6	>10E6	1	0.979	0.607	0.000	0.472	0.000	0.055	0.000	0.000
27	6	387929	>10E6	>10E6	1	0.358	0.344	0.000	0.328	0.000	0.793	0.000	0.019
28	14	>10E6	>10E6	>10E6	1	0.082	0.670	0.000	0.595	0.000	0.115	0.000	0.001
29	8	>10E6	>10E6	>10E6	1	0.365	0.197	0.000	0.097	0.000	0.008	0.000	0.000
30	5	>10E6	>10E6	>10E6	1	0.260	0.642	0.000	0.521	0.000	0.098	0.000	0.003
31	21	31891	>10E6	>10E6	1	0.060	0.253	0.000	0.279	0.000	0.790	0.000	0.000
32	3	2656319	>10E6	>10E6	1	0.579	0.953	0.000	0.781	0.000	0.304	0.000	0.000
33	3	>10E6	>10E6	>10E6	1	0.962	0.581	0.000	0.603	0.000	0.371	0.000	0.000
34	3	7821	>10E6	>10E6	1	0.534	0.883	0.000	0.776	0.000	0.059	0.000	0.000
35	10	9502	>10E6	>10E6	1	0.639	0.122	0.000	0.076	0.000	0.005	0.000	0.000
36	2	6062800	>10E6	>10E6	1	0.756	0.944	0.000	0.753	0.000	0.395	0.000	0.000
37	4	>10E6	>10E6	>10E6	1	0.752	0.429	0.000	0.439	0.000	0.406	0.000	0.000
38	8	231400	>10E6	>10E6	1	0.779	0.161	0.000	0.082	0.000	0.009	0.000	0.000
39	8	3848	>10E6	>10E6	1	0.150	0.634	0.000	0.682	0.000	0.210	0.000	0.037
40	11	>10E6	>10E6	>10E6	1	0.101	0.680	0.000	0.756	0.000	0.205	0.000	0.000
41	4	>10E6	>10E6	>10E6	1	0.442	0.621	0.000	0.697	0.000	0.363	0.000	0.000
42	3	>10E6	>10E6	>10E6	1	0.994	0.606	0.000	0.418	0.000	0.113	0.000	0.000
43	2	2804038	>10E6	>10E6	1	0.899	0.845	0.000	0.849	0.000	0.258	0.000	0.000
44	21	>10E6	>10E6	>10E6	1	0.064	0.204	0.000	0.270	0.000	0.874	0.000	0.541
45	11	27575	>10E6	>10E6	1	0.139	0.281	0.000	0.291	0.000	0.750	0.000	0.000
46	3	2345046	>10E6	>10E6	1	0.689	0.888	0.000	0.718	0.000	0.348	0.000	0.000
47	4	121260	>10E6	>10E6	1	0.416	0.695	0.000	0.736	0.000	0.231	0.000	0.000
48	14	48080	>10E6	>10E6	1	0.093	0.267	0.000	0.313	0.000	0.822	0.000	0.000
49	3	>10E6	>10E6	>10E6	1	0.557	0.609	0.000	0.413	0.000	0.175	0.000	0.000
50	17	>10E6	>10E6	>10E6	1	0.069	0.453	0.000	0.326	0.000	0.007	0.000	0.000
51	2	404060	>10E6	>10E6	1	0.928	0.904	0.000	0.751	0.000	0.047	0.000	0.032
52	5	11023	>10E6	>10E6	1	0.359	0.527	0.000	0.437	0.000	0.073	0.000	0.437
53	5	246098	>10E6	>10E6	1	0.790	0.251	0.000	0.144	0.000	0.008	0.000	0.000
54	3	6725012	>10E6	>10E6	1	0.904	0.616	0.000	0.442	0.000	0.144	0.000	0.000
55	3	2955320	>10E6	>10E6	1	0.818	0.669	0.000	0.514	0.000	0.114	0.000	0.102
56	3	78232	>10E6	>10E6	1	0.703	0.721	0.000	0.583	0.000	0.098	0.000	0.001
57	6	>10E6	>10E6	>10E6	1	0.233	0.821	0.000	0.908	0.000	0.243	0.000	0.000
58	4	>10E6	>10E6	>10E6	1	0.551	0.470	0.000	0.498	0.000	0.744	0.000	0.003
59	3	>10E6	>10E6	>10E6	1	0.819	0.677	0.000	0.706	0.000	0.324	0.000	0.000
60	8	>10E6	>10E6	>10E6	1	0.834	0.138	0.000	0.118	0.000	0.814	0.000	0.000
61	8	14740	>10E6	>10E6	1	0.822	0.153	0.000	0.092	0.000	0.001	0.000	0.000
62	2	4304030	>10E6	>10E6	1	0.785	0.969	0.000	0.837	0.000	0.165	0.000	0.009
63	2	>10E6	>10E6	>10E6	1	0.794	0.974	0.000	0.818	0.000	0.296	0.000	0.000
64	5	1655654	>10E6	>10E6	1	0.802	0.299	0.000	0.199	0.000	0.040	0.000	0.038
65	3	>10E6	>10E6	>10E6	1	0.616	0.698	0.000	0.737	0.000	0.235	0.000	0.000
66	3	>10E6	>10E6	>10E6	1	0.582	0.801	0.000	0.861	0.000	0.398	0.000	0.000
67	6	206892	>10E6	>10E6	1	0.231	0.512	0.000	0.579	0.000	0.682	0.000	0.062
68	5	>10E6	>10E6	>10E6	1	0.364	0.438	0.000	0.305	0.000	0.061	0.000	0.000
69	12	628	>10E6	>10E6	1	0.103	0.430	0.002	0.338	0.000	0.066	0.000	0.017
70	2	>10E6	>10E6	>10E6	1	0.742	0.971	0.000	0.807	0.000	0.101	0.000	0.000
71	3	>10E6	>10E6	>10E6	1	0.772	0.725	0.000	0.532	0.000	0.327	0.000	0.000
72	12	>10E6	>10E6	>10E6	1	0.094	0.580	0.000	0.463	0.000	0.042	0.000	0.001
73	4	>10E6	>10E6	>10E6	1	0.535	0.612	0.000	0.456	0.000	0.092	0.000	0.000
74	12	>10E6	>10E6	>10E6	1	0.562	0.097	0.000	0.009	0.000	0.008	0.000	0.000
75	4	225621	>10E6	>10E6	1	0.563	0.531	0.000	0.518	0.000	0.344	0.000	0.000
76	4	>10E6	>10E6	>10E6	1	0.868	0.366	0.000	0.207	0.000	0.081	0.000	0.000
77	3	1179949	>10E6	>10E6	1	0.988	0.657	0.000	0.491	0.000	0.099	0.000	0.000
78	12	8069	>10E6	>10E6	1	0.340	0.109	0.000	0.066	0.000	0.006	0.000	0.491
79	4	>10E6	>10E6	>10E6	1	0.429	0.462	0.000	0.516	0.000	0.293	0.000	0.001
80	16	>10E6	>10E6	>10E6	1	0.753	0.066	0.000	0.038	0.000	0.487	0.000	0.360
81	14	906599	>10E6	>10E6	1	0.174	0.125	0.000	0.054	0.000	0.431	0.000	0.000
82	13	>10E6	>10E6	>10E6	1	0.127	0.211	0.000	0.139	0.000	0.018	0.000	0.000
83	5	>10E6	>10E6	>10E6	1	0.312	0.483	0.000	0.371	0.000	0.099	0.000	0.000
84	4	70175	>10E6	>10E6	1	0.846	0.317	0.000	0.208	0.000	0.028	0.000	0.000
85	4	>10E6	>10E6	>10E6	1	0.423	0.512	0.000	0.552	0.000	0.410	0.000	0.003
86	7	>10E6	>10E6	>10E6	1	0.180	0.615	0.000	0.533	0.000	0.043	0.000	0.001
87	2	130477	>10E6	>10E6	1	0.937	0.758	0.000	0.614	0.000	0.062	0.000	0.003
88	18	45763	>10E6	>10E6	1	0.068	0.313	0.000	0.376	0.000	0.866	0.000	0.000
89	3	>10E6	>10E6	>10E6	1	0.711	0.614	0.000	0.456	0.000	0.055	0.000	0.000
90	6	1666916	>10E6	>10E6	1	0.703	0.239	0.000	0.123	0.000	0.010	0.000	0.000
91	3	>10E6	>10E6	>10E6	1	0.565	0.623	0.000	0.458	0.000	0.166	0.000	0.002
92	3	>10E6	>10E6	>10E6	1	0.605	0.593	0.000	0.637	0.000	0.472	0.000	0.000
93	23	176	>10E6	>10E6	1	0.047	0.641	0.006	0.569	0.000	0.056	0.000	0.000
94	10	702	>10E6	>10E6	1	0.270	0.171	0.001	0.134	0.000	0.006	0.000	0.000
95	9	305864	>10E6	>10E6	1	0.191	0.269	0.000	0.294	0.000	0.726	0.000	0.000
96	12	4421991	>10E6	>10E6	1	0.942	0.093	0.000	0.066	0.000	0.745	0.000	0.603
97	4	>10E6	>10E6	>10E6	1	0.899	0.381	0.000	0.223	0.000	0.054	0.000	0.000
98	5	155328	>10E6	>10E6	1	0.996	0.279	0.000	0.162	0.000	0.006	0.000	0.000
99	9	>10E6	>10E6	>10E6	1	0.226	0.215	0.000	0.136	0.000	0.016	0.000	0.000
100	6	43747	>10E6	>10E6	1	0.205	0.627	0.000	0.491	0.000	0.241	0.000	0.000

Table 42: Topology Identification Results for Three Bus System with Input Noise (Cases 1 and 2)

Case	Performance Indices				Correct	Topology 1		Topology2		Topology 3		Topology 4	
	PI top 1	PI top 2	PI top 3	PI top 4	Topology	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)
1	21	75	7803	>10E6	1	0.059	0.239	0.015	0.105	0.000	0.007	0.733	0.000
2	16	>10E6	>10E6	>10E6	1	0.082	0.241	0.000	0.146	0.000	0.011	0.000	0.000
3	19	>10E6	>10E6	>10E6	1	0.069	0.200	0.000	0.088	0.000	0.005	0.000	0.000
4	22	>10E6	>10E6	>10E6	1	0.064	0.162	0.000	0.068	0.000	0.024	0.000	0.000
5	27	>10E6	>10E6	>10E6	1	0.045	0.203	0.000	0.104	0.000	0.013	0.000	0.059
6	22	>10E6	>10E6	>10E6	1	0.053	0.305	0.000	0.229	0.000	0.015	0.000	0.000
7	47	>10E6	>10E6	>10E6	1	0.023	0.320	0.000	0.257	0.000	0.013	0.000	0.000
8	17	>10E6	>10E6	>10E6	1	0.077	0.248	0.000	0.152	0.000	0.012	0.000	0.653
9	18	>10E6	>10E6	>10E6	1	0.077	0.194	0.000	0.088	0.000	0.006	0.000	0.000
10	52	>10E6	>10E6	>10E6	1	0.022	0.145	0.000	0.091	0.000	0.014	0.000	0.000
11	17	2469213	>10E6	>10E6	1	0.080	0.208	0.000	0.110	0.000	0.006	0.001	0.000
12	29	>10E6	>10E6	>10E6	1	0.041	0.215	0.000	0.123	0.000	0.011	0.000	0.000
13	17	987372	>10E6	>10E6	1	0.090	0.179	0.000	0.092	0.000	0.007	0.029	0.000
14	35	>10E6	>10E6	>10E6	1	0.031	0.417	0.000	0.315	0.000	0.007	0.000	0.000
15	15	>10E6	>10E6	>10E6	1	0.079	0.458	0.000	0.304	0.000	0.008	0.000	0.000
16	21	>10E6	>10E6	>10E6	1	0.056	0.276	0.000	0.173	0.000	0.012	0.000	0.000
17	23	>10E6	>10E6	>10E6	1	0.054	0.220	0.000	0.145	0.000	0.007	0.000	0.000
18	39	>10E6	>10E6	>10E6	1	0.030	0.201	0.000	0.107	0.000	0.006	0.000	0.000
19	21	>10E6	>10E6	>10E6	1	0.066	0.172	0.000	0.091	0.000	0.011	0.000	0.000
20	19	>10E6	>10E6	>10E6	1	0.072	0.196	0.000	0.094	0.000	0.014	0.000	0.000
21	16	>10E6	>10E6	>10E6	1	0.088	0.241	0.000	0.117	0.000	0.013	0.000	0.000
22	17	>10E6	>10E6	>10E6	1	0.078	0.261	0.000	0.160	0.000	0.012	0.000	0.002
23	24	202297	>10E6	>10E6	1	0.052	0.202	0.000	0.122	0.000	0.013	0.000	0.000
24	21	6893640	>10E6	>10E6	1	0.057	0.261	0.000	0.158	0.000	0.012	0.000	0.000
25	19	>10E6	>10E6	>10E6	1	0.073	0.204	0.000	0.098	0.000	0.005	0.019	0.000
26	28	>10E6	>10E6	>10E6	1	0.039	0.364	0.000	0.272	0.000	0.025	0.000	0.064
27	36	4049387	>10E6	>10E6	1	0.032	0.215	0.000	0.108	0.000	0.007	0.000	0.000
28	50	>10E6	>10E6	>10E6	1	0.022	0.270	0.000	0.194	0.000	0.017	0.000	0.001
29	41	27046	>10E6	>10E6	1	0.029	0.147	0.000	0.062	0.000	0.005	0.474	0.000
30	44	>10E6	>10E6	>10E6	1	0.026	0.222	0.000	0.152	0.000	0.014	0.000	0.007
31	25	>10E6	>10E6	>10E6	1	0.047	0.242	0.000	0.109	0.000	0.006	0.000	0.000
32	29	>10E6	>10E6	>10E6	1	0.044	0.163	0.000	0.091	0.000	0.013	0.000	0.000
33	16	>10E6	>10E6	>10E6	1	0.081	0.263	0.000	0.163	0.000	0.007	0.000	0.000
34	15	2721420	>10E6	>10E6	1	0.080	0.450	0.000	0.315	0.000	0.008	0.000	0.000
35	14	14	2610	8	**4**	0.128	0.168	0.413	0.085	0.000	0.006	0.160	0.568
36	56	1066239	>10E6	>10E6	1	0.023	0.077	0.000	0.035	0.000	0.007	0.101	0.000
37	26	>10E6	>10E6	>10E6	1	0.042	0.402	0.000	0.309	0.000	0.015	0.000	0.000
38	18	22	93564	>10E6	1	0.082	0.158	0.165	0.063	0.000	0.006	0.054	0.000
39	25	>10E6	>10E6	>10E6	1	0.045	0.385	0.000	0.285	0.000	0.012	0.000	0.000
40	65	>10E6	>10E6	>10E6	1	0.016	0.309	0.000	0.249	0.000	0.012	0.000	0.000
41	20	>10E6	>10E6	>10E6	1	0.062	0.233	0.000	0.147	0.000	0.011	0.000	0.000
42	26	>10E6	>10E6	>10E6	1	0.051	0.156	0.000	0.058	0.000	0.007	0.003	0.000
43	17	>10E6	>10E6	>10E6	1	0.080	0.247	0.000	0.121	0.000	0.007	0.000	0.000
44	38	>10E6	>10E6	>10E6	1	0.031	0.182	0.000	0.118	0.000	0.012	0.000	0.000
45	22	>10E6	>10E6	>10E6	1	0.054	0.277	0.000	0.158	0.000	0.011	0.000	0.000
46	23	>10E6	>10E6	>10E6	1	0.059	0.180	0.000	0.091	0.000	0.023	0.000	0.000
47	18	>10E6	>10E6	>10E6	1	0.071	0.265	0.000	0.153	0.000	0.005	0.000	0.000
48	23	>10E6	>10E6	>10E6	1	0.052	0.286	0.000	0.202	0.000	0.023	0.000	0.000
49	32	>10E6	>10E6	>10E6	1	0.043	0.115	0.000	0.032	0.000	0.007	0.069	0.000
50	17	>10E6	>10E6	>10E6	1	0.069	0.453	0.000	0.326	0.000	0.007	0.000	0.000
51	18	>10E6	>10E6	>10E6	1	0.071	0.246	0.000	0.120	0.000	0.012	0.000	0.000
52	27	17086	29567	>10E6	1	0.044	0.235	0.000	0.143	0.000	0.008	0.051	0.000
53	22	>10E6	>10E6	>10E6	1	0.066	0.143	0.000	0.061	0.000	0.011	0.099	0.000
54	21	>10E6	>10E6	>10E6	1	0.059	0.223	0.000	0.108	0.000	0.012	0.000	0.000
55	21	>10E6	>10E6	>10E6	1	0.058	0.248	0.000	0.155	0.000	0.012	0.000	0.000
56	37	>10E6	>10E6	>10E6	1	0.031	0.195	0.000	0.121	0.000	0.008	0.000	0.000
57	22	>10E6	>10E6	>10E6	1	0.066	0.145	0.000	0.068	0.000	0.008	0.000	0.000
58	16	>10E6	>10E6	>10E6	1	0.084	0.243	0.000	0.119	0.000	0.006	0.000	0.192
59	17	>10E6	>10E6	>10E6	1	0.071	0.358	0.000	0.263	0.000	0.013	0.000	0.000
60	11	8	185	34	**2**	0.131	0.309	0.388	0.185	0.818	0.005	0.030	0.845
61	16	5698704	>10E6	>10E6	1	0.081	0.263	0.000	0.154	0.000	0.007	0.000	0.000
62	52	>10E6	>10E6	>10E6	1	0.021	0.232	0.000	0.170	0.000	0.026	0.000	0.000
63	18	>10E6	>10E6	>10E6	1	0.090	0.144	0.000	0.053	0.000	0.007	0.427	0.000
64	20	>10E6	>10E6	>10E6	1	0.062	0.296	0.000	0.190	0.000	0.008	0.000	0.001
65	18	>10E6	>10E6	>10E6	1	0.074	0.211	0.000	0.097	0.000	0.013	0.000	0.000
66	17	>10E6	>10E6	>10E6	1	0.078	0.252	0.000	0.127	0.000	0.024	0.000	0.082
67	36	>10E6	>10E6	>10E6	1	0.032	0.198	0.000	0.108	0.000	0.014	0.002	0.000
68	50	73646	>10E6	>10E6	1	0.029	0.065	0.000	0.032	0.000	0.002	0.571	0.000
69	20	>10E6	>10E6	>10E6	1	0.063	0.235	0.000	0.144	0.000	0.003	0.000	0.000
70	21	>10E6	>10E6	>10E6	1	0.075	0.134	0.000	0.027	0.000	0.011	0.211	0.000
71	45	>10E6	>10E6	>10E6	1	0.024	0.275	0.000	0.180	0.000	0.008	0.000	0.000
72	34	>10E6	>10E6	352265	1	0.035	0.193	0.000	0.101	0.000	0.011	0.000	0.045
73	28	>10E6	98	>10E6	1	0.055	0.106	0.000	0.016	0.035	0.014	0.000	0.000
74	16	>10E6	>10E6	>10E6	1	0.076	0.323	0.000	0.233	0.000	0.008	0.000	0.000
75	36	>10E6	>10E6	>10E6	1	0.034	0.146	0.000	0.060	0.000	0.018	0.477	0.000
76	20	>10E6	>10E6	1420087	1	0.062	0.240	0.000	0.126	0.000	0.013	0.000	0.017
77	23	28	1499649	>10E6	1	0.058	0.172	0.112	0.052	0.000	0.005	0.085	0.000
78	23	>10E6	>10E6	>10E6	1	0.049	0.400	0.000	0.296	0.000	0.011	0.000	0.000
79	24	>10E6	>10E6	>10E6	1	0.048	0.331	0.000	0.243	0.000	0.012	0.000	0.000
80	30	>10E6	>10E6	>10E6	1	0.038	0.251	0.000	0.157	0.000	0.011	0.000	0.000
81	22	826507	>10E6	>10E6	1	0.061	0.193	0.000	0.084	0.000	0.008	0.895	0.000
82	19	>10E6	>10E6	>10E6	1	0.071	0.198	0.000	0.086	0.000	0.013	0.039	0.000
83	21	>10E6	>10E6	320	1	0.058	0.244	0.000	0.124	0.000	0.013	0.055	0.003
84	33	>10E6	>10E6	>10E6	1	0.035	0.278	0.000	0.200	0.000	0.012	0.000	0.000
85	39	>10E6	>10E6	>10E6	1	0.027	0.397	0.000	0.304	0.000	0.013	0.000	0.000
86	16	2778759	>10E6	>10E6	1	0.087	0.251	0.000	0.144	0.000	0.003	0.000	0.000
87	32	>10E6	>10E6	>10E6	1	0.038	0.168	0.000	0.063	0.000	0.011	0.000	0.000
88	29	>10E6	>10E6	>10E6	1	0.040	0.216	0.000	0.120	0.000	0.007	0.000	0.099
89	18	348	79247	>10E6	1	0.074	0.221	0.003	0.103	0.000	0.008	0.898	0.000
90	18	>10E6	>10E6	>10E6	1	0.084	0.156	0.000	0.056	0.000	0.012	0.116	0.000
91	33	>10E6	>10E6	>10E6	1	0.036	0.212	0.000	0.152	0.000	0.013	0.000	0.000
92	28	>10E6	>10E6	>10E6	1	0.041	0.305	0.000	0.208	0.000	0.011	0.000	0.000
93	16	78502	88605	>10E6	1	0.088	0.203	0.000	0.109	0.000	0.005	0.218	0.000
94	15	>10E6	>10E6	>10E6	1	0.083	0.321	0.000	0.205	0.000	0.013	0.000	0.000
95	14	>10E6	>10E6	>10E6	1	0.081	0.585	0.000	0.501	0.000	0.007	0.000	0.000
96	27	>10E6	>10E6	>10E6	1	0.050	0.158	0.000	0.049	0.000	0.007	0.701	0.000
97	24	94945	163	>10E6	1	0.048	0.334	0.000	0.229	0.014	0.011	0.000	0.000
98	46	180	6268	>10E6	1	0.024	0.234	0.006	0.162	0.000	0.017	0.066	0.000
99	19	>10E6	>10E6	>10E6	1	0.087	0.126	0.000	0.032	0.000	0.011	0.278	0.000
100	28	44	>10E6	>10E6	1	0.055	0.104	0.627	0.024	0.000	0.012	0.000	0.000

Table 43: Topology Identification Results for Three Bus System (Case 1 only)

	Performance Indices				Correct	Topology 1	Topology2	Topology 3	Topology 4			Performance Indices				Correct	Topology 1	Topology2	Topology 3	Topology 4
Case	PI top 1	PI top 2	PI top 3	PI top 4	Topology	P(m1)	P(m1)	P(m1)	P(m1)		**Case**	PI top 1	PI top 2	PI top 3	PI top 4	Topology	P(m1)	P(m1)	P(m1)	P(m1)
1	17	65	7666	1	**4**	0.059	0.015	0.000	0.733		51	14	>10E6	>10E6	84300	1	0.071	0.000	0.000	0.000
2	12	>10E6	>10E6	>10E6	1	0.082	0.000	0.000	0.000		52	23	17079	29442	20	**4**	0.044	0.000	0.000	0.051
3	14	>10E6	>10E6	>10E6	1	0.069	0.000	0.000	0.000		53	15	>10E6	>10E6	10	**4**	0.066	0.000	0.000	0.099
4	16	>10E6	>10E6	84627	1	0.064	0.000	0.000	0.000		54	17	>10E6	>10E6	247008	1	0.059	0.000	0.000	0.000
5	22	>10E6	>10E6	>10E6	1	0.045	0.000	0.000	0.000		55	17	>10E6	>10E6	>10E6	1	0.058	0.000	0.000	0.000
6	19	>10E6	>10E6	>10E6	1	0.053	0.000	0.000	0.000		56	32	>10E6	>10E6	>10E6	1	0.031	0.000	0.000	0.000
7	44	>10E6	>10E6	>10E6	1	0.023	0.000	0.000	0.000		57	15	>10E6	>10E6	>10E6	1	0.066	0.000	0.000	0.000
8	13	>10E6	>10E6	>10E6	1	0.077	0.000	0.000	0.000		58	12	>10E6	>10E6	>10E6	1	0.084	0.000	0.000	0.000
9	13	>10E6	>10E6	>10E6	1	0.077	0.000	0.000	0.000		59	14	>10E6	>10E6	>10E6	1	0.071	0.000	0.000	0.000
10	45	>10E6	>10E6	>10E6	1	0.022	0.000	0.000	0.000		60	8	3	1	33	**3**	0.131	0.388	0.818	0.030
11	12	2469204	>10E6	1137	1	0.080	0.000	0.000	0.001		61	12	5698698	>10E6	>10E6	1	0.081	0.000	0.000	0.000
12	24	>10E6	>10E6	>10E6	1	0.041	0.000	0.000	0.000		62	48	>10E6	>10E6	>10E6	1	0.021	0.000	0.000	0.000
13	11	987362	>10E6	34	1	0.090	0.000	0.000	0.029		63	11	>10E6	>10E6	2	**4**	0.090	0.000	0.000	0.427
14	33	>10E6	>10E6	>10E6	1	0.031	0.000	0.000	0.000		64	16	>10E6	>10E6	>10E6	1	0.062	0.000	0.000	0.000
15	13	>10E6	>10E6	>10E6	1	0.079	0.000	0.000	0.000		65	13	>10E6	>10E6	>10E6	1	0.074	0.000	0.000	0.000
16	18	>10E6	>10E6	>10E6	1	0.056	0.000	0.000	0.000		66	13	>10E6	>10E6	>10E6	1	0.078	0.000	0.000	0.000
17	18	>10E6	>10E6	>10E6	1	0.054	0.000	0.000	0.000		67	31	>10E6	>10E6	442	1	0.032	0.000	0.000	0.002
18	34	>10E6	>10E6	9216	1	0.030	0.000	0.000	0.000		68	34	73615	>10E6	2	**4**	0.029	0.000	0.000	0.571
19	15	>10E6	>10E6	>10E6	1	0.066	0.000	0.000	0.000		69	16	>10E6	>10E6	>10E6	1	0.063	0.000	0.000	0.000
20	14	>10E6	>10E6	>10E6	1	0.072	0.000	0.000	0.000		70	13	>10E6	>10E6	5	**4**	0.075	0.000	0.000	0.211
21	11	>10E6	>10E6	>10E6	1	0.088	0.000	0.000	0.000		71	42	>10E6	>10E6	>10E6	1	0.024	0.000	0.000	0.000
22	13	>10E6	>10E6	>10E6	1	0.078	0.000	0.000	0.000		72	28	>10E6	>10E6	352243	1	0.035	0.000	0.000	0.000
23	19	202288	>10E6	90789	1	0.052	0.000	0.000	0.000		73	18	>10E6	28	>10E6	1	0.055	0.000	0.035	0.000
24	17	6893634	>10E6	>10E6	1	0.057	0.000	0.000	0.000		74	13	>10E6	>10E6	>10E6	1	0.076	0.000	0.000	0.000
25	14	>10E6	>10E6	52	1	0.073	0.000	0.000	0.019		75	29	>10E6	>10E6	2	**4**	0.034	0.000	0.000	0.477
26	26	>10E6	>10E6	>10E6	1	0.039	0.000	0.000	0.000		76	16	>10E6	>10E6	1420028	1	0.062	0.000	0.000	0.000
27	31	4049378	>10E6	>10E6	1	0.032	0.000	0.000	0.000		77	17	9	1499446	12	**2**	0.058	0.112	0.000	0.085
28	46	>10E6	>10E6	>10E6	1	0.022	0.000	0.000	0.000		78	20	>10E6	>10E6	>10E6	1	0.049	0.000	0.000	0.000
29	34	27030	>10E6	2	**4**	0.029	0.000	0.000	0.474		79	21	>10E6	>10E6	>10E6	1	0.048	0.000	0.000	0.000
30	39	>10E6	>10E6	>10E6	1	0.026	0.000	0.000	0.000		80	26	>10E6	>10E6	>10E6	1	0.038	0.000	0.000	0.000
31	21	>10E6	>10E6	>10E6	1	0.047	0.000	0.000	0.000		81	16	826495	>10E6	1	**4**	0.061	0.000	0.000	0.895
32	23	>10E6	>10E6	>10E6	1	0.044	0.000	0.000	0.000		82	14	>10E6	>10E6	25	1	0.071	0.000	0.000	0.039
33	12	>10E6	>10E6	>10E6	1	0.081	0.000	0.000	0.000		83	17	>10E6	>10E6	18	1	0.058	0.000	0.000	0.055
34	13	2721417	>10E6	>10E6	1	0.080	0.000	0.000	0.000		84	29	>10E6	>10E6	>10E6	1	0.035	0.000	0.000	0.000
35	8	2	2429	6	**2**	0.128	0.413	0.000	0.160		85	37	>10E6	>10E6	>10E6	1	0.027	0.000	0.000	0.000
36	43	1066210	>10E6	10	**4**	0.023	0.000	0.000	0.101		86	12	2778752	>10E6	>10E6	1	0.087	0.000	0.000	0.000
37	24	>10E6	>10E6	>10E6	1	0.042	0.000	0.000	0.000		87	26	>10E6	>10E6	>10E6	1	0.038	0.000	0.000	0.000
38	12	6	93390	19	**2**	0.082	0.165	0.000	0.054		88	25	>10E6	>10E6	>10E6	1	0.040	0.000	0.000	0.000
39	22	>10E6	>10E6	>10E6	1	0.045	0.000	0.000	0.000		89	14	338	79122	1	**4**	0.074	0.003	0.000	0.898
40	62	>10E6	>10E6	>10E6	1	0.016	0.000	0.000	0.000		90	12	>10E6	>10E6	9	**4**	0.084	0.000	0.000	0.116
41	16	>10E6	>10E6	>10E6	1	0.062	0.000	0.000	0.000		91	28	>10E6	>10E6	>10E6	1	0.036	0.000	0.000	0.000
42	20	>10E6	>10E6	394	1	0.051	0.000	0.000	0.003		92	24	>10E6	>10E6	>10E6	1	0.041	0.000	0.000	0.000
43	12	>10E6	>10E6	>10E6	1	0.080	0.000	0.000	0.000		93	11	78493	88417	5	**4**	0.088	0.000	0.000	0.218
44	33	>10E6	>10E6	>10E6	1	0.031	0.000	0.000	0.000		94	12	>10E6	>10E6	>10E6	1	0.083	0.000	0.000	0.000
45	18	>10E6	>10E6	>10E6	1	0.054	0.000	0.000	0.000		95	12	>10E6	>10E6	>10E6	1	0.081	0.000	0.000	0.000
46	17	>10E6	>10E6	76472	1	0.059	0.000	0.000	0.000		96	20	>10E6	>10E6	1	**4**	0.050	0.000	0.000	0.701
47	14	>10E6	>10E6	>10E6	1	0.071	0.000	0.000	0.000		97	21	94940	72	17250	1	0.048	0.000	0.014	0.000
48	19	>10E6	>10E6	>10E6	1	0.052	0.000	0.000	0.000		98	42	174	6208	15	**4**	0.024	0.006	0.000	0.066
49	23	>10E6	>10E6	15	**4**	0.043	0.000	0.000	0.069		99	11	>10E6	>10E6	4	**4**	0.087	0.000	0.000	0.278
50	14	>10E6	>10E6	>10E6	1	0.069	0.000	0.000	0.000		100	18	2	>10E6	9966214	**2**	0.055	0.627	0.000	0.000

Table 44: Topology Identification Results for Three Bus System (Case 2 only)

	Performance Indices				Correct	Topology 1	Topology2	Topology 3	Topology 4
Case	PI top 1	PI top 2	PI top 3	PI top 4	Topology	P(m2)	P(m2)	P(m2)	P(m2)
1	4	10	138	>10E6	1	0.239	0.105	0.007	0.000
2	4	7	88	>10E6	1	0.241	0.146	0.011	0.000
3	5	11	193	>10E6	1	0.200	0.088	0.005	0.000
4	6	15	41	>10E6	1	0.162	0.068	0.024	0.000
5	5	10	79	17	1	0.203	0.104	0.013	0.059
6	3	4	67	>10E6	1	0.305	0.229	0.015	0.000
7	3	4	74	1874207	1	0.320	0.257	0.013	0.000
8	4	7	81	2	**4**	0.248	0.152	0.012	0.653
9	5	11	178	>10E6	1	0.194	0.088	0.006	0.000
10	7	11	71	>10E6	1	0.145	0.091	0.014	0.000
11	5	9	181	>10E6	1	0.208	0.110	0.006	0.000
12	5	8	88	>10E6	1	0.215	0.123	0.011	0.000
13	6	11	143	>10E6	1	0.179	0.092	0.007	0.000
14	2	3	135	>10E6	1	0.417	0.315	0.007	0.000
15	2	3	126	>10E6	1	0.458	0.304	0.008	0.000
16	4	6	86	>10E6	1	0.276	0.173	0.012	0.000
17	5	7	147	27649	1	0.220	0.145	0.007	0.000
18	5	9	174	>10E6	1	0.201	0.107	0.006	0.000
19	6	11	91	>10E6	1	0.172	0.091	0.011	0.000
20	5	11	70	>10E6	1	0.196	0.094	0.014	0.000
21	4	9	78	>10E6	1	0.241	0.117	0.013	0.000
22	4	6	87	428	1	0.261	0.160	0.012	0.002
23	5	8	75	>10E6	1	0.202	0.122	0.013	0.000
24	4	6	86	7920473	1	0.261	0.158	0.012	0.000
25	5	10	203	>10E6	1	0.204	0.098	0.005	0.000
26	3	4	41	16	1	0.364	0.272	0.025	0.064
27	5	9	134	>10E6	1	0.215	0.108	0.007	0.000
28	4	5	59	1207	1	0.270	0.194	0.017	0.001
29	7	16	207	>10E6	1	0.147	0.062	0.005	0.000
30	5	7	74	152	1	0.222	0.152	0.014	0.007
31	4	9	173	>10E6	1	0.242	0.109	0.006	0.000
32	6	11	80	>10E6	1	0.163	0.091	0.013	0.000
33	4	6	136	123139	1	0.263	0.163	0.007	0.000
34	2	3	133	>10E6	1	0.450	0.315	0.008	0.000
35	6	12	182	2	**4**	0.168	0.085	0.006	0.568
36	13	29	137	>10E6	1	0.077	0.035	0.007	0.000
37	2	3	69	>10E6	1	0.402	0.309	0.015	0.000
38	6	16	174	>10E6	1	0.158	0.063	0.006	0.000
39	3	4	85	>10E6	1	0.385	0.285	0.012	0.000
40	3	4	87	6983306	1	0.309	0.249	0.012	0.000
41	4	7	90	7211758	1	0.233	0.147	0.011	0.000
42	6	17	138	>10E6	1	0.156	0.058	0.007	0.000
43	4	8	152	31393	1	0.247	0.121	0.007	0.000
44	5	8	82	>10E6	1	0.182	0.118	0.012	0.000
45	4	6	91	>10E6	1	0.277	0.158	0.011	0.000
46	6	11	43	>10E6	1	0.180	0.091	0.023	0.000
47	4	7	189	>10E6	1	0.265	0.153	0.005	0.000
48	3	5	43	6188564	1	0.286	0.202	0.023	0.000
49	9	31	148	>10E6	1	0.115	0.032	0.007	0.000
50	2	3	149	>10E6	1	0.453	0.326	0.007	0.000
51	4	8	86	>10E6	1	0.246	0.120	0.012	0.000
52	4	7	126	>10E6	1	0.235	0.143	0.008	0.000
53	7	16	91	>10E6	1	0.143	0.061	0.011	0.000
54	4	9	81	>10E6	1	0.223	0.108	0.012	0.000
55	4	6	86	>10E6	1	0.248	0.155	0.012	0.000
56	5	8	124	>10E6	1	0.195	0.121	0.008	0.000
57	7	15	127	9498	1	0.145	0.068	0.008	0.000
58	4	8	170	5	1	0.243	0.119	0.006	0.192
59	3	4	79	>10E6	1	0.358	0.263	0.013	0.000
60	3	5	184	1	**4**	0.309	0.185	0.005	0.845
61	4	6	147	>10E6	1	0.263	0.154	0.007	0.000
62	4	6	38	>10E6	1	0.232	0.170	0.026	0.000
63	7	19	152	>10E6	1	0.144	0.053	0.007	0.000
64	3	5	132	1479	1	0.296	0.190	0.008	0.001
65	5	10	78	>10E6	1	0.211	0.097	0.013	0.000
66	4	8	42	12	1	0.252	0.127	0.024	0.082
67	5	9	73	>10E6	1	0.198	0.108	0.014	0.000
68	15	31	422	>10E6	1	0.065	0.032	0.002	0.000
69	4	7	355	>10E6	1	0.235	0.144	0.003	0.000
70	7	36	89	>10E6	1	0.134	0.027	0.011	0.000
71	4	6	126	>10E6	1	0.275	0.180	0.008	0.000
72	5	10	87	22	1	0.193	0.101	0.011	0.045
73	9	62	70	>10E6	1	0.106	0.016	0.014	0.000
74	3	4	127	28547	1	0.323	0.233	0.008	0.000
75	7	17	55	>10E6	1	0.146	0.060	0.018	0.000
76	4	8	79	59	1	0.240	0.126	0.013	0.017
77	6	19	203	>10E6	1	0.172	0.052	0.005	0.000
78	3	3	88	>10E6	1	0.400	0.296	0.011	0.000
79	3	4	86	>10E6	1	0.331	0.243	0.012	0.000
80	4	6	87	>10E6	1	0.251	0.157	0.011	0.000
81	5	12	132	>10E6	1	0.193	0.084	0.008	0.000
82	5	12	79	>10E6	1	0.198	0.086	0.013	0.000
83	4	8	75	302	1	0.244	0.124	0.013	0.003
84	4	5	82	>10E6	1	0.278	0.200	0.012	0.000
85	3	3	75	1846919	1	0.397	0.304	0.013	0.000
86	4	7	288	>10E6	1	0.251	0.144	0.003	0.000
87	6	16	90	>10E6	1	0.168	0.063	0.011	0.000
88	5	8	150	10	1	0.216	0.120	0.007	0.099
89	5	10	125	>10E6	1	0.221	0.103	0.008	0.000
90	6	18	85	>10E6	1	0.156	0.056	0.012	0.000
91	5	7	75	>10E6	1	0.212	0.152	0.013	0.000
92	3	5	90	>10E6	1	0.305	0.208	0.011	0.000
93	5	9	188	>10E6	1	0.203	0.109	0.005	0.000
94	3	5	79	>10E6	1	0.321	0.205	0.013	0.000
95	2	2	143	>10E6	1	0.585	0.501	0.007	0.000
96	6	20	146	>10E6	1	0.158	0.049	0.007	0.000
97	3	4	90	>10E6	1	0.334	0.229	0.011	0.000
98	4	6	60	>10E6	1	0.234	0.162	0.017	0.000
99	8	31	92	>10E6	1	0.126	0.032	0.011	0.000
100	10	42	82	>10E6	1	0.104	0.024	0.012	0.000

Table 45: Topology Identification Results for Three Bus System with Input and Output Noise

	Performance Indices				Correct	Topology 1		Topology2		Topology 3		Topology 4	
Case	PI top 1	PI top 2	PI top 3	PI top 4	Topology	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)	P(m1)	P(m2)
1	29	174458	>10E6	>10E6	1	0.886	0.035	0.000	0.098	0.000	0.003	0.000	0.000
2	79	12264	>10E6	>10E6	1	0.013	0.255	0.000	0.193	0.000	0.484	0.000	0.000
3	4	1433159	>10E6	>10E6	1	0.604	0.447	0.000	0.855	0.000	0.070	0.000	0.000
4	4	>10E6	>10E6	>10E6	1	0.342	0.909	0.000	0.551	0.000	0.490	0.000	0.000
5	4	>10E6	>10E6	>10E6	1	0.708	0.362	0.000	0.875	0.000	0.122	0.000	0.024
6	4	398332	>10E6	>10E6	1	0.477	0.611	0.000	0.374	0.000	0.680	0.000	0.000
7	27	>10E6	>10E6	>10E6	1	0.043	0.275	0.000	0.651	0.000	0.066	0.000	0.000
8	10	1325	>10E6	>10E6	1	0.123	0.624	0.001	0.151	0.000	0.156	0.000	0.144
9	5	29218	>10E6	>10E6	1	0.560	0.332	0.000	0.090	0.000	0.080	0.000	0.000
10	3	>10E6	>10E6	>10E6	1	0.728	0.883	0.000	0.312	0.000	0.843	0.000	0.000
11	4	8027286	>10E6	>10E6	1	0.733	0.467	0.000	0.906	0.000	0.063	0.000	0.000
12	5	>10E6	>10E6	>10E6	1	0.985	0.249	0.000	0.228	0.000	0.021	0.000	0.000
13	6	>10E6	>10E6	>10E6	1	0.363	0.325	0.000	0.749	0.000	0.037	0.000	0.000
14	14	>10E6	>10E6	>10E6	1	0.088	0.336	0.000	0.786	0.000	0.035	0.000	0.000
15	6	6004887	>10E6	>10E6	1	0.246	0.696	0.000	0.347	0.000	0.029	0.000	0.000
16	11	1693	>10E6	>10E6	1	0.571	0.109	0.001	0.621	0.000	0.574	0.000	0.000
17	13	>10E6	>10E6	>10E6	1	0.089	0.687	0.000	0.850	0.000	0.026	0.000	0.002
18	3	3056222	>10E6	>10E6	1	0.866	0.451	0.000	0.367	0.000	0.006	0.000	0.000
19	8	494640	>10E6	>10E6	1	0.290	0.208	0.000	0.177	0.000	0.534	0.000	0.000
20	11	6887244	>10E6	>10E6	1	0.108	0.702	0.000	0.080	0.000	0.661	0.000	0.000
21	3	>10E6	>10E6	>10E6	1	0.913	0.701	0.000	0.384	0.000	0.194	0.000	0.000
22	41	6068	>10E6	>10E6	1	0.027	0.250	0.000	0.404	0.000	0.693	0.000	0.284
23	6	86	>10E6	>10E6	1	0.277	0.468	0.012	0.282	0.000	0.387	0.000	0.000
24	3	60149	>10E6	>10E6	1	0.750	0.797	0.000	0.724	0.000	0.420	0.000	0.001
25	15	55578	>10E6	>10E6	1	0.401	0.079	0.000	0.136	0.000	0.001	0.000	0.000
26	4	531793	>10E6	>10E6	1	0.561	0.558	0.000	0.415	0.000	0.054	0.000	0.291
27	6	>10E6	>10E6	>10E6	1	0.973	0.194	0.000	0.525	0.000	0.386	0.000	0.000
28	3	>10E6	>10E6	>10E6	1	0.539	0.614	0.000	0.835	0.000	0.128	0.000	0.293
29	8	428742	>10E6	>10E6	1	0.910	0.139	0.000	0.136	0.000	0.018	0.000	0.000
30	10	>10E6	>10E6	>10E6	1	0.126	0.456	0.000	0.452	0.000	0.165	0.000	0.054
31	40	462492	>10E6	>10E6	1	0.031	0.134	0.000	0.630	0.000	0.555	0.000	0.000
32	2	>10E6	>10E6	>10E6	1	0.947	0.928	0.000	0.668	0.000	0.144	0.000	0.000
33	5	>10E6	>10E6	>10E6	1	0.533	0.349	0.000	0.770	0.000	0.538	0.000	0.001
34	2	20401	>10E6	>10E6	1	0.906	0.742	0.000	0.701	0.000	0.174	0.000	0.000
35	6	1502	>10E6	>10E6	1	0.658	0.206	0.001	0.172	0.000	0.009	0.000	0.784
36	3	3458383	>10E6	>10E6	1	0.872	0.471	0.000	0.448	0.000	0.393	0.000	0.000
37	6	31400	>10E6	>10E6	1	0.247	0.495	0.000	0.617	0.000	0.756	0.000	0.000
38	37	1215265	>10E6	>10E6	1	0.258	0.031	0.000	0.087	0.000	0.074	0.000	0.000
39	9	5333	>10E6	>10E6	1	0.146	0.506	0.000	0.132	0.000	0.017	0.000	0.019
40	9	>10E6	>10E6	>10E6	1	0.126	0.657	0.000	0.574	0.000	0.427	0.000	0.001
41	3	>10E6	>10E6	>10E6	1	0.715	0.837	0.000	0.142	0.000	0.191	0.000	0.000
42	2	575974	>10E6	>10E6	1	0.850	0.897	0.000	0.439	0.000	0.116	0.000	0.000
43	5	2344215	>10E6	>10E6	1	0.382	0.461	0.000	0.866	0.000	0.037	0.000	0.029
44	249	>10E6	>10E6	>10E6	1	0.004	0.055	0.000	0.730	0.000	0.255	0.000	0.000
45	26	10227	>10E6	>10E6	1	0.040	0.853	0.000	0.191	0.000	0.898	0.000	0.000
46	4	388645	>10E6	>10E6	1	0.979	0.382	0.000	0.388	0.000	0.087	0.000	0.000
47	9	107851	>10E6	>10E6	1	0.510	0.144	0.000	0.260	0.000	0.106	0.000	0.000
48	85	27845	>10E6	>10E6	1	0.020	0.029	0.000	0.557	0.000	0.871	0.000	0.017
49	7	>10E6	>10E6	>10E6	1	0.344	0.255	0.000	0.324	0.000	0.235	0.000	0.000
50	3	>10E6	>10E6	>10E6	1	0.961	0.474	0.000	0.419	0.000	0.099	0.000	0.000
51	11	41720	>10E6	>10E6	1	0.103	0.817	0.000	0.076	0.000	0.204	0.000	0.000
52	5	>10E6	>10E6	>10E6	1	0.483	0.345	0.000	0.015	0.000	0.030	0.000	0.000
53	3	1060613	>10E6	>10E6	1	0.811	0.593	0.000	0.391	0.000	0.380	0.000	0.000
54	5	61164	>10E6	>10E6	1	0.334	0.485	0.000	0.487	0.000	0.169	0.000	0.000
55	3	1247430	>10E6	>10E6	1	0.970	0.580	0.000	0.466	0.000	0.028	0.000	0.000
56	3	>10E6	>10E6	>10E6	1	0.461	0.764	0.000	0.863	0.000	0.161	0.000	0.000
57	2	>10E6	>10E6	>10E6	1	0.744	0.917	0.000	0.711	0.000	0.694	0.000	0.065
58	3	>10E6	>10E6	>10E6	1	0.628	0.715	0.000	0.893	0.000	0.180	0.000	0.001
59	20	25780	>10E6	>10E6	1	0.823	0.052	0.000	0.005	0.000	0.624	0.000	0.000
60	18	491748	>10E6	>10E6	1	0.795	0.060	0.000	0.098	0.000	0.006	0.000	0.126
61	3	133433	>10E6	>10E6	1	0.785	0.521	0.000	0.879	0.000	0.018	0.000	0.000
62	4	2924590	>10E6	>10E6	1	0.971	0.330	0.000	0.133	0.000	0.397	0.000	0.000
63	3	>10E6	>10E6	>10E6	1	0.601	0.777	0.000	0.472	0.000	0.068	0.000	0.000
64	4	3958140	>10E6	>10E6	1	0.410	0.731	0.000	0.478	0.000	0.316	0.000	0.000
65	3	3166116	>10E6	>10E6	1	0.805	0.517	0.000	0.311	0.000	0.565	0.000	0.000
66	5	40005	>10E6	>10E6	1	0.573	0.360	0.000	0.721	0.000	0.443	0.000	0.558
67	9	>10E6	>10E6	>10E6	1	0.154	0.368	0.000	0.726	0.000	0.080	0.000	0.000
68	7	767	>10E6	>10E6	1	0.221	0.354	0.001	0.192	0.000	0.040	0.000	0.000
69	2	919886	>10E6	>10E6	1	0.720	0.927	0.000	0.719	0.000	0.281	0.000	0.000
70	3	198562	>10E6	>10E6	1	0.851	0.710	0.000	0.795	0.000	0.657	0.000	0.000
71	28	>10E6	>10E6	>10E6	1	0.038	0.805	0.000	0.275	0.000	0.133	0.000	0.000
72	4	>10E6	>10E6	>10E6	1	0.660	0.461	0.000	0.439	0.000	0.529	0.000	0.225
73	4	>10E6	>10E6	>10E6	1	0.754	0.333	0.000	0.010	0.000	0.060	0.000	0.000
74	5	4703	>10E6	>10E6	1	0.431	0.451	0.000	0.678	0.000	0.494	0.000	0.016
75	4	7532183	>10E6	>10E6	1	0.381	0.535	0.000	0.071	0.000	0.238	0.000	0.000
76	2	580520	>10E6	>10E6	1	0.880	0.843	0.000	0.807	0.000	0.025	0.000	0.093
77	8	20100	>10E6	>10E6	1	0.384	0.193	0.000	0.006	0.000	0.001	0.000	0.000
78	5	>10E6	>10E6	>10E6	1	0.311	0.581	0.000	0.587	0.000	0.098	0.000	0.000
79	6	1573847	>10E6	>10E6	1	0.480	0.274	0.000	0.065	0.000	0.290	0.000	0.000
80	14	191963	>10E6	>10E6	1	0.108	0.210	0.000	0.192	0.000	0.405	0.000	0.000
81	26	>10E6	>10E6	>10E6	1	0.049	0.176	0.000	0.127	0.000	0.029	0.000	0.000
82	10	>10E6	>10E6	>10E6	1	0.115	0.942	0.000	0.169	0.000	0.796	0.000	0.000
83	5	148083	>10E6	>10E6	1	0.637	0.314	0.000	0.303	0.000	0.052	0.000	0.000
84	3	>10E6	>10E6	>10E6	1	0.920	0.604	0.000	0.499	0.000	0.691	0.000	0.000
85	9	>10E6	>10E6	>10E6	1	0.136	0.578	0.000	0.014	0.000	0.149	0.000	0.000
86	4	27469	>10E6	>10E6	1	0.929	0.368	0.000	0.280	0.000	0.195	0.000	0.000
87	90	>10E6	>10E6	>10E6	1	0.011	0.849	0.000	0.503	0.000	0.307	0.000	0.000
88	5	>10E6	>10E6	>10E6	1	0.877	0.263	0.000	0.706	0.000	0.324	0.000	0.367
89	14	26655	>10E6	>10E6	1	0.252	0.102	0.000	0.073	0.000	0.000	0.000	0.000
90	3	>10E6	>10E6	>10E6	1	0.629	0.714	0.000	0.610	0.000	0.084	0.000	0.000
91	6	>10E6	>10E6	>10E6	1	0.428	0.252	0.000	0.649	0.000	0.321	0.000	0.000
92	25	420	>10E6	>10E6	1	0.054	0.149	0.002	0.884	0.000	0.161	0.000	0.000
93	14	1893	>10E6	>10E6	1	0.121	0.191	0.001	0.068	0.000	0.037	0.000	0.000
94	16	1762	>10E6	>10E6	1	0.088	0.199	0.001	0.575	0.000	0.660	0.000	0.000
95	8	>10E6	>10E6	>10E6	1	0.809	0.156	0.000	0.092	0.000	0.888	0.000	0.000
96	5	>10E6	>10E6	>10E6	1	0.424	0.354	0.000	0.039	0.000	0.172	0.000	0.000
97	3	20505	>10E6	>10E6	1	0.585	0.770	0.000	0.538	0.000	0.007	0.000	0.000
98	54	1656660	>10E6	>10E6	1	0.107	0.022	0.000	0.016	0.000	0.039	0.000	0.000
99	17	24691	>10E6	>10E6	1	0.065	0.767	0.000	0.093	0.000	0.686	0.000	0.000
100	6	4527537	>10E6	>10E6	1	0.585	0.245	0.000	0.003	0.000	0.002	0.000	0.000

Table 46: Three Bus System Analog Security Assessment Results for Line Three Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.534	2.165	0.000	0.000
2	0.986	21.280	1.664	0.089	0.000	0.000
3	0.815	-16.903	0.000	0.000	2.050	0.761

Table 47: Three Bus System Numerical Integration Results for Line Three Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.510	2.017	0.000	0.000
2	1.000	20.833	1.630	0.134	0.000	0.000
3	0.820	-16.349	0.000	0.000	2.000	0.750

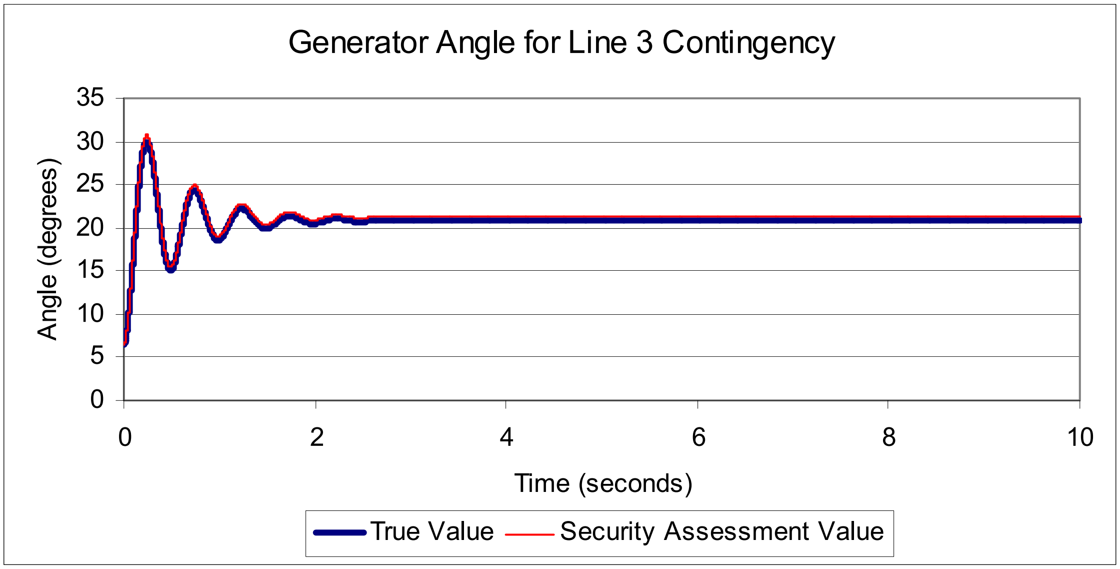

Figure 69: Three Bus System Generator Two Angle for Line Three Contingency

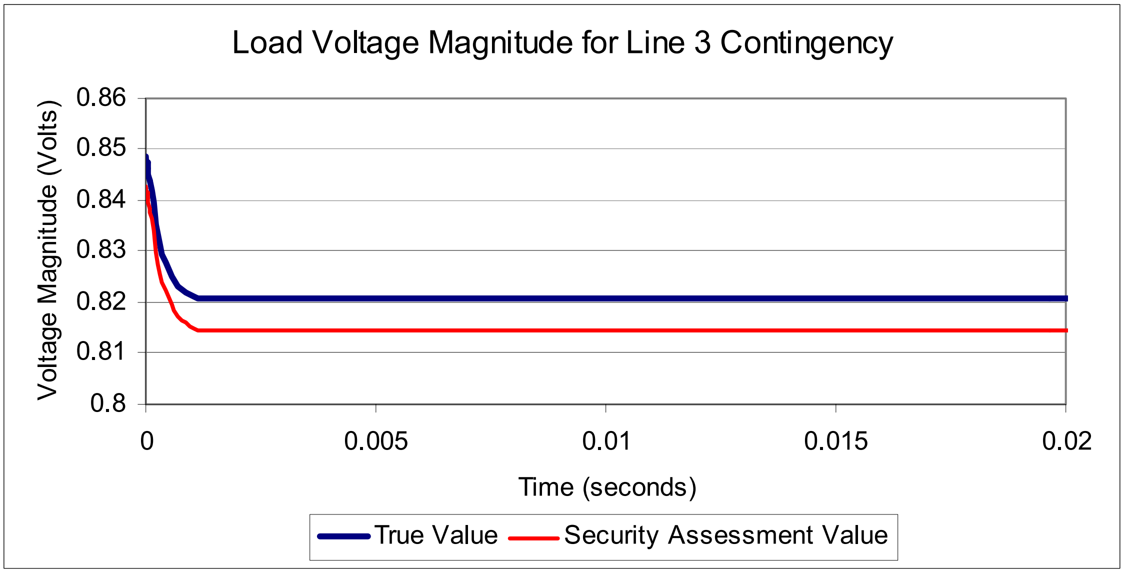

Figure 70: Three Bus System Load Voltage Magnitude for Line Three Contingency

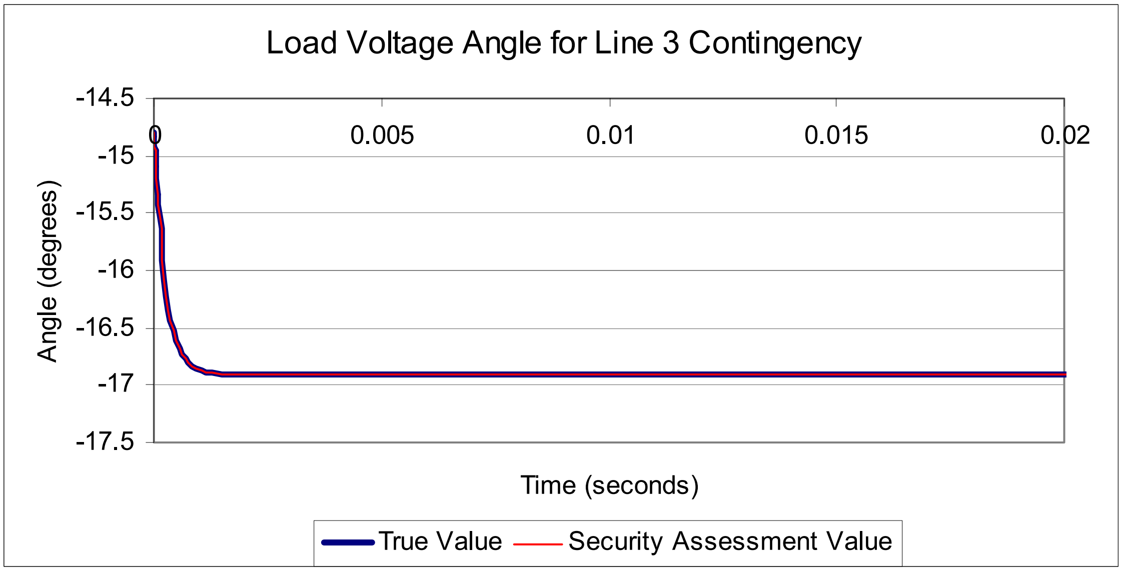

Figure 71: Three Bus System Load Voltage Angle for Line Three Contingency

Table 48: Topology Identification Results for Nine Bus System

	Performance Indices							Correct		Performance Indices							Correct
Case	PI top 1	PI top 2	PI top 3	PI top 4	PI top 5	PI top 6	PI top 4	Topology	Case	PI top 1	PI top 2	PI top 3	PI top 4	PI top 5	PI top 6	PI top 4	Topology
1	12	89	>10E6	616179	26	>10E6	>10E6	1	51	9	2907	>10E6	280475	2399	>10E6	9316	1
2	10	1409	>10E6	705547	2184	>10E6	>10E6	1	52	10	747	>10E6	659251	1660	>10E6	>10E6	1
3	17	>10E6	>10E6	>10E6	30	>10E6	>10E6	1	53	11	>10E6	>10E6	>10E6	3021	>10E6	>10E6	1
4	10	>10E6	>10E6	2425209	3496	>10E6	>10E6	1	54	9	796	>10E6	954064	631	>10E6	>10E6	1
5	10	>10E6	>10E6	4952810	764	>10E6	>10E6	1	55	11	63	>10E6	203661	32	>10E6	>10E6	1
6	14	22203	>10E6	35553	22	708	1492	1	56	9	2222	>10E6	1981973	949	>10E6	>10E6	1
7	12	>10E6	>10E6	3494347	27	>10E6	>10E6	1	57	9	67	>10E6	287568	27	>10E6	21247	1
8	10	2079	>10E6	1828127	31	>10E6	>10E6	1	58	9	992	>10E6	910319	32	>10E6	12607	1
9	22	>10E6	>10E6	3746727	18	>10E6	2828	5	59	11	>10E6	>10E6	4378937	480	>10E6	>10E6	1
10	9	1092	>10E6	518603	28	>10E6	1156382	1	60	15	>10E6	>10E6	8569675	26	>10E6	>10E6	1
11	9	1734	>10E6	6766438	5260	>10E6	>10E6	1	61	8	3531	>10E6	2854258	28	>10E6	>10E6	1
12	8	1045	>10E6	1321280	1430	>10E6	>10E6	1	62	10	52	>10E6	118226	808	2036	1859	1
13	10	2030	>10E6	542459	27	>10E6	4032	1	63	12	80	>10E6	547446	27	>10E6	30	1
14	12	>10E6	>10E6	7818012	1227	>10E6	>10E6	1	64	10	1786	>10E6	2210188	24	>10E6	>10E6	1
15	13	>10E6	>10E6	4783400	27	>10E6	199950	1	65	10	2126	>10E6	1505725	1498778	>10E6	>10E6	1
16	8	1027	>10E6	905505	837568	>10E6	>10E6	1	66	12	>10E6	>10E6	9669259	29	>10E6	>10E6	1
17	8	965	>10E6	610362	1524	>10E6	>10E6	1	67	10	>10E6	>10E6	1721377	2926	>10E6	>10E6	1
18	16	>10E6	>10E6	2012071	20	>10E6	>10E6	1	68	9	>10E6	>10E6	4669550	30	>10E6	>10E6	1
19	10	>10E6	>10E6	2308670	4949	>10E6	>10E6	1	69	14	>10E6	>10E6	1853773	25483	>10E6	>10E6	1
20	13	103	>10E6	819309	24	>10E6	276648	1	70	10	1651	>10E6	1071711	21	>10E6	>10E6	1
21	11	>10E6	>10E6	9467234	27	>10E6	>10E6	1	71	9	84	>10E6	509437	26	>10E6	>10E6	1
22	9	82	>10E6	571878	467	>10E6	>10E6	1	72	9	>10E6	>10E6	3225767	32	>10E6	49796	1
23	13	>10E6	>10E6	>10E6	23	>10E6	>10E6	1	73	11	>10E6	>10E6	3460591	714	>10E6	344403	1
24	9	>10E6	>10E6	1288403	27	>10E6	2216593	1	74	14	>10E6	>10E6	5169755	20	>10E6	1185920	1
25	9	>10E6	>10E6	445491	1503	>10E6	8600846	1	75	11	51	>10E6	46978	806	1662	>10E6	1
26	9	1487	>10E6	516449	29	>10E6	9693	1	76	10	79	>10E6	483137	25	>10E6	>10E6	1
27	11	2195	>10E6	6212023	28	>10E6	2315	1	77	10	>10E6	>10E6	1081918	2865	>10E6	4950	1
28	12	110	>10E6	1282118	22	>10E6	>10E6	1	78	10	464	>10E6	2621122	21	>10E6	>10E6	1
29	9	3282	>10E6	883380	26	>10E6	>10E6	1	79	11	>10E6	>10E6	6162791	818	>10E6	37229	1
30	12	>10E6	>10E6	>10E6	>10E6	>10E6	>10E6	1	80	14	>10E6	>10E6	9297992	>10E6	>10E6	>10E6	1
31	11	>10E6	>10E6	5148317	32	>10E6	>10E6	1	81	11	828	>10E6	1917212	28	>10E6	>10E6	1
32	12	>10E6	>10E6	1634864	25	>10E6	319706	1	82	8	1628	>10E6	938815	6623	>10E6	>10E6	1
33	10	51	>10E6	108925	25	57219	123419	1	83	10	338	>10E6	977279	4542	>10E6	>10E6	1
34	9	1456	>10E6	635742	8663	>10E6	>10E6	1	84	8	2887	>10E6	1679970	30	>10E6	>10E6	1
35	8	913	>10E6	1421853	7554	>10E6	>10E6	1	85	10	74	>10E6	401054	31	>10E6	10531	1
36	12	3259	>10E6	2480189	1060	>10E6	>10E6	1	86	9	422	>10E6	469746	2433	>10E6	>10E6	1
37	10	>10E6	>10E6	7435301	1212	>10E6	>10E6	1	87	9	123	>10E6	1841973	26	>10E6	>10E6	1
38	10	>10E6	>10E6	7589346	832	>10E6	1695527	1	88	11	>10E6	>10E6	4744928	2015	>10E6	977664	1
39	15	>10E6	>10E6	>10E6	29	>10E6	98	1	89	8	5157	>10E6	1819690	39	>10E6	>10E6	1
40	10	>10E6	>10E6	2777548	27	>10E6	>10E6	1	90	14	67541	>10E6	130833	18	>10E6	>10E6	1
41	12	7688	>10E6	619904	61	>10E6	1653214	1	91	10	66	>10E6	218948	30	>10E6	116203	1
42	9	907	>10E6	503406	29	>10E6	98094	1	92	12	85	>10E6	482367	25	>10E6	>10E6	1
43	9	512	>10E6	2356047	26	>10E6	>10E6	1	93	9	76	>10E6	422549	1647	>10E6	>10E6	1
44	8	1138	>10E6	1052621	27	>10E6	766550	1	94	12	>10E6	>10E6	6558207	2525	>10E6	4725	1
45	9	100	>10E6	1050576	1668	>10E6	1146537	1	95	9	>10E6	>10E6	4563738	3607	>10E6	>10E6	1
46	10	2994	>10E6	591821	19	>10E6	>10E6	1	96	12	97	>10E6	770000	20	>10E6	>10E6	1
47	8	342	>10E6	385095	1462	>10E6	>10E6	1	97	9	325	>10E6	563027	28	>10E6	>10E6	1
48	13	>10E6	>10E6	7883307	22	>10E6	>10E6	1	98	14	>10E6	>10E6	>10E6	>10E6	>10E6	1401233	1
49	14	>10E6	>10E6	>10E6	27	>10E6	>10E6	1	99	8	59	>10E6	167107	2580	>10E6	>10E6	1
50	8	1080	>10E6	554957	773	>10E6	114121	1	100	8	>10E6	>10E6	1783161	3523	>10E6	>10E6	1

Table 49: Topology Identification Results for Nine Bus System with Input and Output Noise

Case	Performance Indices							Correct		Case	Performance Indices							Correct
	PI top 1	PI top 2	PI top 3	PI top 4	PI top 5	PI top 6	PI top 4	Topology			PI top 1	PI top 2	PI top 3	PI top 4	PI top 5	PI top 6	PI top 4	Topology
1	13	616016	>10E6	615941	35	228241	>10E6	1		51	11	2582	>10E6	280085	2217	>10E6	10373	1
2	12	1206	>10E6	685080	1385	>10E6	>10E6	1		52	10	814	>10E6	659212	1653	>10E6	>10E6	1
3	16	>10E6	>10E6	>10E6	30	>10E6	>10E6	1		53	11	3823	>10E6	>10E6	>10E6	>10E6	>10E6	1
4	12	>10E6	>10E6	2425206	3244	>10E6	>10E6	1		54	10	>10E6	>10E6	953641	411	>10E6	>10E6	1
5	10	1171	>10E6	4952857	198	>10E6	>10E6	1		55	14	66	>10E6	203678	31	>10E6	>10E6	1
6	17	53	>10E6	35557	21	>10E6	>10E6	1		56	12	2226	>10E6	1981936	1062	>10E6	>10E6	1
7	14	>10E6	>10E6	3494313	43	>10E6	>10E6	1		57	10	1438	>10E6	287575	30	>10E6	2621911	1
8	11	1825089	>10E6	1724913	31	>10E6	>10E6	1		58	10	995	>10E6	910289	38	>10E6	24368	1
9	19	>10E6	>10E6	>10E6	23	>10E6	5389794	1		59	11	>10E6	>10E6	4379283	708	>10E6	36362	1
10	11	1093	>10E6	518643	29	>10E6	57793	1		60	19	>10E6	>10E6	8569672	712	>10E6	>10E6	1
11	10	>10E6	>10E6	6766455	3180	>10E6	>10E6	1		61	10	3531	>10E6	2854270	550	>10E6	>10E6	1
12	10	975320	>10E6	1321183	1449	>10E6	357685	1		62	13	87609	>10E6	118230	1067	>10E6	910848	1
13	12	>10E6	>10E6	542090	45	>10E6	>10E6	1		63	17	525821	>10E6	545846	2073	>10E6	192	1
14	14	>10E6	>10E6	7817992	1060	>10E6	>10E6	1		64	11	2322	>10E6	2210189	24	>10E6	>10E6	1
15	14	>10E6	>10E6	4783402	30	>10E6	34148	1		65	12	2124	>10E6	1506610	1501604	>10E6	6185	1
16	11	>10E6	>10E6	905369	455	>10E6	>10E6	1		66	14	>10E6	>10E6	9669271	30	>10E6	>10E6	1
17	9	1165	>10E6	610269	712	>10E6	>10E6	1		67	12	687	>10E6	1720255	>10E6	>10E6	>10E6	1
18	14	>10E6	>10E6	2011896	20	>10E6	>10E6	1		68	13	>10E6	>10E6	4669588	32	>10E6	>10E6	1
19	12	707	>10E6	2307966	6497	>10E6	>10E6	1		69	14	>10E6	>10E6	1853769	25411	>10E6	>10E6	1
20	39	9098	>10E6	819331	24	>10E6	9417	5		70	12	101	>10E6	1071700	27	>10E6	>10E6	1
21	13	>10E6	>10E6	9467217	127	>10E6	>10E6	1		71	11	108	>10E6	509070	132	>10E6	>10E6	1
22	10	85	>10E6	571616	655	>10E6	>10E6	1		72	11	3102076	>10E6	3225718	31	>10E6	26886	1
23	16	>10E6	>10E6	>10E6	40	>10E6	>10E6	1		73	12	>10E6	>10E6	3460527	141	>10E6	2513747	1
24	11	>10E6	>10E6	1288408	31	>10E6	>10E6	1		74	16	>10E6	>10E6	5169835	27	>10E6	9010115	1
25	11	444751	>10E6	445764	1302	>10E6	89609	1		75	12	28937	>10E6	46908	589	1611	2201717	1
26	11	1516	>10E6	516466	7990	>10E6	1150	1		76	11	75	>10E6	483106	159	>10E6	>10E6	1
27	14	2211	>10E6	6202785	26	>10E6	1155	1		77	12	>10E6	>10E6	1081546	3046	>10E6	9657	1
28	12	1054310	>10E6	1282174	21	>10E6	>10E6	1		78	12	318	>10E6	2703616	33	>10E6	>10E6	1
29	10	3279	>10E6	883399	651	>10E6	>10E6	1		79	12	>10E6	>10E6	6162613	223	>10E6	3237327	1
30	14	>10E6	>10E6	>10E6	>10E6	>10E6	>10E6	1		80	17	>10E6	>10E6	9298027	>10E6	>10E6	>10E6	1
31	14	>10E6	>10E6	5148297	55	>10E6	>10E6	1		81	11	1857617	>10E6	1917238	27	>10E6	>10E6	1
32	16	>10E6	>10E6	1634877	29	>10E6	9577912	1		82	10	1638	>10E6	938764	32	>10E6	>10E6	1
33	12	82515	>10E6	108952	140	57209	520678	1		83	11	341	>10E6	977252	4588	>10E6	>10E6	1
34	10	1455	>10E6	635469	8521	>10E6	>10E6	1		84	10	1681802	>10E6	1679654	28	>10E6	>10E6	1
35	10	>10E6	>10E6	1421754	1024	>10E6	>10E6	1		85	11	398317	>10E6	>10E6	38	>10E6	>10E6	1
36	13	3254	>10E6	2479522	>10E6	>10E6	>10E6	1		86	11	446431	>10E6	469745	4074	>10E6	>10E6	1
37	11	1194	>10E6	7416594	1223	>10E6	>10E6	1		87	10	1103	>10E6	1842006	27	>10E6	779555	1
38	18	>10E6	>10E6	7589414	27	>10E6	>10E6	1		88	11	>10E6	>10E6	4744935	1910	>10E6	>10E6	1
39	18	>10E6	>10E6	>10E6	4205	>10E6	8529744	1		89	10	2964	>10E6	1819666	4497	>10E6	>10E6	1
40	11	669	>10E6	2777544	25	>10E6	>10E6	1		90	18	100148	>10E6	>10E6	31	>10E6	329863	1
41	12	579669	>10E6	619015	28	>10E6	>10E6	1		91	11	4384	>10E6	218678	30	>10E6	>10E6	1
42	10	910	>10E6	503393	978	>10E6	475742	1		92	11	94	>10E6	482390	25	>10E6	>10E6	1
43	12	1165	>10E6	2354672	29	>10E6	>10E6	1		93	10	419836	>10E6	>10E6	1128	>10E6	>10E6	1
44	12	98	>10E6	1052466	1382	>10E6	>10E6	1		94	13	>10E6	>10E6	6555807	2520	>10E6	>10E6	1
45	12	103	>10E6	>10E6	1514	>10E6	2215734	1		95	11	>10E6	>10E6	4563741	1884	>10E6	>10E6	1
46	13	3108	>10E6	>10E6	29	>10E6	>10E6	1		96	14	763325	>10E6	770000	24	>10E6	>10E6	1
47	11	81	>10E6	385089	1263	>10E6	>10E6	1		97	13	8462369	>10E6	562837	43	>10E6	>10E6	1
48	17	>10E6	>10E6	6266407	21	>10E6	>10E6	1		98	14	>10E6	>10E6	>10E6	1289	>10E6	1189	1
49	29	>10E6	>10E6	>10E6	29	>10E6	>10E6	1		99	11	168424	>10E6	167083	3203	>10E6	>10E6	1
50	10	424310	>10E6	554999	1029	>10E6	405496	1		100	11	>10E6	>10E6	1782998	1459	>10E6	>10E6	1

Table 50: Topology Identification Results for Nine Bus System with Output Noise

	Performance Indices							Correct
Case	PI top 1	PI top 2	PI top 3	PI top 4	PI top 5	PI top 6	PI top 7	Topology
1	21	29929	>10E6	333257	133	>10E6	>10E6	1
2	31	>10E6	>10E6	139	104	>10E6	72116	1
3	22	>10E6	>10E6	67	406	>10E6	>10E6	1
4	29	>10E6	4065310	>10E6	63205	>10E6	44	1
5	21	6217251	>10E6	8611	61	>10E6	132103	1
6	55	>10E6	>10E6	>10E6	2652	1254	>10E6	1
7	27	2816	>10E6	>10E6	1218	>10E6	>10E6	1
8	11	>10E6	>10E6	330	23	>10E6	88312	1
9	26	>10E6	>10E6	38496	>10E6	>10E6	>10E6	1
10	69	>10E6	>10E6	402304	>10E6	>10E6	>10E6	1
11	18	>10E6	466889	>10E6	133	>10E6	>10E6	1
12	32	>10E6	>10E6	>10E6	152	>10E6	594	1
13	22	>10E6	>10E6	>10E6	37	>10E6	248	1
14	235501	>10E6	86	>10E6	>10E6	>10E6	654	3
15	21	>10E6	>10E6	>10E6	8183	>10E6	387521	1
16	15	>10E6	>10E6	2318757	31	>10E6	28863	1
17	40	>10E6	>10E6	>10E6	>10E6	>10E6	>10E6	1
18	266	>10E6	>10E6	110455	>10E6	13116	>10E6	1
19	44	>10E6	>10E6	62435	>10E6	200	>10E6	1
20	31	>10E6	>10E6	72422	>10E6	2742	>10E6	1
21	53	>10E6	>10E6	9822583	>10E6	>10E6	51521	1
22	34	418	>10E6	2507	1244	>10E6	>10E6	1
23	46	7755	>10E6	>10E6	>10E6	746594	>10E6	1
24	20	244764	>10E6	12552	151	>10E6	1542196	1
25	79	28	>10E6	>10E6	>10E6	>10E6	53914	2
26	2256	>10E6	>10E6	7443110	86	>10E6	905338	5
27	57	>10E6	>10E6	>10E6	192807	>10E6	>10E6	1
28	36	155399	>10E6	>10E6	97	>10E6	137046	1
29	24	>10E6	>10E6	>10E6	>10E6	>10E6	>10E6	1
30	25	>10E6	>10E6	>10E6	29	>10E6	34956	1
31	94	>10E6	50	>10E6	1940	>10E6	32946	3
32	25	>10E6	>10E6	453	65	>10E6	>10E6	1
33	27	114	>10E6	>10E6	>10E6	162089	>10E6	1
34	21	>10E6	>10E6	63	45	>10E6	>10E6	1
35	22	501	>10E6	5311145	16	>10E6	131060	5
36	35	>10E6	>10E6	>10E6	162	>10E6	6373	1
37	37	>10E6	740	>10E6	9991	>10E6	11796	1
38	43	>10E6	>10E6	>10E6	21584	>10E6	1546	1
39	47	33	>10E6	>10E6	3620	>10E6	1281086	2
40	24	>10E6	>10E6	364	116	>10E6	12510	1
41	33	>10E6	395826	>10E6	48	>10E6	264	1
42	16	>10E6	>10E6	5614	2664	>10E6	>10E6	1
43	171	>10E6	>10E6	>10E6	>10E6	>10E6	>10E6	1
44	23	>10E6	>10E6	1707	49	1630746	>10E6	1
45	71545	>10E6	>10E6	>10E6	>10E6	>10E6	8315	7
46	94041813	3686	>10E6	53	>10E6	505	>10E6	4
47	12	>10E6	>10E6	162	1146	>10E6	7461	1
48	16	>10E6	2598	>10E6	62	>10E6	>10E6	1
49	17	4379	>10E6	6235	20	>10E6	387	1
50	53	>10E6	>10E6	63848	202	>10E6	334849	1
51	17	>10E6	>10E6	21	501	>10E6	>10E6	1
52	15	>10E6	>10E6	6205	30	>10E6	119596	1
53	25	350	>10E6	>10E6	1649	>10E6	45216	1
54	30	>10E6	>10E6	1865782	41	>10E6	>10E6	1
55	21	627940	>10E6	17130	1603	>10E6	>10E6	1
56	56	203	>10E6	3427	>10E6	462	>10E6	1
57	75	>10E6	48	>10E6	>10E6	>10E6	322	3
58	56	183	>10E6	>10E6	>10E6	>10E6	>10E6	1
59	28	415	>10E6	4687770	13885	>10E6	>10E6	1
60	56	443	>10E6	5032	>10E6	>10E6	>10E6	1
61	30	212	>10E6	2577811	>10E6	4694	>10E6	1
62	55	>10E6	>10E6	>10E6	1296757	>10E6	1084	1
63	22	>10E6	>10E6	7062973	331	1750	>10E6	1
64	69	>10E6	>10E6	>10E6	630	>10E6	>10E6	1
65	26	>10E6	>10E6	>10E6	>10E6	>10E6	>10E6	1
66	28	>10E6	>10E6	207	24	>10E6	5679	5
67	21	674871	>10E6	48515	477	>10E6	2560	1
68	29	2108	>10E6	387	>10E6	878	>10E6	1
69	20	>10E6	>10E6	1417	1198	>10E6	>10E6	1
70	23	>10E6	>10E6	41	25	459	>10E6	1
71	19	492	>10E6	>10E6	7853	>10E6	258343	1
72	21451	>10E6	>10E6	>10E6	34712	311	>10E6	6
73	22	>10E6	>10E6	>10E6	735	>10E6	208058	1
74	15	>10E6	>10E6	>10E6	30	>10E6	75018	1
75	31	55	>10E6	>10E6	>10E6	>10E6	>10E6	1
76	26	28	>10E6	>10E6	>10E6	>10E6	>10E6	1
77	42	2983	>10E6	18184	>10E6	>10E6	905571	1
78	29	173	>10E6	>10E6	124	>10E6	>10E6	1
79	66	>10E6	>10E6	25	21	>10E6	>10E6	5
80	24	>10E6	3952	>10E6	>10E6	>10E6	53549	1
81	548	54	>10E6	>10E6	70	>10E6	85700	2
82	24993	>10E6	1239	>10E6	>10E6	>10E6	91	7
83	19	>10E6	>10E6	580371	2680	>10E6	329	1
84	25	1141	>10E6	74	>10E6	33793	>10E6	1
85	17	>10E6	>10E6	5270	17	>10E6	>10E6	5
86	320	>10E6	28	>10E6	44	>10E6	11561	3
87	36	>10E6	>10E6	>10E6	20845	>10E6	216	1
88	24	51	>10E6	>10E6	37899	>10E6	>10E6	1
89	20	>10E6	>10E6	>10E6	3081	>10E6	>10E6	1
90	28	93	>10E6	>10E6	4638	>10E6	324431	1
91	19	>10E6	>10E6	788	80927	>10E6	6712	1
92	23	4171321	>10E6	>10E6	859	>10E6	2366105	1
93	51	>10E6	>10E6	3634	>10E6	203	>10E6	1
94	28	>10E6	>10E6	3320164	>10E6	2949	>10E6	1
95	35	>10E6	>10E6	>10E6	>10E6	>10E6	2440590	1
96	32	35	>10E6	>10E6	>10E6	>10E6	>10E6	1
97	81	>10E6	105972	>10E6	>10E6	233	>10E6	1
98	36	>10E6	68	>10E6	>10E6	>10E6	>10E6	1
99	40	>10E6	>10E6	98	>10E6	>10E6	>10E6	1
100	36	>10E6	>10E6	2639	47	136	>10E6	1

Table 51: Input Identification Steps for Nine Bus System

Step	**Inputs**											
	V1	**θ1**	**V2**	**P2**	**V3**	**P3**	**P5**	**Q5**	**V7**	**P7**	**P9**	**Q9**
1	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2841	0.9801	0.9960	1.2629	0.5067
2	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2843	0.9803	0.9958	1.2627	0.5069
3	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2845	0.9805	0.9956	1.2625	0.5071
4	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2847	0.9807	0.9954	1.2623	0.5073
5	**1.0000**	**0.0000**	**1.0013**	**1.6329**	**0.9885**	**0.8571**	**0.9125**	**0.2849**	**0.9809**	**0.9952**	**1.2621**	**0.5075**
6	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2851	0.9811	0.9950	1.2619	0.5077
7	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2853	0.9813	0.9948	1.2617	0.5079
8	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2855	0.9815	0.9946	1.2615	0.5081
9	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2857	0.9817	0.9944	1.2613	0.5083
10	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2859	0.9819	0.9942	1.2611	0.5085
11	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2861	0.9821	0.9940	1.2609	0.5087
12	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2863	0.9823	0.9938	1.2607	0.5089
13	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2865	0.9825	0.9936	1.2605	0.5091
14	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2867	0.9827	0.9934	1.2603	0.5093
15	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2869	0.9829	0.9932	1.2601	0.5095
16	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2871	0.9831	0.9930	1.2599	0.5097
17	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2873	0.9833	0.9928	1.2597	0.5099
18	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2875	0.9835	0.9926	1.2595	0.5101
19	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2877	0.9837	0.9924	1.2593	0.5103
20	1.0000	0.0000	1.0013	1.6329	0.9885	0.8571	0.9125	0.2879	0.9839	0.9922	1.2591	0.5105

Table 52: Input Identification Data and Results for Nine Bus System

Step	**Measurements**						**P(m)**
	V5	**θ5**	**Q7**	**θ7**	**V9**	**θ9**	
1	0.9720	-4.0959	0.3676	0.6894	0.9551	-4.4248	0.9052
2	0.9720	-4.0938	0.3648	0.6919	0.9551	-4.4219	0.9123
3	0.9721	-4.0917	0.3621	0.6944	0.9551	-4.4191	0.9049
4	0.9721	-4.0896	0.3593	0.6969	0.9552	-4.4162	0.9133
5	**0.9721**	**-4.0875**	**0.3566**	**0.6994**	**0.9552**	**-4.4134**	**0.9192**
6	0.9721	-4.0854	0.3538	0.7019	0.9552	-4.4105	0.9092
7	0.9721	-4.0833	0.3511	0.7044	0.9552	-4.4077	0.9014
8	0.9721	-4.0812	0.3483	0.7069	0.9553	-4.4048	0.8959
9	0.9722	-4.0791	0.3455	0.7094	0.9553	-4.4020	0.8923
10	0.9722	-4.0770	0.3428	0.7119	0.9553	-4.3992	0.8653
11	0.9722	-4.0750	0.3400	0.7144	0.9554	-4.3963	0.8585
12	0.9722	-4.0729	0.3373	0.7169	0.9554	-4.3935	0.8539
13	0.9722	-4.0708	0.3345	0.7194	0.9554	-4.3906	0.8511
14	0.9723	-4.0687	0.3317	0.7218	0.9554	-4.3878	0.8487
15	0.9723	-4.0666	0.3290	0.7243	0.9555	-4.3850	0.8467
16	0.9723	-4.0645	0.3262	0.7268	0.9555	-4.3821	0.8449
17	0.9723	-4.0624	0.3234	0.7293	0.9555	-4.3793	0.8433
18	0.9723	-4.0603	0.3207	0.7318	0.9556	-4.3764	0.8311
19	0.9724	-4.0583	0.3179	0.7343	0.9556	-4.3736	0.8286
20	0.9724	-4.0562	0.3151	0.7367	0.9556	-4.3708	0.8263

Table 53: Nine Bus System Analog Security Assessment Results for Line Two Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.751	0.238	0.000	0.000
2	0.996	4.755	1.634	0.228	0.000	0.000
3	0.988	-3.330	0.855	0.201	0.000	0.000
4	0.987	-2.510	0.000	0.000	0.000	0.000
5	0.897	-16.391	0.000	0.000	0.911	0.285
6	0.977	-6.579	0.000	0.000	0.000	0.000
7	0.968	-5.910	0.000	0.000	0.996	0.354
8	0.987	-1.226	0.000	0.000	0.000	0.000
9	0.957	-6.207	0.000	0.000	1.264	0.506

Table 54: Nine Bus System Numerical Integration Results for Line Two Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.736	0.212	0.000	0.000
2	1.000	4.809	1.630	0.201	0.000	0.000
3	1.000	-3.132	0.850	0.223	0.000	0.000
4	0.989	-2.458	0.000	0.000	0.000	0.000
5	0.908	-15.850	0.000	0.000	0.900	0.300
6	0.988	-6.413	0.000	0.000	0.000	0.000
7	0.976	-5.786	0.000	0.000	1.000	0.350
8	0.993	-1.167	0.000	0.000	0.000	0.000
9	0.960	-6.077	0.000	0.000	1.250	0.500

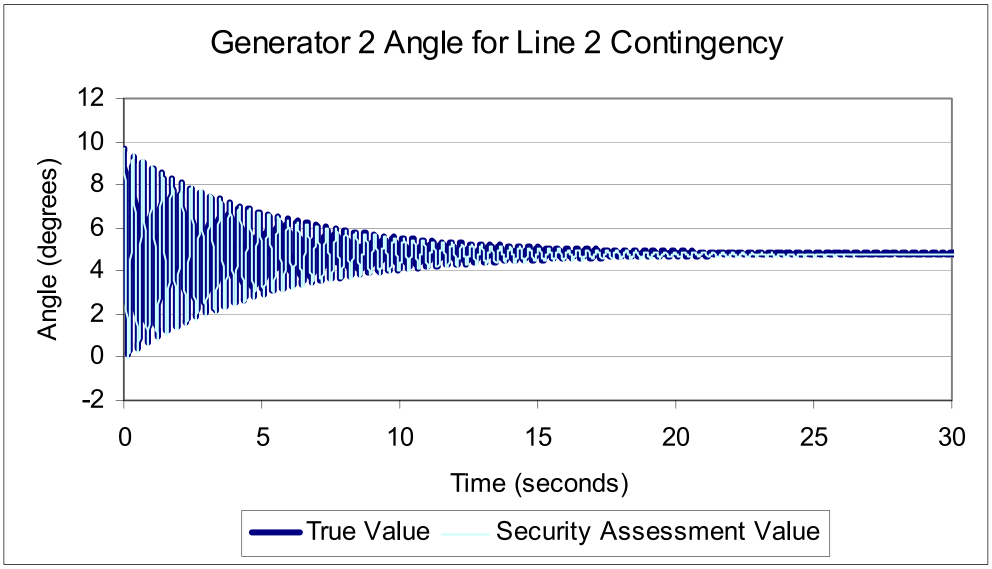

Figure 72: Nine Bus System Generator Two Angle for Line Two Contingency

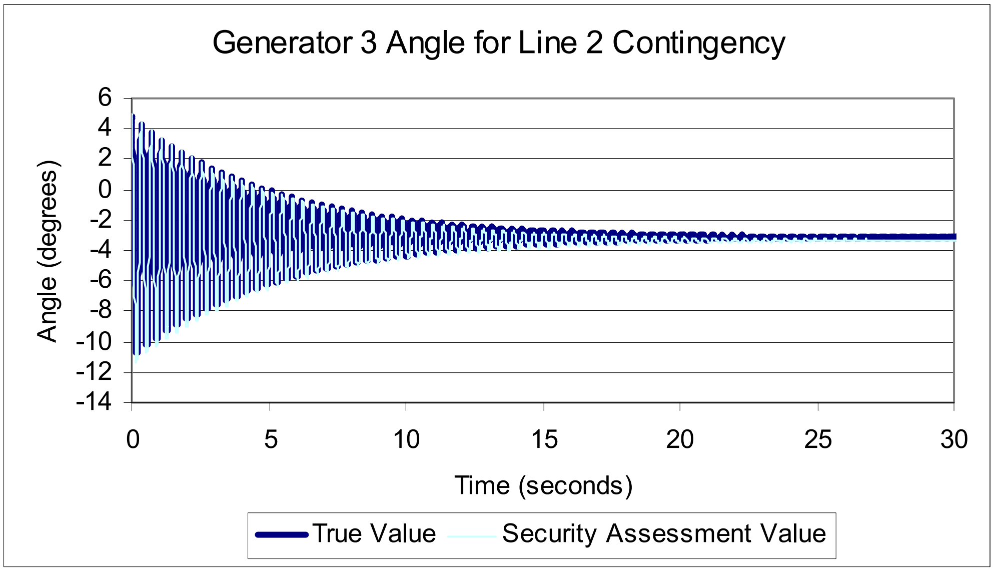

Figure 73: Nine Bus System Generator Three Angle for Line Two Contingency

Table 55: Nine Bus System Analog Security Assessment Results for Line Three Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.787	0.684	0.000	0.000
2	0.996	19.430	1.634	0.347	0.000	0.000
3	0.988	20.663	0.855	0.060	0.000	0.000
4	0.962	-2.702	0.000	0.000	0.000	0.000
5	0.919	-7.902	0.000	0.000	0.911	0.285
6	0.986	17.720	0.000	0.000	0.000	0.000
7	0.967	12.618	0.000	0.000	0.996	0.354
8	0.980	13.196	0.000	0.000	0.000	0.000
9	0.922	-1.626	0.000	0.000	1.264	0.506

Table 56: Nine Bus System Numerical Integration Results for Line Three Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.772	0.664	0.000	0.000
2	1.000	19.122	1.630	0.317	0.000	0.000
3	1.000	21.236	0.850	0.081	0.000	0.000
4	0.963	-2.648	0.000	0.000	0.000	0.000
5	0.919	-7.760	0.000	0.000	0.900	0.300
6	0.997	17.267	0.000	0.000	0.000	0.000
7	0.976	12.311	0.000	0.000	1.000	0.350
8	0.985	12.936	0.000	0.000	0.000	0.000
9	0.926	-1.578	0.000	0.000	1.250	0.500

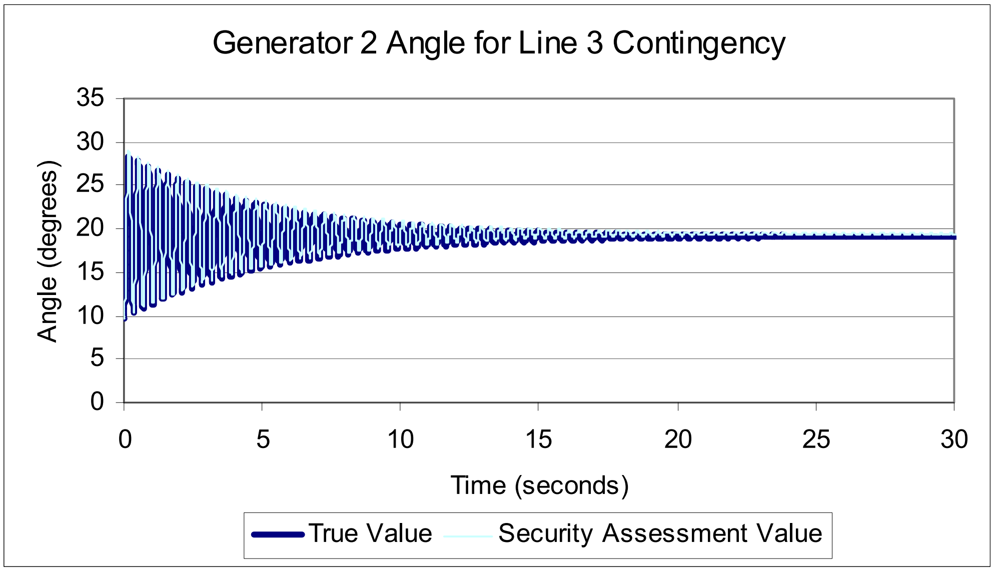

Figure 74: Nine Bus System Generator Two Angle for Line Three Contingency

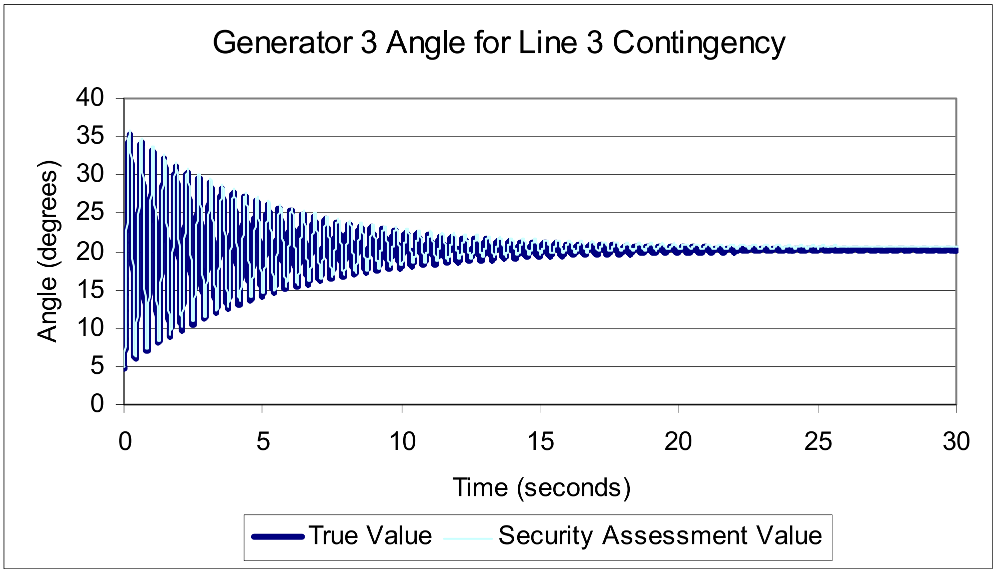

Figure 75: Nine Bus System Generator Three Angle for Line Three Contingency

Table 57: Nine Bus System Analog Security Assessment Results for Line Four Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	1.570	0.268	0.000	0.000
2	0.996	2.049	1.634	0.151	0.000	0.000
3	X	X	X	X	0.000	0.000
4	0.989	-5.271	0.000	0.000	0.000	0.000
5	0.977	-9.828	0.000	0.000	0.911	0.285
6	0.997	-9.168	0.000	0.000	0.000	0.000
7	0.979	-8.517	0.000	0.000	0.996	0.354
8	0.992	-3.905	0.000	0.000	0.000	0.000
9	0.960	-8.914	0.000	0.000	1.264	0.506

Table 58: Nine Bus System Numerical Integration Results for Line Four Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	1.559	0.250	0.000	0.000
2	1.000	2.059	1.630	0.158	0.000	0.000
3	X	X	X	X	0.000	0.000
4	0.990	-5.207	0.000	0.000	0.000	0.000
5	0.977	-9.705	0.000	0.000	0.900	0.300
6	0.999	-9.097	0.000	0.000	0.000	0.000
7	0.982	-8.472	0.000	0.000	1.000	0.350
8	0.995	-3.887	0.000	0.000	0.000	0.000
9	0.962	-8.800	0.000	0.000	1.250	0.500

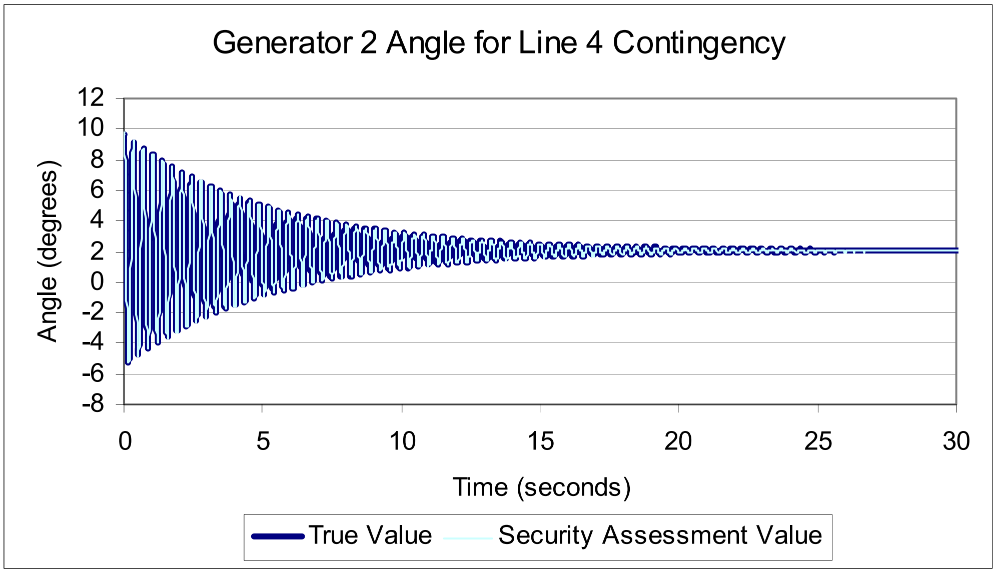

Figure 76: Nine Bus System Generator Two Angle for Line Four Contingency

Table 59: Nine Bus System Analog Security Assessment Results for Line Five Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.741	0.344	0.000	0.000
2	0.996	6.162	1.634	0.415	0.000	0.000
3	0.988	8.911	0.855	-0.099	0.000	0.000
4	0.981	-2.492	0.000	0.000	0.000	0.000
5	0.967	-2.824	0.000	0.000	0.911	0.285
6	0.995	5.786	0.000	0.000	0.000	0.000
7	0.942	-3.925	0.000	0.000	0.996	0.354
8	0.975	0.400	0.000	0.000	0.000	0.000
9	0.948	-5.725	0.000	0.000	1.264	0.506

Table 60: Nine Bus System Numerical Integration Results for Line Five Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.727	0.301	0.000	0.000
2	1.000	6.495	1.630	0.409	0.000	0.000
3	1.000	8.849	0.850	-0.072	0.000	0.000
4	0.984	-2.440	0.000	0.000	0.000	0.000
5	0.972	-2.756	0.000	0.000	0.900	0.300
6	1.005	5.597	0.000	0.000	0.000	0.000
7	0.946	-3.945	0.000	0.000	1.000	0.350
8	0.980	0.359	0.000	0.000	0.000	0.000
9	0.951	-5.626	0.000	0.000	1.250	0.500

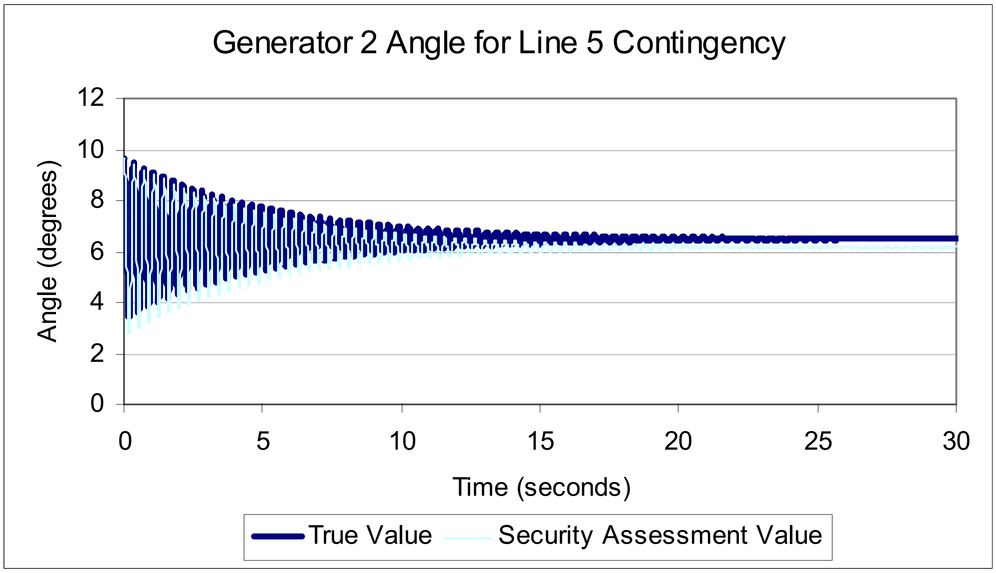

Figure 77: Nine Bus System Generator Two Angle for Line Five Contingency

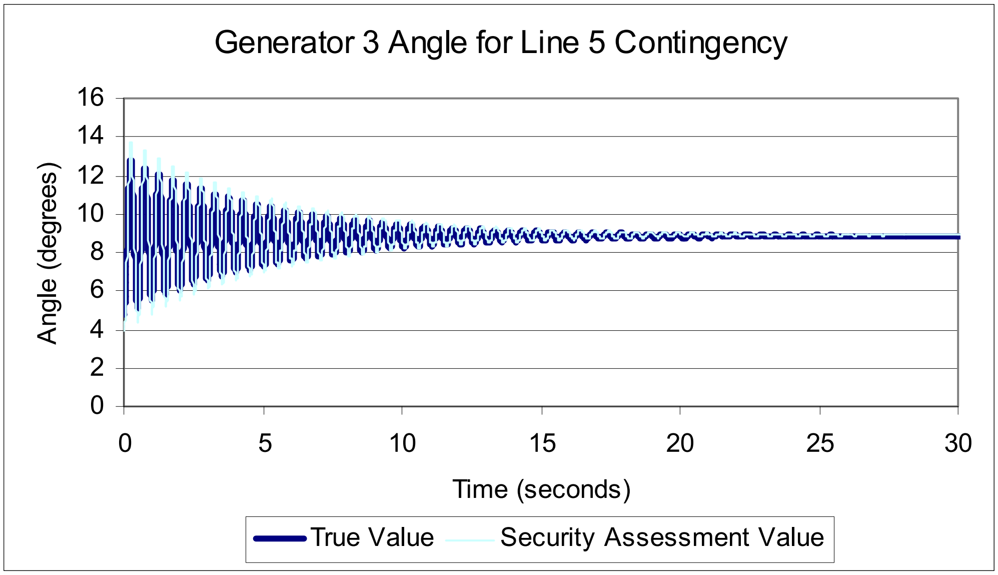

Figure 78: Nine Bus System Generator Three Angle for Line Five Contingency

Table 61: Nine Bus System Analog Security Assessment Results for Line Six Contingency

Bus #	**Voltage**		**Generation**		**Load**	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.814	0.481	0.000	0.000
2	0.996	22.215	1.634	0.265	0.000	0.000
3	0.988	-7.757	0.855	0.301	0.000	0.000
4	0.973	-2.760	0.000	0.000	0.000	0.000
5	0.956	-8.900	0.000	0.000	0.911	0.285
6	0.971	-10.845	0.000	0.000	0.000	0.000
7	0.924	-17.063	0.000	0.000	0.996	0.354
8	0.985	15.276	0.000	0.000	0.000	0.000
9	0.929	-0.929	0.000	0.000	1.264	0.506

Table 62: Nine Bus System Numerical Integration Results for Line Six Contingency (True Values)

Bus #	**Voltage**		**Generation**		**Load**	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.801	0.437	0.000	0.000
2	1.000	22.896	1.630	0.261	0.000	0.000
3	1.000	-7.808	0.850	0.323	0.000	0.000
4	0.976	-2.708	0.000	0.000	0.000	0.000
5	0.961	-8.816	0.000	0.000	0.900	0.300
6	0.982	-10.909	0.000	0.000	0.000	0.000
7	0.936	-17.009	0.000	0.000	1.000	0.350
8	0.989	15.183	0.000	0.000	0.000	0.000
9	0.933	-0.084	0.000	0.000	1.250	0.500

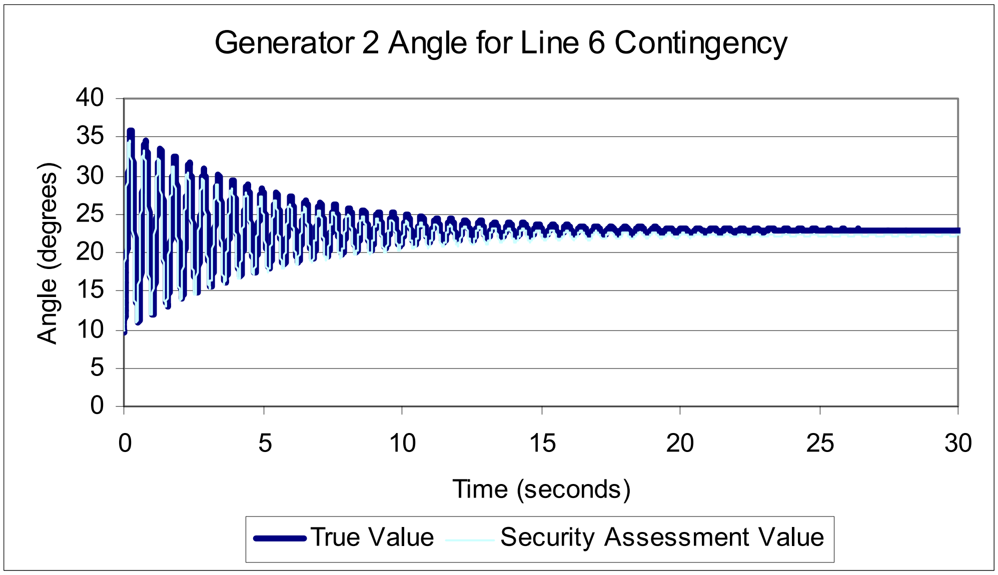

Figure 79: Nine Bus System Generator Two Angle for Line Six Contingency

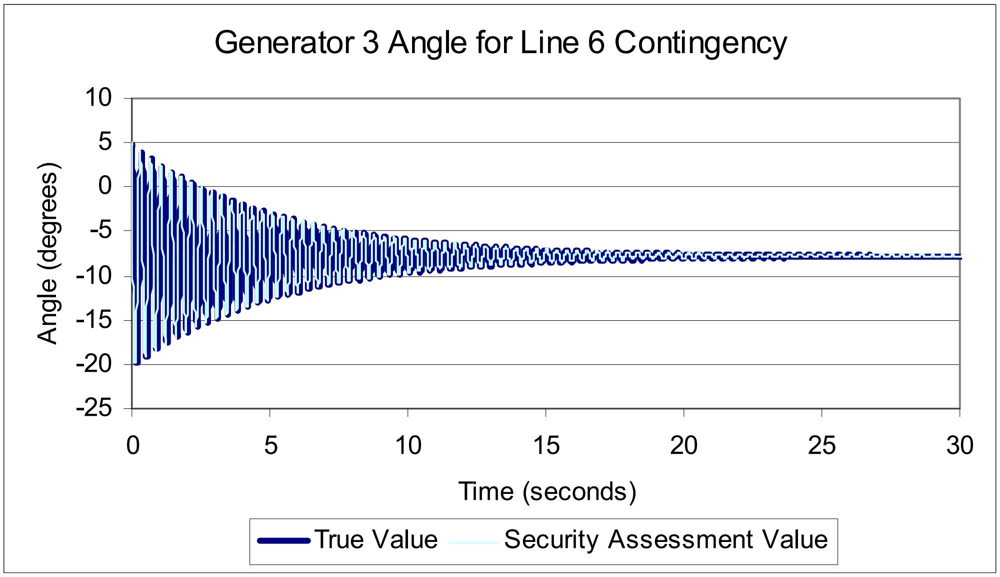

Figure 80: Nine Bus System Generator Three Angle for Line Six Contingency

Table 63: Nine Bus System Analog Security Assessment Results for Line Seven Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	2.366	0.545	0.000	0.000
2	X	X	X	X	0.000	0.000
3	0.988	-10.224	0.855	0.094	0.000	0.000
4	0.978	-8.008	0.000	0.000	0.000	0.000
5	0.964	-13.091	0.000	0.000	0.911	0.285
6	0.984	-13.197	0.000	0.000	0.000	0.000
7	0.955	-18.213	0.000	0.000	0.996	0.354
8	0.961	-17.501	0.000	0.000	0.000	0.000
9	0.941	-15.506	0.000	0.000	1.264	0.506

Table 64: Nine Bus System Numerical Integration Results for Line Seven Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	2.349	0.484	0.000	0.000
2	X	X	X	X	0.000	0.000
3	1.000	-10.180	0.850	0.124	0.000	0.000
4	0.981	-7.925	0.000	0.000	0.000	0.000
5	0.970	-12.947	0.000	0.000	0.900	0.300
6	0.994	-13.172	0.000	0.000	0.000	0.000
7	0.965	-18.079	0.000	0.000	1.000	0.350
8	0.970	-17.356	0.000	0.000	0.000	0.000
9	0.947	-15.313	0.000	0.000	1.250	0.500

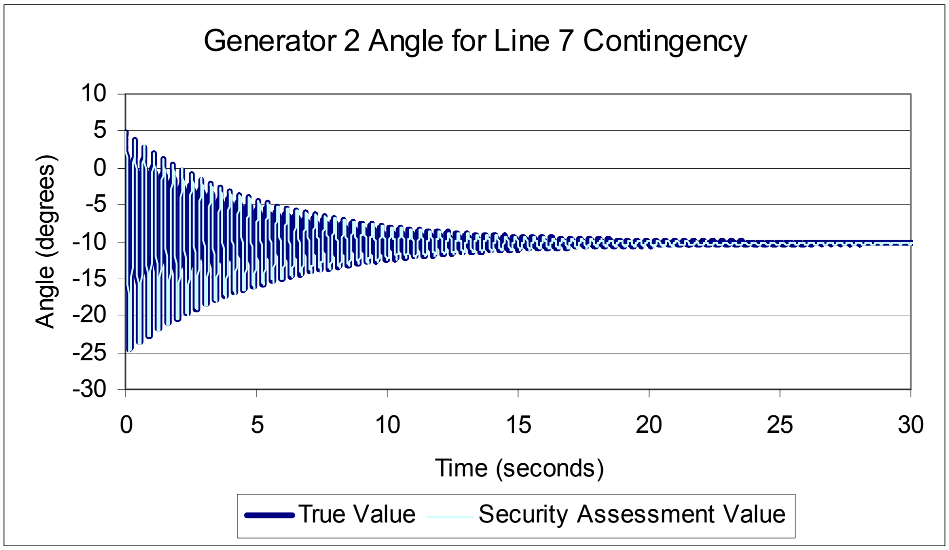

Figure 81: Nine Bus System Generator Two Angle for Line Seven Contingency

Table 65: Nine Bus System Analog Security Assessment Results for Line Eight Contingency

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.828	0.892	0.000	0.000
2	0.996	32.811	1.634	0.287	0.000	0.000
3	0.988	19.029	0.855	0.176	0.000	0.000
4	0.950	-2.878	0.000	0.000	0.000	0.000
5	0.928	0.228	0.000	0.000	0.911	0.285
6	0.979	15.741	0.000	0.000	0.000	0.000
7	0.963	19.655	0.000	0.000	0.996	0.354
8	0.983	26.696	0.000	0.000	0.000	0.000
9	0.887	-9.909	0.000	0.000	1.264	0.506

Table 66: Nine Bus System Numerical Integration Results for Line Eight Contingency (True Values)

Bus #	Voltage		Generation		Load	
	Mag (p.u.)	Ang(deg)	P (p.u.)	Q (p.u.)	P (p.u.)	Q (p.u.)
1	1.000	0.000	0.812	0.845	0.000	0.000
2	1.000	32.138	1.630	0.254	0.000	0.000
3	1.000	18.618	0.850	0.212	0.000	0.000
4	0.952	-2.813	0.000	0.000	0.000	0.000
5	0.933	0.248	0.000	0.000	0.900	0.300
6	0.989	15.313	0.000	0.000	0.000	0.000
7	0.971	19.123	0.000	0.000	1.000	0.350
8	0.989	26.059	0.000	0.000	0.000	0.000
9	0.890	-9.717	0.000	0.000	1.250	0.500

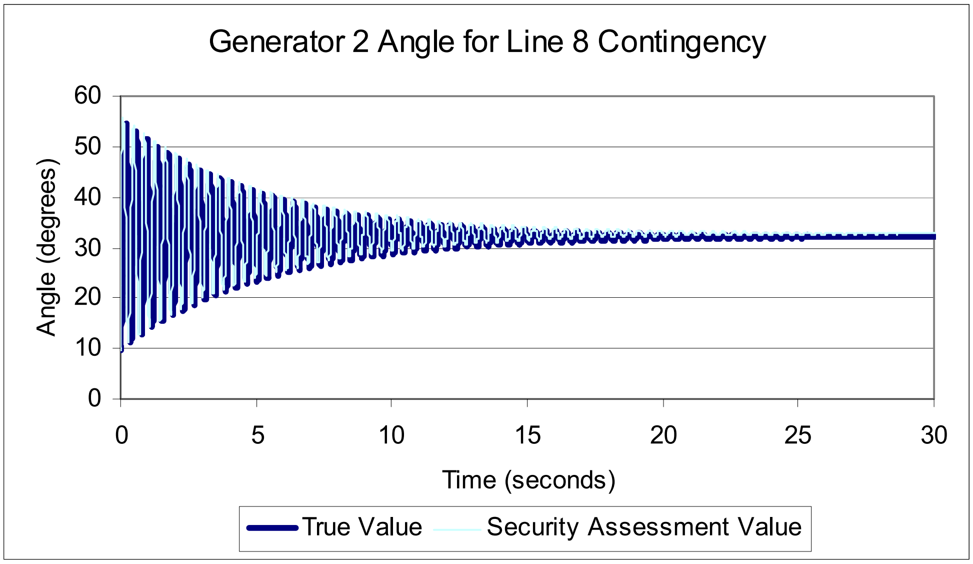

Figure 82: Nine Bus System Generator Two Angle for Line Eight Contingency

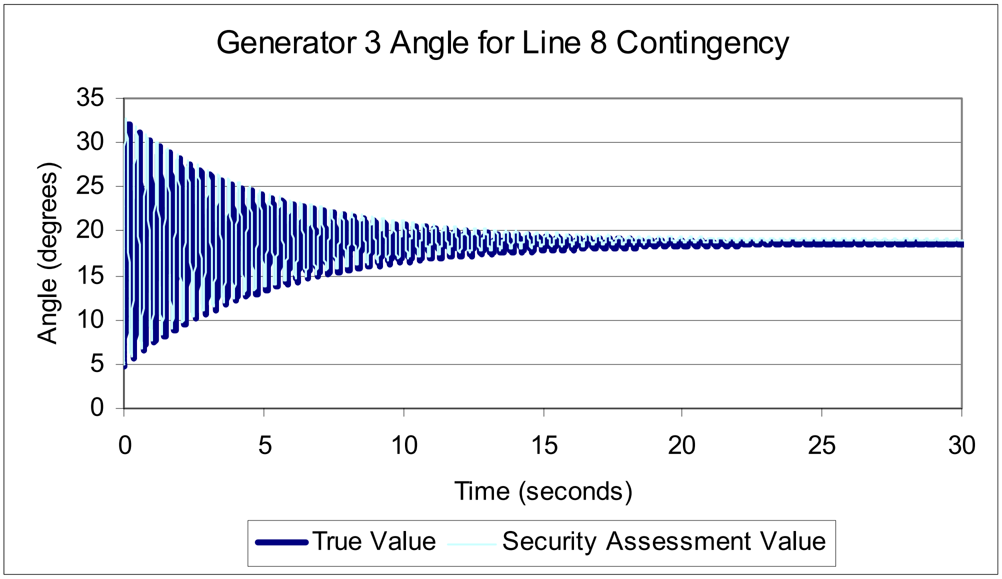

Figure 83: Nine Bus System Generator Three Angle for Line Eight Contingency

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Publications:

- St. Leger and C. Nwankpa, “Configuration of a Large Scale Analog Emulator for Power System Analysis,” *Proceedings of the IEEE PowerTech 2007 Conference,* July 2007, Lausanne Switzerland.
- J.C. Jimenez, A. St. Leger and C. Nwankpa, “Reconfigurable Phase Shifting Transformer for Analog Computation,” *Proceedings of the IEEE PowerTech 2007 Conference,* July 2007, Lausanne Switzerland.
- V.Cecchi, A. St. Leger, K. Miu and C. Nwankpa, “Experimental Setup for Investigating Gamma Transmission Line Models in the Presence of Non-Fundamental Frequencies,” *Proceedings of the IEEE Power Engineering Society General Meeting*, June 2007, Tampa, FL, USA.
- St. Leger, J.C. Jimenez, A. Fu, S. Djimbinov, S.E. Soeurn, S.S. Lwin, and C. Nwankpa, “Analog Emulation of a Reconfigurable Tap Changing Transformer,” Proceedings of the 2007 International Symposium on Circuits and Systems (ISCAS 2007), May 27-30, 2007, New Orleans, USA.
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- Deese, C. Nwankpa, and A. St.Leger, "Effect of System Size on Analog Emulation Based Steady-State Power Flow Analysis," Proceedings of the 49th IEEE International Midwest Symposium on Circuits and Systems, 2006.
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- St. Leger and C. Nwankpa, "Static Generator Model for Analog Power Flow Computation," Proceedings of the 2006 International Symposium on Circuits and Systems (ISCAS 2006), Island of Kos, Greece, May 21-24, 2006.
- Nwankpa, A. Deese, Q. Liu, A. St. Leger and J. Yakaski "Power System on a Chip (PSoC)," Proceedings of the 2006 International Symposium on Circuits and Systems (ISCAS 2006), Island of Kos, Greece, May 21-24, 2006.
- St. Leger and C. Nwankpa, "Reconfigurable Transmission Line Model for Analog Power Flow Computation," Proceedings of the 15th Power Systems Computation Conference, Liege, Belgium, August 22-26, 2005.
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- V. Cecchi, A. St. Leger, K. Miu and C. Nwankpa, “Loading Studies for Power Transmission Line Models in the Presence of Non-Fundamental Frequencies,” *Proceedings of the 2007 Summer Computer Simulation Conference (SCSC ’07)*, July, 2007, San Diego, CA, USA.