Unbalanced Power Converter Modeling for AC/DC Power Distribution Systems

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ABSTRACT

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In power distribution systems, the installation of power electronics based equipment has grown rapidly for ac/dc system coupling, system protection, alternative energy source interface, etc. This thesis will focus on power electronic component and system modeling techniques and three-phase ac/dc power flow analysis for power distribution systems. First, mathematical models are developed for unbalanced power electronic converters, such as thyristor converters, diode rectifiers, and Pulse-Width-Modulated (PWM) converters. The modeling approach captures the imbalance of distribution systems using three, delta-connected, single-phase converters. In order to perform system analysis, these models have been incorporated into two types of ac/dc power flow solvers: (i) a three-phase backward/forward sequential solver and (ii) a three-phase unified solver using the modified nodal analysis method. Both solvers have been applied to unbalanced radial and weakly meshed distribution systems. Finally, an ac/dc system hardware test bed was created to validate the mathematical models and the performance of the power flow solvers. Extensive hardware tests, time domain simulations, and steady-state analysis have been performed.

CHAPTER 1. INTRODUCTION

Recent developments in power electronics offer the possibility of wide-scale integration of power electronics based devices into power systems [1]. Resulting benefits would include improved control of the delivered power, high energy efficiency and high power density. In order to implement these devices into distribution systems successfully, system wide analysis should be performed in order to understand their impacts on system planning and operation. As such, appropriate mathematical models and application tools, are desired to capture the characteristics of power electronic devices. This thesis will address power electronic device modeling techniques and three-phase ac/dc power flow analysis for power distribution systems.

1.1 Motivations

In power systems, *ac/dc* conversion using power converters has been developed and installed in transmission systems in past decades [2]. With a focus on power distribution systems, the implementation of power electronic devices has grown rapidly in recent years, such as in terrestrial distribution systems [3], shipboard power systems [4], and transportation systems [5]. For example, adjustable-speed drives are replacing constant speed electric motor-driven systems in industry to improve efficiency by controlling the motor speed. Power electronics have also been used as interface to transfer power from alternative energy sources, such as wind, photovoltaic, into the utility systems. In shipboard power systems, power converters introduce the potential to actively control the coupling of ac/dc systems. They can be operated faster than electromechanical devices to open/close circuits and prevent the spread of faults using zonal electrical distribution [4].

The installation of these power electronic devices may have either positive or negative impacts on the operation and control of distribution systems. To investigate the impacts of these new devices, it is essential to establish a foundation to investigate their properties and to incorporate them in planning and operation studies. Fundamental tools for power system analysis include component and system modeling and steady-state ac/dc power flow. The models and power flow have been used in many applications in planning and operation, such as protection system design, service restoration, power quality analysis, etc. The applications require appropriate models to reflect the actual behavior of system components as well as robust and efficient power flow solution algorithms.

Historically in the power industry, the main power electronics applications have been in High Voltage Direct Current (HVDC) systems, solid state VAR compensators, unified power flow controllers, and others. As a result, a number of models were created to handle these devices and implemented in power flow solvers, see for example [6-12]. In HVDC systems, large inductors are installed in the dc systems to smooth dc currents. Thus, many converter models and subsequent power flow formulations assumed the systems to be three-phase with constant dc currents. In [6-9], the network and loads are assumed to be three-phase balanced. In these models, the converter ac currents were assumed to be filtered and had sinusoidal waveforms with low distortion. The current magnitudes were calculated by performing FFT analysis on the tri-state square ac currents before filters. The dc systems were modeled as constant power ac loads in the power flow solvers.

Some three-phase, unbalanced systems, converter models have also been developed

for HVDC system analysis. In [10][11], a three-phase thyristor converter model was proposed. The imbalance of systems was captured by the conducting periods of thyristors on each phase. In [12], three-phase thyristor converters were modeled as equivalent sequence regulation transformers using modulation theory. In these three-phase models, it was still assumed that the dc currents were constant.

In contrast, power distribution systems are inherently unbalanced systems consisting of single, two and three-phase components and subsystems. Also because of limited space [13], often there are not enough filtering devices to eliminate the harmonics generated by power electronic devices. In addition, installation of large dc capacitors amplifies dc current ripples in some distribution system devices, such as Adjustable Speed Drives (ASDs), As such, the Total Harmonic Distortion (THD) in the dc currents and ac currents could be much higher, e.g. THD is among 40-60% for ASDs [13], than those in HVDC systems. For these reasons, the previous modeling approaches and power flow solvers for HVDC system analysis are not directly applicable to power distribution systems. New modeling techniques are desired to capture the properties of the power electronic devices and to be implemented in distribution system analysis tools.

Furthermore, these new mathematical models and analysis tools should be tested and validated in real-life environments. It is noted that real system data is not always accessible and it is also impractical to perform experiments on real systems for the sole purpose of validation. As such, it is desired to develop scaled-down, flexible, ac/dc system hardware test beds.

1.2 Objectives

The objectives of this work are to

(i) Investigate characteristics of power converters and develop mathematical models for distribution system analysis

(ii) Develop new power flow solvers with appropriate mathematical models to support improved distribution system planning and operation

(iii) Develop hardware and software tools to validate power converter models and the performance of power flow solvers

The framework of this thesis is shown in Figure 1.1.

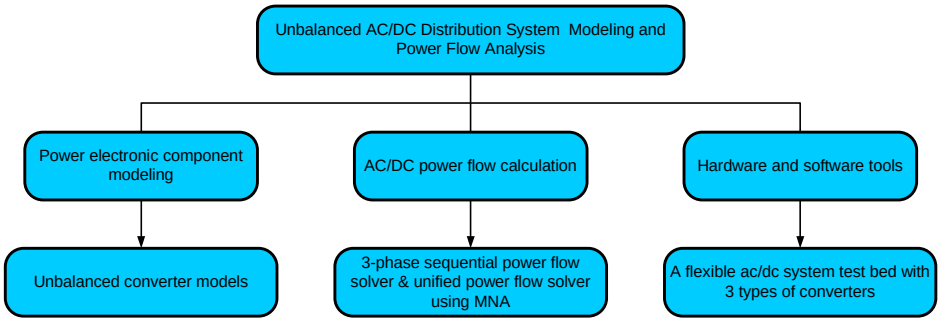


Figure 1.1 The framework of this thesis

The work in this thesis addresses the above objectives and makes the following contributions.

1.3 Summary of Contributions

This thesis provides the following contributions toward improving distribution system operation and control in the presence of power electronic devices:

- Detailed unbalanced converter models using three, delta-connected, single-phase converters for:
  - Three-phase full bridge thyristor converters and diode rectifiers
  - Three-phase Pulse-Width-Modulated (PWM) converters

- Three-phase ac/dc power flow solvers for uni-directional and bi-directional power flow studies in radial or weakly meshed distribution systems
  - A backward/forward sequential solver using a subsystem ranking method
  - A unified solver using the modified nodal analysis method
  - Detailed simulation results on radial and weakly meshed three-phase distribution systems
- A flexible hardware test bed for studying ac/dc power flow and evaluating mathematical system models and analysis tools

1.4 Organization of Thesis

This thesis is organized as follows. In Chapter 2, a new converter modeling approach is proposed for unbalanced power converters. The approach utilizes three, single-phase converters to model three-phase converters under unbalanced operating conditions. The models are able to capture system imbalance using the single-phase converters. The contributions of the single-phase converters to ac/dc power flow are determined by participation coefficients. By introducing equivalence criteria, the converter models become equivalent to three-phase converters with respect to both RMS fundamental ac and average dc currents. They are valid for converters operating in either rectifier mode or inverter mode. The modeling approach is applied to three types of three-phase converters: (i) thyristor converters; (ii) diode rectifiers; and (iii) PWM converters. The three converter models are validated in time domain simulation and steady- state analysis.

Using the converter models from Chapter 2, a three-phase sequential solver and a three-phase unified solver are developed in Chapter 3 and Chapter 4, respectively, for distribution ac/dc power flow studies. In the sequential solver, ac and dc power flows in

subsystems are solved using an iterative backward/forward algorithm. A subsystem ranking method is proposed to determine the sequence for solving power flow. In the unified solver, steady-state Modified Nodal Analysis (MNA) method is implemented to solve ac and dc power flow in a unified manner. Using MNA, impacts among ac and dc systems can be analyzed directly. The ac/dc power flow iterations, which may cause divergence problems, in sequential solvers are avoided. In addition, existing ac and dc nodal analysis programs can be extended to develop the unified power flow program conveniently with moderate modifications.

In order to validate the performance of the theoretical converter models and the power flow solvers, a three-phase ac/dc system hardware test bed has been developed and will be presented in Chapter 5. The test bed contains a flexible network and loads as well as three different three-phase converters: (i) a full-bridge thyristor converter; (ii) a full bridge diode rectifier; and (iii) a variable frequency converter consisting of a diode rectifier and a PWM inverter. Using the test bed, balanced or unbalanced ac/dc systems can be set up for power flow studies. Special attention is paid to the design of the variable frequency converter while the thyristor converter and diode rectifier are existing devices. Using the test bed, ac/dc power flow has been studied in a real-life environment. In addition, time domain simulations using MATLAB Simulink and power flow analysis using the solvers developed in Chapters 3 and 4 have been performed. The delta-connected converter models and the performance of the ac/dc power flow solvers are validated by comparing the steady-state results with the hardware test results. In Chapter 6, conclusions are drawn for this work with outlined contributions. Possible future work is also discussed.

CHAPTER 2. UNBALANCED CONVERTER MODELING: DIODE RECTIFIER, THYRISTOR CONVERTER AND PULSE-WIDTH-MODULATED (PWM) CONVERTER

In this chapter, three-phase converter models are proposed for power distribution system analysis. The models allow for converter operation with continuous and discontinuous dc currents. The following three types of converters are investigated:

- Line-frequency full bridge diode rectifiers
- Line-frequency full bridge thyristor converters
- Pulse-width-modulated (PWM) converters

These converters are modeled using three, delta-connected, single-phase converters. The models are equivalent to three-phase converters with respect to RMS fundamental ac and average dc currents. They can be used in analysis tools such as ac/dc power flow.

Unbalanced converter models are desired to capture characteristics of distribution systems. Power converter based devices, such as adjustable speed drives (ASDs), dc motor drives, flexible AC transmission system (FACTS) devices, have been used at various voltage levels in distribution systems. Distribution systems contain single-phase, two-phase, and three-phase components. As such, the ac voltages applied to and the ac currents flowing in the converters are generally unbalanced.

However, use of these devices results in distorted currents in both the ac and dc systems. Usually, installations of power electronics devices in distribution systems are

limited by physical space [13]. Consequently, the dc inductors, if present, have small inductance and may not be able to significantly reduce the harmonics in the dc currents generated by the converters. Typical ac currents in High Voltage Direct Current (HVDC) links, DC drives, and ASDs [13] are shown Figure 2.1. It can be seen that the current in the HVDC link has less distortion while the currents in the DC drive and ASD are highly distorted.

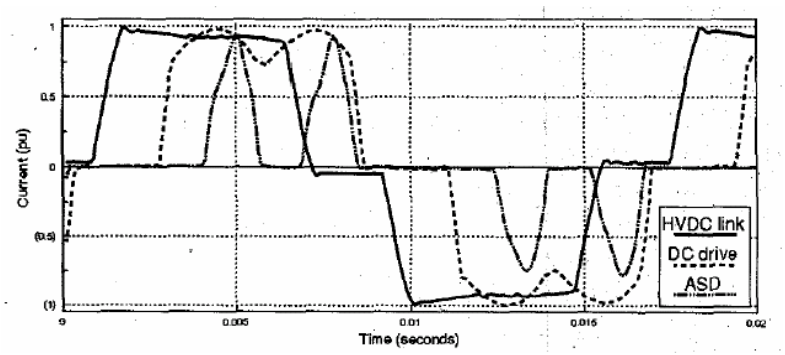


Figure 2.1 Typical current waveforms of HVDC links, 6-pules dc drives, and adjustable speed drives [13]

Traditional converter models for HVDC system studies are not directly applicable to converters in distribution systems. In HVDC systems, thyristor converters have been used for ac/dc conversion with large dc link inductors. The majority of the ac components in the dc link currents are eliminated. Then, based on pure dc currents and tri-state square-wave ac currents, single-phase [6]-[9] and three-phase [10]-[12] converter models have been proposed for HVDC power flow studies. Single-phase HVDC converter models have also been used in power flow studies for certain balanced small ac/dc systems [13][15] and transit railway power systems [16]. In the above models, it was assumed that the dc currents were constant with no harmonics. The converter ac currents

at the fundamental frequency were obtained by performing Fast Fourier Analysis (FFT) on the square-wave shape ac currents. However, the assumption of a constant dc current generally does not hold for ac/dc systems with small dc inductance or large dc capacitance and appropriate models are desired.

More recently, new three-phase converter topologies have been proposed for unbalanced distribution systems [17-19]. Time domain simulations were performed with detailed power electronic device models to verify the feasibility and efficiency of the converters. However, time domain analysis requires detailed component models and becomes complicated and time consuming for large-scale power systems. In order to implement these converters in power flow studies, frequency domain models are desired.

Unbalanced converter models using three, Y-connected, grounded, single-phase converters were proposed for distribution system power flow studies in [20]-[22]. The models used single-phase converters to capture the imbalance in the ac currents. It was assumed that the dc current was continuous and converter ac real power was balanced. In this thesis, the Y-connected models are expanded and improved by using three, delta-connected, single-phase converters. The new models relieve the above two assumptions in the Y-connected models.

The three, delta-connected, single-phase converters in the new model capture the imbalance of ac real power and the ac currents. The contributions of the single-phase converters to the dc link current are represented using participation coefficients. The delta-connected models are equivalent to three-phase converters in terms of both the

RMS fundamental ac currents entering the three-phase converters and the average dc link current. The modeling approach is illustrated in Figure 2.2. The models are:

- Applicable under significantly unbalanced operating conditions
- Valid for converters with either continuous or discontinuous dc currents
- Applicable to both rectifier and inverter operation modes
- Appropriate for both unidirectional and bi-directional power flow studies

They can be used for ac/dc power flow studies in both balanced and unbalanced distribution systems.

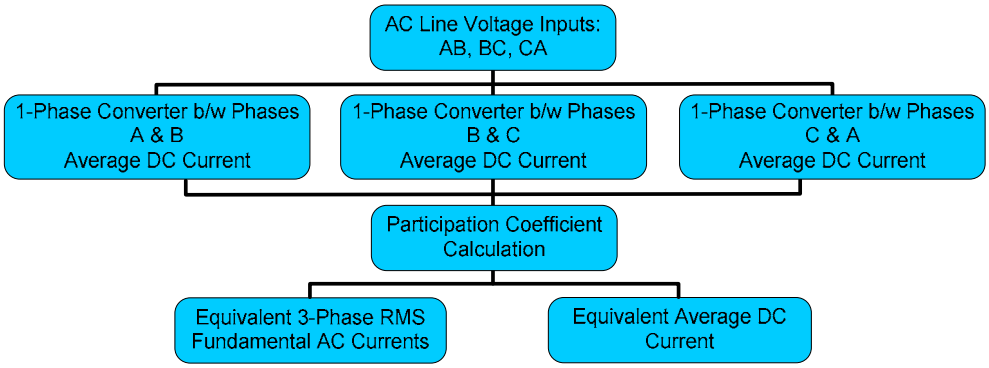


Figure 2.2 The unbalanced, delta-connected converter modeling approach

In the following subsections, equivalent delta-connected models are first proposed for three-phase diode/thyristor converters and PWM converters. Then, an example of the model implemented for converters operating under significantly unbalanced conditions is presented. MATLAB Simulink simulations are performed for a three-phase four-bus ac/dc system. The delta-connected models are tested and verified in both time domain and steady-state. The results are compared with those obtained from the Y-connected models [20]. Hardware tests of the models will be presented in Chapter 5.

2.1 Unbalanced Diode Rectifier and Thyristor Converter Models

The diode rectifiers and thyristor converters under investigation are three-phase line-frequency full bridge converters [1]. It is noted that diode rectifiers have similar characteristics as thyristor converters with zero firing angles. As such, this subsection focuses on modeling thyristor converters. The diode rectifier model follows the same approach and will be discussed at the end of this subsection.

2.1.1 Thyristor Converter Model

The circuit diagram of a three-phase full bridge thyristor converter is shown in Figure 2.3. Please note that the following notation is used:

V_T^{ab}, V_T^{bc}, V_T^{ca}: the RMS line-to-line voltages on the converter ac bus

I_T^a, I_T^b, I_T^c: the RMS ac currents entering the three-phase converters

T_1 to T_6: the six thyristors forming the bridge

L_{dc}, C_{dc}, R_{dc}: the dc inductor, capacitor, and resistor respectively

$I_{T,dc}^{3\phi}$: the average dc current through the dc link

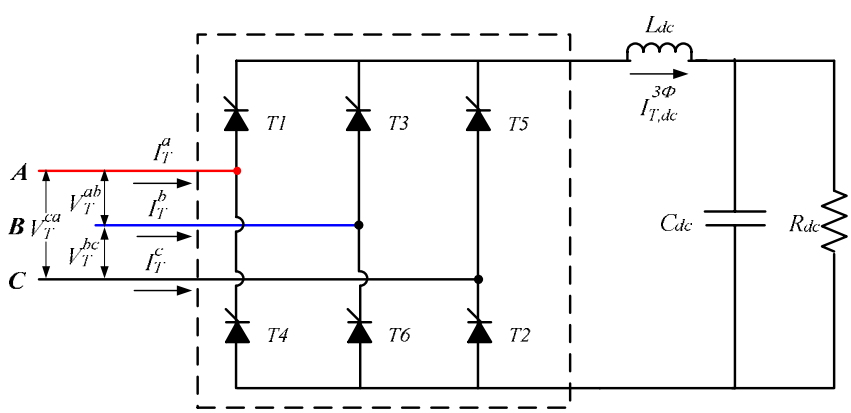


Figure 2.3 Three-phase line-frequency full bridge thyristor converter

The following assumptions are made for the three-phase thyristor converters:

A1. Equi-distant control is used

A2. All firing angles are known

A3. Commutation angles are known

A4. The percentage of the real power loss is known and constant

The dc current of a three-phase converter is either continuous or discontinuous, depending on the network. For example, DC drives usually do not have dc link filters [13] and the dc motor inductance results in continuous dc currents. On the other hand, dc capacitors are generally installed for ac/dc/ac power conversion [1]. For example, most ASDs have large dc capacitors to sustain dc voltages. The capacitors amplify dc current ripples and cause discontinuous dc currents. In order to develop appropriate models for both conduction modes, the following assumptions are made for the dc systems:

A5. The dc capacitor is ignored when the converter is operated in the continuous conduction mode

A6. The dc capacitor voltage is constant when the converter is operated in the discontinuous conduction mode

Based on these assumptions, an equivalent model is developed using three, delta-connected, single-phase thyristor converters as shown in Figure 2.4 with the following notation:

I_T^{ab}, I_T^{bc}, I_T^{ca}: the RMS ac currents entering the three single-phase converters

$I_{T,dc}^{ab}$, $I_{T,dc}^{bc}$, $I_{T,dc}^{ca}$: the average dc currents in the three single-phase converters

$I_{T,dc}^{3\_\Delta}$: the average dc link current

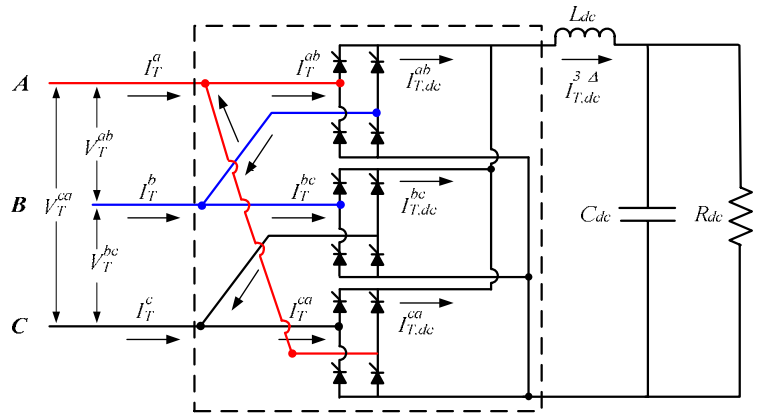


Figure 2.4 Three-phase delta-connected thyristor converter model

In the model, the ac sides of the three single-phase converters are delta-connected. Each converter contributes ac currents to two phases. The dc sides of the converters are in parallel. The sum of the dc currents in the converters gives the dc link current. The model is equivalent to three-phase converters with respect to both the RMS fundamental ac currents entering the three-phase converters and the average dc link current. Details will now be presented.

2.1.1.1 Delta-Connection Approach

The delta-connection modeling approach can be illustrated using the following MATLAB Simulink example for a three-phase unbalanced thyristor converter in the continuous conduction mode. Using the SimPowerSystems toolbox, the converter is operated at firing angles of 10 degrees with a constant resistive dc load. Figure 2.5 shows

the converter instantaneous ac currents, i_T^a, i_T^b, i_T^c, and dc current, $i_{T,dc}^{3\phi}$.

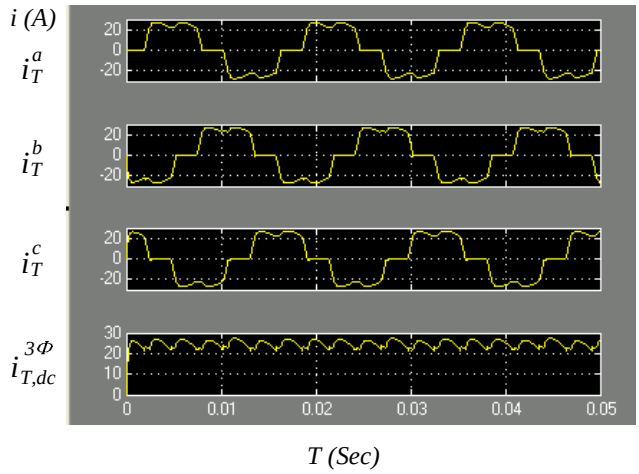


Figure 2.5 The ac and dc currents in a three-phase thyristor converter

From Figure 2.5, the currents in the equivalent, delta-connected thyristor converter model can be obtained through the following observations with T1 to T6 referred to thyristors in Figure 2.3:

- $i_T^{ab}(t)$ is instantaneous ac current flowing between phase *a* and phase *b* when the thyristor pair (T1, T6) or (T3, T4) conducts;
- $i_T^{bc}(t)$ is instantaneous ac current flowing between phase *b* and phase *c* when the thyristor pair (T2, T3) or (T5, T6) conducts;
- $i_T^{ca}(t)$ is instantaneous ac current flowing between phase *c* and phase *a* when the thyristor pair (T1, T2) or (T4, T5) conducts;
- $i_{T.dc}^{ab}(t)$ is instantaneous dc current in the thyristor pairs (T1, T6) and (T3, T4);
- $i_{T,dc}^{bc}(t)$ is instantaneous dc current in the thyristor pairs (T2, T3) and (T5, T6);
- $i_{T,dc}^{ca}(t)$ is instantaneous dc current in the thyristor pairs (T1, T2) and (T4, T5).

Please note that the same approach can be applied to the diode rectifier model and the

PWM converter model.

The currents in the delta-connected model are generated in MATLAB Simulink and shown in Figure 2.6. It is noted that the dc current in each single-phase converter includes nearly linear segments, which correspond to the dc currents through the single-phase converter during commutation. Compared with i_T^a, i_T^b, i_T^c, and $i_{T,dc}^{3\phi}$, it can be seen that the following relationship holds:

$$i_T^a(t) = i_T^{ab}(t) - i_T^{ca}(t),\ \ i_T^b(t) = i_T^{bc}(t) - i_T^{ab}(t),\ \ i_T^c(t) = i_T^{ca}(t) - i_T^{bc}(t) \tag{2.1}$$

$$i_{T,dc}^{3\phi}(t) = i_{T,dc}^{3-\Delta}(t) = i_{T,dc}^{ab}(t) + i_{T,dc}^{bc}(t) + i_{T,dc}^{ca}(t) \tag{2.2}$$

Let i_T^{ab}, i_T^{bc}, and i_T^{ca} be the ac currents and $i_{T,dc}^{ab}$, $i_{T,dc}^{bc}$, $i_{T,dc}^{ca}$ be the dc currents in the three single-phase converters. The model becomes equivalent to the three-phase converter with respect to the ac currents and dc current as shown in (2.1) and (2.2).

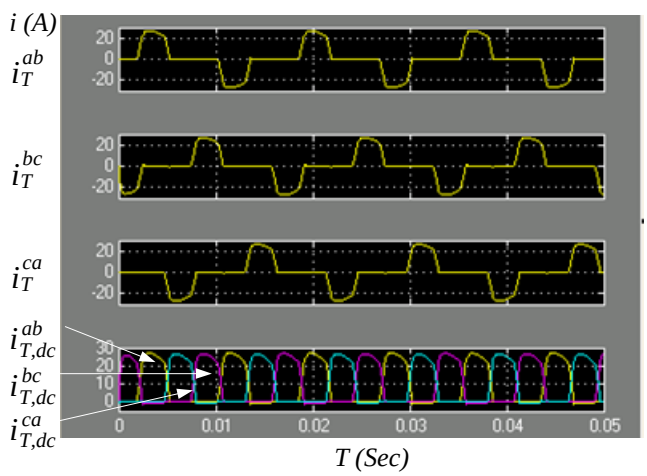


Figure 2.6 The ac and dc currents in the delta-connected converter model

From the above analysis, it can be seen that the single-phase converters have the following characteristics:

(i) Each converter rectifies/inverts one line-to-line voltage;

(ii) At each frequency, each phase current equals the difference of the ac currents entering two single-phase converters, e.g., at the fundamental frequency:

$$I_T^a = I_T^{ab} - I_T^{ca}\ ,\ \ I_T^b = I_T^{bc} - I_T^{ab}\ , I_T^c = I_T^{ca} - I_T^{bc} \tag{2.3}$$

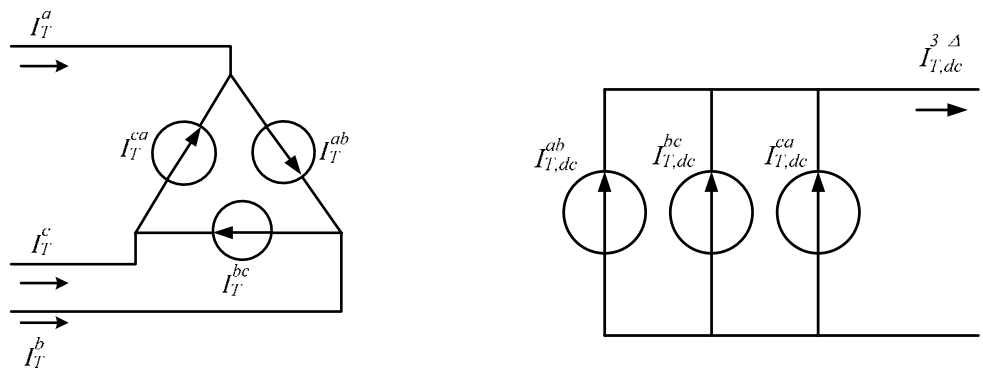
(iii) Their average dc currents add and the sum is the average dc link current:

$$I_{T,dc}^{3\_\Delta} = I_{T,dc}^{ab} + I_{T,dc}^{bc} + I_{T,dc}^{ca} \tag{2.4}$$

(iv) Their average dc power, $P_{T,dc}^{ab}$, $P_{T,dc}^{bc}$, $P_{T,dc}^{ca}$, adds and the sum is the power through the dc link, $P_{T,dc}^{3\_\Delta}$:

$$P_{T,dc}^{3\_\Delta} = P_{T,dc}^{ab} + P_{T,dc}^{bc} + P_{T,dc}^{ca} \tag{2.5}$$

In the model, the ac current in a single-phase converter always flows between the two phases to which it is connected. Hence, the three single-phase converters can be treated as delta-connected current components in the ac systems. On the dc side, the dc link current is equal to the sum of the three dc currents in the single-phase converters. Equivalent ac and dc components are created as shown in Figure 2.7. Based on the equivalent circuits, three-phase converters and the model will be equivalent using participation coefficients and equivalence coefficients. The details are now presented.



(a) The equivalent delta-connected component in ac systems

(b) The equivalent parallel component in dc systems

Figure 2.7 Equivalent ac and dc components of the delta-connected converter model

2.1.2 Determining DC Current and Power in the Delta-Connected Model

The average dc currents, $I_{T,dc}^{LL}$, with $LL \in \{ab, bc, ca\}$, and the average dc power, $P_{T,dc}^{LL}$, in the single-phase converters are now calculated. Figure 2.8 shows the dc currents in a three-phase thyristor converter and the three single-phase converters. It is noted that $i_{T,dc}^{LL}$ and $i_{T,dc}^{3\phi}$ are the same during the full conduction of the three-phase converter. The following notation is used.

$i_{T,dc}^{3\phi}$: the instantaneous dc current in the three-phase converter

$i_{T,dc}^{LL}$: the instantaneous dc currents in the single-phase converters

Subscript $_{1,2}$: start and end respectively

θ_1^{LL}: the starting angles of the linear increasing periods in the single-phase converters, determined by the firing angles

u_1^{LL}: the conduction angles of the linear increasing periods in the single-phase

converters or the commutation angles of the three-phase converter

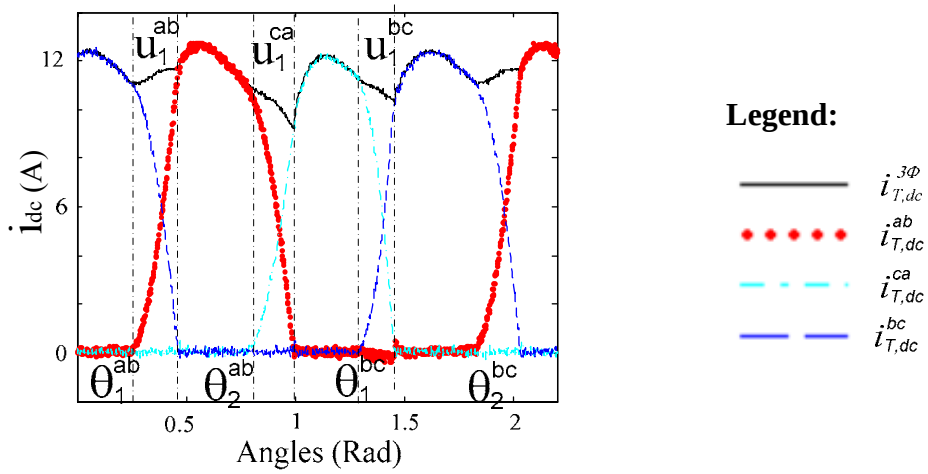


Figure 2.8 The dc currents in a three-phase thyristor converter, $i_{T,dc}^{3\phi}$, and the three single-phase converters, $i_{T,dc}^{LL}$

In order to simplify the model and preserve the real power, the following assumptions are made:

A7. $i_{T,dc}^{LL}$ changes linearly during commutation of the corresponding thyristors in three-phase converters.

A8. During conduction, each single-phase converter's output voltage is equal to that of the three-phase converter. Otherwise, it is open circuit.

A9. The percentages of the real power losses in the single-phase converters are equal to that of the three-phase converter.

Using the above assumptions, the dc current in each single-phase converter, $i_{T,dc}^{LL}$, consists of the following four periods: (ω- the fundamental frequency)

- $\theta_1^{LL} \le \omega t \le \theta_1^{LL} + u_1^{LL}$ - Linear increasing period. $i_{T,dc}^{LL}$ increases linearly from zero when the three-phase converter is in commutation;

- $\theta_1^{LL} + u_1^{LL} \le \omega t \le \theta_2^{LL}$ - Full conduction period. $i_{T,dc}^{LL}$ is equal to $i_{T,dc}^{3\phi}$ and the three-phase converter is in the full conduction.
- $\theta_2^{LL} \le \omega t \le \theta_2^{LL} + u_2^{LL}$ - Linear decreasing period. $i_{T,dc}^{LL}$ decreases linearly to zero when the three-phase converter is in the commutation. θ_2^{LL} is the commutation starting angle. u_2^{LL} is the commutation angle.
- Otherwise, the dc current is equal to zero.

The conduction starting angles, θ_1^{LL}, are dependent on the dc voltages, the firing angles, and the conduction modes. Detailed expressions will be presented in the following sections.

It is noted in Figure 2.8 that during the commutation of the three-phase converter, the dc current in one single-phase converter increases from zero while the dc current in another single-phase converter decreases to zero. As such, the following relationship holds for θ_2^{LL} and u_2^{LL}.

$$\theta_2^{ab} = \theta_1^{ca}, \quad \theta_2^{bc} = \theta_1^{ab}, \quad \theta_2^{ca} = \theta_1^{bc}$$

$$u_2^{ab} = u_1^{ca}, \quad u_2^{bc} = u_1^{ab}, \quad u_2^{ca} = u_1^{bc}$$

Given the conduction angles, the average dc current in each single-phase converter is equal to the average of the instantaneous dc current in a period of π:

$$\begin{aligned} I_{T,dc}^{LL} &= \frac{1}{\pi}\int_0^{\pi} i_{T,dc}^{LL}(\omega t)\, d(\omega t) \\ &= \frac{1}{\pi}\left[\int_{\theta_1^{LL}}^{\theta_1^{LL}+u_1^{LL}} i_{T,dc}^{LL}(\omega t)\cdot d(\omega t) + \int_{\theta_1^{LL}+u_1^{LL}}^{\theta_2^{LL}} i_{T,dc}^{LL}(\omega t)\cdot d(\omega t) + \int_{\theta_2^{LL}}^{\theta_2^{LL}+u_2^{LL}} i_{T,dc}^{LL}(\omega t)\cdot d(\omega t)\right] \end{aligned} \tag{2.6}$$

Based on A8, the dc voltage, $v_{T,dc}^{ab}$, on the single-phase converter between phase *a* and

phase *b* can be determined using the dc voltage on the three-phase converter [1]:

$$v_{T,dc}^{ab}(\omega t)=\begin{cases}\frac{1}{2}\left[v_T^{ab}(\omega t)-v_T^{bc}(\omega t)\right] & \theta_1^{ab}\le\omega t\le\theta_1^{ab}+u_1^{ab}\\ v_T^{ab}(\omega t) & \theta_1^{ab}+u_1^{ab}\le\omega t\le\theta_2^{ab}\\ \frac{1}{2}\left[v_T^{ab}(\omega t)-v_T^{ca}(\omega t)\right] & \theta_2^{ab}\le\omega t\le\theta_2^{ab}+u_2^{ab}\\ v_{T,dc}(\omega t) & otherwise\end{cases} \tag{2.7}$$

where:

v_T^{LL} : the instantaneous line-to-line converter voltages

In a similar manner, $v_{T,dc}^{bc}$ and $v_{T,dc}^{ca}$ follow. The average dc power can be calculated by averaging the instantaneous power in a period of π:

$$P_{T,dc}^{LL}=\frac{1}{\pi}\int_{\theta_1^{LL}}^{\theta_2^{LL}+u_2^{LL}} v_{T,dc}^{LL}(\omega t)\cdot i_{T,dc}^{LL}(\omega t)\cdot d(\omega t) \tag{2.8}$$

The instantaneous dc currents in the single-phase converters are determined differently for the continuous and discontinuous conduction modes. Thus, the average dc current and the average dc power are different in the two conduction modes. They will be discussed respectively next.

2.1.2.1 Continuous Conduction

In the continuous conduction mode, the dc capacitor can be assumed to be zero from A5. During the full conduction period, the dc output voltage, $v_{T,dc}^{LL}(\omega t)$, is equal to the line-to-line voltage, $v_T^{LL}(\omega t)$, as given in (2.7). The instantaneous dc currents, $i_{T,dc}^{LL}$, satisfy the Kirchoff's Current Law (KCL) in the dc system:

$$v_{T,dc}^{LL}(\omega t)=L_{dc}\frac{d\left(i_{T,dc}^{LL}(\omega t)\right)}{dt}+R_{dc}\cdot i_{T,dc}^{LL}(\omega t) \tag{2.9}$$

It is assumed that $\frac{L_{dc}}{R_{dc}}$ is small and then $\frac{di}{dt}$ can be neglected. With the line-to-line voltages defined as:

$$v_T^{LL}(\omega t) = \sqrt{2}\left|V_T^{LL}\right| \cdot \sin\left(\omega t + \delta_{V_T}^{LL}\right) \tag{2.10}$$

where:

$\left|V_T^{LL}\right|$, $\delta_{V_T}^{LL}$: the magnitudes and phase angles of the RMS fundamental line-to-line converter voltages respectively

The dc currents can be simplified as:

$$\begin{aligned} i_{T,dc}^{LL}(\omega t) &\approx \frac{v_{T,dc}^{LL}(\omega t)}{R_{dc}} \\ &= \frac{\sqrt{2}\left|V_T^{LL}\right|}{R_{dc}}\left|\sin\left(\omega t + \delta_{V_T}^{LL}\right)\right| \end{aligned} \tag{2.11}$$

During the linear conduction periods, $i_{T,dc}^{LL}$ changes linearly and is continuous at the boundary of linear conduction periods and the full conduction period. $i_{T,dc}^{LL}$ at $\theta_1^{LL} + u_1^{LL}$ and θ_2^{LL} can be determined using (2.11) and $i_{T,dc}^{LL}$ can be represented as:

$$i_{T,dc}^{LL}(\omega t) = \begin{cases} \frac{\sqrt{2}\left|V_T^{LL}\right|}{R_{dc}}\left|\sin\left(\theta_1^{LL} + u_1^{LL} + \delta_{V_T}^{LL}\right)\right| \cdot \frac{\left(\omega t - \theta_1^{LL}\right)}{u_1^{LL}} & \theta_1^{LL} \le \omega t \le \theta_1^{LL} + u_1^{LL} \\ \frac{\sqrt{2}\left|V_T^{LL}\right|}{R_{dc}}\left|\sin\left(\omega t + \delta_{V_T}^{LL}\right)\right| & \theta_1^{LL} + u_1^{LL} \le \omega t \le \theta_2^{LL} \\ \frac{\sqrt{2}\left|V_T^{LL}\right|}{R_{dc}}\left|\sin\left(\theta_2^{LL} + \delta_{V_T}^{LL}\right)\right| \cdot \left(1 - \frac{1}{u_2^{LL}} \cdot \left(\omega t - \theta_2^{LL}\right)\right) & \theta_2^{LL} \le \omega t \le \theta_2^{LL} + u_2^{LL} \\ 0 & otherwise \end{cases} \tag{2.12}$$

The average dc current, $I_{T,dc}^{LL}$, can be obtained by substituting (2.12) into (2.6):

$$I_{T,dc}^{LL} = \frac{\sqrt{2}\left|V_T^{LL}\right|}{2\pi R_{dc} \cdot u_1^{LL}}\left|\sin\left(\theta_1^{LL} + u_1^{LL} + \delta_{V_T}^{LL}\right)\right| + \frac{\sqrt{2}\left|V_T^{LL}\right|}{2\pi R_{dc} \cdot u_2^{LL}}\left|\sin\left(\theta_2^{LL} + \delta_{V_T}^{LL}\right)\right| \tag{2.13}$$

$$+\frac{\sqrt{2}\left|V_T^{LL}\right|}{\pi R_{dc}}\left(-\cos\left(\theta_2^{LL} + \delta_{V_T}^{LL}\right) + \cos\left(\theta_1^{LL} + u_1^{LL} + \delta_{V_T}^{LL}\right)\right)$$

The conduction angles, θ_1^{LL}, θ_2^{LL}, are determined as follows. With equi-distant control from A1, the firing angle, α_{ab}, is specified to control the thyristors between phase *a* and phase *b*. θ_1^{ab} can be calculated using the line-to-line voltage v_T^{ca} at $\theta_1^{ab} - \alpha_{ab}$, where v_T^{ca} is equal to zero:

$$v_T^{ca}\left(\theta_1^{ab} - \alpha_{ab}\right) = \sqrt{2}\left|V_T^{ca}\right|\sin\left(\theta_1^{ab} - \alpha_{ab} + \delta_{V_T}^{ca}\right) = 0 \tag{2.14}$$

$$\theta_1^{ab} = \theta_2^{bc} = \alpha_{ab} - \delta_{V_T}^{ca} \tag{2.15}$$

θ_1^{LL} and θ_2^{LL} of other single-phase converters are determined:

$$\theta_1^{ca} = \theta_2^{ab} = \theta_1^{ab} + \frac{1}{3}\pi \tag{2.16}$$

$$\theta_1^{bc} = \theta_2^{ca} = \theta_1^{ca} + \frac{1}{3}\pi \tag{2.17}$$

The average power, $P_{T,dc}^{LL}$, in each single-phase thyristor converter can be obtained by substituting $v_{T,dc}^{LL}$ and $i_{T,dc}^{LL}$ in different periods into (2.8). Next, $I_{T,dc}^{LL}$ and $P_{T,dc}^{LL}$ are calculated for the discontinuous conduction mode.

2.1.2.2 Discontinuous Conduction

In the discontinuous conduction mode, it is assumed that the dc capacitor voltage, $V_{C_{dc}}$, is constant. The instantaneous dc link current is equal to zero in the three-phase converter when the thyristors are fired. Hence, there is no commutation and u_1^{LL} and u_2^{LL} are equal to zero. $i_{T,dc}^{LL}$ is equal to the dc current in L_{dc} during

the conduction period (θ_1^{LL} , θ_2^{LL}):

$$i_{T,dc}^{LL}(\omega t)=\frac{1}{\omega L_{dc}}\int_{\theta_1^{LL}}^{\omega t}\left[\sqrt{2}\left|V_T^{LL}\right|\sin\left(\omega t+\delta_{V_T}^{LL}\right)-V_{C_{dc}}\right]d(\omega t) \tag{2.18}$$

$$=\frac{\sqrt{2}\left|V_T^{LL}\right|}{\omega L_{dc}}\left[\cos\left(\theta_1^{LL}+\delta_{V_T}^{LL}\right)-\cos\left(\omega t+\delta_{V_T}^{LL}\right)\right]-\frac{V_{C_{dc}}}{\omega L_{dc}}\left(\omega t-\theta_1^{LL}\right)$$

Otherwise, $i_{T,dc}^{LL}$ is equal to zero. Therefore, $i_{T,dc}^{LL}$ can be represented as:

$$i_{T,dc}^{LL}(\omega t)=\begin{cases}A_{LL}\cdot\cos(\omega t)+B_{LL}\cdot\sin(\omega t)+C_{LL}\cdot\omega t+D_{LL} & \theta_1^{LL}\le\omega t\le\theta_2^{LL}\\ 0 & otherwise\end{cases} \tag{2.19}$$

where:

$$A_{LL}=\frac{-\sqrt{2}\left|V_T^{LL}\right|}{\omega L_{dc}}\cos\left(\delta_{V_T}^{LL}\right),\quad B_{LL}=\frac{\sqrt{2}\left|V_T^{LL}\right|}{\omega L_{dc}}\sin\left(\delta_{V_T}^{LL}\right),$$

$$C_{LL}=-\frac{V_{C_{dc}}}{\omega L_{dc}},\qquad D_{LL}=-A_{LL}\cdot\cos\left(\theta_1^{LL}\right)-B_{LL}\cdot\sin\left(\theta_1^{LL}\right)-C_{LL}\cdot\theta_1^{LL}$$

Then, the average dc current, $I_{T,dc}^{LL}$, can be obtained:

$$I_{T,dc}^{LL}=\frac{1}{\pi}\left[A_{LL}\cdot\left(\sin\left(\theta_2^{LL}\right)-\sin\left(\theta_1^{LL}\right)\right)+B_{LL}\cdot\left(-\cos\left(\theta_2^{LL}\right)+\cos\left(\theta_1^{LL}\right)\right)\right] \tag{2.20}$$

$$+\frac{1}{\pi}\left[\frac{C_{LL}}{2}\cdot\left(\left(\theta_2^{LL}\right)^2-\left(\theta_1^{LL}\right)^2\right)+D_{LL}\cdot\left(\theta_2^{LL}-\theta_1^{LL}\right)\right]$$

Two different cases are considered to determine the conduction angles, θ_1^{LL} and θ_2^{LL}. In the first case, the thyristors are fired when $v_{T,dc}\ge V_{C_{dc}}$. The thyristors start to conduct immediately. θ_1^{LL} is determined in (2.15) to (2.17). At θ_2^{LL}, $i_{T,dc}^{LL}$ decreases to zero in (2.18). θ_2^{LL} can be solved using the Newton method.

In the second case, the thyristors are fired when $v_{T,dc}<V_{C_{dc}}$. The thyristors do not conduct until $v_{T,dc}$ becomes equal to $V_{C_{dc}}$:

$$v_{T,dc}^{LL}\left(\theta_1^{LL}\right)=\sqrt{2}\left|V_T^{LL}\right|\cdot\left|\sin\left(\theta_1^{LL}+\delta_{V_T}^{LL}\right)\right|=V_{C_{dc}} \tag{2.21}$$

θ_1^{LL} can be determined:

$$\theta_1^{LL} = \sin^{-1}\left(\frac{V_{T,dc}}{\sqrt{2}\left|V_T^{LL}\right|}\right) - \delta_{V_T}^{LL} \qquad 0 \le \theta_1^{LL} \le 2\pi \tag{2.22}$$

θ_2^{LL} is determined in the same manner as the first case.

Since there is no commutation, $P_{T,dc}^{LL}$, in the discontinuous conduction mode can be determined using $v_{T,dc}^{LL}$ and $i_{T,dc}^{LL}$:

$$P_{T,dc}^{LL} = \frac{1}{\pi}\int_{\theta_1^{LL}}^{\theta_2^{LL}} v_{T,dc}^{LL}(\omega t)\cdot i_{T,dc}^{LL}(\omega t)\cdot d(\omega t) \tag{2.23}$$

$$= \frac{1}{\pi}\int_{\theta_1^{LL}}^{\theta_2^{LL}} \sqrt{2}\left|V_T^{LL}\right|\cdot\sin\left(\omega t + \delta_{V_T}^{LL}\right)\cdot\left[A_{LL}\cdot\cos(\omega t) + B_{LL}\cdot\sin(\omega t) + C_{LL}\cdot\omega t + D_{LL}\right]\cdot d(\omega t)$$

From above, it can be seen that $I_{T,dc}^{LL}$ and $P_{T,dc}^{LL}$ are not balanced either in the continuous conduction mode or in the discontinuous conduction mode because of the unbalanced voltages. Hence, the contributions of the single-phase converters to the dc link current and the dc power are not equal. This difference is now captured by introducing three scalar dc current participation coefficients, λ_I^{ab}, λ_I^{bc}, λ_I^{ca}, and three scalar dc power participation coefficients, λ_P^{ab}, λ_P^{bc}, λ_P^{ca}, into the model.

2.1.3 Participation Coefficients

In distribution systems, ac voltages and ac currents are generally unbalanced in both magnitude and phase. Hence, each single-phase converter in the delta-connected model contributes differently to the current and the power through the dc link. It is important to determine the contribution of each single-phase converter to the total dc current and power. Three current participation coefficients, $\lambda_{T,I}^{ab}$, $\lambda_{T,I}^{bc}$, $\lambda_{T,I}^{ca}$, are introduced to capture the imbalance of the ac current magnitudes of three-phase converters. $\lambda_{T,I}^{ab}$ is

defined as the ratio of the average dc current, $I_{T,dc}^{ab}$, in the single-phase converter between phase *a* and phase *b* to the sum of the average dc currents in the three single-phase converters:

$$\lambda_{T,I}^{ab} = \frac{I_{T,dc}^{ab}}{I_{T,dc}^{ab} + I_{T,dc}^{bc} + I_{T,dc}^{ca}} \tag{2.24}$$

In a similar manner, $\lambda_{T,I}^{bc}$ and $\lambda_{T,I}^{ca}$ follow.

Three real power participation coefficients, $\lambda_{T,P}^{ab}$, $\lambda_{T,P}^{bc}$, $\lambda_{T,P}^{ca}$, are introduced to capture the imbalance of ac real power in three-phase converters in terms of average dc power in the single-phase converters. $\lambda_{T,P}^{ab}$ is defined as the ratio of the average dc power , $P_{T,dc}^{ab}$, of the single-phase converter between phase *a* and phase *b* to the sum of the average dc power on the three single-phase converters:

$$\lambda_{T,P}^{ab} = \frac{P_{T,dc}^{ab}}{P_{T,dc}^{ab} + P_{T,dc}^{bc} + P_{T,dc}^{ca}} \tag{2.25}$$

Similarly, $\lambda_{T,P}^{bc}$ and $\lambda_{T,P}^{ca}$ follow. Next, the delta-connected model will be made equivalent to a three-phase converter with respect to the RMS fundamental ac and the average dc currents.

2.1.4 Equivalence Transformation

From above, three-phase thyristor converters are modeled as three, delta-connected, singe-phase converters. The models are made equivalent with respect to the RMS fundamental ac and the average dc currents entering/leaving the three-phase converter. A dc equivalence coefficient, $K_{T,dc}$, is introduced to equalize the dc link currents in Figure

2.3 and Figure 2.4. It is defined as the ratio of the average dc current of a three-phase thyristor converter, $I_{T,dc}^{3\phi}$, to the average dc current, $I_{T,dc}^{3\_\Delta}$, of the delta-connected model:

$$K_{T,dc} = \frac{I_{T,dc}^{3\phi}}{I_{T,dc}^{3\_\Delta}} \tag{2.26}$$

$I_{T,dc}^{3\phi}$ is equal to the average of the instantaneous dc current in a period of 2π:

$$\begin{aligned} I_{T,dc}^{3\phi} &= \frac{1}{2\pi}\int_0^{2\pi} i_{T,dc}^{3\phi}(t)\cdot d(\omega t) \\ &= \frac{1}{2\pi}\int_0^{2\pi}\left[\left(i_{T,dc}^{ab}(t)+i_{T,dc}^{ca}(t)\right)+\left(i_{T,dc}^{bc}(t)+i_{T,dc}^{ab}(t)\right)+\left(i_{T,dc}^{ca}(t)+i_{T,dc}^{bc}(t)\right)\right]\cdot d(\omega t) \\ &= I_{T,dc}^{3\_\Delta} \end{aligned} \tag{2.27}$$

Thus,

$$K_{T,dc} = 1 \tag{2.28}$$

Now, the ac sides of the two models will be equalized with respect to the RMS fundamental ac currents. From the ac equivalent representation of the converter model in Figure 2.9, it can be seen that the phase currents entering a three-phase converter can be obtained using the ac currents entering the delta-connected single-phase converters:

$$I_T^a = I_T^{ab} - I_T^{ca}, \quad I_T^b = I_T^{bc} - I_T^{ab}, I_T^c = I_T^{ca} - I_T^{bc} \tag{2.29}$$

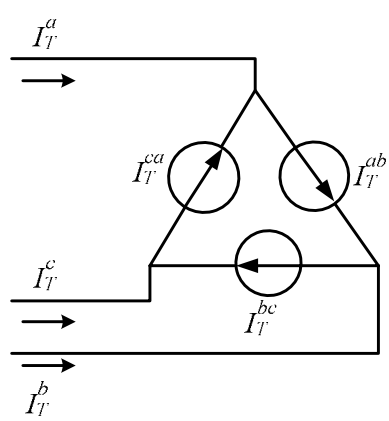


Figure 2.9 The ac equivalent component of the delta-connected converter model

It is noted that instantaneous ac current, i_T^{LL}, is periodic and its absolute value gives the instantaneous dc current:

$$\left|i_T^{LL}(\omega t)\right| = i_{T,dc}^{LL}(\omega t) \tag{2.30}$$

By performing Fourier analysis on i_T^{LL}, the current magnitude, $\left|I_T^{LL}\right|$, can be obtained:

$$\left|I_T^{LL}\right| = \frac{\sqrt{a_{LL}^2 + b_{LL}^2}}{\sqrt{2}} \tag{2.31}$$

where:

a_{LL}, b_{LL}: the Fourier coefficients of the fundamental component in i_T^{LL}

The Fourier coefficients of the fundamental component can be calculated as follows. Details are provided in Appendix A:

$$a_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}(\omega t)\cdot\cos(\omega t)\cdot d(\omega t) \tag{2.32}$$

$$b_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}(\omega t)\cdot\sin(\omega t)\cdot d(\omega t) \tag{2.33}$$

AC equivalence coefficients, K_T^{LL}, are introduced to relate the ac current magnitudes, $\left|I_T^{LL}\right|$, to the average dc currents, $I_{T,dc}^{LL}$, in the single-phase converters. It is defined as:

$$K_T^{LL} = \frac{\left|I_T^{LL}\right|}{I_{T,dc}^{LL}} \tag{2.34}$$

From A9, the real power on the ac side of each single-phase converter is equal to the average dc power in the single-phase converter multiplied by a loss factor:

$$P_T^{LL} = P_{T,dc}^{LL}\cdot C_T^{loss} \tag{2.35}$$

where:

P_T^{LL}: the ac real power in the single-phase converters in the equivalent model

C_T^{loss}: the loss factor of the single-phase converters. $C_T^{loss} > 1$ for lossy rectifiers, $C_T^{loss} < 1$ for lossy inverters, $C_T^{loss} = 1$ for lossless converters

2.1.5 Diode Rectifier Model

Three-phase diode rectifiers are also operated in either the continuous conduction mode or the discontinuous conduction mode. In both conduction modes, the delta-modeling approach for thyristor converters applies. In order to determine the parameters of the model, the conduction angles, θ_1^{LL}, θ_2^{LL}, are calculated differently for diode rectifiers.

In the continuous conduction mode, the conduction of the diodes depends on the line-to-line voltages on the rectifier. For the single-phase rectifier between phase *a* and phase *b*, the following equations holds at θ_1^{ab} and θ_2^{ab}:

$$v_D^{ca}\left(\theta_1^{ab}\right) = \sqrt{2}\left|V_D^{ca}\right|\sin\left(\theta_1^{ab} + \delta_{V_D}^{ca}\right) = 0 \tag{2.36}$$

$$v_D^{bc}\left(\theta_2^{ab}\right) = \sqrt{2}\left|V_D^{bc}\right|\sin\left(\theta_2^{ab} + \delta_{V_D}^{bc}\right) = 0 \tag{2.37}$$

where:

$v_D^{LL}(\omega t)$: the instantaneous line-to-line voltages

$\left|V_D^{LL}\right|, \delta_{V_D}^{LL}$: the magnitudes and angles of the RMS fundamental line-to-line voltages

Solving (2.36) and (2.37) gives θ_1^{ab} and θ_2^{ab}:

$$\theta_1^{ab} = -\delta_{V_D}^{ca}, \quad \theta_2^{ab} = -\delta_{V_D}^{bc} \tag{2.38}$$

Similarly, the conduction angles of the other two single-phase diode rectifiers are obtained:

$$\theta_1^{bc} = -\delta_{V_D}^{ab}, \quad \theta_2^{bc} = -\delta_{V_D}^{ca} \tag{2.39}$$

$$\theta_1^{ca} = -\delta_{V_D}^{bc}, \quad \theta_2^{bc} = -\delta_{V_D}^{ab} \tag{2.40}$$

In the discontinuous conduction mode, the conduction angles are determined in the same manner as thyristor converters with zero firing angles.

2.2 Unbalanced Pulse-Width-Modulated (PWM) Converter Model

Three-phase PWM converters, shown in Figure 2.10, are modeled using three, delta-connected, single-phase PWM converters in Figure 2.11 with the following notation:

V_{PWM}^{LL} : the RMS line-to-line voltages on the single-phase PWM converters

I_{PWM}^{p} : the RMS ac currents entering three-phase PWM converters, $p \in \{a,b,c\}$

I_{PWM}^{LL} : the RMS ac currents entering the single-phase PWM converters

$I_{PWM,dc}^{LL}$: the average dc currents of the single-phase PWM converters

$I_{PWM,dc}^{3\phi}$: the average dc link current in three-phase PWM converters

$I_{PWM,dc}^{3\_\Delta}$: the average dc link currents in the model

$V_{PWM,dc}$: the dc voltage of three-phase PWM converters

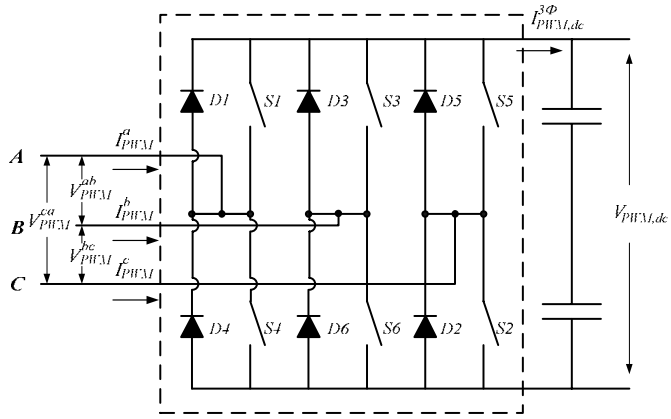


Figure 2.10 Three-phase PWM converter

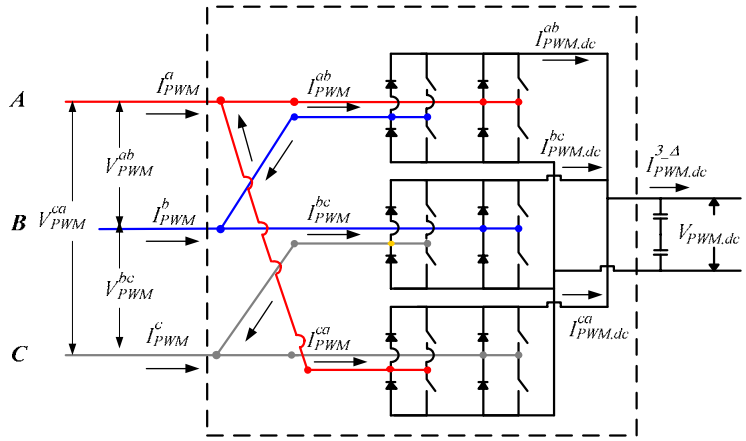


Figure 2.11 Three-phase delta-connected PWM converter model

In Figure 2.11, the ac sides of the single-phase converters are delta-connected. The dc sides of the converters are in parallel. Each single-phase PWM rectifier (inverter) has a line-to-line voltage, V_{PWM}^{LL}, as input (output). Their common dc output (input) is the voltage on the dc link, $V_{PWM,dc}$. The following assumptions are made for PWM converters:

A10. Bipolar PWM switching scheme is used;

A11. The amplitude modulation ratios, m_{LL}, are less than or equal to 1.

where: $m_a = \dfrac{\hat{V}_{control}}{\hat{V}_{tri}}$,

$\hat{V}_{control}$: the peak amplitude of the sinusoidal control signal.

$\hat{V}_{tri}$: the amplitude of the switching-frequency triangular signal

From the assumptions, the line-to-line voltage magnitudes, $\left|V_{PWM}^{LL}\right|$, at the fundamental frequency and the dc voltage, $V_{PWM,dc}$, satisfy the following equation:

$$\left|V_{PWM}^{LL}\right| = \frac{\sqrt{3}\cdot m_{LL}}{2\sqrt{2}}\cdot V_{PWM,dc} \tag{2.41}$$

The ac currents entering the single-phase PWM converter have the following relationship with the ac phase currents entering the three-phase PWM converters:

$$I_{PWM}^{a} = I_{PWM}^{ab} - I_{PWM}^{ca}\ ,\ \ I_{PWM}^{b} = I_{PWM}^{bc} - I_{PWM}^{ab}\ , I_{PWM}^{c} = I_{PWM}^{ca} - I_{PWM}^{bc}$$

$$I_{PWM}^{ab} + I_{PWM}^{ca} + I_{PWM}^{bc} = 0 \tag{2.42}$$

The real power, P_{PWM}^{LL}, in each single-phase PWM converter is:

$$P_{PWM}^{LL} = real\left(V_{PWM}^{LL}\ \cdot\left(I_{PWM}^{LL}\right)^{*}\right) \tag{2.43}$$

It is also assumed that A4 and A9 in the thyristor converter model hold for the PWM converter model. The following relationship exists between the ac real power and dc power on each single-phase PWM converter:

$$P_{PWM}^{LL} = P_{PWM,dc}^{LL}\cdot C_{PWM}^{loss} \tag{2.44}$$

where:

C_{PWM}^{loss} : the loss factor, $C_{PWM}^{loss} > 1$ for lossy rectifiers, $C_{PWM}^{loss} < 1$ for lossy inverters, $C_{PWM}^{loss} = 1$ for lossless converters

Then, $I_{PWM,dc}^{LL}$ can be formulated as a function of the ac currents, I_{PWM}^{LL} :

$$I_{PWM,dc}^{LL} = \frac{P_{PWM,dc}^{LL}}{V_{PWM,dc}} = \frac{P_{PWM}^{LL}}{C_{PWM}^{loss} \cdot V_{PWM,dc}} \tag{2.45}$$

$$= \frac{real\left(V_{PWM}^{LL} \cdot \left(I_{PWM}^{LL}\right)^{*}\right)}{C_{PWM}^{loss} \cdot V_{PWM,dc}}$$

The average dc current in the dc link is equal to the sum of the average dc current in each single-phase PWM converter:

$$I_{PWM,dc}^{3\phi} = I_{PWM,dc}^{3\_\Delta} = I_{PWM,dc}^{ab} + I_{PWM,dc}^{bc} + I_{PWM,dc}^{ca} \tag{2.46}$$

The average power in the dc link, $P_{PWM,dc}^{3\phi}$, is determined by the dc voltage and average dc current:

$$P_{PWM,dc}^{3\phi} = V_{PWM,dc} \cdot I_{PWM,dc}^{3\phi} \tag{2.47}$$

$$= P_{PWM,dc}^{ab} + P_{PWM,dc}^{bc} + P_{PWM,dc}^{ca} = P_{PWM,dc}^{3\_\Delta}$$

Using the above formulation, the delta-connected model is equivalent to three-phase PWM converters with respect to both the RMS fundamental ac phase currents entering the three-phase converters and the average dc current. The real power is also preserved.

2.3 Three-Phase Converter Model Under Two-Phase Operating Conditions

Three-phase converters are generally operated under three-phase conditions. Protection systems will trip the converters at significantly unbalanced operating conditions such as heavily unbalanced ac loads, short circuits or open circuits. However, it might be possible to operate three-phase converters with only two phases under certain emergency circumstances where uninterrupted power supply is desired. The

proposed modeling approach can be applied to perform system analysis under this condition. An example is shown in Figure 2.12 with a three-phase thyristor converter under two-phase operating conditions. It is assumed that there is an open circuit on phase *c* but the thyristors are still operated under the equi-distant control. There is no current on phase *c* but there are currents on phases *a* and *b* in the converter.

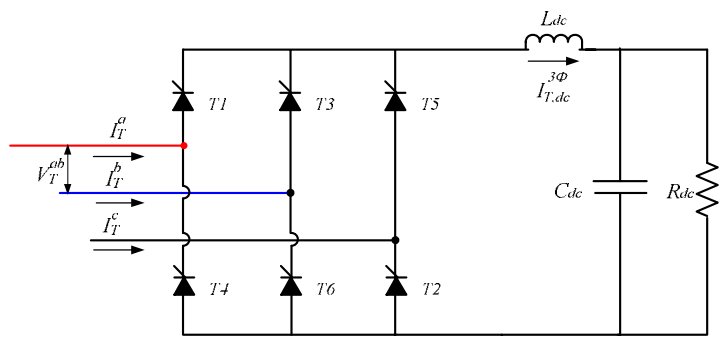


Figure 2.12 A three-phase thyristor converter under two-phase operating condition with phase *c* open

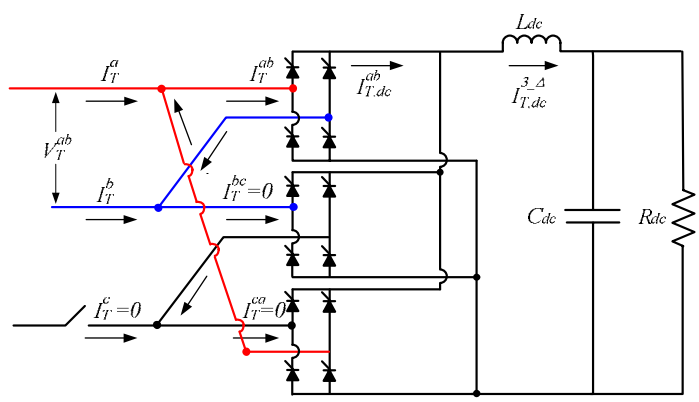


Figure 2.13 The equivalent model of a three-phase converter under two-phase operating condition with phase *c* open

The three-phase converter in Figure 2.12 is equivalent to the delta-connected model with open circuits on the two single-phase converters connected to phase *c*. The

equivalent circuit is shown in Figure 2.13. The average dc currents on the three single-phase converters will be:

$$I_{T,dc}^{ab} = \frac{1}{\pi}\int_0^{\pi} i_{T,dc}^{ab}(t)\cdot(\omega t), \qquad I_{T,dc}^{bc} = 0, \qquad I_{T,dc}^{ca} = 0 \tag{2.48}$$

As such, only the participation coefficients $\lambda_{T,I}^{ab}$ and $\lambda_{T,P}^{ab}$ are not equal to zero:

$$\lambda_{T,I}^{ab} = 1, \qquad \lambda_{T,I}^{bc} = 0, \qquad \lambda_{T,I}^{ca} = 0 \tag{2.49}$$

$$\lambda_{T,P}^{ab} = 1, \qquad \lambda_{T,P}^{bc} = 0, \qquad \lambda_{T,P}^{ca} = 0 \tag{2.50}$$

In the model, the current magnitude, $\left|I_T^{ab}\right|$, is calculated using $\lambda_{T,I}^{ab}$, $K_{T,dc}$, and K_T^{ab}. I_T^{bc} and I_T^{ca} are equal to zero. Therefore, the currents in phase *a* and phase *b*, I_T^a, I_T^b, in the three-phase converter are determined by I_T^{ab} only:

$$I_T^a = I_T^{ab} - I_T^{ca} = I_T^{ab} \tag{2.51}$$

$$I_T^b = I_T^{bc} - I_T^{ab} = -I_T^{ab} \tag{2.52}$$

The same approach can be used for three-phase diode converters and three-phase PWM converters under significant unbalanced conditions. Next, the delta-connected models are investigated in steady-state analysis and are compared with three-phase converters in time domain simulations.

2.4 Evaluation of Unbalanced AC/DC Converter Models

Delta-connected converter models are developed in this chapter for steady-state analysis such as power flow studies, in unbalanced distribution systems. They are equivalent to three-phase converters with respect to the RMS fundamental ac and the average dc currents. Since traditional HVDC converter models for steady-state analysis

are not directly applicable to distribution system converters, they cannot be used to evaluate the delta-connected models. As an alternative, three-phase converters are studied by performing time domain simulations. Time domain analysis can provide accurate voltage and current profile with detailed component models for unbalanced circuits. As such, time domain simulation results can be used to assess the delta-connected models. Three types of converters are investigated:

- Three-phase thyristor converters
- Three-phase diode rectifiers
- Three-phase PWM converters

Each of the above converters is embedded into an unbalanced ac/dc system as the benchmarks and is tested in Simulink.

For comparison, the three-phase converters are modeled and studied using the corresponding delta-connected models in steady-state. By applying the same voltages on the converters as those in the benchmarks, the equivalence coefficients and participation coefficients are calculated for the delta-connected, single-phase converters. Then using the model, the ac currents and ac power in three-phase converters are compared with those obtained from the benchmarks.

2.4.1 Three-Phase Thyristor Converter Benchmark and Evaluation of the Delta-Connected Model

In order to study three-phase thyristor converters, a 4-bus unbalanced ac/dc system was created with the circuit diagram shown in Figure 2.14. In the system, three-phase, balanced, 208 V_{LL} power is fed to a 4-bus system with two identical, three-phase, unbalanced distribution lines and a three-phase full-bridge thyristor converter. Both ac lines are decoupled and their parameters are scaled down from actual distribution lines. There are two loads in the system: an unbalanced ac load on bus 2 and a dc load on bus 4. Both of the loads are constant impedance loads. The parameters of the system components are shown in Table 2.1.

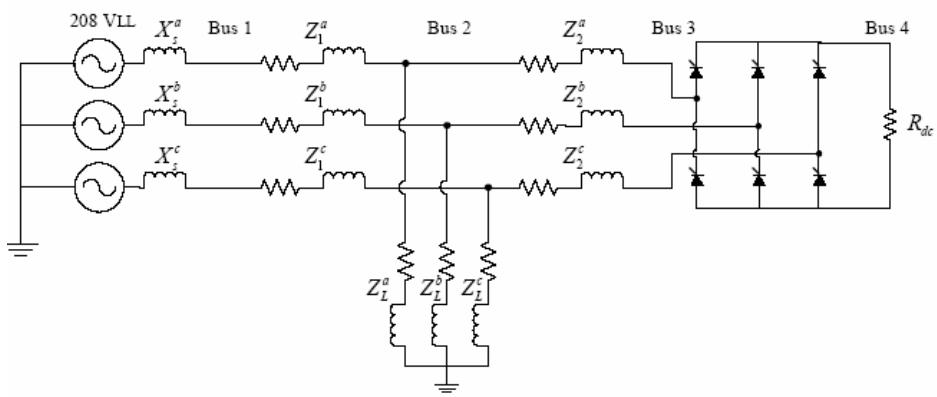


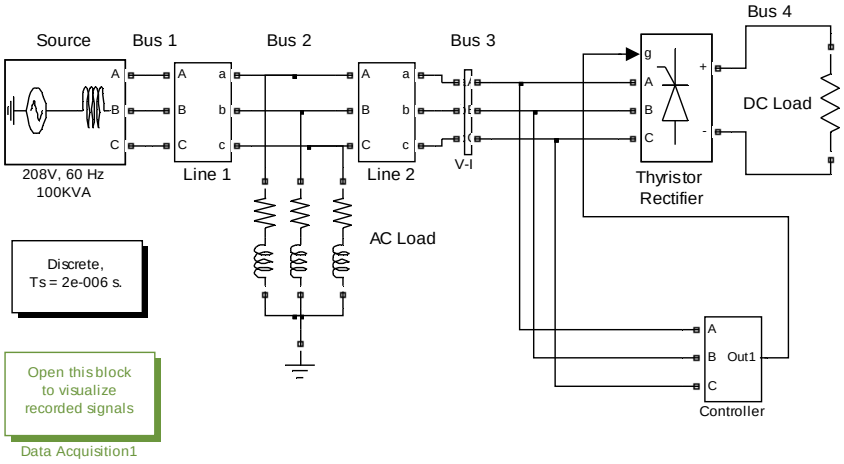
Figure 2.14 The circuit diagram of a 4-bus unbalanced ac/dc system with a three-phase thyristor converter

Table 2.1 Component parameters of the 4-bus ac/dc system with a three-phase thyristor converter

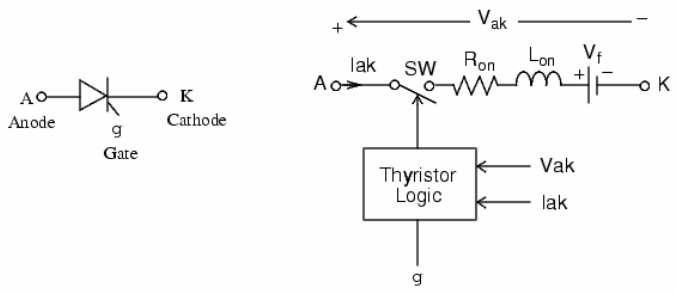
Parameters	Values
Source line-to-line voltage	208 V @ 60 Hz
Source impedance	$X_s^a = X_s^b = X_s^c = 0.3 \quad \Omega$
Line 1 & 2 impedance	$Z_1^a = Z_2^a = 0.1410 + j0.4400 \quad \Omega$ $Z_1^b = Z_2^b = 0.1370 + j0.4420 \quad \Omega$ $Z_1^c = Z_2^c = 0.1210 + j0.4460 \quad \Omega$
AC load impedance	$Z_L^a = 20 + j9 \quad \Omega$ $Z_L^b = 10 + j4.5 \quad \Omega$ $Z_L^c = 7 + j3.2 \quad \Omega$
DC load impedance	$R_{dc} = 10 \quad \Omega$
Converter snubber resistance	100 Ω
Converter snubber capacitance	0.1 uF
Converter conducting impedance	0.001 Ω
Converter forward voltage	0.7 V
Firing angles	10°

2.4.1.1 Simulation Results of the Thyristor Converter Benchmark

The circuit in Figure 2.14 was built in MATALAB Simulink using the SimPowerSystems Toolbox for time domain simulation. The Simulink circuit is shown in Figure 2.15. The thyristor model in the three-phase full-bridge thyristor converter is simulated as a resistor R_{on}, an inductor L_{on}, and a DC voltage source V_f, connected in series with a switch. The switch is controlled by a logical signal depending on the voltage V_{ak}, the current I_{ak}, and the gate signal g.



(a) The 4-bus unbalanced ac/dc system diagram



(b) The detailed thyristor model in MATLAB Simulink

Figure 2.15 The Simulink circuit of the 4-bus unbalanced ac/dc system with a three-phase thyristor converter

A discrete solver was selected with a step size of 2 us. Each simulation has been run for 0.05 seconds, which corresponds to approximately three cycles at 60 Hz. After this time, the initial transients in the voltage and current waveforms diminish and the variation of ac and dc voltages, currents and power calculated in Simulink is less than 0.01%. It is noted that the converter's ac bus is Bus 3 and its dc bus is Bus 4. In order to evaluate the model, the following signals directly related to the three-phase thyristor

converter were measured and shown in Figure 2.15 and Figure 2.16.

- The line-to-neutral voltages on Bus 3, $v_T^p(t)$, $p \in \{a,b,c\}$
- The ac currents entering the thyristor converter, $i_T^p(t)$
- The dc voltage on Bus 4, $v_{T,dc}(t)$
- The dc current, $i_{T,dc}^{3\phi}(t)$

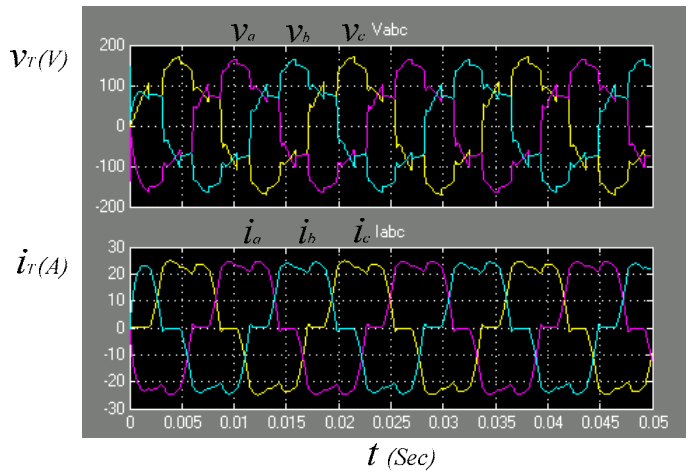


Figure 2.15 Line-to-neutral voltages (top) and ac currents (bottom) in the three-phase thyristor converter benchmark

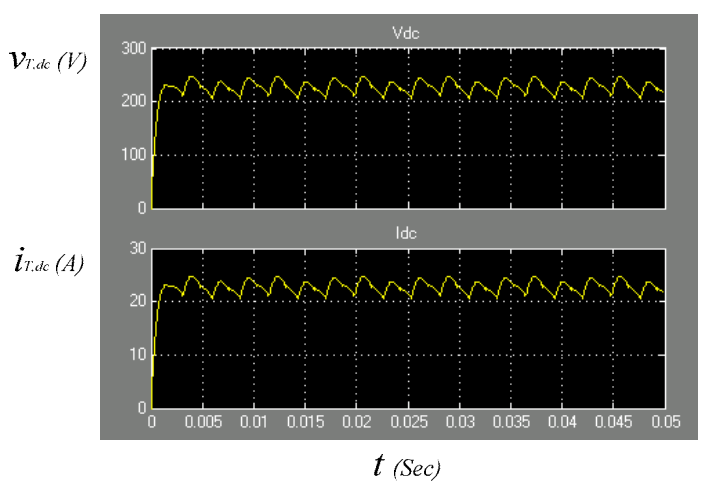


Figure 2.16 DC voltage (top) and dc current (bottom) in the three-phase thyristor converter benchmark

The ac voltages, currents, power at 60 Hz and dc voltage, current and power were calculated using measurement blocks from the SimPowerSystems Toolbox and are shown in Table 2.2.

Table 2.2 Numerical results of the three-phase thyristor converter benchmark using Simulink

Parameters	AC Values at 60Hz on Bus 3		
	Phase A	Phase B	Phase C
V_T^p (V)	$105.5890\angle\text{-}10.48^o$	$103.0332\angle\text{-}132.29^o$	$102.1528\angle 106.47^o$
I_T^p (A)	$17.6314\angle\text{-}26.48^o$	$18.0152\angle\text{-}147.88^o$	$17.4477\angle 91.71^o$
S_T^p (VA)	1789.5708+j513.1080	1787.8748+j498.8428	1723.5181+j454.0926
	DC Values on Bus 4		
$V_{T,dc}$ (V)	228.7181		
$I_{T,dc}^{3\phi}$ (A)	22.8718		
$P_{T,dc}^{3\phi}$ (W)	5242.9501		

Since the voltages applied on the converter are unbalanced, both the ac currents and power entering the converter are also unbalanced. The total real power entering the converter is *5300.9637* watts. Compared with the dc power, the converter real power loss is *1.09%*.

2.4.1.2 Evaluating the Delta-Connected Thyristor Converter Model

The three-phase thyristor converter was studied using the equivalent delta-connected model in steady-state. The goal is to determine whether the participation coefficients and equivalence coefficients can provide accurate estimation of ac currents and real power in

the three-phase converter. As such, it is assumed that the dc voltage in the model is equal to those obtained from Simulink.

First, the participation coefficients and the equivalence coefficients in the model were calculated using (2.24), (2.25), and (2.34). The results are provided in Table 2.3.

Table 2.3 Current participation coefficients, $\lambda_{T,I}^{LL}$, power participation coefficients, $\lambda_{T,P}^{LL}$, and equivalence coefficients, K_T^{LL} ,in the 1-phase thyristor converters

Parameters	Line AB	Line BC	Line CA
$\lambda_{T,I}^{LL}$	0.3447	0.3339	0.3214
$\lambda_{T,P}^{LL}$	0.3501	0.3356	0.3143
K_T^{LL}	1.3369	1.3407	1.3412

Remarks:

- $\lambda_{T,I}^{LL}$ are not equal because the unbalanced line-to-line voltages applied on the single-phase converters resulted in unequal average dc currents in the single-phase converters..
- $\lambda_{T,P}^{LL}$ are not equal and the ratios among them are not the same as those among $\lambda_{T,I}^{LL}$. It is because both the dc currents and voltages are different among the single-phase converters.
- K_T^{LL} are the ratios between the magnitudes of the RMS fundamental ac currents and the average dc currents in the model. They are not equal because the

different distortions in the currents gave different magnitudes obtained from an FFT in (2.31).

By applying the dc voltage on the dc load, the dc current and dc power can be calculated. They are equal to those obtained from Simulink. Using the model's coefficients, the dc currents and dc power in the single-phase converters were calculated. Thus, the ac currents and real power entering the single-phase converters were calculated, given the converter loss percentage equal to that in the benchmark. Then, the ac currents, I_T^p, and power, S_T^p, entering the three-phase converter were calculated. In addition, I_T^p and S_T^p are also calculated using the Y-connected model in [21]. The results from both models are shown in Table 2.4. I_T^p and S_T^p are compared to those from the benchmark using the following formula:

$$\Delta\left|I_T^p\right| = \left|\frac{\left|I_T^p\right|_{model} - \left|I_T^p\right|_{benchmark}}{\left|I_T^p\right|_{benchmark}}\right| \cdot 100\%$$

$$\Delta\left|S_T^p\right| = \left|\frac{\left|S_T^p\right|_{model} - \left|S_T^p\right|_{benchmark}}{\left|S_T^p\right|_{benchmark}}\right| \cdot 100\%$$

The difference is in percentage with respect to the benchmark.

Table 2.4 The ac currents, I_T^p, and ac power, S_T^p in the three-phase thyristor converter using the Δ-connected model and the Y -connected model

Parameters	Δ- Connected Model	$\Delta\left\|I_T^p\right\|$ (%)	Y-Connected Model	$\Delta\left\|I_T^p\right\|$ (%)
I_T^a (A)	$17.4907\angle\text{-}26.67^o$	0.7981	$16.9421\angle\text{-}26.48^o$	3.9096
I_T^b (A)	$17.9806\angle\text{-}147.23^o$	0.1922	$16.6002\angle\text{-}147.88^o$	**7.8546**

I_T^c (A)	$17.5918\angle 91.66^o$	**0.8256**	$16.3784\angle 91.71^o$	6.1288
	Δ - Connected Model	$\Delta\left\|S_T^p\right\|$ (%)	Y-Connected Model	$\Delta\left\|S_T^p\right\|$ (%)
S_T^a (VA)	1767.6931+j517.0740	0.7979	1766.9879+j311.5221	**3.6218**
S_T^b (VA)	1788.47718+j466.8529	0.1922	1766.9879+j311.5221	3.3355
S_T^c (VA)	1744.7727+j458.76203	**0.8255**	1766.9879+j311.5221	0.6686

Remarks:

- The maximal error in the ac currents and ac power is 0.8256% in the delta-connected converter model. It is attributed to I_T^c.
- The maximal error in the ac currents and ac power is 7.8546% in the wye-connected converter model. The source of the error is the assumption that the ac power entering the converter is balanced.

Here, the delta-connected modeling approach outperforms the Y-connected modeling approach and is preferable. Thus, a focus on the delta-connected modeling error is now investigated.

Error Analysis:

Two main sources of error come from assumptions A7 and A9 on the delta-connected converter model:

A7. The dc currents are linear in the model during the commutation of the three-phase converter.

A9. The power loss percentages of the single-phase converters are balanced.

Time domain simulations show that the converter dc currents during commutation were nonlinear. Hence, assumption A7 introduced errors in the dc currents in steady-state analysis. As a consequence, the magnitudes of the RMS fundamental ac currents in the single-phase converters, $\left|I_T^{LL}\right|$, are affected. Assumption A9 affects the ac real power in the single-phase converters, P_T^{LL}. Since I_T^p and S_T^p are calculated using $\left|I_T^{LL}\right|$ and P_T^{LL} from the delta-connected model, A7 and A9 affect both I_T^p and S_T^p.

In order to study which assumption contributes relatively more errors, a balanced three-phase converter was tested and the impact of A9 was minimized. The results are provided in Appendix B. It is shown that the maximal error is 0.6042% in steady-state because of the linearized dc current during the converter commutation. If A7 contributes a similar percentage of errors in both balanced and unbalanced converters, then A7 contributes relatively more errors to the converter model than A9.

2.4.2 Three-Phase Diode Rectifier Benchmark and Evaluation of the Delta-Connected Model

The same 4-bus ac/dc circuit in Figure 2.14 is used to test three-phase diode rectifiers. The thyristor converter is replaced with a three-phase full bridge diode rectifier, which is now used as the benchmark.

2.4.2.1 Simulation Results of the Diode Rectifier Benchmark

The benchmark circuit was built in Simulink. The diode rectifier's snubber parameters and forward voltage are equal to those in Table 2.1. The same discrete solver

and simulation time were used as the thyristor converter benchmark. Table 2.5 shows the ac and dc voltages, currents, and power from the benchmark.

Table 2.5 Numerical results of the three-phase diode rectifier benchmark using Simulink

Parameters	AC Values at 60Hz on Bus 3		
	Phase A	Phase B	Phase C
V_D^p (V)	$106.1004\angle -10.79^o$	$103.5642\angle -132.61^o$	$102.6879\angle 106.17^o$
I_D^p (A)	$17.8382\angle -24.53^o$	$18.2050\angle -145.92^o$	$17.6458\angle 93.74^o$
S_D^p (VA)	1838.5146+j449.3539	1834.7559+j434.0173	1769.7272+j390.1061
	DC Values on Bus 4		
$V_{D,dc}$ (V)	231.8597		
$I_{D,dc}^{3\phi}$ (A)	23.1860		
$P_{D,dc}^{3\phi}$ (W)	5387.1708		

The total real power entering the diode rectifier is 5443 Watt and the loss is 1.03%.

2.4.2.2 Evaluating the Delta-Connected Diode Rectifier Model

The evaluation of the diode rectifier model follows the same procedure as that of the thyristor converter model. The three-phase diode rectifier was studied in steady-state using the delta-connected model. It is assumed that the ac voltages and dc voltage applied on the model are equal to those in time domain analysis. The converter loss percentage is equal to the benchmark.

First, the coefficients, $\lambda_{D,I}^{LL}$, $\lambda_{D,P}^{LL}$, K_D^{LL}, in the delta-connected models were calculated and provided in Table 2.6. Since the dc voltage in the model is equal to that

obtained from Simulink, the calculated dc current and dc power are equal to those obtained from Simulink. Using the model, the ac currents, I_D^p , and power, S_D^p, entering the three-phase diode rectifier were calculated. The results are shown in Table 2.7. For comparison, the steady-state analysis results on the Y-connected model are also provided in Table 2.7. I_D^p and S_D^p are compared with those obtained from the benchmark with the difference in percentage with respect to the benchmark.

Table 2.6 Current participation coefficients, $\lambda_{D,I}^{LL}$, power participation coefficients, $\lambda_{D,P}^{LL}$, and equivalence coefficients, K_D^{LL}, in the 1-phase diode rectifiers

Parameters	Line AB	Line BC	Line CA
$\lambda_{D,I}^{LL}$	0.3447	0.3359	0.3195
$\lambda_{D,P}^{LL}$	0.3484	0.3372	0.3144
K_D^{LL}	1.3330	1.3354	1.3394

Table 2.7 The ac currents, I_D^p, and ac power, S_D^p in the three-phase diode rectifier using the Δ-connected model in steady-state analysis

Parameters	Δ-Connected Model	$\Delta\left\|I_D^p\right\|$ (%)	Y-Connected Model	$\Delta\left\|I_D^p\right\|$ (%)
I_D^a (A)	$17.7960\angle$-24.71^o	0.2365	$17.4887\angle$- 30.17^o	1.9594
I_D^b (A)	$18.0898\angle$-145.40^o	0.6329	$17.1369\angle$-148.08^o	**5.8670**
I_D^c (A)	$17.7570\angle 94.12^o$	0.6303	$16.8989\angle 93.47^o$	4.2330
	Δ-Connected Model	$\Delta\left\|S_D^p\right\|$ (%)	Y-Connected Model	$\Delta\left\|S_D^p\right\|$ (%)
S_D^a (VA)	1859.8136+j526.5384	0.2361	1814.3+j424.33	1.5197

S_D^b (VA)	1835.6097+j549.9678	**0.6332**	1814.3+j424.33	1.1332
S_D^c (VA)	1747.5704+j465.924	0.6191	1814.3+j424.33	2.8049

Remarks:

- $\lambda_{D,I}^{LL}$, $\lambda_{D,P}^{LL}$, K_D^{LL} displayed similar characteristics as those in the thyristor converter model.
- In Table 2.7, I_D^p and S_D^p obtained from the delta-connected model are close to those obtained in the benchmark. The maximal error is 0.6332%. The sources of the errors are the assumptions on the dc current and converter loss.
- Again, the delta-connected modeling approach provided more accurate results than the Y-connected modeling approach.

2.4.3 Three-Phase PWM Inverter Benchmark and Evaluation of the Delta-Connected Model

A three-phase PWM inverter was used as the benchmark to evaluate the delta-connected PWM converter model. The inverter was embedded in a 4-bus unbalanced ac/dc system with the circuit diagram shown in Figure 2.17.

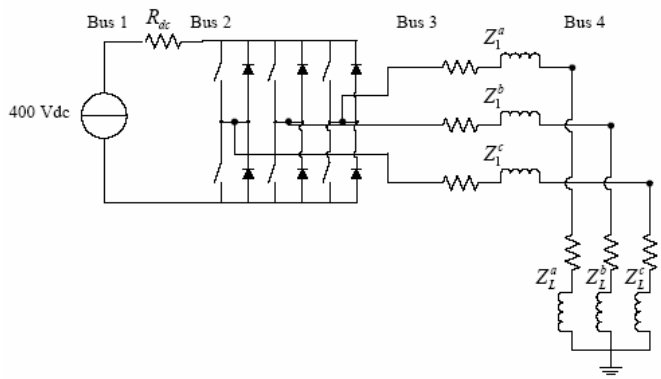


Figure 2.17 The circuit diagram of a 4-bus unbalanced ac/dc system with a three-phase PWM inverter

In Figure 2.17, a 400 V_{dc} source feeds dc power to a three-phase PWM inverter through a dc line. The inverter's output line-to-line voltages are regulated at balanced 208 V_{LL} and supply a three-phase, unbalanced, constant impedance load on Bus 4 through a three-phase unbalanced distribution line. The three phases of the line are decoupled and parameters are scaled down from actual distribution lines. The parameters of the system components are shown in Table 2.8.

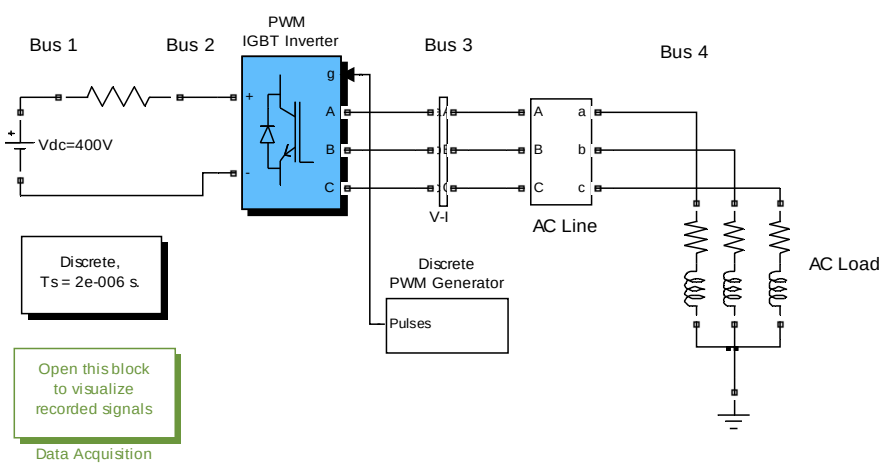
Table 2.8 Component parameters of the 4-bus ac/dc system with a three-phase PWM inverter

Parameters	Values
Source voltage	400 V_{dc}
Line impedance	$Z_1^a = 0.1410 + j0.4400 \ \Omega$ $Z_1^b = 0.1370 + j0.4420 \ \Omega$ $Z_1^c = 0.1210 + j0.4460 \ \Omega$

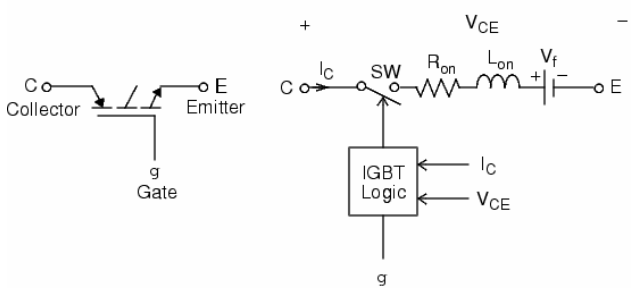
AC load impedance	$Z_L^a = 10 + j4.5 \quad \Omega$ $Z_L^a = 9 + j4\ \Omega$ $Z_L^c = 7 + j3.2 \quad \Omega$
DC line	$R_{dc} = 1 \quad \Omega$
Inverter snubber resistance	5000 Ω
Inverter forward voltage	0 V
Modulation ratio	0.883

2.4.3.1 Simulation Results of the PWM Inverter Benchmark

The benchmark was built in Simulink using the SimPowerSystems Toolbox with the circuit shown in Figure 2.19.a. The IGBT model in the three-phase, PWM converter is shown in Figure 2.19.b. The IGBT is simulated as a series combination of a resistor R_{on}, inductor L_{on}, and a DC voltage source V_f in series with a switch controlled by a logical signal (g > 0 or g = 0.



(b) The 4-bus unbalanced AC/DC system diagram



(b) The detailed IGBT model in MATLAB Simulink

Figure 2.18 The Simulink circuits of the 4-bus unbalanced ac/dc system with a three-phase IGBT PWM inverter

Each simulation has been run for 0.05 seconds with a step size of 2 uS. The waveforms of the ac voltages and currents on the PWM inverter were captured and are shown in Figure 2.19. The following parameters were calculated using the measurement blocks from the SimPowerSystems Toolbox and provided in Table 2.9.

- The ac line-to-neutral voltages on the PWM inverter ac bus, V_{PWM}^{p}
- The ac phase currents leaving the PWM inverter, I_{PWM}^{p}
- The complex ac power leaving the PWM inverter, S_{PWM}^{p}
- The average dc voltage, current, and power of the PWM inverter, $V_{PWM,dc}$, $I_{PWM,dc}^{3\phi}$, $P_{PWM,dc}^{3\phi}$, respectively

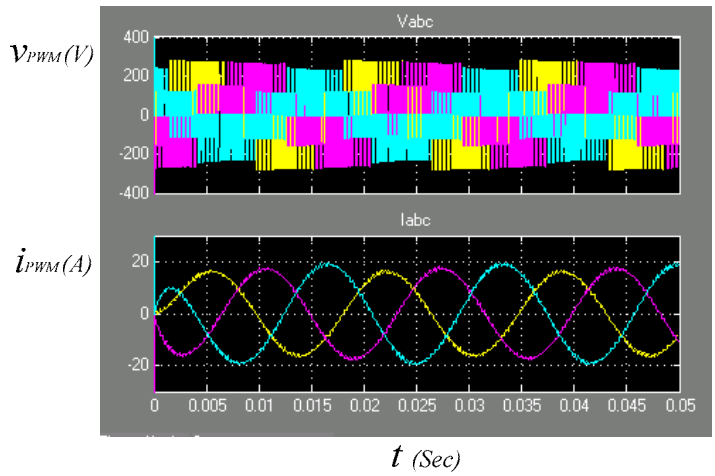


Figure 2.19 Line-to-neutral voltages (top) and ac currents (bottom) in the three-phase PWM inverter benchmark

Table 2.9 Numerical results of the three-phase PWM inverter benchmark using Simulink

Parameters	AC Values at 60Hz on Bus 3		
	Phase A	Phase B	Phase C
V_{PWM}^{p} (V)	$129.0121\angle\text{-}3.934^{o}$	$124.5795\angle\text{-}114.67^{o}$	$107.9349\angle 118.95^{o}$
I_{PWM}^{p} (A)	$11.4374\angle\text{-}29.93^{o}$	$12.2624\angle\text{-}140.59^{o}$	$13.4968\angle 91.86^{o}$
S_{PWM}^{p} (VA)	1326.3773+j646.558	1373.8864+j667.9173	1296.8449+j663.6267
	DC Values on Bus 2		
$V_{PWM,dc}$ (V)	389.3541		
$I_{PWM,dc}^{3\phi}$ (A)	10.6459		
$P_{PWM,dc}^{3\phi}$ (W)	4145.0378		

Remarks:

- The three-phase current leaving the PWM inverter is unbalanced due to the unbalanced line and load. As a consequence, the phase voltage is unbalanced.
- The real power loss is $\left(1-\sum_{p\in\{a,b,c\}} P_{PWM}^{p} \Big/ P_{PWM,dc}^{3\phi}\right)\cdot 100\% = 3.57\%$

2.4.3.2 Evaluating the Delta-Connected PWM Converter Model

In order to evaluate the delta-connected model, the three-phase PWM inverter was modeled using three, delta-connected, single-phase PWM converters for steady-state analysis. The PWM inverter output line-to-line ac voltages were calculated using the modulation ratio and the dc voltage in the benchmark. Then, the ac currents, I_{PWM}^{LL}, and complex power, S_{PWM}^{LL}, in the model were calculated by applying the calculated ac voltages to the ac system. It is assumed the loss percentage of the model is equal to that of the benchmark. Then, the average dc currents, $I_{PWM,dc}^{LL}$ and power, $P_{PWM,dc}^{LL}$ in the single-phase PWM inverters were also calculated using (2.44) and (2.45).

Using the equivalent model, the ac and dc voltages, currents, and power in the three-phase PWM inverter are calculated using (2.42), (2.46) and (2.47). They are compared with those obtained in the benchmark using Simulink. The results are shown in Table 2.10 with the errors in percentage with respect to the benchmark.

Table 2.10 Comparison of the benchmark and the three-phase PWM inverter using the delta-connected model in steady-state analysis

Parameters	AC Values at 60Hz on Bus 3		
	Benchmark	Δ-Connected Model	$\Delta\left\|I_T^p\right\|$ (%)
I_T^a (A)	$11.4374\angle\text{-}29.93^o$	$11.4762\angle\text{-}29.80^o$	0.3390
I_T^b (A)	$12.2624\angle\text{-}140.59^o$	$12.3043\angle\text{-}140.52^o$	0.3421
I_T^c (A)	$13.4968\angle 91.85^o$	$13.5357\angle 91.95^o$	0.2885
	Benchmark	Δ-Connected Model	$\Delta\left\|S_T^p\right\|$ (%)

S_T^a (VA)	1326.3773+j646.558	1332.2296+j645.9408	0.3384
S_T^b (VA)	1373.8864+j667.9173	1379.5136+j668.3047	**0.3425**
S_T^c (VA)	1296.8449+j663.6267	1301.6988+j668.3047	0.2883
	DC Values on Bus 2		
	Benchmark	Δ-Connected Model	Error (%)
$I_{PWM,dc}^{3\phi}$ (A)	10.6459	10.6895	**0.4095**
$P_{PWM,dc}^{3\phi}$ (W)	4145.0378	4151.9994	0.4092

Remarks:

- The maximal error of the ac parameters is 0.3425%. It is mainly attributed to the line-to-line ac voltages, which are assumed to be balanced in steady-state analysis.
- The maximal error of the dc parameters is 0.4095%. It is larger than the error in the ac parameters. It is mainly attributed to the assumption of the balanced loss in the single-phase PWM converters. For balanced systems, this should not introduce errors.

2.5 Comments

In this chapter, unbalanced converter models were proposed for distribution system steady-state analysis, such as power flow studies. The modeling approach used three, single-phase, delta-connected converters to model three-phase converters. It can capture the imbalance of the network and is applicable to converters operating in both the

continuous and discontinuous conduction modes under significantly unbalanced operating conditions.

The modeling approach has been applied to three types of converters: three-phase full-bridge diode rectifiers, full-bridge thyristor converters (rectifier and inverter), and PWM converters (rectifier and inverter) respectively. For the diode and thyristor converter models, equivalence coefficients are introduced to provide an equivalent transformation between the model and the three-phase converter with respect to both the RMS fundamental ac and the average dc currents in the three-phase converter.

Time domain simulations have been performed to test three-phase converters in unbalanced ac/dc systems. The simulation results were used to verify the delta-connected models in steady-state. It is shown that the models provided accurate estimation of the unbalanced ac currents and power in three-phase converters.

The models can be applied to study ac/dc power flow in distribution systems. With the appropriate converter models, ac/dc power flow solvers can be developed to study unbalanced distribution systems. In the following chapters, three-phase sequential and unified ac/dc power flow solvers are proposed respectively.

CHAPTER 3. THREE-PHASE SEQUENTIAL DISTRIBUTION AC/DC POWER FLOW

In this chapter, a three-phase sequential power flow solver is proposed incorporating the converter models developed in Chapter 2. The power flow equations are solved successively between ac systems and dc systems. For illustration, an ac/dc system is shown in Figure 2.1 with two ac/dc converters. In this thesis, while solving ac power flow, the dc system is represented as equivalent delta-connected ac components on the converter ac buses. While solving dc power flow, the ac systems are represented as equivalent dc components on the converter dc buses.

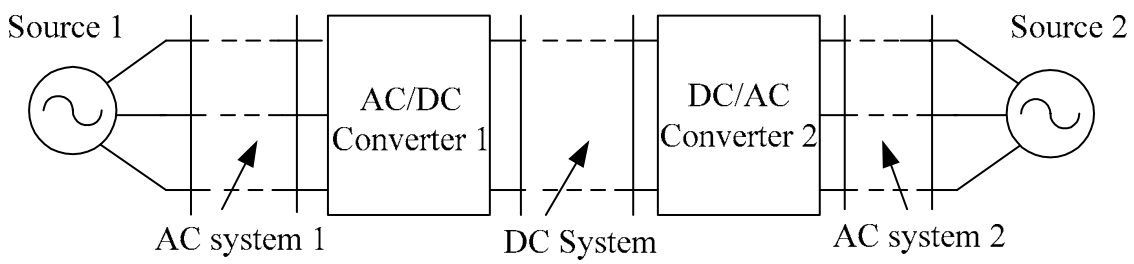


Figure 3.1 A sample ac/dc system

Sequential power flow solvers were first developed in the 1970's [8] for HVDC system analysis. In the past three decades, various sequential solvers have been proposed for balanced [9], [25]-[28] and unbalanced [10]-[12] HVDC systems. Since HVDC systems are typically balanced, power flow equations were established using single-phase component models. In unbalanced power flow solvers, three-phase converter models were proposed with constant dc currents. In the above solvers, the ac power flow was solved using either the Newton-Raphson method [9][10] or fast decoupled Newton

methods [27]. The dc power flow was solved using either the Gauss-Seidel method [26][27] or the Newton method [8][10][28].

The sequential solvers for HVDC system analysis are not directly applicable to distribution power flow studies. Distribution systems are unbalanced with single-phase, two-phase, and three-phase network branches and loads. Additionally, distribution system converters often generate voltages and currents with high harmonics because of inadequate filtering devices. As such, a three-phase solver is developed in this chapter with unbalanced component models. The delta-connected converter models capture the impacts of the distorted voltages and currents in power flow. Some features of the sequential solver include:

- Integration of unbalanced converter models into existing three-phase ac and dc power flow solvers, capturing system's imbalance;
- Consideration of different converter control schemes and operating conditions;
- Applications for uni-directional and bi-directional power flow studies in distribution systems with radial or weakly meshed structures.

This chapter is organized as follows. First, power flow component models are proposed. Then, the power flow problem formulation is developed using these models. A three-phase sequential solver using the implicit Z-bus Gauss method is proposed and tested in MATLAB simulations. The results are obtained and presented.

3.1 Three-Phase Power Flow Component Models

In order to develop three-phase ac/dc power flow solvers, appropriate ac and dc component models are desired. In this thesis, three-phase models from [29] are used for ac transformers, distribution lines, switches, and loads. For dc components, distribution lines and switches are modeled using pure resistances. DC loads are treated as constant resistance (Z), constant current (I), and constant real power load (P), or linear combination ZIP loads. The dc inductance and capacitance in the dc filters are considered in the converter models.

The ac and dc systems are interconnected with various types of converters. Since the ac and dc power flow are solved separately in the sequential solver, equivalent power flow components have been developed to decouple the ac and dc systems. Depending on the converter's types, various equivalent components are built using the unbalanced delta-connected converter models. In the ac systems, the dc systems are modeled as delta-connected ac loads for rectifiers and sources for inverters on the converter ac buses. In the dc systems, the ac systems are modeled as dc sources for rectifiers and loads for inverters on the converter dc buses. The parameters of the equivalent ac and dc components depend on the converter models and the previous power flow solutions. For example, Figure 3.2 shows the decoupled ac and dc systems for one operation scheme of the sample system in Figure 3.1. Details are presented next for the equivalent ac and dc power flow components.

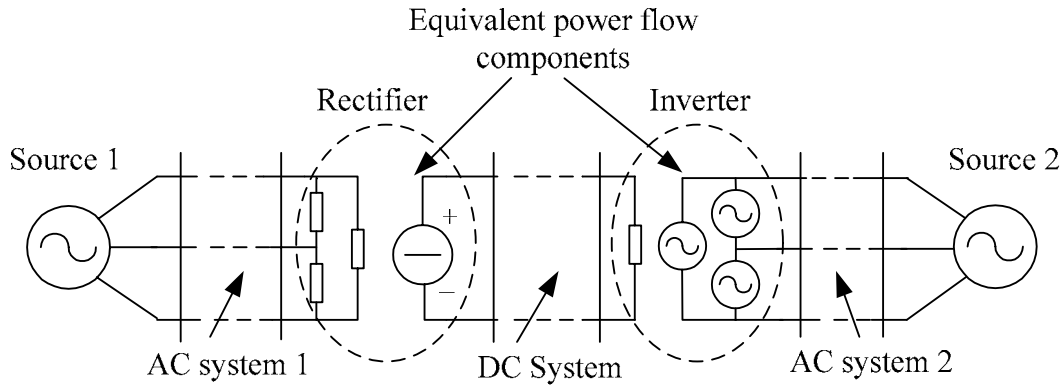


Figure 3.2 Decoupled ac and dc systems used in the sequential power flow solver

3.1.1 Equivalencing the DC Systems to AC Power Flow Components

On the converter ac buses, the dc systems can be modeled as different delta-connected components, depending on the converter type and operating mode. A summary of the equivalent power flow components are provided in Table 3.1 with the equivalent single-phase ac circuits and the following notation.

superscript^{LL} *ab*, *bc*, or *ca*

subscript$_{D,\,T,\,PWM}$ diode rectifiers, thyristor converters, and PWM converters respectively

subscript$_{Conv}$ *D*, *T*, or *PWM*

CCCL/ CCCS: the current controlled current load/source

$\beta_{Conv,I}^{LL}$ the coefficients between converter ac and dc currents

I_{Conv}^{LL} the RMS fundamental ac currents in the delta-connected model

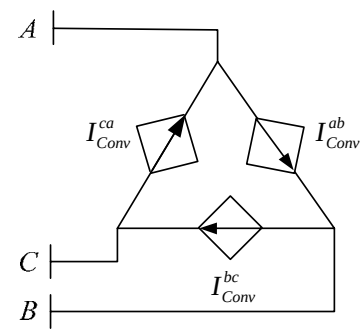
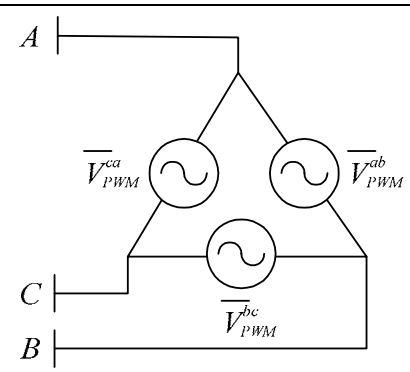
$I_{Conv,dc}^{3\phi}$ the average dc link current

V_{Conv}^{LL} the RMS fundamental line-to-line converter voltages

Note: CCCL and CCCS have the same equivalent ac component but opposite signs for

the ac currents.

Table 3.1 Equivalent power flow components for the DC systems

Converter Types	Converter Control Schemes on the AC Side	Equivalent 3-Phase AC Components
Diode Rectifier	None	 CCCL - $I_{Conv}^{LL} = \beta_{Conv,I}^{LL} \cdot I_{Conv,dc}^{3\phi}$
Thyristor Converter	Rectifier – None	The same as CCCL
	Inverter – None	CCCS
PWM Converter	AC current control with unity power factor	The same as CCCL
	AC voltage control	 Voltage Source

If a dc system is interconnected with an ac system using a thyristor converter or a diode rectifier, it can be made equivalent to a three-phase, delta-connected, current controlled current load (source) for a rectifier (inverter). The magnitudes of the ac currents and the ac real power in the equivalent component are determined by the

converter models from Chapter 2 and are dependent on the dc current and the dc power respectively. (3.1), (3.2) present the ac current and real power in terms of the average dc current and average dc power in the thyristor converter model:

$$\left|I_T^{LL}\right| = \left(\frac{K_T^{LL}}{K_{T,dc}}\lambda_{T,I}^{LL}\right)\cdot I_{T,dc}^{3\phi} \tag{3.1}$$

$$P_T^{LL} = \left(\lambda_{T,P}^{LL}\cdot C_T^{loss}\right)\cdot P_{T,dc} \tag{3.2}$$

where:

K_T^{LL}, $K_{T,dc}$: the ac and dc equivalence coefficients in the model respectively

$\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$: the current and power participation coefficients of each single-phase converter in the model respectively

P_T^{LL}, $P_{T,dc}$: the ac real power in the single-phase converters and the average dc link power respectively

When a dc system is interconnected with an ac system using a current controlled PWM converter, the dc system can also be modeled as a three-phase, delta-connected, current controlled current component. The parameters of the equivalent component are determined by the delta-connected PWM converter model. In the model, the three-phase real power entering the single-phase PWM converters is balanced and the reactive power is equal to zero. In addition, the ac real power is equal to the dc power in the converter multiplied by a loss factor, C_{PWM}^{loss}:

$$I_{PWM}^{LL} = \frac{P_{PWM}^{LL}}{\left(V_{PWM}^{LL}\right)^*} = \frac{V_{PWM,dc}\cdot C_{PWM}^{loss}}{3\cdot\left(V_{PWM}^{LL}\right)^*} I_{PWM,dc} = \beta_{PWM,I}^{LL}\cdot I_{PWM,dc} \tag{3.3}$$

If the PWM converter is operated using the ac voltage control, the inverter's output

ac voltage is typically regulated. As such, the dc system can be modeled as a three-phase, delta-connected, voltage source with specified voltage magnitudes and angles on the converter ac bus:

$$V_{PWM}^{LL} = \overline{V}_{PWM}^{LL} \tag{3.4}$$

Next, the ac systems are made equivalent to dc power flow components for dc power flow calculations.

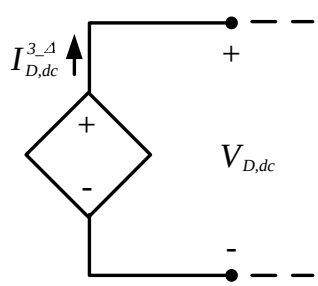
3.1.2 Equivalencing the AC Systems to DC Power Flow Components

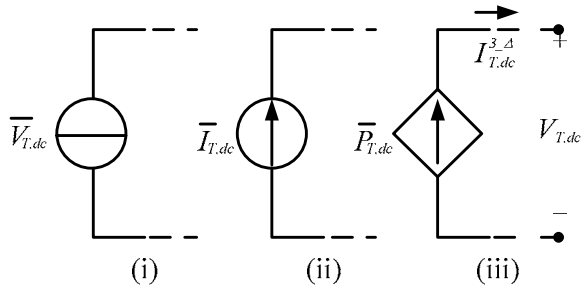
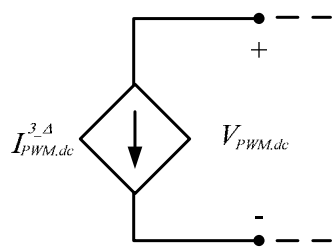
On the converter dc buses, the ac systems are modeled as different equivalent sources or loads, according to the converter's control schemes. A summary of the equivalent power flow components are provided in Table 3.2 with the following notation:

VCVS/VCVL the voltage controlled voltage source/load

VCCS/VCCL the voltage controlled current source/load

Table 3.2 Equivalent dc power flow components for the AC systems

Converter Types	Converter Control Schemes on the DC Side	Equivalent DC Components
Diode Rectifier	None	 VCVS

Thyristor Converter	(i) Constant dc voltage (ii) Constant dc current (iii) Constant dc power (iv) Constant firing angles	 (i) Constant voltage source/load (ii) Constant current source/load (iii) VCCS/VCCL (iv) VCVS/VCVL
PWM Converter	AC current control	Constant voltage source/load
	AC voltage control	 CCCS/CCCL

For an uncontrollable diode rectifier, the average dc voltage, $V_{D,dc}$, is the sum of the integration of the dc voltages on the single-phase diode rectifier:

$$V_{D,dc} = \frac{1}{\pi} \sum_{LL \in \{ab,bc,ca\}} \int_{\theta_1^{LL}}^{\theta_2^{LL}} v_{D,dc}^{LL}(t) \cdot dt \tag{3.5}$$

where:

θ_1^{LL}, θ_2^{LL}: the conduction angles of the single-phase converters

Substituting (2.7) into (3.5), $V_{D,dc}$ can be expressed in term of the line-to-line complex voltage, V_D^{ab}, V_D^{bc}.

$$V_{D,dc} = A_D^{ab} \cdot V_D^{ab} + A_D^{bc} \cdot V_D^{bc} + A_D^{ca} \cdot \left(-V_D^{ab} - V_D^{bc}\right) \tag{3.6}$$

where: $A_D^{LL} = \frac{e^{-j\delta_{V_D}^{LL}}}{\pi} \int_{\theta_1^{LL}}^{\theta_2^{LL}} v_{D,dc}^{LL}(t) \cdot dt$

Thus, the ac system can be modeled as a voltage controlled voltage source on the diode rectifier dc bus.

For a thyristor converter, four control schemes are typically used to obtain- (i) constant dc voltage; (ii) constant dc current; (iii) constant dc power; and (iv) minimal reactive power using constant firing angles. Thus, the following equivalent models can be used to represent the ac system in the dc system respectively:

(i) A constant voltage component

$$V_{T,dc} = \overline{V}_{T,dc} \tag{3.7}$$

(ii) A constant current component

$$I_{T,dc}^{3\phi} = \overline{I}_{T,dc} \tag{3.8}$$

(iii) A voltage controlled current component

$$I_{T,dc}^{3\phi} = \frac{\overline{P}_{T,dc}}{V_{T,dc}} \tag{3.9}$$

(iv) A voltage controlled voltage component similar to the diode rectifier

$$V_{T,dc} = \frac{1}{\pi} \sum_{LL \in \{ab,bc,ca\}} \int_{\theta_1^{LL}}^{\theta_2^{LL}} v_{T,dc}^{LL}(t) \cdot dt \tag{3.10}$$

$$= A_T^{ab} \cdot V_T^{ab} + A_T^{bc} \cdot V_T^{bc} + A_T^{ca} \cdot \left(-V_T^{ab} - V_T^{bc}\right)$$

where:

$\overline{V}_{T,dc}$, $\overline{I}_{T,dc}$, $\overline{P}_{T,dc}$: the constant dc voltage, current, and power respectively

$A_T^{LL} = \frac{e^{-j\delta_{V_T}^{LL}}}{\pi} \int_{\theta_1^{LL}}^{\theta_2^{LL}} v_{T,dc}^{LL}(t) \cdot dt$

The current controlled PWM converter's dc voltage is maintained at a constant value by the dc capacitor. As such, the ac system can be represented as a constant voltage source (rectifier) or load (inverters) on the converter dc bus:

$$V_{PWM,dc} = \overline{V}_{PWM,dc} \tag{3.11}$$

For a voltage controlled PWM converter, the dc voltage may vary with the ac loads. Using the real power relationship in the PWM converter model, the ac system can be modeled as a current controlled current source (rectifier) or load (inverter) on the converter dc bus. Please note in (3.12) that the conjugate of the ac power, $\left(S_{PWM}^{LL}\right)^*$, entering the single-phase converters is deliberately selected to represent $I_{PWM,dc}^{3\phi}$ in terms of I_{PWM}^{LL} instead of $\left(I_{PWM}^{LL}\right)^*$:

$$\begin{aligned} I_{PWM,dc}^{3\phi} &= \frac{P_{PWM,dc}}{V_{PWM,dc}} = \frac{\sum_{LL} real\left(\left(S_{PWM}^{LL}\right)^*\right)}{V_{PWM,dc} \cdot C_{PWM}^{loss}} = \frac{\sum_{LL} real\left(\left(V_{PWM}^{LL}\right)^* \cdot I_{PWM}^{LL}\right)}{V_{PWM,dc} \cdot C_{PWM}^{loss}} \\ &= \sum_{LL} \beta_{PWM,dc}^{LL} \cdot I_{PWM}^{LL} \end{aligned} \tag{3.12}$$

where:

$\beta_{PWM,dc}^{LL}$: the coefficients between the dc current and the ac currents in the PWM converter model

Now, the power flow formulation is presented for the sequential solver using the above component models.

3.2 AC/DC Power Flow Formulation

In this subsection, steady-state nodal analysis equations are established on both ac buses and dc buses for the sequential power flow solver. On each phase of an ac bus, there are four parameters – the voltage magnitude and angle, and the injected real power and reactive power. With two parameters known, the other two can be determined. On each dc bus, there are two parameters – the voltage and the real power. With one parameter known, the other one can be determined.

A list of parameters is provided in Table 3.3 with the following notation. AC quantities are vectors sized according to the number of existing phases at the bus. DC quantities are scalars.

subscript$_{sub,\ ac,\ dc}$: the substation, ac buses, and dc buses respectively

subscript$_{D,T,PWM}$: diode rectifiers, thyristor converters, and PWM converters

$|V|$, δ_V : voltage magnitudes and angles respectively

P, Q : real and reactive power injections respectively

$|I|$: current magnitudes

Next, the ac/dc power flow formulation will be presented.

Table 3.3 A list of known and unknown parameters in AC/DC power systems

AC Buses	Bus Types	Known Parameters	Unknown Parameters
Generation - Substation	*Slack Bus*	$\lvert V_{sub}\rvert$, $\delta_{V_{sub}}$	P_{sub} , Q_{sub}
Generation	$P\lvert V\rvert$	P_{ac} , $\lvert V_{ac}\rvert$	Q_{ac}, $\delta_{V_{ac}}$
Load	PQ	P_{ac}, Q_{ac}	$\lvert V_{ac}\rvert$, $\delta_{V_{ac}}$
Diode Rectifier	$P\lvert I\rvert$	P_D , Q_D ($\lvert I_D\rvert$)	$\lvert V_D\rvert$, δ_{V_D}
Thyristor Converter	$P\lvert I\rvert$	P_T, Q_T ($\lvert I_T\rvert$)	$\lvert V_T\rvert$, δ_{V_T}

PWM Converter	*PQ*	P_{PWM} , Q_{PWM} (ac current control)	$\|V_{PWM}\|$, $\delta_{V_{PWM}}$
	(i) Slack	$\|V_{PWM}\|$, $\delta_{V_{PWM}}$ (ac voltage control)	P_{PWM} , Q_{PWM}
	(ii) P|V|	P_{PWM} , $\|V_{PWM}\|$ (ac voltage control)	$\delta_{V_{PWM}}$, Q_{PWM}
DC Buses	**Bus Types**	**Known Parameters**	**Unknown Parameters**
Generation	*V*	V_{dc}	P_{dc}
Load	*P*	P_{dc}	V_{dc}
Diode Rectifier	*V*	$V_{D,dc}$	$P_{D,dc}$
Thyristor Converter	*V*	$V_{T,dc}$ (dc voltage control)	$P_{T,dc}$
	P	$P_{T,dc}(I_{T,dc})$ (dc current control)	$V_{T,dc}$
		$P_{T,dc}$ (dc power control)	$V_{T,dc}$
PWM Converter	*V*	$V_{PWM,dc}$ (ac current control)	$P_{PWM,dc}$
	P	$P_{PWM,dc}$ (ac voltage control)	$V_{PWM,dc}$

Note: For an ac voltage controlled PWM converter, the term “decoupled” means that the converter’s ac bus and the substation are not in the same ac subsystem. The term “coupled” means that the ac bus and the substation are in the same ac subsystem.

(i) The converter’s ac bus is treated as a slack bus if the ac bus and the substation are decoupled.

(ii) The converter’s ac bus is treated as a P|V| bus if the ac bus and substation are coupled.

3.2.1 AC and DC System Nodal Analysis Equations

In this thesis, both the ac and dc power flow are formulated using nodal analysis. Complex ac voltages and dc voltages are chosen as state variables and solved using bus current injections. The constant impedance loads are added in the admittance matrix. The

constant currents loads are added in the current injection vector. The constant power loads are represented as voltage dependent current loads and added in the current injection vector. The voltage dependent current loads are updated at each iteration. General matrix forms of the ac and dc nodal analysis equations are given in (3.13) and (3.14) respectively:

$$\begin{bmatrix} Y_{sub} & Y_{sub,ac} & 0 \\ \left[Y_{sub,ac}\right]^T & Y_{ac} & Y_{ac,Conv} \\ 0 & \left[Y_{ac,Conv}\right]^T & Y_{Conv} \end{bmatrix} \begin{bmatrix} V_{sub} \\ V_{ac} \\ V_{Conv} \end{bmatrix} = \begin{bmatrix} I_{sub,L}(V) \\ I_{ac,L}(V) \\ I_{Conv,L}(V) + B_{Conv,ac} I_{Conv}(V) \end{bmatrix} \tag{3.13}$$

$$\begin{bmatrix} G_{dc} & G_{dc,Conv} \\ \left[G_{dc,Conv}\right]^T & G_{Conv} \end{bmatrix} \begin{bmatrix} V_{dc} \\ V_{Conv,dc} \end{bmatrix} = \begin{bmatrix} I_{dc,L}(V) \\ I_{Conv,L_{dc}}(V) + I_{Conv,dc}(V) \end{bmatrix} \tag{3.14}$$

where:

$n_{ac} \in \mathbb{R}$: the number of ac buses, excluding the substation bus and converter ac buses

$n_{dc} \in \mathbb{R}$: the number of dc buses, excluding the converter dc buses

$n_{Conv} \in \mathbb{R}$: the number of converters

$V_{sub} \in \mathbb{C}^3$: the complex voltage vector of the substation bus

$V_{ac} \in \mathbb{C}^{3n_{ac}}$: the complex voltage vector of ac buses, excluding the substation and converter ac buses

$V_{Conv} \in \mathbb{C}^{3n_{Conv}}$: the complex voltage vector of converter ac buses

$V_{dc} \in \mathbb{R}^{n_{dc}}$: the voltage vector of dc buses, excluding converter dc buses

$V_{Conv,dc} \in \mathbb{R}^{n_{Conv}}$: the voltage vector of converter dc buses

$I_{sub,L}(V) \in \mathbb{C}^3$: the complex load current injection vector of the substation bus

$I_{ac,L}(V) \in \mathbb{C}^{3n_{ac}}$: the complex load current injection vector of ac buses, excluding the substation and converter ac buses

$I_{Conv}(V) \in \mathbb{C}^{3n_{Conv}}$: the complex current injection vector of converter ac buses from the converter model

$B_{Conv,ac} \in \mathbb{R}^{3\times 3}$: the transformation matrix converting delta-connected currents in the converter model into the currents in three-phase converters

$I_{Conv,L}(V) \in \mathbb{C}^{3n_{Conv}}$: the complex load current injection vector of converter ac buses

$I_{dc,L}(V) \in \mathbb{R}^{n_{dc}}$: the load current injection vector of dc buses, excluding the substation and converter dc buses

$I_{Conv,L_{dc}}(V) \in \mathbb{R}^{n_{Conv}}$: the load current injection vector of converter dc buses

$I_{Conv,dc}(V) \in \mathbb{R}^{n_{Conv}}$: the current injection vector of converter dc currents

$Y_{sub} \in \mathbb{C}^{3\times 3}$, $Y_{sub,ac} \in \mathbb{C}^{3\times 3n_{ac}}$, $Y_{ac} \in \mathbb{C}^{3n_{ac}\times 3n_{ac}}$, $Y_{Conv} \in \mathbb{C}^{3n_{Conv}\times 3n_{Conv}}$, $Y_{ac,Conv} \in \mathbb{C}^{3n_{ac}\times 3n_{Conv}}$:

the admittance matrices on the ac buses

$G_{dc} \in \mathbb{R}^{n_{dc}\times n_{dc}}$, $G_{Conv} \in \mathbb{R}^{n_{Conv}\times n_{Conv}}$, $G_{dc,Conv} \in \mathbb{R}^{n_{dc}\times n_{Conv}}$:

the conductance matrices on the dc buses

Three-phase ac power flow and dc power flow are solved separately by decoupling the ac and dc systems at the converter buses. While solving for the ac state variables, the dc power flow is treated to be constant and the dc systems are modeled as delta-connected current injections on the converter ac buses in (3.13). The equivalent currents are calculated using the converter models from Chapter 2 and the dc power flow calculated in the present ac/dc iteration. Since the contributions of the dc systems are

already included in the current vector, the ac nodal admittance matrix can be established by neglecting the converters and the dc systems.

While solving for the dc state variables, the ac power flow is treated to be constant. The ac systems are modeled as dc current injections on the converter dc buses in (3.14). The equivalent currents are calculated using the converter models and the ac power flow calculated in the present ac/dc iteration. Again, the conductance matrix can be established by neglecting the ac systems. Details are presented next to present on how to integrate different types of converters in the steady-state nodal analysis equations.

3.2.2 Converter AC Bus Equations

On the converter ac buses, the nodal analysis equations are modified to include the contributions of the dc systems to the ac power flow according to the converter type. The following two types of converters are considered:

A. Thyristor converters and diode rectifiers

B. PWM converters

3.2.2.1 Thyristor Converters and Diode Rectifiers

The treatment of thyristor converters in ac systems and the related ac equations are described here. The treatment of diode rectifiers follows in the same approach. In (3.13), a thyristor converter ac bus is treated as a P|I| bus. The dc system is modeled as a three-phase, delta-connected P|I| component. The real power, P_T^{LL}, and the current magnitudes, $\left|I_T^{LL}\right|$, are calculated in (3.1) and (3.2). They are updated when the dc power flow is updated.

The phase current injections from three-phase thyristor converters, I_T, in (3.13) can

be represented using the ac currents in the delta-connected model:

$$I_T = \begin{bmatrix} -I_T^a \\ -I_T^b \\ -I_T^c \end{bmatrix} = B_{T,ac} \cdot \begin{bmatrix} I_T^{ab} \\ I_T^{bc} \\ I_T^{ca} \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} I_T^{ab} \\ I_T^{bc} \\ I_T^{ca} \end{bmatrix} \tag{3.15}$$

The current angles, $\delta_{I_T}^{LL}$, are calculated in (3.16) using the converter ac voltages from previous ac power flow iteration. The angles are updated at each ac iteration:

$$\delta_{I_T}^{LL} = \delta_{V_T}^{LL} - \cos^{-1}\left(\frac{P_T^{LL}}{\left|V_T^{LL}\right| \cdot \left|I_T^{LL}\right|} \right) \tag{3.16}$$

3.2.2.2 PWM Converters

The treatment of PWM converters in ac systems depends on their control schemes and the connection with the substation. The following cases are considered here:

- AC current controlled converter
- AC voltage controlled converter with the ac bus (i) decoupled; (ii) coupled with the substation

As a consequence, the related ac equations are different.

- **AC Current Controlled Converter**

For a current controlled PWM converter, the converter's ac bus is treated as a PQ bus in (3.13). The dc system is modeled as a three-phase, delta-connected, voltage dependent current component. The component currents are calculated in (3.3) using the converter ac voltages from the previous ac/dc power flow iteration and the real power from the dc power flow. They are transformed to phase currents and added in the current injection vector.

- **AC Voltage Controlled Converter**

For a voltage controlled PWM converter, the converter's ac bus is treated as a constant voltage bus in (3.13). The dc system is modeled as a three-phase, delta-connected component with constant voltages in the ac system. The magnitudes of the line-to-line voltages and the difference of the voltage angles are specified:

$$\left|V_{PWM}^{LL}\right| = \left|\overline{V}_{PWM}^{LL}\right|, \quad \delta_{V_{PWM}}^{ab} - \delta_{V_{PWM}}^{bc} = \overline{\Delta\delta}_{V_{PWM}}^{ab\_bc}, \quad \delta_{V_{PWM}}^{bc} - \delta_{V_{PWM}}^{ca} = \overline{\Delta\delta}_{V_{PWM}}^{bc\_ca} \tag{3.17}$$

where:

$\left|\overline{V}_{PWM}^{LL}\right|$: the specified ac voltage magnitudes on the PWM converter

$\delta_{V_{PWM}}^{LL}$: the phase angles of the converter line-to-line voltages

$\overline{\Delta\delta}_{V_{PWM}}^{ab\_bc}$, $\overline{\Delta\delta}_{V_{PWM}}^{bc\_ca}$: the difference of the line-to-line voltage angles

The actual voltage angles are determined by the connection of the converter with the substation. Two cases are considered as follows.

- Converter AC Bus Decoupled from the Substation

The PWM converter's ac bus is treated as a slack bus when the ac bus is decoupled from the substation. The voltage angle on phase *a* is chosen as the reference for all state variables on the inverter ac side and set to zero degree. $\delta_{V_{PWM}}^{ab}$ can be set to thirty degrees.

- Converter AC Bus Coupled with the Substation.

The PWM converter's ac bus is treated as a P|V| bus when the ac bus is coupled with the substation. In order to determine the voltage angles, it is assumed that the total ac real power, $\overline{P}_{PWM}^{3\phi}$, in the converter is given:

$$P_{PWM}^{ab} + P_{PWM}^{bc} + P_{PWM}^{ca} = \overline{P}_{PWM}^{3\phi} \tag{3.18}$$

Using (3.18) as a constraint, the voltage angles are calculated iteratively. Initially, $\delta^{ab}_{V_{PWM}}$ is set to thirty degrees with respect to the substation. The converter voltage angles are adjusted at each power flow iteration using the bisection method until the difference between the calculated three-phase real power and $\overline{P}^{3\phi}_{PWM}$ is within a tolerance range.

3.2.3 Converter DC Bus Equations

On the converter dc buses, the contributions of the ac systems to the dc power flow are represented using current injections in the nodal analysis equations. Depending on the converter's type and control scheme, the converter buses are treated differently in the dc nodal analysis equation (3.14). The following two types of converters are addressed:

A. Thyristor converters and diode rectifiers

B. PWM converters

3.2.3.1 Thyristor Converters and Diode Rectifiers

For a thyristor converter, the converter's dc bus is treated as (i) a voltage bus for the converters with the constant dc voltage or the minimal firing angles; (ii) a power bus for the converters with the constant dc current or dc power. The ac systems are modeled as:

- Constant voltage sources with specified voltages for the dc voltage control;
- Voltage controlled voltage components for the constant firing angle control. The dc voltage is updated when the ac power flow is updated;
- Constant current components for the dc current control;
- Voltage dependent current components with constant power for the dc power control. Each power flow iteration, the currents are updated.

For a diode rectifier, the dc bus is treated as a voltage bus. The dc voltage is calculated using the converter's ac voltages and is updated when the ac power flow is updated.

3.2.3.2 PWM Converters

The treatment of the dc bus of a PWM converter is dependent on the converter's control scheme. For an ac current controlled PWM converter, the dc bus is treated as a voltage bus in (3.14). The converter's dc voltage is sustained by the dc capacitor and is constant. The ac system is modeled as a constant dc voltage component. The current in the voltage component is determined by the dc power flow.

For an ac voltage controlled PWM converter, the dc bus is treated as a PQ bus in (3.14). The ac system is modeled as a voltage dependent current component. The current is calculated using the ac real power obtained in present ac/dc power flow iteration as follows:

$$I_{PWM,dc}^{3\phi} = \frac{\sum_{L\in\{ab,bc,ca\}} P_{PWM}^{LL}}{V_{PWM,dc} \cdot C_{PWM}^{loss}} \tag{3.19}$$

The ac real power is updated when the ac power flow is updated. By appropriately modeling the ac and dc subsystems in the nodal analysis equations, the ac power flow and dc power flow can be solved sequentially.

3.3 Solution Algorithm

In sequential power flow solvers, ac and dc voltages in subsystems are computed in a sequential manner. The convergence of the solvers is affected by the sequence of solving power flow. As such, a subsystem ranking method is developed to determine the sequence. The ac/dc power flow in both radial and weakly meshed systems can be solved using a backward/forward algorithm initiated by subsystem ranks.

3.3.1 Ranking Method

The ranking method assigns a rank, R_i, to each subsystem i in the network, $i \in \{1...N\}$, where N is the number of subsystems. The sequence for solving power flow can be determined using subsystem ranks. Power flow studies require all network, loads, and other static parameters. Thus, the operating modes and control schemes are known for all of the converters and can be used to determine the ranks.

The relationship between two adjacent subsystems is defined first according to the operating mode of the interconnecting converter. For two adjacent subsystems, $subsys_i$ and $subsys_j$, where $i \neq j$, $i, j \in \{1...N\}$, $subsys_i$ is called a parent subsystem of $subsys_j$ and $subsys_j$ is called a child subsystem of $subsys_i$ if

(i) $subsys_i$ is on the ac side of an interconnecting rectifier, or

(ii) $subsys_i$ is on the dc side of an interconnecting inverter.

In both cases, power is fed from $subsys_i$ to its child subsystem, $subsys_j$.

The ranking method assigns a subsystem one rank higher than its parent subsystems. All of the subsystems can be ranked using the following steps.

Step 1. For an *N*-subsystem network, select a main source. If there are multiple sources, any one of the sources can be chosen as the main source.

Step 2. Perform a breadth-first search from the main source. Determine all of the subsystems and the relationship among them according to the operating modes of the interconnecting converters. Initialize all subsystem ranks to -*N*.

Step 3. Determine the subsystem containing the main source, defined as $subsys_1$. Assign $R_1=1$.

Step 4. Determine all of the adjacent subsystems of $subsys_1$, defined as $adj\left(subsys_1\right)$.

For each $subsys_i$, $i \in adj(subsys_1)$,

Step 4.a. Assign $R_i=1-1=0$ if $subsys_i$ is a parent subsystem of $subsys_1$.

Step 4.b. Assign $R_i=1+1=2$ if $subsys_i$ is a child subsystem of $subsys_1$.

Step 4.c. Add these adjacent subsystems into an empty subsystem list, *subsysList.*

Step 5. For each $subsys_i$, $i \in subsysList$, determine $adj\left(subsys_i\right)$. For each $subsys_j$, $j \in adj\left(subsys_i\right)$,

Step 5.a. Assign $R_j = max(R_i - 1, R_j)$ if $subsys_j$ is a parent subsystem of $subsys_i$.

Step 5.b. Assign $R_j = max(R_i + 1, R_j)$ if $subsys_j$ is a child subsystem of $subsys_i$.

Step 5.c. Remove $subsys_i$ from *subsysList* and add $subsys_j$ in *subsysList.*

Step 6. Go to *Step 5* if *subsysList* is not empty. Otherwise, all of the subsystems are ranked. Sort the subsystems according to their ranks.

The subsystem ranks are determined in *Step 5.a* and *Step 5.b*. For radial systems or meshed systems with loops only existing in individual subsystems, there is only one path from $subsys_1$ to any subsystem. For meshed systems with loops among subsystems,

there may be multiple paths from $subsys_1$ to a subsystem. The final rank is equal to the highest rank assigned to this subsystem during the ranking process. As such, each subsystem will only have one rank after *Step 6*.

For example, Figure 3.3 shows an ac/dc system with five converters. There are two ac subsystems and three dc subsystems. The operating modes of the converters and the power flow directions are shown in the figure.

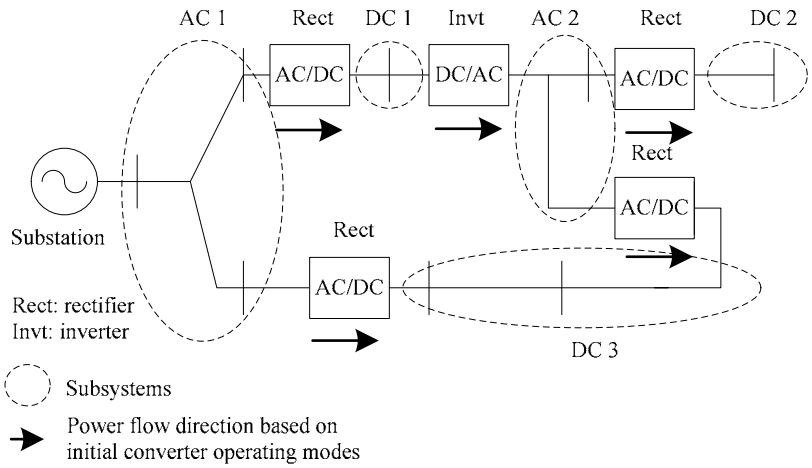


Figure 3.3 The one-line diagram of a sample ac/dc system with 5 subsystems

Each subsystem's rank is shown in Table 3.4. Subsystem AC 1 contains the substation and has $R_1 = 1$. It is noted that there are two paths from the substation to subsystem AC 2 with ranks 3 and 1. Thus, the final rank of AC2 is equal to $max(3,1)=3$.

Table 3.4. The ranks of the subsystems in the sample system

Rank	1	2	3	4
Subsystem #	AC 1	DC 1, DC3	AC 2	DC 2

A backward/forward algorithm is developed to solve ac/dc power flow in a sequential manner based on the subsystem ranks. The algorithm is discussed next.

3.3.2 Backward/Forward Algorithm

After the subsystems are ranked, a backward/forward iteration process is performed to solve ac/dc power flow. The solution algorithm is illustrated in Figure 3.4 and it includes:

- A backward sweep calculating unknown complex ac voltages and dc voltages from the highest ranked subsystems, R_{max}, to the lowest ranked subsystems, R_{min};
- A forward sweep calculating unknown complex ac voltages and dc voltages from the subsystems with R_{min} to the subsystems with R_{max}.

It is noted that subsystems might have different ranks if different sources are selected as the main source in multi-source networks. But the order of solving power flow in the backward and forward sweeps will be the same. For subsystems with the same rank, the computation order within each backward or forward sweep does not matter.

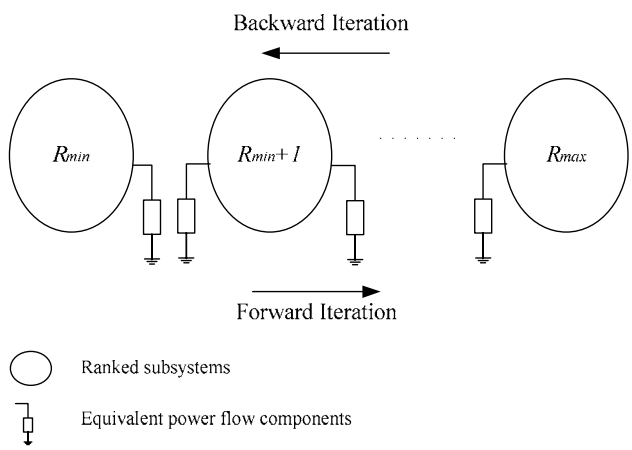


Figure 3.4 The backward/forward sequential ac/dc power flow

For each subsystem, adjacent subsystems are modeled as equivalent power flow components based on the delta-connected converter models. The parameters of the

equivalent components are calculated using the power flow obtained from the latest backward sweep or forward sweep.

The backward sweep is performed first and followed by a forward sweep. This is because the convergence of sequential solvers is sensitive to the initial states of each subsystem during the ac/dc iterations. Calculating power flow for subsystems with higher ranks first provides a good estimation of the equivalent power flow components.

The above backward/forward iteration process is performed repeatedly until the difference of the following parameters is within a tolerance range between two consecutive backward/forward sweeps:

- The unknown three-phase complex ac voltages and the dc voltages
- The participation coefficients and equivalence coefficients of the converter models

An implicit Z-bus Gauss method [23][24] is utilized to compute the ac and dc voltages in (3.13) and (3.14). In the ac nodal analysis equation (3.13), the voltages on the substation and on the ac voltage controlled PWM converters (e.g. inverter) are specified. In the dc nodal analysis equation (3.14), the specified dc voltages include the voltages on diode rectifiers, dc voltage controlled thyristor converters, and ac current controlled PWM converters (e.g. rectifier). The unknown voltages, V_2, are solved in an iterative manner using the specified voltages, V_1:

$$V_2^{(k)} = Y_{22}^{-1} \cdot \left[I_2^{(k-1)} \left(V_2^{(k-1)} \right) - Y_{21} \cdot V_1 \right] \tag{3.20}$$

where: k is the sweep number

Y_{22}, Y_{21}: the self and mutual nodal admittance sub-matrices on the buses with unknown voltages

$I_2(V_2)$: the vector of three-phase ac and dc currents injected into buses, which are functions of unknown voltages

The solution procedure of the sequential solver includes the following steps:

Step 1. Search and partition the network.

Step 1.a. Determine the operating modes of the converters. Divide the network into *ac* and *dc* subsystems at the converter buses.

Step 1.b. Rank the subsystems.

Step 2. Initialize all of the ac and dc voltages. Set the current rank R=R_{max} and sweep number k=1. Continue with a backward sweep.

Step 3. For all subsystems with rank R, compute the voltages in the subsystems.

Step 3.a. Compute the ac voltages for each ac subsystem with rank R

- Add the equivalent power flow components of the adjacent subsystems in the ac nodal analysis equation (3.13).
- Update the unknown ac voltages using (3.20). Calculate $\lambda_{Conv,I}^{LL}$, $\lambda_{Conv,P}^{LL}$, and K_{Conv}^{LL}, where $Conv \in \{D,T\}$, $LL \in \{ab,bc,ca\}$ in the interconnecting converter models.
- Determine the parameters of the equivalent power flow components of the present ac subsystem, based on the converter models. Go to Step 4.

Step 3.b. Compute the dc voltages for each dc subsystem with rank R

- Add the equivalent power flow components of the adjacent subsystems in the dc nodal analysis equation (3.14).

- Update the unknown dc voltages using (3.20). Calculate $\lambda_{Conv,I}^{LL}$, $\lambda_{Conv,P}^{LL}$, and K_{Conv}^{LL} in the interconnecting converter models.
- Determine the parameters of the equivalent power flow components of the present dc subsystem, based on the converter models. Go to Step 4.

Step 4. Select subsystems with a new rank

Step 4.a. For a backward sweep, set the current rank to *R=R-1*. If $R \geq R_{\min}$, go to *Step 3*. Otherwise, the backward sweep is complete. Go to *Step 5*.

Step 4.b. For a forward sweep, set the current rank to *R=R+1*. If $R \leq R_{\max}$, go to *Step 3*. Otherwise, the forward sweep is complete. Go to *Step 5*.

Step 5. Check for convergence of the ac/dc power flow

Step5.a. Calculate the following parameters between two consecutive sweeps, *k* and *k-1*, *i.e.*, a backward sweep and a forward sweep.

- The absolute value of the difference in the unknown complex voltages

$$\left|V_2^{(k)} - V_2^{(k-1)}\right|$$

- The difference in current participation coefficients, $\lambda_{Conv,I}^{LL}$, power participation coefficients, $\lambda_{Conv,P}^{LL}$, and equivalence coefficients, K_{Conv}^{LL}, of the diode/thyristor converter models

$$\left|\left(\lambda_{Conv,I}^{LL}\right)^{(k)} - \left(\lambda_{Conv,I}^{LL}\right)^{(k-1)}\right|,\ \left|\left(\lambda_{Conv,P}^{LL}\right)^{(k)} - \left(\lambda_{Conv,P}^{LL}\right)^{(k-1)}\right|,\ \left|\left(K_{Conv}^{LL}\right)^{(k)} - \left(K_{Conv}^{LL}\right)^{(k-1)}\right|$$

Note: $(\bullet)^{(k)}$ represents parameters at k^{th} sweep

Step 5.b. Go to *Step 7* if the maximal difference is within a tolerance range, e.g. $\varepsilon \leq 10^{-8}$. Otherwise, go to *Step 6*.

Step 6. Set the sweep number to $k=k+1$. Start a new backward or forward ac/dc power flow sweep.

Step 6.a. Select all subsystems with:

- $R=R_{max}$ for the backward sweep
- $R=R_{min}$ for the forward sweep

Step 6.b. Go to *Step 3* to calculate the power flow for the subsystems with rank R.

Step 7. Output the ac/dc power flow solutions.

A flow chart of the sequential solver is shown in Figure 3.5. The following subsection focuses on the application of the solver to ac/dc power flow studies.

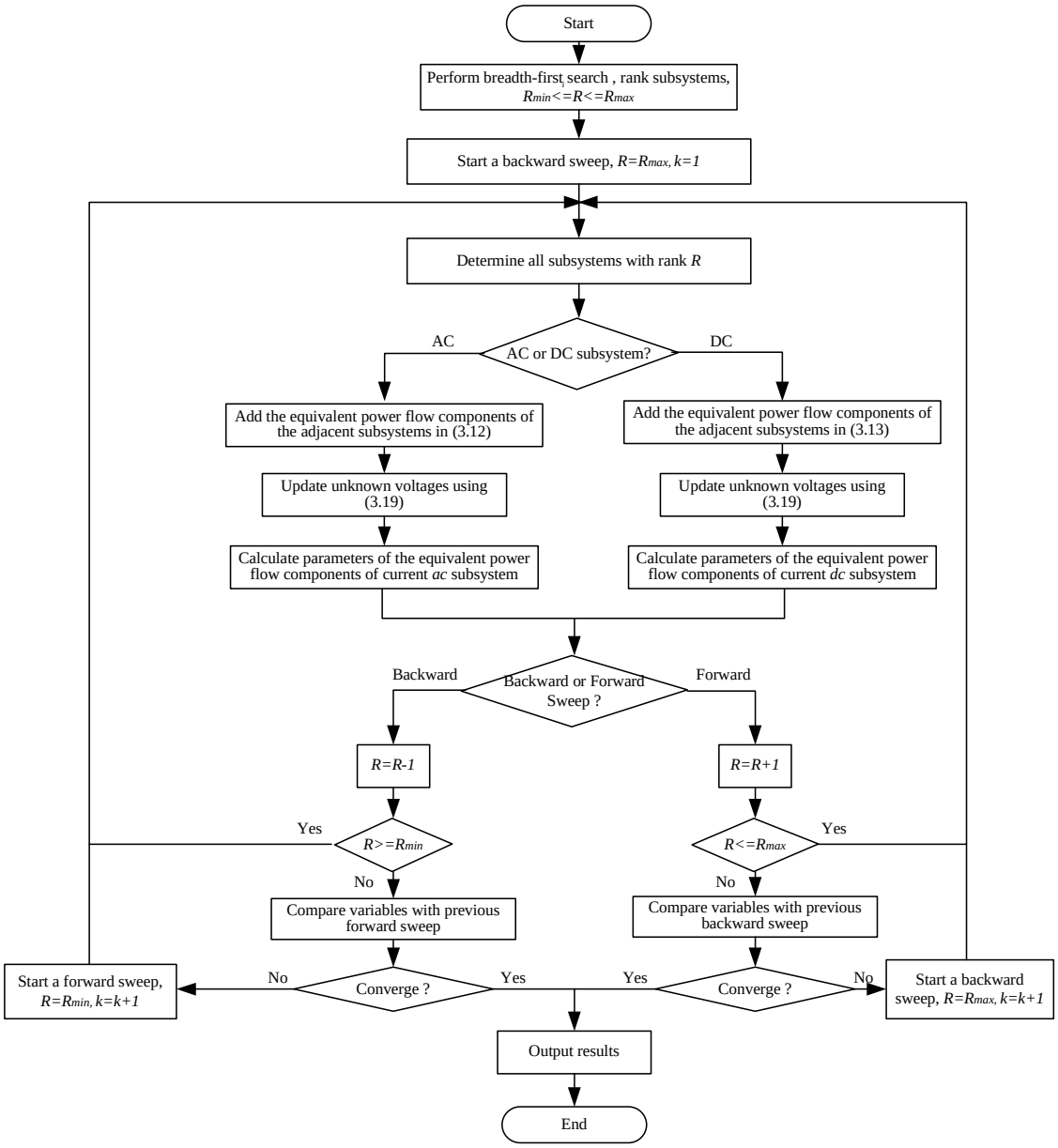


Figure 3.5 Flow chart of the 3-phase sequential *ac/dc* power flow solver

3.4 MATLAB Numerical Results

The power flow algorithm was programmed in MATLAB. It was tested on a 1.5 GHz, 1024 MB computer for bi-directional power flow studies in a three-phase 12-bus system shown in Figure 3.6. Bus 1 is the main source bus and the network contains:

- A three-phase back-to-back thyristor converter placed between ac bus 4 and dc bus 7, allowing currents to flow in both directions
- A three-phase PWM converter placed between ac bus 9 and dc bus 8
- Five ac constant impedance loads and one dc constant impedance load
- A Distributed Generator (DG) placed on bus 11.

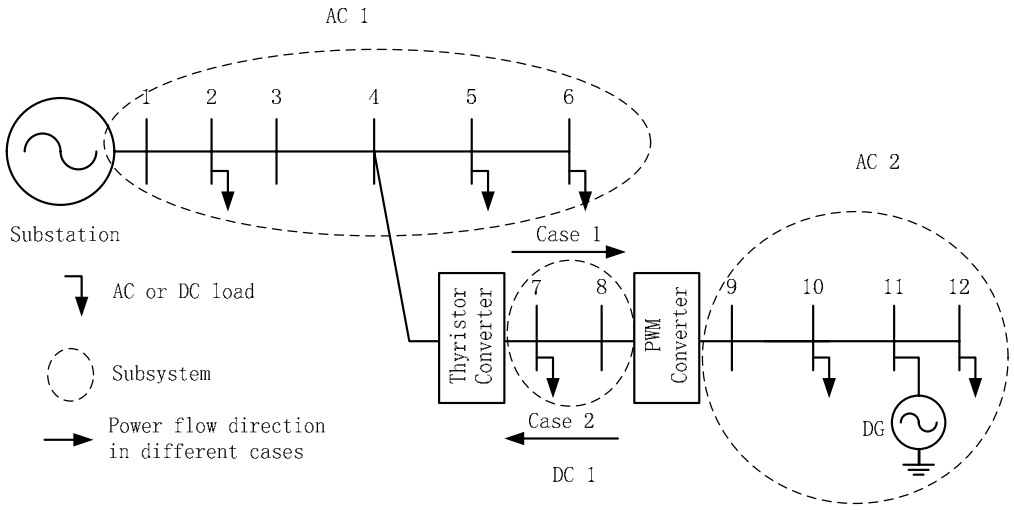


Figure 3.6 A one-line diagram of the 12-bus AC/DC system

Note:

- the ac side of a thyristor converter is the subsystem containing the thyristor converter ac bus, e.g., bus 1 to bus 6 in subsystem AC 1 in Figure 3.6.
- the ac side of a PWM converter is the subsystem containing the PWM converter ac bus, e.g., bus 9 to bus 12 in subsystem AC 2 in Figure 3.6.

The substation was chosen as the main source. The system was divided into the

following three subsystems as shown in Figure 3.6:

- AC 1: bus 1 to bus 6
- DC 1: bus 7 and bus 8
- AC 2: bus 9 to bus 12

The system ranks are determined by the operation modes of the converters.

Two cases were studied to demonstrate that the sequential solver can handle changes in the direction of power flow across the converters. In Case 1, the load on the ac side of the PWM converter was heavy. Power was fed from the substation to the ac side of the PWM converter. In Case 2, the load on the ac side of the PWM converter was light. The DG fed power to the ac side of the thyristor converter. Some parameters used in both cases are listed below:

- The ac voltage on bus 1 was specified as balanced at 1 p.u.;
- Equi-distant control was used for the thyristor converter;
- The commutation angles of the thyristor converter were assumed to be 15 degrees;
- The percentage of the converter real power loss was assumed to be 1%.
- The capacity of the DG was 0.8 MW.

Case 1:

The loads in the system were unbalanced and are shown in Table 3.5. The total load is 4.15 MW. The real power loads on the ac side of the PWM converter was 1.65 MW. The DG outputted power at its full capacitor (0.8 MW). Since the load is larger than the DG's output. Power was fed to the ac side of the PWM converter from the substation through the converters. The following settings were used:

- The thyristor converter operated in the rectifier mode. The firing angles were set to a minimum value (10 degrees) to minimize the consumed reactive power;
- The PWM converter operated in the inverter mode using the ac voltage control. The ac voltage was balanced at 1 p.u.;
- PWM converter ac bus was the slack bus on the ac side of the PWM converter with sufficient capacitance for reactive power determined by the network;
- The ac currents and ac power in the converters were defined as the values injected from the converter models into the ac systems;
- The DG was modeled as a source with constant power (0.8+j0.4 MVA).

Table 3.5 Nominal loads for the 12-bus system in *Case 1*, [MW,MVAR]

Bus	P_a+jQ_a	P_b+jQ_b	P_c+jQ_c
2	0.2+j0	0.4+j0	0.8+j0
5	0.1+j0	0.1+j0	0.1+j0
6	0.2+j0.067	0.2+j0.067	0.2+j0.067
10	0.3+j0.133	0.3+j0.133	0.3+j0.133
11 (DG)	-0.267-j0.133	-0.267-j0.133	-0.267-j0.133
12	0.3+j0.1	0.25+j0.15	0.2+j0.06
7(dc)	0.2		

The sequential *ac*/*dc* power flow solver was applied to the test network. The ranks of the subsystems are given in Table 3.6 based on the ranking method.

Table 3.6 The subsystem ranks in *Case 1*

Rank	*1*	*2*	*3*
subsystem	AC 1	DC 1	AC 2

The tolerance range was set to $\varepsilon \le 10^{-8}$. In order to observe the convergence behavior of the sequential solver, the total number of backward sweeps and forward sweeps, the number of implicit Z-bus iterations and the power flow run time were counted for the following two methods:

M1. the voltages in each subsystem are updated only once at each backward or forward sweep

M2. the voltages in each subsystem are solved at each backward or forward sweep

Table 3.7 Convergence comparison of the sequential method in *Case 1*

	# of backward & forward sweeps	*# of implicit Z-bus iterations*	*Run Time (Sec)*
M1	8	17	0.500
M2	8	35	0.563

Both methods converged to the same solution. Table 3.7 shows that method M1 solved the power flow in 17 iterations, 18 fewer than method M2. This implies that M1 requires fewer flops to solve the power flow. As such, M1 is faster than M2, as indicated by the run time. The simulation results are presented in the following tables and figures:

- Table 3.8 presents the bus voltage magnitudes for each phase. Figure 3.7 shows the unbalanced ac voltage magnitudes
- Table 3.9 presents the ac voltages, ac currents, ac power, participation coefficients, and equivalence coefficients of the thyristor converter model
- Table 3.10 presents the ac voltages, ac currents, and ac power of the PWM converter model

Table 3.8 Bus voltage magnitudes in *Case 1*, |V|: [pu]

	$\|V_a\|$	$\|V_b\|$	$\|V_c\|$
Bus 1	1	1	1
Bus 2	0.997772	0.995201	0.99475
Bus 3	0.996896	0.994329	0.993879
Bus 4	0.99583	0.993267	0.992818
Bus 5	0.994713	0.992156	0.991704
Bus 6	0.99391	0.991359	0.990903
Bus 7 (dc)	2.198731		
Bus 8 (dc)	2.196538		
Bus 9	1	1	1
Bus 10	0.99863	0.998718	0.999167
Bus 11	0.998556	0.998733	0.999631

Bus 12	0.997287	0.997554	0.998902

Note: The dc voltage base was equal to the ac voltage base

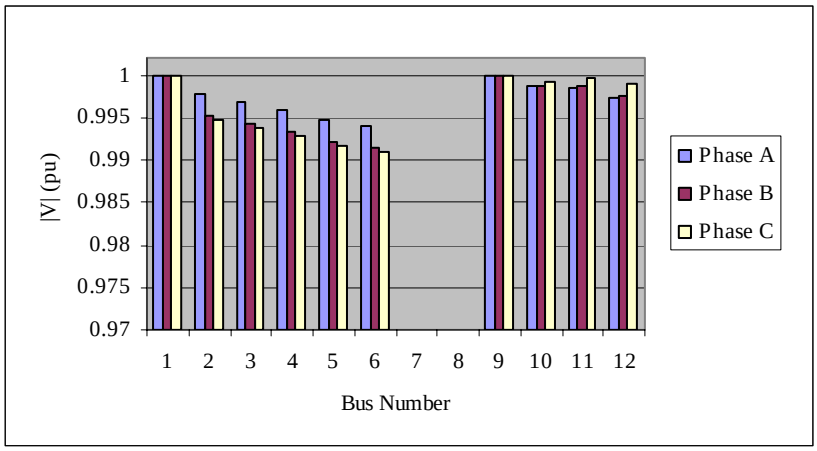


Figure 3.7 AC bus voltage magnitudes in Case 1

From Figure 3.7, it can be seen that the voltages on the ac side of the thyristor converter are unbalanced, e.g, bus 6, because the loads are unbalanced. The voltages on bus 9 are regulated by the PWM converter and are balanced. Since the loads are unbalanced on the ac side of the PWM converter, other buses voltages are unbalanced.

Table 3.9 Parameters of the thyristor converter in *Case 1*, V, I: [pu, deg], S: [pu]

Parameters	*Line AB*	*Line BC*	*Line CA*
V_T^{LL}	$0.9947\angle 29.73^o$	$0.9939\angle -90.34^o$	$0.9934\angle 149.72^o$
I_T^{LL}	$10.99e^{-3}\angle -167.50^o$	$10.97e^{-3}\angle 72.68^o$	$10.96e^{-3}\angle -47.23^o$
S_T^{LL}	$-10.44e^{-3}-j3.24e^{-3}$	$-10.43e^{-3}-j3.19e^{-3}$	$-10.42e^{-3}-j3.14e^{-3}$
$\lambda_{T,I}^{LL}$	0.333724	0.333396	0.33288
$\lambda_{T,P}^{LL}$	0.333536	0.333373	0.333091
K_T^{LL}	1.348963	1.34896	1.348964

Table 3.10 Parameters of the PWM converter in *Case 1*, V, I: [pu, deg], S: [pu]

Parameters	*Line AB*	*Line BC*	*Line CA*
V_{PWM}^{LL}	$1\angle 30^o$	$1\angle -90^o$	$1\angle 150^o$
I_{PWM}^{LL}	$10.389e^{-3}\angle -16.73^o$	$9.572e^{-3}\angle -147.93^o$	$7.209e^{-3}\angle 105.56^o$
S_{PWM}^{LL}	$9.949e^{-3}+j2.99e^{-3}$	$8.457e^{-3}+j4.484e^{-3}$	$6.982e^{-3}+j1.798e^{-3}$

The participation coefficients, $\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$, of the thyristor converter model were not equal because the ac loads were unbalanced. As a consequence, the ac currents, I_T^{LL}, and ac power, S_T^{LL}, were unbalanced. The model was able to reflect the imbalance of the system. The ac currents, I_{PWM}^{LL}, and ac power, S_{PWM}^{LL}, in the PWM converter model were also unbalanced because of the unbalanced loads on the ac side of the PWM converter.

Case 2:

In Case 2, the power flow direction in the converters was reversed from Case 1. The loads in the system are provided in Table 3.11. The DG was operated as the slack bus. It supplied all ac loads on the ac side of the PWM converter (0.5 MW). Since its output limit was set to 0.8 MW, it also supplied the dc load. The following settings were used:

- Thyristor converter operated in the inverter mode with the constant dc power control. The dc power entering the thyristor converter was 0.1 MW. The firing angles were equal to 10 degrees;
- PWM converter operated in the rectifier mode using the ac current control with $V_{PWM,dc,}$ at Bus 8 set to 2.2 p.u;
- The DG was modeled as the slack bus for the ac side of the PWM converter. The ac voltage was balanced at 1 p.u..

Table 3.11 Nominal loads for the 12-bus system in *Case 2*, [MW,MVAR]

Bus	P_a+jQ_a	P_b+jQ_b	P_c+jQ_c
2	0.2+j0	0.4+j0	0.8+j0
5	0.2+j0	0.2+j0	0.2+j0
6	0.267+j0.1	0.267+j0.1	0.267+j0.1
10	0.067+j0.033	0.067+j0.033	0.067+j0.033
12	0.1+j0.05	0.15+j0.07	0.1+j0.06
7(dc)	0.05		

Based on the ranking method, the ranks of the three subsystems are provided in Table 3.12. It is noted that the computation order was reversed from Case 1. This was because power was fed from the ac side of the PWM converter to the ac side of the thyristor converter in Case 2.

Table 3.12 The subsystem ranks in *Case 2*

Rank	*-1*	*0*	*1*
subsystem	AC 2	DC 1	AC 1

The convergence behavior of the sequential solver was investigated again using the two methods in Case 1. The sweep number and implicit Z-bus iteration number are given in Table 3.13 with the power flow run time.

Table 3.13 Convergence comparison of the sequential solver in *Case 2*

	# of backward & forward sweeps	*# of implicit Z-bus iterations*	*Run Time (Sec)*
M1	5	11	0.297
M2	3	15	0.313

Both methods resulted in the same power flow solutions. The ac/dc power flow converged after 11 iterations using M1, 4 fewer than M2. The running time shows that M1 is faster than M2. The simulation results are presented in the following tables:

- Table 3.14 presents the bus voltage magnitudes for each phase and Figure 3.8 shows the unbalanced ac voltage magnitudes
- Table 3.15 presents the ac voltages, ac currents, ac power, participation coefficients, and equivalence coefficients of the thyristor converter model
- Table 3.16 presents the ac voltages, ac currents, and ac power of the PWM converter model

Table 3.14 Bus voltage magnitudes in *Case 2*, |V|: [pu]

	$\|V_a\|$	$\|V_b\|$	$\|V_c\|$
Bus 1	1	1	1
Bus 2	0.998649	0.996079	0.995619
Bus 3	0.998074	0.995511	0.995043
Bus 4	0.997372	0.994816	0.994342
Bus 5	0.995642	0.993097	0.992617
Bus 6	0.994542	0.992004	0.991519
Bus 7 (dc)	2.199627		
Bus 8 (dc)	2.199996		
Bus 9	0.999395	0.999395	0.999395
Bus 10	0.999548	0.999548	0.999548
Bus 11	1	1	1
Bus 12	0.99953	0.999287	0.999605

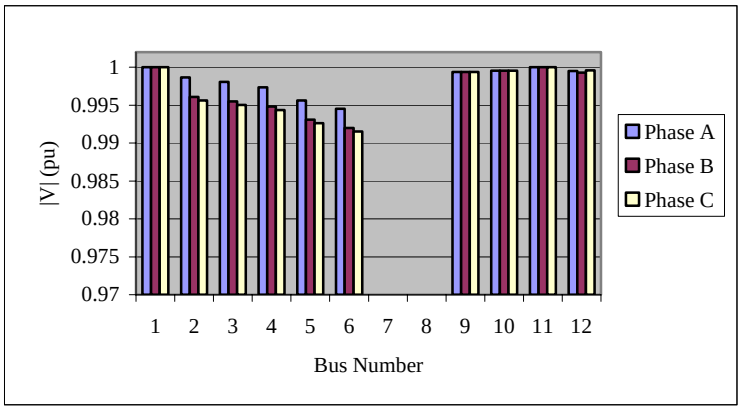


Figure 3.8 AC bus voltage magnitudes in *Case 2*

Table 3.15 Parameters of the thyristor converter model in *Case 2*, V, I: [pu, deg], S:[pu]

Parameters	*Line AB*	*Line BC*	*Line CA*
V_T^{LL}	$0.9962\angle 29.80^o$	$0.9954\angle -90.25^o$	$0.9943\angle 149.80^o$
I_T^{LL}	$1.063e^{-3}\angle 50.56^o$	$1.062e^{-3}\angle -69.7^o$	$1.061e^{-3}\angle 170.19^o$
S_T^{LL}	$0.991e^{-3}$-j$0.376e^{-3}$	$0.990e^{-3}$-j$0.371e^{-3}$	$0.989e^{-3}$-j$0.368e^{-3}$
$\lambda_{T,I}^{LL}$	0.333728	0.333394	0.332877
$\lambda_{T,P}^{LL}$	0.333538	0.333372	0.33309
K_T^{LL}	1.348963	1.34896	1.348964

Table 3.16 Parameters of the PWM converter model in *Case 2*, V, I: [pu, deg], S:[pu]

Parameters	*Line AB*	*Line BC*	*Line CA*
V_{PWM}^{LL}	$0.9994\angle 29.98^{o}$	$0.9994\angle -90^{o}$	$0.9994\angle 149.99^{o}$
I_{PWM}^{LL}	$1.458e^{-3}\angle -150.02^{o}$	$1.458e^{-3}\angle 89.98^{o}$	$1.458e^{-3}\angle -30.02^{o}$
S_{PWM}^{LL}	$-1.46e^{-3}+j0$	$-1.46e^{-3}+j0$	$-1.46e^{-3}+j0$

From the above results, it is shown that the power flow in the thyristor converter and the PWM converter was reversed from that in Case 1. On the ac side of the thyristor converter, unbalanced voltages were applied on the thyristor converter. $\lambda_{T,I}^{LL}$ and $\lambda_{T,P}^{LL}$ were not equal in the delta-connected model, causing unbalanced I_T^{LL} and S_T^{LL}. It is noted that the thyristor converter consumed reactive power although it was operated as an inverter.

On the ac side of the PWM converter, the ac power in the converter model was balanced and the reactive power was equal to zero as expected. Due to the balanced loads between the PWM converter and the DG, whose ac bus was chosen as the slack bus, the ac voltages and ac currents in the PWM converter model were also balanced.

3.5 Comments

In this chapter, a three-phase sequential power flow solver was developed for ac/dc power flow studies. The three-phase delta-connected converter models proposed in Chapter 2 have been incorporated in the sequential solver to model three-phase converters under unbalanced operating conditions. In order to determine the sequence for solving power flow, a ranking method was proposed to rank the subsystems. The ac/dc power flow was solved using a backward/forward algorithm based on subsystem ranks.

The solution algorithm was tested in a radial system for bi-directional power flow studies. The results showed that the sequential solver was robust and converged for the test system using the backward/forward algorithm and the ranking method. The convergence behavior of the solver was improved by updating subsystem voltages only once at each backward/forward iteration. The results also showed that the converter models captured the imbalance of the system and appropriately modeled three-phase converters at different operating modes and control schemes.

CHAPTER 4. THREE-PHASE UNIFIED DISTRIBUTION AC/DC POWER FLOW

In this chapter, a three-phase unified solver is proposed for ac/dc power flow studies using the delta-connected converter models. Steady-state Modified Nodal Analysis (MNA) method is used to incorporate the nodal analysis equations describing dc networks, converter dc terminals, and converter controls with the nodal analysis equations of ac systems. AC state variables and dc state variables are coupled in the modified nodal analysis equations and solved in a unified manner.

Unified solvers were introduced in the 1970's for HVDC system analysis [7][9][32][33]. In order to improve convergence characteristics, existing ac power flow solvers were expanded to single-phase unified ac/dc solvers using the Newton-Raphson method [7][9], a fast decoupled method [32], and a second-order method [33]. Balanced converter models [6], assuming constant dc currents, have been used to couple ac and dc state variables in power flow equations. Similar single-phase, unified approaches using Newton-based methods have been proposed for power flow studies in small ac/dc power systems [14][15] and electrified transit railway power systems [16].

The above unified solvers are not directly applicable to distribution power flow studies because distribution systems are unbalanced and have more distorted voltages and currents than HVDC systems. The power flow equations describing HVDC converters are not appropriate for distribution system converters. Thus, the unbalanced converter models proposed in Chapter 2 cannot be integrated into traditional unified solvers directly. As such, a MNA-based unified solver is proposed using three-phase component models

for distribution power flow studies. In MNA, ac and dc currents in the converter models are chosen as additional state variables. In addition to nodal analysis equations, a set of equations are established to describe the converter models. As such, the ac and dc variables are coupled and can be solved in a unified manner. Some features of the MNA-based unified solver are:

- Direct analysis of the interaction between the ac systems and the dc systems;
- Avoidance of potential divergence problems between ac and dc power flow iterations in sequential solvers;
- Easy development with moderate modifications on existing power flow programs;
- Applying for uni-directional and bi-directional power flow studies.

This chapter is organized as follows. First, the MNA equations used in the unified solver are established with a focus on the converter buses. The delta-connected models are incorporated into the MNA equations for diode/thyristor converters and PWM converters. Then, a solution algorithm is presented, followed by results obtained from a MATLAB implementation. Some comments are made at the end of this chapter.

4.1 AC/DC Power Flow Formulation in MNA

Modified nodal analysis is used to formulate the unified ac/dc power flow problem. MNA is a circuit analysis method based on nodal analysis using the admittance matrix. In nodal analysis, equivalent models are needed for both voltage sources and current dependent components. These models change the structure of the circuits and the admittance matrix becomes unsymmetrical. In addition, the currents of these components can only be obtained by post-processing.

MNA was introduced in [34][35] to manage the above difficulties with nodal analysis. In MNA, the currents in the voltage sources and current dependent components are chosen as additional state variables with the voltages. It keeps the original symmetrical nodal admittance matrix and modified nodal analysis equations can be easily established.

In Chapter 3, three-phase converters were made equivalent to voltage sources or current dependent components using the delta-connected models as shown in Table 3.1 and Table 3.2. Thus, MNA can be used to analyze ac/dc systems. A set of steady-state MNA equations are established in (4.1) with a (7×7) block modified admittance matrix:

$$\left[\begin{array}{ccc|cc|cc} Y_{sub} & Y_{sub,ac} & 0 & 0 & 0 & 0 & 0 \\ Y_{sub,ac} & Y_{ac} & Y_{ac,Conv} & 0 & 0 & 0 & 0 \\ 0 & Y_{ac,Conv} & Y_{Conv} & 0 & 0 & B_{Conv,ac} & 0 \\ \hline 0 & 0 & 0 & G_{dc} & G_{dc,Conv} & 0 & 0 \\ 0 & 0 & 0 & G_{dc,Conv} & G_{Conv} & 0 & B_{Conv,dc} \\ \hline 0 & 0 & C_{Conv,1} & 0 & C_{Conv,2} & D_{Conv,1} & D_{Conv,2} \\ 0 & 0 & C_{Conv,3} & 0 & C_{Conv,4} & D_{Conv,3} & D_{Conv,4} \end{array}\right] \left[\begin{array}{c} V_{sub} \\ V_{ac} \\ V_{Conv} \\ \hline V_{dc} \\ V_{Conv,dc} \\ \hline I_{Conv} \\ I_{Conv,dc} \end{array}\right] = \left[\begin{array}{c} I_{sub,L}(V) \\ I_{ac,L}(V) \\ I_{Conv,L}(V) \\ \hline I_{dc,L}(V) \\ I_{Conv,L_{dc}}(V) \\ \hline F_{Conv} \\ F_{Conv,dc} \end{array}\right] \quad (4.1)$$

where in addition to the notation defined in (3.12) and (3.13):

$n_{ac} \in \mathbb{R}$: the number of ac buses, excluding the substation bus and converter ac buses

$n_{dc} \in \mathbb{R}$: the number of dc buses, excluding the converter dc buses

$n_{Conv} \in \mathbb{R}$: the number of converters

$V_{sub} \in \mathbb{C}^3$: the complex voltage vector of the substation bus

$V_{ac} \in \mathbb{C}^{3n_{ac}}$: the complex voltage vector of ac buses, excluding the substation and converter ac buses

$V_{Conv} \in \mathbb{C}^{3n_{Conv}}$: the complex voltage vector of converter ac buses

$V_{dc} \in \mathbb{R}^{n_{dc}}$: the voltage vector of dc buses, excluding converter dc buses

$V_{Conv,dc} \in \mathbb{R}^{n_{Conv}}$: the voltage vector of converter dc buses

$I_{Conv}(V) \in \mathbb{C}^{3n_{Conv}}$:the complex current injection vector of converter ac buses from the converter model

$I_{Conv,dc}(V) \in \mathbb{R}^{n_{Conv}}$: the current injection vector of converter dc buses

$B_{Conv,ac}$, $B_{Conv,dc}$: the sub-matrices representing the converter's current contributions

$C_{Conv,i}$, $D_{Conv,i}$: the sub-matrices related to the converter models, $i \in \{1,2,3,4\}$

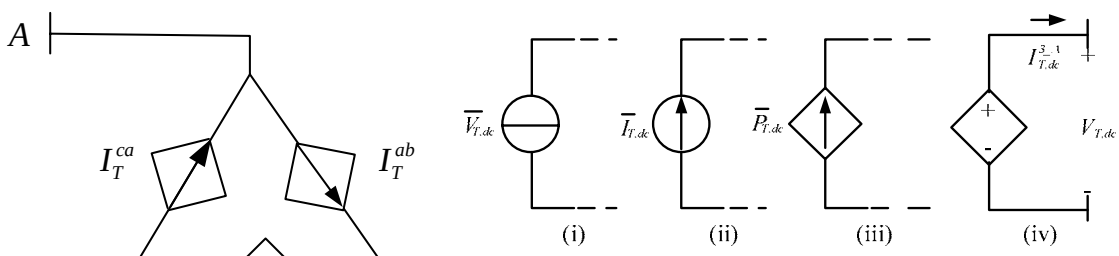
F_{Conv} , $F_{Conv,dc}$: the vectors of constant elements related to the converter models

In (4.1), the top three rows correspond to the ac MNA equations on all ac buses. The contributions of the dc systems to the ac power flow are represented using I_{Conv} . The 4th and 5th rows correspond to the dc MNA equations on all dc buses. The contributions of the ac systems to the dc power flow are represented using $I_{Conv,dc}$. The 6th and 7th rows correspond to appropriate converter models for ac and dc voltages, currents, and power which are discussed in the following subsections for three-phase diode/thyristor converters and PWM converters respectively.

4.1.1 Modified Nodal Analysis Equations for Thyristor Converters and Diode Rectifiers

In Chapter 2, three-phase thyristor converters and diode rectifiers were modeled using three, delta-connected, single-phase converters. Since thyristor converters and diode rectifiers have similar models, this subsection focuses on thyristor converters. Diode rectifiers are discussed briefly at the end.

Based on the delta-connected model, a thyristor converter and the connected dc system can be represented using a delta-connected, current controlled current component on the converter ac bus. The ac system is modeled according to the converter control scheme on the converter dc bus. The equivalent ac and dc power flow components are shown in Figure 4.1.



(a) Equivalent ac components

(b) Equivalent dc components

(i) Constant voltage control

(ii) Constant current control

(iii) Constant power control

(iv) Constant firing angle control

Figure 4.1 The equivalent ac (a) and dc (b) power flow components for ac/dc systems interconnected with three-phase thyristor converters

MNA introduces the complex ac currents and the dc current in the converter model as state variables in the unified solver. As such, the state variables related to thyristor converters include:

- Three line-to-ground complex ac voltages on a grounded bus, $V_T = \begin{bmatrix} V_T^a & V_T^b & V_T^c \end{bmatrix}^T$ or two line-to-line complex ac voltages on an ungrounded bus, $V_T = \begin{bmatrix} V_T^{ab} & V_T^{bc} \end{bmatrix}^T$
- Three complex ac currents in the delta-connected model, $I_T = \begin{bmatrix} I_T^{ab} & I_T^{bc} & I_T^{ca} \end{bmatrix}^T$
- A dc voltage on the converter dc bus, $V_{T,dc}$
- A dc current injected into the converter dc bus from the converter model, $I_{T,dc}^{3\phi}$

The ac and dc MNA equations on thyristor converter buses are established in (4.2) and (4.3) respectively. These two sets of equations correspond to the MNA equations on the 3rd and 5th rows of (4.1):

$$\begin{bmatrix} Y_{T,ac} & Y_{T,T} & \vdots & B_{T,ac} \end{bmatrix} \begin{bmatrix} V_{ac} \\ V_T \\ \hline I_T \end{bmatrix} = \begin{bmatrix} I_{T,L} \end{bmatrix} \tag{4.2}$$

$$\begin{bmatrix} G_{T,dc} & G_{T,T} & \vdots & B_{T,dc} \end{bmatrix} \begin{bmatrix} V_{dc} \\ V_{T,dc} \\ \hline I_{T,dc}^{3\phi} \end{bmatrix} = \begin{bmatrix} I_{T,L_{dc}} \end{bmatrix} \tag{4.3}$$

where:

$$B_{T,ac} = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \text{ for a grounded ac bus}$$

$$B_{T,ac} = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \text{ for an ungrounded ac bus}$$

$$B_{T,dc} = -1$$

It is noted that the ac and dc currents injected from three-phase thyristor converters into the system are represented by $B_{T,ac} \cdot I_T$ and $B_{T,dc} \cdot I_{T,dc}^{3\phi}$ in (4.2) and (4.3) respectively.

The converter equations on the 6th and 7th rows of (4.1) are established using the delta-connected model. First, the ac power injected into the ac bus from the single-phase converters can be represented in (4.4). Please note in (4.4) that the conjugate of the ac power is deliberately selected to represent the power in terms of I_T^{LL} instead of $\left(I_T^{LL}\right)^*$:

$$\left(V_T^{LL}\right)^* \cdot I_T^{LL} = \left(P_T^{LL} + j \cdot Q_T^{LL}\right)^* = \left(P_T^{LL} - j \cdot \sqrt{\left(\left|V_T^{LL}\right| \cdot \left|I_T^{LL}\right|\right)^2 - \left(P_T^{LL}\right)^2}\right)^* \tag{4.4}$$

where:

P_T^{LL}, Q_T^{LL} : the real and reactive power injections from the converter model respectively,

Note: Q_T^{LL} is negative because thyristor converters consume reactive power.

In the model, both $\left|I_T^{LL}\right|$ and P_T^{LL} can be represented as functions of the dc current, $I_{T,dc}^{3\phi}$:

$$\left|I_T^{LL}\right| = \frac{K_T^{LL}}{K_{T,dc}} \lambda_{T,I}^{LL} \cdot I_{T,dc}^{3\phi} \tag{4.5}$$

$$P_T^{LL} = -C_T^{loss} \cdot \lambda_{T,P}^{LL} \cdot P_{T,dc} = -C_T^{loss} \cdot \lambda_{T,P}^{LL} \cdot V_{T,dc} \cdot I_{T,dc}^{3\phi} \tag{4.6}$$

where:

$\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$: the dc current and dc power participation coefficients respectively

K_T^{LL}, $K_{T,dc}$: the ac and dc equivalence coefficients respectively

C_T^{loss}: the loss factor of the model

Substituting (4.5) and (4.6) into (4.4), the following equation is obtained for each single-phase converter in the model:

$$\left(V_T^{LL}\right)^* \cdot I_T^{LL} + \left[C_T^{loss} \cdot \lambda_{T,p}^{LL} \cdot V_{T,dc} - j \frac{1}{sign(I_{T,dc}^{3\phi})} \sqrt{\left(\left| V_T^{LL} \right| \cdot \frac{K_T^{LL}}{K_{T,dc}} \cdot \lambda_{T,I}^{LL} \right)^2 - \left[C_T^{loss} \cdot \lambda_{T,P}^{LL} \cdot V_{T,dc} \right]^2} \right] \cdot I_{T,dc}^{3\phi} = 0 \tag{4.7}$$

In addition, one of the following converter control equations is used in the MNA equations:

- Constant dc voltage control

$$V_{T,dc} = \overline{V}_{T,dc} \tag{4.8}$$

- Constant dc current control

$$I_{T,dc}^{3\phi} = \overline{I}_{T,dc} \tag{4.9}$$

- Constant dc power control

$$V_{T,dc} \cdot I_{T,dc}^{3\phi} = \overline{P}_{T,dc} \tag{4.10}$$

- Constant firing angle control for minimal reactive power

$$V_{T,dc} = \frac{1}{\pi} \sum_{LL \in \{ab,bc,ca\}} \int_{\theta_1^{LL}}^{\theta_2^{LL}} v_{T,dc}^{LL}(t) \cdot dt \tag{4.11}$$

$$= A_T^{ab} \cdot V_T^{ab} + A_T^{bc} \cdot V_T^{bc} + A_T^{ca} \cdot \left(-V_T^{ab} - V_T^{bc} \right)$$

For diode rectifiers, the same approach follows. Since diode rectifiers are not controllable, the dc control equations in (4.8) to (4.11) are replaced by the converter dc voltage, $V_{D,dc}$. $V_{D,dc}$ can be expressed in terms of the line-to-line voltages V_D^{ab} and V_D^{bc} in (3.6), which is repeated here:

$$V_{D,dc} = A_D^{ab} \cdot V_D^{ab} + A_D^{bc} \cdot V_D^{bc} + A_D^{ca} \cdot \left(-V_D^{ab} - V_D^{bc} \right) \tag{4.12}$$

where:

$$A_D^{LL} = \frac{e^{-j\delta_{V_D}^{LL}}}{\pi} \int_{\theta_1^{LL}}^{\theta_2^{LL}} v_{D,dc}^{LL}(t) \cdot dt$$

Next, the MNA equations are established for PWM converters.

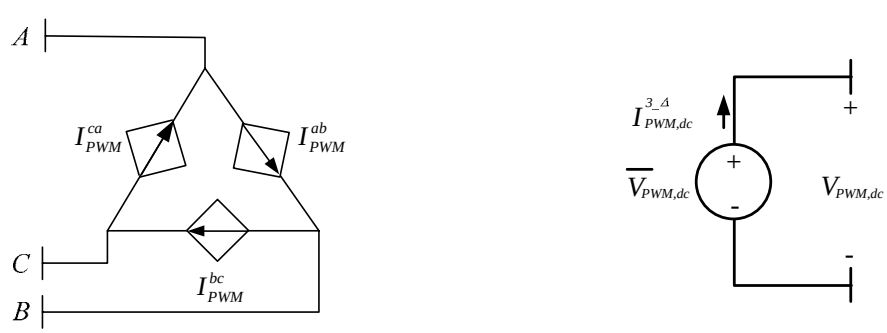
4.1.2 Modified Nodal Analysis Equations for PWM Converters

A three-phase PWM converter can be made equivalent to three, delta-connected, single-phase converters. PWM converters are generally operated by two control schemes:

- ac current control
- ac voltage control

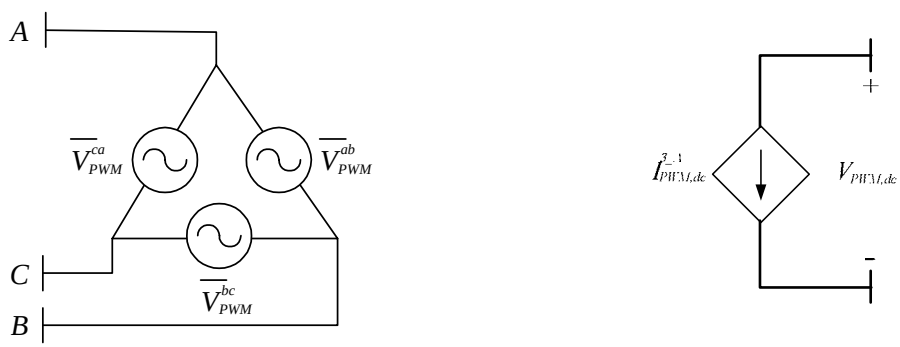
For an ac current controlled converter (e.g. rectifier), the connected dc system can be modeled as a delta-connected, current controlled current component on the converter ac bus. The ac system is modeled as a dc component with constant voltage on the dc bus. The equivalent power flow components are shown in Figure 4.2.

For an ac voltage controlled converter (e.g. inverter), the connected dc system is modeled as a delta-connected voltage component on the converter ac bus. The ac system is modeled as a current controlled current component on the dc bus. The equivalent power flow components are shown in Figure 4.3.



(a) (b)

Figure 4.2 The equivalent ac (a) and dc (b) power flow components for ac/dc systems interconnected with ac current controlled PWM converters



(a) (b)

Figure 4.3 The equivalent ac (a) and dc (b) power flow components for ac/dc systems interconnected with ac voltage controlled PWM converters

For PWM converters with either of the two control schemes, the state variables include:

- Three line-to-ground complex ac voltages on a grounded bus, $V_{PWM} = \begin{bmatrix} V_{PWM}^{a} & V_{PWM}^{b} & V_{PWM}^{c} \end{bmatrix}^T$ or two line-to-line complex ac voltages on an ungrounded bus, $V_{PWM} = \begin{bmatrix} V_{PWM}^{ab} & V_{PWM}^{bc} \end{bmatrix}^T$
- Three complex ac currents in the delta-connected model, $I_{PWM} = \begin{bmatrix} I_{PWM}^{ab} & I_{PWM}^{bc} & I_{PWM}^{ca} \end{bmatrix}^T$
- A dc voltage on the converter dc bus, $V_{PWM,dc}$
- A dc current injected into the converter dc bus from the converter model, $I_{PWM,dc}$

The ac and dc MNA equations on the PWM converter buses are established in (4.13) and (4.14) respectively:

$$\begin{bmatrix} Y_{PWM,ac} & Y_{PWM,PWM} & \vdots & B_{PWM,ac} \end{bmatrix} \begin{bmatrix} V_{ac} \\ V_{PWM} \\ \hline I_{PWM} \end{bmatrix} = \begin{bmatrix} I_{PWM,L} \end{bmatrix} \tag{4.13}$$

$$\left[G_{PWM,dc} \quad G_{PWM,PWM} \;\vdots\; B_{PWM,dc} \right] \begin{bmatrix} V_{dc} \\ V_{PWM,dc} \\ \hline I_{PWM,dc} \end{bmatrix} = \left[I_{PWM,L_{dc}} \right] \tag{4.14}$$

where:

$$B_{PWM,ac} = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \text{ for a grounded ac bus}$$

$$B_{PWM,ac} = \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \text{ for an ungrounded ac bus}$$

$$B_{PWM,dc} = -1$$

The ac and dc currents injected from three-phase PWM converters into the system are represented with $B_{PWM,ac} \cdot I_{PWM}$ and $B_{PWM,dc} \cdot I_{PWM,dc}$ in (4.13) and (4.14) respectively.

The PWM converter equations on the 6th and 7th rows of (4.1) are established using the delta-connected model and converter's control schemes as follows.

4.1.2.1 AC Current Controlled PWM Converters

For an ac current controlled PWM converter, the ac real power is balanced and the reactive power is equal to zero in the single-phase PWM converters. In order to represent the power in terms of I_{PWM}^{LL}, the conjugate of the converter ac power is used and the following two equations hold:

$$\left(V_{PWM}^{ab}\right)^{*} \cdot I_{PWM}^{ab} = \left(V_{PWM}^{bc}\right)^{*} \cdot I_{PWM}^{bc} \tag{4.15}$$

$$\left(V_{PWM}^{bc}\right)^{*} \cdot I_{PWM}^{bc} = \left(-V_{PWM}^{ab} - V_{PWM}^{bc}\right)^{*} \cdot I_{PWM}^{ca} \tag{4.16}$$

Also, the sum of the three-phase real power is equal to the dc power multiplied by a loss factor, C_{PWM}^{loss}. Since the ac reactive power is zero, the following equation holds:

$$-C_{PWM}^{loss} \cdot V_{PWM,dc} \cdot I_{PWM,dc} = \left(V_{PWM}^{ab}\right)^{*} \cdot I_{PWM}^{ab} + \left(V_{PWM}^{bc}\right)^{*} \cdot I_{PWM}^{bc} + \left(-V_{PWM}^{ab} - V_{PWM}^{bc}\right)^{*} \cdot I_{PWM}^{ca} \quad (4.17)$$

On the converter dc bus, the dc voltage is constant:

$$V_{PWM,dc} = \overline{V}_{PWM,dc} \quad (4.18)$$

4.1.2.2 AC Voltage Controlled PWM Converters

For an ac voltage controlled PWM converter, the line-to-line voltages, V_{PWM}^{LL}, are regulated with specified magnitude and angle difference:

$$V_{PWM}^{ab} = \left|\overline{V}_{PWM}^{ab}\right| \cdot e^{j\delta_{V_{PWM}}^{ab}} \quad (4.19)$$

$$V_{PWM}^{bc} = \left|\overline{V}_{PWM}^{bc}\right| \cdot e^{j\left(\delta_{V_{PWM}}^{ab} - \overline{\Delta\delta}_{V_{PWM}}^{ab\_bc}\right)} \quad (4.20)$$

where:

$\left|V_{PWM}^{LL}\right|$, $\delta_{V_{PWM}}^{LL}$: the magnitudes and angles of the converter line-to-line voltages

$\left|\overline{V}_{PWM}^{LL}\right|$: the specified magnitudes of the converter line-to-line voltages

$\overline{\Delta\delta}_{V_{PWM}}^{ab\_bc}$: the specified angle difference between V_{PWM}^{ab} and V_{PWM}^{bc}

If the converter ac bus and the substation are in different subsystems, the voltage angle on phase *a*, $\delta_{V_{PWM}}^{a}$, is chosen as the reference for the ac subsystem connected to the PWM converter. $\delta_{V_{PWMi}}^{ab}$ is constant and equal to thirty degrees for balanced voltages. If the converter ac bus and the substation are in the same subsystem, $\delta_{V_{PWM}}^{ab}$ is referred to the substation and unknown. It is updated using the calculated voltages at each power flow iteration.

The sum of the ac currents in the delta-connected model is equal to zero:

$$I_{PWM}^{ab} + I_{PWM}^{bc} + I_{PWM}^{ca} = 0 \tag{4.21}$$

In addition, the real power on the ac and dc sides of the converter satisfies the following relationship:

$$-C_{PWM}^{loss} \cdot V_{PWM,dc} \cdot I_{PWM,dc} = P_{PWM}^{ab} + P_{PWM}^{bc} + P_{PWM}^{ca} \tag{4.22}$$

$$= \frac{1}{2} \cdot \left[\left(V_{PWM}^{ab} \right)^* \cdot I_{PWM}^{ab} + \left(V_{PWM}^{bc} \right)^* \cdot I_{PWM}^{bc} + \left(-V_{PWM}^{ab} - V_{PWM}^{bc} \right)^* \cdot I_{PWM}^{ca} \right]$$

$$+ \frac{1}{2} \left[\left(V_{PWM}^{ab} \right) \cdot \left(I_{PWM}^{ab} \right)^* + \left(V_{PWM}^{bc} \right) \cdot \left(I_{PWM}^{bc} \right)^* + \left(-V_{PWM}^{ab} - V_{PWM}^{bc} \right) \cdot \left(I_{PWM}^{ca} \right)^* \right]$$

4.2 Solution Algorithm

The implicit Z-bus Gauss method is used to solve (4.1). First, the modified nodal admittance matrix is built. The original admittance matrices of all ac and dc subsystems are constant and existing ac and dc nodal analysis programs can be used to develop them. In addition, $B_{Conv,ac}$ and $B_{Conv,dc}$ are constant and only need to be built once. On the other hand, $C_{Conv,i}$ and $D_{Conv,i}$ are functions of the converter model coefficients and the state variables. They need to be updated at each iteration.

It is noted that state variables include ac and dc currents in the converter models. Thus, new notation is introduced in (4.1). Some of the state variables are specified and defined as U_1 below:

- the ac voltages on the substation or ac voltage controlled PWM converters;
- the dc voltages on dc voltage controlled thyristor converters or on ac current controlled PWM converters;
- The dc currents in dc current controlled thyristor converters.

Other state variables, U_2, are solved using U_1. Assume that (4.1) is reorganized as:

$$\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \end{bmatrix} = \begin{bmatrix} F_1(U_1) \\ F_2(U_2) \end{bmatrix} \tag{4.23}$$

where:

$M_{11}(U_1,U_2)$, $M_{12}(U_1,U_2)$: the self and mutual modified admittance sub-matrices on the buses with the specified state variables

$M_{22}(U_1,U_2)$, $M_{21}(U_1,U_2)$: the self and mutual modified admittance sub-matrices on the buses with the unspecified state variables

$F_1(U_1)$, $F_2(U_2)$: the modified current injection vector, which are functions of state variables, on the buses with the specified and unspecified state variables, respectively

Thus, U_2 can be solved in an iterative manner:

$$U_2^{(k)} = \left[M_{22}^{(k-1)}\left(U_2^{(k-1)}\right)\right]^{-1} \cdot \left[F_2^{(k-1)}\left(U_2^{(k-1)}\right) - M_{21}^{(k-1)}\left(U_2^{(k-1)}\right) \cdot U_1 \right] \tag{4.24}$$

where:

k: iteration number

M_{21}, M_{22}, and F_2, are functions of U_2. They are updated at each iteration until the difference of U_2 between two consecutive iterations is within a tolerance range.

The solution procedure of the unified power flow solver includes the following steps:

Step 1. Search the network and determine all converters and subsystems

Step 1.a. Choose all complex ac voltages and dc voltages as the state variables;

Step 1.b. Determine the appropriate converter models. Choose the complex ac currents and dc currents in the converter models as the state variables;

Step 1.c. Initialize the state variables and the coefficients of converter models.

Step 2. Build the constant sub-matrices in (4.1)

Step 2.a. Build the original admittance matrices for the ac and dc subsystems, excluding the converters;

Step 2.b. Build $B_{Conv,ac}$, $B_{Conv,dc}$;

Step 2.c. Add constant elements into the modified current injection vector.

Step 3. Solve the ac/dc power flow using the implicit Z-bus Gauss method

Step 3.a. Calculate the non-constant elements in $C_{Conv,i}$, $D_{Conv,i}$;

Step 3.b. Calculate the voltage dependent elements in the modified current injection vector;

Step 3.c. Update the unspecified state variables, U_2, using (4.24);

Step 3.d. Solve the converter models and update the coefficients of the models using the updated state variables;

Step 3.e. Compare U_2 with those obtained from the previous iteration, $\Delta U_2^{(k)} = \left| U_2^{(k)} - U_2^{(k-1)} \right|$, k= iteration number

- If $\max\left(\Delta U_2^{(k)}\right) \le \varepsilon = 10^{-8}$, power flow converges and go to *Step 4*.
- Otherwise, go to *Step 3.a* for next iteration.

Step 4. Output ac/dc power flow solutions.

A flow chart of the three-phase unified power flow solver is shown in Figure 4.4. The following section focuses on the application of the solvers to general structure power flow studies.

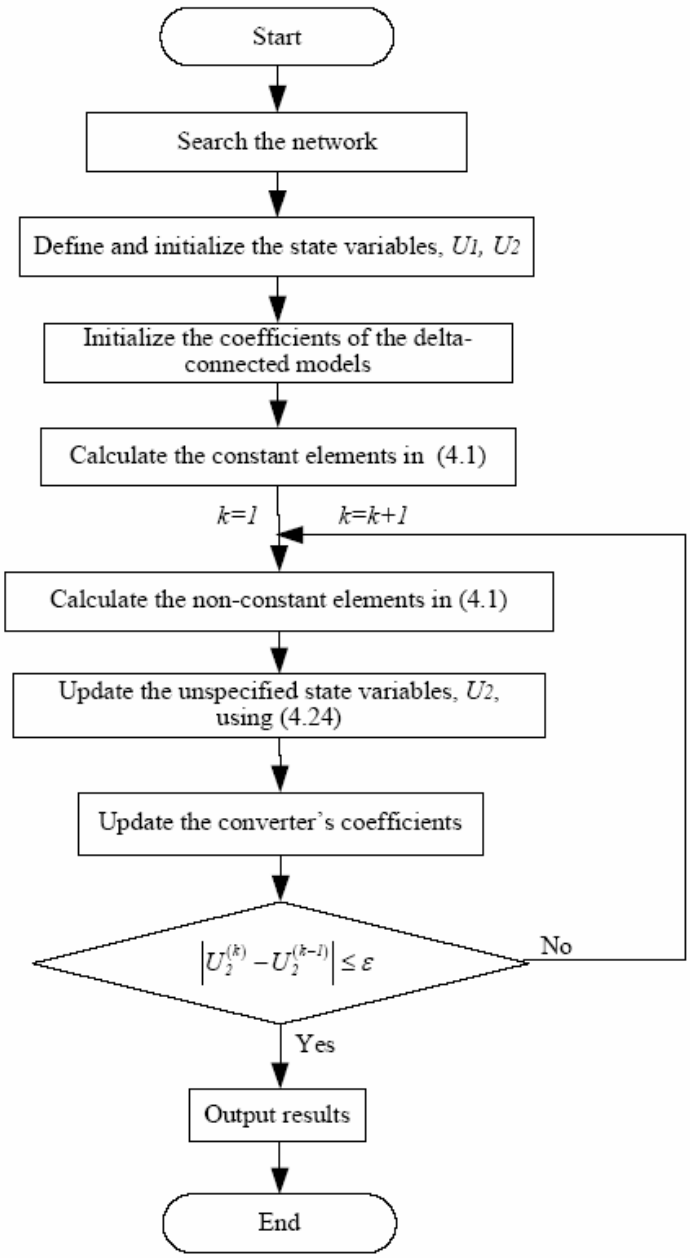


Figure 4.4 The flow chart of the three-phase MNA based unified ac/dc power flow solver

4.3 MATLAB Numerical Results

The power flow algorithm was tested on a meshed, three-phase, 25-bus system shown in Figure 4.5. This type of system structure mimics a shipboard power system. Bus 1 is the power source bus and this network contains:

- A three-phase back-to-back thyristor converter placed between ac bus 18 and dc bus 23, allowing the ac and dc currents to flow in both directions;
- A three-phase PWM converter placed between ac bus 10 and dc bus 25;
- Four constant impedance and two constant power ac loads and one constant impedance dc load.

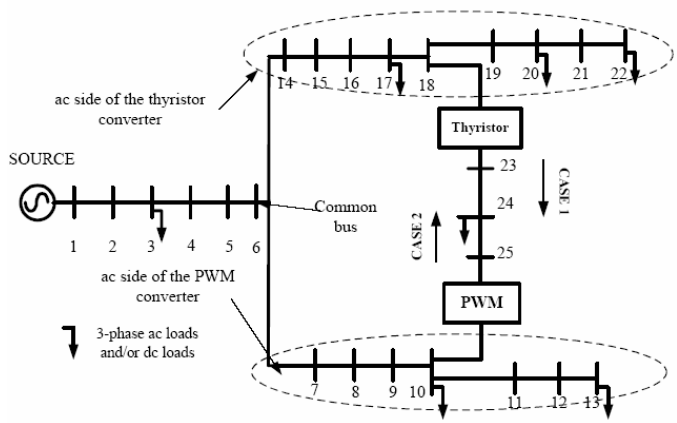


Figure 4.5 A one-line diagram of the 25-bus system

Note:

- "Common bus" is the first bus on the path from the thyristor back to the substation and the path from PWM converters back to the substation, e.g., bus 6 in Figure 4.5;
- ac side of a thyristor converter is the subsystem from the common bus to the thyristor converter ac bus and downstream buses, e.g., bus 6 to bus 22 in Figure 4.5;

- ac side of a PWM converter is the subsystem from the common bus to the PWM converter ac bus and downstream ac buses, e.g., bus 6 to bus 13 in Figure 4.5.

Two cases were studied to show how ac/dc power flow was solved by the unified solver using the delta-connected converter models. In both cases, the amount and the direction of the power flow were controlled by the converters to balance current flow and to improve voltages. In *Case 1*, the load on the ac side of the PWM converter was heavy. Power was fed to the ac side of the PWM converter through the converters. The thyristor converter was operated in the rectifier mode and the PWM converter was operated in the inverter mode.

In *Case 2*, the load on the ac side of the thyristor converter was heavy. Power was fed to the ac side of the thyristor converter through the converters. The thyristor converter was operated in the inverter mode and the PWM converter was operated in the rectifier mode. Some parameters used in both cases are listed below:

- The ac voltage on bus 1 was balanced at 1 p.u.;
- The commutation angles of the thyristor converter were set to 15 degrees;
- 0.200 MVar capacitors were installed on each phase at the thyristor ac bus (bus 18) to provide reactive power for the thyristor converter;
- The percentage of the thyristor and PWM converter real power losses was 1%.

In both cases, the parameters of the converters are defined according to their control modes. The thyristor converter was operated by one of the following two control schemes:

- Constant firing angle control – the minimal firing angles were specified in degrees to minimize the consumed reactive power;

- Constant dc power control – the nominal dc power was specified and the firing angles were specified in degrees.

The PWM converter was operated by the ac current control. The PWM converter dc voltage was specified in per unit.

Case 1: the system is balanced with 5.1MW total load. In Table 4.1, the loads on the ac side of the PWM converter (2.2MW) were larger than those on the ac side of the thyristor converter (1.2MW).

Table 4.1 Nominal loads for the 25-bus system in *Case 1*, [MW,MVAR]

Bus	P_a+jQ_a	P_b+jQ_b	P_c+jQ_c
3	0.5+j0	0.5+j0	0.5+j0
10	0.533+j0.267	0.533+j0.267	0.533+j0.267
13	0.2+j0.067	0.2+j0.067	0.2+j0.067
17	0.1+j0.033	0.1+j0.033	0.1+j0.033
20	0.2+j0.067	0.2+j0.067	0.2+j0.067
22	0.1+j0.033	0.1+j0.033	0.1+j0.033
24(dc)	0.2		

Two scenarios were tested. In *Case 1a*, no power was transferred to the ac side of the PWM converter through the PWM converter ($P_{PWM,ac}=0$). Here, only the thyristor converter supplied the dc system. In *Case 1b*, power was transferred to the ac side of the PWM converter through the PWM converter ($P_{PWM,ac}>0$). In both scenarios, the bus voltages and converter model currents were solved and were the same using both the sequential and unified solvers.

Case 1a: ($P_{PWM,ac}$=0)

Initially, $P_{PWM,ac}$ was zero. The thyristor converter was operated in the rectifier mode using the constant firing angle control to minimize the consumed reactive power. The firing angles were 10 degrees. The thyristor converter provided power for the dc network.

The power flow results are provided in the following figures and tables:

- Figure 4.6 plots the ac line currents on phase *a* in the balanced system and Table 4.2 presents the maximum line currents on the ac sides of the converters.
- Figure 4.7 plots the ac voltage magnitudes on phase *a* in the balanced system and Table 4.3 presents the bus voltage magnitudes on the ac sides of the converters.
- Table 4.4 presents the current participation coefficients, $\lambda_{T,I}^{LL}$, power participation coefficients, $\lambda_{T,P}^{LL}$, and equivalence coefficients, K_T^{LL}, in the thyristor converter model.

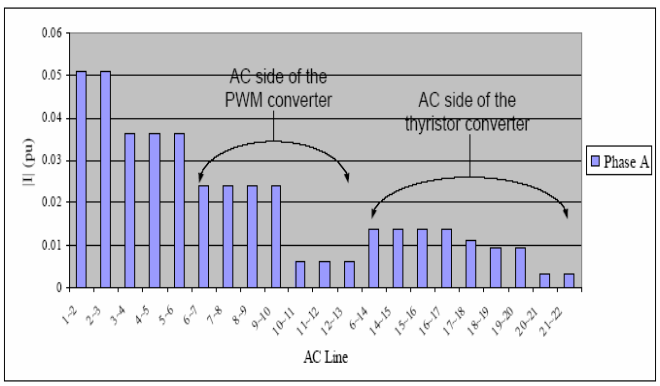


Figure 4.6 AC line current magnitudes on phase *a* in *Case 1a*

Table 4.2 Maximum current magnitudes on the *ac* sides of the converters in *Case 1a* with $P_{PWM,ac} = 0$ MW, |I|: [pu]

AC Area	*Line with I_{max}*	$\|I_a\|$	$\|I_b\|$	$\|I_c\|$
PWM Side	*bus6-bus7*	0.023877	0.023877	0.023877
Thyristor Side	*bus6-bus14*	0.013766	0.013766	0.013766

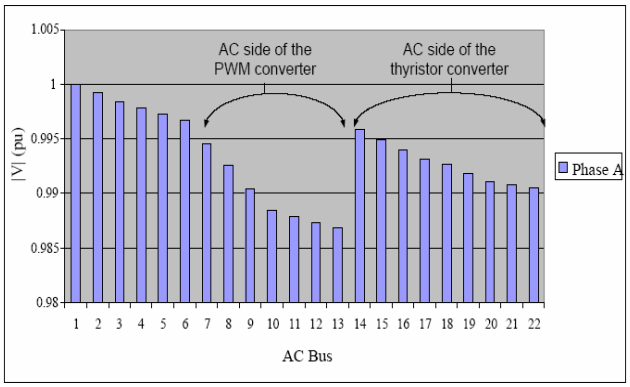


Figure 4.7 AC bus voltage magnitudes on phase *a* in *Case 1a*

Table 4.3 AC bus voltage magnitudes on the *ac* sides of the converters in *Case 1a* with $P_{PWM,ac} = 0$ MW, |V|: [pu]

Bus	$\|V_a\|$	$\|V_b\|$	$\|V_c\|$
1	1	1	1
10	0.988416	0.988416	0.988416
11	0.987895	0.987895	0.987895
12	0.987375	0.987375	0.987375
13	0.986855	0.986855	0.986855
18	0.992627	0.992627	0.992627
19	0.991843	0.991843	0.991843
20	0.99106	0.99106	0.99106
21	0.990799	0.990799	0.990799
22	0.990538	0.990538	0.990538

Table 4.4 Coefficients of the delta-connected thyristor converter model in *Case 1a* with $P_{PWM,ac} = 0$ MW

Parameters	*Line ab*	*Line bc*	*Line ca*
$\lambda_{T,I}^{LL}$	0.333333	0.333333	0.333333
$\lambda_{T,P}^{LL}$	0.333333	0.333333	0.333333
K_T^{LL}	1.348964	1.348964	1.348964

Remarks:

- In Figure 4.6, the line currents on the ac side of the PWM converter are larger than those on the ac side of the thyristor converter. It is because the ac side of the PWM converter is more heavily loaded;

- In Table 4.2, the feeder imbalance can also be observed. The maximal line currents on the ac side of the PWM converter (line 6-7) were $\left(\frac{0.023877}{0.013766}-1\right)\cdot 100\% \approx 73\%$ higher than those on the ac side of the thyristor converter (line 6-14);
- In Figure 4.7 and Table 4.3, the voltage magnitudes on the ac side of the PWM converter were relatively low, e.g., bus 10, caused by the high line currents;
- In Table 4.4, $\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$ and K_T^{LL} are balanced in the thyristor converter model because the system is balanced;
- The total real power loss was 36.5 KW.

It is noted that the feeder currents were significantly unbalanced. This can be improved by transferring power from the thyristor converter to the ac side of the PWM converter. As a consequence, the low bus voltages can also be improved and the loss could be reduced. It is illustrated in *Case 1b*.

***Case 1b*: ($P_{PWM,ac} > 0$)**

In this scenario, real power was transferred through the PWM converter to the ac side of the PWM converter ($P_{PWM,ac} > 0$) with the following settings:

- The thyristor converter operated as a dc power controlled rectifier;
- The PWM converter operated as an ac current controlled inverter with unity power factor;
- The dc voltage on the PWM converter dc bus (bus 25) was set to 2.2 p.u. with the dc voltage base equal to the ac voltage base.

The thyristor converter dc power, $P_{T,dc}$, and PWM converter ac power, $P_{PWM,ac}$, were estimated with:

$$P_{T,dc} = \frac{P_{PWM,load} - P_{T,load} + P_{dc,load}}{2} = 0.6 \quad \text{MW} \tag{4.25}$$

$$P_{PWM,ac} = \frac{P_{PWM,load} - P_{T,load} - P_{dc,load}}{2} = 0.4 \quad \text{MW} \tag{4.26}$$

where:

$P_{T,load}$: total loads on the ac side of the thyristor converter

$P_{PWM,load}$: total loads on the ac side of the PWM converter

$P_{dc,load}$: total dc loads

Power flow was solved and results are displayed in Figure 4.8, Figure 4.9, and Table 4.5 to Table 4.8.

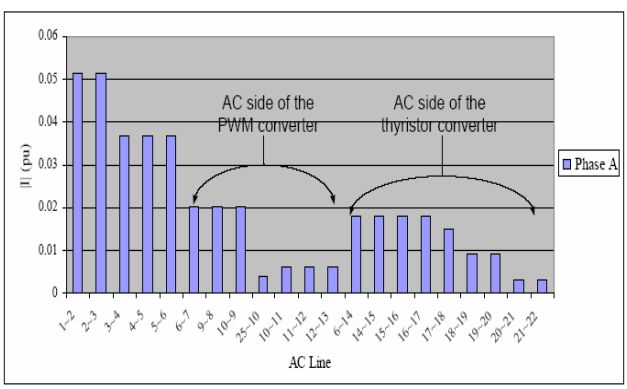


Figure 4.8 AC line current magnitudes on phase *a* in *Case 1b*

Table 4.5 Maximum current magnitudes on the *ac* sides of the converters in *Case 1b* with $P_{PWM,ac} = 0.4$ MW, |I|: [pu]

AC Area	*Line with Imax*	$\lvert I_a \rvert$	$\lvert I_b \rvert$	$\lvert I_c \rvert$
PWM Side	*bus6-bus7*	0.0202	0.0202	0.0202
Thyristor Side	*bus6-bus14*	0.0180	0.0180	0.0180

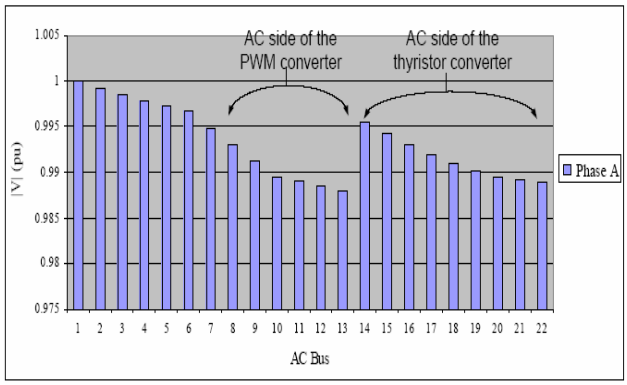


Figure 4.9 AC bus voltage magnitudes on phase *a* in *Case 1b*

Table 4.6 Bus voltage magnitudes on the *ac* sides of the converters in *Case 1b* with $P_{PWM,ac} = 0.4$ MW, |V|: [pu]

Bus	$\|V_a\|$	$\|V_b\|$	$\|V_c\|$
1	1	1	1
10	0.9895	0.9895	0.9895
11	0.98898	0.98898	0.98898
12	0.988459	0.988459	0.988459
13	0.987938	0.987938	0.987938
18	0.990957	0.990957	0.990957
19	0.990175	0.990175	0.990175
20	0.989393	0.989393	0.989393
21	0.989132	0.989132	0.989132
22	0.988872	0.988872	0.988872

Table 4.7 Coefficients of the delta-connected thyristor converter model in *Case 1a* with $P_{PWM,ac} = 0.4$ MW

Parameters	*Line ab*	*Line bc*	*Line ca*
$\lambda_{T,I}^{LL}$	0.333333	0.333333	0.333333
$\lambda_{T,P}^{LL}$	0.333333	0.333333	0.333333
K_T^{LL}	1.348964	1.348964	1.348964

Table 4.8 AC power injected into the ac system from the three-phase converters in *Case 1b* with $P_{PWM,ac} = 0.4$ MW, S: [MW, MVAR]

Converter Bus	P_a+jQ_a	P_b+jQ_b	P_c+jQ_c	*Total*
10	0.1364+j0	0.1364+j0	0.1364+j0	0.4092
18	-0.2020-j0.0345	-0.2020-j0.0345	-0.2020-j0.0345	-0.606-0.1035

Compared to *Case 1a*, it was found in *Case 1b* that:

- the high currents were reduced on the ac side of the PWM converter with better feeder balance, e.g., currents in line 6-7 is $\left(\frac{0.0202}{0.0180}-1\right)\cdot 100\% \approx 12\%$ higher than the currents in line 6-14 in Table 4.5;
- the bus voltages were improved on the ac side of the PWM inverter as shown in Figure 4.9 and Table 4.6;
- in Table 4.7, the thyristor converter model's coefficients are the same as those in *Case 1a* because the system is still balanced;
- in Table 4.8, the thyristor converter consumed 0.606 MW from the ac system, including 1% converter loss. 0.4092 MW was transferred to the ac side of the PWM converter as desired;
- the real power loss was reduced to 33.9 KW.

From the above two scenarios, it can be seen that the unified solver can handle changes of power flow direction across converters in balanced ac/dc systems. In *Case 2*, the test 25-bus system became unbalanced and ac/dc power flow was studied.

Case 2: the system is unbalanced and the total loads are 4.85 MW as shown in Table 4.9. The loads on the ac side of the thyristor converter (2.1 MW) are larger than those on the ac side of the PWM converter (0.95 MW).

Table 4.9 Nominal loads for the 25-bus system in *Case 2*, [MW, MVAR]

Bus	P_a+jQ_a	P_b+jQ_b	P_c+jQ_c
3	0.5+j0	0.5+j0	0.6+j0
10	0.25+j0.1	0.2+j0.05	0.2+j0.15
13	0.1+j0.033	0.1+j0.033	0.1+j0.033
17	0.1+j0.033	0.1+j0.033	0.1+j0.033

20	0.35+j0.2	0.35+j0.3	0.4+j0.2
22	0.25+j0.1	0.25+j0.1	0.2+j0.08
24(dc)	0.2		

Two scenarios were tested. In *Case 2a*, $P_{PWM,ac}$ was equal to zero and the thyristor converter supplied the dc system. In *Case 2b*, power was transferred to the ac side of the thyristor converter through the PWM converter ($P_{PWM,ac} < 0$) to improve the current flow and bus voltages on the ac side of the thyristor converter.

Case 2a: ($P_{PWM,ac} = 0$)

In this scenario, no power was transferred through the PWM converter. The thyristor converter was operated in the rectifier mode using the constant firing angle control. The firing angles were set to 10 degrees. Power flow was solved and the ac line current magnitudes and ac bus voltage magnitudes were plotted in Figure 4.10 and Figure 4.11. Please see Table 4.10 and Table 4.11 for the maximal line currents and bus voltages on the ac sides of the converters. Table 4.12 presents the coefficients of the thyristor converter models.

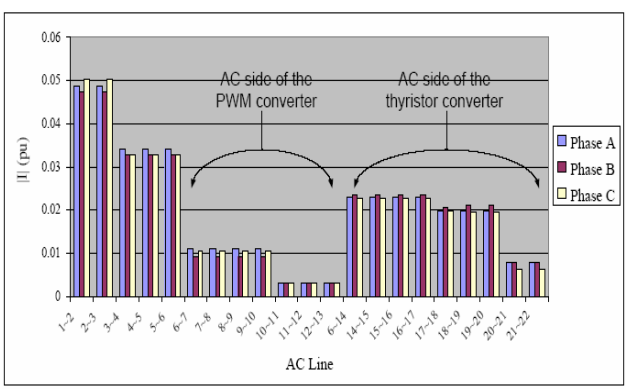


Figure 4.10 AC line current magnitudes in *Case 2a*

Table 4.10 Maximum current magnitudes on AC sides of the converters in *Case 2a* with $P_{PWM,ac} = 0$ MW, |I|: [pu]

AC Area	*Line with Imax*	$\|I_a\|$	$\|I_b\|$	$\|I_c\|$
PWM Side	*bus6-bus7*	0.01115	0.00929	0.010467
Thyristor Side	*bus6-bus14*	0.02291	0.02362	0.022806

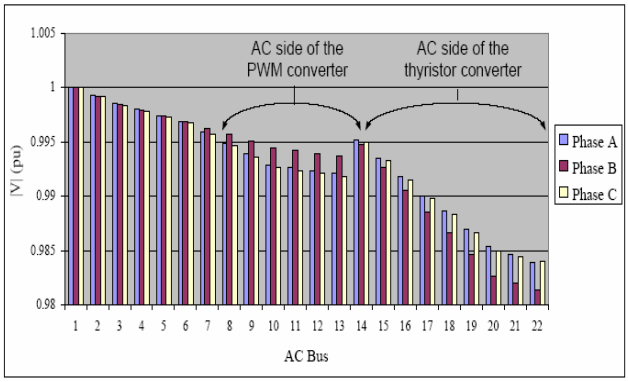


Figure 4.11 AC bus voltage magnitudes in *Case 2a*

Table 4.11 AC bus voltage magnitudes in *Case 2a* with $P_{PWM,ac} = 0$ MW, |V|: [pu],

Bus	$\|V_a\|$	$\|V_b\|$	$\|V_c\|$
1	1	1	1
10	0.992873	0.994481	0.99263
11	0.992611	0.994219	0.992369
12	0.99235	0.993957	0.992108
13	0.992088	0.993695	0.991847
18	0.988615	0.986672	0.988292
19	0.986978	0.984656	0.986631
20	0.985341	0.98264	0.984971
21	0.984603	0.981982	0.984474
22	0.983865	0.981325	0.983977

Table 4.12 Coefficients of the delta-connected thyristor converter model in *Case 2a* with $P_{PWM,ac} = 0$ MW

Parameters	*Line ab*	*Line bc*	*Line ca*
$\lambda_{T,I}^{LL}$	0.332997	0.33342	0.333582
$\lambda_{T,P}^{LL}$	0.333157	0.333375	0.333468
K_T^{LL}	1.348966	1.348968	1.348964

Remarks:

- In Figure 4.10 and Table 4.10, the line currents on the ac side of the thyristor converter were significantly higher than those on the ac side of the PWM converter, e.g., the current on phase *a* in line 6-14 was $\left(\frac{0.02291}{0.01115}-1\right)\cdot 100\% \approx 105\%$ higher than that in line 6-7;
- In Figure 4.11 and Table 4.11, the voltages on the ac side of the thyristor converter (bus 18 to bus 22) were relatively low;
- In Table 4.12, the three coefficients, $\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$, K_T^{LL}, in the delta-connected thyristor converter model were unbalanced because of the unbalanced converter ac voltages caused by the unbalanced ac loads;
- The total power loss was 38.11 MW.

In order to balance the feeder current flow, real power was transferred from the PWM converter to the ac side of the thyristor converter in *Case 2b.* As a consequence, the voltages can be improved and real power loss could be reduced.

***Case 2b*:** ($P_{PWM,ac}$ <0)

In this scenario, the PWM converter was operated as a rectifier. It supplied the dc system and transferred power to the ac side of the thyristor converter. The following settings were used:

- The thyristor converter operated as a dc power controlled inverter;
- The PWM converter operated as an ac current controlled rectifier with unity power factor;
- The PWM converter dc voltage was constant and set to 2.2 p.u.

$P_{T,dc}$ and $P_{PWM,ac}$ were estimated using following equations:

$$P_{T,dc} = -\left(\frac{P_{T,load} - P_{PWM,load} - P_{dc,load}}{2} \right) = -0.475 \quad \text{MW} \tag{4.27}$$

$$P_{PWM,ac} = -\left(\frac{P_{T,load} - P_{PWM,load} + P_{dc,load}}{2} \right) = -0.675 \quad \text{MW} \tag{4.28}$$

Power flow was solved and the results are provided in the following figures and tables:

- Figure 4.12 plots the ac line current magnitudes and Table 4.13 presents the maximal currents on the ac sides of the converters;
- Figure 4.13 plots the ac bus voltage magnitudes and Table 4.14 presents the bus voltage magnitudes on the ac sides of the converters;
- Table 4.15 provides the thyristor converter model's coefficients;
- Table 4.16 provides the ac power injected from the converters into the ac system.

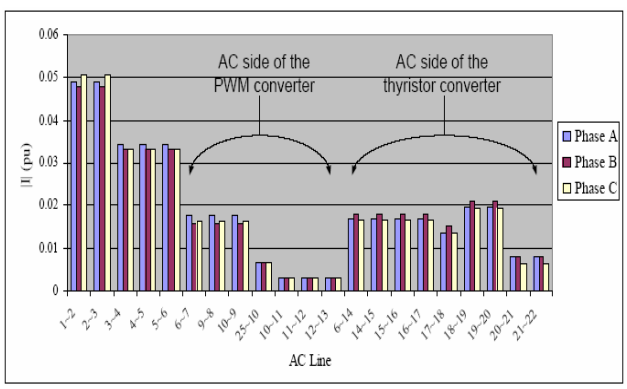


Figure 4.12 AC line current magnitudes in *Case 2b*

Table 4.13 Maximum current magnitudes on the *ac* sides of the converters in *Case 2b* with $P_{PWM,ac} = -0.675$ MW, |I|: [pu]

AC Area	*Line with I_{max}*	$\lvert I_a \rvert$	$\lvert I_b \rvert$	$\lvert I_c \rvert$
PWM Side	*bus6-bus7*	0.0175	0.0158	0.0165
Thyristor Side	*bus6-bus14*	0.0169	0.0181	0.0168

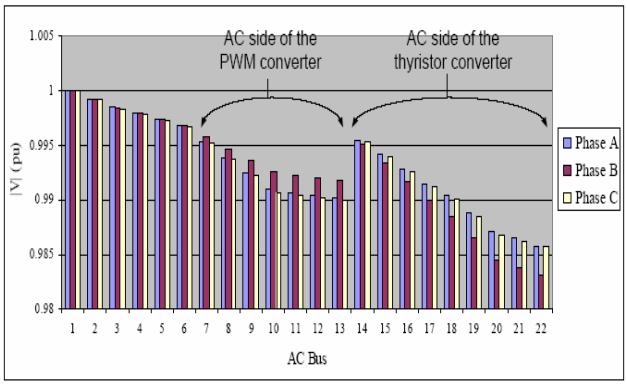


Figure 4.13 AC bus voltage magnitudes in *Case 2b*

Table 4.14 Bus voltage magnitudes on the *ac* sides of the converters in *Case 2b* with $P_{PWM,ac} = -0.675$ MW, |V|: [pu]

Bus	$\|V_a\|$	$\|V_b\|$	$\|V_c\|$
1	1	1	1
10	0.990981	0.992583	0.990738
11	0.99072	0.992321	0.990477
12	0.990458	0.992059	0.990217
13	0.990197	0.991798	0.989956
18	0.990453	0.988501	0.990127
19	0.988813	0.986481	0.988464
20	0.987174	0.984462	0.986801
21	0.986434	0.983803	0.986302
22	0.985695	0.983144	0.985804

Table 4.15 Coefficients of the delta-connected thyristor converter model in *Case 2b* with $P_{PWM,ac} = -0.675$ MW

Parameters	*Line ab*	*Line bc*	*Line ca*
$\lambda_{T,I}^{LL}$	0.332999	0.333418	0.333583
$\lambda_{T,P}^{LL}$	0.333158	0.333374	0.333469
K_T^{LL}	1.348966	1.348968	1.348964

Table 4.16 AC power injected into the ac system from the three-phase converters in *Case 2b* with $P_{PWM,ac} = -0.675$ MW, S: [MW, MVAR]

Converter Bus	P_a+jQ_a	P_b+jQ_b	P_c+jQ_c	*Total*
10	-2.1946 +j0	-2.1981 +j0	-2.1940 +j0	-6.5867
18	1.5711-j0.5586i	1.5638-j0.5560	1.5676-j0.5645	4.7025-j1.6791

Compared to *Case 2a*, it is found in *Case 2b* that:

- the feeder currents were more balanced than *Case 2a* as shown in Figure 4.12. In Table 4.13, the currents in line 6-14 became close to those in line 6-7;
- the ac voltages on the ac side of the thyristor converter were improved as shown in Figure 4.13 and Table 4.14;
- Table 4.15 shows that the coefficients of the thyristor converter model were unbalanced and were slightly different from those in *Case 2a*. It is because the system imbalance was changed by transferring power through the converters;
- the loss was reduced to 33.3 KW.

From the above two scenarios, it is shown that the unified solver can solve ac/dc power flow for unbalanced systems with the converters operating at various modes.

4.4 Comments

In this chapter, a three-phase unified power flow solver was developed. The modified nodal analysis method (MNA) was implemented in the solver. It introduced the converter ac and dc currents as additional state variables in the nodal analysis equations. As a consequence, the ac and dc power flow equations are coupled at converters. AC and dc state variables can be solved in a unified manner. In MNA, unbalanced converter models proposed in Chapter 2 have been used. The models capture the imbalance of ac/dc systems using three, delta-connected, single-phase converters and can be included in modified nodal analysis equations conveniently.

The unified solver can be developed using existing nodal analysis based solvers with moderate modifications. MATLAB numerical studies show that it converged to the same solution as the sequential solver.

CHAPTER 5. HARDWARE TEST BED FOR AC/DC POWER FLOW STUDIES

In this chapter, a hardware test bed is presented for three-phase AC/DC power system analysis. It consists of a flexible three-phase AC/DC network with three types of AC/DC converters. The test bed can be used to explore characteristics of various types of converters and to study AC/DC power flow in balanced and unbalanced systems. Mathematical converter models and AC/DC power flow analysis tools can also be validated using the test bed.

AC/DC power system hardware platforms are desired for research and education purposes. In [36], a laboratory has been built for power quality analysis. Additional power quality test systems have been proposed in [37][38][39]. However, AC/DC power system studies were not the focus of the above laboratories. In [40][41], power distribution system laboratories have been developed for AC distribution system analysis, such as power flow studies. Also in [41], AC/DC power system studies can be performed. In this thesis, delta-connected power converter models were proposed for distribution system power flow studies. They were incorporated in a three-phase sequential and a unified power flow solvers and were validated using steady-state simulations. Hardware tests are desired to validate accuracies of the models and the solvers.

The test bed presented in this chapter provides a flexible hardware platform for unbalanced AC/DC system analysis. Three types of three-phase converters are available: (i) a full bridge thyristor converter, (ii) a full bridge diode rectifier, and (iii) a variable

frequency AC/DC/AC converter. The variable frequency converter consists of a diode rectifier, a LC low-pass filter and a PWM inverter. The test bed also contains a three-phase multi-tap line and adjustable AC and DC loads. As such, balanced or unbalanced AC/DC systems can be set up for power flow studies.

This chapter is organized as follows. First, the design of the test bed is illustrated with a focus on the variable frequency converter. Second, hardware tests on AC/DC power flow are presented for unbalanced systems with the three types of converters respectively. In order to verify the hardware test results, the test systems are developed in MATLAB Simulink using SimPowerSystems Toolbox. Time domain simulations are performed and the resulting AC and DC voltages, currents, and power are compared with those obtained from the hardware tests. In addition, the sequential and unified power flow solvers in Chapter 3 and Chapter 4 are applied to the test systems for steady-state analysis using the delta-connected converter models. The steady-state power flow results, e.g., bus voltages and line currents, are compared with those obtained from the hardware tests to validate the converter models and the power flow solvers.

5.1 Three-Phase AC/DC System Hardware Test Bed

A three-phase AC/DC system hardware test bed was developed for balanced and unbalanced AC/DC power flow studies. It consists of the following components:

- A 208 V_{LL} power supply and a three-phase, Wye-ground/Wye autotransformer
- A three-phase line with a 7-tap reactor on each phase (0.5 / 1.0 / 2.0 / 3.0 / 6.0 / 12.0 / 24.0 Ohms)
- A three-phase diode rectifier, a thyristor converter, and a variable frequency converter
- A multi-tap DC inductor, L_{dc}, a multi-tap DC capacitor, C_{dc}, and adjustable resistive DC loads, R_{dc}
- Three-phase adjustable resistive, R_p, inductive, L_p, and capacitive, C_p, AC loads, $p \in \{a,b,c\}$

Two generic system setups on the test bed are shown in Figure 5.1 and Figure 5.2. Photographs of the actual hardware are provided in Appendix E and Appendix F.

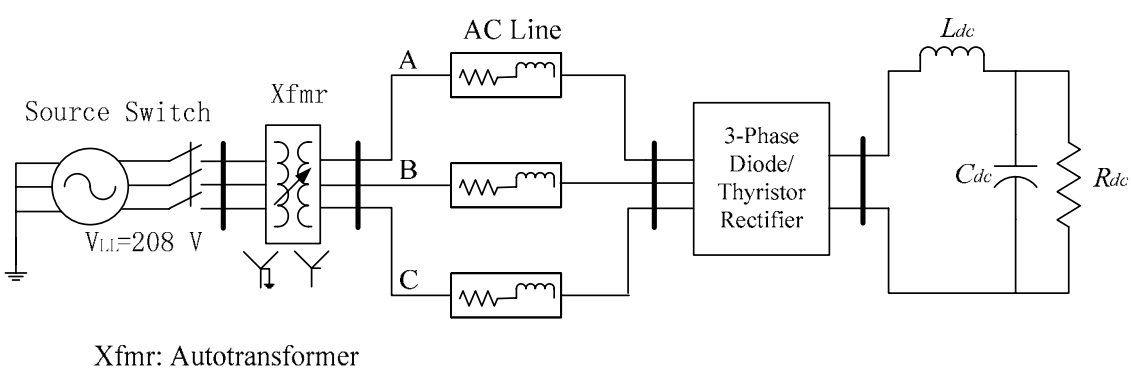


Figure 5.1 An AC/DC system setup with a three-phase diode rectifier/thyristor converter on the test bed

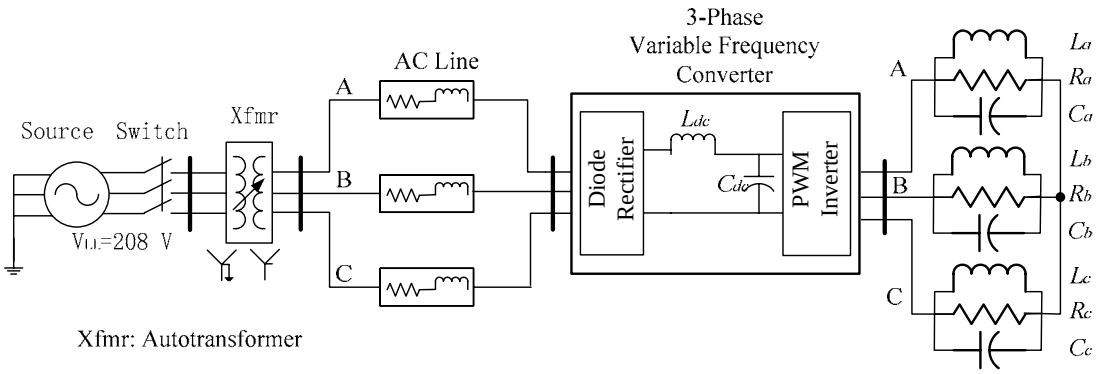


Figure 5.2 An AC/DC system setup with a three-phase variable frequency converter on the test bed

In the test bed, three-phase, 208 V_{LL}, 60 Hz, AC power is fed to the AC/DC system through a three-phase autotransformer for safety reasons. The output of the transformer is connected to three reactors, which model a three-phase line. Thus, the line can be manually configured to be balanced or unbalanced. The AC power is fed into a three-phase converter through the line. Three types of three-phase converters are available:

- a full-bridge thyristor converter module (208 V, 100 A) developed in Center for Electric Power Engineering (CEPE) at Drexel University [40];
- an off-the-shelf full-bridge diode rectifier (600 V, 100A, Fuji 6RI100E [43]);
- a specially designed variable frequency converter (208 V, 100 A) consisting of a diode rectifier and a PWM Insulated-Gate-Bipolar-Transistor (IGBT) inverter.

Carbon filament light bulbs are used as resistive loads. Multi-tap inductors and capacitors are also available for AC loads or DC filtering devices. Next, the design of the variable frequency converter is presented.

5.2 Three-Phase Variable Frequency Converter

A three-phase variable frequency converter was designed for AC/DC power flow studies. A block diagram of the converter is shown in Figure 5.3. Details of the hardware setup are provided in Appendix F.

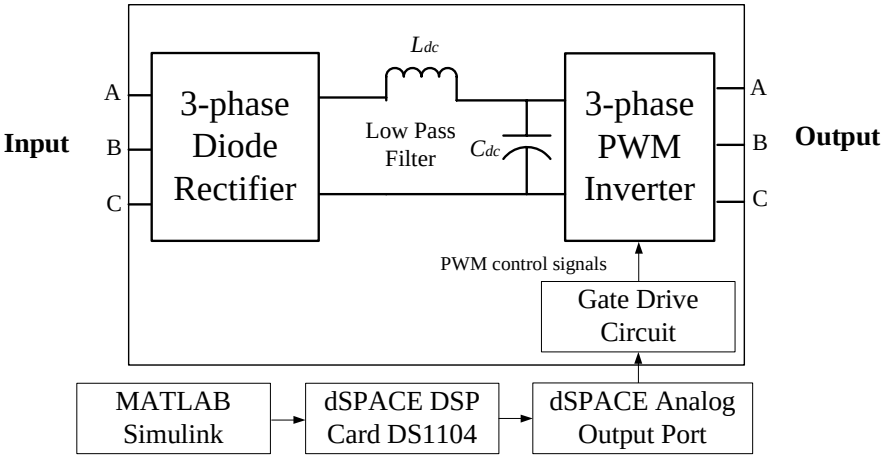


Figure 5.3 The block diagram of the three-phase AC/DC/AC variable frequency converter

The three-phase converter consists of the following three stages:

- AC/DC power rectification using a diode rectifier
- DC harmonics filtering using a LC low pass filter
- DC/AC variable frequency inversion using a PWM inverter

At the rectifier stage, a Fuji Electric 6RI100E series rectifier is used. This is a single unit, three-phase full bridge rectifier. It is capable of 100 A continuous output at up to 600 V.

The DC filter stage consists of a LC low pass filter, which contains a hand wrapped inductor and a capacitor bank with multiple commercially available capacitors in parallel. The inductor was hand wrapped because of high current requirement (up to 100 A). It

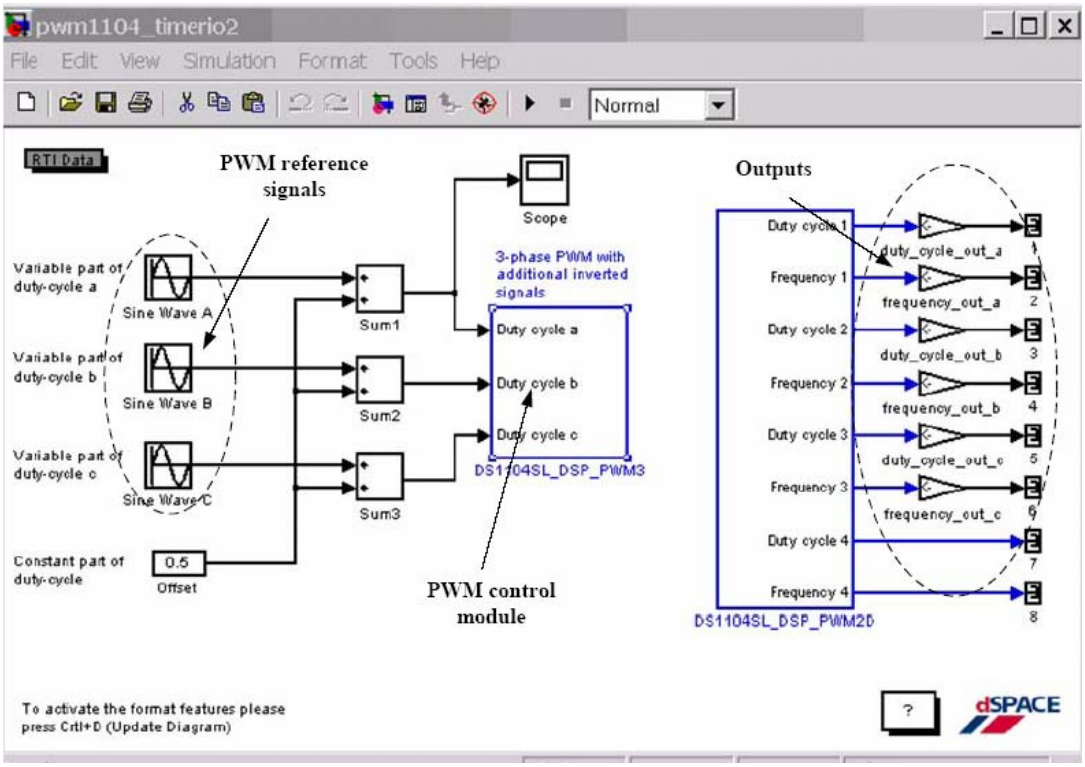
was tested at various current levels and the average inductance is 6.41 mH with a standard deviation of 0.28 mH. DC capacitors were then selected with total capacitance of 18600 uF. They hold a nearly constant DC voltage at the PWM inverter DC bus with maximal peak-to-peak ripples of 0.2 V at 280 V (0.07%).

At the inverter stage, a three-phase PWM inverter was designed and constructed using three dual IGBTs (PowerEX CM100DU-12F) [44]. They are rated at 100 A continuous output at up to 600 V. In order to operate the IGBTs, a control system was developed using a real-time PWM controller kit (dSPACE DS1104) [45]. This kit integrates a variety of control hardware and software into a package providing a wide range of applications. It has a built-in PWM DSP controller generating PWM control signals and acquiring feedback signals. The PWM switching program was developed in MATLAB Simulink. A screen capture of the Simulink control circuit is shown in Figure 5.4.a. The fundamental frequency, the switching frequency, and the modulation ratios of the PWM control signals can be conveniently set in the PWM inverter control module in Figure 5.4.b.

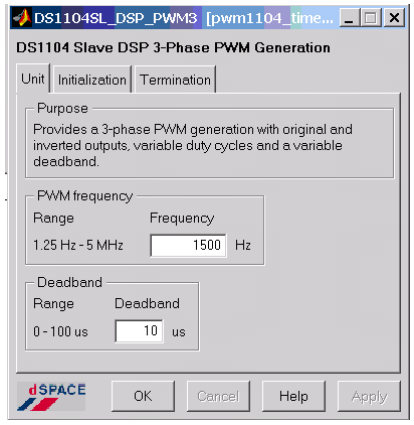
The control signals are downloaded from MATLAB Simulink to the dSPACE card and then fed into an IGBT drive circuit (PowerEX BG2B) [46]. The drive circuit amplifies the control signals to an appropriate voltage level (-8 V / +15 V) to operate the IGBTs. It also isolates the control circuit from the IGBTs for short circuit protection.

Using this variable frequency converter as well as the thyristor converter and the diode rectifier, unbalanced AC/DC systems can be set up on the test bed for power flow

studies. The unbalanced delta-connected converter models proposed in Chapter 2 can be validated. Next, both hardware experiments and corresponding software simulations are presented for AC/DC power flow studies.



(a)



(b)

Figure 5.4 The PWM inverter control circuit (a) and PWM control module (b) in MATLAB Simulink for the dSPACE DS1104 DSP card

5.3 AC/DC Power Flow Studies using a Thyristor Converter and a Diode Rectifier

Three-phase AC/DC power flow was first studied using the test bed setup shown in Figure 5.1. Since thyristor converters and diode rectifiers have similar properties, the following two cases are presented in this subsection:

Case 1: A 3-bus 3-phase AC/DC system with the thyristor converter

Case 2: A 3-bus 3-phase AC/DC system with the diode rectifier

For evaluation purposes, unbalanced networks are created using the following settings for the three reactors in both cases:

Phase A: 0.5 Ohms, *Phase B: 1 Ohm,* *Phase C: 2 Ohms*

Please note that the reactors do not represent lines in real systems. They can be considered as the internal impedance of the Thevenin equivalent circuit for unbalanced AC systems. The reactors' impedance is calculated using the hardware test results.

The test procedure was illustrated in Appendix E. During the tests, AC and DC voltages and currents were measured and recorded at each bus using the following equipment with accuracies in percentage from corresponding specification sheets:

- Four 500 V : 1 V differential voltage probes (Tektronix P5200, $\pm 3\%$) [47]
- Two 150 A current probes (Tektronix TCP303) and two 5 A : 1 V current amplifiers (Tektronix TCPA300, $\pm 1\%$) [48];
- One 100 MHz 4-channel digital oscilloscope (Tektronix TDS3014, $\pm 2\%$) [49];

Using the voltage probes, the three-phase voltages at individual buses were measured simultaneously. But voltages at different buses were measured at different times. Using the two current probes, only currents on phase *a* and phase *b* were measurement simultaneously. Although, all signals cannot be measured simultaneously, the transformer's output voltages were kept constant when the measurements were taken at different times.

The recorded data was saved in EXCEL spreadsheets. MATLAB programs were developed to analyze the data numerically. An FFT function from MATLAB was used to calculate magnitudes and phase angles of the measured voltages and currents at various frequencies. It is assumed that the measured steady-state bus voltages and line currents are constant. As such, the line impedance and load impedance can be calculated using the bus voltages and line currents measured at different times. It is noted that the line impedance can also be determined by measuring the voltage across the line and the line current simultaneously. Tests have shown that the difference of the calculated impedance using the above two methods is less than 0.01 Ohms. In order to keep all measurements in short time, the first method was used during the tests.

Time domain simulations have been performed to verify the hardware test results. Steady-state power flow analysis has also been performed and compared with the hardware results to validate the converter models and the power flow solvers.

5.3.1 3-Bus Unbalanced AC/DC System with a Thyristor Converter

In Case 1, the three-phase thyristor converter was used in the test bed to study power flow in an unbalanced AC/DC system as shown in Figure 5.5.

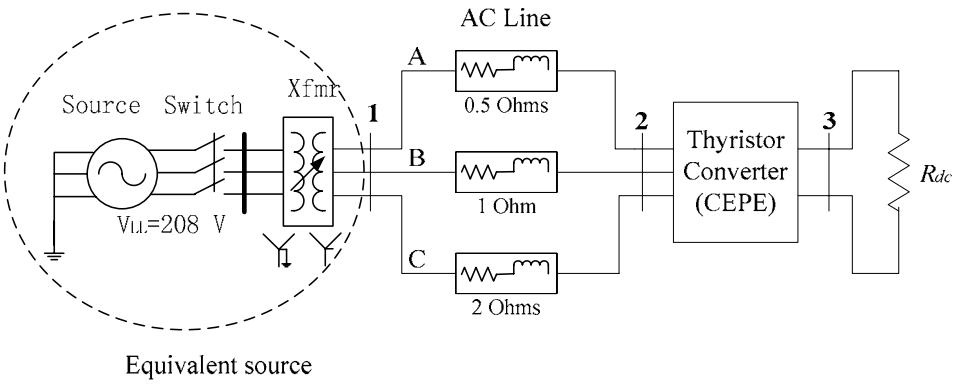


Figure 5.5 The 3-bus unbalanced AC/DC system with a three-phase thyristor converter

It is noted that the parameters of the autotransformer, such as impedance and input/output ratios, have not been rigorously tested. For power flow study purposes, the AC power supply and the autotransformer are integrated into an equivalent ideal source with constant voltages. The voltages are equal to the measured voltages at the autotransformer output in the hardware tests. The thyristor converter is operated in the rectifier mode by a control card (PTR6000-208) [50] using equi-distant control. The firing angles can be altered manually and are 120 degrees apart among the three phases. There is a resistive DC load at the output of the thyristor converter.

5.3.1.1 Hardware Test Results

The hardware tests were performed at 208 V_{LL}. The three-phase AC and DC voltages and currents were measured at bus 1, bus 2, and bus 3. The voltage and current waveforms were plotted in MATLAB using the measured data and are shown in Figure 5.6 to Figure 5.8, where $p \in \{a,b,c\}$.

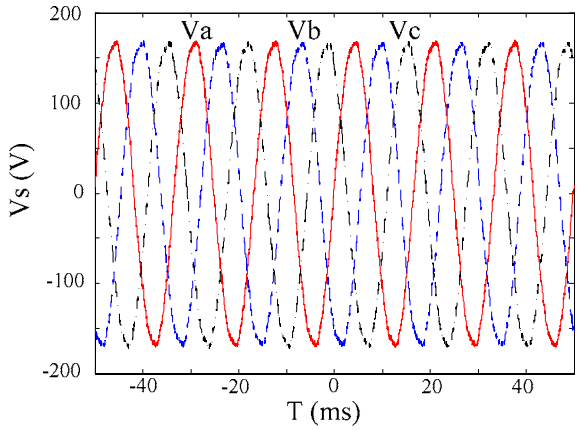


Figure 5.6 Waveforms of the 3-phase line-to-neutral voltages at bus 1 in the 3-bus AC/DC system with a thyristor converter

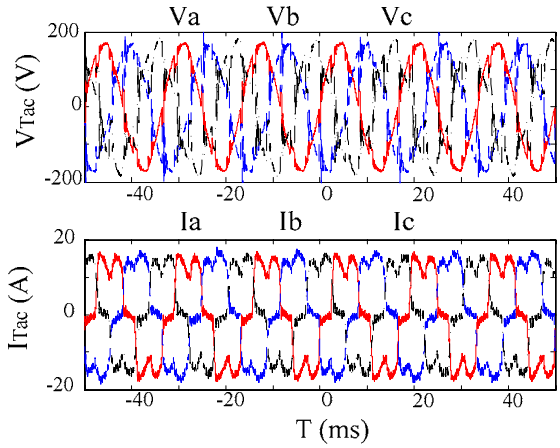


Figure 5.7 Waveforms of V_T^p (top) and I_T^p (bottom) at bus 2 in the 3-bus AC/DC system with a thyristor converter

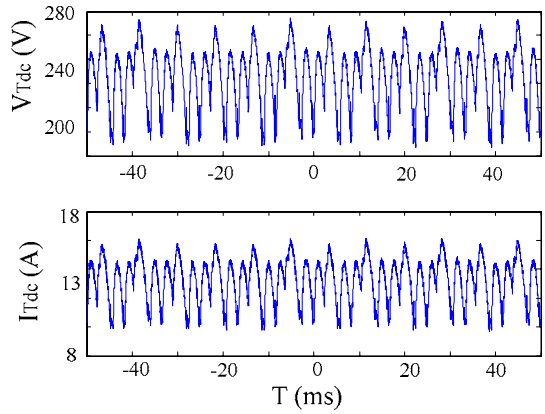


Figure 5.8 Waveforms of $V_{T,dc}$ (top) and $I_{T,dc}^{3\phi}$ (bottom) at bus 3 in the 3-bus AC/DC system with a thyristor converter

Remarks:

- In Figure 5.6, the voltages at bus 1 are close to pure sinusoidal waves because the source holds the voltages;
- In Figure 5.7, V_T^p are distorted because of the commutation of the thyristor converter and transients generated by firing thyristors. I_T^p is much distorted and unbalanced caused by the thyristor converter;
- In Figure 5.8, $V_{T,dc}$ and $I_{T,dc}^{3\phi}$ have the same shapes because there is only a resistive DC load in the DC network.

A MATLAB program was developed to analyze the AC and DC signals. It is noted that the converter AC bus is bus 2 and its DC bus is bus 3. Thus, power flow related to the converter can be calculated. In addition, the converter firing angles, α_T^p, and commutation angles, u_T^p were determined using the converter AC voltage waveforms. The power flow results are provided in the following tables:

- Table 5.1 presents the magnitudes and phase angles of the AC (60Hz) and DC voltages at bus 1 to bus 3;
- Table 5.2 presents the magnitudes and phase angles of the AC (60Hz) and DC currents in line 1-2 and the DC load. The source currents and the converter AC currents are equal to the currents in line 1-2;
- Table 5.3 presents the AC and DC voltages, currents, and power related to the thyristor converter as well as α_T^p and u_T^p.

Please note that the voltage on phase *a* at bus 1 was chosen as the reference.

Table 5.1 Voltage profile in the 3-bus AC/DC system with a thyristor converter from hardware tests, V: [V, deg]

Bus #	V_a	V_b	V_c
1	$119.0974\angle 0^o$	$119.0300\angle -120.04^o$	$120.4284\angle 120.04^o$
2	$114.9246\angle -2.09^o$	$111.7571\angle -123.80^o$	$106.7714\angle 112.0311^o$
3(DC)	209.0531		

Table 5.2 Current profile in the 3-bus AC/DC system with a thyristor converter from hardware tests, I: [A, deg]

Line/Load	I_a	I_b	I_c
1-2	$9.5345\angle -33.70^o$	$9.8691\angle -156.18^o$	$9.3056\angle 83.12^o$
DC load	12.5498		

Table 5.3 AC and DC voltages, currents, and power in the 3-phase thyristor converter from hardware tests, V: [V, deg], I: [A, deg], S: [W,Var], α ,u : [deg]

Parameters	*AC Values on Bus 2*		
	Phase A	*Phase B*	*Phase C*
V_T^p	$114.9246\angle -2.09^o$	$111.7571\angle -123.80^o$	$106.7714\angle 112.0311^o$
I_T^p	$9.5345\angle -33.70^o$	$9.8691\angle -156.18^o$	$9.3056\angle 83.12^o$
S_T^p	933.2+j574.2	931.5+j590.6	869.7+j480.3

α_T^p	32.4	152.43	270.83
u_T^p	9.80	5.20	9.5
	DC Values on Bus 3		
$V_{T,dc}$	209.0531		
$I_{T,dc}^{3\phi}$	12.5498		
$P_{T,dc}^{3\phi}$	2623.6		

Remarks:

- The voltages at bus 1 are approximately balanced. The thyristor converter AC voltages, V_T^p, are unbalanced because of the unbalanced line. The unbalanced V_T^p resulted in the unbalanced AC currents, I_T^p, and power, S_T^p;
- V_T^p and I_T^p have different imbalance characteristics. $\left|V_T^a\right|$ is larger than $\left|V_T^b\right|$ and $\left|V_T^c\right|$. But $\left|I_T^b\right|$ is larger than $\left|I_T^a\right|$ and $\left|I_T^c\right|$. This is because I_T^p depend on the line-to-line voltages and the control of the thyristor converter;
- The difference among the firing angles is close but not equal to 120 degrees. It is attributed to the distortions in the AC voltages and the accuracy of the converter control card;
- The commutation angles are not equal because of the unbalanced line and unbalanced converter AC voltages;
- Real power loss of the three-phase thyristor converter is

$$\left(1-\frac{P_{T,dc}^{3\phi}}{\sum_{p\in\{a,b,c\}} real\left(S_T^p\right)}\right)\cdot 100\% = 4.06\%$$

In order to verify the hardware test results using time domain analysis, the following parameters were also calculated:

- Table 5.4 presents voltages up to the 7th harmonic at bus 1. Voltages over 7th harmonics were significantly smaller and were ignored.
- Table 5.5 presents line impedance at 60 Hz, Z_{line}, and DC load resistance, R_{dc}.

Table 5.4 Voltages at bus 1 in the 3-bus AC/DC system with a thyristor converter from hardware tests, V: [V, deg], Freq: [Hz]

Frequency	V_a	V_b	V_c
0	8.5702	12.6884	7.6622
60	$119.0974\angle 0^o$	$119.0300\angle -120.04^o$	$120.4284\angle 120.04^o$
180	$0.9139\angle 80.64^o$	$1.1852\angle 23.72^o$	$0.5417\angle 107.63^o$
300	$0.8768\angle 209.82^o$	$0.8536\angle -15.99^o$	$0.6489\angle 91.23^o$
420	$0.9621\angle 107.17^o$	$0.8280\angle -32.55^o$	$0.6605\angle 216.91^o$

Table 5.5 Line and load impedance in the 3-bus AC/DC system with a thyristor converter from hardware tests, Z, R: [Ω]

Parameters	*Phase A*	*Phase B*	*Phase C*
Z_{line}	0.1301+j0.6082	0.1415+j1.0969	0.2801+j2.2566
R_{dc}	16.6579		

Remarks:

- In Table 5.4, the 3rd harmonic is relatively large compared to 5th and 7th harmonics. This is because that unbalanced converters may generate all odd harmonics in AC systems instead of $(6k\pm 1)f_1$, k is an integer number,

harmonics from balanced converters, where f_1 is the fundamental frequency;

- In Table 5.5, the line impedances are consistent with the tap-settings.

Next, time domain analysis on the 3-bus unbalanced AC/DC system is presented.

5.3.1.2 Time Domain Simulation Results

The 3-bus unbalanced AC/DC system tested on the test bed was studied in time domain using MATLAB Simulink. The circuit was built using the SimPowerSystems Toolbox and shown in Figure 5.9.

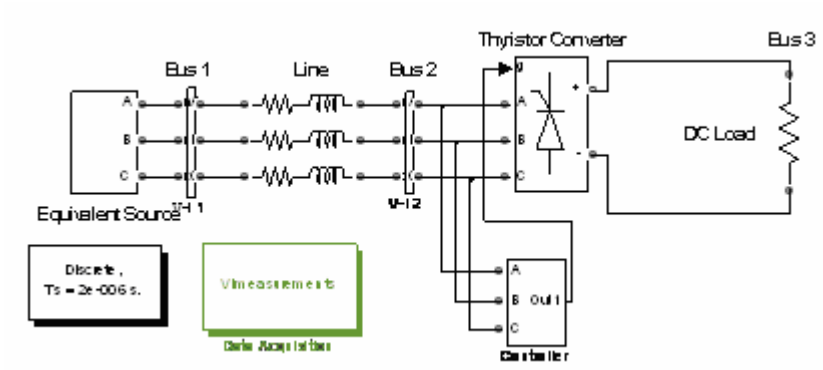


Figure 5.9 The Simulink circuit of the 3-bus AC/DC system with a thyristor converter

The parameters of the circuit components are chosen as follows:

- the voltages of the equivalent source included up to 7th harmonic from Table 5.4;
- the impedances of the AC line and DC load were equal to those in Table 5.5;
- the thyristor converter was operated using equi-distant control. The firing angle was equal to 32.4 degrees on phase *a*;
- the converter forward voltage was set to 1 V and the internal impedance was set to 0.28 Ohms so that the converter loss percentage matched the hardware test

results.

A discrete solver was used to solve the circuit in time domain with a step size of 2 us. Each simulation has been run for 0.1 seconds, at which the initial transients diminished. The AC and DC voltages and currents at bus 1, bus 2, and bus 3 were measured and calculated using measurement blocks from the SimPowerSystems Toolbox. Since the voltages at bus 1 were specified, only the parameters at bus 2 and bus 3, which are the converter AC and DC buses respectively, are provided in Table 5.6.

Table 5.6 AC and DC voltages, currents, and power in the thyristor converter from time domain analysis, V: [V, deg], I: [A, deg], S: [W,Var]

Parameters	*AC Values on Bus 2*		
	Phase A	*Phase B*	*Phase C*
V_T^p	115.0268∠-2.09^o	111.8071∠-124.03^o	106.2686∠111.81^o
I_T^p	9.4816∠-32.61^o	10.1960∠-154.33^o	9.6031∠82.80^o
S_T^p	939.48+j553.94	984.32+j575.06	892.53+j494.81
	DC Values on Bus 3		
$V_{T,dc}$	209.0296		
$I_{T,dc}^{3\phi}$	12.5483		
$P_{T,dc}^{3\phi}$	2622.98		

The difference of the voltages, currents, and power obtained from time domain analysis and the hardware tests was calculated using (5.1) and shown in Table 5.7:

$$\Delta|X| = \left|\frac{|X_1| - |X_2|}{|X_2|}\right| \cdot 100\% \tag{5.1}$$

where:

X: V, I, S

X_1: values obtained from time domain analysis

X_2: values obtained from hardware tests

Table 5.7 Difference of AC and DC voltages, currents, and power on the thyristor converter between time domain analysis and hardware tests, ΔV, ΔI, ΔS: [%]

Parameters	*Phase A*	*Phase B*	*Phase C*
$\Delta\left\|V_T^p\right\|$	0.09	0.04	0.47
$\Delta\left\|I_T^p\right\|$	0.55	3.31	3.19
$\Delta\left\|S_T^p\right\|$	0.47	**3.36**	2.71
$\Delta V_{T,dc}$	0.01		
$\Delta I_{T,dc}^{3\phi}$	0.01		
$\Delta P_{T,dc}^{3\phi}$	0.02		

Error Analysis:

The maximal difference is 3.36%. It is mainly attributed to the following sources of errors in the hardware parameters:

- Non-simultaneous measurements and fluctuations of system parameters, such as the source voltages;
- The accuracies of the measurement devices.

Other factors affecting the results include the unknown thyristor internal impedance and non-perfect equi-distant control of the thyristor converter.

Overall, it can be seen that the power flow results from time domain analysis and hardware tests are consistent. Next, the delta-connected model and steady-state power flow solvers will be validated using the 3-bus AC/DC system in steady-state analysis.

5.3.1.3 Steady-State Power Flow Analysis Results

For steady-state analysis, the sequential and unified power flow solvers from Chapter 3 and Chapter 4 were applied to the 3-bus unbalanced AC/DC system. The system parameters were equal to those obtained from the hardware tests. The source voltages at bus 1 only included the voltages at 60 Hz. The thyristor converter was operated using equi-distant control and the firing angle was equal to 32.4 degrees on phase *a*. The real power loss of the converter was set to 4.06% from the hardware tests.

The three-phase thyristor converter was modeled using three, delta-connected, single-phase thyristor converters. The participation coefficients, $\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$, and equivalence coefficients, K_T^{LL}, were used to make the model equivalent to the three-phase converter. These coefficients were calculated and provided in Table 5.8.

Table 5.8 Coefficients of the thyristor converter model from steady-state analysis

Parameters	*Line AB*	*Line BC*	*Line CA*
$\lambda_{T,I}^{LL}$	0.3521	0.3301	0.3179
$\lambda_{T,P}^{LL}$	0.3654	0.3264	0.3082
K_T^{LL}	1.3402	1.3482	1.3504

Remarks

- $\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$ are unbalanced in the single-phase converters because of unbalanced converter AC voltages caused by the unbalanced network;
- K_T^{LL} are unbalanced because the linear conduction angles, which are equal to the commutation angles, of the single-phase converters are unbalanced.

Using the converter model, AC/DC power flow was solved using the sequential and unified solvers. Both solvers obtained the same bus voltages. The results are provided in the following tables:

- Table 5.9 presents the AC and DC voltages, currents, and power related to the thyristor converter;
- Table 5.10 presents the difference of the voltages, currents, and power between steady-state analysis and hardware tests. The difference was obtained using (5.1).

Table 5.9 AC and DC voltages, currents, and power in the 3-phase thyristor converter from steady-state analysis, V: [V, deg], I: [A, deg], S: [W,Var]

Parameters	*AC Values on Bus 2*		
	Phase A	*Phase B*	*Phase C*
V_T^p	$114.8163\angle\text{-}2.09^o$	$111.2067\angle\text{-}124.27^o$	$106.2631\angle 111.97^o$
I_T^p	$9.7591\angle\text{-}33.45^o$	$10.2412\angle\text{-}157.12^o$	$9.3136\angle 80.72^o$
S_T^p	953.17 + j589.07	941.27 + j641.15	850.21 + j506.59
	DC Values on Bus 3		
$V_{T,dc}$	209.4374		
$I_{T,dc}^{3\phi}$	12.5728		

$P_{T,dc}^{3\phi}$	2633.2

Table 5.10 Difference of AC and DC voltages, currents, and power in the 3-phase thyristor converter between steady-state analysis and hardware tests, ΔV, ΔI, ΔS: [%]

Parameters	*Phase A*	*Phase B*	*Phase C*
$\Delta\left\|V_T^p\right\|$	0.09	0.49	0.48
$\Delta\left\|I_T^p\right\|$	2.36	**3.77**	0.09
$\Delta\left\|S_T^p\right\|$	2.26	3.25	0.38
$\Delta V_{T,dc}$	0.18		
$\Delta I_{T,dc}^{3\phi}$	0.18		
$\Delta P_{T,dc}^{3\phi}$	0.37		

Remarks:

- The difference in the voltages is relatively small and the difference in the current and power is relatively large;
- The maximal difference is 3.77% in $\Delta\left\|I_T^p\right\|$. It is slightly larger than the difference (3.36%) between time domain simulations and hardware tests.

Error Analysis:

In addition to the sources of errors in the hardware parameters, the discrepancy is also attributed to the following assumptions in the delta-connected converter model:

- the DC currents in the single-phase converters are linear during commutation of the 3-phase converter;
- loss percentages of the single-phase converter in the model are equal.

These assumptions introduced additional errors into the AC currents and power in the three-phase converter compared to the hardware test results.

In both time domain analysis and steady-state power flow analysis, the power flow results are close to those obtained from the hardware tests. In the following subsection, hardware tests of AC/DC power flow are performed using the test bed for a 3-bus AC/DC system with a three-phase diode rectifier. Time domain analysis and steady-state analysis are also performed to verify the hardware test results and to validate the delta-connected diode rectifier model and the power flow solvers.

5.3.2 3-Bus Unbalanced AC/DC System with a Diode Rectifier

In Case 2, the diode rectifier was used in the test bed to study power flow in a 3-bus unbalanced AC/DC system. The system setup is shown in Figure 5.10. The source and the autotransformer were integrated into an equivalent ideal source with specified voltages. There was a resistive DC load at the output of the diode rectifier.

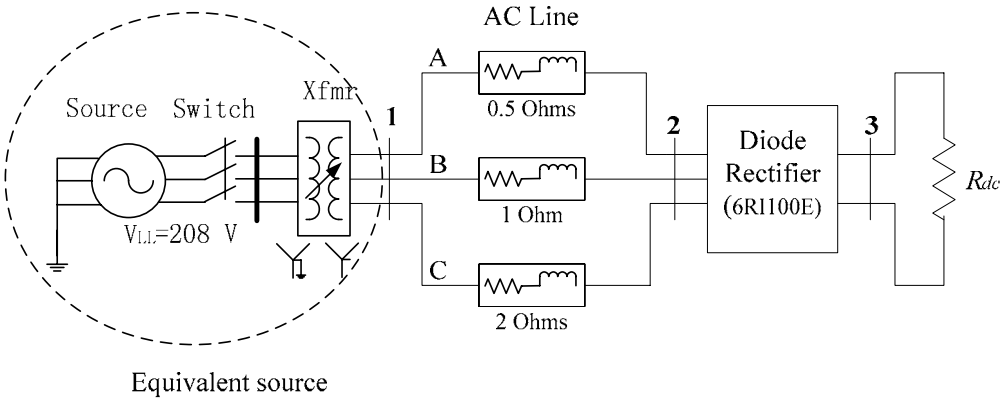


Figure 5.10 The 3-bus AC/DC system with a three-phase diode rectifier

5.3.2.1 Hardware Test Results

Hardware tests were performed at 208 V_{LL}. AC and DC voltages and currents were measured at bus 1, bus 2, and bus 3. The waveforms were plotted using the measured data in MATLAB and are shown in Figure 5.11 to Figure 5.13.

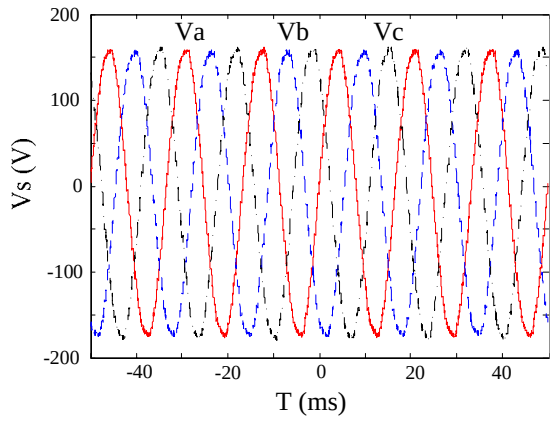


Figure 5.11 Waveforms of the 3-phase line-to-neutral voltages at bus 1 in the 3-bus AC/DC system with a diode rectifier

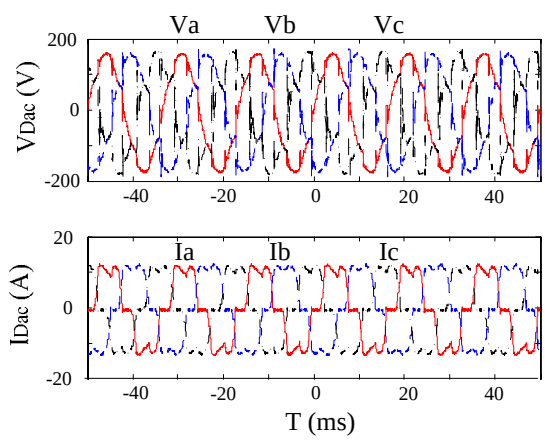


Figure 5.12 Waveforms of V_D^p (top) and I_D^p (bottom) at bus 2 in the 3-bus AC/DC system with a diode rectifier

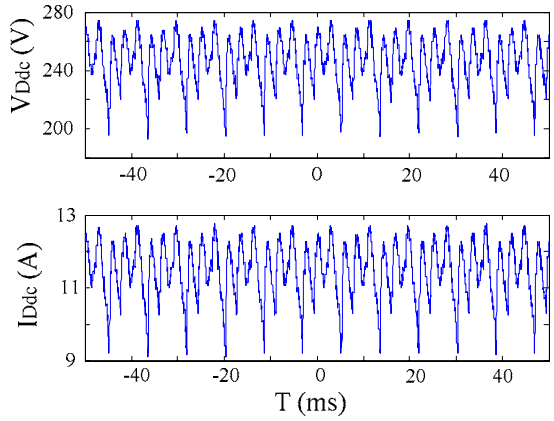


Figure 5.13 Waveforms of $V_{D,dc}$ (top) and $I_{D,dc}^{3\phi}$ (bottom) at bus 3 in the 3-bus AC/DC system with a diode rectifier

Remarks:

- The voltage and current waveforms are similar to those in the AC/DC system with a thyristor converter.

Using the MATLAB program developed with the test bed, the following power flow results are obtained:

- Table 5.11 presents the magnitudes and phase angles of the AC (60Hz) and DC voltages at bus 1 to bus 3;
- Table 5.12 presents the magnitudes and phase angles of the AC (60Hz) and DC currents in the line 1-2 and the DC load;
- Table 5.13 presents the AC and DC voltages, currents, and power related to the diode rectifier and the commutation angles.

Table 5.11 Voltage profile in the 3-bus AC/DC system with a diode rectifier from hardware tests, V: [V, deg]

Bus #	V_a	V_b	V_c
1	$118.1319\angle 0^o$	$118.5764\angle -120.20^o$	$118.9372\angle 120.59^o$
2	$115.8062\angle -2.68^o$	$114.8582\angle -125.34^o$	$111.8674\angle 111.10^o$
3 (DC)	247.0683		

Table 5.12 Current profile in the 3-bus AC/DC system with a diode rectifier from hardware tests, I: [A, deg]

Line/Load	I_a	I_b	I_c
1-2	$8.6458\angle -14.46^o$	$9.3034\angle -136.06^o$	$8.8301\angle 101.08^o$
3-ground (DC)	11.4815		

Table 5.13 AC and DC voltages, currents, and power in the diode rectifier from hardware tests, V: [V, deg], I: [A, deg], S: [W,Var], u : [deg]

Parameters	*AC Values on Bus 2*		
	Phase A	*Phase B*	*Phase C*
V_D^p	$115.8062\angle -2.68^o$	$114.8582\angle -125.34^o$	$111.8674\angle 111.10^o$
I_D^p	$8.6458\angle -14.46^o$	$9.3034\angle -136.06^o$	$8.8301\angle 101.08^o$
S_D^p	980.0740 + j204.7795	1049.9226+ j198.7901	972.7273+j171.9228
u_D^p	25	21	23
	DC Values on Bus 3		
$V_{D,dc}$	247.0683		
$I_{D,dc}^{3\phi}$	11.4815		
$P_{D,dc}^{3\phi}$	2836.7233		

Remarks:

- In Table 5.13, the AC voltages and currents of the diode rectifier have similar properties as those of the unbalanced thyristor converter in Case 1;

- Real power loss of the three-phase diode rectifier is 5.33%.

For simulation purposes, voltages up to the 7th harmonic were calculated at bus 1 and shown in Table 5.14. Line impedance at 60 Hz and DC load resistance were calculated and provided in Table 5.15.

Table 5.14 Voltages at bus 1 in the 3-bus AC/DC system with a diode rectifier from hardware tests, V: [V, deg], Freq: [Hz]

Frequency	V_a	V_b	V_c
0	8.0027	8.5188	8.8522
60	$118.1319\angle 0^o$	$118.5764\angle -120.20^o$	$118.9372\angle 120.59^o$
180	$1.2792\angle 75.1711^o$	$1.5587\angle 37.1505^o$	$0.7345\angle 101.397^o$
300	$0.5180\angle 220.1061^o$	$1.0426\angle -28.0433^o$	$0.6748\angle 140.4118^o$
420	$1.1604\angle 73.8763^o$	$0.9682\angle -65.1693^o$	$0.9799\angle 184.8491^o$

Table 5.15 Line and load impedance in the 3-bus AC/DC system with a diode rectifier from hardware tests, Z, R: [Ω]

Parameters	*Phase A*	*Phase B*	*Phase C*
Z_{line}	0.1188 + j0.6742	0.1295 + j1.1881	0.2203 + j2.2945
R_{dc}	21.5188		

Next, time domain analysis on the 3-bus AC/DC system is presented.

5.3.2.2 Time Domain Simulation Results

The 3-bus AC/DC system with a diode rectifier was developed in MATLAB Simulink using the SimPowerSystems Toolbox. The circuit is shown in Figure 5.14 with the following parameters:

- The voltages of the equivalent source were equal to those in Table 5.14;
- The impedance of the AC line and DC load are equal to those in Table 5.15;
- For the diode rectifier, the forward voltage was 1 V and the internal impedance was 0.51 Ohms according to the parameters of the three-phase diode rectifier.

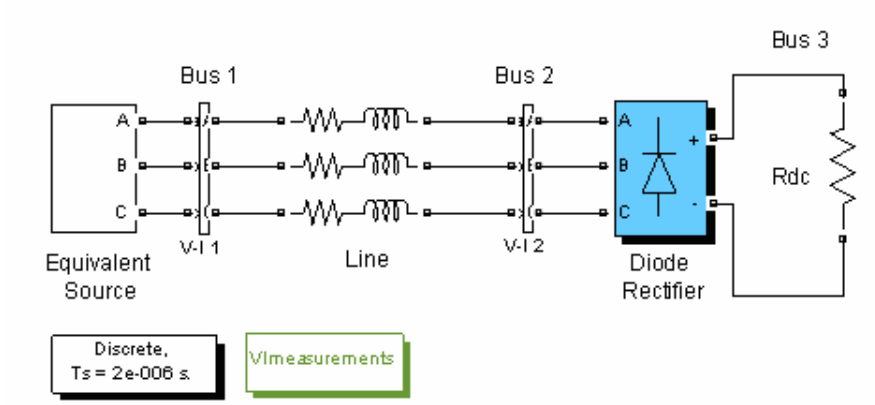


Figure 5.14 The Simulink circuit of the 3-bus AC/DC system with a diode rectifier

A discrete solver was used to solve the circuit in time domain with a step size of 2 us. Each simulation has been run for 0.1 seconds. The power flow results are provided in the following tables:

- Table 5.16 presents the AC and DC voltages, currents, and power related to the diode rectifier;
- Table 5.17 presents the difference of the voltages, currents, and power related to the diode rectifier between time domain analysis and hardware tests. The difference was calculated using (5.1).

Table 5.16 AC and DC voltages, currents, and power in the 3-bus AC/DC system from time domain analysis, V: [V, deg], I: [A, deg], S: [W,Var]

Parameters	*AC Values on Bus 2*		
	Phase A	*Phase B*	*Phase C*
V_D^p	$115.8022\angle -2.6718^o$	$114.9011\angle -125.3326^o$	$111.9617\angle 111.1250^o$
I_D^p	$8.6631\angle -14.4661^o$	$9.2849\angle -135.8620^o$	$8.8001\angle 101.3035^o$
S_D^p	982.026+j205.0539	1048.8809+j194.9553	970.8339+j168.0673
	DC Values on Bus 3		

$V_{D,dc}$	247.1478
$I_{D,dc}^{3\phi}$	11.4852
$P_{D,dc}^{3\phi}$	2836.7233

Table 5.17 Difference of AC and DC voltages, currents, and power in the diode rectifier between time domain analysis and hardware tests, ΔV, ΔI, ΔS: [%]

Parameters	*Phase A*	*Phase B*	*Phase C*
$\Delta\left\|V_D^p\right\|$	0.003	0.037	0.084
$\Delta\left\|I_D^p\right\|$	0.200	0.198	**0.339**
$\Delta\left\|S_D^p\right\|$	0.1961	0.1622	0.2567
$\Delta V_{D,dc}$	0.032		
$\Delta I_{D,dc}^{3\phi}$	0.032		
$\Delta P_{D,dc}^{3\phi}$	0.064		

Remarks:

- The maximal difference is 0.339%. It is mainly attributed to the non-simultaneous measurements and the accuracies of the measurement devices.

Time domain simulations for unbalanced diode rectifier are more consistent with the hardware test results than the unbalanced thyristor converter. It might because the non-simultaneous measurements were more consistent during the diode rectifier tests. In addition, it is noted that the diode rectifier conducted naturally while the non-ideal equi-distant control on the thyristor converter introduced errors between the hardware tests and time-domain simulations.

5.3.2.2 Steady-State Power Flow Analysis Results

The power flow solvers were validated using the 3-bus unbalanced AC/DC system with a diode rectifier. The same system parameters were used in the power flow solvers as those in the hardware tests. The power flow results were compared with those obtained from the hardware tests and presented in the following tables:

- Table 5.18 presents the participation coefficients, $\lambda_{D,I}^{LL}$, $\lambda_{D,P}^{LL}$, and equivalence coefficients, K_D^{LL} in the diode converter model;
- Table 5.19 presents the diode rectifier AC and DC voltages, currents, and power;
- Table 5.20 presents the difference of the voltages, currents, and power between steady-state analysis and hardware tests. The difference is calculated using (5.1).

Table 5.18 Coefficients of the diode rectifier model from steady-state analysis

Parameters	*Line AB*	*Line BC*	*Line CA*
$\lambda_{D,I}^{LL}$	0.3482	0.3612	0.2906
$\lambda_{D,P}^{LL}$	0.3442	0.3583	0.2975
K_D^{LL}	1.3420	1.3315	1.3517

Table 5.19 AC and DC voltage, currents and power in the 3-phase diode rectifier from steady-state analysis

Parameters	*AC Values on Bus 2*		
	Phase A	*Phase B*	*Phase C*
V_D^p *(V)*	$115.8186\angle -2.69^o$	$114.7955\angle -125.30^o$	$112.1357\angle 111.24^o$
I_D^p *(A)*	$8.7215\angle -14.14^o$	$9.2542\angle -136.50^o$	$8.6783\angle 101.59^o$
S_D^p *(VA)*	990+j200.5	1042.1+j206.3	959.4+j163.2
	DC Values on Bus 3		

$V_{D,dc}$ (V)	246.8656
$I_{D,dc}^{3\phi}$ (A)	11.4721
$P_{D,dc}^{3\phi}$ (W)	2832.1

Table 5.20 Difference of AC and DC voltages, currents, and power in the 3-phase diode rectifier between steady-state analysis and hardware tests, ΔV, ΔI, ΔS: [%]

Parameters	*Phase A*	*Phase B*	*Phase C*
$\Delta\left\|V_D^p\right\|$	0.01	0.05	0.24
$\Delta\left\|I_D^p\right\|$	0.88	0.53	**1.72**
$\Delta\left\|S_D^p\right\|$	0.89	0.58	1.48
$\Delta V_{D,dc}$	0.08		
$\Delta I_{D,dc}^{3\phi}$	0.08		
$\Delta P_{D,dc}^{3\phi}$	0.16		

Remarks:

- The power flow obtained from steady-state analysis is close to the hardware results with the maximal error of 1.72% ;
- The errors in steady-state analysis are larger than those (0.339%) obtained in time domain analysis. This is mainly attributed to the assumptions in the converter model in addition to the non-simultaneous measurements.

From above, it is shown that the power flow solvers provide steady-state power flow solutions that are consistent with the hardware test results. The delta-connected model in the solvers appropriately modeled the three-phase diode rectifier.

5.4 AC/DC Power Flow Studies using a Variable Frequency Converter

AC/DC power flow was also tested in a 5-bus AC/DC-DC/AC unbalanced system using the test bed setup in Figure 5.2. The variable frequency converter was used. The system circuit diagram is shown in Figure 5.15 with the power supply and the autotransformer integrated into an equivalent source.

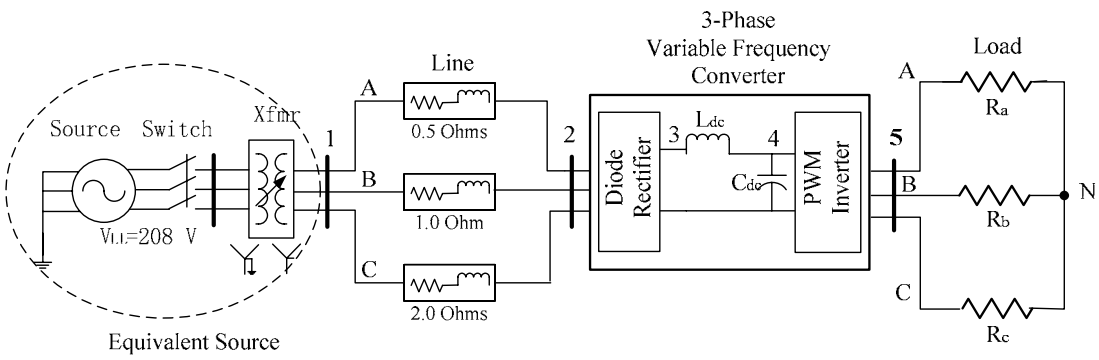


Figure 5.15 The 5-bus AC/DC system using the variable frequency converter

In Figure 5.15, the output of the equivalent source is 120 V_{LL}. The settings of the three-phase line are:

Phase A: 0.5 Ohms, *Phase B: 1.0 Ohm,* *Phase C: 2.0 Ohms*

They were chosen for evaluation purpose only and do not represent actual line parameters. The variable frequency converter supplies a three-phase, wye-connected, ungrounded resistive load. The impedances of the AC line and AC load were calculated using the hardware test results. The test procedure was described in Appendix F. The following parameters were chosen for the PWM inverter:

- the fundamental frequency, f_1, was set to 60 Hz;
- the switching frequency, f_s, was set to 1500 Hz, which is 25 times of f_1. The

PWM inverter output AC voltages contain harmonics at $f_s \pm 2f_1$ and $2f_s \pm f_1$;

- the modulation ratios were equal to 0.8.

During the tests, AC and DC voltages and currents were measured and recorded at each bus using four differential voltage probes (Tektronix P5200, $\pm 3\%$), two current probes (Tektronix TCP303) and one digital oscilloscope (Tektronix TDS3014, $\pm 2\%$).

5.4.1 Hardware Test Results

The AC and DC voltages and currents were measured at bus 1 to bus 5 during the tests. Since the PWM inverter is not grounded, line-to-line voltages were measured at the PWM inverter AC bus (bus5). The waveforms of the AC and DC voltage and currents are shown in Figure 5.16 to Figure 5.20.

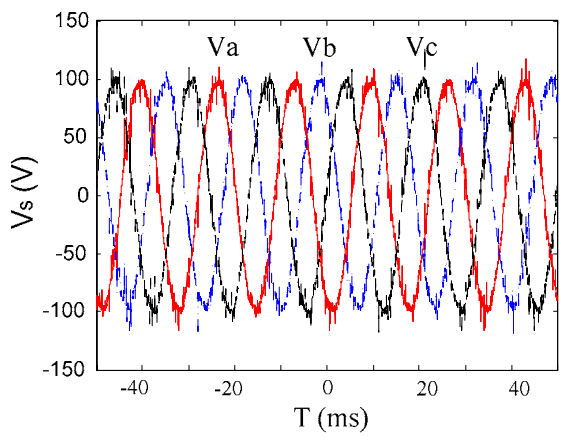


Figure 5.16 Waveforms of the 3-phase line-to-neutral voltages at bus 1 in the 5-bus AC/DC system with a variable frequency converter

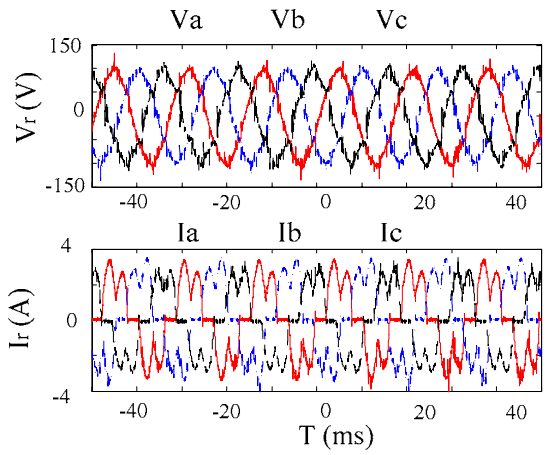


Figure 5.17 Waveforms of V_D^p (top) and I_D^p currents (bottom) at bus 2 in the 5-bus AC/DC system with a variable frequency converter

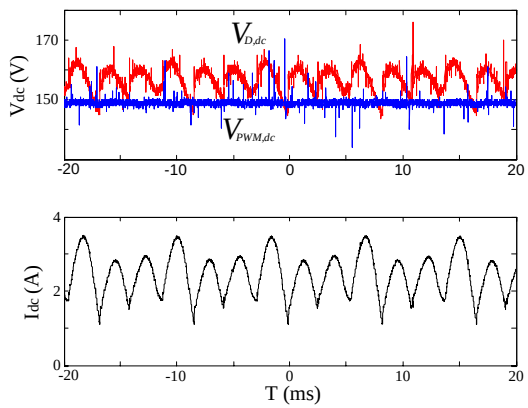


Figure 5.18 Waveforms of $V_{D,dc}$, $V_{PWM,dc}$ (top) and $I_{D,dc}^{3\phi}$ (bottom) at bus 3 and bus 4 in the 5-bus AC/DC system with a variable frequency converter

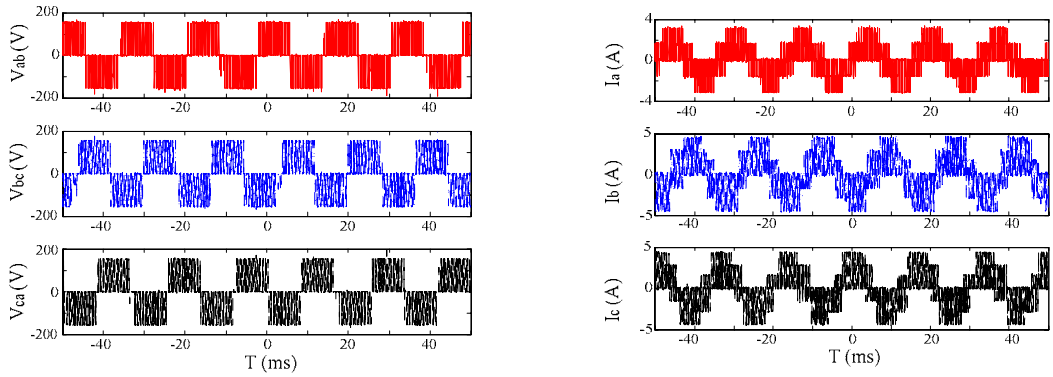


Figure 5.19 Waveforms of V_{PWM}^{LL} (left) and I_{PWM}^{p} (right) at bus 5 in the 5-bus AC/DC system with a variable frequency converter

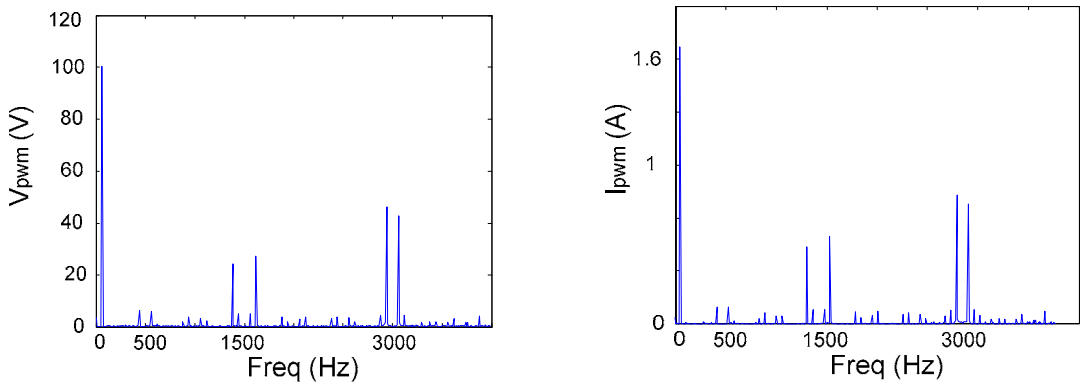


Figure 5.20 FFT of V_{PWM}^{ab} (left) and I_{PWM}^{a} (right) at bus 5 in the 5-bus AC/DC system with a variable frequency converter

Remarks:

- The diode rectifier DC voltage, $V_{D,dc}$, contains large ripples as expected. The PWM inverter DC voltage, $V_{PWM,dc}$, is nearly constant because of the large capacitors. The spikes in $V_{PWM,dc}$ are caused by the switching of IGBTs;
- The DC current is continuous because of the large DC inductor;
- V_{PWM}^{LL} and I_{PWM}^{LL} contains harmonics at high frequencies as expected. The FFT analysis in Figure 5.20 shows that the harmonic frequencies are at $1500 \pm 2 \cdot 60$ Hz and 3000 ± 60 Hz. It is consistent with the system design.

The steady-state voltage and current profiles are provided in Table 5.21 and Table 5.22. All of the voltages and currents are referred to the voltage on phase *a* at bus 1.

Table 5.21 Voltage profile in the 5-bus AC/DC system with a variable frequency converter from hardware tests, V: [V, deg]

Bus #	V_a	V_b	V_c
1	$70.21\angle 0^o$	$70.15\angle -119.95^o$	$69.10\angle 120.30^o$
2	$69.46\angle -0.93^o$	$68.71\angle -121.49^o$	$67.94\angle 117.20^o$
3 (DC)	156.77		
4(DC)	148.90		
Bus #	V_{ab}	V_{bc}	V_{ca}
5	$70.03\angle 30.13^o$	$68.95\angle -90.20^o$	$70.08\angle 150.62^o$
5-N	$49.9980\angle 3.80^o$	$33.0579\angle -110.52^o$	$39.2000\angle 107.08^o$

Table 5.22 Current profile in the 6-bus AC/DC system with a variable frequency converter from hardware tests, I: [A, deg]

Line/Load	I_a	I_b	I_c
1-2	$1.9405\angle -8.50^o$	$2.0610\angle -132.36^o$	$1.8850\angle 106.35^o$
3-4 (DC)	2.5307		
5-N	$1.1619\angle 3.80^o$	$1.8538\angle -110.52^o$	$1.7422\angle 107.08^o$

Remarks:

- The source voltages at bus 1 are nearly balanced;
- The PWM inverter line-to-line AC voltages at bus 5 are unbalanced. It is attributed to the unbalanced voltage drops on the IGBTs caused by the unbalanced load currents;
- The diode rectifier AC currents are unbalanced because of the unbalanced AC voltages applied on the diode rectifier;
- The PWM inverter AC currents are unbalanced because of the unbalanced load;
- The real power loss in the diode rectifier is:

$$\Delta P_{D,loss} = \left[1 - \frac{V_{D,dc} \cdot I_{D,dc}}{\sum_{p \in \{a,b,c\}} real\left[V_D^p \cdot \left(I_D^p \right)^* \right]} \right] \times 100\% = 0.4323\%$$

- The efficiency of the PWM inverter, $P_{PWM,eff}$, is calculated using the AC real power consumed by the resistive AC load and the PWM inverter DC power:

$$P_{PWM,eff} = \left(\frac{\sum_{p \in \{a,b,c\}} real\left(V_{5-N}^p \cdot \left(I_{5-N}^p \right)^* \right)}{V_{PWM} \cdot I_{PWM}} \right) \cdot 100\% = 49.80\%$$

The efficiency of the PWM inverter is under 50% because the AC real power is calculated using the fundamental voltages and currents only. It is noted that no AC filter was installed on the PWM inverter. Thus, the AC currents contained large harmonics when PWM inverter AC voltages were applied on the resistive AC load. As a consequence, much power is wasted in harmonics.

For time domain analysis purposes, the harmonic voltages at bus 1 were calculated and provided in Table 5.23. The AC line impedance (60 Hz), DC line resistance, and AC load impedance (60 Hz) were calculated and shown in Table 5.24.

Table 5.23 Voltages at bus 1 in the 5-bus AC/DC system with a variable frequency converter from hardware tests, V: [V, deg], Freq: [Hz]

Frequency	V_a	V_b	V_c
0	0.5194	0.6220	3.2268
60	$70.2101 \angle 0^o$	$70.1483 \angle 240.04^o$	$69.0958 \angle 120.30^o$
180	$0.8360 \angle 78.20^o$	$1.0545 \angle 29.99^o$	$0.4062 \angle 86.48^o$
300	$0.0782 \angle -33.54^o$	$0.2231 \angle 72.28^o$	$0.3119 \angle 203.75^o$
420	$1.0621 \angle 83.26^o$	$0.9565 \angle -43.71^o$	$0.9002 \angle 199.47^o$

Table 5.24 Line and load impedance in the 5-bus AC/DC system with a variable frequency converter, Z, R: [Ω]

Parameters	*Phase A*	*Phase B*	*Phase C*
Z_{line}	0.3338 + j0.6566	0.5101 + j1.0441	0.1912 + j2.1836
R_{dc}	3.2103		
Z_{load}	43.0312	17.8325	22.5003

5.4.2 Time Domain Simulation Results

The 5-bus AC/DC system with a variable frequency converter was tested in time domain using Simulink. The circuit is built using SimPowerSystems Toolbox and shown in Figure 5.21. The parameters of system components were set using the hardware test results.

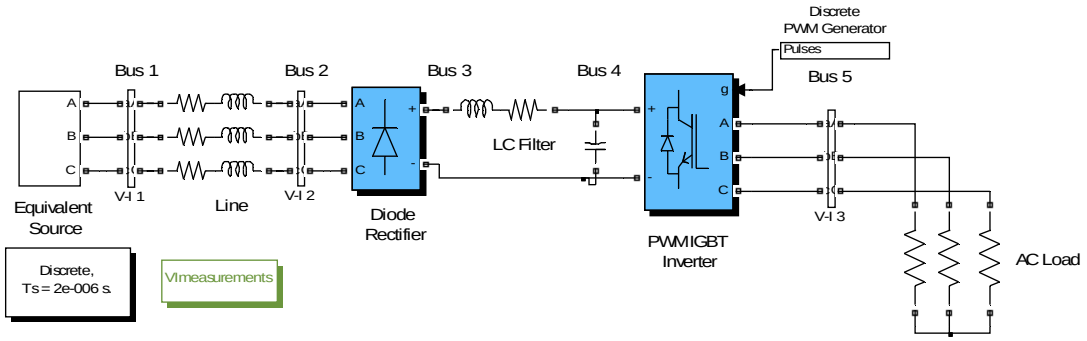


Figure 5.21 The Simulink circuit of the 5-bus AC/DC system with a variable frequency converter

A discrete solver was chosen for simulation with a step size of 2 us. The simulation time was set to 1 second in order to minimize the initial transients. The voltages and currents at each bus were measured using the measurement blocks from the SimPowerSystems Toolbox. The simulation results are presented in the following tables:

- Table 5.25 and Table 5.26 present the voltage and current magnitudes and phase angles respectively;

- Table 5.27 and Table 5.28 present the difference of the voltages and currents between time domain analysis and hardware tests. The difference was calculated using (5.1).

Table 5.25 Voltage profile in the 5-bus AC/DC system with a variable frequency converter from time domain analysis, V: [V, deg]

Bus #	V_a	V_b	V_c
1	$70.21\angle 0^o$	$70.15\angle -119.95^o$	$69.10\angle 120.30^o$
2	$69.3873\angle -0.97^o$	$68.7012\angle -121.54^o$	$67.8827\angle 116.94^o$
3 (DC)	155.5982		
4(DC)	147.4954		
Bus #	V_{ab}	V_{bc}	V_{ca}
5	$69.8029\angle 29.38^o$	$68.8113\angle -89.93^o$	$70.0366\angle 150.42^o$

Table 5.26 Current profile in the 6-bus AC/DC system with a variable frequency converter from time domain analysis, I: [A, deg]

Line/Load	I_a	I_b	I_c
1-2	$1.9510\angle -8.46^o$	$2.0687\angle -131.73^o$	$1.9127\angle 106.79^o$
3-4 (DC)	2.5313		
5-N	$1.1511\angle 3.59^o$	$1.8595\angle -110.09^o$	$1.7502\angle 106.94^o$

Table 5.27 Voltage difference in the 5-bus AC/DC system between time domain simulation and hardware tests, Δ|V |: [%]

Bus #	$\Delta\|V_a\|$	$\Delta\|V_b\|$	$\Delta\|V_c\|$
2	0.10	0.01	0.08
3 (DC)	0.75		
4(DC)	**0.94**		
Bus #	$\Delta\|V_{ab}\|(\%)$	$\Delta\|V_{bc}\|(\%)$	$\Delta\|V_{ca}\|(\%)$
5	0.32	0.20	0.06

Table 5.28 Current difference in the 5-bus AC/DC system between time domain simulation and hardware tests, Δ|I |: [%]

Line/Load	$\Delta\|I_a\|$	$\Delta\|I_b\|$	$\Delta\|I_c\|$
1-2	0.54	0.38	**1.47**
3-4	0.02		

(DC)			
5-N	0.93	0.31	0.46

Remarks:

- The maximal difference is 1.47%. It is mainly attributed to the non-simultaneous measurements.

Next, AC/DC power flow in the 5-bus system is calculated using the power flow solvers in steady-state and compared with the hardware test results.

5.4.3 Steady-State Power Flow Analysis Results

The sequential and unified power flow solvers were applied to the 5-bus AC/DC system with the variable frequency converter. The parameters of the system components were equal to those obtained from the hardware tests. The source voltages at bus 1 only included the fundamental voltages and were set to those in Table 5.23. The real power loss percentage of the diode rectifier was equal to 0.4323% from the hardware tests. The PWM inverter was operated by the AC voltage control. The PWM converter AC voltage, V_{PWM}^{LL}, was balanced and the magnitude was equal to 70 V. The efficiency of the PWM inverter was equal to 49.80% from the hardware tests. The simulation results are presented in the following tables:

- Table 5.29 presents the participation coefficients, $\lambda_{D,I}^{LL}$, $\lambda_{D,P}^{LL}$, and equivalence coefficients, K_D^{LL} in the diode rectifier model;
- Table 5.30 and Table 5.31 present the voltage and current magnitudes and phase angles respectively;

- Table 5.32 and Table 5.33 present the difference of the voltages and currents between steady-state analysis and the hardware tests respectively. The difference was calculated using (5.1).

Table 5.29 Coefficients of the diode rectifier model in the 5-bus AC/DC system with a variable frequency converter from steady-state analysis

Parameters	*Line AB*	*Line BC*	*Line CA*
$\lambda_{D,I}^{LL}$	0.3570	0.3492	0.2937
$\lambda_{D,P}^{LL}$	0.3574	0.3491	0.2935
K_D^{LL}	1.3504	1.3410	1.3546

Table 5.30 Voltage profile in the 5-bus AC/DC system with a variable frequency converter from steady-state analysis, V: [V, deg]

Bus #	V_a	V_b	V_c
1	$70.21\angle 0^o$	$70.15\angle -119.95^o$	$69.10\angle 120.30^o$
2	$69.3262\angle -0.96^o$	$68.5869\angle -121.48^o$	$67.7422\angle 116.98^o$
3 (DC)	156.0532		
4(DC)	147.8326		
Bus #	V_{ab}	V_{bc}	V_{ca}
5	$70.00\angle 30^o$	$70.00\angle -90^o$	$70.00\angle 150^o$

Table 5.31 Current profile in the 5-bus AC/DC system with a variable frequency converter from steady-state analysis, I: [A, deg]

Line/Load	I_a	I_b	I_c
1-2	$1.9889\angle -10.64^o$	$2.0889\angle -134.85^o$	$1.9078\angle 104.71^o$
3-4 (DC)	2.5607		
5-N	$1.1562\angle 3.47^o$	$1.8678\angle -110.29^o$	$1.7565\angle 106.76^o$

Table 5.32 Voltage difference in the 5-bus AC/DC system between steady-state analysis and hardware tests, Δ|V |: [%]

Bus #	$\Delta\|V_a\|$	$\Delta\|V_b\|$	$\Delta\|V_c\|$
2	0.19	0.18	0.29
3 (DC)	0.46		

4(DC)	0.72		
Bus #	$\Delta\|V_{ab}\|(\%)$	$\Delta\|V_{bc}\|(\%)$	$\Delta\|V_{ca}\|(\%)$
5	0.04	**1.52**	0.11

Table 5.33 Current difference in the 5-bus AC/DC system between steady-state analysis and hardware tests, Δ|I |: [%]

Line/Load	$\Delta\|I_a\|$	$\Delta\|I_b\|$	$\Delta\|I_c\|$
1-2	**2.49**	1.35	1.21
3-4 (DC)	1.19		
5-N	0.49	0.76	0.82

Remarks:

- The maximal difference calculated using (5.1) in the voltages is 1.52% and the maximal difference in the currents is 2.49%. They are larger than that (1.47%) in time domain analysis.
- The errors are attributed to the assumptions in the diode rectifier model and the PWM inverter model in addition to the non-simultaneous measurements.

5.5 Comments

In this chapter, a flexible three-phase AC/DC system test bed was presented. It has been used to perform hardware tests for unbalanced AC/DC power flow studies with the presence of a thyristor converter, a diode rectifier, and a variable frequency converter. The test results were used to investigate the properties of power converters under unbalanced operating conditions. Time domain simulations have been performed to verify the hardware test results. It was found that the AC/DC power flow was consistent between time domain analysis and hardware tests when the accuracies of the measurement devices were considered.

The sequential and unified power flow solvers proposed in Chapter 3 and Chapter 4 were applied to the AC/DC systems set up on the test bed. The accuracy of the solvers was validated by comparing steady-state power flow results with those obtained from the hardware tests. It was found that the difference was within 4%, which is mainly attributed to the delta-connected converter models and the accuracies of the measured data. It can be improved by using more accurate and automated measurement systems.

CHAPTER 6. CONCLUSIONS

This thesis has focused on system modeling and steady-state analysis for unbalanced AC/DC distribution systems using hardware validated power electronic device models. The contributions are summarized and conclusions are drawn in this chapter. In addition, future work is discussed.

6.1 Contributions

This thesis presented new ac/dc power flow analysis tools with new converter component models. First, unbalanced models were created for power electronic devices in distribution systems. The following contributions have been made:

- Detailed models, consisting of three, delta-connected, single-phase converters, for three-phase thyristor converters, diode rectifiers, and PWM converters;
- Introduction of the participation coefficients to capture unbalanced contributions of the single-phase converters;
- The equivalence transformation between the models and three-phase converters using the equivalence coefficients;

The models are applicable to systems under significantly unbalanced conditions. The delta-connected models use the single-phase converters to capture the imbalance of distribution systems. They are valid for both unbalanced rectifiers and inverters with either continuous or discontinuous dc currents. Comparisons between time domain analysis and steady-state analysis demonstrated the effectiveness of the models and their consistency with three-phase converter benchmarks in Simulink.

Second, the converter models have been implemented into distribution system ac/dc

power flow studies. The following contributions have been made:

- Development of equivalent ac and dc power flow components using the delta-connected converter models;
- A three-phase sequential power flow solver using a backward/forward algorithm and a subsystem ranking method;
- A three-phase unified power flow solver using Modified Nodal Analysis (MNA) method;

In the sequential solver, the ranking method effectively determined the sequence for solving power flow in the backward/forward algorithm. In the MNA based unified solver, converter currents were solved with ac and dc voltages in a unified manner. The solver can be developed conveniently using existing nodal analysis programs because original nodal admittance matrix structure is maintained in MNA.

Detailed numerical simulation studies have been performed in radial and meshed networks for bi-directional ac/dc power flow studies. Simulation results show that both the sequential and unified solvers were robust and converged to the same results for the same radial or weakly meshed system. The equivalent power flow components of the converters and connected ac or dc subsystems appropriately modeled ac and dc subsystems.

Third, a hardware platform with software analysis tools has been developed to validate the converter models and the ac/dc power flow solvers. The following contributions have been made:

- A three-phase ac/dc system test bed containing a three-phase thyristor converter, a diode rectifier, and a variable frequency converter;

- The design of the variable frequency converter and its control circuit;
- Data analysis functions and time domain simulation circuits;

Detailed hardware tests, time domain simulations, and steady-state analysis have been performed for ac/dc power flow studies. The test bed has a flexible structure and can be configured as balanced or unbalanced ac/dc systems with various types of converters. The hardware test results can be used to investigate properties of unbalanced ac/dc systems and to validate power converter models and steady-state power flow solvers. The comparison among the hardware tests, time domain simulations, and steady-state power flow calculation has shown that the power flow solvers, which used the delta-connected converter models, provided consistently accurate results which are equal or less than 3.77% from the hardware results and time domain analysis results.

6.2 Future Work

With increasing power electronic devices, distribution systems are facing new challenges, such as changes in power quality, the need for new protection coordination schemes, etc. These changes should be studied in both software simulated environments and hardware environments. As such, the ideas and contents in Chapter 2 to Chapter 5 can be extended for research in the following areas.

6.2.1 System Modeling and Analysis

The steady-state converter models can be applied to harmonics analysis. Power quality problems are major concerns with power electronic devices entering distribution systems. This is because power electronic devices with insufficient filtering generate harmonics in a wide frequency range under unbalanced operating conditions. The delta-

connected modeling approach can be used to capture the properties of unbalanced voltages and currents at different frequencies. The models can be implemented in harmonic power flow solvers to investigate power quality.

6.2.2 Application to Planning and Operation

The power converter models and power flow solvers can also be used for new protection scheme design. Power electronic devices have been used as protection devices to prevent the spread of faults in certain circumstances. With appropriate control schemes, they can open and close circuits in micro-seconds instead of milliseconds by traditional circuit breakers. As such, new appropriate protection schemes are desired. To develop the new protection schemes, the impacts of these power electronic devices on systems can be studied using the delta-connected models and power flow solvers.

6.2.3 Hardware and Software Test-Beds for Multi-Frequency Systems

In order to validate potential distribution system applications, the ac/dc system test bed presented in Chapter 5 can be used to develop new hardware and software tools. In [37], a reconfigurable distribution system laboratory with an ac, three-phase, 36-bus network has been developed. The test-bed can be integrated into this laboratory to create large systems simulating shipboard power systems, distribution systems with alternative energy sources, etc. In addition to hardware, software packages can be developed and incorporated with the hardware for system analysis such as harmonic power flow studies, power quality analysis, etc.

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Appendix A. Fourier Coefficients of the AC Currents in the Delta-Connected Thyristor Converter Model

To determine the magnitudes of the ac currents in the delta-connected model, FFT analysis is performed on the time varying ac current. The formulation used to calculate the Fourier coefficients at the fundamental frequency includes:

$$a_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}\left(\omega t\right)\cdot\cos\left(\omega t\right)\cdot d\left(\omega t\right) \tag{A.1}$$

$$b_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}\left(\omega t\right)\cdot\sin\left(\omega t\right)\cdot d\left(\omega t\right) \tag{A.2}$$

The dc currents, $i_{T,dc}^{LL}\left(\omega t\right)$, in the single-phase converters are used because they have the following relation with the ac currents.

$$i_{T,dc}^{LL}\left(\omega t\right) = \left|i_T^{LL}\left(\omega t\right)\right| \tag{A.3}$$

The dc currents are different for converters in continuous and discontinuous conditions. They are illustrated as follows.

A.1 Continuous Conduction

For continuous conduction, $i_{T,dc}^{LL}\left(\omega t\right)$ is given in (A.4). Substituting the current into (A.1) and (A.2) gives a_{LL}, b_{LL}.

$$i_{T,dc}^{LL}\left(\omega t\right) = \begin{cases} \dfrac{\sqrt{2}\left|V_T^{LL}\right|}{R_{dc}}\left|\sin\left(\theta_1^{LL}+u_1^{LL}+\delta_{V_T}^{LL}\right)\right|\cdot\dfrac{\left(\omega t-\theta_1^{LL}\right)}{u_1^{LL}} & \theta_1^{LL}\le\omega t\le\theta_1^{LL}+u_1^{LL} \\ \dfrac{\sqrt{2}\left|V_T^{LL}\right|}{R_{dc}}\left|\sin\left(\omega t+\delta_{V_T}^{LL}\right)\right| & \theta_1^{LL}+u_1^{LL}\le\omega t\le\theta_2^{LL} \\ \dfrac{\sqrt{2}\left|V_T^{LL}\right|}{R_{dc}}\left|\sin\left(\theta_2^{LL}+\delta_{V_T}^{LL}\right)\right|\cdot\left(1-\dfrac{1}{u_2^{LL}}\cdot\left(\omega t-\theta_2^{LL}\right)\right) & \theta_2^{LL}\le\omega t\le\theta_2^{LL}+u_2^{LL} \\ 0 & otherwise \end{cases} \tag{A.4}$$

$$a_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}(\omega t)\cdot\cos(\omega t)\cdot d(\omega t) \tag{A.5}$$

$$= \frac{2}{\pi}\left[\int_{\theta_1^{LL}}^{\theta_1^{LL}+u_1^{LL}} i_{T,dc}^{LL}(t)\cdot\cos(\omega t)\cdot d(\omega t)\right.$$

$$+\int_{\theta_1^{LL}+u_1^{LL}}^{\theta_2^{LL}} i_{T,dc}^{LL}(t)\cdot\cos(\omega t)\cdot d(\omega t)$$

$$\left.+\int_{\theta_2^{LL}}^{\theta_2^{LL}+u_2^{LL}} i_{T,dc}^{LL}(t)\cdot\cos(\omega t)\cdot d(\omega t)\right]$$

$$= a_{LL,1}\cdot\left[f_1\left(\theta_1^{LL}+u_1^{LL}\right)-f_1\left(\theta_1^{LL}\right)-\theta_1^{LL}\cdot\left[\cos\left(\theta_1^{LL}\right)-\cos\left(\theta_1^{LL}+u_1^{LL}\right)\right]\right]$$

$$+a_{LL,2}\cdot\left[f_2\left(\theta_2^{LL}\right)-f_2\left(\theta_1^{LL}+u_1^{LL}\right)\right]$$

$$+a_{LL,3}\cdot\left[-f_3\left(\theta_2^{LL}+u_2^{LL}\right)+f_3\left(\theta_2^{LL}\right)+\left(\theta_2^{LL}+u_2^{LL}\right)\cdot\left[\cos\left(\theta_2^{LL}\right)-\cos\left(\theta_2^{LL}+u_2^{LL}\right)\right]\right]$$

Where:

$$a_{LL,1} = \frac{2\sqrt{2}\left|V_{T,LL}\right|\cdot\sin\left(\theta_1^{LL}+u_1^{LL}+\theta_{T,LL}\right)}{\pi R_{dc}\cdot u_1^{LL}},\quad a_{LL,2} = \frac{2\sqrt{2}\left|V_{T,LL}\right|}{\pi R_{dc}},$$

$$a_{LL,3} = \frac{2\sqrt{2}\left|V_{T,LL}\right|\cdot\sin\left(\theta_2^{LL}+\theta_{T,LL}\right)}{\pi R_{dc}\cdot u_2^{LL}}$$

$$f_1(x) = \sin(x)-x\cdot\cos(x),\quad f_2(x) = -\frac{1}{4}\sin\left(2\cdot x+\theta_{T,LL}\right)+\frac{1}{2}\cos\left(\theta_{T,LL}\right)\cdot x$$

$$f_3(x) = f_1(x)$$

$$b_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}(\omega t)\cdot\sin(\omega t)\cdot d(\omega t) \tag{A.6}$$

$$= \frac{2}{\pi}\left[\int_{\theta_1^{LL}}^{\theta_1^{LL}+u_1^{LL}} i_{T,dc}^{LL}(t)\cdot\sin(\omega t)\cdot d(\omega t)\right.$$

$$+\int_{\theta_1^{LL}+u_1^{LL}}^{\theta_2^{LL}} i_{T,dc}^{LL}(t)\cdot\sin(\omega t)\cdot d(\omega t)$$

$$+\int_{\theta_2^{LL}}^{\theta_2^{LL}+u_2^{LL}} i_{T,dc}^{LL}(t)\cdot\sin(\omega t)\cdot d(\omega t)\Bigg]$$

$$=b_{LL,1}\cdot\left[g_1\left(\theta_1^{LL}+u_1^{LL}\right)-g_1\left(\theta_1^{LL}\right)-\theta_1^{LL}\cdot\left[\sin\left(\theta_1^{LL}+u_1^{LL}\right)-\sin\left(\theta_1^{LL}\right)\right]\right]$$

$$+b_{LL,2}\cdot\left[g_2\left(\theta_2^{LL}\right)-g_2\left(\theta_1^{LL}+u_1^{LL}\right)\right]$$

$$+b_{LL,3}\cdot\left[-f_3\left(\theta_2^{LL}+u_2^{LL}\right)+f_3\left(\theta_2^{LL}\right)+\left(\theta_2^{LL}+u_2^{LL}\right)\cdot\left[\sin\left(\theta_2^{LL}+u_2^{LL}\right)-\sin\left(\theta_2^{LL}\right)\right]\right]$$

where

$$b_{LL,1}=a_{LL,2},\quad b_{LL,2}=a_{LL,2},\quad b_{LL,3}=a_{LL,3}$$

$$g_1(x)=\cos(x)+x\cdot\sin(x),\quad g_2(x)=-\frac{1}{4}\cos\left(2\cdot x+\theta_{T,LL}\right)+\frac{1}{2}\sin\left(\theta_{T,LL}\right)\cdot x,$$

$$g_3(x)=g_1(x)$$

A.2 Discontinuous Conduction

For discontinuous conduction, $i_{T,dc}^{LL}(\omega t)$ is given in (A.7) and . Substituting it into (A.1)in (2.28) (A.2) gives a_{LL}, b_{LL}.

$$i_{T,dc}^{LL}(\omega t)=\begin{cases}A_{LL}\cdot\cos(\omega t)+B_{LL}\cdot\sin(\omega t)+C_{LL}\cdot\omega t+D_{LL} & \theta_1^{LL}\le\omega t\le\theta_2^{LL}\\ 0 & otherwise\end{cases}\qquad\text{(A.7)}$$

where:

$$A_{LL}=\frac{-\sqrt{2}\left|V_T^{LL}\right|}{\omega L_{dc}}\cos\left(\delta_{V_T}^{LL}\right),\quad B_{LL}=\frac{\sqrt{2}\left|V_T^{LL}\right|}{\omega L_{dc}}\sin\left(\delta_{V_T}^{LL}\right),$$

$$C_{LL}=-\frac{V_{C_{dc}}}{\omega L_{dc}},\qquad D_{LL}=-A_{LL}\cdot\cos\left(\theta_1^{LL}\right)-B_{LL}\cdot\sin\left(\theta_1^{LL}\right)-C_{LL}\cdot\theta_1^{LL}$$

$$a_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}(\omega t)\cdot\cos(\omega t)\cdot d(\omega t)$$

$$= \frac{2}{\pi}\int_{\theta_1^{LL}}^{\theta_2^{LL}} \left[A\cdot\cos(\omega t)+B\cdot\sin(\omega t)+C\cdot\omega t+D\right]\cdot\cos(\omega t)\cdot d(\omega t)$$

$$= \frac{2}{\pi}\Big[A\cdot\left[f_1\left(\theta_2^{LL}\right)-f_1\left(\theta_1^{LL}\right)\right]+B\cdot\left[f_2\left(\theta_2^{LL}\right)-f_2\left(\theta_1^{LL}\right)\right]$$

$$+C\cdot\left[f_3\left(\theta_2^{LL}\right)-f_3\left(\theta_1^{LL}\right)\right]+D\cdot\left(\theta_2^{LL}-\theta_1^{LL}\right)\Big]$$

Where:

$$f_1(x)=\frac{x}{2}+\frac{1}{4}\sin(2x),\quad f_2(x)=-\frac{1}{4}\cos(2x),\quad f_3(x)=\cos(x)+x\cdot\sin(x)$$

$$b_{LL} = \frac{2}{\pi}\int_0^{\pi} i_{T,dc}^{LL}(\omega t)\cdot\sin(\omega t)\cdot d(\omega t)$$

$$= \frac{2}{\pi}\int_{\theta_1^{LL}}^{\theta_2^{LL}} \left[A\cdot\cos(\omega t)+B\cdot\sin(\omega t)+C\cdot\omega t+D\right]\cdot\sin(\omega t)\cdot d(\omega t)$$

$$= \frac{2}{\pi}\Big[A\cdot\left[g_1\left(\theta_2^{LL}\right)-g_1\left(\theta_1^{LL}\right)\right]+B\cdot\left[g_2\left(\theta_2^{LL}\right)-g_2\left(\theta_1^{LL}\right)\right]$$

$$+C\cdot\left[g_3\left(\theta_2^{LL}\right)-g_3\left(\theta_1^{LL}\right)\right]+D\cdot\left(\theta_2^{LL}-\theta_1^{LL}\right)\Big]$$

where:

$$g_1(x)=f_1(x),\quad g_2(x)=\frac{x}{2}-\frac{1}{4}\sin(2x),\quad g_3(x)=\sin(x)-x\cdot\cos(x)$$

Appendix B. Three-Phase Thyristor Converter Benchmark and Evaluation of the Delta-Connected Model in Balanced AC/DC Systems

To study three-phase thyristor converters, a 4-bus balanced ac/dc system was created with the same circuit diagram shown in Figure 2.14. The parameters of the system components are shown in Table B.1.

Table B.1 Component parameters of the 4-bus balanced ac/dc system with a three-phase thyristor converter

Parameters	Values
Source line-to-line voltage	208 V @ 60 Hz
Source impedance	$X_s^p = 0.3 \quad \Omega \quad p \in \{a,b,c\}$
Line 1 & 2 impedance	$Z_1^p = Z_2^p = 0.1410 + j0.4400$
AC load impedance	$Z_L^p = 20 + j9 \quad \Omega$
DC load impedance	$R_{dc} = 10 \quad \Omega$
Converter snubber resistance	100 Ω
Converter snubber capacitance	0.1 uF
Converter conducting impedance	0.001 Ω
Converter forward voltage	0.7 V
Firing angles	10°

B.1 Simulation Results of the 3-Phase Thyristor Converter Benchmark

The circuit in Figure 2.14 was built in MATALAB Simulink using the SimPowerSystems Toolbox for time domain simulation. The Simulink circuit is shown in Figure B.1.

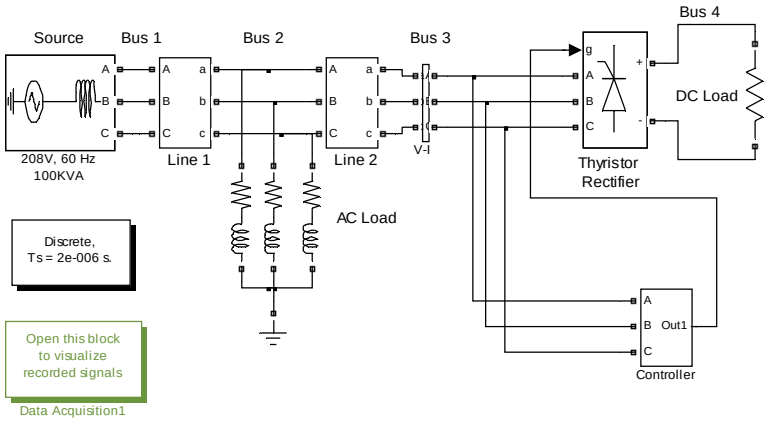


Figure B.1 The Simulink circuit of the 4-bus balanced ac/dc system with a three-phase thyristor converter

A discrete solver was selected with a step size of 2 us. Each simulation has been run for 0.05 seconds. To evaluate the model, the following signals directly related to the three-phase thyristor converter were measured and shown in Figure B.2 and Figure B.3.

- The line-to-neutral voltages on Bus 3, $v_T^p(t)$, $p \in \{a,b,c\}$
- The ac currents entering the thyristor converter, $i_T^p(t)$
- The dc voltage on Bus 4, $v_{T,dc}(t)$
- The dc current, $i_{T,dc}^{3\phi}(t)$

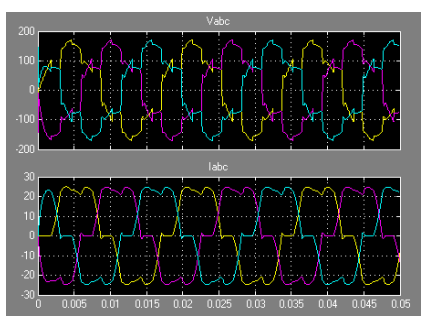


Figure B.2 Line-to-neutral voltages (top) and ac currents (bottom) in the three-phase balanced thyristor converter benchmark

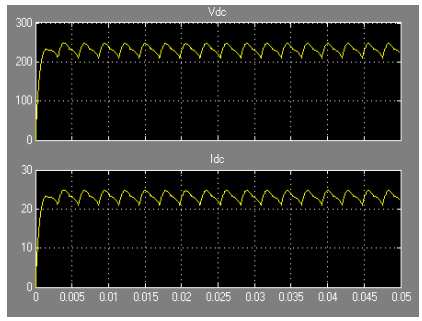


Figure B.3. Dc voltage (top) and dc current (bottom) in the three-phase balanced thyristor converter benchmark

The ac voltages, currents, power at 60 Hz and dc voltage, current and power were calculated using measurement blocks from the SimPowerSystems Toolbox and are shown in Table B.2.

Table B.2 Numerical results of the three-phase balanced thyristor converter benchmark using Simulink

Parameters	AC Values at 60Hz on Bus 3		
	Phase A	Phase B	Phase C
V_T^p (V)	$105.4292\angle -10.71^o$	$105.4280\angle -130.72^o$	$105.4275\angle 109.29^o$
I_T^p (A)	$17.9998\angle -26.30^o$	$17.9994\angle -146.30^o$	$17.9998\angle 93.70^o$
S_T^p (VA)	1827.9253+j509.8274	1827.8970+j509.7593	1827.5181+j509.8309
	DC Values on Bus 4		
$V_{T,dc}$ (V)	232.7067		
$I_{T,dc}^{3\phi}$ (A)	23.2707		
$P_{T,dc}^{3\phi}$ (W)	5415.2037		

Since the system is balanced, both the ac currents and power entering the converter are also unbalanced. The total real power entering the converter is 5483.3 watts. Compared with the dc power, the converter real power loss is *1.04%*.

B.2 Evaluating the Delta-Connected Thyristor Converter Model

The three-phase thyristor converter was studied using the equivalent delta-connected model in steady-state. First, the participation coefficients and the equivalence coefficients

in the model were calculated using (2.24), (2.25), and (2.34). It is assumed that the ac and dc voltages applied on the model are equal to those in the benchmark. The results are provided in Table B.3. $\lambda_{T,I}^{LL}$, $\lambda_{T,P}^{LL}$, and K_T^{LL} are all equal on the three single-phase converters because the system is balanced.

Table B.3 Current participation coefficients, $\lambda_{T,I}^{LL}$, power participation coefficients, $\lambda_{T,P}^{LL}$, and equivalence coefficients, K_T^{LL} ,in the 1-phase thyristor converters

Parameters	Line AB	Line BC	Line CA
$\lambda_{T,I}^{LL}$	0.3334	0.3333	0.3333
$\lambda_{T,P}^{LL}$	0.3334	0.3333	0.3333
K_T^{LL}	1.3408	1.3408	1.3408

Using the model, the ac currents, I_T^p , and power, S_T^p , entering the three-phase converter were calculated and compared with those obtained in the benchmark. The results are shown in Table B.4 with the difference in percentage with respect to the benchmark. The maximal error in the ac currents and ac power is 0.6062%. It is attributed to $I_{T,dc}^{3\phi}$.

Table B.4 The ac currents, I_T^p , and ac power, S_T^p in the three-phase thyristor converter using the Δ-connected model

Parameters	Δ - Connected Model	$\Delta\left\|I_T^p\right\|$ (%)
I_T^a (A)	18.0143 $\angle$ -26.47 ^{o}	0.5246
I_T^b (A)	18.0137 $\angle$ -146.47 ^{o}	0.5255
I_T^c (A)	18.0133 $\angle$ 93.53 ^{o}	0.5291
	Δ - Connected Model	$\Delta\left\|S_T^p\right\|$ (%)
S_T^a (VA)	1827.8 + j515.9	0.5239
S_T^b (VA)	1827.8 + j5156	0.5258
S_T^c (VA)	1827.7 + j5158	0.5095
$I_{T,dc}^{3\phi}$	23.1301	0.6042

Appendix C. Case Files for the 12-Bus AC/DC System

Case 1

```
ARTIFICIAL TEST CASE
12 BUS SYSTEM, 1 THYRISTOR RECTIFIER BETWEEN BUS 3-4 1 PWM INVERTER BETWEEN
BUS 6-7, 2 DC LINE, 1 DC LOAD

ARTIFICIAL DISTRIBUTION SYSTEM
ARTIFICIAL LOAD LEVELS

END/ TITLE
TEST, 200
100000
END/ PARAMS
    BUS1    12.47    0.00    0.00    0    1    .00    .00    BUS 1
    BUS2    12.47    0.10    0.00    0    1    .00    .00    BUS 2
    BUS3    12.47    0.20    0.00    0    1    .00    .00    BUS 3
    BUS4    12.47    0.30    0.00    0    1    .00    .00    BUS 4
    BUS5    12.47    0.40    0.00    0    1    .00    .00    BUS 5
    BUS6    12.47    0.50    0.00    0    1    .00    .00    BUS 6
    BUS7    12.47    0.60    0.00    0    1    .00    .00    BUS 7
    BUS8    12.47    0.70    0.00    0    1    .00    .00    BUS 8
    BUS9    12.47    0.80    0.00    0    1    .00    .00    BUS 9
    BUS10   12.47    0.90    0.00    0    1    .00    .00    BUS 10
    BUS11   12.47    0.50    0.10    0    1    .00    .00    BUS 11
    BUS12   12.47    0.50    0.10    0    1    .00    .00    BUS 11
END/ NODES
BUS1    12.47    0.00 0.05 0.00 0.05
END/ SOURCE
BUS1   BUS2   L 1 ABC L15207    1.00
BUS2   BUS3   L 1 ABC L14652    1.00
BUS3   BUS4   L 1 ABC L15644    1.00
BUS4   BUS5   L 1 ABC L17676    1.00
BUS5   BUS6   L 1 ABC L17676    1.00
BUS4   BUS7   C 1 ABC
BUS7   BUS8   L 1 D    L15055    1.00
BUS8   BUS9   C 1 ABC
BUS9   BUS10 L 1 ABC L17676    1.00
BUS10 BUS11 L 1 ABC L17676    1.00
BUS11 BUS12 L 1 ABC L17676    1.00
END/ BRANCH
END/ TRANSF
BUS2    1    2    200.0    0.0    400.0    0.0    800.0    0.0
BUS5    1    22    300 0
BUS6    1    22    600 200
BUS7    1    22    200 0
BUS10   1   22    900.0    400.0
BUS11   1    21    -800 -400
BUS12   1    2    300    100    250 150 200 60
END/ LOADS
END/ CONSUM
END/ PV
BUS4 BUS7 1 0    0 600    16.8345 10 10 10
BUS9 BUS8 2 1    1 600    12.47 30 12.47 -90 12.47 150 600 1.0 1.0 1.0
END/ PWRCVT
```

Case 2

```
ARTIFICIAL TEST CASE
12 BUS SYSTEM, 1 THYRISTOR INVERTER BETWEEN BUS 3-4 1 PWM RECTIFIER BETWEEN
BUS 6-7, 2 DC LINE, 1 DC LOAD

ARTIFICIAL DISTRIBUTION SYSTEM
ARTIFICIAL LOAD LEVELS

END/ TITLE
TEST, 200
100000
END/ PARAMS
    BUS1    12.47    0.00    0.00    0    1    .00    .00    BUS 1
    BUS2    12.47    0.10    0.00    0    1    .00    .00    BUS 2
    BUS3    12.47    0.20    0.00    0    1    .00    .00    BUS 3
    BUS4    12.47    0.30    0.00    0    1    .00    .00    BUS 4
    BUS5    12.47    0.40    0.00    0    1    .00    .00    BUS 5
    BUS6    12.47    0.50    0.00    0    1    .00    .00    BUS 6
    BUS7    12.47    0.60    0.00    0    1    .00    .00    BUS 7
    BUS8    12.47    0.70    0.00    0    1    .00    .00    BUS 8
    BUS9    12.47    0.80    0.00    0    1    .00    .00    BUS 9
    BUS10   12.47    0.90    0.00    0    1    .00    .00    BUS 10
    BUS11   12.47    0.50    0.10    0    1    .00    .00    BUS 11
    BUS12   12.47    0.50    0.10    0    1    .00    .00    BUS 11
END/ NODES
BUS1    12.47    0.00 0.05 0.00 0.05
END/ SOURCE
BUS1    BUS2    L 1 ABC L15207    1.00
BUS2    BUS3    L 1 ABC L14652    1.00
BUS3    BUS4    L 1 ABC L15644    1.00
BUS4    BUS5    L 1 ABC L17676    1.00
BUS5    BUS6    L 1 ABC L17676    1.00
BUS4    BUS7    C 1 ABC
BUS7    BUS8    L 1 D    L15055    1.00
BUS8    BUS9    C 1 ABC
BUS9    BUS10 L 1 ABC L17676    1.00
BUS10 BUS11 L 1 ABC L17676    1.00
BUS11 BUS12 L 1 ABC L17676    1.00
END/ BRANCH
END/ TRANSF
BUS2    1    2    200.0    0.0    400.0    0.0    800.0    0.0
BUS5    1    22    600 0
BUS6    1    22    800 300
BUS7    1    22    50 0
BUS10    1    22    200.0    100.0
BUS12    1    2    100    50    150 70 100 60
END/ LOADS
END/ CONSUM
BUS11 4 800 12.47
END/ PV
BUS4 BUS7 1 1    6 600    -100 10 10 10
BUS9 BUS8 2 0    3 600    27.434 1 1 1
END/ PWRCVT
```

Appendix D. Case Files for the 25-Bus AC/DC System

Case 1A. Summer Load Ppwm=0 MW

```
ARTIFICIAL TEST CASE
25 BUS SYSTEM, 1 RECTIFIER BETWEEN BUS 18-23 1 PWM BETWEEN BUS 10-25, 2 DC LINE, 1
DC LOAD

ARTIFICIAL DISTRIBUTION SYSTEM
ARTIFICIAL LOAD LEVELS

END/ TITLE
TEST, 200
100000
END/ PARAMS
    BUS1   34.50   0.00   0.00   0   1   .00   .00   BUS 1
    BUS2   34.50   0.10   0.00   0   1   .00   .00   BUS 2
    BUS3   34.50   0.20   0.00   0   1   .00   .00   BUS 3
    BUS4   34.50   0.30   0.00   0   1   .00   .00   BUS 4
    BUS5   34.50   0.40   0.00   0   1   .00   .00   BUS 5
    BUS6   34.50   0.50   0.00   0   1   .00   .00   BUS 6
    BUS7   34.50   0.60   0.00   0   1   .00   .00   BUS 7
    BUS8   34.50   0.70   0.00   0   1   .00   .00   BUS 8
    BUS9   34.50   0.80   0.00   0   1   .00   .00   BUS 9
    BUS10  34.50   0.90   0.00   0   1   .00   .00   BUS 10
    BUS11  34.50   0.50   0.10   0   1   .00   .00   BUS 11
    BUS12  34.50   0.50   0.20   0   1   .00   .00   BUS 12
    BUS13  34.50   0.50   0.30   0   1   .00   .00   BUS 13
    BUS14  34.50   0.50   0.40   0   1   .00   .00   BUS 14
    BUS15  34.50   0.50   1.50   0   1   .00   .00   BUS 15
    BUS16  34.50   0.50   1.50   0   1   .00   .00   BUS 16
    BUS17  34.50   0.50   1.50   0   1   .00   .00   BUS 17
    BUS18  34.50   0.50   1.50   0   1   .00   .00   BUS 18
    BUS19  34.50   0.50   0.20   0   1   .00   .00   BUS 12
    BUS20  34.50   0.50   0.30   0   1   .00   .00   BUS 13
    BUS21  34.50   0.50   0.40   0   1   .00   .00   BUS 14
    BUS22  34.50   0.50   1.50   0   1   .00   .00   BUS 15
    BUS23  34.50   0.50   1.50   0   1   .00   .00   BUS 16
    BUS24  34.50   0.50   1.50   0   1   .00   .00   BUS 17
    BUS25  34.50   0.50   1.50   0   1   .00   .00   BUS 18
END/ NODES
BUS1    34.50    0.00 0.05 0.00 0.05
END/ SOURCE
BUS1   BUS2   L 1 ABC L17676    1.00
BUS2   BUS3   L 1 ABC L17676    1.00
BUS3   BUS4   L 1 ABC L17676    1.00
BUS4   BUS5   L 1 ABC L17676    1.00
BUS5   BUS6   L 1 ABC L17676    1.00
BUS6   BUS7   L 1 ABC L17676    5.00
BUS7   BUS8   L 1 ABC L17676    5.00
BUS8   BUS9   L 1 ABC L17676    5.00
BUS9   BUS10 L 1 ABC L17676    5.00
BUS10 BUS11 L 1 ABC L17676    5.00
BUS11 BUS12 L 1 ABC L17676    5.00
BUS12 BUS13 L 1 ABC L17676    5.00
BUS6   BUS14 L 1 ABC L17676    5.00
```

```
BUS14 BUS15 L 1 ABC L17676     5.00
BUS15 BUS16 L 1 ABC L17676     5.00
BUS16 BUS17 L 1 ABC L17676     5.00
BUS17 BUS18 L 1 ABC L17676     5.00
BUS18 BUS19 L 1 ABC L17676     5.00
BUS19 BUS20 L 1 ABC L17676     5.00
BUS20 BUS21 L 1 ABC L17676     5.00
BUS21 BUS22 L 1 ABC L17676     5.00
BUS23 BUS24 L 1 D     L17676     1.00
BUS24 BUS25 L 1 D     L17676     1.00
BUS18 BUS23 C 1 ABC
BUS10 BUS25 C 0 ABC
END/ BRANCH
END/ TRANSF
BUS3    1    2     500.0    0.0     500.0    0.0    500.0   0.0
BUS10   1    22    1600     800
BUS13   1    22    600      200
BUS17   1    22    300      100
BUS20   1    22    600      200
BUS22   1    22    300      100
BUS24   1    12      200    0
BUS18   1    22     0      -600
END/ LOADS
END/ CONSUM
END/ PV
BUS18 BUS23 1 0   0 600   45.8674 10 10 10
BUS10 BUS25 2 1   1 600   34.224 30 34.224 -90 34.224 150 0 1.0 1.0 1.0
END/ PWRCVT
```

Case 1B. Summer Load Ppwm=0.4 MW

```
ARTIFICIAL TEST CASE
25 BUS SYSTEM, 1 RECTIFIER BETWEEN BUS 18-23 1 PWM BETWEEN BUS 10-25, 2 DC LINE, 1
DC LOAD

ARTIFICIAL DISTRIBUTION SYSTEM
ARTIFICIAL LOAD LEVELS

END/ TITLE
TEST, 200
100000
END/ PARAMS
    BUS1    34.50    0.00    0.00    0    1    .00    .00   BUS 1
    BUS2    34.50    0.10    0.00    0    1    .00    .00   BUS 2
    BUS3    34.50    0.20    0.00    0    1    .00    .00   BUS 3
    BUS4    34.50    0.30    0.00    0    1    .00    .00   BUS 4
    BUS5    34.50    0.40    0.00    0    1    .00    .00   BUS 5
    BUS6    34.50    0.50    0.00    0    1    .00    .00   BUS 6
    BUS7    34.50    0.60    0.00    0    1    .00    .00   BUS 7
    BUS8    34.50    0.70    0.00    0    1    .00    .00   BUS 8
    BUS9    34.50    0.80    0.00    0    1    .00    .00   BUS 9
    BUS10   34.50    0.90    0.00    0    1    .00    .00   BUS 10
    BUS11   34.50    0.50    0.10    0    1    .00    .00   BUS 11
    BUS12   34.50    0.50    0.20    0    1    .00    .00   BUS 12
    BUS13   34.50    0.50    0.30    0    1    .00    .00   BUS 13
    BUS14   34.50    0.50    0.40    0    1    .00    .00   BUS 14
```

```
    BUS15  34.50   0.50   1.50   0   1    .00    .00  BUS 15
    BUS16  34.50   0.50   1.50   0   1    .00    .00  BUS 16
    BUS17  34.50   0.50   1.50   0   1    .00    .00  BUS 17
    BUS18  34.50   0.50   1.50   0   1    .00    .00  BUS 18
    BUS19  34.50   0.50   0.20   0   1    .00    .00  BUS 12
    BUS20  34.50   0.50   0.30   0   1    .00    .00  BUS 13
    BUS21  34.50   0.50   0.40   0   1    .00    .00  BUS 14
    BUS22  34.50   0.50   1.50   0   1    .00    .00  BUS 15
    BUS23  34.50   0.50   1.50   0   1    .00    .00  BUS 16
    BUS24  34.50   0.50   1.50   0   1    .00    .00  BUS 17
    BUS25  34.50   0.50   1.50   0   1    .00    .00  BUS 18
END/ NODES
BUS1    34.50    0.00 0.05 0.00 0.05
END/ SOURCE
BUS1  BUS2   L 1 ABC L17676    1.00
BUS2  BUS3   L 1 ABC L17676    1.00
BUS3  BUS4   L 1 ABC L17676    1.00
BUS4  BUS5   L 1 ABC L17676    1.00
BUS5  BUS6   L 1 ABC L17676    1.00
BUS6  BUS7   L 1 ABC L17676    5.00
BUS7  BUS8   L 1 ABC L17676    5.00
BUS8  BUS9   L 1 ABC L17676    5.00
BUS9  BUS10 L 1 ABC L17676    5.00
BUS10 BUS11 L 1 ABC L17676    5.00
BUS11 BUS12 L 1 ABC L17676    5.00
BUS12 BUS13 L 1 ABC L17676    5.00
BUS6  BUS14 L 1 ABC L17676    5.00
BUS14 BUS15 L 1 ABC L17676    5.00
BUS15 BUS16 L 1 ABC L17676    5.00
BUS16 BUS17 L 1 ABC L17676    5.00
BUS17 BUS18 L 1 ABC L17676    5.00
BUS18 BUS19 L 1 ABC L17676    5.00
BUS19 BUS20 L 1 ABC L17676    5.00
BUS20 BUS21 L 1 ABC L17676    5.00
BUS21 BUS22 L 1 ABC L17676    5.00
BUS23 BUS24 L 1 D    L17676    1.00
BUS24 BUS25 L 1 D    L17676    1.00
BUS18 BUS23 C 1 ABC
BUS10 BUS25 C 1 ABC
END/ BRANCH
END/ TRANSF
BUS3    1    2     500.0    0.0     500.0    0.0    500.0   0.0
BUS10   1    22    1600     800
BUS13   1    22    600      200
BUS17   1    22    300      100
BUS20   1    22    600     200
BUS22   1    22    300     100
BUS24   1    12      200    0
BUS18   1    22     0      -600
END/ LOADS
END/ CONSUM
END/ PV
BUS18 BUS23 1 0   6 600   600 10 10 10
BUS10 BUS25 2 1   3 600   45 0 1.0 1.0 1.0
END/ PWRCVT
```

Case 2A. Winter Load Ppwm=0 MW

ARTIFICIAL TEST CASE
25 BUS SYSTEM, 1 RECTIFIER BETWEEN BUS 18-23 1 PWM BETWEEN BUS 10-25, 2 DC LINE, 1 DC LOAD

ARTIFICIAL DISTRIBUTION SYSTEM
ARTIFICIAL LOAD LEVELS

END/ TITLE
TEST, 200
100000
END/ PARAMS

BUS1	34.50	0.00	0.00	0	1	.00	.00	BUS 1
BUS2	34.50	0.10	0.00	0	1	.00	.00	BUS 2
BUS3	34.50	0.20	0.00	0	1	.00	.00	BUS 3
BUS4	34.50	0.30	0.00	0	1	.00	.00	BUS 4
BUS5	34.50	0.40	0.00	0	1	.00	.00	BUS 5
BUS6	34.50	0.50	0.00	0	1	.00	.00	BUS 6
BUS7	34.50	0.60	0.00	0	1	.00	.00	BUS 7
BUS8	34.50	0.70	0.00	0	1	.00	.00	BUS 8
BUS9	34.50	0.80	0.00	0	1	.00	.00	BUS 9
BUS10	34.50	0.90	0.00	0	1	.00	.00	BUS 10
BUS11	34.50	0.50	0.10	0	1	.00	.00	BUS 11
BUS12	34.50	0.50	0.20	0	1	.00	.00	BUS 12
BUS13	34.50	0.50	0.30	0	1	.00	.00	BUS 13
BUS14	34.50	0.50	0.40	0	1	.00	.00	BUS 14
BUS15	34.50	0.50	1.50	0	1	.00	.00	BUS 15
BUS16	34.50	0.50	1.50	0	1	.00	.00	BUS 16
BUS17	34.50	0.50	1.50	0	1	.00	.00	BUS 17
BUS18	34.50	0.50	1.50	0	1	.00	.00	BUS 18
BUS19	34.50	0.50	0.20	0	1	.00	.00	BUS 12
BUS20	34.50	0.50	0.30	0	1	.00	.00	BUS 13
BUS21	34.50	0.50	0.40	0	1	.00	.00	BUS 14
BUS22	34.50	0.50	1.50	0	1	.00	.00	BUS 15
BUS23	34.50	0.50	1.50	0	1	.00	.00	BUS 16
BUS24	34.50	0.50	1.50	0	1	.00	.00	BUS 17
BUS25	34.50	0.50	1.50	0	1	.00	.00	BUS 18

END/ NODES
BUS1 34.50 0.00 0.05 0.00 0.05
END/ SOURCE

BUS1	BUS2	L	1	ABC	L17676	1.00
BUS2	BUS3	L	1	ABC	L17676	1.00
BUS3	BUS4	L	1	ABC	L17676	1.00
BUS4	BUS5	L	1	ABC	L17676	1.00
BUS5	BUS6	L	1	ABC	L17676	1.00
BUS6	BUS7	L	1	ABC	L17676	5.00
BUS7	BUS8	L	1	ABC	L17676	5.00
BUS8	BUS9	L	1	ABC	L17676	5.00
BUS9	BUS10	L	1	ABC	L17676	5.00
BUS10	BUS11	L	1	ABC	L17676	5.00
BUS11	BUS12	L	1	ABC	L17676	5.00
BUS12	BUS13	L	1	ABC	L17676	5.00
BUS6	BUS14	L	1	ABC	L17676	5.00
BUS14	BUS15	L	1	ABC	L17676	5.00
BUS15	BUS16	L	1	ABC	L17676	5.00

```
BUS16 BUS17 L 1 ABC L17676     5.00
BUS17 BUS18 L 1 ABC L17676     5.00
BUS18 BUS19 L 1 ABC L17676     5.00
BUS19 BUS20 L 1 ABC L17676     5.00
BUS20 BUS21 L 1 ABC L17676     5.00
BUS21 BUS22 L 1 ABC L17676     5.00
BUS23 BUS24 L 1 D     L17676     1.00
BUS24 BUS25 L 1 D     L17676     1.00
BUS18 BUS23 C 1 ABC
BUS10 BUS25 C 0 ABC
END/ BRANCH
END/ TRANSF
BUS3    1    2     500.0    0.0     500.0    0.0    600.0   0.0
BUS10   1    2     250    100        200      50   200      150
BUS13   1    22    300    100
BUS17   1    22    300      100
BUS20   1    2     350      200      350      300      400      200
BUS22   1    2     250      100      250      100      200      80
BUS24   1    12    200    0
BUS18   1    22     0      -600
END/ LOADS
END/ CONSUM
END/ PV
BUS18 BUS23 1 0   0 600   45.8674 10 10 10
BUS10 BUS25 2 1   1 600   34.224 30 34.224 -90 34.224 150 0 1.0 1.0 1.0
END/ PWRCVT
```

Case 2B. Winter Load Ppwm=-0.675 MW

```
ARTIFICIAL TEST CASE
25 BUS SYSTEM, 1 RECTIFIER BETWEEN BUS 18-23 1 PWM BETWEEN BUS 10-25, 2 DC LINE, 1
DC LOAD

ARTIFICIAL DISTRIBUTION SYSTEM
ARTIFICIAL LOAD LEVELS

END/ TITLE
TEST, 200
100000
END/ PARAMS
    BUS1    34.50    0.00    0.00    0    1    .00    .00   BUS 1
    BUS2    34.50    0.10    0.00    0    1    .00    .00   BUS 2
    BUS3    34.50    0.20    0.00    0    1    .00    .00   BUS 3
    BUS4    34.50    0.30    0.00    0    1    .00    .00   BUS 4
    BUS5    34.50    0.40    0.00    0    1    .00    .00   BUS 5
    BUS6    34.50    0.50    0.00    0    1    .00    .00   BUS 6
    BUS7    34.50    0.60    0.00    0    1    .00    .00   BUS 7
    BUS8    34.50    0.70    0.00    0    1    .00    .00   BUS 8
    BUS9    34.50    0.80    0.00    0    1    .00    .00   BUS 9
    BUS10   34.50    0.90    0.00    0    1    .00    .00   BUS 10
    BUS11   34.50    0.50    0.10    0    1    .00    .00   BUS 11
    BUS12   34.50    0.50    0.20    0    1    .00    .00   BUS 12
    BUS13   34.50    0.50    0.30    0    1    .00    .00   BUS 13
    BUS14   34.50    0.50    0.40    0    1    .00    .00   BUS 14
    BUS15   34.50    0.50    1.50    0    1    .00    .00   BUS 15
```

```
    BUS16  34.50   0.50   1.50   0   1    .00    .00  BUS 16
    BUS17  34.50   0.50   1.50   0   1    .00    .00  BUS 17
    BUS18  34.50   0.50   1.50   0   1    .00    .00  BUS 18
    BUS19  34.50   0.50   0.20   0   1    .00    .00  BUS 12
    BUS20  34.50   0.50   0.30   0   1    .00    .00  BUS 13
    BUS21  34.50   0.50   0.40   0   1    .00    .00  BUS 14
    BUS22  34.50   0.50   1.50   0   1    .00    .00  BUS 15
    BUS23  34.50   0.50   1.50   0   1    .00    .00  BUS 16
    BUS24  34.50   0.50   1.50   0   1    .00    .00  BUS 17
    BUS25  34.50   0.50   1.50   0   1    .00    .00  BUS 18
END/ NODES
BUS1   34.50   0.00 0.05 0.00 0.05
END/ SOURCE
BUS1  BUS2  L 1 ABC L17676   1.00
BUS2  BUS3  L 1 ABC L17676   1.00
BUS3  BUS4  L 1 ABC L17676   1.00
BUS4  BUS5  L 1 ABC L17676   1.00
BUS5  BUS6  L 1 ABC L17676   1.00
BUS6  BUS7  L 1 ABC L17676   5.00
BUS7  BUS8  L 1 ABC L17676   5.00
BUS8  BUS9  L 1 ABC L17676   5.00
BUS9  BUS10 L 1 ABC L17676   5.00
BUS10 BUS11 L 1 ABC L17676   5.00
BUS11 BUS12 L 1 ABC L17676   5.00
BUS12 BUS13 L 1 ABC L17676   5.00
BUS6  BUS14 L 1 ABC L17676   5.00
BUS14 BUS15 L 1 ABC L17676   5.00
BUS15 BUS16 L 1 ABC L17676   5.00
BUS16 BUS17 L 1 ABC L17676   5.00
BUS17 BUS18 L 1 ABC L17676   5.00
BUS18 BUS19 L 1 ABC L17676   5.00
BUS19 BUS20 L 1 ABC L17676   5.00
BUS20 BUS21 L 1 ABC L17676   5.00
BUS21 BUS22 L 1 ABC L17676   5.00
BUS23 BUS24 L 1 D   L17676   1.00
BUS24 BUS25 L 1 D   L17676   1.00
BUS18 BUS23 C 1 ABC
BUS10 BUS25 C 1 ABC
END/ BRANCH
END/ TRANSF
BUS3   1   2   500.0   0.0   500.0   0.0   600.0   0.0
BUS10  1   2   250   100   200   50   200   150
BUS13  1   22  300   100
BUS17  1   22  300   100
BUS20  1   2   350   200   350   300   400   200
BUS22  1   2   250   100   250   100   200   80
BUS24  1   12  200   0
BUS18  1   22  0   -600
END/ LOADS
END/ CONSUM
END/ PV
BUS18 BUS23 1 1   6 600   475 10 10 10
BUS10 BUS25 2 0   3 600   43.8209 0 1.0 1.0 1.0
END/ PWRCVT
```

Appendix E. Test Manual for a 3-Phase AC/DC System with a Diode Rectifier or a Thyristor Converter

E.1 Objective

Perform experiments to study ac/dc power flow in a three-phase unbalanced ac/dc system with a three-phase diode rectifier or a three-phase thyristor converter

E.2 Hardware Devices

- AC power supply – CEPE station 1-4
- 1 3-phase knife switch
- 1 3-phase autotransformer
- 3 multi-tap reactors (#19, #20, and #21 in CEPE)
- 1 3-phase diode rectifier (Fuji Electric 6RI100E)
- 1 3-phase thyristor converter (CEPE design)
- 1 dc load (light banks on output A-I)

E.3 Test Equipment

- 1 oscilloscope - Tektronix TDS 4013
- 4 high voltage differential probes - Tektronix P5200
- 2 current probes and amplifiers - Tektronix TCP 303, TCPA-300
- 1 digital meter - Fluke 37

E.4 Introduction

In this experiment, ac/dc power flow was studied in a three-phase unbalanced

ac/dc system with a three-phase full bridge diode rectifier or a three-phase full bridge thyristor converter. The diode rectifier is a Fuji Electric's 6RI100E series rectifier. This is a single unit, three-phase full bridge rectifier. It is capable of 100 A continuous outputs at up to 600 V. The thyristor converter is developed in Center for Electric Power Engineering (CEPE) at Drexel University as shown in Figure E.1.

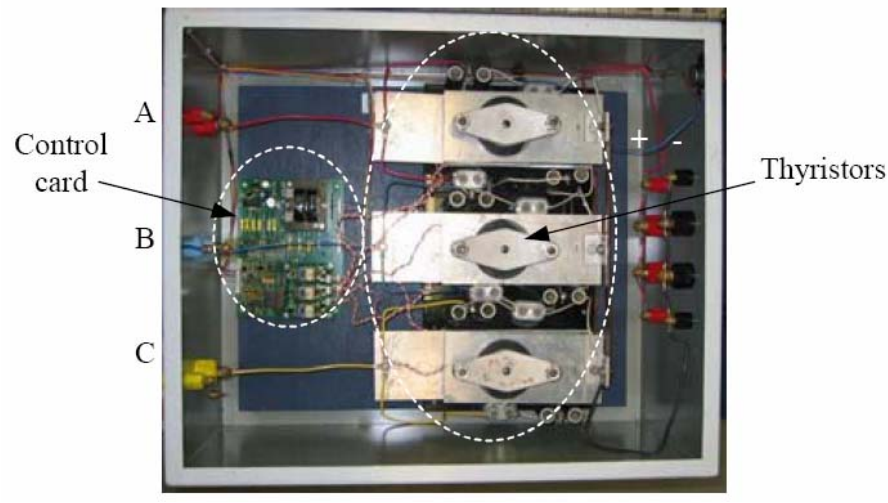


Figure E.1 The full-bridge three-phase thyristor converter in CEPE

The thyristor converter consists of six GE thyristors. There is a control card (PTR6000-208) operating thyristors using the equi-distant control. The firing angles can be altered manually.

E.5 Experimental Setup

The test circuit for the 3-bus ac/dc system is shown in Figure E.2. The actual hardware setup is shown in Figure E.3 for the ac/dc system with the thyristor converter. A three-phase source provides 208V ac power on a power station. The power is fed into a three-phase, wye-ground/wye autotransformer. The neutral of the transformer is connected to the ground on the power station. The outputs of the transformer feed into a

three-phase ac line. The ac line consists of three 7-tap reactors (0.5 / 1.0 / 2.0 / 3.0 / 6.0 / 12.0 /24.0 Ohms) in a transmission line box. The following settings are used:

Phase A: 0.5 Ohms, *Phase B: 1 Ohm,* *Phase C: 2 Ohms*

The ac line is connected to the input port of the three-phase ac/dc converter, which is at bus 2 shown in Figure E.2. The output of the converter, which is at bus 3, supplies a resistive dc load. The load is mimicked using carbon filament light bulbs (120 Vac). Three panels of light bulbs are connected in series. Each group can have 1 to 60 light bulbs connected in parallel.

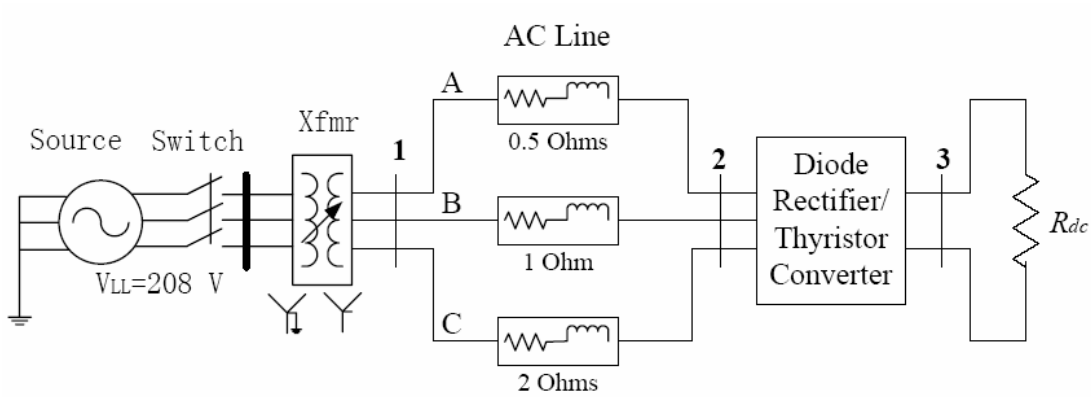


Figure E.2 The circuit diagram of the three-phase ac/dc system with a three-phase diode rectifier or a three-phase thyristor converter

Figure E.3 The hardware setup of the three-phase ac/dc system with a three-phase thyristor converter

E.6 Test Procedure

This test will study power flow in the three-phase unbalanced ac/dc system. The test includes the following steps:

Step 1. Close the knife switch and turn on the ac power on the power station;

Step 2. Increase the output voltages of the autotransformer to 208 V line-to-line (rms). Check the voltages using the digital meter;

Step 3. Switch on 60 light bulbs on each panel;

Step 4. For the thyristor converter, adjust the firing angles manually to desired values;

Step 5. Capture the following voltages and currents using the voltage probes and current probes. Record the data in EXCEL spreadsheets using the oscilloscope. The voltage probes are set to 500V:1V. The current probes are set to 5A:1V.

- 3-phase line-to-ground voltages at Bus 1 and Bus 2
- DC voltage at Bus 3
- 3-phase currents entering bus 2
- DC current in the dc load at Bus 3

Step 6. Decrease the output voltages of the autotransformer to zero;

Step 7. Turn off the power and open the knife switch.

Appendix F. Test Manual for a 3-Phase AC/DC System with a Variable Frequency Converter

F.1 Objective

Perform experiments for ac/dc power flow studies in a three-phase unbalanced ac/dc system with a variable frequency converter

F.2 Hardware Devices

- AC power supply – CEPE station 3
- 1 3-phase knife switch
- 1 3-phase autotransformer
- 3 multi-tap reactors (#19, #20, and #21 in CEPE)
- 1 3-phase variable frequency converter
- 1 PC (C3A) with dSPACE DS1104 DSP card and MATLAB 6.1 with simulink
- 1 3-phase ac load (light banks on outlets C and D)

F.3 Test Equipment

- 1 oscilloscope-Tektronix TDS 4013
- 4 high voltage differential probes - Tektronix P5200
- 2 sets of current probes and amplifiers – Tektronix TCP 303, TCPA-300
- 1 digital meter - Fluke 37

F.4 Introduction

In this experiment, ac/dc power flow was studied in a three-phase unbalanced ac/dc system with a three-phase variable frequency converter. The converter consists of three parts as shown in Figure F.1. The actual converter is shown in Figure F.2.

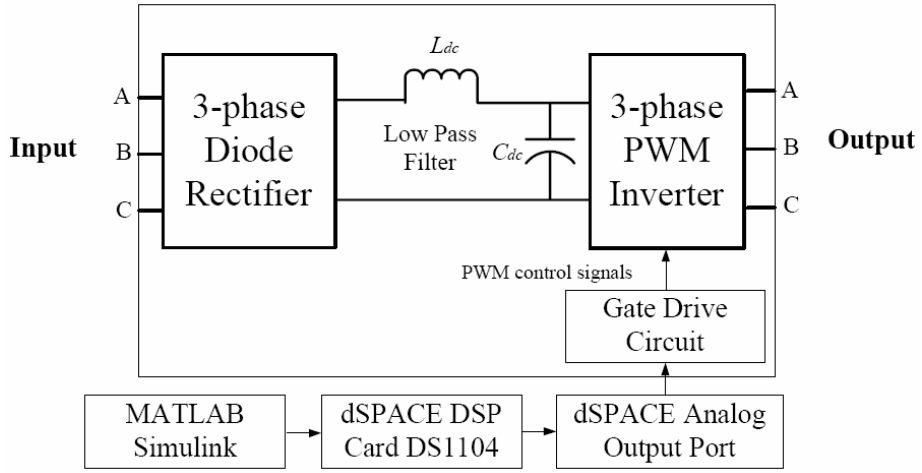


Figure F.4 The block diagram of the 3-phase ac/dc/ac variable frequency converter

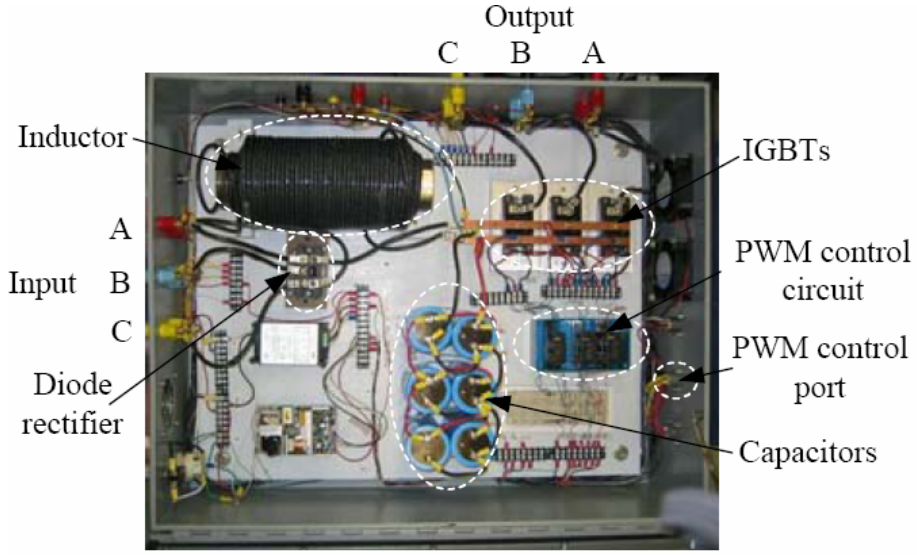


Figure F.5 The hardware of the 3-phase ac/dc/ac variable frequency converter

The first part is a 100A three-phase diode rectifier from Fuji Company (Fuji 6RI100E-060). The rectifier can convert the ac signals into dc signals. A low pass filter is installed on the dc link to filter out the high frequency signals generated by the rectifier. The third part of the converter is a three-phase, full bridge, Pulse-Width-Modulated (PWM) inverter. The inverter has three sets of two-Isolated Gate Bipolar Transistors (IGBTs) from International Rectifier Company (GA100TS60U). By switching the IGBTs, the inverter may convert the dc signals to ac signals at various frequencies.

The control of the IGBTs is achieved by using a controller board from dSPACE (DS1104). MATLAB Simulink is utilized to generate the PWM signals. The PWM control signals are downloaded to the board, then fed into a gate drive circuit, which is also built in the converter box, through an interface box. The gate drive circuit will amplify the control signals to an appropriate voltage level (-8 V / +15 V) to switch the IGBTs. DC supplies are installed to provide power for the gate drive circuits.

F.5 Experimental Setup

The test circuit for the ac/dc system is shown in Figure F.3. The actual hardware setup is shown in Figure F.4. In the system, a three-phase source provides 208V ac power on a power station. The power is fed into a three-phase, wye-ground/wye autotransformer after a three-phase knife switch. The neutral of the transformer is connected to the ground on the power station. The outputs of the transformer feed into a three-phase ac line. The ac line consists of three 7-tap reactors (0.5 / 1.0 / 2.0 / 3.0 / 6.0 / 12.0 /24.0 Ohms) in a transmission line box. The following settings are used:

Phase A: 0.5 Ohms, *Phase B: 1 Ohm,* *Phase C: 2 Ohms*

The ac line is connected to the input port of the converter, which is at bus 2 shown in the figure. The output of the converter, which is at bus 5, is connected to a three-phase, wye-connected, ungrounded resistive load. The constant resistive loads are carbon filament light bulbs.

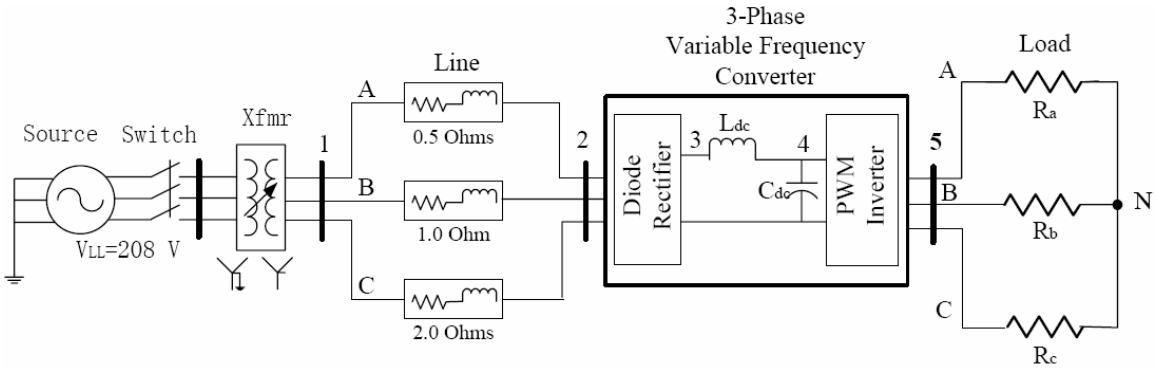


Figure F.6 The circuit diagram of the three-phase ac/dc system with a three-phase variable frequency converter

Figure F.7 The hardware setup of the three-phase ac/dc system with a three-phase variable frequency converter

In order to control the PWM inverter using the dSPACE board, an interface chassis is connected to the dSPACE card in the PC. The control cable is plugged in the PWM slave I/O port on the interface. The other end of the control cable is connected to the controller input port on the converter.

F.6 Test Procedure

The test procedure includes the following 3 parts:

- Software setup
- Gate drive circuit test
- AC/DC power flow test

F.6.1 Software Setup

In order to operate the IGBT in the PWM inverter, control signals are generated by a DSP card from dSPACE 1104. The DSP card is controlled by software programs developed in MATLAB Simulink. The setup procedure for the software program includes the following steps:

Step 1. Before running the experiment, the Simulink (MABLAB R12.1/6.1) and dSPACEDeskControl must be installed on the computer with dSPACE 1104 DSP card.

Step 2. Open dSPACEDeskControl software. Then open MATLAB from dSPACEDeskControl. The default Simulink library in MATLAB is for DS1003 DSP card. We need to type “rti1104” under MATLAB after MATLAB is opened from dSPACEDeskControl. Then the software will switch from DS1003 to DS1104. All blocks of DS1104 will appear.

Step 3. Open PWMConverter.mdl in Simulink. It is noted that the settings: “Simulation->Simulation Parameters->system target file & template make file” MUST be changed to DS1104.tlc and DS1104.tmf as shown below in Figure F.5.

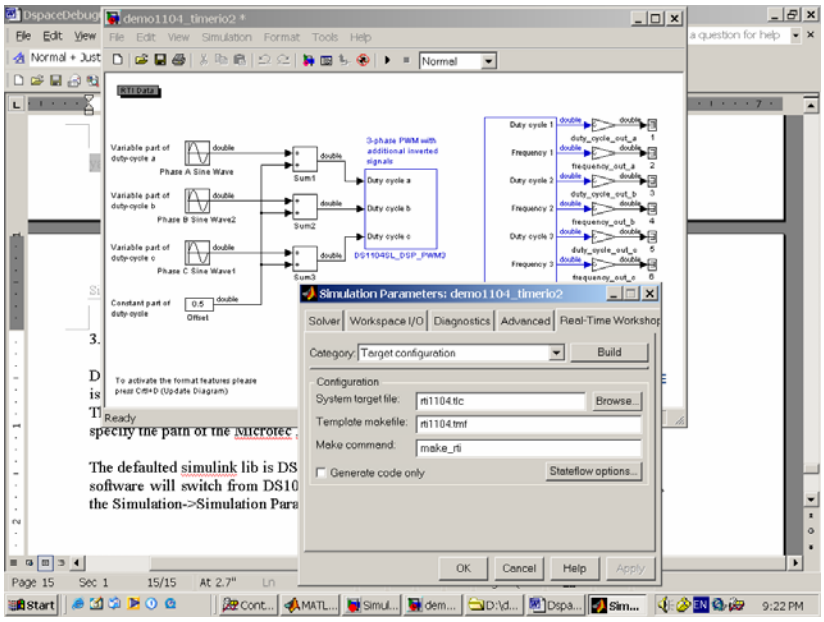
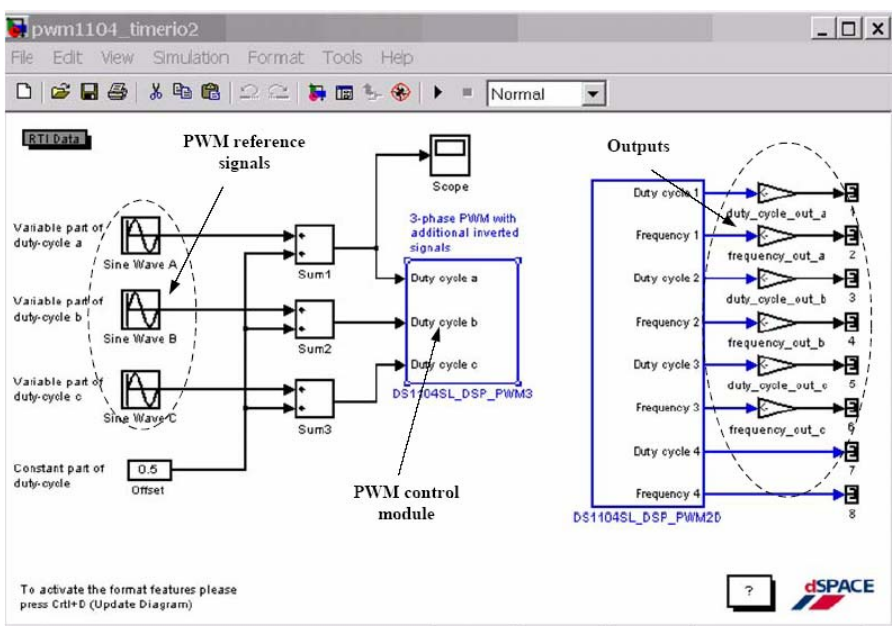
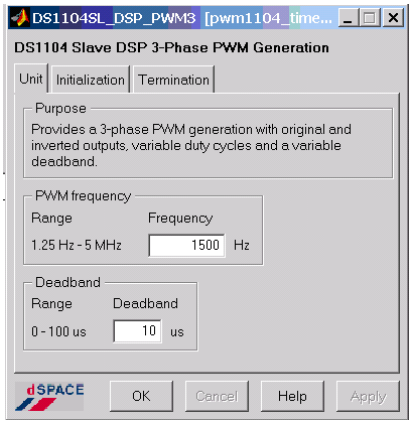


Figure F.5. Simulink Setting for the dSPACE 1104 DSP Card

The simulation circuit in PWMConverter.mdl is shown in Figure F.6.



(a)



(b)

Figure F.6 The PWM inverter control circuit (a) and PWM control module (b) in MATLAB Simulink for the dSPACE DS1104 DSP card

Step 4. The fundamental frequency of the control signals is set to 60Hz. The switching frequency of the PWM controller is set to 1500Hz. The modulation is set to 0.8. The deadband between two control signals on each phase is set between 10uS to 20 uS.

Step 5. Download the code to the dSPACE card to generate PWM control signals by using “Ctrl+B”.

F.6.2 Gate Drive Circuit Test

This test is to determine whether the gate drive circuits can generate appropriate control signals to switch the IGBTs on the inverter. The ac power is turned off in the experiment. The test procedure includes the following steps:

Step 1. Run the Simulink, and open PWMConverter.mdl. The fundamental frequency of the control signals is set to 60Hz. The switching frequency of the PWM controller is set to 1500Hz. The modulation is set to 0.8. The deadband between two control signals on each phase is set to 20 uS.

Step 2. Turn on the dc supply in the converter box for the gate drive circuit.

Step 3. Download the code to the dSPACE board to generate PWM control signals by using Ctrl+B.

Step 4. Compare the inputs and outputs of the six gate drive circuits using the voltage probes and the oscilloscope. Make sure the output of each channel of gate drive circuits is out of phase of its input and the output voltage is between -8V and 15V.

Step 5. Compare the waveforms of the two signals for the dual IGBT module on each phase and check if they are out of phase. Perform Fast Fourier Transform (FFT) on the oscilloscope to check the frequency of the control signals. Also check if the dead-band on each phase is consistent with the specified values.

Step 6. Capture the line-to-line signals at the output of the inverter at open circuit. Check if the signals are 120 degree apart.

F.6.3 AC/DC System Test

This test will study power flow in the three-phase unbalanced ac/dc system. The test includes the following steps:

Step 1. Run the Simulink, open PWMConverter.mdl. The fundamental frequency of the control signals is set to 60Hz. The switching frequency of the PWM controller is set to 1500Hz. The deadband between two control signals on each phase is set to 20uS;

Step 2. Turn on the dc supply for the gate drive circuit;

Step 3. Download the code to the dSPACE board to generate PWM control signals by using Ctrl+B;

Step 4. Close the knife switch. Turn on the ac power on the power station;

Step 5. Increase the output voltages of the autotransformer slowly. First, check the dc voltage and the PWM inverter output voltages with diode rectifier input line-to-line voltage at 10 to 30 V.

Step 6. Then, increase the rectifier input line-to-line voltage to 120V (rms). Check the line voltages using the digital meter;

Step 7. Capture the following voltages and currents using the voltage probes and current probes. Record the data in EXCEL spreadsheets using the oscilloscope. The voltage probes are set to 500V:1V. The current probes are set to 5A:1V.

- 3-phase line-to-ground voltages at Bus 1 and Bus 2
- DC voltages at Bus 3 and Bus 4
- 3-phase line-to-line voltages at Bus 5
- 3-phase voltages across the ac load
- 3-phase currents entering bus 2
- DC current on the dc link from Bus 3 to Bus 4
- 3-phase currents in the ac load on Bus 5

Step 8. Decrease the output voltages of the autotransformer to zero.

Step 9. Turn off the power and open the knife switch.

VITA

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SELECTED PUBLICATIONS

[1] V. Cecchi, X. Yang, K. Miu, and C. Nwankpa, "Instrumentation and measurement of a power distribution system laboratory for meter placement and network reconfiguration studies," *submitted to IEEE Transactions on Instrumentation and Measurement*.

[2] X. Yang, S. Carullo, K. Miu, and C. Nwankpa, "Reconfigurable distribution automation and control laboratory: a multi-phase, radial power flow experiment," *IEEE Transactions on Power Systems*, vol. 20, Aug. 2005, pp. 1207-1214.

[3] R. Stoicescu, K. Miu, C. Nwankpa, D. Niebur, and X. Yang, "Three-phase converter models for unbalanced radial power flow studies," *IEEE Transactions on Power Systems*, vol. 17, Nov. 2002, pp. 1016-1021.

[4] V. Cecchi, X. Yang, and K. Miu, "Measurement and control of a power distribution system laboratory for network reconfiguration studies," *Proc. IEEE Instrumentation and Measurement Technology Conference*, Sorrento, Italy, April 24 - 27, 2006.

[5] C. Nwankpa, K. Miu, D. Niebur, X. Yang, and S. Carullo, "Power transmission and distribution system laboratories at Drexel University," *Proc. IEEE Power Engineering Society General Meeting*, San Francisco, CA, June 12-16, 2005.

[6] X. Yang, V. Cecchi, K. Miu, and C. Nwankpa, "Reconfigurable distribution automation and control laboratory: a network reconfiguration experiment for load balancing and loss reduction in power distribution systems," *Proc. American Society for Engineering Education Annual Conference & Exposition*, Portland, OR, June 12-15, 2005.

[7] X. Yang, and K. Miu, "3-phase converter models for unbalanced radial distribution power flow studies - thyristor rectifier and pulse-width-modulated inverter," *Proc. IEEE Power Engineering Society General Meeting*, Denver, CO, June 6-9, 2004.

[8] R. Stoicescu, K. Miu, C. Nwankpa, D. Niebur, and X. Yang, "A general approach to distribution converter models," *Proc. IEEE Power Engineering Society General Meeting Panel Session*, Denver, CO, June 6-9, 2004.