Emulation of Power System Load Dynamic Behavior Through Reconfigurable Analog Circuits

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Abstract – **Emulation of power system dynamic load behavior is a viable alternative to popular simulation methods. In this paper, a circuit designed to emulate the dynamic behavior of power system loads is presented. It is constructed from common analog components and is fully reconfigurable via a set of analog input signals. As load behavior is heavily dependent on that of the external network, it is important to demonstrate how this reconfigurable analog load emulation module (RALEM) may be utilized in dynamic power flow studies. Such a demonstration is presented. These studies provide the network's transient and steady-state flow of power in real-time or faster. This is of importance as popular simulation methods cannot provide a solution with such speed.**

I. INTRODUCTION

The behavior of power system loads is heavily dependent on that of the external network. One can not be studied without consideration of the other. This combined behavior is described by a set of differential and algebraic expressions. Typically these expressions are studied through simulation methods, methods in which the system is discretized and software algorithms utilize input parameters to calculate solutions. An example would be a software algorithm utilizing the Newton-Raphson solver to perform power flow studies. Simulation methods have been studied extensively and been proven to provide precise solutions.

It is important to note that viable alternatives do exist. It is possible to study these expressions through emulation methods, methods in which analog hardware utilizes input signals for configuration while measurement devices extract voltage potentials as output. With a reconfigurable design the emulation hardware operates in a similar manner to a software algorithm. The user requires no knowledge of the hardware's internal operation. The circuit utilizes a set of input signals to yield a set of desired output unique to that configuration.

This paper presents the design of a circuit capable of emulating the dynamic behavior of power system loads. It is constructed from common analog components and is fully reconfigurable via a set of analog input signals. The reconfigurable analog load emulation module (RALEM) is utilized in dynamic power flow studies. This method is unique as:

- Emulation, unlike simulation, methods ensure any solution is physically realizable.
- Emulation, unlike simulation, time is controllable and independent of the system size and complexity.

It is the fore-mentioned advantages over simulation which provide the motivation to develop accurate and practical emulation hardware. This goal is achievable through the use of VLSI (very large scale integration) technology. Research conducted in this area is allowing smaller, more efficient, and more accurate analog chips to be produced. Utilizing these advances it will be possible to place hundreds or thousands of RALEM circuits on a single silicon chip [1].

II. LOAD BEHAVIOR

A. Static Load Behavior

The static behavior of a power system load describes the steady-state relationship between the load power consumption (S_L) and load voltage (V_L). This behavior is modeled algebraically in (1). However, it is a linearization around an operating point consisting of the nominal load power consumption (S_0) and nominal load voltage (V_0). Typically, the complex nominal load voltage is equal to that of the network, and the complex nominal load power consumption is equal to that of the physical load.

$$S_L = P_L + jQ_L = S_0 \sum_{\alpha=1}^{3} K_{(\alpha)} \left(\frac{V_L}{V_0} \right)^{\alpha-1} \quad (1)$$

The ZIP or combination type load essentially models complex static load behavior through a parallel connection of three basic load types as shown in fig. 1. Each type maintains a constant electrical characteristic as load voltage varies. The constant power, current, and admittance values are defined in (2), (3), and (4).

$$S_C = K_1 \frac{S_0}{1} \quad (2)$$

$$I_C = K_2 \frac{S_0}{V_0} \quad (3)$$

$$Y_C = K_3 \frac{S_0}{V_0^2} \quad (4)$$

Each of the three components of the ZIP load model expression shown in (1) has a corresponding scaling coefficient. These coefficients must be defined based on the actual static behavior of the physical load. They can be easily extracted from a Taylor Series expansion of this relationship as shown in (5) [2].

$$S_L = f(V_L) \approx S_C + I_C V_L + Y_C V_L^2 + O^3 \quad (5)$$

This paper assumes that all loads close to their respective operating point at all times and therefore (1) is always valid.

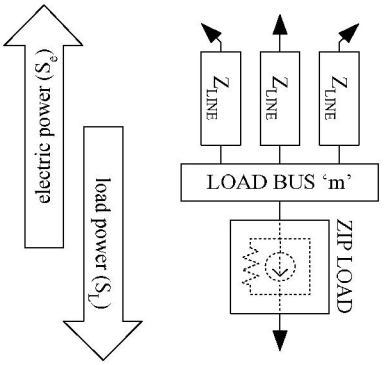

Fig. 1. ZIP Load

B. Dynamic Load Behavior

The dynamic behavior of a power system load describes the manner in which the load's bus voltage changes with respect to time. At a bus 'm', dynamic load behavior is dictated by the initial bus voltage, the load power consumption (S_L) as defined in (1), and the electric power injections (S_e) as defined in (6). The direction of these power flows is evident in fig. 1.

$$S_e^m = P_e^m + jQ_e^m = \sum_{k=1}^{n} |V_m||V_k| e^{j\theta_{ik}} (G_{mk} - jB_{mk}) \quad (6)$$

At bus 'm', this behavior can be decomposed into two decoupled relationships described differentially in (7) and (8) [3].

$$\frac{\partial |V_m|}{\partial t} = -\left|K_Q^m\right| \left(Q_e^m + Q_L^m \right) \quad (7)$$

$$\frac{\partial \delta_m}{\partial t} = -\left|K_P^m\right| \left(P_e^m + P_L^m \right) \quad (8)$$

The steady-state represents the state in which, at a bus 'm', the load power consumption (S_L^m) and electric power injections (S_e^m) equal one another satisfying the conservation of power principle. The rate at which the transient behavior dictated in (7) and (8) settles to a steady-state value can be controlled through two differential time constants (K_Q^m, K_P^m). As the magnitude of this coefficient grows, the transients will settle to their steady-state value more rapidly [3].

III. Emulation of AC Systems with DC Networks

Emulation of AC systems is performed utilizing four decoupled DC networks as shown in fig. 2.

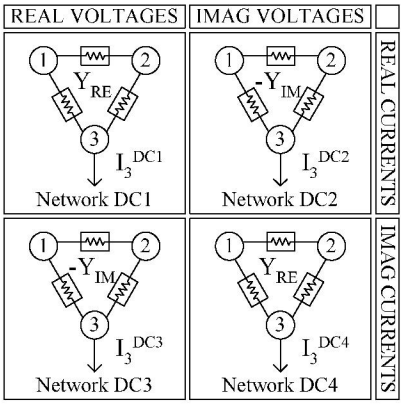

Fig. 2. DC Emulation Networks

Each network contains the same number of buses as the original AC system and is connected in the same manner. The DC network voltages are defined with respect to a given bus 'm' in (9) and (10).

$$\mathrm{Re}\left(V_m^{AC}\right) = V_m^{DC1} = V_m^{DC3} \quad (9)$$

$$\mathrm{Im}\left(V_m^{AC}\right) = V_m^{DC2} = V_m^{DC4} \quad (10)$$

The DC network line conductances are defined with respect to a given line 'm' in (11) and (12).

$$\mathrm{Re}\left(Y_m^{AC}\right) = G_m^{DC1} = G_m^{DC4} \quad (11)$$

$$-\mathrm{Im}\left(Y_m^{AC}\right) = G_m^{DC2} = G_m^{DC3} \quad (12)$$

The complex AC load current is defined with respect to a bus 'm' as a combination of the four DC network load currents. This relationship is shown in (13). The same relationship applies for line currents [7].

$$\mathrm{Re}\left(I_{\mathrm{m}}^{\mathrm{AC}}\right)+j\,\mathrm{Im}\left(I_{\mathrm{m}}^{\mathrm{AC}}\right)=\left(I_{\mathrm{m}}^{\mathrm{DC1}}+I_{\mathrm{m}}^{\mathrm{DC2}}\right)+j\left(I_{\mathrm{m}}^{\mathrm{DC4}}-I_{\mathrm{m}}^{\mathrm{DC3}}\right) \quad (13)$$

IV. RALEM Design

The behavior of the reconfigurable analog load emulation module (RALEM) circuit is defined by (1), (7), and (8). It maintains these relationships using a looped feedback design. Initially measurement devices read the currents entering the circuit from the load bus within the four DC networks. An analog computational engine utilizes those measurements to calculate updated real and imaginary bus voltages consistent with (1), (7), and (8). Finally controllable voltage sources apply these updated real and imaginary voltages to the DC network load buses as dictated in (9) and (10). The process is detailed in fig. 3.

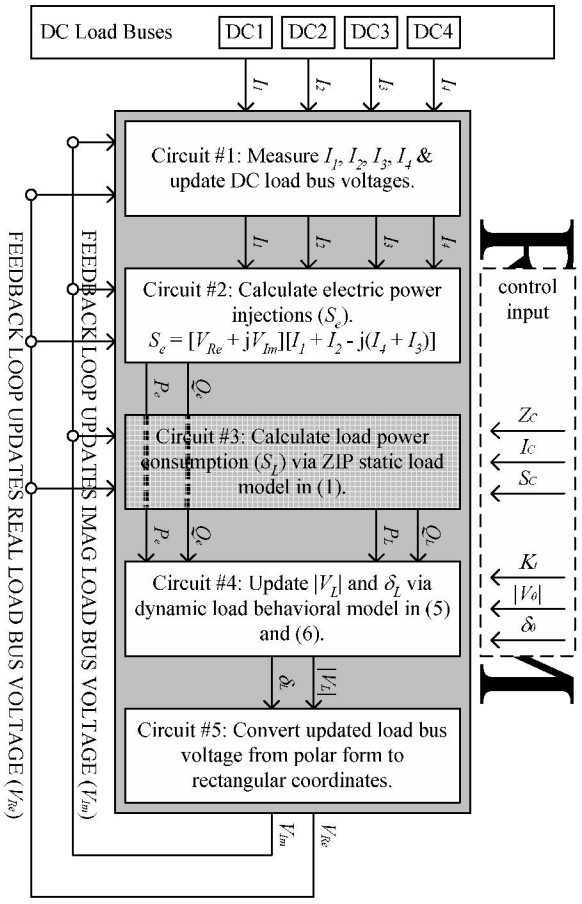

Fig. 3. RALEM Design Overview

The circuit is implemented in analog hardware utilizing a combination of traditional amplifiers, operational transconductance amplifiers, analog 4-quadrant multiplier chips, analog trigonometric function converter chips, and CMOS analog switches. It is reconfigured using a set of nine analog control signals. Note that Z_C, I_C, and S_C have both real and imaginary components requiring separate DC control signals. The analog input control signal labeled K_t^m controls both differential time constants defined in (7) and (8) [6]. The RALEM circuit design assumes equivalent recovery rates for both real and reactive dynamic behavior.

V. RALEM Testing

As load behavior is heavily dependent on that of the external network, it is important to demonstrate how this reconfigurable analog load emulation module (RALEM) may be utilized in dynamic power flow studies. It is used below to provide the dynamic behavior of the load bus voltage within a standard 3-bus network. The test results provided below present a comparison between power flow solutions yielded through two methods: emulation and simulation. Analysis of these results assumes the solution provided by simulations methods to be ideal, and utilizes it as a benchmark with which to compare the accuracy of emulation methods [1].

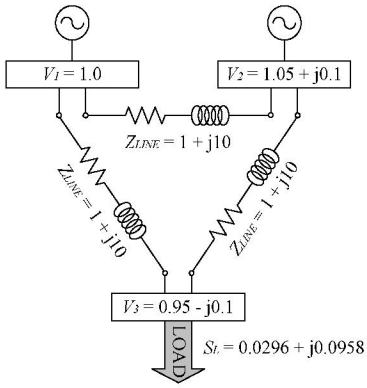

Fig. 4. 3-Bus Simulated / Ideal Power Flow Solution (Case #1)

A. Simulated Power Flow Solution

The 3-bus power flow solution shown (case #1) in fig. 4. is provided by a Newton-Raphson power flow solver simulated in MATLAB Release 12. This is considered the ideal or desired solution. Note that all values are given in per unit.

B. Emulated Power Flow Solution

In order to obtain dynamic behavior of the load bus voltage through emulation the design outlined in fig. 3. is implemented in Cadence OrCAD Capture CIS v10.1 Network transmission lines are implemented using standard resistors as outlined in (11) and (12). Network generators are implemented with ideal voltage sources as outlined in (9) and (10).

The RALEM is configured using a set of nine analog control signals. Table 1 outlines this configuration.

Table 1. RALEM Control Values (Case #1)

Control Signal	Real	Imag.
Constant Load Admittance (Y_C)	0	0
Constant Load Current (I_C)	0	0
Constant Load Power (S_C)	0.0296 p.u.	0.0958 p.u.
Initial Load Bus Voltage Mag $\|V_0\|$	1 p.u.	n/a
Initial Load Bus Voltage Angle (δ_0)	0	n/a
Differential Time Constants ($K_t = K_P, K_Q$)	38.4	n/a

C. *Power Flow Solution Comparison*

The steady-state load bus power flow solutions provided by the RALEM circuit match the ideal simulated values very closely. The test cases were performed. For case #1, the emulation method yields a steady-state real load bus voltage of 0.927V with an error of 2.42% when compared to the value yielded through simulation, 0.95V. For case #2, the emulation method yields a steady-state imaginary load bus voltage of -0.102V with an error of 1.95% when compared to the value yielded through simulation, -0.10V. The dynamic behavior of the load is presented in fig. 5 and fig. 6.

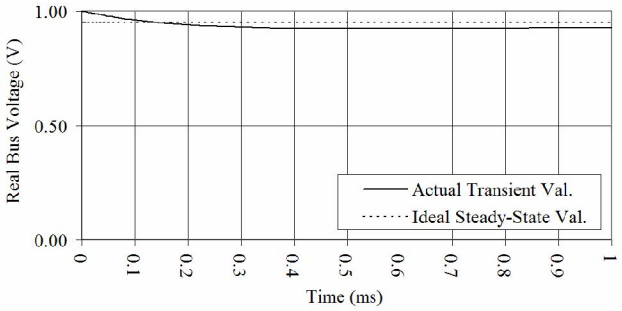

Fig. 5. Transient Real Load Bus Voltage vs. Time (Case #1)

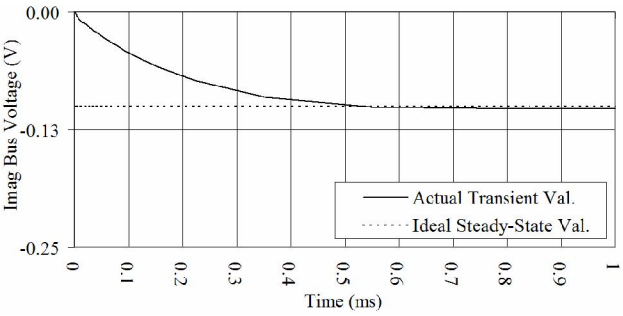

Fig. 6. Transient Imaginary Load Bus Voltage vs. Time (Case #1)

Three test cases were performed, results for cases #2 and #3 are found in table 2.

Table 2. Comparison of Power Flow Solutions (3 Test Cases)

	Simulation Solution		Emulation Solution		Error	
Case #	Real V	Imag V	Real V	Imag V	%	%
1	0.950	-0.100	0.927	-0.102	2.421	2.000
2	0.900	-0.125	0.878	-0.128	2.483	2.010
3	0.875	-0.150	0.853	-0.153	2.545	2.100

VI. CONCLUSIONS

Analysis of the emulation test results in comparison to that provided by simulation demonstrates that use of the RALEM and emulation methods is an accurate and viable alternative to simulation. The emulated load bus power flow solution matches that provided by simulation with less than 3% error. The advantages of analog emulation outlined in the introduction section clearly outweigh this small error.

The next step of this research is to examine how this technology can be refined. Ideally this technology would be used to perform fast and accurate contingency analysis on large power systems. The technology lends itself to such a use as it yields an accurate solution quickly and is completely reconfigurable. The main restricting qualities of this technology currently are size and supply power consumption, however advances in VLSI (very large scale integration) technology will make allow the construction of small, efficient, and practical emulation hardware. The research presented in this paper is meant to be an initial step in the development of this system on a chip architecture.

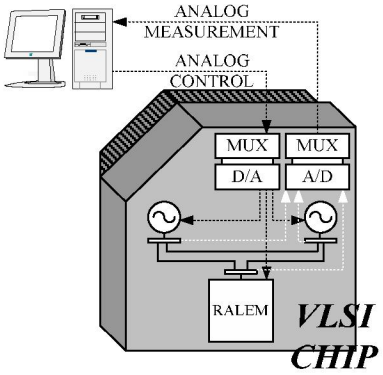

Fig. 7. System on a Chip Technology

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