Xenon difluoride etching of sacrificial layers for fabrication of microelectromechanical devices

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ABSTRACT OF THE
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Mechanical elements in microelectromechanical system (MEMS) structures require releasing in order to function correctly. Thus sacrificial layers must be etched away. Traditionally the etching of these sacrificial layers has been done with wet etching. However, this typically causes stiction related problems. One way to try to avoid stiction is to replace the use of liquids with dry vapor-based etch technologies.

Xenon difluoride (XeF_2) is a fluorine-based dry vapor etch that provides isotropic etching for e.g. silicon (Si). The purpose of this thesis is to present the characterization of the XeF_2 etch process with various different materials typically used in MEMS. Firstly, the etch rates for the materials are determined. The results show that poly-Si and molybdenum (Mo) are reactive materials, Tungsten (W) is a conditionally reactive material, SiO_2 and Si_3N_4 are low attack materials, Al_2O_3 and AlN are non-reactive materials. Secondly, the performed under etching tests provide a vertical etch rate of 3.8 - 4.9 µm / min for poly-Si sacrificial layers under photoresist mask and SiO_2 hard mask. The achieved etch rates are high enough that successful etching of polysilicon sacrificial layers can be obtained. The final test in this thesis presents results obtained from a simplified self-supporting device structure. A successful release demonstrating the vast potential of XeF_2 etching in microfabrication is obtained with a lateral etch rate of ~ 15 µm / min.

The vertical and lateral etching tests presented in this thesis, both with the test and device structures, provide important information about the behavior of XeF_2 in different etching environments. Based on the results it is possible to determine processes that are compatible with XeF_2 etching. Furthermore, the results presented here provide valuable help in determining the suitable etching parameters for the processes. Thus the data collected for this thesis is a useful reference when considering the implementation of XeF_2 etching.

Keywords: etching, dry etching, xenon difluoride (XeF_2) etching, dry vapor-phase etching, isotropic etching, microelectromechanical systems (MEMS)

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Mikroelektromekaanisten systeemien (MEMS) mekaaniset komponentit tarvitsevat komponentin valmistusvaiheessa mekaanisten osien vapauttamisen toimiakseen oikein. Vapautus on mahdollista toteuttaa syövyttämällä uhrautuvia kerroksia. Perinteisesti uhrautuvat kerrokset on syövytetty pois märkäsyövytyksen avulla. Märkäsyövytys aiheuttaa kuitenkin yleensä ongelman, jossa vapautetut elementit ja puhdas substraatti pääsevät kosketuksiin toistensa kanssa ja näin ollen tarttuvat toisiinsa. Pintojen tartuttua toisiinsa on niitä mahdotonta enää irrottaa. Hyvä tapa välttää tämä ongelma on vaihtaa märkäsyövytys kaasufaasi-syövytykseen.

Ksenondifluoridi (XeF_2) on fluoripohjainen kaasufaasi-syövytin, jonka avulla pitäisi pystyä syövyttämään isotrooppisesti esimerkiksi piitä (Si). Tämän diplomityön tarkoituksena on karakterisoida ksenondifluoridi-syövytysprosessi erilaisten syövytystestien avulla. Työn ensimmäisessä vaiheessa määritettiin tyypillisesti MEMS-rakenteissa käytettävien materiaalien syöpymisnopeuksia. Tulokset osoittavat, että poly-Si ja molybdeeni (Mo) ovat XeF_2 kaasulle reagoivia materiaaleja, Volframi (W) tietyissä olosuhteissa reagoiva, SiO_2 ja Si_3N_4 reagoivat rajoitetusti, kun taas Al_2O_3 ja AlN ovat materiaaleja, jotka eivät reagoi XeF_2 kaasulle lainkaan. Työn toisessa vaiheessa suoritetut alle-syöpymiskokeet osoittivat, että pystysuora syöpymisnopeus resistin tai oksidimaskin alla oleville uhrautuville poly-Si kerroksille on 3.8 - 4.9 µm / min. Nämä tulokset todistavat, että uhrautuvia poly-Si kerroksia voidaan etsata XeF_2 kaasulla onnistuneesti. Työn viimeisessä vaiheessa suoritettiin kattavia syövytyskokeita yksinkertaistetulle itsekantavalle rakenteelle. Edellä mainittu rakenne vapautettiin onnistuneesti ja lateraaliseksi syöpymisnopeudeksi mitattiin ~ 15 µm / min. Nämä tulokset osoittavat XeF_2 syövytyksen valtavan potentiaalin.

Työssä suoritetuista syöpymisnopeustesteistä, alle-syöpymistesteistä, sekä yksinkertaistetulle itsekantavalle rakenteelle tehdyistä syövytyskokeista saatiin erittäin tärkeää tietoa XeF_2 käyttäytymisestä erilaisissa tilanteissa. Tässä työssä esitettyjen tulosten perusteella on mahdollista määrittää ne prosessit, jotka ovat yhteensopivia XeF_2 syövytyksen kanssa. Tästä johtuen työhön kerätty data toimii hyödyllisenä vertailuaineistona sovellettaessa XeF_2 syövytystä.

Avainsanat: syövytys, kuivasyövytys, ksenondifluoridi-syövytys (XeF_2), kaasufaasi-syövytys, isotrooppinen syövytys, mikrosysteemit (MEMS)

Preface

First, I would like to thank my supervisor Prof. Hele Savin for giving me the opportunity to do this thesis under her supervision. Additionally, I am grateful for her efforts in guiding this thesis to the right direction. I am also extremely thankful to my advisor Jaakko Saarilahti. Without his guidance on the experimental part of the thesis, this work would only be a literature review. His expertise in micromachining and cleanroom work in general was highly valuable. I am also grateful to my other advisor Tuomas Pensala who made sure this thesis is a compact package of information. His ideas helped significantly during the writing process. The experimental part of this thesis was conducted in the cleanroom facilities of Micronova Nanofabrication Centre at VTT/Aalto University. I would like to thank cleanroom operator Kirsi Järvi for helping with the processing of the test samples and teaching the basics of lithography. Additionally, I would like to thank Jukka Lappeteläinen for always making sure that the XeF_2 etcher was up and running.

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I am extremely grateful to my family for all the love and support they have given throughout my life. Ville, without your efforts none of this would have been possible. There would be no degree nor thesis. Know that I am forever grateful for all the things you have done to help me succeed. Finally, I would like to thank my significant other. Sara, you have always been there for me no matter what. Thank you for the journey so far. I cannot wait to experience all the things life has in store for us.

Otaniemi, 15.2.2019

Jonne Vähänissi

"Risk comes from not knowing what you are doing!"
-Warren Buffett

Contents

Symbols and abbreviations

Symbols

A	exposed etching area [cm^2]
C	concentration
C_b	gas concentration
C_s	etch front concentration
D	diffusion constant
d	molecule diameter
ER	vertical etch rate
J	diffusion flux
N_A	Avogadro's constant
p	pressure
R	universal gas constant
S	vertical etch rate scaled to 1 cm^2
T	temperature [K]
t	time
U	backflow velocity
ε	reaction probability
λ	mean-free path
π	pi mathematical constant

Abbreviations

Al_2O_3	aluminum oxide
ALD	atomic layer deposition
AlN	aluminum nitride
Au	gold
BF_3	boron trifluoride
BrF_3	bromine trifluoride
BrF_5	bromine pentafluoride
ClF	chlorine monofluoride
ClF_3	chlorine trifluoride
CMOS	complementary metal-oxide-semiconductor
CZ	Czochralski process
DC	direct current
F	fluoride
F_2	difluoride
FBAR	film bulk acoustic resonator
Ge	germanium
H_2O	dihydrogen monoxide
HF	hydrofluoric acid
IC	integrated circuit
IF_5	iodine pentafluoride
IoT	internet of things
LPCVD	low-pressure chemical vapor deposition
MEMS	microelectromechanical systems
MFP	mean free path
Mo	molybdenum
MOS	metal-oxide-semiconductor
N_2	nitrogen
NF_3	nitrogen trifluoride
PECVD	plasma-enhanced chemical vapor deposition
PF_3	phosphorus trifluoride
PF_5	phosphorus pentafluoride
Poly-Si	polysilicon

PVDF-TrFE	polyvinylidene fluoride-trifluoroethylene
RF	radio frequency
SCCM	standard cubic centimeters per minute
SEM	scanning electron microscope
Si	silicon
Si_3N_4	silicon nitride
SiF_4	silicon tetrafluoride
SiGe	silicon-germanium
SiO_2	silicon oxide
Ti	titanium
TiW	titanium tungsten
W	tungsten
Xe	xenon
XeF_2	xenon difluoride

1. Introduction

Micro-electromechnical systems (MEMS) are tiny integrated devices that combine both electrical and mechanical components [1]. MEMS have the ability to generate effects on the macro scale and the ability to actuate, sense and control on the micro scale. In addition to integrated circuits, MEMS are the components that have enabled the building of the information society and their role is all the time becoming more significant as Internet of things (IoT) is on the verge of a complete breakthrough.

The evolvement of MEMS is highly dependent on the advances in microfabrication techniques. Etching and especially silicon etching is considered to be one of the most important processes in the fabrication of MEMS since devices that are designed for actuating or sensing purposes tend to require releasing or freeing of the microstructure [2]. The layers removed in the so-called releasing step or sacrificial process are referred to as sacrificial layers. The sacrificial processes in this context, refer to processes were a three-dimensional structure is manufactured via utilizing a sacrificial layer. The release etching can be realized by wet or dry techniques.

The most typical problem when utilizing wet etching in the releasing step is stiction. Stiction in this concept refers to the problem in which the freely moving microstructures stay adhered to each other, reducing the device yields [3]. This problem occurs when the solutions used in the etching process dry and the capillary force formed begins to pull the freely moving microstructures together or down to the substrate. Upon contact other forces such as electrostatic and van der Waals force are in key role when a permanent adhesion is formed again [3]–[6]. Additionally, wet HF etching will corrode all metals on the wafer that are exposed to it, e.g. aluminum.

To avoid these issues, dry vapor-phase etching has been proposed as a potential solution [2]. For example, xenon difluoride (XeF_2) and hydrogen fluoride (HF) have already been intensively researched and both vapors have been successfully utilized for this purpose. What makes vapor-phase etching even more attractive is the fact that it simplifies and replaces the whole sequence of etching while typical wet etching process requires multiple rinsing and drying steps. The simplicity of vapor-

phase etching can be explained by stating that the only process parameters required for a typical etching step are flow rates, pressure and temperature [7]. The downside of vapor-phase etching is that the current equipment are not suitable for batch processing. It is only possible to process a single wafer at a time, which prevents the utilization of vapor-phase etching in mass production. Additionally, the cost of XeF_2, is relatively large in comparison to solvents required in HF wet etching, which typically consist only of a mixture of HF and water.

This thesis will concentrate especially on XeF_2, which is a dry vapor etch that provides isotropic etching for silicon (Si), molybdenum (Mo), germanium (Ge) and silicon-germanium (SiGe). XeF_2 etching was first applied for MEMS back in 1995 at the University of California in Los Angeles [8].

The goal of this thesis is to characterize the XeF_2 etching process thoroughly and compare the obtained results with existing research. The first aim is to determine vertical etch rates for various materials typically used in MEMS. By determining the etch rates it is possible to divide the materials into four groups: 1) reactive materials; 2) conditionally reactive materials; 3) low attack materials; and 4) non-reactive materials. Determination of the etch rates is extremely important since, when a new process is being designed it is crucial to know the etch rates for each layer [9]. The second aim is to perform under etching tests, where the goal is to examine the etching process of few selected materials which are located under a masking material. This gives an idea how a real sacrificial etching step would function. The final goal is to conduct etching tests with a simplified device structure. The information gathered with these tests will be utilized when designing the XeF_2 etching step for the actual device structure. Overall, this thesis tries to provide all the necessary knowledge that is required for the implementation of XeF_2 etching into a new or an existing device process.

The structure of this thesis is divided into five chapters. First, a short introduction to the topic in general followed with an overview of XeF_2 etching in microfabrication is given. Topics such as the basic principles and application areas of XeF_2 etching are discussed. In addition, a comparison between XeF_2 and other vapor-phase dry etching methods is conducted. The third chapter concentrates on the experimental

methods used in this thesis. An overall look at the characterization of the XeF_2 etch process is presented. Obtained results are presented in chapter four. Finally, conclusions of the work are drawn in chapter five.

2. XeF_2 etching in microfabrication

This chapter covers the basic principles of XeF_2 etching. Topics such as theory behind XeF_2 etching, possible application areas and comparison to similar etching techniques are discussed.

2.1. Principles of XeF_2 etching

Xenon difluoride is a fluorine-based compound that can be used in dry vapor etching. It etch provides isotropic etching (at least) for Si, Mo, SiGe and Ge. The term fluorine-based indicates that when a chemical reaction between the XeF_2 gas and the substrate occurs, F_2 does the actual etching and Xe acts as the carrier gas. According to previous studies, XeF_2 has been reported to provide a high selectivity between Si and multiple typical MEMS materials, such as, photoresist, silicon dioxide, and aluminum. E.g. a selectivity of 1000:1 [10] has been reported between Si and SiO_2. This value means that the etch rate of Si is 1000 times faster than that of SiO_2. In other words, when 1000 nm of Si is etched, only 1 nm of SiO_2 is consumed. In addition of providing high selectivity, XeF_2 requires no ion bombardment or external energy sources to etch silicon, which makes it relatively easy to integrate with other processes. In normal conditions, XeF_2 is a white solid. However, pressures above the atmospheric pressure induce the XeF_2 to sublimate from solid to gas already at room temperature [8], [11]–[15].

The primary chemical reaction between XeF_2 and silicon is shown in equation (1),

$$2XeF_{2\,(g)} + Si_{(s)} \rightarrow SiF_{4\,(g)} + 2Xe_{(g)} \quad (1)$$

where SiF_4 is silicon tetrafluoride, *g* is gas and *s* is solid. Both, the primary reaction product SiF_4, and the secondary reaction product Xe, are volatile at room temperature [8], [11], [12], [16]–[19]. The etching process of Si with XeF_2 can be divided into a sequence of steps: 1) mass diffusion of the XeF_2 gas during which the gas diffuses (from the reactor) to the surface of the etch openings on the mask which act as the entry point for the gas; 2) diffusion of the gas during which the gas diffuses

through the etch openings all the way down to the cavity; 3) adsorption of XeF_2 during which the gas adsorption at the silicon surface takes place; 4) dissociation of the XeF_2 molecule; 5) formation of the Si-F bond; 6) desorption of the SiF_4; and 7) removing the products back to the reactor. [2] The whole process is described in detail in Figure 1. In addition, the different chemical reactions are shown in equations (2) - (5).

$$2XeF_{2\,(g)} + Si_{(s)} \rightarrow 2XeF_{2\,(ads)} + Si_{(s)} \tag{2}$$

$$2XeF_{2\,(ads)} + Si_{(s)} \rightarrow 2Xe_{(ads)} + 4F_{(ads)} + Si_{(s)} \tag{3}$$

$$2Xe_{(ads)} + 4F_{(ads)} + Si_{(s)} \rightarrow 2Xe_{(ads)} + SiF_{4\,(ads)} \tag{4}$$

$$2Xe_{(ads)} + SiF_{4\,(ads)} \rightarrow 2Xe_{(g)} + SiF_{4\,(g)} \tag{5}$$

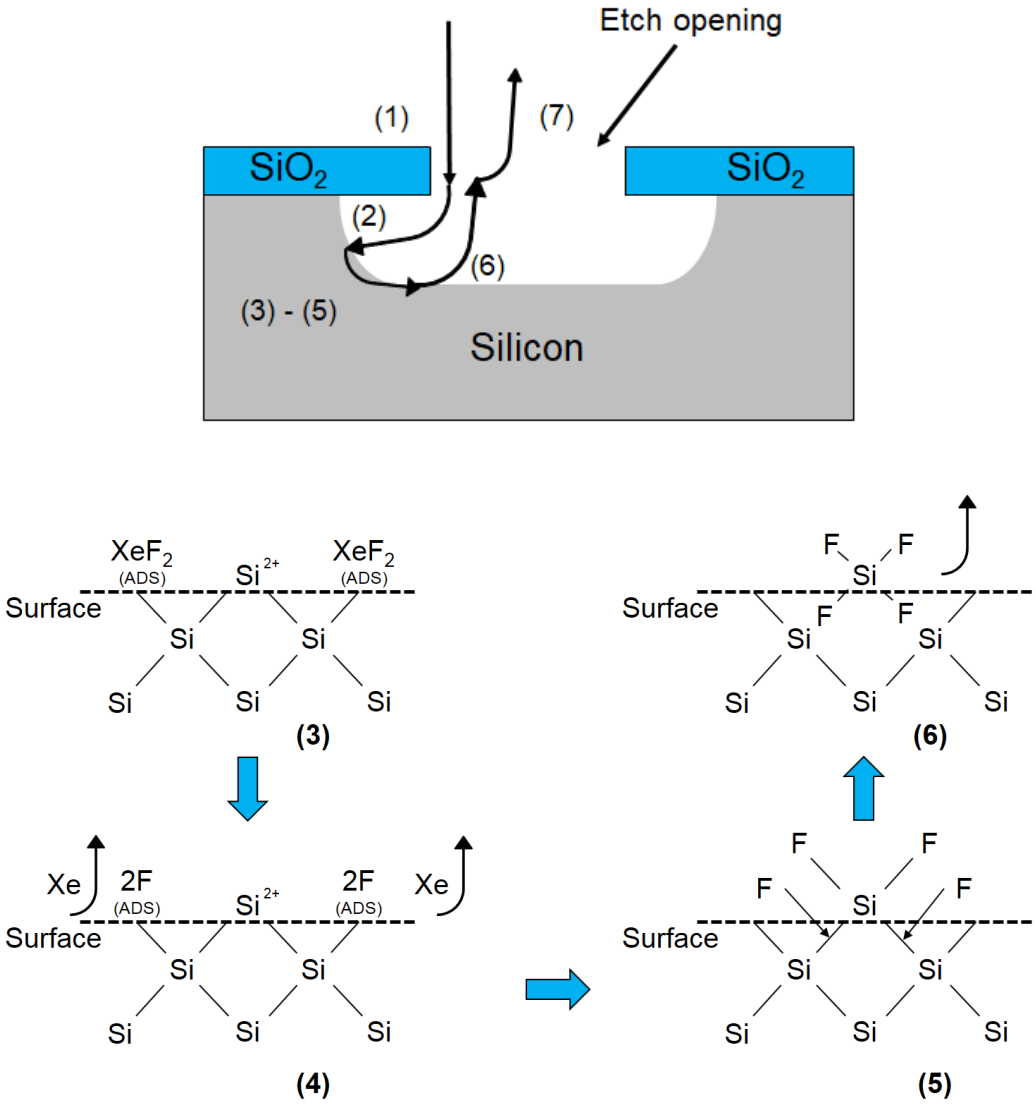


Figure 1. A basic schematic of the XeF_2 etching of silicon. The schematic depicts the different steps (1)-(7) during a typical silicon etching process with XeF_2. (1) Mass diffusion of the XeF_2 gas. The gas diffuses from the reactor to the surface of the etch opening. (2) The XeF_2 gas diffuses through the etching window to the etched cavity. (3) Adsorption of the XeF_2 gas. (4) Dissociation of the XeF_2 molecule. (5) Formation of the Si-F bond. (6) Desorption of the SiF_4. (7) The products are transferred back to the reactor from the wafer surface. This figure has been adapted from [2].

Typically, diffusion is the limiting factor in chemical reactions, which is also the case with XeF_2. A diffusion or a chemical reaction model, shown in equation (6), can be used to understand XeF_2 etching:

$$\frac{\delta C}{\delta t} + U \cdot \nabla C = D \cdot \nabla^2 C \tag{6}$$

where U is the backflow velocity, D is the diffusion constant and $C(x,y,z,t)$ is the concentration of the XeF_2 gas. If the convective term, which is the material derivative ($U \cdot \nabla C$), is neglected, equation (6) can be written as: [15]

$$\frac{\delta C}{\delta t} = D \cdot \nabla^2 C \tag{7}$$

Mean free path (MFP) is the average distance that a molecule or an atom can travel between collisions. It depends on the size of the molecule or the atom. As stated earlier, typically diffusion is the limiting factor in chemical reactions. Thus it is important to understand the relation between MFP and diffusion coefficient. Diffusion coefficient is the product of MFP, the average molecular speed and the average time between the collisions. MFP for the XeF_2 gas can be calculated from:

$$\lambda = \frac{RT}{\sqrt{2}\pi d^2 N_A p} \tag{8}$$

where T is temperature in kelvin, R is the universal gas constant, N_A is the Avogadro's constant, p is pressure in pascal and d is the molecule diameter.

The mean-free path for XeF_2 is about 10 µm at 3 Torr pressure, thus it can be assumed that the diffusion of the XeF_2 gas obeys Fick's law:

$$J = -D \cdot \nabla C \tag{9}$$

where J is the diffusion flux $(J = J_x, J_y, J_z)$.

For XeF_2 etching the boundary condition is:

$$C(x(t), y(t), z(t), t) = C_s \tag{10}$$

where *(x(t), y(t), z(t))* is the etch front and C_s is the etching front concentration. Small etching areas, such as chips, have smaller XeF_2 consumption due to smaller silicon volume. Thus it is possible to keep the XeF_2 gas concentration constant in the etching chamber. For this case, the initial condition for XeF_2 etching can be written as:

$$c(x, y, 0, t) = C_b \tag{11}$$

where symbol C_b describes the XeF_2 gas concentration in the chamber. In comparison, large etching areas, such as wafers, have higher XeF_2 consumption due to larger silicon volume. Thus the XeF_2 gas concentration changes as a function of time. For this case, the initial condition for XeF_2 etching can be written as:

$$c(x, y, 0, t) = C_b \cdot k_1(t) e^{-k_2(t)} \tag{12}$$

where the additional term $k_1(t)e^{-k_2(t)}$ describes the concentration of the XeF_2 gas as a function of time. Equations (6) - (12) described above can be used to understand and model the behavior of XeF_2 etching.

A typical setup required to conduct XeF_2 etching is shown in Figure 2. XeF_2 etching can be done with both continuous flow and pulsed flow modes. Typically, systems with high throughput tend to utilize continuous flow mode either with or without a carrier gas. In this case the gas is distributed to the process chamber via a showerhead. Additionally, the design of the chamber is done so that the gas flow will setup a boundary layer directly above the wafer. This boundary layer will allow a uniform diffusion of the reactive species thus resulting in a good etch uniformity across the wafer [20].

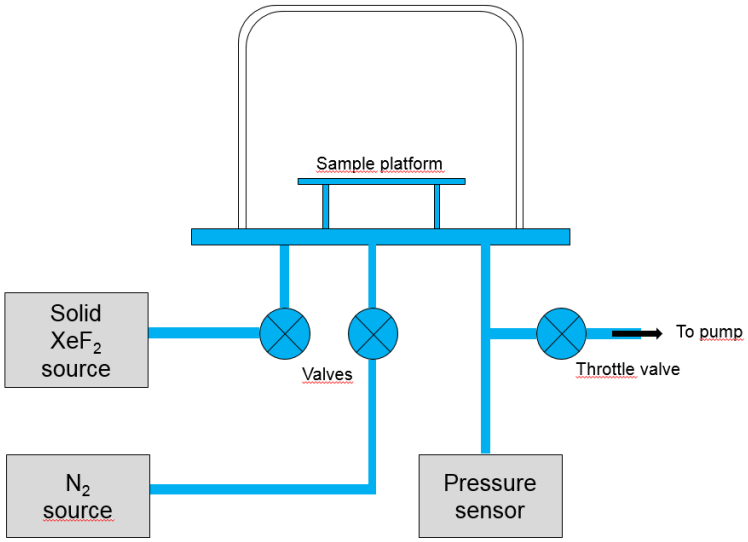
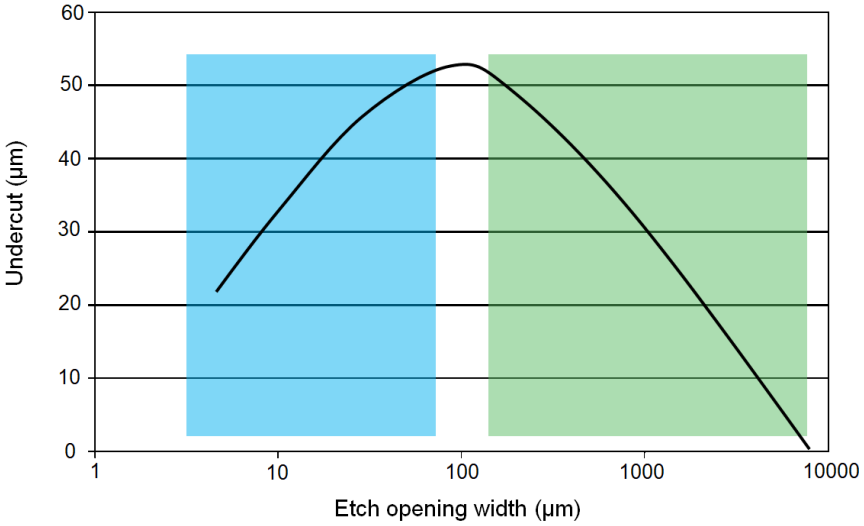


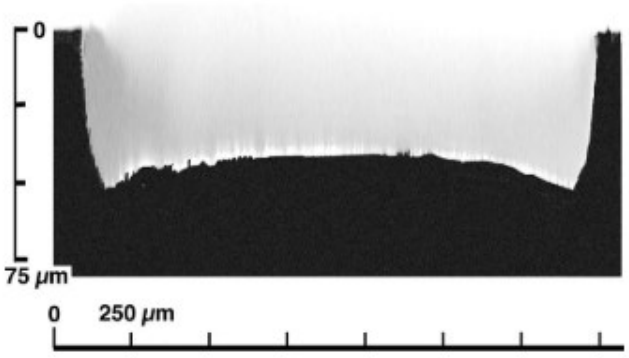
Figure 2. A simple schematic of a XeF_2 etch system. In a XeF_2 etching process the XeF_2 valve would be opened first. Simultaneously the pump is throttled in order to achieve the desired pressure. This is required to sublimate the XeF_2 from solid to gas. After the etching, the system is purged with an N_2 step.

In some cases, the pulsed flow mode may offer substantial advantages performance wise. The basic working principle of the pulsed flow mode is to have an isolated reservoir prior the actual process chamber. This isolated reservoir is filled with XeF_2 gas or a mixture of XeF_2 and e.g. nitrogen. The gas or the mixture is kept at a certain predetermined pressure. The process continues so that the valve between the reservoir and the actual process chamber is quickly opened, allowing a pulse of XeF_2 gas or the mixture to enter. The etching step continues until all of the XeF_2 has been consumed. After this the process chamber is evacuated and the cycle is repeated as many times as necessary [20]. The pulsed flow mode has three key advantages: 1) it has better penetration due to the rapid pulsing and evacuation of the process chamber, which will repeatedly push the XeF_2 deeper into long and narrow spaces; 2) by-products are removed after each cycle, which improves the selectivity; 3) maximum efficiency (which in this concept refers to the usage of the XeF_2) can be achieved if throughput is not a concern since the delay time between the pulses can be defined so that almost all of the XeF_2 is consumed [20]. Thus, the pulsed flow mode has been widely used in previous studies [11], [21], [22].

As described earlier in this chapter, when determining etch rates with XeF_2 etching, the most important factors are the amount of exposed silicon area and the size of the etch openings. Small areas of silicon tend to consume XeF_2 slowly resulting in etch rates that are approximately proportional to pressure. These processes are known as “pressure limited”. In comparison, large areas such as full-sized wafers consume all of the XeF_2 on contact. These processes are known as “flow limited” [20]. Additionally, the size of etch openings affects the etch rate significantly. For example, if the etching windows are between 5 to 100 µm in diameter, diffusion determines the etch rate. On the other hand, if the etching windows are between 100 to 10 000 µm, the exposed silicon area determines the etch rate, as shown in Figure 3. The size of the etch openings may also cause the trenching effect, which is also shown in Figure 3. The trenching effect appears when the diameter of the etch opening is much larger than the MFP.



a)



b)

Figure 3. a) A simple depiction of how the size of an etch opening affects undercut. Blue box on the figure indicates the area where the etch rate is determined by diffusion. Green box on the figure indicates the area where etch rate is determined by the exposed etching area. b) Illustrates the trenching effect, which is a situation where the etch depth at the edges is deeper than at the center. The trenching effect appears when the diameter of the etch opening is much larger than the MFP. This figure has been taken from [20] [23].

2.2. XeF_2 etching vs. other vapor-phase dry etching methods

Silicon can be etched spontaneously with various fluorine-based vapor etchants. Spontaneous in this context means that no plasma activation is required. Materials that belong to this family in addition to XeF_2 are chlorine trifluoride (ClF_3), bromine trifluoride (BrF_3), bromine pentafluoride (BrF_5), and iodine pentafluoride (IF_5). ClF_3 and BrF_3 have similar chemical properties as XeF_2, e.g. very low vapor pressure [24]. As XeF_2, also all the other four materials etch silicon isotropically and provide nearly complete selectivity over SiO_2 [23]. In addition, similarly to XeF_2, previous studies have shown that ClF_3, BrF_3, BrF_5 and IF_5 all seem to react with silicon from a physisorbed layer.

However, not all fluorine-containing compounds etch silicon spontaneously under the same conditions. E.g. previous studies have shown that the biggest difference between XeF_2 and other fluorides such as chlorine monofluoride (ClF), boron trifluoride BF_3, nitrogen trifluoride (NF_3), phosphorus trifluoride (PF_3) and phosphorus pentafluoride (PF_5) is the fact that XeF_2 is able to etch silicon spontaneously at room temperature, which is a substantial advantage [25].

In comparison to plasma etching, it is much more difficult to control the different parameters including the etch depth and the etch rate when using XeF_2 due to the overall simplicity of the etching process. Thus, as already stated earlier, XeF2 etching is typically applied in situations where the accuracy of the etching is not critical, e.g. in removal of sacrificial layers.

The vapor-phase etching of silicon is a similar process no matter which of the fluorine-based vapor etchants is used. In general, samples are exposed to reactive gases and areas that are not supposed to be etched are protected with masking materials. The gas molecules tend to travel randomly in the free space located above the sample. When the gas molecules collide with the surface of the sample they may stick to it. A reaction between the molecule and the substrate may occur, causing a formation of other compounds, which typically have a gaseous form. At some point

this will lead to the formation of a fluorosilyl layer, which comprises of Si atoms and F atoms [23].

A comparison between XeF_2 the other typical reactants ClF_3, BrF_3, BrF_5, IF_5, ClF, F_2 and F, is shown in Table 1. It compares etch rates, reaction probabilities and pressures of these reactants. There are significant differences in the etch rates. XeF_2 has the second highest silicon etch rate (45 300 Å/min) whereas BrF_3 has the highest silicon etch rate (50 000 Å/min), and F_2 has the lowest etch rate (3 Å/min).

XeF_2 has the highest reaction probability with silicon ($\varepsilon_{XeF2} = 1.2 \times 10^{-2}$). BrF_3 has the second highest ($\varepsilon_{BrF3} = 2.4 \times 10^{-3}$), but it is already five times less than ε_{XeF2}. F_2 has the lowest reaction probability ($\varepsilon_{F2} = 9 \times 10^{-9}$).

Table 1. Comparison of XeF_2 to various other reactants: pressures, silicon etch rates and reaction probabilities at room temperature. According to the chart XeF_2 provides the second highest etch rate (only slightly lower than BrF_3) and clearly the highest reaction probability (e.g. five times larger in comparison to BrF_3). This table has been adapted from [25].

Reactant	Pressure (Torr)	Etch rate (Å / min)	Probability ε(Si)
XeF_2	0.2	45 300	1.2×10^{-2}
ClF_3	4.7	5 500	4.5×10^{-5}
BrF_3	1.0	50 000	2.4×10^{-3}
BrF_5	8.1	11 800	7.8×10^{-5}
IF_5	4.6	9 900	1.3×10^{-4}
ClF	5.0	<10	$<6 \times 10^{-8}$
F_2	10	3	9×10^{-9}
F	0.2	4 600	4.1×10^{-4}

As stated earlier, there are various different dry etching process technologies that are utilized in the releasing of MEMS structures. However, there are two clear mainstream technologies that are widely used in both manufacturing and academia. These two mainstream technologies are XeF_2 etching and HF etching. As stated earlier, XeF_2 etching is an ideal solution when etching e.g. sacrificial polysilicon layers. However, if the sacrificial layer is fabricated from silicon dioxide (SiO_2), the best dry etching method is HF vapor-phase etching. Since it does not etch silicon, HF can be considered as a complementary technology with XeF_2. HF vapor etching technology is typically used in the release of polysilicon microstructures [3]. There are two possible ways to release a microstructure with HF vapor. In the first method, the standard HF (49%) is vaporized in an H_2O solution. The second approach uses anhydrous HF mixed with a catalyst that can be alcohol vapor, water vapor or a mixture of these two. As a side note, without the catalyst, the anhydrous HF will not etch SiO_2 at all.

In conclusion, XeF_2 belongs to the family of fluorine-based vapor etchants. It is one of the two mainstream gas phase etchants. As mentioned earlier, since HF etches SiO_2 and not e.g. polysilicon, it is a complementary technology to XeF_2. This means that XeF_2 and HF do not share possible application areas and thus there is demand for both of them. The downsides of XeF_2 etching include the rather high cost of the technique and the fact that typically only one wafer can be processed at a time. Since at least until now XeF_2 etching has not been the best option for mass production, there remains work to be done before it can be declared as the number one vapor-phase etching technology.

2.3. Application areas of XeF_2 etching

XeF_2 has been widely utilized for etching sacrificial silicon layers in R&D applications for multiple years. In certain situations, XeF_2 is preferred over HF since it offers advantages such as the ability to be utilized even when there are doped SiO_2 layers in the structure, a better compatibility with piezoelectric materials, a better silicon nitride selectivity and a low attack on SiO_2. In addition, the fact that polymers

are not penetrated nor attacked at all during etching makes it superior to HF in some application areas [20].

Current application areas of XeF_2 etching include optical MEMS, resonators, microphones, bolometers and RF switches. E.g. XeF_2 has been used in the fabrication of piezoelectric MEMS devices such as, resonators [11, 12], switches [28] and bulk acoustic wave filters [29]. All of these applications benefit from the fact that XeF_2 has a low attack on metals that are typically used as electrodes, on piezoelectric materials and on other materials that are utilized in order to tune the performance [20]. Additionally, by adding an XeF_2 etch step to the manufacturing process of piezoelectric MEMS, it is possible to simplify the fabrication significantly since it replaces the back side bulk process, which can often include both bonding and a simplified front side process that is used to remove the sacrificial silicon layer [20].

Studies have shown that by using XeF_2 in the fabrication process of RF switches, which includes both capacitive switches and contact switches, one can increase performance and yield [30]. This increase in performance and yield comes purely due to XeF_2 not attacking the metals nor the dielectrics used in the switches [20]. This is extremely helpful in the case of capacitive MEMS switches, where there are two metal electrodes that are separated from each other by a thin dielectric layer.

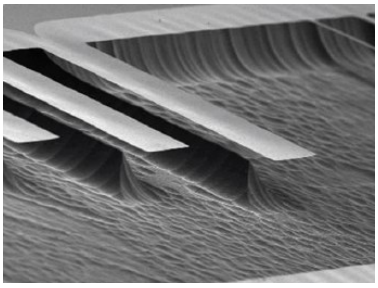
The fact that XeF_2 is compatible with aluminium makes it an ideal option for releasing MEMS mirrors, e.g., XeF_2 etching was utilized in the fabrication of the Stanford Grating Light Valve, which itself has been used to manufacture projected displays and optical attenuators by multiple different companies [31]. The choice of using XeF_2 etching was crucial to the process since it leaves the reflective aluminium surfaces optically unaltered. Additionally, the fact that XeF_2 has a low etch rate on SiO_2, was crucial in the fabrication of larger optical MEMS including the Analog Devices iMEMS mirrors [32].

XeF_2 etching has also been widely used in the fabrication of micro-bolometers and MEMS thermopiles [18, 19]. XeF_2 has been utilized in the creation of thermal isolation cavities and to define the structure. Mitsubishi IR-SC1 was the first camera

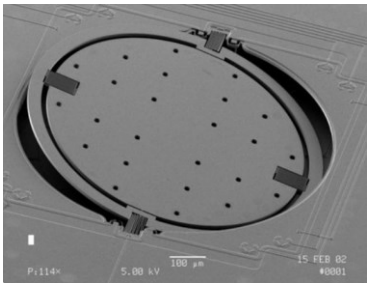
that had one of the first commercial IR sensors that was manufactured via XeF_2 etching. The ever increasing demand for better sensitivity requires even smaller and thinner sensing cells. Thus currently XeF_2 etching and atomic layer deposition (ALD) is used in the fabrication of micro-bolometer cells that are even thinner than 10 nm [35].

Even though XeF_2 etching is not typically utilized in the fabrication of traditional inertial MEMS, there are still emerging devices that could use it in the removal of sacrificial silicon layers. E.g., gyroscopes that are made using semi-spherical resonators benefit from the high selectivity that XeF_2 etching provides [21, 22].

Since XeF_2 etching provides very high selectivity for aluminium, SiO_2, SiN and photoresist, it is considered to be a very useful etchant for postprocessing of complementary metal-oxide-semiconductor (CMOS) integrated circuits [11], [24 - 25]. XeF_2 etching was originally utilized for exposing the undersides of MOS transistors. This was done by etching the underlying silicon substrate away [40]. A collection of images showing various applications that have utilized XeF_2 etching in the fabrication process is shown in Figure 4.



a)



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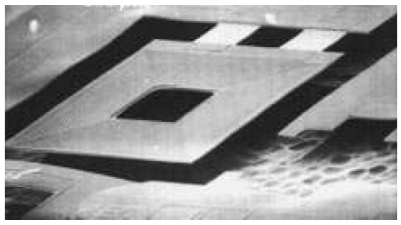
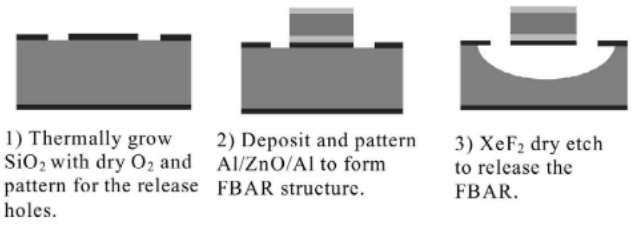


c)



d)

Figure 4. A collection of images showing the various applications that have utilized XeF_2 etching in the fabrication process. a) SEM image of cantilevers fabricated via XeF_2 release etch. b) SEM image of a silicon micromirror, the undercut is achieved with XeF_2 etching. c) A scanning electron microscope (SEM) image of a CMOS integrated circuit. The structure is a suspended rectangular spiral inductor, which consists of CMOS metallization layers. The undercut in the structure is done with XeF_2. d) Cross-sectional depiction of the fabrication process for a thin film bulk acoustic wave resonator (FBAR). The structure is released from the silicon substrate by using XeF_2 etching. The images to this figure have been taken from [29], [40], [41].

Some recent applications from 2018 that have utilized XeF_2 etching are microparabolic reflectors and MEMS resonators [42], [43]. The microparabolic reflectors are utilized in IR antenna coupled detectors. XeF_2 was chosen as the etch method due to its simplicity, cost efficiency and ability to create complex three-dimensional (3D) structures while still maintaining the CMOS compatibility. The fabrication process of the microparabolic reflector is shown in Figure 5. The process is divided into two parts: 1) part a, the creation of the cavity, and 2) part b, filling of the created cavity. In part a the cavity is created by using XeF_2 etching. First the sample is patterned with lithography. SU8 resist is used as masking material since it does not react with XeF_2. The etched cavity is then coated with gold (Au), which is deposited via RF sputtering. The XeF_2 etching parameters for this particular design are five cycles of 30 second pulses with 3 Torr input pressure. These parameters are similar to the ones used in this thesis on the simplified device structure.

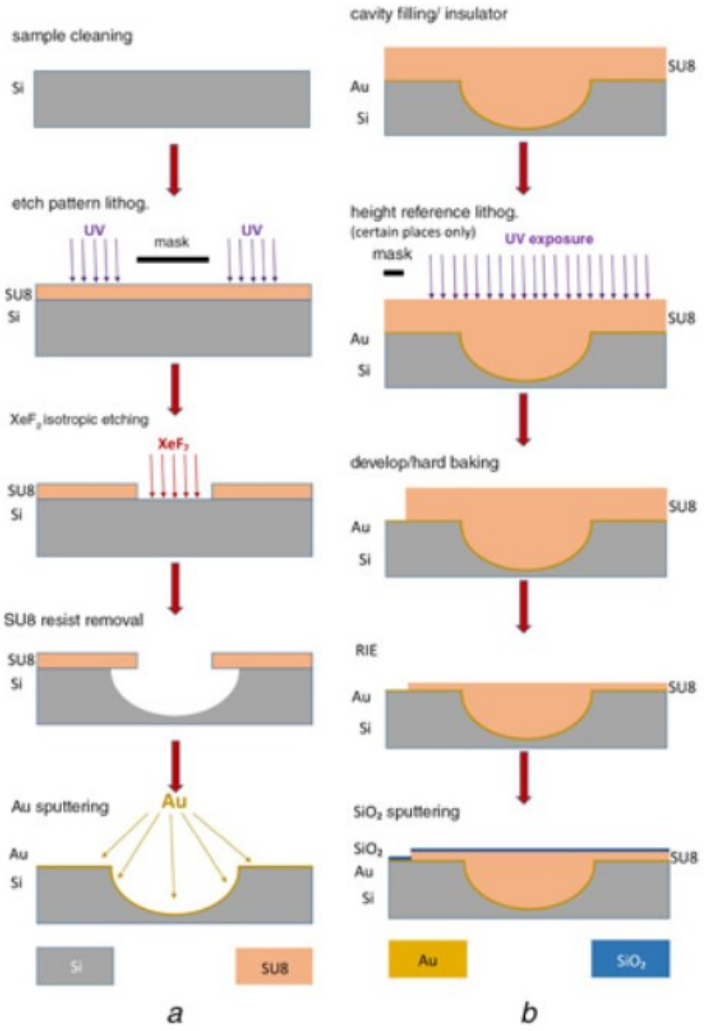


Figure 5. Full fabrication process of the microparabolic reflector. The process is divided into two parts. Part a consists of the steps required for the creation of the cavity and part b consists of the steps required for the filling of the cavity. The first step after standard cleaning is etch patterning, which is done with lithography. SU8 resist is used as a masking material since it does not react with XeF_2. After patterning, XeF_2 etching is utilized in the fabrication of the cavity. In the next step the etched the cavity is coated by sputtering Au. After sputtering the sample is patterned again. Next step in the process is reactive ion etching (RIE), which is used to reduce the thickness of the SU8 layer. Final step is SiO_2 sputtering. The figure is from [42].

XeF_2 etching has also been recently used in the fabrication of a polyvinylidene fluoride- trifluoroethylene (PVDF-TrFE)/SiO_2 composite film bulk acoustic resonator (FBAR), which is used for frequency-modulated sensor applications [44]. The process flow of the FBAR is shown in Figure 6. XeF_2 etching was used in the final step where the device is released from the underlying Si substrate.

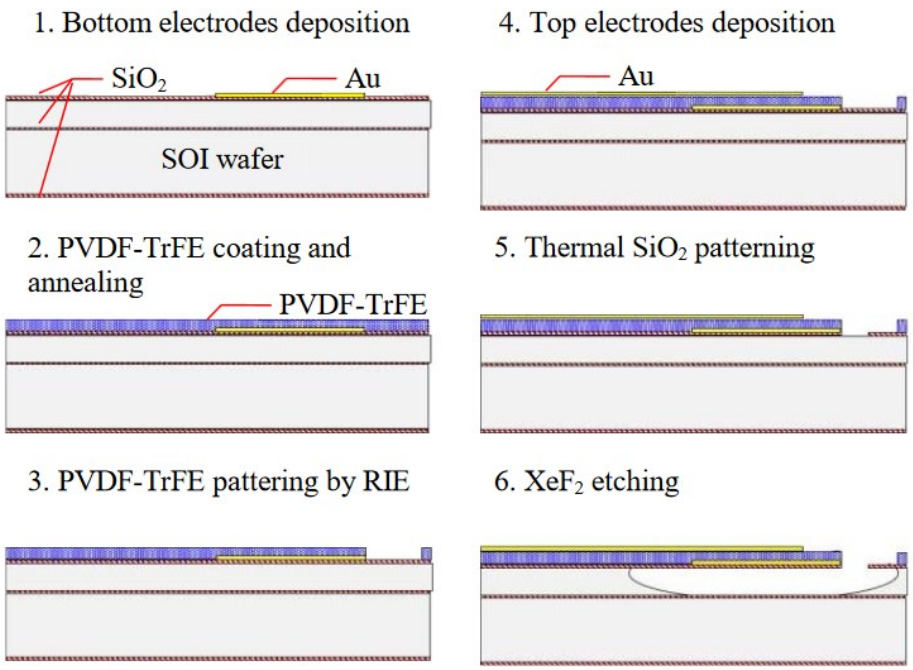


Figure 6. Fabrication process of PVDF-TrFE/SiO2 composite FBAR. XeF_2 etching was used in the final step where the device is released from the Si substrate. This figure has been taken from [44].

3. Experimental methods

This chapter covers the experimental methods used in this thesis to characterize the XeF_2 etch process. First, the fabrication of samples used in the experiments is described. Next, the details and the exact parameters of the actual XeF_2 etching are discussed. Finally, the characterization of the samples is described in detail.

3.1. Sample fabrication

In this thesis three different types of samples, denoted as groups A, B and C, were used. The different sample types are presented in Figure 7. Group A samples consisted only of a silicon substrate on top of which thin films were deposited prior to the XeF_2 etching. A patterned photoresist layer was used as an etching mask. Two different mask design were used depending on whether it was the intention to study the etch rates of different materials or the under etching. Group B samples had the same basic structure than group A samples, but prior to etching, a hard mask material was deposited on top and patterned via lithography. These samples were used in particular to study the under etching and the mask design was the same that was used for group A under etching samples. Group C samples were more complicated as they were used in testing XeF_2 etching in a typical device fabrication process. Prior to etching, the samples were preprocessed according to the process flow of a simplified device structure.

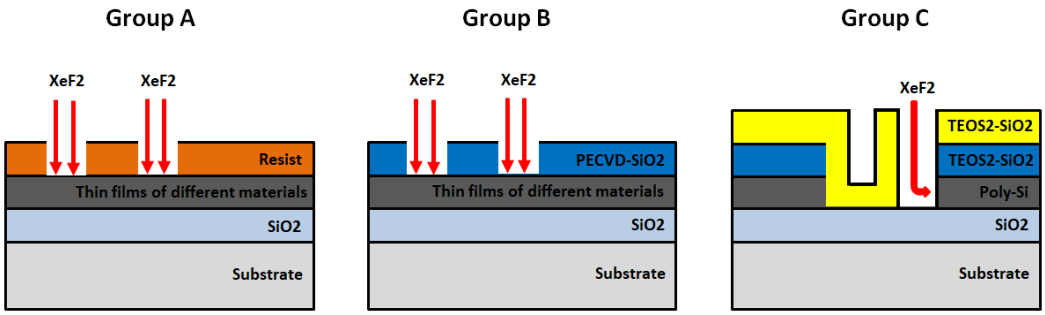


Figure 7. The different samples types. Group A samples consisted only of a silicon substrate on top of which thin films were deposited prior to the XeF2 etching. Group B samples had the same basic structure than group A samples, but prior to etching, a hard mask material was deposited on top. Group C samples were more complicated as they were used in testing XeF2 etching in a typical device fabrication process.

All the wafers used in the study were standard 150 mm single side polished (SSP) wafers. The substrate material was p-type Czochralski (CZ) silicon with thickness of 675 ± 15 µm, resistivity between 1-50 Ωcm and <100> orientation. The processing of all group A and B samples started with the same first preprocessing step, which was the standard SC1 + HF + SC2 cleaning sequence, also known as RCA clean. This was followed by thermal oxidation. The thermal oxidation was performed with a Centrotherm tube furnace at 1050 °C for 60 minutes with a target SiO_2 thickness of 500 nm. The process used wet oxidation, which has a faster deposition rate than dry oxidation. The basic reaction occurring during wet oxidation is:

$$Si(s) + 2H_2O(g) \rightarrow SiO_2(s) + 2H_2(g) \quad (13)$$

Oxide was removed from selected wafers and replaced by an approximately 1000 nm thick polysilicon layer. The polysilicon layer was grown with a Centrotherm tube furnace. AlN, Al_2O_3, Ti/Mo, Si_3N_4, SiO_2 and TiW/W films were grown on the wafers with thermal oxide. All the materials, deposition methods and recipes are shown in Table 2.

Table 2. Materials and deposition methods used in the etch rate tests.

Material	**Deposition method**
AlN	sputtering (Von Ardenne CS 730 S Sputtering system)
Al_2O_3	ALD (Picosun ALD reactor SUNALE R-150B)
Ti/Mo	sputtering (Von Ardenne CS 730 S Sputtering system)
poly-Si	LPCVD (Centrotherm diffusion furnace)
Si_3N_4	PECVD (Oxford Plasmapro system 100) LPCVD (Centrotherm diffusion furnace)
SiO_2	LPCVD (Centrotherm diffusion furnace)
TiW/W	sputtering (Von Ardenne CS 730 S Sputtering system)

Materials studied in this thesis were chosen due to the fact that they are used in current device fabrication processes at VTT. Thus the idea was to get as comprehensive study as possible. Another motivation to examine the XeF_2 etching of AlN, Al_2O_3, Ti/Mo, SiO_2 TiW/W and poly-Si was the fact that these all are used in a new device structure, which has been designed at VTT. Thus it is important to know their reaction with XeF_2 gas.

AlN, Ti/Mo and TiW/W were deposited via sputtering utilizing the Von Ardenne sputtering system, which has two chambers that can be used for direct current (DC), and radio frequency (RF) sputtering processes. AlN films were deposited in the DC chamber with pulsed DC. Ti/Mo and TiW/W, where both Ti and TiW function as the adhesion layers, were also deposited in the DC chamber. A 50 nm thick Al_2O_3 was grown with ALD reactor SUNALE R-150B. Si_3N_4, was deposited with plasma-enhanced chemical vapor deposition (PECVD) Oxford Plasmapro system 100 and Centrotherm low-pressure chemical vapor deposition (LPCVD) diffusion furnace. As with Si_3N_4, SiO_2 was also grown with Centrotherm LPCVD diffusion furnace.

For group A samples, after thin film deposition, a lithography step was carried out. Two different photomask designs were used. For samples used to determine the etch rate, the photomask design shown in Figure 8 and standard lithography was used. This mask created a total of four different etch opening shapes: 1) small rectangle; 2) large rectangle; 3) small circle; and 4) large circle. The diameter was 1561 µm for the smaller opening shapes and 1961 µm for the large opening shapes. The lithography step consisted of four different steps. The first step was priming, which was done with the Primer oven YES tool. After priming the wafers were coated with resists by using the Resist track AIO tool. The third step was exposure, which was done with Mask aligner SUSS MA150. After exposure the patterned resist was developed with Resist track AIO tool. All the equipment, recipes and process parameters used are listed in Table 3. For group A samples used in the under etching tests, another mask design and stepper lithography was used. The exposure step was done with Wafer Stepper FPA 3000 i4. Additionally, a reticle, shown in Figure 9,

was used instead of the earlier mask. After these steps the group A samples were ready for the actual XeF_2 etching.

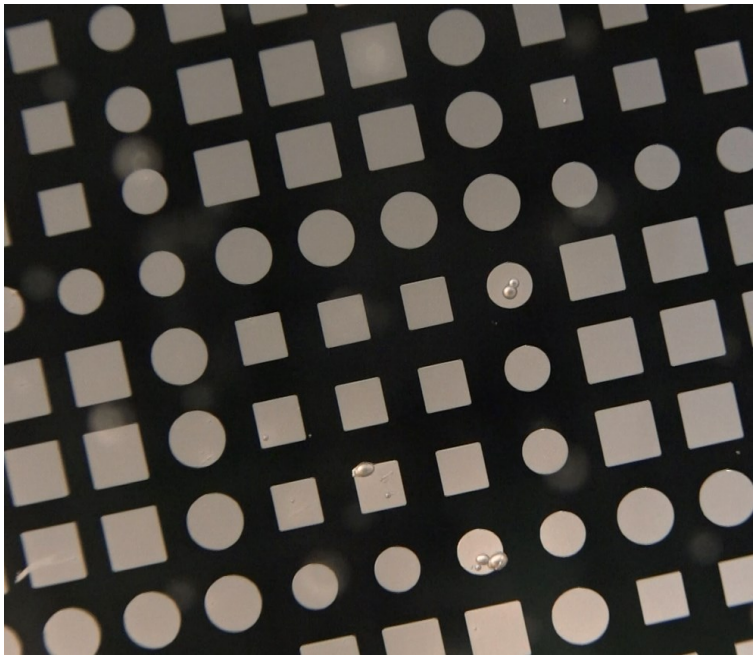


Figure 8. An image of a sample with the pattern created via lithography. The photomask that was used in the study provided a total of four different etching window shapes: 1) small rectangle diameter 1561 µm; 2) large rectangle diameter 1961 µm; 3) small circle diameter 1561 µm; 4) large circle diameter 1961 µm.

Table 3. A chart of the lithography process. The process consisted of four steps. Each step, equipment, recipe and process parameter is listed in the table. The resist used with all samples was positive photoresist AZ726 MIF.

Step	**Equipment**	**Process parameters**
Priming	Primer oven YES	HDMS 150 °C 20 min
Resist coating	Resist track AIO	SPR700, 2500RPM, 1.5 µm, Top EBR off, SB Contact 90C 60 s
Exposure	Mask aligner SUSS MA150	Exposure time 13 s, Intensity 26 mW/cm^2
Developing	Resist track AIO	AZ726 MIF, RT, 60 s

For group B samples used in the under etching tests, the process continued after the thin film depositions similarly as for group A samples. However, before lithography, an SiO_2 layer was deposited with PECVD Oxford Plasmapro system 100 to the samples to serve as a hardmask. After this lithography to pattern the hard mask was done similarly as in the case of group A under etching test samples. After the lithography the samples were etched with Oxide etcher LAM 4520. This was done in order to create the etch openings. After these steps the group B samples were ready for the actual XeF_2 etching.

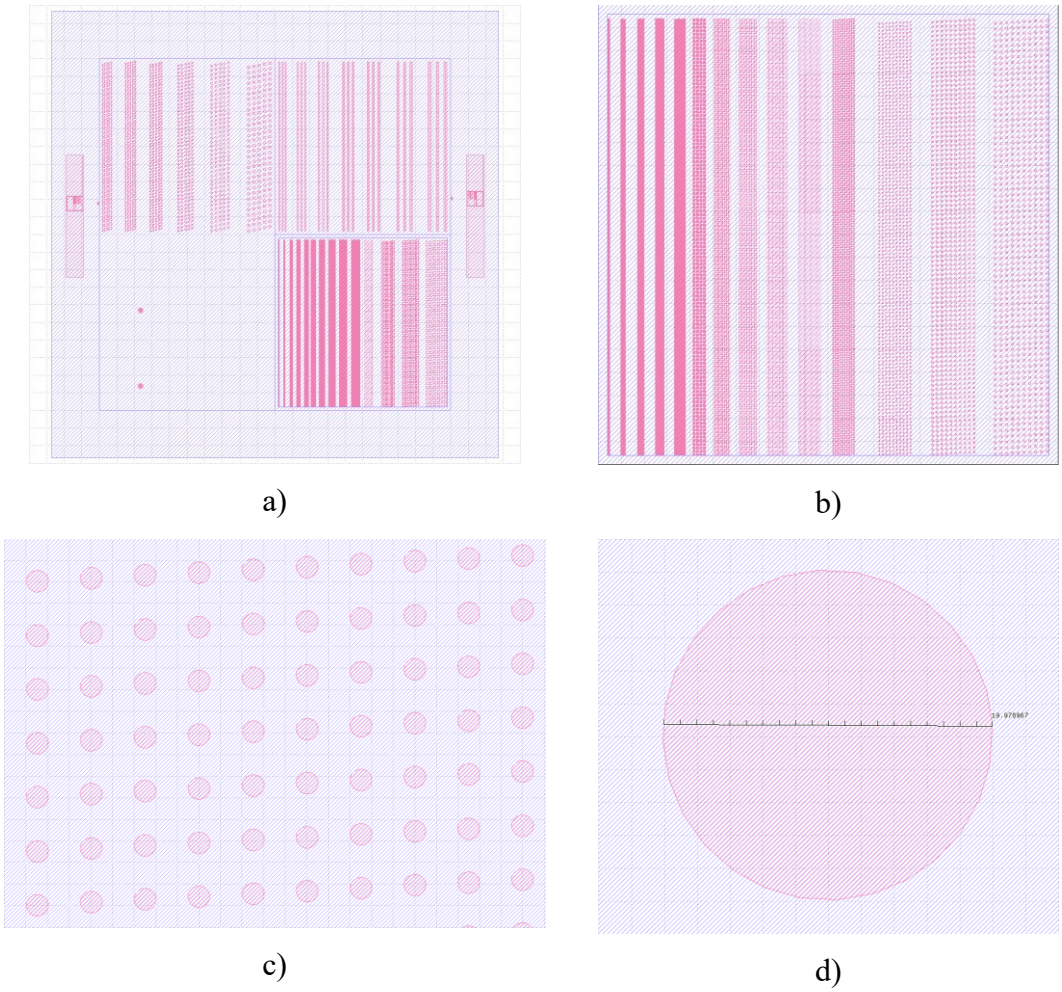


Figure 9. An image of the reticle. a) Full image of the reticle. The part used in the lithography process is the right bottom quarter. b) A magnification of the used quarter. The used part had a set of circles divided into columns. The columns were constructed with circles that had the same diameter. c) A magnification of the column that was used in the under etching study. d) Image of an individual circle. The diameter of the circle was 20 µm and the distance between each circle was 30 µm.

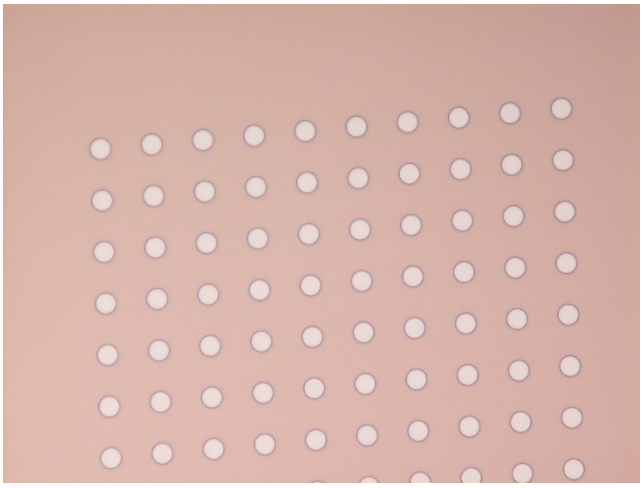


Figure 10. An optical microscope image of a typical group B sample (in this case TiW/W) after lithography. The diameter of the circles in the column is 20 µm and the distance between them is 30 µm.

For group C samples, the preprocessing necessary for the device structure was done prior to the XeF_2 etching. There were a total of five samples, which all had the same structure. First step was the deposition of a 1000 nm poly-Si layer, which was done on top of the 500 nm thermal oxide. This was followed by a 500 nm TEOS SiO_2 deposition. Poly-Si was deposited with Centrotherm diffusion furnace and TEOS SiO_2 was deposited with Centrotherm LPCVD diffusion furnace B2 TEOS. After depositions all the samples were annealed in Centrotherm diffusion furnace at 800 degrees for 30 minutes. Next step in the process was lithography, which was done to all the samples. The process followed the same steps as earlier expect that the exposure step was done with Wafer Stepper FPA 3000-i4. A total of 32 chips were on a single wafer. One chip contained 182 components.

After lithography, the next step was the fabrication of the lateral etch stop. This was done in order to limit the etched area. The etch stop was fabricated by etching a five micrometer wide trench to TEOS SiO_2 and poly-Si layers. The TEOS SiO_2 and poly-Si layers were plasma etched with Oxide etcher LAM 4520 and Polysilicon etcher LAM 4420. The etch rate for SiO_2 and polysilicon with these devices are approximately 500 nm and 350 nm per minute. Final phase in the lateral etch stop fabrication was the deposition of 500 nm thick LPCVD TEOS SiO_2 layer. After that it was necessary to open up a route for the XeF_2 gas. A 20 micrometer wide trench was plasma etched utilizing the same two etchers as above. Additionally, etching was

again stopped on the first SiO_2 layer. The full fabrication process of the simplified device structure is shown in Figure 11. The list of devices and recipes used in the plasma etching step are shown in Table 4. Selected designs from the reticle used in the lithography step are shown in Figure 12.

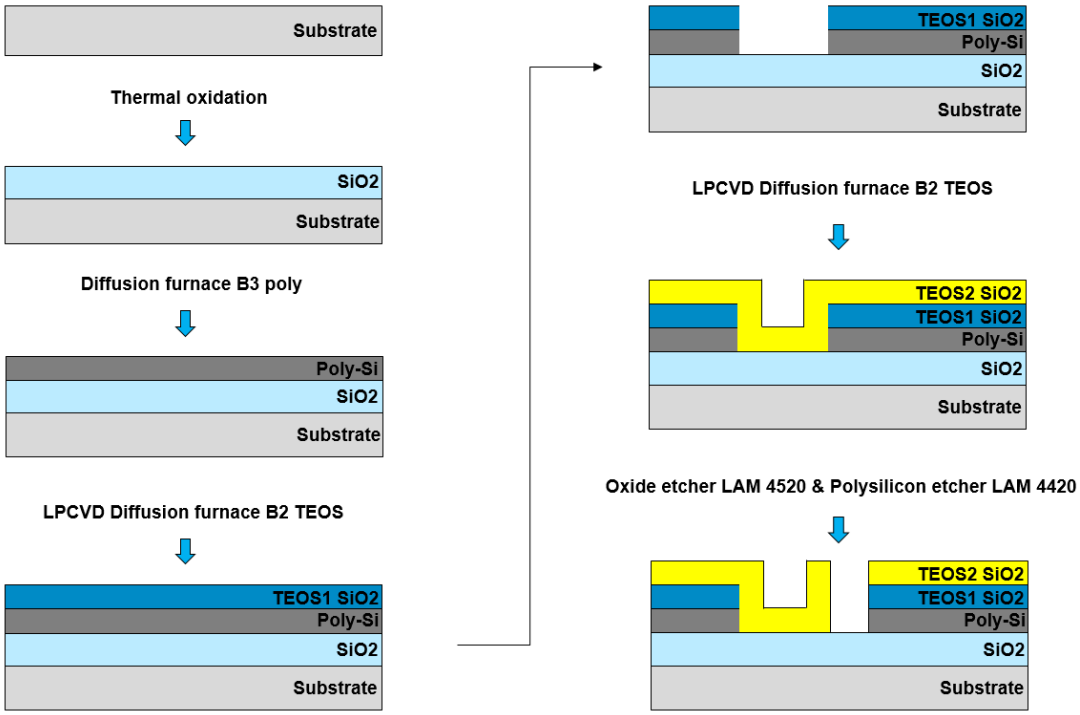


Figure 11. The full fabrication process of the simplified device structure used in the etch tests. First step in the process was thermal oxidation. The thickness of the first SiO_2 layer was 500 nm. Second step was poly-Si deposition. The thickness of the poly-Si layer was 1000 nm. Third step was the deposition of the TEOS SiO_2 layer, which was 500 nm. After the depositions the samples were annealed at 800 degrees for 30 minutes. Fifth step was the fabrication of the lateral etch stop, which started with the etching of 5 µm wide trench on TEOS SiO_2 and poly-Si. After etching another 500 nm thick TEOS SiO_2 layer was grown on top. Final step in the fabrication process was the etching of the trench. The purpose of the trench was to open a route for the XeF_2 etch step.

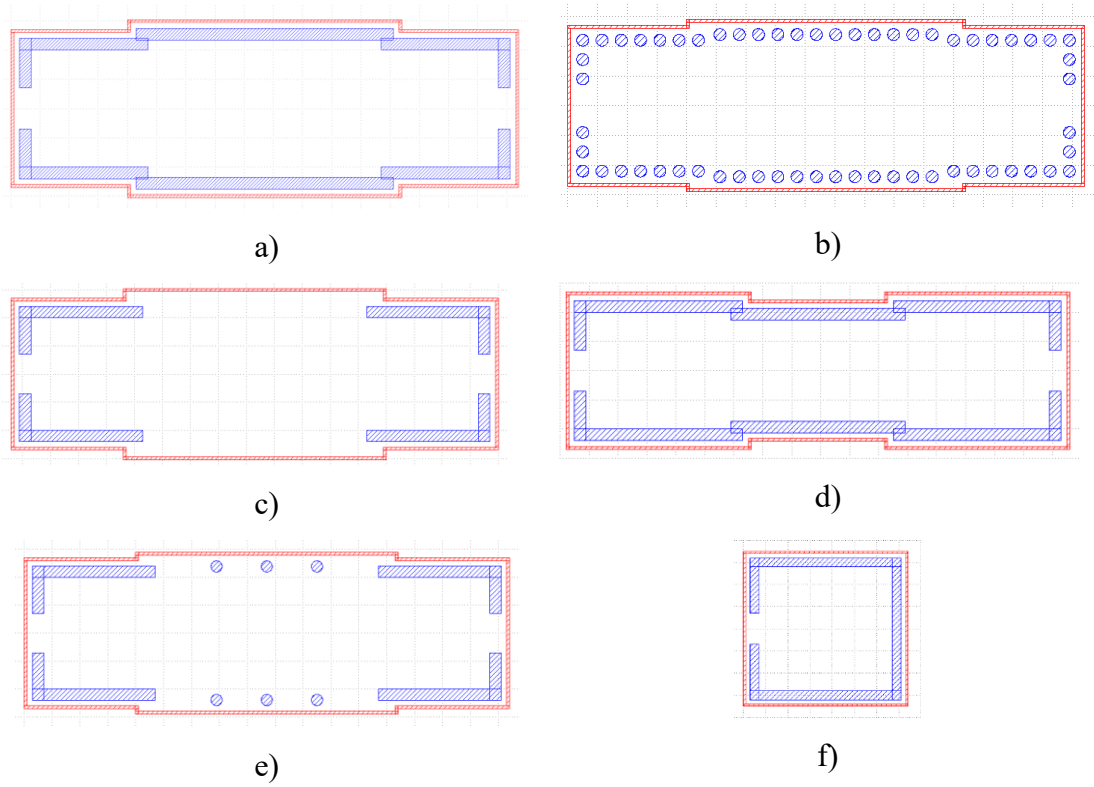


Figure 12. a)-f) Images of different etch opening designs taken from the reticle used in the simplified device structure etching tests. The lateral etch stop for each component was done according to the red structure and the trench was done according to the blue structure. The width of the red line is 5 µm and the width of the blue line is 20 µm. The distance between the two structures is 5 µm. a) The basic structure with maximum distance in the middle, which should thus require more etching than the other designs. b) The same basic structure but this time with circles as etching windows. c) A test structure with no etching windows in the middle. This should slow down the etching significantly. d) The basic structure with minimum distance in the middle, which should thus require less etching than the other designs. e) A test structure with the combination of circles and regular etching windows. f) A test structure for the simple rectangle component.

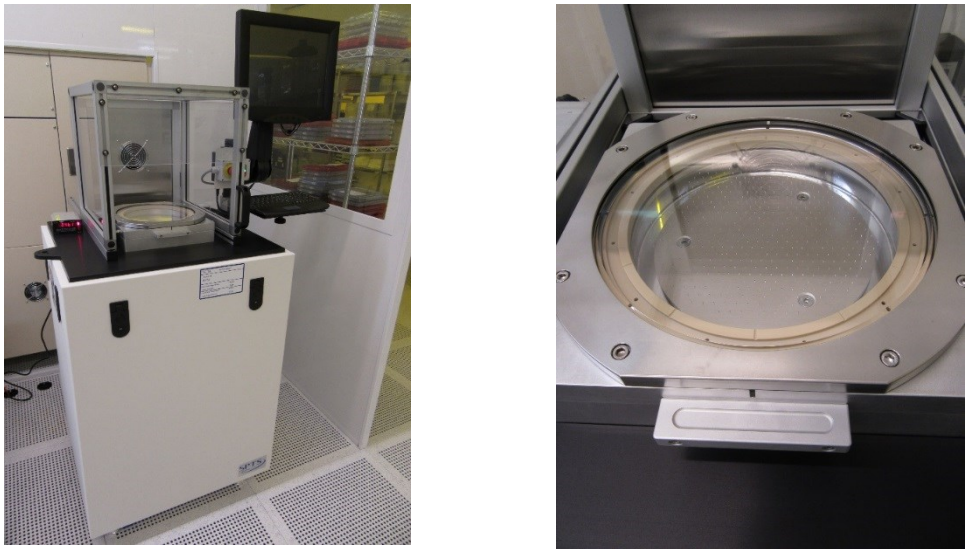
Table 4. List of tools and recipes used in the plasma etching steps.

Tools	**Etch rate**
Oxide etcher LAM 4520	approx. 500 nm/min
Polysilicon etcher LAM 4420	approx. 350 nm/min

3.2. XeF_2 etching

3.2.1. SPTS Xactix Xetch X4 Series XeF_2 Etcher

All the XeF_2 etching steps conducted in this thesis were done with SPTS Xactix Xetch X4 Series XeF_2 Etcher. An overall picture of the XeF_2 etcher and a close-up of its process chamber is shown in Figure 13. [45] The system has two expansion chambers which enables faster etching due to the possibility to increase the pressure of two gasses, used in the etching process, to the desired level at the same time, and a mass flow controller, which is used in the continuous process to control the XeF_2 flow. Additionally, it is possible to have two supplies for the XeF_2 gas. A basic schematic of the system can be seen in Figure 14.



a) b)

Figure 13. An image of the SPTS Xactix Xetch X4 Series XeF_2 Etcher. b) Etching chamber of the XeF_2 etcher. The purpose of the showerhead glass is to supply the XeF_2 gas uniformly for the sample. Under the sample platform there is a thermocouple that provides temperature information during the etching. The wafer holder, shown in image b), can be easily changed. The largest wafer holder for this particular etcher is for a 200 mm wafer.

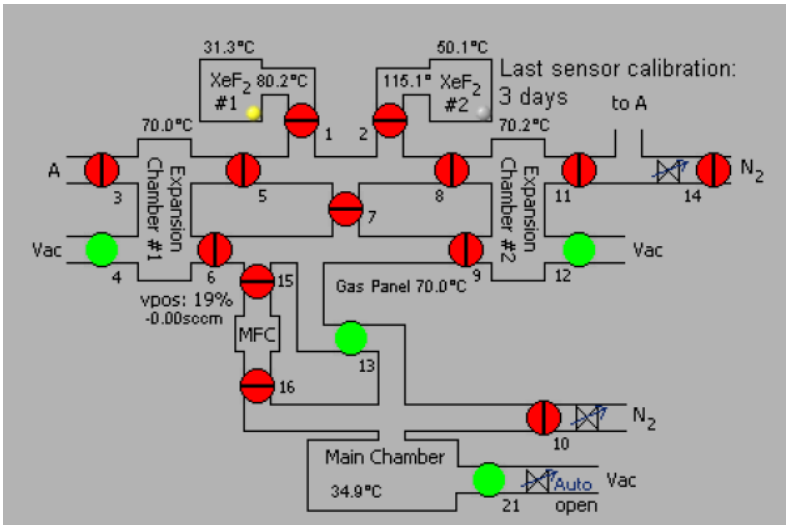


Figure 14. A basic schematic of the XeF_2 system (SPTS Xactix Xetch X4 Series XeF_2 Etcher). In the system there are two expansion chambers that enable faster etching. A mass flow controller used in the continuous process to control the XeF_2 flow. Additionally, there is also a possibility, as shown in the top, to have two supplies for the XeF_2 gas [45].

There are two possible processes when etching with the SPTS Xactix Xetch X4 Series XeF_2 Etcher. These processes are known as continuous flow and pulsed flow processes [45]. Both processes were used in the etching tests of this thesis. In a continuous flow process, the only three parameters that are required are etch time, pressure and flow. Thus a constant flow and pressure is maintained throughout the etching. In the SPTS Xactix Xetch X4 Series XeF_2 Etcher, there is only one working mode for continuous flow processes, which is called MFC Flow Through. In a pulsed flow process, the XeF_2 gas is pulsed in the chamber either with or without dilution. In addition, it is possible to add delays between the cycles. This allows the etched sample to cool down before the next pulse. In order to enhance the cool down of the sample, it is possible to add N_2 [45].

There are total of seven different etching modes in the SPTS Xactix Xetch X4 Series XeF_2 Etcher. These modes are Normal mode, Single Exp Normal, Advanced Normal, Multi-lot Etch mode, Normal with Delays, High conductivity and MFC Flow Through. In the normal mode, the XeF_2 gas is pulsed either with or without dilution. It is possible to add N_2 to the process in order to slow down the etch or improve the selectivity. The typical amount of dilution is between 5 and 10 Torr. Values that are below this range will have little effect. As mentioned above, the SPTS Xactix Xetch

X4 Series XeF_2 Etcher has two expansion chambers thus the Single Exp Normal mode, allows the user to determine whether to use one or two chambers. With only one expansion chamber the overall etch time is increased due to the fact that the chamber has to be completely empty before re-filling. The Advanced Normal mode, allows the user to determine a threshold on how far the expansion and process chambers are pumped before the following cycle is started. In the Multi-lot Etch mode, it is possible to determine the recipes and the sequences of recipes ahead of time. This is typically useful if a technician is conducting an experiment. In the Normal with Delays mode, it is possible to add a delay between the cycles. This is mainly done in order to allow the sample to cool down before the next cycle. The High Conductivity mode, is similar to the previous mode. However, this mode allows the addition of N_2 during the delay step. The addition of N_2 helps the sample to cool down better. The MFC Flow Through mode, can be said to be the simplest mode since, there are only three parameters to set. These parameters are etch time, pressure and flow. Typically, it is faster to etch with this mode than with pulsed modes since, after the process chamber reaches the target pressure the system is in a steady state. As an example, a typical continuous flow recipe could be 0.5 Torr, 5 sccm for several minutes. The modes used in this thesis were MFC Flow Through, High Conductivity, Normal with Delays and Normal mode.

3.2.2. Description of the used XeF_2 processes

Four recipes in total were used in this study. All the recipes are named after the parameters. First recipe that was utilized was 5m0.5p5s (MFC Flow Through), which is a continuous flow recipe. Parameters required for this recipe, as the name implies, are flow (5 sccm), pressure (0.5 Torr) and total etch time (5 min). The values on the recipe name are pre-set values, which are altered according to the etching process. The only parameter that was altered during the study was total etch time, others remained as constant. Second recipe used in the study was de10x30x10-3.0p0.0n (High Conductivity), which is a pulsed flow recipe. Parameters required for this recipe are number of cycles, etch time, chill, time, XeF_2, N_2 and chill pressures. In this recipe, as described in the previous paragraph, it is possible to add a pulse of N_2 during the delay to enhance the cool down of the sample. Again, numbers in the

recipe name indicate the pre-set values for the different parameters, e.g. 10 cycles, 30 seconds etch, 10 second chill time, 3.0 Torr pressure for XeF_2 and 0.0 Torr pressure for N_2. Third recipe utilized in the study was de10x30x10-3.0p0.0n (Normal with Delays), which is almost identical with recipe number two, only difference is that it is not possible to add N_2 to the delay step. The fourth recipe used was no10x15-3.0p0.0n (Normal mode), which is also a pulsed flow recipe. Parameters required for this recipe are number of cycles (10 cycles), etch time (15 s) and XeF_2 pressure (3.0 Torr). In addition, it is possible to add N_2 (0.0 Torr) in order to improve selectivity or to slow down the etching process. Again, the recipe name indicates the pre-set parameters. All etching recipes and parameters used in this thesis are shown in Table 5. Most of the materials were etched with different recipes. The combinations are shown in Table 6.

Table 5. Table of the recipes used in the study. Each parameter is explained in detail to understand the differences of the recipes.

Parameter	**MFC Flow Through: 5m0.5p5s**	**High Conductivity: de10x30x10-3.0p0.0n**	**Norma with Delays: de10x30x10-3.0p0.0n**	**Normal mode: no10x15-3.0p0.0n**
Etch time[1]	X / (5 min)	X / (30 s)	X / (30 s)	X / (15 s)
Flow[2]	X / (5 sscm)			
XeF_2 pressure[3]	X / (0.5 Torr)	X / (3.0 Torr)	X / (3.0 Torr)	X / (3.0 Torr)
N_2 pressure[4]		X / (0.0 Torr)	X (optional)	X (optional)
Chill pressure[5]		X / (3.0 Torr)		
Chill time[6]		X / (10 s)		
Etch delay[7]			X / (10 s)	
Number of cycles[8]		X / (10 cycles)	X / (10 cycles)	X / (10 cycles)

[1] Etch time defines the duration of the etch step.

[2] Flow defines the flow in standard cubic centimeters per minute [$\boldsymbol{cm^3/min}$].

[3] XeF_2 pressure determines the pressure of XeF_2 in Torr

[4] N_2 pressure defines the pressure of N_2 in Torr. Adding N_2 can improve the selectivity since it dilutes the mixture. Alternatively, the etch can also be slowed down by adding N_2.

[5] Chill pressure determines the pressure that is maintained during the chill time when the sample is cooling.

[6] Chill time determines the time reserved for cooling the sample between cycles.

[7] Etch delay defines the time used for delays between the etch cycles. Allows the sample to cooldown before the next cycle.

[8] Number of cycles determines the total amount of etch cycles.

Table 6. A list of materials and recipes used in etching. Numbers in the recipe name indicate the pre-set values for the different parameters, e.g. de10x30x10-3.0p0.0n means 10 cycles, 30 seconds etch, 10 second chill time, 3.0 Torr pressure for XeF_2 and 0.0 Torr pressure for N_2.

Material	**XeF_2 etcher recipe**
AlN	5m0.5p5s (MFC Flow Through) de10x30x10-3.0p0.0n (High Conductivity) de10x30x10-3.0p0.0n (Normal with Delays) no10x15-3.0p0.0n (Normal mode)
Al_2O_3	5m0.5p5s (MFC Flow Through) de10x30x10-3.0p0.0n (High Conductivity) no10x15-3.0p0.0n (Normal mode)
Ti/Mo	5m0.5p5s (MFC Flow Through) de10x30x10-3.0p0.0n (High Conductivity)
Poly-Si	5m0.5p5s (MFC Flow Through)
Si_3N_4	5m0.5p5s (MFC Flow Through) de10x30x10-3.0p0.0n (High Conductivity) de10x30x10-3.0p0.0n (Normal with Delays) no10x15-3.0p0.0n (Normal mode)
SiO2	5m0.5p5s (MFC Flow Through) de10x30x10-3.0p0.0n (Normal with Delays)
TiW/W	5m0.5p5s (MFC Flow Through) de10x30x10-3.0p0.0n (High Conductivity)

3.3. Characterization methods

The characterization of the samples was done with either Reflectometer (FilmTek 2000M), Stulys profilometer (Veeco Dektak V200Si) or an optical microscope depending on the sample. In order to obtain the vertical etch rate it is necessary to measure the etch depth of the etched recess. This can be done either with a reflectometer or with a stulys profilometer, depending on if the thin film is transparent or not. In order to obtain the lateral etch rate it is necessary to measure the width of the etched cavity. This can be done with an optical microscope.

FilmTek 2000M is a system designed for material characterization, especially for thin film thickness measurements [46]. In this thesis, the tool was used to manually measure the thin film thicknesses in different locations. Samples with Al_2O_3, SiO_2, Si_3N_4, and poly-Si were measured with FilmTek. The FilmTek measurements were conducted after each etching step. All the measurement locations can be seen in Figure 15. For each sample a total of ten positions was measured.

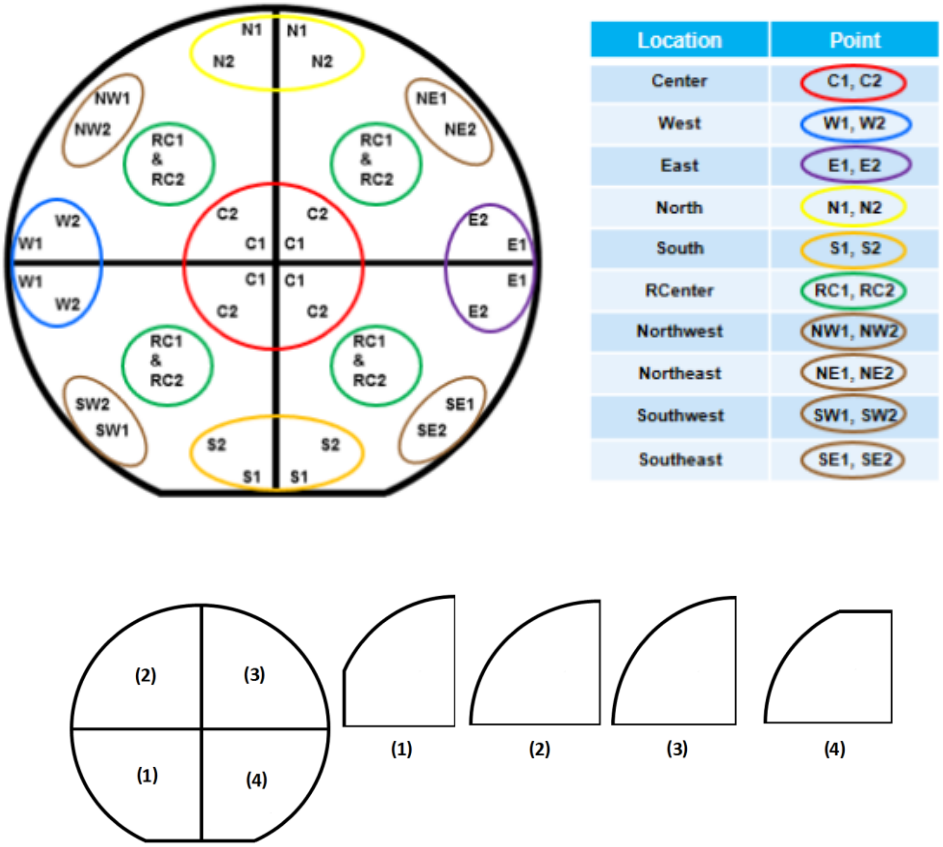


Figure 15. Thickness measurement locations. All the samples were measured from ten different spots after each etching step. For a full-sized wafer the measurements were taken in the following locations: Center 1, Center 2, West 1, West 2, East 1, East 2, North 1, North 2, South 1 and South 2. For the quarter pieces the measurements were taken in the following locations, depending on which piece was under study: Center 1, Center 2, West 1, West 2, East 1, East 2, North 1, North 2, South 1, South 2, Real Center 1, Real Center 2, Northwest 1, Northwest 2, Northeast 1, Northeast 2, Southwest 1, Southwest 2, Southeast 1 and Southeast 2.

Veeco Dektak V200si stulys profilometer was used to manually measure the thin film thicknesses in different locations. Samples that were impossible to measure with the Reflectometer FilmTek 2000M were measured with the stulys profilometer. These materials were AlN, Ti/Mo and TiW/W [47]. The thin film thicknesses of the samples were also measured from ten different positions. The measured positions are shown in Figure 15. Since these samples were characterized with a stulys profilometer it was necessary to remove resist from the wafers. The removal of the resists was done by dipping the samples into a container that was filled with acetone. Each sample was kept in the container for 20-25 minutes.

FilmTek 2000M and Veeco Dektak V200Si were used in the vertical etch rate characterization of the materials, which was the initial part of the study. Since they both measure the thin film thickness, only the etch depth and the vertical etch rate was determined.

The under etching samples were characterized with an optical microscope. An image was taken after each etching step and the images were imported to Klayout software [48] which is a layout viewer and editor used to create, e.g. photomasks and reticles. The images were positioned on top of the used reticle design in order to obtain the under etch rates. In this test only the lateral etch rate was studied, thus there are no measurements for vertical etch rates.

The simplified device test structure samples were also characterized with an optical microscope. Multiple images were taken after each etching step to compare the behavior of different designs. Images were taken with both a regular optical microscope and an optical microscope with infrared (IR) detector. With the latter it was possible to determine an approximation for the poly-Si etch rate. The optical microscope with IR detector was operated via computer by Matrox Inspector 8 software. The software allowed to measure distances in pixels. With a conversion table it was possible to convert these lengths measured in pixels to nanometers. Parameters used in the conversion are shown in Table 7 and the users of the optical microscope have determined these values. As mentioned above, in this test only the lateral etch rate was studied, thus there are no measurements for vertical etch rates,

however, in this case it is not necessary to know the vertical etch rate since the lateral length is a lot larger and thus the vertical length will be etched in any case.

Table 7. Pixels to nanometers conversion table for the optical microscope with IR detector. The chart depicts the equivalent for one pixel distance in nanometers depending on the used magnification. The conversion table has been created by users of the optical microscope.

Magnification	Pixel	Distance in nanometers (nm)
100x	1	84.7
50x	1	166.4
20x	1	413.1
10x	1	826.2
5x	1	1652.4

4. Results and Discussion

The goal of this thesis was to characterize the XeF_2 etch process thoroughly. This chapter presents all the measured data, the analysis done based on the data and thoroughly discusses the findings. In addition, the obtained results are compared with manufacturer's data and data found in literature. Finally, some future perspectives are discussed.

4.1. XeF_2 etching tests

4.1.1. Etch rates & selectivities

The vertical etch rates in this study were determined from the measured thin film thicknesses by dividing the etch depth with etching time. The calculated etch rates are shown in Table 8 & 9 and presented in Figure 16. For Al_2O_3, AlN, LTO-SiO_2 and PECVD-Si_3N_4 etch tests the exposed etching area was 9.8 cm^2. Due to this, the scaling was done simply by taking the product of the vertical etch rate and the exposed etching area. This was the case for poly-Si and LPCVD-TEOS-SiO_2 as well, except these two samples were only etched with the total exposed etching area of 39.2 cm^2, thus the area used in the calculations was different. For LPCVD-Si_3N_4, Ti/Mo and TiW/W, etch tests were conducted with both exposed etching areas. Thus the scaling was done by taking the product of the vertical etch rate and the exposed etching area for both data points and then taking the average of these two values. In general, this type of scaling gave reasonable values since they matched quite well with previous studies. Thus the approximations were sufficient for this study. The values for Ti/Mo and TiW/W had surprising variation between the different exposed etching areas. This could have been due to problems with sputtering. There was high variation in the thickness of both films in different locations on the wafer, which leads to problems since it was assumed that the thickness of the thin film was uniform across the wafer.

The scaling of the vertical etch rates was done as shown in equation (14):

$$ER \cdot A = S \tag{14}$$

where ER is vertical etch rate (nm / min), A is exposed area (cm^2) and S is the vertical etch rate (nm / min) scaled to 1 cm^2.

*Table 8. A list of vertical etch rates for each material. The etch rates presented here are averages calculated from the measured data. First part in the table presents the results for materials with exposed etching area of 9.8 cm^2. Second part in the table presents the results for materials with exposed etching area of 39.2 cm^2. In the final part the results for all the materials are scaled to etch rate (nm / min) per 1 cm^2. Symbol * after vertical etch rate indicates that the value is an average of the 9.8 cm2 and 39.2 cm2 values.*

Material	**Vertical etch rate [nm / min]**
Exposed etching area 9.8 cm^2	
Al_2O_3	0
AlN	0
LPCVD-Si_3N_4	12
LTO-SiO_2	2
PECVD-Si_3N_4	20
Ti/Mo	60
TiW/W	53
Exposed etching area 39.2 cm^2	
LPCVD-Si_3N_4	4
LPCVD-TEOS-SiO_2	0.1
Poly-Si	100
Ti/Mo	57
TiW/W	16
Vertical etch rates scaled to 1 cm^2 [nm / min]	
Al_2O_3	0
AlN	0
LPCVD-Si_3N_4	137*
LPCVD-TEOS-SiO_2	4
LTO-SiO_2	24
PECVD-Si_3N_4	194
Poly-Si	3930
Ti/Mo	1370*
TiW/W	613*

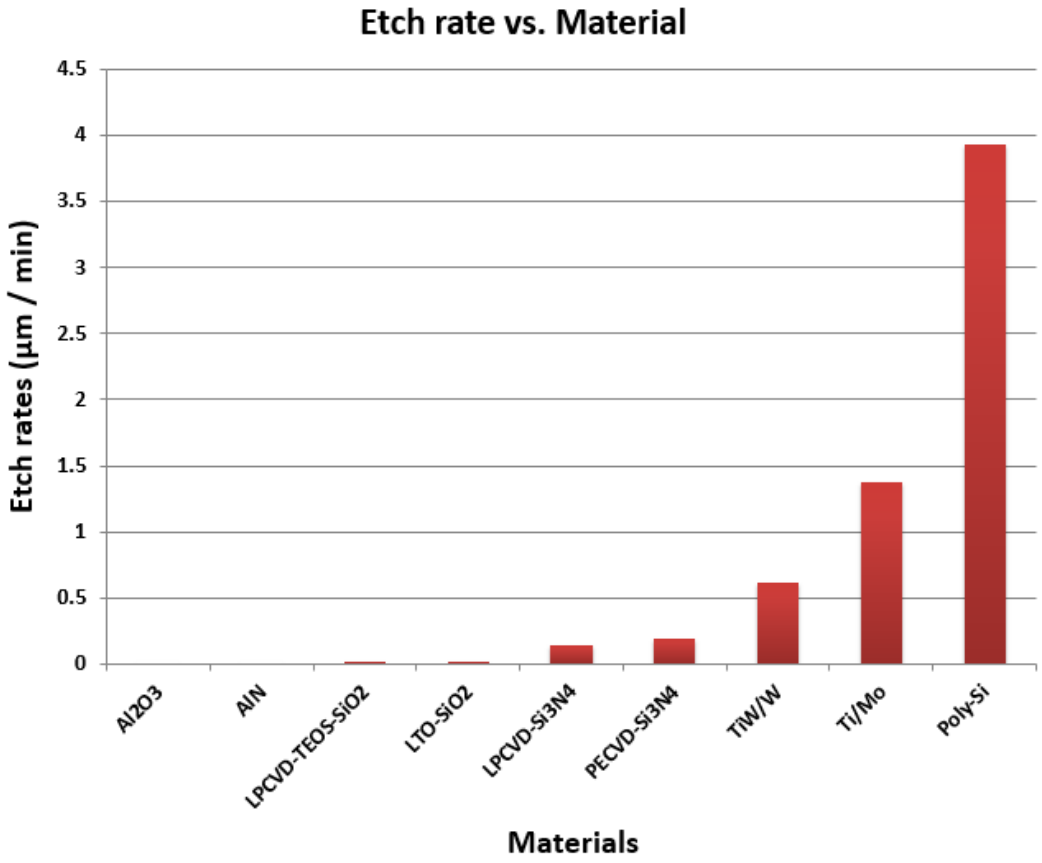


Figure 16. Etch rates for each material. The etch rates presented in this figure are the values which are scaled to etch rate (µm / min) per 1 cm^2. As can be seen from the figure poly-Si has the fastest etch rate. On the other end the etch rate for Al_2O_3 and AlN is zero.

*Table 9. The scaled and rounded vertical etch rates as µm / min. Symbol * after vertical etch rate indicates that the value is an average of the 9.8 cm^2 and 39.2 cm^2 values.*

Vertical etch rates scaled to 1 cm^2 [µm / min]	
Al_2O_3	0
AlN	0
LPCVD-Si_3N_4	0.14*
LPCVD-TEOS-SiO_2	0.004
LTO-SiO_2	0.02
PECVD-Si_3N_4	0.19
Poly-Si	3.9
Ti/Mo	1.4*
TiW/W	0.61*

4.1.2. Under etching tests

The under etching tests were done in order to obtain information about how XeF_2 releasing works. As described in chapter 3, the results for the under etch tests were obtained via utilizing an optical microscope and the Klayout software. The lateral etch rates were calculated from the overlapping images. An example of the images taken between the etching steps are shown in Figure 17. The length of one etching step was 2.5 minutes. E.g. Image a) from Figure 17 is taken after the first etching step. As seen from the picture there is a clear sign (indicated with the red arrow) that the under etching is progressing. Alternatively, image b) from Figure 17 is taken after the second etching step. Again the under etching has progressed well.

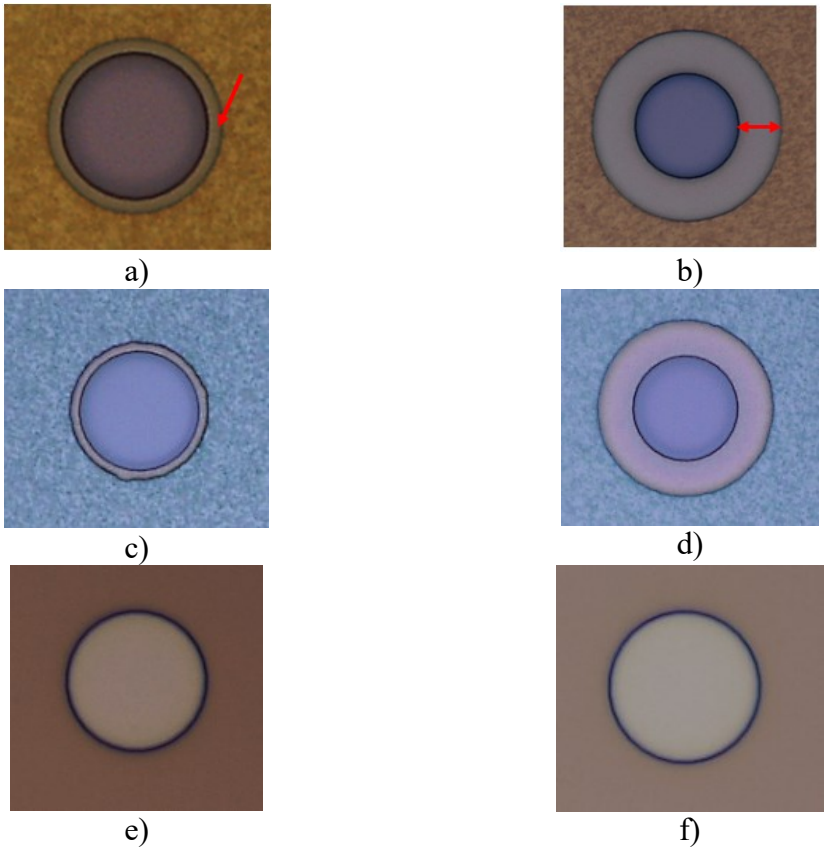


Figure 17. Images taken between etching steps with an optical microscope. The red arrows indicate the progress of under etching. E.g. the difference between images a) and b) is in tens of micrometers. a)-b) Images of the poly-Si sample with resist as a mask. c)-d) Pictures of the poly-Si sample with SiO_2 hard mask. e)-f) Images of the W sample with resist as a mask. The under etching progress can be observed from pictures a)-d). In images e)-f) there appears to be no under etching whatsoever. The difference between the images is approximately 2.5 minutes.

The total exposed etching area was 3.5 cm^2. The exposed etching area is shown in Figure 18. Poly-Si with resist masking had the fastest lateral etch rate: 4.9 µm /min. The lateral etch rate for poly-Si with SiO_2 hard mask was 3.8 µm /min. The difference between these two can be explained with the fact that XeF_2 does not react with resist but does react with SiO_2. Thus this reaction may slow down the etch rate. The total etch time for both poly-Si samples was 10 minutes. The total etch time for the TiW/W was 13 minutes. During the tests TiW/W did not etch at all. The obtained results indicate that XeF_2 is a suitable option for the etching sacrificial poly-Si layers with both resist and SiO_2 hard mask. XeF_2 did not etch the sacrificial TiW/W layer. However, a vertical etch rate 0.61 µm / min was obtained with TiW/W thus structures that have TiW/W layers should considered passivation when utilizing XeF_2 etching. The results obtained from the under etch tests are presented in Table 10.

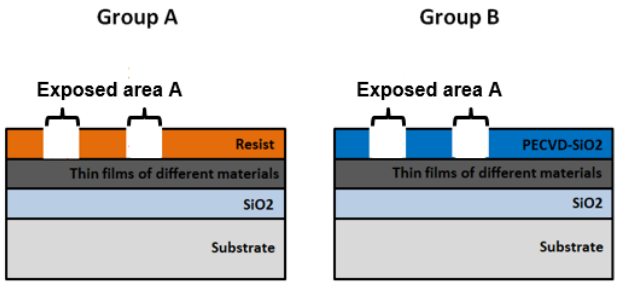


Figure 18. Depiction of the exposed etching areas. The exposed etching area is determined by calculating the total area of all etch openings.

Table 10. Results obtained in the under etching study. Lateral etch rates for W and poly-Si with resists and SiO_2 hardmask. The fastest etch rate was obtained with poly-Si/resist. The difference between the poly-Si/resist and poly-Si/SiO_2 can be explained with the fact that XeF_2 gas does not attack resist and reacts with SiO_2. The total etch time for these two was 10 min and 13 min for W. During the study W did not etch at all. The total exposed etching area was 3.5 cm^2.

Material	Lateral etch rate (µm /min)
Poly-Si	4.9
Poly-Si/SiO2	3.8
TiW/W	0.0

4.1.3. Simplified device etching tests

Since the results obtained from the previous etching tests were promising it was expected that the etching process would work well also with the simplified device. The samples were etched with a pulsed flow mode utilizing the "de10x30x10-3.0p0.0n high conductivity" recipe. As described in the methods chapter 3.2.2., this recipe requires the following parameters number of cycles, etch time, chill time, XeF_2, N_2 and chill pressures. Only the amount of cycles was varied in this test. The other parameters remained constant throughout the study. Etch time was 30 seconds, chill time was 15 seconds, XeF_2 pressure was 3 Torr, N_2 pressure was 10 Torr and chill pressure was 3 Torr, as shown in Table 11. The test indicated that a total of 15 minutes of etching was required in order to release all the components on the wafer. The average etch rate for the sacrificial poly-Si layer was between 14 and 19µm per minute. The total exposed etching area was 1.5 cm^2. The releasing sequence of a single smaller structure is shown in Figure 19. All inspected structures were successfully released, which indicates that it is possible to obtain high yield with XeF_2 etching and thus these results prove in general the high potential of XeF_2 etching in sacrificial processes.

Table 11. Parameters used in the simplified device etch tests. The samples were etched with a pulsed flow mode utilizing the "de10x30x10-3.0p0.0n high conductivity" recipe, which requires the following parameters: number of cycles, etch time, chill time, XeF_2, N_2 and chill pressures. Only the amount of cycles was varied in this test.

Parameter	Value
Number of cycles	2-10
Etch time	30 s
Chill time	15 s
XeF_2 pressure	3 Torr
N_2 pressure	10 Torr
Chill pressure	3 Torr

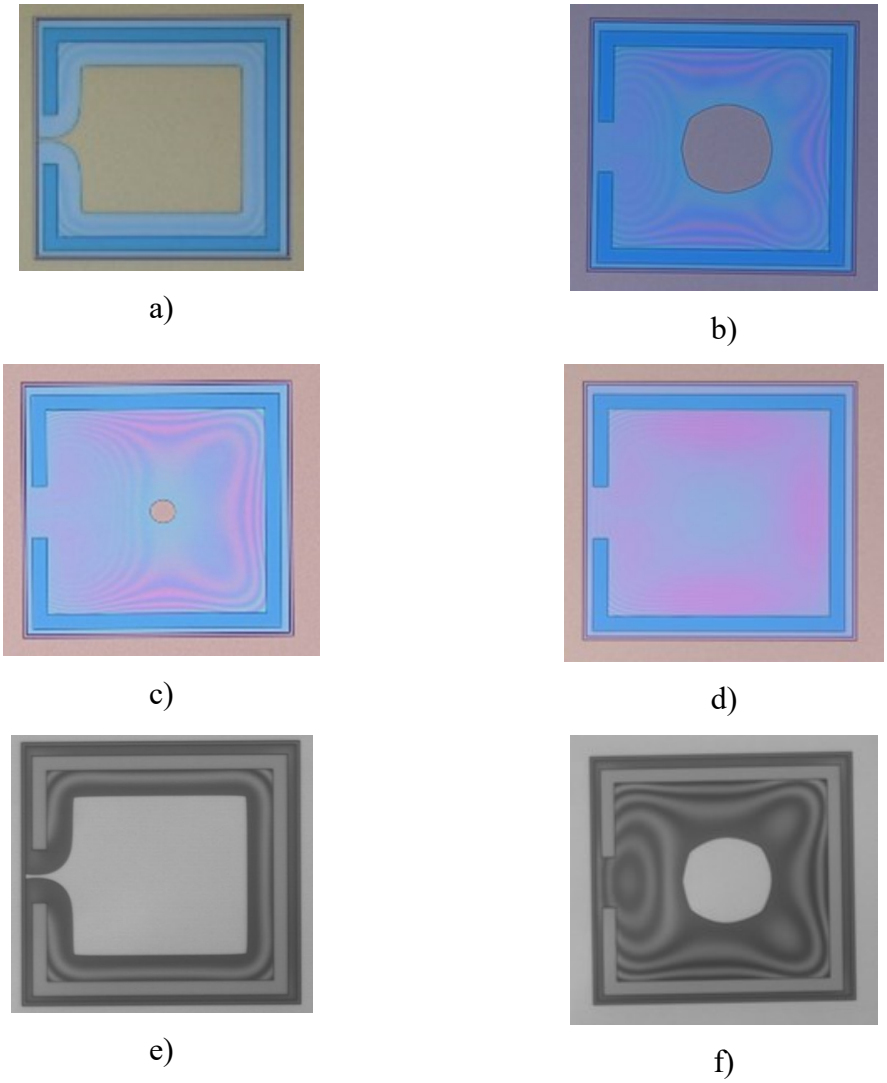


Figure 19. A collection of images taken during the simplified device release tests. Images a)-f) show an etching process of a simple rectangle self-supporting structure. The pictures are taken between the etching steps. Images a)-d) were taken with an regular optical microscope. Images e) and f) were taken with IR optical microscope in order to determine an approximation for the lateral etch rate.

The simple rectangle self-supporting structures, shown in Figure 19, were the first components that were fully released. This was expected since the volume of the Si to be etched was much smaller. The various rectangle structures etched quite similarly. The biggest difference that was noticed occured between components that had discrete circles as etch openings and components that had long trenches as etch openings. From these two the ones with discrete circles as etching windows etched

faster. By far the slowest etching was observed with the test component that had no etch openings in the middle of the structure. Images of these structures are shown in Figure 20.

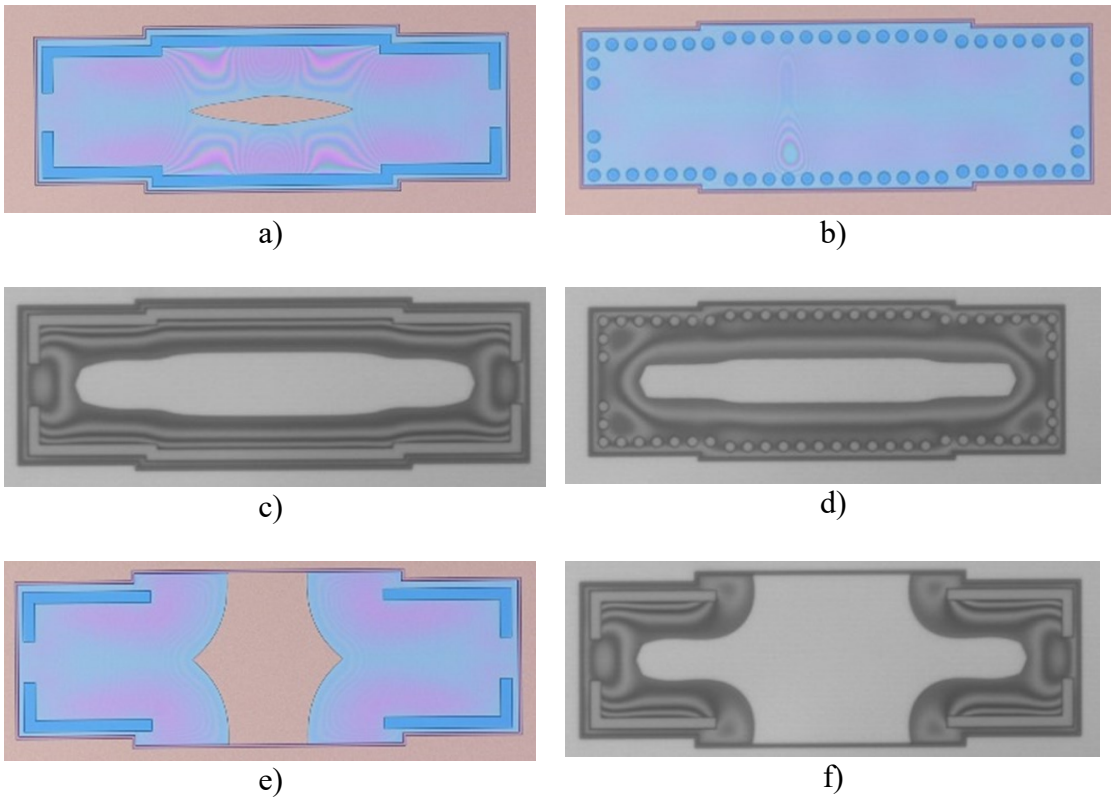
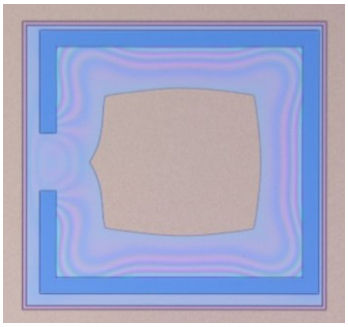


Figure 20. Images of different components from the simplified device structure etching tests. From images a)-d) it is possible to see that the component that had circles as etching windows was released faster than the similar component with rectangles as etching windows. Test structure, shown in images e) and f), had the slowest etching as was anticipated.

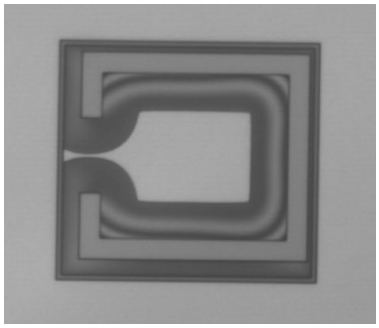
After performing the first XeF_2 etching step for the device structures it was clear that the etching process did not start as was expected. It could be observed that only few components on the wafer reacted with XeF_2. These few observed reactions indicated that the etching windows were not fully open. This was confirmed with an optical microscope that showed only few source points where XeF_2 could get into contact with the sacrificial poly-Si layer. Thus the etching only occurred in few fronts. The problem was caused either by resist residue or poor adjustment of the TEOS SiO_2 etching parameters. Due to this it was necessary to add an HF wet etch step to the fabrication process of the test samples. First, the samples were dipped into 1:50 HF

solvent for 30 seconds. After this, the samples were rinsed with water and dried with a spin rinse drier. This step can be avoided in future processes by adjusting the parameters of the TEOS SiO_2 etching steps or by making sure all of the resist is carefully removed and that there is no residue left. After the additional HF step, it was possible to continue the XeF_2 etching normally.

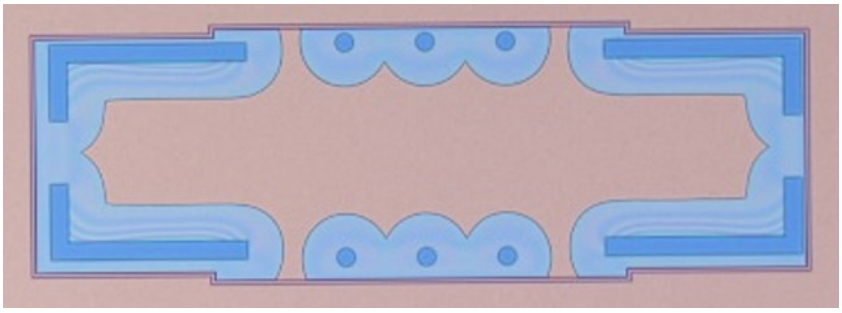
Three test wafers were properly aligned between the different layers but the remaining two were misaligned, as shown in Figure 21. The distance between the lateral etch stop and the etch opening should be 10 µm at all locations as was decided in the designing phase. The misalignment was most probably caused by an alignment error during the lithography step with the wafer stepper, especially because the lithography was done to all the wafers at the same run. One reason for the problem could be the distance between different alignment marks. An example alignment mark is shown in Figure 22. For some reason in some cases the wafer stepper may interpret the edges of the alignment marks as a new mark. However, the cause for the misalignment problem was not confirmed. For future utilization of the used reticles the wafer stepper job in general, parameters etc. should be checked carefully.



a)



b)



c)

Figure 21. Images of the samples with misaligned layers. The distance between the lateral etch stop and etching window should be 10 µm in all locations, which is not the case as can be seen from the pictures. However, this had no significant effect on the etch tests. Images a) and b) were taken from the simple rectangle self-supporting structures. Image c) was taken from a simplified decvice structure.

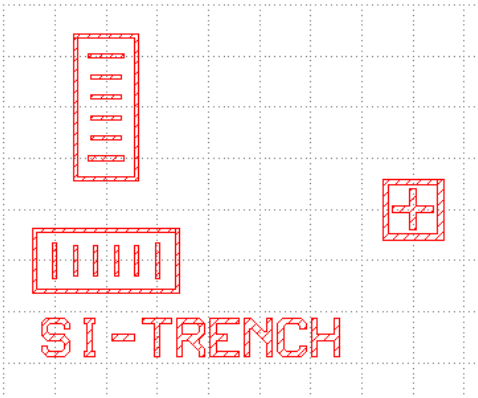


Figure 22. An image of an alignment mark required for the wafer stepper. The machine aligns the different layers horizontally and vertically via these marks. If the alignment marks are too close to each other the stepper might not find the other mark at all. Other problem could be that the stepper interprets the inner lines wrong and mixes them with the outer lines that form the "fence" that surrounds the actual alignment lines.

4.2. Comparison to manufacturer's selectivity data and new findings

The manufacturer of the XeF_2 etcher has provided typical selectivities for various materials. With the data obtained in this thesis it was possible to compare the obtained results with the ones given by the manufacturer by calculating approximations for the selectivities. A comparison between the data is shown in Table 12. From the reactive materials the selectivities for LPCVD-TEOS-SiO_2 poly-Si, Ti/Mo and TiW/W fit best with what previous studies had reported. Materials LTO-SiO_2, LPCVD-Si_3N_4 and PECVD-Si_3N_4 had significant differences in comparison to the selectivities provided by the manufacturer. Already during the experimental part it was noticed that especially Si_3N_4 samples etched faster than was originally anticipated. It was the most surprising result that was obtained in this study. According to previous studies, Si_3N_4 has been stated to have as good selectivity as SiO_2 [10]. The results presented in this thesis indicate that throughout the tests Si_3N_4 had far worse selectivity than SiO_2. The average etch rate for LPCVD-Si_3N_4 was nearly six times faster than LTO-SiO_2 etch rate and nearly 35 times faster than LPCVD-TEOS-SiO_2 etch rate. A far bigger difference was calculated between PECVD Si_3N_4 / LTO-SiO_2 and PECVD Si_3N_4 / LPCVD-TEOS-SiO_2. The average etch rate for PECVD-Si_3N_4 was eight times faster than LTO-SiO_2 etch rate and 49 times faster than LPCVD-TEOS-SiO_2 etch rate.

It has been previously reported that the selectivity of Si_3N_4 shows a substantial correlation with the temperature of the substrate [10]. Lower temperature diminishes the attack while higher temperature increases it. Additionally, it has been studied that the attack on Si_3N_4 correlates heavily to the presence of etch byproducts. It has also been reported that there seems to be no attack on blanket Si_3N_4 films [10]. Previous results indicate that the actual attack on Si_3N_4 does not come from XeF_2 directly but from the byproducts that are created in the reaction between Si and XeF_2. In addition, as the formulation becomes more silicon rich, the attack on Si_3N_4 films increases [10]. Some studies imply that etch recipes that utilize N_2 in the process seem to have worse selectivity. The reason behind this is considered to be the potential moisture impurities in the N_2 [10], [49]. These findings are rather recent and were

unfortunately noticed only after the tests were already made. Thus, unfortunately, the Si_3N_4 etch tests in this thesis were mostly done with recipes that included N_2 in the XeF_2 etch process. Originally this was thought to improve selectivity since during the experimental part even with continuous flow recipe the etch rate seemed to be fast. Another reason behind these results could be that the quality of the Si_3N_4 thin films was bad. At least some of the LPCVD-Si_3N_4 samples were previously used as monitoring wafers. This could affect the results since the depositions were not done just before the etch tests.

The etch rate for LTO-SiO_2 was also surprisingly high. The deposition was done with the so-called "sparse loading", which leads to uniform thickness across the wafers. However, the wafers for these tests were loaded in dummy wafer locations, which could affect the quality of the thin film thus resulting in higher etch rate. It has also been previously studied that the attack on oxides is partly caused by the presence of HF in the etching chamber, which is formed due to the combination of moisture and XeF_2 [10].

Table 12. Comparison between the selectivities presented in literature and the approximations for the selectivities calculated from the obtained results. The ratio is stated with the value of Si on the left and the value of the material on the right, e.g. ratio 1000:1 would mean that if 1000 microns of Si is removed then 1 micron of the material in question is removed. Parts of this table are adapted from [10].

Material	**Highest reported selectivity**	**Lowest reported selectivity**	**Selectivity from measurements**
Al_2O_3	Non-reactive	Non-reactive	Non-reactive
AlN	Non-reactive	Non-reactive	Non-reactive
LPCVD-Si_3N_4	∞:1	90:1	30:1
LPCVD-TEOS-SiO_2	∞:1	700:1	1000:1
LTO-SiO_2	∞:1	700:1	200:1
PECVD-Si_3N_4	∞:1	90:1	25:1
Poly-Si	1:1	1:1	1:1
Ti/Mo	2:1	2:1	3:1
TiW/W	Very low	6:1	6:1

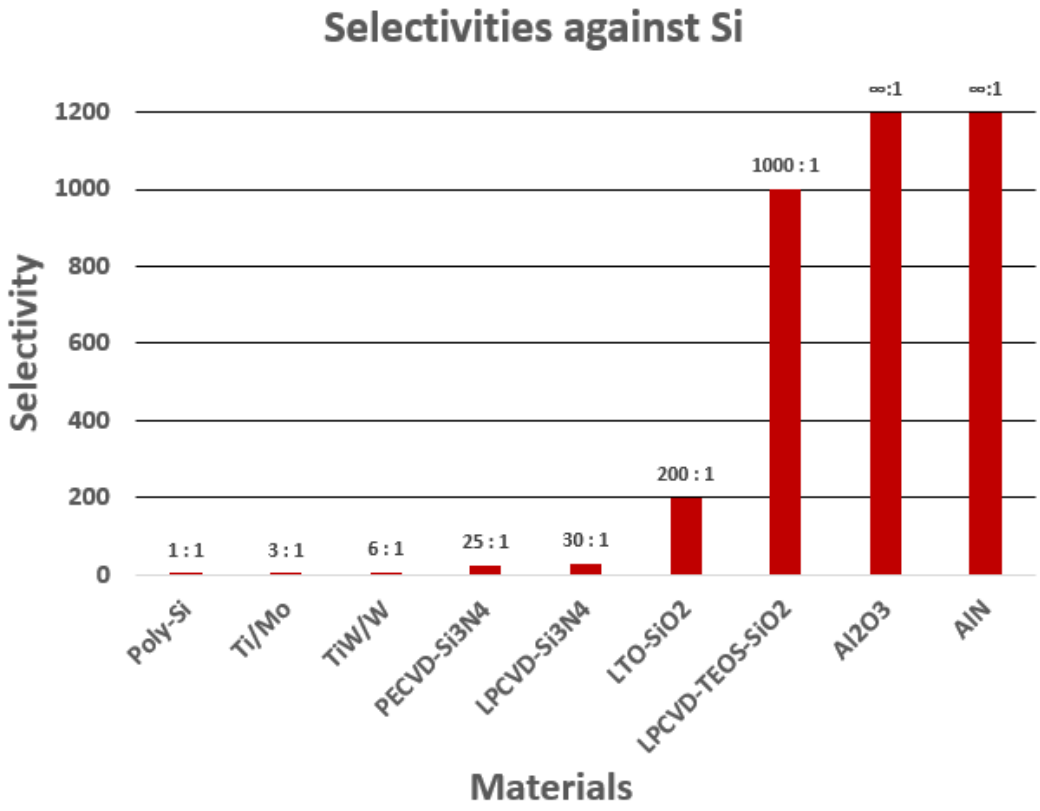


Figure 23. Selectivities against Si. Al_2O_3 and AlN had infinite selectivity. LPCVD-TEOS-SiO2 had 1000:1, LTO-SiO_2 had 200:1, LPCVD-Si_3N_4 had 30:1, PECVD-Si_3N_4 had 25:1 TiW/W had 6:1, Ti/Mo had 3:1 and poly-Si had 1:1.

4.3. Future interests

As demonstrated in this thesis, XeF_2 etching can be used successfully in the release step of simplified device structures. Thus the next logical goal would be the implementation of the XeF_2 etching step into the fabrication process of MEMS, piezoMEMS and microacoustic device structures. However, e.g. typically microacoustic device designs may also contain materials that are sensitive or react with XeF_2 including Mo and W. Thus, before implementation, some necessary changes should be done to the design. For example, the sensitive layers could be protected via passivation. In this thesis, the materials that have proven to work as passivation layers are AlN, Al_2O_3 and SiO_2. From these Al_2O_3 grown with ALD could be a good solution even with difficult structures due to its high uniformity and conformality. In addition, since Al_2O_3 did not react at all with XeF_2, only a thin layer would be required for the fabrication of a functioning etch stop. This can be easily realized by ALD due to extremely precise thickness control it provides. Especially acoustic and microacoustic device structures with reflector stack design, with the addition of a cavity, consisting of alternating layers of high acoustic impedance material and low acoustic impedance material, such as Mo and W, are extremely sensitive for deformations in the edges of the thin film stack. A thin protective Al_2O_3 could do the trick and enable the use of XeF_2 etching [50]–[52]. Therefore, the lateral etch stop structure created in this thesis, which was fabricated for the simplified microacoustic structures, could be utilized in various processes.

Alternatively, the tests indicate that XeF_2 etching suits perfectly with fabrication processes that require some kind of releasing step with Si, Mo or poly-Si as a sacrificial layer. As stated earlier, XeF_2 has been successfully used in the fabrication of various cantilevers, resonators, anchors, microtransducers, actuators, etc. As previous studies and now this thesis have shown, the strengths of XeF_2 etching are in sacrificial processes. In addition, since it is a complementary technology to HF vapor-phase etching its status as a dry vapor-phased Si etchant remains unchallenged.

5. Conclusions

One of the key steps in surface micromachining is the removal of sacrificial layers. These layers are etched away in order to release the mechanical elements in MEMS structures. For this release etching, vapor-phase dry techniques have shown their superiority over corresponding wet techniques. Due to the ability of being able to completely avoid stiction related problems, vapor-phase dry etching has been of great interest to the MEMS community. Without stiction related problems, higher and higher manufacturing yields can be achieved. Currently, the two mainstream vapor-phase technologies that are widely used in both academia and industry are HF and XeF_2 based etchs. Being complementary methods to each other, together they form the perfect combination. HF is suitable for sacrificial oxide layers and does not attack e.g. Si whereas XeF_2 is suitable for e.g. sacrificial poly-Si layers and does not attack oxides. This thesis concentrated on the XeF_2 vapor-phase dry etching technique.

The goal of this thesis was to characterize the XeF_2 etch process. This was done by performing various etch tests with different materials. The first step in the characterization process was to measure vertical etch rates for AlN, Al_2O_3, Ti/Mo, poly-Si, Si_3N_4, SiO_2 and TiW/W. AlN and Al_2O_3 did not react with XeF_2, thus both materials can be used as passivation layers, which was expected. Poly-Si and Ti/Mo had the fastest vertical etch rates, as was assumed ($ER_{p\text{-}Si}$ = 3.9 µm / min and $ER_{Ti/Mo}$ = 1.4 µm / min). Both were highly reactive with XeF_2 and, thus can be used successfully as sacrificial layers. The vertical etch rates for LPCVD-TEOS-SiO_2 (ER = 0.004 µm / min) and LTO-SiO_2 (ER = 0.02 µm / min) were low, which indicates that both are low attack materials. Both SiO_2 films can also be used as masking materials. LPCVD-Si_3N_4 and PECVD-Si_3N_4 can be defined as low attack materials. However, the vertical etch rates (ER_{LPCVD} = 0.14 µm / min and ER_{PECVD} = 0.19 µm / min) were surprisingly high since previous studies indicate that the selectivity of Si_3N_4 against Si should be almost as good as the selectivity of SiO_2. This could be caused by the use of recipes that included N_2 in the process. Previous studies imply that recipes that utilize N_2 in the process seem to have poorer selectivity. The reason

behind this is considered to be the potential moisture impurities in the N_2. Lastly, the vertical etch rate for TiW/W was 0.61 µm / min. However, the lateral etch rate for TiW/W was 0 µm / min. The tests indicated that it is a conditionally reactive material. Thus if it is used in structures that are etched with XeF_2, it should be protected.

In addition to the vertical etch rate measurements, the lateral etch rate achieved with XeF_2 was characterized. Samples that were tested were poly-Si with resist mask, poly-Si with SiO_2 hard mask and TiW/W with resist mask. Poly-Si with resist mask had the fastest lateral etch rate: 4.9 µm /min. The etch rate for poly-Si with SiO_2 hard mask was 3.8 µm /min. The difference between these two can be explained with the fact that XeF_2 does not react with resist but does react with SiO_2 slowing down the etch rate. In any case, the achieved lateral etch rates prove that successful etching of polysilicon sacrificial layers can be obtained with XeF_2 etching and with the used masking materials. In the case of TiW/W no under etching was observed at all, thus indicating that TiW/W would not be a good sacrificial layer when etching with XeF_2.

The final experiment done for this thesis was the etching of the simplified device structure, which consisted of multiple TEOS SiO2 layers and a sacrificial poly-Si layer. The aim was to verify the release process and to obtain an approximation for the lateral etch rate of poly-Si. After the initial problems with etch openings, caused by the errors in previous processing steps, the test was in the end successfully completed. A 150 mm wafer, containing 32 chips with 5824 components, was fully released after 15 minutes of XeF_2 etching with pulsed flow mode. This demonstrated the suitability of XeF_2 etching on a device level. The obtained approximation for the lateral etch rate was between 14 to 19 µm per minute. The total exposed etching area was 1.5 cm^2 and the maximum distance between the etch openings was approximately 240 µm. The difference between these lateral etch rates and the ones obtained from the under etching tests can be explained with the difference in the exposed etching area.

The results presented in this thesis clearly demonstrate the vast potential of XeF_2 etching in microfabrication. The next logical step would be to implement a XeF_2 etching step into a new or an existing device fabrication process. Nevertheless, the

results presented here provide already valuable help in determining the suitable process and etching parameters. As an example, XeF_2 etching could be utilized in the manufacturing of microacoustic filters. Additionally, any kind of process that requires a releasing step is a potential target for the implementation of XeF_2 etching, as long as the sacrificial materials are reactive with XeF_2. Hopefully, the results provided in this thesis will accelerate the use and popularity of XeF_2 etching in MEMS processing even further.

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A Recipes and tools

Table 13. Materials, deposition tools and recipes used in the etch rate tests.

Material	Deposition tool	Recipe
AlN	Sputtering system VA	SCALNV2
Al_2O_3	ALD reactor SUNALE R-150B	AO-R300 50cyc
Ti/Mo	Sputtering system VA	timo_1w.tec
poly-Si	Centrotherm diffusion furnace B3 poly	B80AMO 1000
Si_3N_4	PECVD Oxford Plasmapro system 100 Centrotherm LPCVD Diffusion furnace B4 nitride	PRO-SiN-2-300 3, High quality SLNit7LS
SiO_2	Centrotherm LPCVD Diffusion furnace B1 LTO Centrotherm LPCVD Diffusion furnace B2 TEOS	LTO_V 69 SLTEOS_v 113
TiW/W	Sputtering system VA	W_6in 1.2.tec

Table 14. A chart of the lithography process. The process consisted of four steps. Each step, equipment, recipe and process parameter are listed in the table.

Step	Equipment	Recipe	Process parameters
Priming	A10 primer oven YES	Standard	HDMS 150 °C 20 min
Resist coating	A09 resist track AIO coat	Coat25spr, pump1=1	SPR700, 2500RPM, 1.5 µm, Top EBR off, SB Contact 90C 60 s
Exposure	A02 Mask aligner SUSS MA150	6"prox	Exposure time 13 s, Intensity 26 mW/cm^2
Developing	A09 resist track AIO develop	bake_only1 develop_only1	AZ726 MIF, RT, 60 s

Table 15. List of the devices and recipes used in the plasma etching step.

Device	Recipe
Oxide etcher LAM 4520	550 (etch rate approx. 500 nm/min)
Polysilicon etcher LAM 4420	405 (etch rate approx. 350 nm/min)
Diffusion furnace A4 Annealing	n2ann_vv 800 30