W/D-Bands Single-Chip Systems in a 0.13μm SiGe BiCMOS Technology – Dicke Radiometer, and Frequency Extension Module for VNAs

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Abstract

Recent advances in silicon-based process technologies have enabled to build low-cost and fully-integrated single-chip millimeter-wave systems with a competitive, sometimes even better, performance with respect to III-V counterparts. As a result of these developments and the increasing demand for the applications in the millimeter-wave frequency range, there is a growing research interest in the field of the design and implementation of the millimeter-wave systems in the recent years. In this thesis, we present two single-chip D-band front-end receivers for passive imaging systems and a single-chip W-band frequency extension module for VNAs, which are implemented in IHP's 0.13μm SiGe BiCMOS technology, SG13G2, featuring HBTs with f_t/f_{max} of 300GHz/500GHz.

First, the designs, implementations, and measurement results of the sub-blocks of the radiometers, which are SPDT switch, low-noise amplifier (LNA), and power detector, are presented. Then, the implementation and experimental test results of the total power and Dicke radiometers are demonstrated. The total power radiometer has a noise equivalent temperature difference (NETD) of 0.11K, assuming an external calibration technique. In addition, the dependence of the NETD of the total power radiometer upon the gain-fluctuation is demonstrated. The NETD of the total power radiometer is 1.3K assuming a gain-fluctuation of %0.1. The front-end receiver of the total power radiometer occupies an area of 1.3 mm^2. The Dicke radiometer achieves an NETD of 0.13K, for a Dicke switching of 10 kHz, and its total chip area is about 1.7 mm^2. The quiescent power consumptions of the total power and Dicke radiometers are 28.5 mW and 33.8 mW, respectively. The implemented radiometers show the lowest NETD in the literature and the Dicke switching concept is employed for the first time beyond 100 GHz.

Second, we present the design methodologies, implemantation methods, and results of the sub-blocks of the frequency extension module, such as down-conversion mixer, frequency quadrupler, buffer amplifier, Wilkinson power divider, and dual-directional coupler. Later, the implemantation, characterization and experimental test results of the single-chip frequency extension module are demonstrated. The frequency extension module has a dynamic range of about 110 dB, for an IF resolution bandwidth of 10 Hz, with an output power which varies between -4.25 dBm and -0.3 dBm over the W-band. It has an input referred 1-dB compression point of about 1.9 dBm. The directivity of the frequency extension module is better than 10 dB along the entire W-band, and its maximum value is approximately 23 dB at around 75.5 GHz. Finally, the measured s-parameters of a W-band horn-antenna, which are performed by either the designed frequency extension module and a commercial one, are compared. This study is the first demonstration of a single-chip frequency extension module in a silicon-based semiconductor technology.

0.13µm SiGe BiCMOS W/D-Band Tek-Çip Sistemler – Dicke Radyometresi, ve VNA'lar için Frekans Genişletici Modül

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Özet

Silikon bazlı proses teknolojilerindeki son gelişmeler, düşük maliyetli ve tamamen entegre tek çipli milimetre-dalga sistemlerinin, III-V muadillerine göre rekabetçi, bazen daha da iyi bir performansa sahip olmasını sağlamıştır. Bu gelişmeler ve milimetrik dalga frekansı alanındaki uygulamalara olan artan talebin bir sonucu olarak, son yıllarda milimetre-dalga sistemlerinin tasarımı ve uygulanması alanında giderek artan bir araştırma ilgisi bulunmaktadır. Bu tez çalışmasında, IHP'nin 0.13µm SiGe BiCMOS teknolojisinde gerçeklenen, tekli çipli D-bant ön uç alıcıları (toplam güç ve Dicke radyometre) ve VNA'lar için tek çipli W-bant frekans uzatma modülü sunulmaktadır.

İlk olarak, SPDT anahtarı, düşük gürültü kuvvetlendirici (LNA) ve güç dedektörü olan radyometrelerin alt bloklarının tasarımları, uygulamaları ve ölçüm sonuçları sunulmaktadır. Daha sonra, toplam güç ve Dicke radyometrelerinin gerçeklenmesi ve deneysel test sonuçları gösterilmiştir. Toplam güç radyometresi, harici bir mekanik anahtarlama olduğu varsayılarak 0.07K'lık bir gürültü eşdeğer sıcaklık farkına (NETD) sahiptir. Ek olarak, toplam güç radyometrisinin NETD'nin kazanım-dalgalanması üzerindeki bağımlılığı gösterilmektedir. Toplam güç radyometresinin NETD'si,% 0.1'lik bir kazanç dalgalanması varsayılarak 1.3K olarak bulunmuştur. Toplam güç radyometresinin ön uç alıcısı 1.3 mm^2'lik bir alanı kaplar. Dicke radyometresi, 10 kHz'lik bir Dicke anahtarlaması için 0.13K'lık bir NETD elde eder ve toplam yonga alanı yaklaşık 1.7 mm^2'dir. Toplam gücün ve Dicke radyometrelerinin sukunet halinde güç tüketimi sırasıyla 28.5 mW ve 33.8 mW'dir. Gerçeklenen radyometreler literatürdeki en düşük NETD performansını gösterir ve Dicke anahtarlama kavramı 100 GHz'nin ötesinde ilk kez kullanılmıştır.

İkincisi, aşağı-dönüşüm karıştırıcısı, frekans dörtleyici, tampon kuvvetlendirici, Wilkinson güç bölücü ve çift yönlü kuplör gibi frekans genişletme modülünün alt-bloklarının tasarım metodolojilerini, gerçeklenme yöntemlerini ve elde edilen sonuçları sunulmaktadır. Daha sonra, tek çipli frekans uzatma modülünün implemantasyon, karakterizasyon ve deneysel test sonuçları gösterilmiştir. Frekans uzatma modülü, 10 Hz'lik bir IF çözünürlük bant genişliği için yaklaşık 110 dB'lik bir dinamik aralığa sahiptir ve W-bandı üzerinde -4.25 dBm ve -0.3 dBm arasında değişen bir çıkış gücü vardır. Girişe tanımlı 1 dB sıkıştırma noktası yaklaşık 1.9 dBm'dir. Frekans genişletme modülünün yönelimi tüm W-bandı boyunca 10 dB'den daha iyidir ve maksimum değeri yaklaşık 75.5 GHz'de yaklaşık 23 dB'dir. Son olarak, tasarlanan frekans uzatma modülü ve ticari bir tanesi tarafından gerçekleştirilen bir W-band horn-anteninin ölçülen s-parametreleri karşılaştırılır ve tek-çipli frekans uzatma modülünün çalışması bu şekilde doğrulanır. Bu çalışma, bir silikon tabanlı yarı iletken teknolojisinde uygulanan tek-çip frekans uzatma modülünün ilk gösterimidir.

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List of Abbreviations

AM	Amplitude Modulation
BEOL	Back-end-of-line
BJT	Bipolar Junction Transistor
BV_{CEO}	collector-emitter Breakdown Voltage
CB	Common-base
CE	Common-emitter
CMOS	Complementary Metal-Oxide-Semiconductor
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HPBW	Half Power Beam Width
IF	Intermediate Frequency
ISS	Impedance Standard Substrate
LNA	Low-noise amplifier
MIM	Metal-insulator-metal
NEP	Noise Equivalent Power
NETD	Noise Equivalent Temperature Difference
PLL	Phase-locked-loop
RF	Radio-frequency
SiGe	Silicon-germanium
SNA	Scalar Network Analyzer
SPDT	Single-pole Double-throw
SRF	Self-resonance frequency
SoC	System-on-a-chip
SOL	Short-open-load
SOLT	Short-open-load-through
TRL	Through-reflect-line
WLAN	Wireless Local Area Network
VNA	Vector Network Analyzer

1. Introduction

1.1. Millimeter-wave Monolithic Integrated Circuits

In these days, there is a steadily increasing interest in the millimeter-wave spectrum that refers to the frequency range of 30 GHz to 300 GHz, thanks to the recent advances in silicon-based semiconductor technologies [1]. The millimeter-wave frequency band has significant features that make it convenient and attractive for many applications such as multi-Gb/s wireless communications [2], automotive RADARs [3], passive imaging systems [4], and sensors [5]. Operating in the millimeter-wave spectrum promises larger bandwidth, smaller size, and better resolution than the microwave frequencies (300 MHz – 30 GHz). However, the millimeter-wave systems suffer from having limited range due to the very high free-space path-losses.

Figure 1 shows the low-atmospheric attenuation windows in the millimeter-wave spectrum (35, 77, 94, 140, 220 GHz), and the atmospheric attenuation levels for various weather conditions. The widest window after 60 GHz is between 75 and 110 GHz, and this frequency band is known as W-band. This broad low-atmospheric attenuation window makes W-band suitable for many different applications, including either short-range and long-range automotive RADARs [6], passive imaging systems [7], and point-to-point wireless links [8]. Another low-atmospheric attenuation window which is around the center of the D-band (110-170 GHz) makes this frequency band applicative for several applications, in particular, radiometers [9], high-speed wireless communications [10], and radar sensors [11].

The integration capability of SiGe heterojunction bipolar transistor (HBT) technology with complementary metal-oxide-semiconductor (CMOS) process has enabled to build the RF front-end and baseband circuits together on a single-chip, and this concept is named as system-on-a-chip (SoC). In the recent literature, there are several studies that present fully-integrated millimeter-wave systems. For instance, Figure 2 shows the millimeter-wave SoCs: a 120 GHz SiGe BiCMOS distance sensor [13] and a 143-152 GHz radar transceiver with built-in calibration [14].

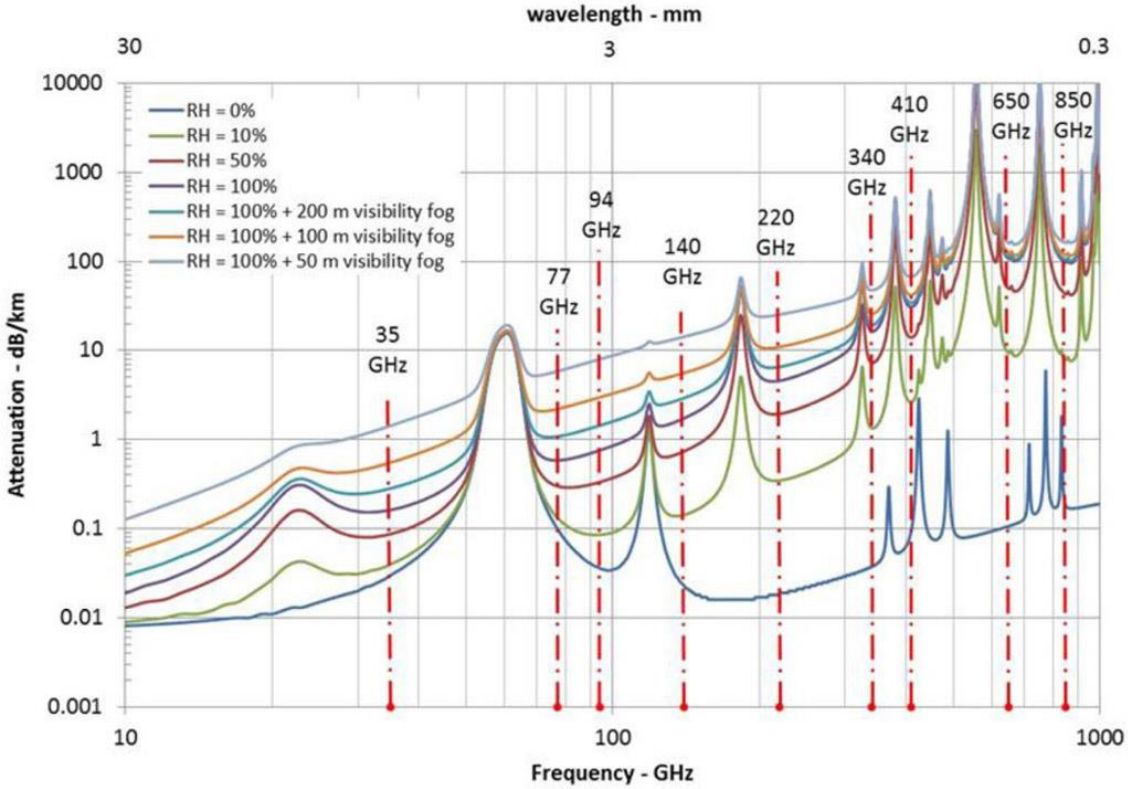

Figure 1 Amount of atmospheric attenuation for various relative humidity (RH) values [12].

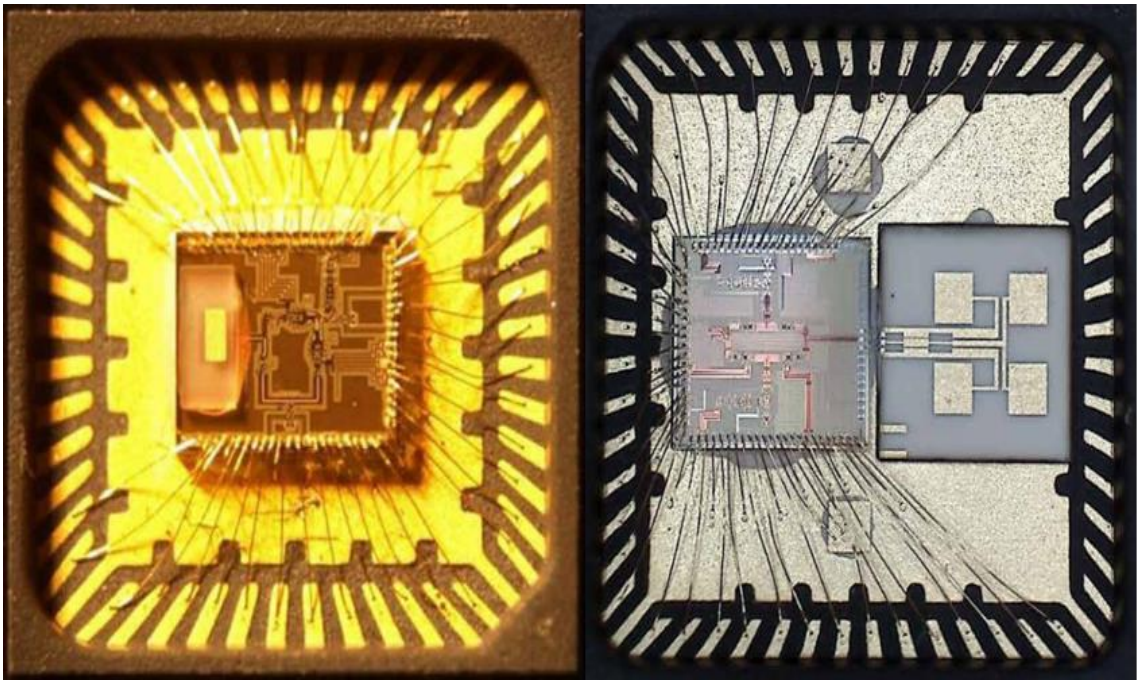

Figure 2 Single-chip millimeter-wave systems: (left) 120 GHz distance sensor [13] (right) 143-152 GHz radar transceiver with built-in calibration [14].

One of the primary applications in the millimeter-wave spectrum is the imaging of the observing targets. Detection and processing of electromagnetic waves make the observation of an object or a scene possible and allow to build imaging systems in this way. The microwave or millimeter-wave imaging systems can be grouped into two main categories, active imaging systems (RADARs) and passive imaging systems (radiometers). Active imaging systems are capable of acquiring information on the distance, speed, and direction of the target [15].

An active imaging system radiates electromagnetic signals generated by the signal source of itself and measuring either the reflected and scattered electromagnetic waves from the scene. Therefore, they require the signal sources and transmitter channels in addition to receiver parts, and that would result in high implementing and operating costs.

On the other hand, the passive imaging systems' operating principle relies on detection and processing of already existing electromagnetic waves. According to Max Planck's black-body radiation law [16], all objects spontaneously and continuously radiates electromagnetic waves proportional to their physical temperature. In addition to black-body radiation, the targeted object might reflect electromagnetic waves arising due to other electromagnetic sources in the background of the targeted object. The power of the emitted and reflected electromagnetic waves is contingent upon the physical temperature and the emissivity constant of the object. These dependencies, especially the relationship between the power of the emitted electromagnetic waves and the physical temperature, can be processed to create an image of the targeted object and scene [17]. Although the passive imaging systems do not require to transmit electromagnetic waves to the targeted object or scene, they need a high-gain and low-noise receivers to detect the weak levels of the emitted electromagnetic waves by the objects.

The millimeter-wave imaging systems are mainly used to detect the threat materials such as concealed weapons and explosives. Although the active imaging systems promise higher scan speed and operation independent of the ambient temperature, the detection of hidden objects is much more difficult than with the passive imaging systems [18]. Because the specular reflections might occur due to the structures of the fabric surfaces of the clothes and this would reduce the quality of the images. For this reason, passive imaging methods, including radiometers and infrared detectors, based on black-body radiation are preferred instead of active illumination techniques [19]. The operating

frequencies of the infrared detectors extend from few tens of THz to the edge of the visible spectrum (430 THz). Such high-frequency signals can only pass through thin clothes, so the infrared detectors are not capable to thoroughly detect the hidden threats [20]. Figure 3 shows the passive millimeter-wave and infrared images of a concealed weapon. As can be seen from the figure, the passive millimeter-wave systems (radiometers) are better than the infrared detectors in the detection of the hidden objects [21].

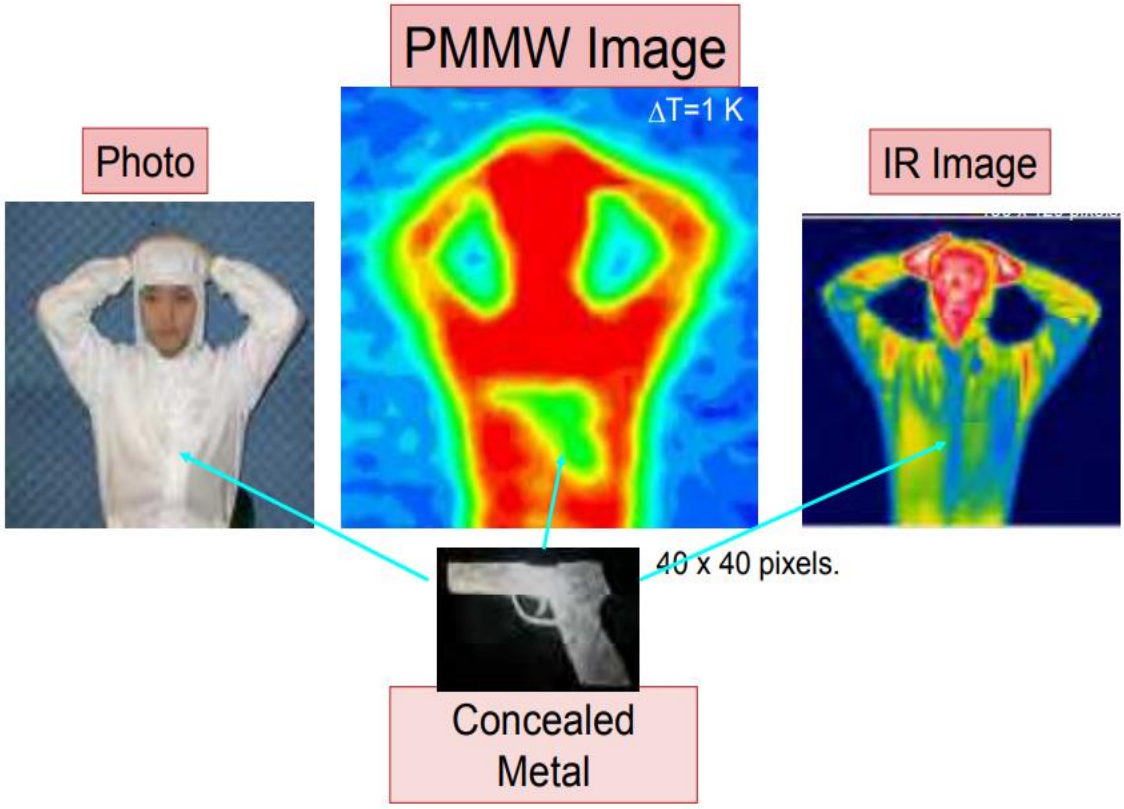

Figure 3 Passive millimeter-wave (PMMW) and infrared (IF) images of a concealed weapon [21].

1.2. Characterizations of Millimeter-wave Monolithic Integrated Circuits

Scattering parameters (or S-parameters) are very useful in the characterization of the small-signal behaviors of the RF, microwave and millimeter-wave electronic circuits. The network analyzers are widely used to measure the s-parameters of the active and passive circuits. The network analyzers can be grouped under two main titles: scalar network analyzer (SNA) and vector network analyzer (VNA). Although SNAs can measure only the amplitude properties of the signals, VNAs are capable of also measuring the phase relationships between the incident, reflected and transmitted signals in addition to their

amplitude qualities. For this reason, VNAs are preferred to characterize the small-signal properties of electronic networks fully.

Three market leaders are operating in the field of VNA manufacturing: Anritsu, Keysight, and Rohde&Schwarz. The base units of the present state-of-the-art VNAs on the market operate from hundreds of Hz up to 70 GHz without using any frequency extension module (Anritsu MS4640B VectorStar [22], Keysight N5247B PNA-X [23], Rohde&Schwarz ZVA67 [24]). Figure 4 shows the Keysight N5247B PNA-X Microwave Network Analyzer which is operating across the frequency range of 900 Hz to 67 GHz. However, they can be configured with frequency extension modules for measurements beyond 70 GHz. The frequency range of a VNA is determined primarily by the lower and upper-frequency edges of its reflectometer parts. The increasing demand for millimeter-wave systems has led to significant research efforts in the domain of low-cost and high-performance millimeter-wave reflectometers. Ulker and Weikle presented a W-band six-port reflectometer based on the sampled-transmission line implemented by the WR-10 rectangular waveguide and configurated with three GaAs Schottky diodes to reduce the complexity of the frequency extension modules [26]. After that, Roberts and Noujeim demonstrated a tethered E-band (60-90 GHz) GaAs reflectometer based on the nonlinear-transmission-line (NLTL) technology to build frequency extension modules in smaller sizes [27]. Finally, a W-band single-chip reflectometer implemented in SiGe BiCMOS technology was successfully presented [28]. Also, a fully-integrated VNA that can operate from 50 GHz to 100 GHz was implemented in SiGe BiCMOS technology [29]. Despite these efforts to extend the frequency ranges and reduce the sizes of the reflectometers, the technical trend is to employ the frequency extender modules, which consists of reflectometers and frequency multiplication chains, to expand the frequency range of the VNAs, as discussed in detail in Section 3.1. Figure 5 shows the Anritsu MS4640B VectorStar VNA whose the operating frequency is extended to 145 GHz by the frequency extension modules which have 0.8mm coaxial outputs. The waveguide-based frequency extension modules have to be employed beyond 145 GHz since there are no coaxial standards. Wohlgemuth *et al.* proposed an inventive solution to the frequency limitations and expensive and cumbersome structures of the waveguide-based frequency extension modules, and they successfully demonstrated an active probe that consists of a GaAs single-chip frequency extension module for on-wafer s-parameter measurements [30].

Figure 4 Keysight N5247B PNA-X Microwave Network Analyzer, 900 Hz to 67 GHz [23].

Figure 5 Anritsu VectorStar ME7838A Millimeter-Wave System, 70 kHz to 125 GHz [25].

1.3. SiGe BiCMOS Technology

Recent developments and ongoing advances in SiGe BiCMOS technologies have made it possible to produce low cost, fully integrated single-chip millimeter-wave systems with a competitive, sometimes even better, performance compared to III-V counterparts. In addition to its superior high-frequency performance, the integration capability of the RF front-end and baseband circuits on a single-chip makes the SiGe HBT BiCMOS technology more convenient and cost-effective solution for millimeter-wave SoCs than the III-V counterparts. Table 1 summarizes the respective performances of various semiconductor technologies for RF integrated circuits.

Ge has a smaller bandgap of 0.66 eV than that of Si (1.12 eV). This technology uses bandgap engineering to form the base region of the transistor. By this way, the base of the transistor is formed by the SiGe compound, resulting in higher electron injection and thus higher current gain (β). Moreover, the minority carriers are accelerated across the base region thanks to the speeded diffusive transport of minority carriers, and this results in the reduced base transit time (τ_b) [31]. In addition, the parasitic capacitances and resistances are reduced by the help of the smaller structure which is vertically and laterally scaled. There are mainly two figures of merit to evaluate the high-frequency performances of the semiconductor technologies: the unity current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}). The unity current gain of a transistor is typically found by the small-signal current gain for the short-circuited output, and f_T is the frequency at where the current gain is equal to unity. The f_T of a BJT can be found using equation (1), where τ_b is the base transit time, τ_c is the collector transit time, gm is the transconductance of the transistor, C_π and C_μ are parasitic capacitances, and r_e and r_c are parasitic resistances. The other important performance metric of a transistor, f_{MAX} which is the frequency where the power gain is equal to one, is given by equation (2). As can be seen from the equations, the f_T and f_{MAX} can be improved using the SiGe compound's advantages which are mentioned above.

$$f_T = \frac{1}{2\pi}\left(\tau_b + \tau_c + \frac{1}{gm}(C_\pi + C_\mu) + (r_e + r_c)C_\mu\right)^{-1} \quad (1)$$

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}} \quad (2)$$

In this thesis study, the IHP's 0.13µm SiGe BiCMOS technology, SG13G2, featuring HBTs with $f_t/f_{max}/BV_{CEO}$ of 300GHz/500GHz/1.6V [32]. The all-aluminum BEOL comprise five thin metallization layers (M1-M5) and two thick layers (TM2-TM1) for high-quality on-chip inductor and transmission line designs. The BEOL also offers MIM capacitors and three types of polysilicon resistors. The detailed cross-section of the IHP's SiGe BiCMOS process (SG13G2) is depicted in Figure 6.

Table 1 Respective performance summaries of Various Semiconductor Technologies for Radio Frequency Integrated Circuits [31].

(Excellent: ↑↑; Very Good: ↑; Good: 0; Fair: ↓; Poor: ↓↓)

Performance Metric	SiGe HBT	SiGe BJT	Si CMOS	III-V MESFET	III-V HBT	III-V HEMT
Frequency Response	↑	0	0	↑	↑↑	↑↑
1/f and Phase Noise	↑↑	↑	↓	↓↓	0	↓↓
Broadband Noise	↑	0	0	↑	↑	↑↑
Linearity	↑	↑	↑	↑↑	↑	↑↑
Output Conductance	↑↑	↑	↓	↓	↑↑	↓
Transconductance /area	↑↑	↑↑	↓↓	↓	↑↑	↓
Power Dissipation	↑↑	↑	↓	↓	↑	0
CMOS Integration	↑↑	↑↑	N/A	↓↓	↓↓	↓↓
IC Cost	0	0	↑	↓	↓	↓↓

1.4. Motivation

As mentioned in the previous sections, opportunities in the millimeter-wave spectrum and the latest developments in SiGe BiCMOS technology have led to significant research efforts and increased interest in low-cost and single-chip millimeter-wave systems.

One of the objectives of this thesis is to design and implement a fully-integrated D-band front-end receiver based on Dicke radiometer architecture for passive imaging systems. The temperature resolution of a Dicke radiometer is mainly determined by the performances of its sub-blocks which are power detector, LNA, and SPDT switch. In order to develop a state-of-the-art Dicke radiometer, the trade-offs and bottlenecks that limit the performances of the sub-blocks will be analyzed and

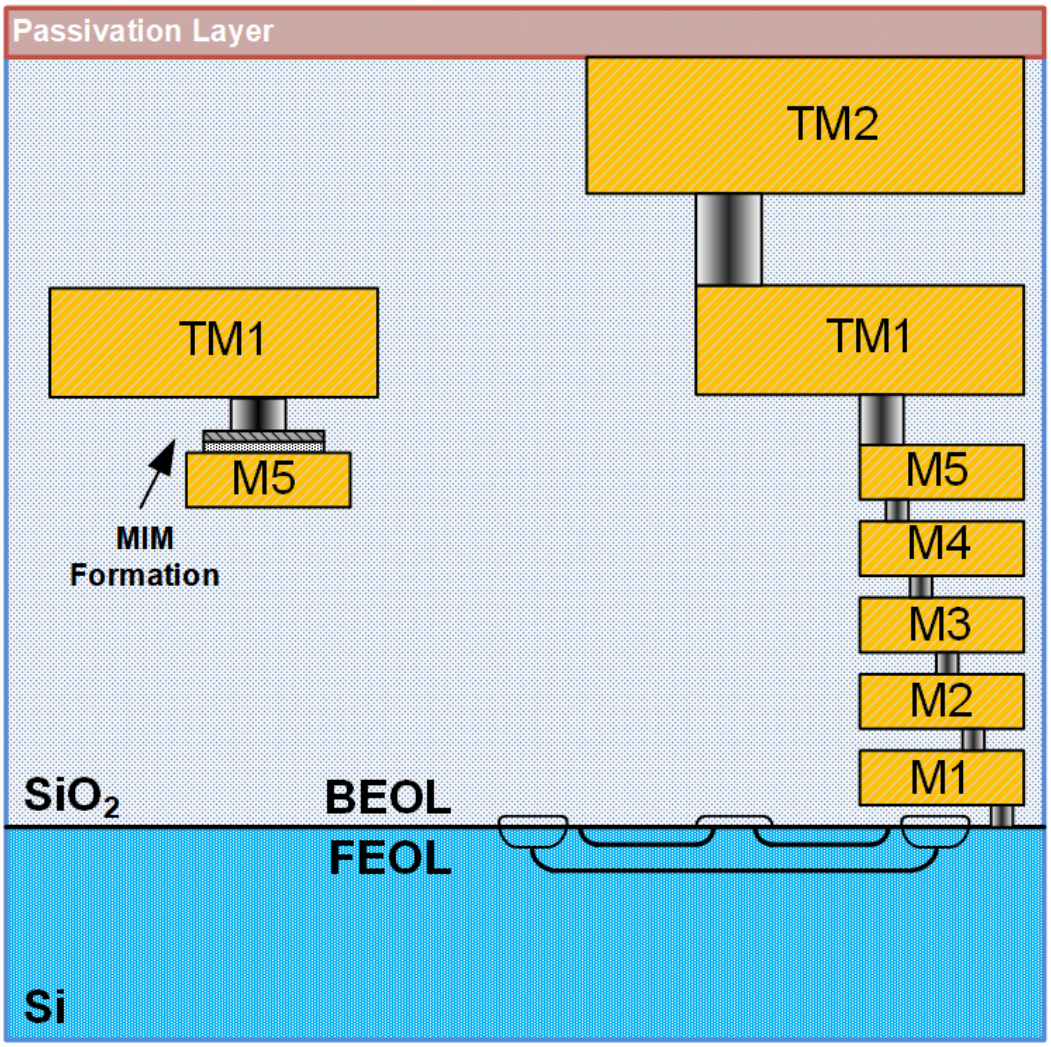

Figure 6 A detailed cross-section of the IHP's 0.13µm SiGe BiCMOS process, SG13G2.

investigated. And beyond that, new approaches and existing solutions will be utilized to find the optimum design points for the trade-offs and to break the bottlenecks.

Another aim of this work is to present the design, implementation, and characterization of a single-chip W-band frequency extension module for VNAs to make the characterizations of the millimeter-wave integrated circuits easier and less costly. Within this scope, the required sub-blocks that are capable of performing the operations of the frequency extension modules will be designed, and they will be implemented on a single-chip to build a fully-integrated W-band frequency extension module.

1.5. Organization

This thesis consists of four chapters that are organized as follows.

Chapter 2 begins with the basics of passive imaging systems, including theoretical calculations and radiometer architectures. Then, design approaches, implementations and

simulation and measurement results of the sub-blocks such as power detector, LNA, and SPDT switch are presented. Finally, the implementation of the total power and Dicke radiometers, the measurement results of these implemented radiometers, and the comparison with similar studies are shown.

Chapter 3 begins with the basics of the s-parameter measurements using frequency extension modules. Then, design approaches, implementations and simulation and measurement results of the frequency extension modules' sub-blocks such as the down-converter mixer, frequency quadrupler, amplifier, Wilkinson power divider and dual directional coupler are presented. Finally, the implementation of the single-chip frequency extension module for vector network analyzers and the comparison of the measurement results with a commercial frequency extension module are presented.

Chapter 4 concludes the thesis with the summary of work and some additional discussions on the suggested solutions to solve existing problems and provides information on possible future studies to improve the work.

2. D-Band Total Power and Dicke Radiometers

This section begins with the fundamental operating principles and the basic receiver architectures, also their theoretical sensitivity calculations, of the passive imaging systems. Then, the designs, implementations, and measurement results of the sub-blocks of the passive imaging systems are presented. Also, the comparisons of each sub-block with the previously reported studies are summarized. After that, the experimental results of the implemented radiometers are demonstrated. Finally, the comparison of the implemented radiometers with the studies in the literature are presented.

2.1. Fundamentals of Passive Imaging Systems

2.1.1 Detection Principles

Essentially, radiometers (or passive imaging systems) can be considered as high-sensitive receivers that are used to detect the electromagnetic radiation emitted by the objects which have a physical temperature. According to Max Planck's black-body radiation law [16], all objects spontaneously and continuously emit electromagnetic waves proportional to their physical temperature. The spectral brightness of a black body is described by Planck's black-body radiation law, as presented in equation (3), where B_f is the black-body spectral brightness (W$\cdot m^{-2} \cdot sr^{-1} \cdot Hz^{-1}$), f is the frequency (Hz), h is Planck's constant of $6.63 \times 10^{-34}\, J \cdot s$, k is Boltzmann's constant of $1.38 \times 10^{-23}\, J/K$, T is the physical temperature (K), and c is the speed of light of $3 \times 10^{8}\, m/s$. Figure 7 shows the spectral radiation of objects at different physical temperatures.

$$B_f = \frac{2hf^3}{c^2} \times \left(\frac{1}{e^{\frac{hf}{kt}} - 1} \right) \tag{3}$$

In the millimeter-wave frequency domain (30 – 300 GHz) and below, Planck's black-body radiation equation can be approximated to equation (4), which is also known as Rayleigh-Jeans's approximation, using Taylor polynomial expansion ($hf/kT \ll 1$). As can be seen from equation (4), the Rayleigh-Jeans' approximation points a linear relationship between the spectral brightness and the physical temperature. This linear relationship is valid with a less than 3% error for the frequencies below 300 GHz. Thence, it is very useful to use the Rayleigh-Jeans's approximation to analyze the amount of the electromagnetic power emitted by an object, and to calculate the amount of the power collected by the antenna in a passive imaging system. Figure 8 shows the comparison of

the Planck's black-body radiation law and the Rayleigh-Jeans's approximation. As also can be seen from the figure, the discrepancy between the Planck's black-body radiation law and the Rayleigh-Jean's approximation is decreasing with the increase of the frequency, as expected.

$$B_f = \frac{2f^2kT}{c^2} \tag{4}$$

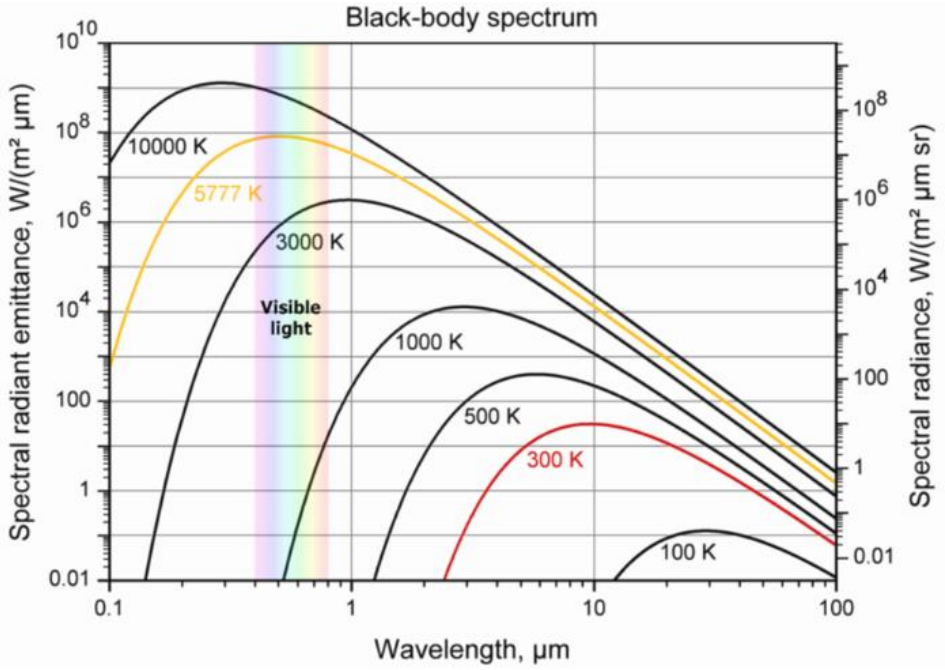

Figure 7 Spectral radiation of objects at different physical temperatures [33].

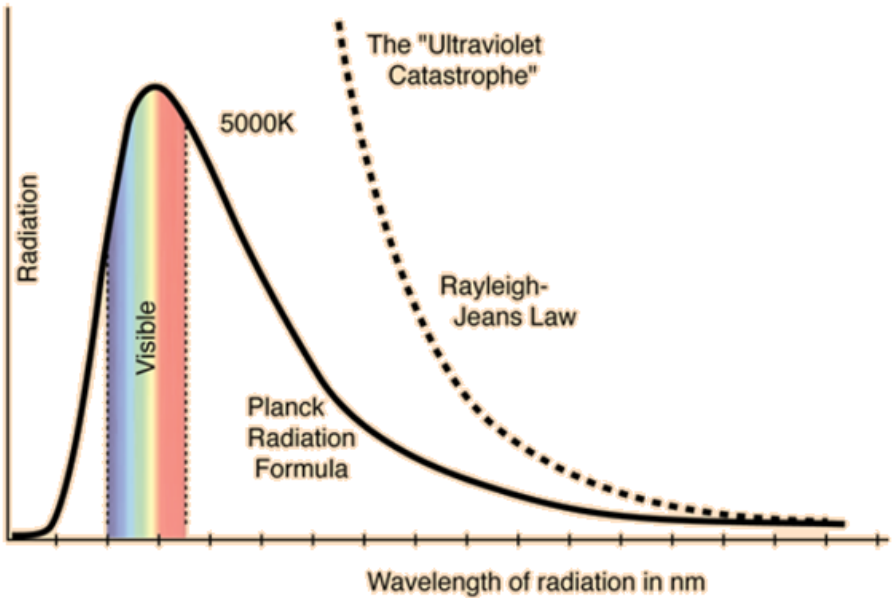

Figure 8 Comparison of the Planck's black-body radiation law and the Rayleigh-Jeans' approximation [34].

Figure 9 demonstrates a basic detection operation of a passive imaging receiver. The front-end circuit of the passive imaging receiver is fed by an antenna which has a radiation pattern symbolized by $A(\theta, \phi)$. The total area of the observation scene is determined by the half power beam width (HPBW) of the antenna. The power of the electromagnetic radiation picked up by the antenna is proportional to the sum of the electromagnetic radiation emitted by the scene (T_B), and the reflected electromagnetic radiation from the scene (T_{SC}) which arises due to the hot objects at the background. The electromagnetic signal picked up by the antenna is amplified by a high-gain LNA, and then converted to DC-voltage information by a power detector. The DC-signal generated by the front-end circuit of the passive imaging system can be transferred to the digital domain by an ADC to create an image of the observation scene, after the baseband process.

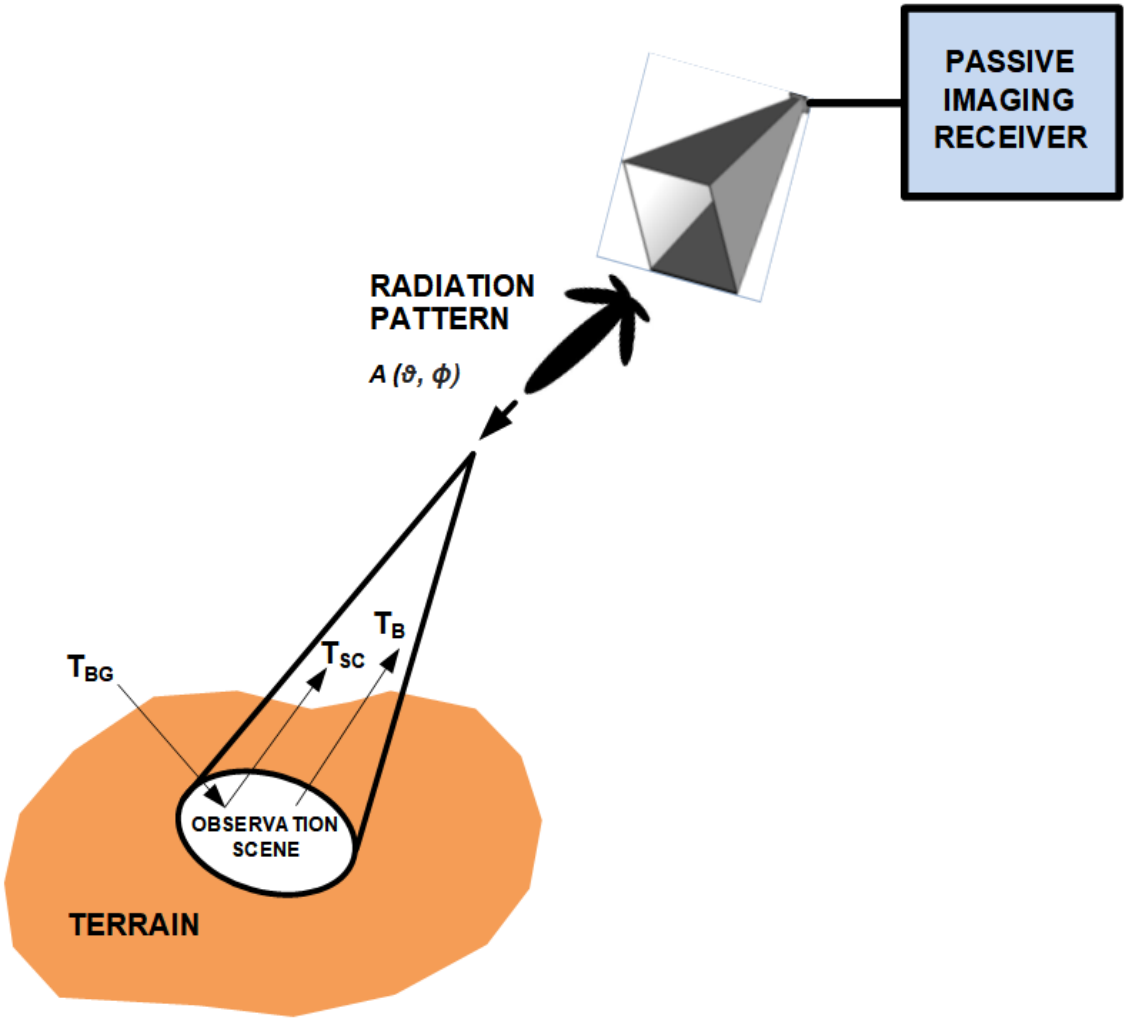

Figure 9 Demonstration of the basic detection operation of a radiometer.

The procedure described in [35] was followed to calculate the amount of the power picked up by the antenna. Assuming that the brightness is same across the hemisphere and the incident radiation is same over the surface and ignoring the free space path loss between the target scene and the antenna, the received power (P_{rec}) can be expressed by equation (5) where B_f is the black-body spectral brightness, f is the frequency, A_e is the effective area of the antenna, $A(\theta, \phi)$ is the radiation pattern of the antenna [35].

$$P_{rec} = \frac{1}{2} A_e \int_f \iint_\Omega B_f A(\theta, \phi) d\Omega df \tag{5}$$

The brightness temperature (T_B) is equal to the multiplication of the physical temperature (T) of the object by its emissivity (e) which is the measure of the radiating capability of an object compared to a black-body ($T_B = eT$). The emissivity values (e) of the common objects are briefly presented in Table 2. In addition to the brightness temperature (T_B), the other source that should be taken into account is the electromagnetic radiation (T_{SC}), which is reflected by the target object, of the other hot objects at the background. This electromagnetic radiation is equal to the multiplication of the physical temperature of the hot objects at the background, which is named as illuminator after now, by the reflectivity (p) of the target object ($T_{SC} = eT_{illuminator}$). The reflectivity value of an object is equal to $1 - e$. As a result, the total brightness temperature (T_{total}) of the target object is equal to the sum of these two temperatures, and it can be expressed by equation (6).

$$T_{total} = T_B + T_{SC} = eT + pT_{illuminator} \tag{6}$$

Table 2 The effective emissivity values of various materials [35].

	Effective Emissivity		
Surface	**44 GHz**	**94 GHz**	**140 GHz**
Bare metal	0.01	0.04	0.06
Painted metal	0.03	0.10	0.12
Painted metal under carvas	0.18	0.24	0.30
Painted metal under camouflage	0.22	0.39	0.46
Dry gravel	0.88	0.92	0.96
Dry asphalt	0.89	0.91	0.94
Dry concrete	0.86	0.91	0.95
Smooth Water	0.47	0.59	0.66
Rough or hard-packed dirt	1.00	1.00	1.00

Assuming a bandwidth of 40 GHz at 140 GHz center frequency, an effective emissivity of 0.5, a 1 mm^2 effective antenna area with an isotropic pattern, a target scene temperature of 290K, and 5 cm distance between the target and the antenna, the amount of the power picked up by the antenna is calculated to be $1.2825 \times 10^{-15}\, W$, which equals to approximately -119 dBm. Even if a horn antenna with a gain of 23 dBi is used, the input power of the receiver would be no more than -95 dBm. For this reason, a specially designed receiver with low noise and high gain is required to amplify the signal picked up by the antenna.

2.1.2 Radiometer Architectures and Theoretical Sensitivity Calculations

Total power radiometer and Dicke radiometer topologies are two most common architectures that used in millimeter-wave passive imaging systems. These two radiometer topologies can be implemented in either two different types of the receiver architectures: direct detection architecture and superheterodyne architecture. In the direct detection receiver architecture, which is shown in Figure 10 and Figure 11 for total power radiometer and Dicke radiometer topologies, respectively, the detection of the power of the signal is performed at the RF frequencies without performing any down-conversion operation. On the contrary, in the superheterodyne receiver architecture, which is shown in Figure 12 and Figure 13 for total power radiometer and Dicke radiometer topologies, respectively, the detection of the power of the signal is performed at the IF frequencies after the down-conversion operation. Although the total power radiometer and Dicke radiometer topologies are very similar to each other, there is a significant difference that is emerged because of the single-pole-double-throw (SPDT) switch which is placed between the antenna and the LNA.

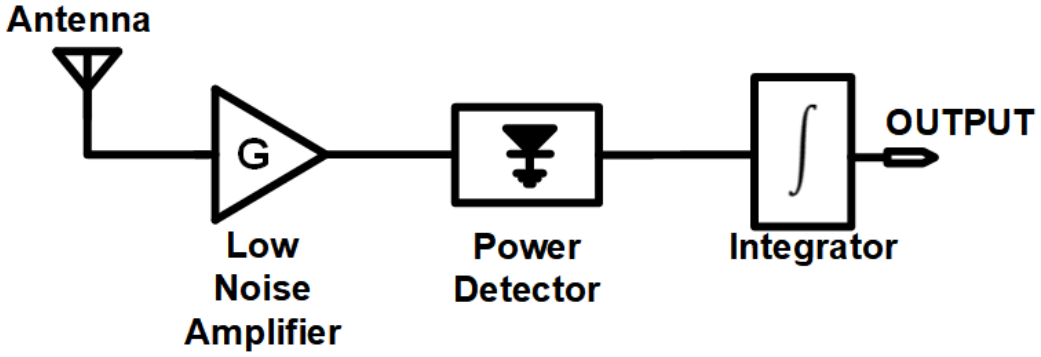

Figure 10 Block schematic of a total power radiometer configured as a direct detection receiver.

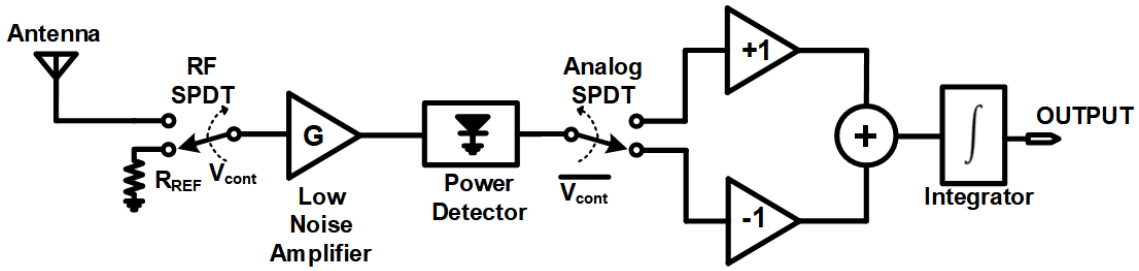

Figure 11 Block schematic of a Dicke radiometer configured as a direct detection receiver.

As shown in Figure 12 and Figure 13 a superheterodyne receiver architecture down-converts the RF signal to an IF. Before the down-conversion, the signal is amplified by an LNA since the amplitude of the signal picked up by the antenna is very low. The down-converted signal is then amplified again by an IF amplifier. The amplification of an IF signal is much easier and useful than the RF frequencies since the performances of the active devices, such as noise, power linearity, and gain, are much better in the lower frequencies. However, adding a mixer and a local oscillator (LO) increases the power consumption, the chip area, and the level of the complexity. In addition to these drawbacks, the superheterodyne receiver architecture suffers from an unstable operation problem due to the local oscillator's dependence on the temperature. The output power and the frequency of the LO signal are varying with the temperature, and it would result in an error of the detection of the power level picked up by the antenna. These stability issues could be solved by thermal control circuits and phase-locked-loop (PLL) techniques, but the power consumption, the chip area, and the complexity level would surge.

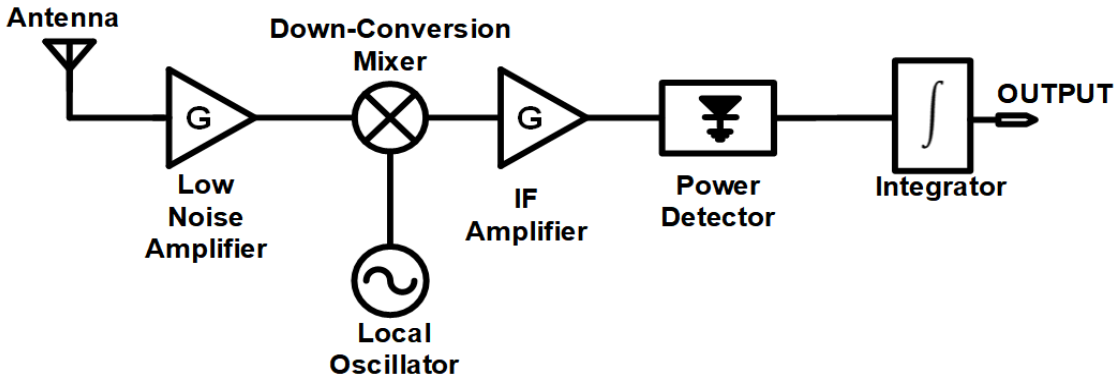

Figure 12 Block schematic of a total power radiometer configured as a superheterodyne receiver.

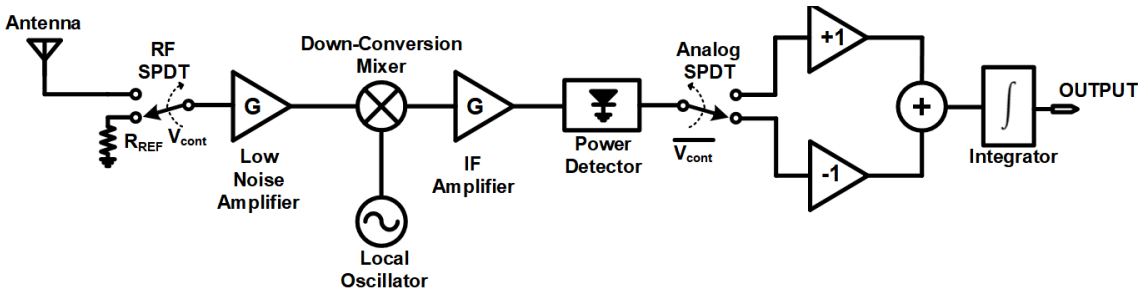

Figure 13 Block schematic of a Dicke radiometer configured as a superheterodyne receiver.

On the contrary to the superheterodyne receiver architecture, the direct detection receiver architecture does not include a mixer and local oscillator so that it does not require the associated circuitries such as temperature control circuits and PLL networks. Thence, the power consumption, the chip area and the level of the complexity are significantly reduced. In the direct detection of radiometer architecture, the power detector operates at the directly RF frequencies instead of IF frequencies. Therefore, the signal should be very amplified before the power detector, and so that the main challenge here is to design a high-gain LNA. Furthermore, the direct detection radiometer architectures promise wider bandwidth than the superheterodyne radiometer architectures since the available bandwidth is not limited by the down-conversion operation and the IF amplifier. Thus, they promise better temperature resolution than the superheterodyne radiometers.

With this comparison in mind, the direct detection receiver architecture was found to be very useful compared to the superheterodyne receiver architecture for the passive imaging systems. Therefore, it was decided to build total power radiometer and Dicke radiometer systems in the direct detection receiver configuration.

2.1.2.1 Total Power Radiometer

Figure 10 shows the detailed block diagram of the direct-detection total power radiometer architecture. An LNA amplifies the signal picked by the antenna since the amplitude of the received signal is very low, around -100 dBm as analyzed in Section 2.1.1. After that, a power detector, which is operating in the square-law region, produces an output voltage proportional to the power of the signal. Using an integrator, this DC output signal is averaged over the entire period (τ), which is called the back-end integration time, to minimize the impact of the system noise on the signal as much as possible. The integrated

output signal can be converted to digital form using an ADC and a data acquisition, and then processed by a computer or a specific digital signal processor (DSP). This radiometer channel can be considered as a single pixel element, and a two-dimensional (2D) images can be created either by implementing a 2D radiometer array, by using a mechanical scanner that enable to scan both in the X- and Y- direction, or by using a hybrid solution of them.

Passive imaging systems are characterized by their noise equivalent temperature difference ($NETD$), also known as radiometric resolution or thermal resolution. Besides, in the literature, there are also a few studies that call it as noise equivalent delta temperature ($NE\Delta T$). The noise equivalent temperature difference, or the thermal resolution, can be defined as the minimum change in the brightness temperature of the target capable of generating a detectable voltage change at the output of the radiometer.

The noise equivalent temperature difference of a total power radiometer can be approximately expressed by equation (7) [36], where T_s is the overall system equivalent noise temperature, B_{RF} is the effective RF noise bandwidth of the radiometer, τ is the back-end integration time, ΔG is the rms gain-fluctuation of the LNA, and G is the gain of the LNA.

$$NETD = T_S \sqrt{\frac{1}{B_{RF}\tau} + \left(\frac{\Delta G}{G}\right)^2} \tag{7}$$

As can be seen from the equation, one of the limiting factors of the thermal resolution is the overall system equivalent noise temperature (T_S), which is equal to the sum of the antenna noise temperature (T_A) and the equivalent noise temperature of the front-end receiver (T_{E-R}). The equivalent noise temperature of the front-end receiver can be calculated using equation (8), where T_{E-LNA} is the equivalent noise temperature of the LNA, and T_{E-PD} is the equivalent noise temperature of the power detector. The equivalent noise temperature of the power detector can be calculated by equation (9) [37]. Herewith, the equivalent noise temperature of the front-end receiver can be reduced by enhancing the gain of the LNA, reducing the noise equivalent power (NEP_{PD}) of the power detector, and enhancing the effective bandwidth of the LNA.

$$T_{E-R} = T_{E-LNA} + \frac{T_{E-PD}}{G} \tag{8}$$

$$T_{E-PD} = \frac{NEP_{PD}}{k\sqrt{B_{RF}}} \tag{9}$$

Similarly, the equivalent noise temperature of the front-end receiver can be directly found by equation (10), using the noise equivalent power (NEP_R) of the overall front-end receiver circuit that consists of the LNA and the power detector.

$$T_{E-R} = \frac{NEP_R}{k\sqrt{B_{RF}}} \tag{10}$$

Another important factor that dictates the thermal resolution is the effective RF noise bandwidth of the radiometer which can be calculated using the gain of the LNA (G_{LNA}) by equation (11) [36]. In addition, the back-end integration time (τ), which is typically 30ms for the passive imaging systems, has a significant effect on the NETD of the radiometer.

$$B_{RF} = \frac{\left[\int_0^\infty G_{LNA}(f)df\right]^2}{\int_0^\infty G_{LNA}^2(f)df} \tag{11}$$

As can be seen from equation (7), the gain fluctuations term might be the dominant term, and so that degrades the noise equivalent temperature difference performance significantly. The gain fluctuations in the system arise because of the 1/f flicker noises of the active devices. Thence, their periods are much smaller than the back-end integration time, and so they cannot be eliminated by the integrator. In order to alleviate these gain fluctuations, periodic calibration techniques based on mechanical scanning can be used [38], and in this case the noise equivalent temperature difference equation (7) of the radiometer is reduced to the simple form described by equation (12) since the gain fluctuation term ($\Delta G/G$) can be neglected because it will be very small relative to the term of ($1/B_{RF}\tau$). However, these type solutions are not usually preferred since they make the passive imaging system very bulky and costly.

$$NETD = T_S\sqrt{\frac{1}{B_{RF}\tau}} \tag{12}$$

2.1.2.2 Dicke Radiometer

R. Dicke proposed an ingenious solution to evade the problems related to the gain fluctuations that arise due to $1/f$ flicker noises of the active devices [39]. In this solution,

a single-pole-double-throw (SPDT) switch, which is called Dicke switch, is placed between the antenna and the LNA as presented in Figure 11 that shows the detailed block diagram of the direct-detection Dicke radiometer architecture. The output of the SPDT switch is connected to the input of the LNA. One of the inputs of the SPDT switch is connected to the antenna, and the other one is connected to a reference resistance (R_{REF}) which is also known as the calibration reference load. In this way, the input of the LNA is continuously switched between the antenna and the calibration reference load with a frequency which known as Dicke switching frequency (f_D).

During one half of the Dicke switching period which is called the observation period, the signal picked by the antenna is transmitted to the input of the LNA. During the other half of the Dicke switching period which is called the calibration period, the noise power generated by the calibration reference impedance (R_{REF}) is transmitted to the input of the LNA. On the other hand, in the observation period, the DC signal produced by the power detector is directed to the positive path of the operational amplifier based subtractor circuit by the analog SPDT switch. On the contrary, in the calibration period, the DC signal produced by the power detector is directed to the negative path of the operational amplifier based subtractor circuit by the analog SPDT. And then, the difference of the signals obtained in the observation and calibration periods is taken by integrating the signal at the output of the operational amplifier based subtractor circuit by the integrator circuit. As a result, the noise equivalent temperature difference of a Dicke radiometer can be approximately expressed by equation (13) [40], where $T_{E-Dicke-R}$ is the equivalent noise temperature of the front-end receiver, T_{REF} is the calibration reference load, and $B_{Dicke-RF}$ is the effective RF noise bandwidth of the Dicke radiometer.

$$NETD_{Dicke} = \sqrt{\frac{2(T_A + T_{E-Dicke-R})^2 + 2(T_{REF} + T_{E-Dicke-R})^2}{B_{Dicke-RF}\tau} + \left(\frac{\Delta G}{G}\right)^2 (T_A - T_{REF})^2} \quad (13)$$

It is important to highlight here that the Dicke switching frequency should be set much higher than the $1/f$ flicker corner frequency of the front-end receiver to effectively employ the solution. Because, as mentioned before, the gain-fluctuations occur due to the $1/f$ flicker noise sources of the front-end receiver. If the Dicke switching period is set to be much smaller than the periods of the gain-fluctuations of the receiver, the gain will remain approximately the same for both of the observation and calibration periods. In

essence, by the Dicke switching technique, the output spectrum of the radiometer is shifted from DC to the Dicke switching frequency (f_D). Therefore, the output signal of the radiometer, which is a difference of the signals obtained in the observation and calibration periods, will be not affected by the gain-fluctuations of the front-end receiver if the physical noise temperature of the calibration reference load (T_{REF}) is equal to the antenna noise temperature (T_A), as presented in equation (14) where $T_{Dicke-S}$ is the overall system equivalent noise temperature which is equal to the sum of the antenna noise temperature (T_A) and the equivalent noise temperature of the front-end receiver ($T_{E-Dicke-R}$). As can be seen from the comparison of the NETD equations of the total power (7) and Dicke radiometers (14), the temperature resolution of the Dicke radiometer is twice that of the total power radiometer since the effective observation time reduces to its half (%50 duty cycle). In spite of this penalty factor of 2 in the Dicke radiometer, the improvement in the NETD performance is very much better than that of the total power radiometer since it is more than compensated by eliminating the gain-fluctuation term.

$$NETD_{Dicke} = 2T_{Dicke-S}\sqrt{\frac{1}{B_{Dicke-RF}\tau}} \tag{14}$$

The equivalent noise temperature of the front-end receiver of a Dicke radiometer can be calculated using equation (15), where T_{E-SPDT} is the equivalent noise temperature of the SPDT switch, G_{SPDT} is the gain of the SPDT switch, and G_{LNA} and is the gain of the LNA

$$T_{E-Dicke-R} = T_{E-SPDT} + \frac{T_{E-LNA}}{G_{SPDT}} + \frac{T_{E-PD}}{G_{SPDT}G_{LNA}} \tag{15}$$

Furthermore, the equivalent noise temperature of the front-end receiver of a Dicke radiometer can be directly found by equation (16), using the noise equivalent power ($NEP_{Dicke-R}$) of the overall front-end receiver circuit that consists of the SPDT switch, LNA, and the power detector.

$$T_{E-Dicke-R} = \frac{NEP_{Dicke-R}}{k\sqrt{B_{Dicke-RF}}} \tag{16}$$

The effective RF noise bandwidth of a Dicke radiometer can be calculated by equation (17) using the pre-detector gain ($G_{pre-detector}$).

$$B_{RF} = \frac{\left[\int_0^\infty G_{pre-detector}(f)df\right]^2}{\int_0^\infty G_{pre-detector}^2(f)df} \tag{17}$$

Finally, the integrated output signal can be converted to digital form using an ADC and data acquisition and then processed by a computer or a specific digital signal processor (DSP). As mentioned for the total power radiometer in Section 2.1.2.1, this radiometer channel is considered as a single pixel element, and a two-dimensional (2D) images can be created by using the aforementioned techniques.

2.2. Power Detector

2.2.1 Circuit Design and Implementation

The NETD of a radiometer is determined mainly by the NEP performance of the power detector. That is why starting with the design of the power detector to build a radiometer can be considered as a good starting point. The power detector produces an output voltage proportional to the input power. The relationship between the input power and the output voltage should be as linear as possible to detect the power difference at the input accurately. Therefore, the power detector should be operated in the square-law region.

The circuit schematic of the designed power detector is shown in Figure 14. A cascode like configuration was utilized for the first time beyond 100 GHz to perform power detection operation, and its NEP performance was analyzed for the first time for SiGe HBT technology. The CE transistor (Q1) produces a second-order DC current response to the input power. The first order response is eliminated by the shunt capacitor of 340 fF placed between the CE (Q1) and CB (Q2) transistors. Moreover, since this shunt capacitor acts almost perfect AC grounding path for operating frequency range, the input impedance of the CE transistor is isolated from the rest of the circuit. The CB transistor (Q2) can be considered as a unity gain current buffer. Although the output noise voltage is slightly increased by the CB transistor (Q2), it makes easier for the CE transistor (Q1) to remain in the forward active regime since the CB transistor (Q2) keeps the collector voltage of the CE (Q1) transistor as constant as possible. This improvement is presented in Figure 15 using the same load resistor (100 kΩ) and same bias voltage values. As can be seen from the figure, although the CE transistor (Q1) starts to operate in the saturation region for input powers larger than -24 dBm when operating stand-alone, it is kept staying in the forward-active region when configured with the CB transistor (Q2). In addition, it has been shown that a SiGe HBT biased with a forced emitter current can have a collector-emitter breakdown voltage (BV_{CEO}) that is twice as high as its nominal value [41]. Thence, the supply voltage V_{CC} of the power detector can be set to higher voltage values,

and it makes possible use of larger load resistor which results with larger responsivity and better NEP performance as will be explained later in this section.

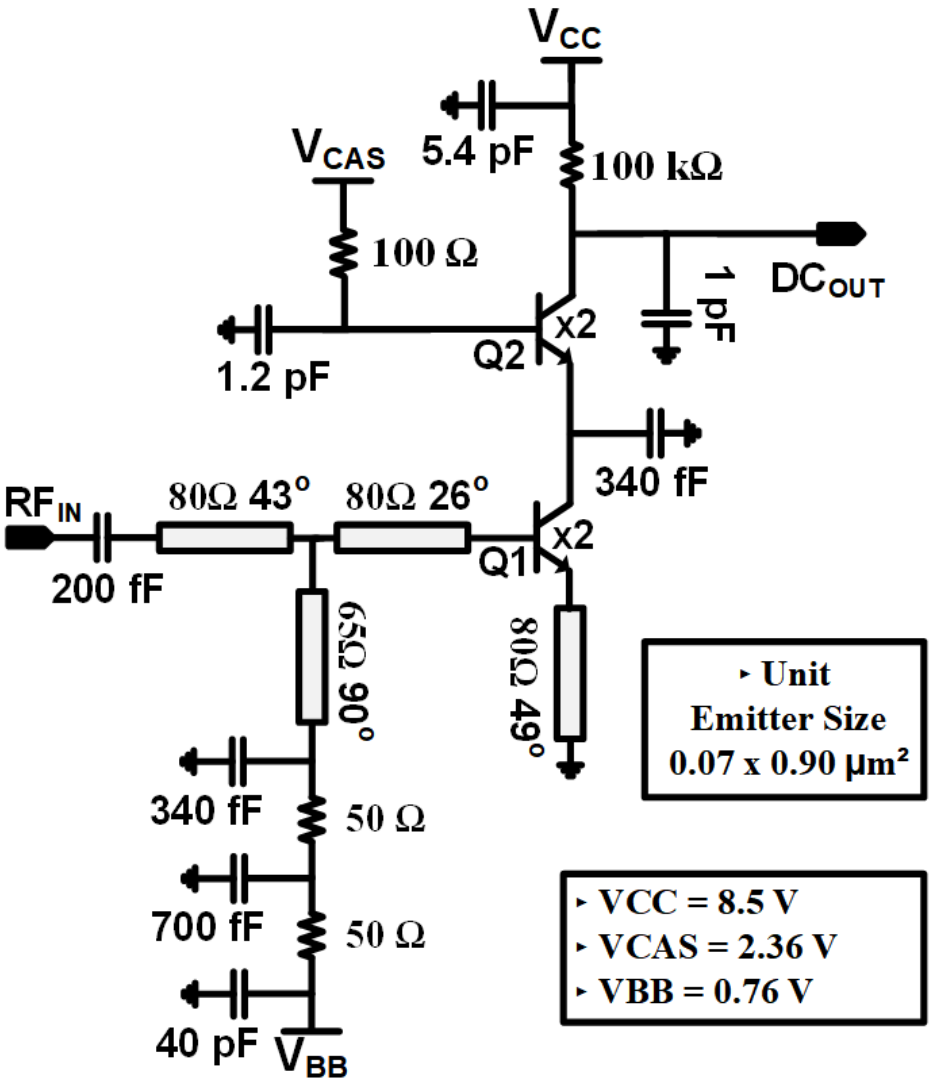

Figure 14 Circuit schematic of the D-band power detector (Electrical lengths of the transmission lines are given for 140 GHz).

In the cascode topology, the collector current of the whole circuit is determined by the CE transistor (Q1) since the current gain of the CB transistor is equal to one. Thus, assuming that the input signal at the base of the CE transistor is a sinusoidal-wave with an amplitude of $V_{in,}$ and a frequency of f, the collector current (I_c) can be expressed by equation (18) neglecting early voltage effect; where I_s is the saturation current, V_{BE} is the base-emitter bias voltage of the CE transistor (Q1), and V_T is the thermal voltage which equals to kT/q. It should be noted that equation (18) is valid for a transistor operating in the forward-active region.

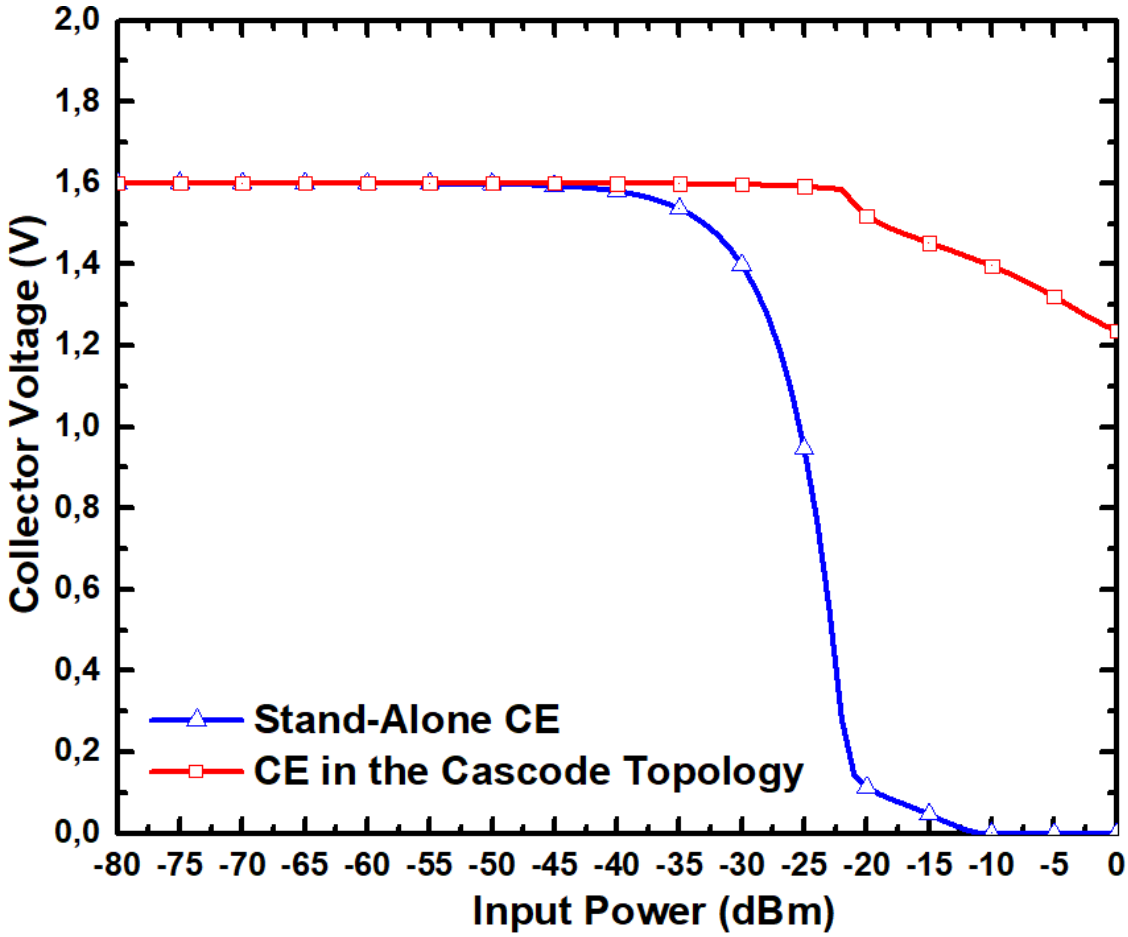

Figure 15 Collector voltage value of the CE transistor (Q1) in stand-alone operation and in the cascode configuration.

$$I_c = I_s e^{\frac{V_{BE} + V_{in}\sin(2\pi f t)}{V_T}} \tag{18}$$

If the quiescent current term ($I_s e^{V_{BE}/V_T}$) is subtracted from equation (18), the multiplication of the remaining expression with the load resistor (R_{LOAD}) gives the generated output voltage response to the input signal. Thence the output voltage response to the input signal is expressed by equation (19) where I_{CQ} is the quiescent collector current. Expanding equation (19) into Taylor's series and ignoring third and higher order terms, the output voltage response ($V_{out\text{-}response}$) can be approximated by equation (20).

$$V_{out-response} = I_{CQ} \times (e^{\frac{V_{in}\cos(2\pi f t)}{V_T}} - 1) \times R_{LOAD} \tag{19}$$

$$V_{out-response} \cong I_{CQ} \times (\frac{V_{in}\cos(2\pi f t)}{V_T} + \frac{V_{in}^2}{4V_T^2} + \frac{V_{in}^2\cos(2\pi(2f)t)}{4V_T^2}) \times R_{LOAD} \tag{20}$$

As can be seen from equation (20), it includes DC, fundamental and second harmonic components. The fundamental and second harmonic components can be easily removed

using a shunt-capacitor at the output of the CE transistor, as employed in Figure 14. Therefore, the DC voltage response ($V_{out\text{-}response\text{-}dc}$) to the input signal can be approximately expressed by equation (21). The DC output voltage response is proportional to the square of the input voltage of the transistor. This also points why the power detection operation is called as "square-law operation".

$$V_{out-response-dc} \cong I_{CQ} \times (\frac{V_{in}^2}{4V_T^2}) \times R_{LOAD} \tag{21}$$

Rewriting equation (21) in terms of the available power from source (P_{avs}), the impedance of the source (Z_s) and the input impedance (Z_{in}), the voltage response at the output ($V_{out\text{-}response\text{-}dc}$) to the input signal can be expressed by equation (22). The validity of equation (22) is demonstrated by comparison of the calculated and simulated result, as shown in Figure 16. The slight difference between the calculated and simulated curves can be attributed to the non-idealities of the I-V characteristics of the transistors.

$$V_{out-response-dc} \cong I_{CQ} \times (\frac{8P_{avs}Re\{Z_s\}\left|\frac{Z_{in}}{Z_s+Z_{in}}\right|^2}{4V_T^2}) \times R_{LOAD} \tag{22}$$

The responsivity of power detector, which defined as the change in dc output voltage per unit input power, is one of the most crucial performance metrics for radiometer systems. The responsivity (β) can be calculated by dividing equation (22) by the available source power (P_{avs}), as presented in equation (23) where α is a function of the input impedance (Z_{in}) and the impedance of the signal source (Z_s) ($\alpha = Re\{Z_s\}|Z_{in}/(Z_s+Z_{in})|^2$). As indicated in equation (23), the responsivity (β) of power detector is proportional to the quiescent current (I_{CQ}) and the load resistor (R_{LOAD}) of the power detector, and inversely proportional to the square of its operating temperature. It is quite worth to say here that the analysis for the responsivity presented above is valid under the condition that the input power is small enough to guarantee that the transistors are operating in the forward-active region.

$$\beta = \frac{V_{out-response-dc}}{P_{avs}} \cong I_{CQ}\left(\frac{8Re\{Z_s\}\left|\frac{Z_{in}}{Z_s+Z_{in}}\right|^2}{4V_T^2}\right)R_{LOAD} = \alpha\frac{I_{CQ}}{V_T^2}R_{LOAD} \tag{23}$$

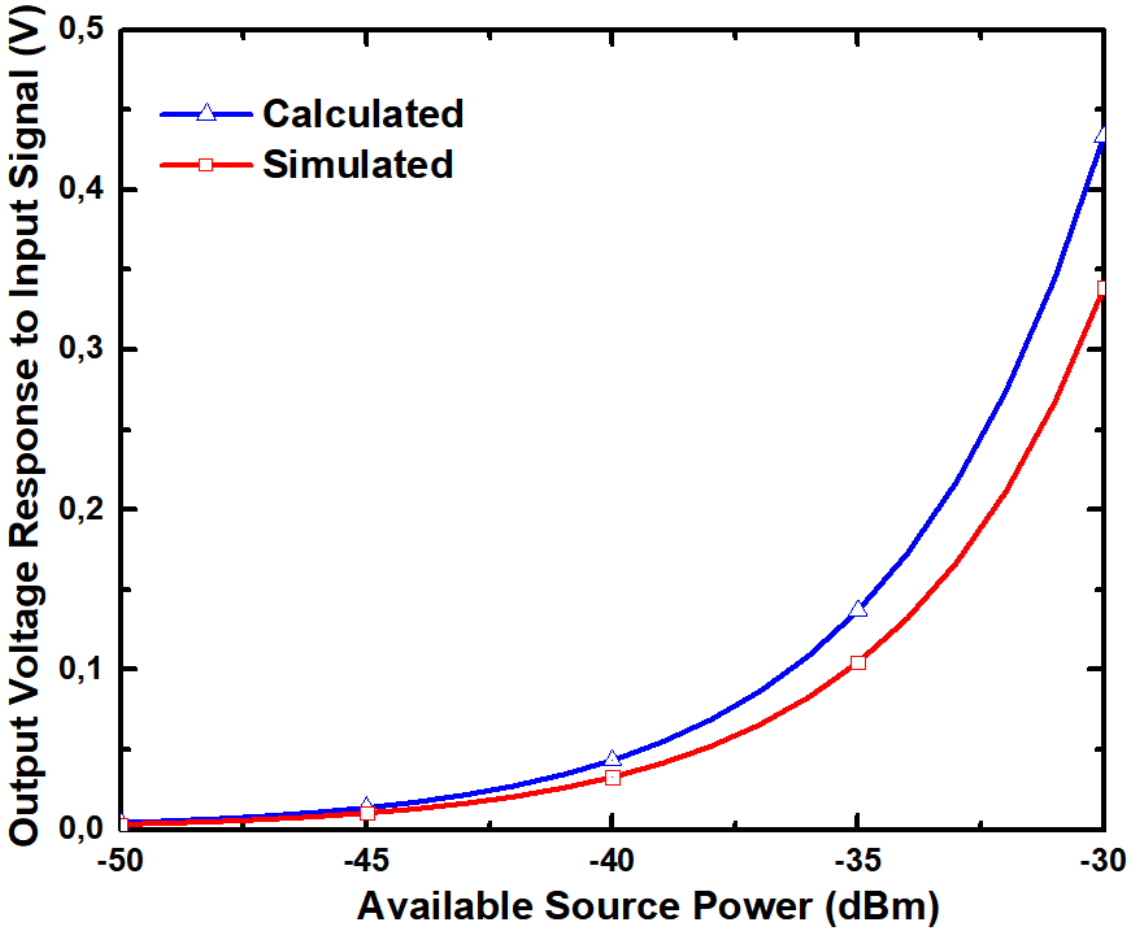

Figure 16 Output voltage response to the available source power.

The NEP (in $W/Hz^{1/2}$) of a power detector, which is defined as the ratio of the output noise voltage spectral density (S_{vo}) (in $V/Hz^{1/2}$) to the responsivity (β) as indicated in equation (24), is considered as the obvious figure-of-merit of the power detectors in the passive imaging systems.

$$NEP = \frac{S_{vo}}{\beta} \tag{24}$$

The NEP points out the minimum input power that can be detected. In other words, the NEP defines the required minimum input power to obtain a unity signal-to-noise ratio at the output of the power detector. In order to find out the expression of the NEP of a power detector, we first need to figure out the output noise power spectral density ($\overline{V_n^2}/\Delta f$) of the power detector. There are four major noise sources at low frequencies in a SiGe HBT: the flicker noise ($1/f$), the thermal noise of the parasitic base resistance (V_{rbn}), the base shot noise (i_{bn}), and the collector shot noise (i_{cn}). The flicker noise (or $1/f$ noise) can be ignored since the circuit will be modulated at the Dicke switching frequency (10 kHz)

which is far above the $1/f$ corner frequency illustrated in Figure 17 that shows the low-frequency output noise voltage spectral density of the designed circuit. The low-frequency small-signal equivalent circuit of the cascode configuration based power detector including the major noise sources is shown in Figure 18. It should not be forgotten here that the base-emitter and collector output resistances (r_{be} and r_o) represent real parts of impedances without having thermal noise. The base-emitter, collector-base, collector-emitter, and collector-substrate capacitances can be ignored because they behave as open circuits in the frequency of interest (10 kHz). The total output noise power spectral density ($\overline{V_{no}^2}/\Delta f$) was derived by considering Figure 18. The superposition theorem was applied to calculate the total output noise power spectral density ($\overline{V_{no}^2}/\Delta f$) since the correlation between the presented noise sources can be ignored in the frequency domain of interest. The output noise power spectral density terms due to each noise source were derived, as presented in equations (25(32), where *k* is the Boltzmann constant, I_{BQ} and I_{CQ} are quiescent currents. The total output noise power spectral density ($\overline{V_{no}^2}/\Delta f$) is equal to the sum of all these terms. When the parameters in these terms are roughly evaluated, it is clear that the collector shot noise of the CE transistor (i_{cn1}) and the thermal noise of the load resistor (v_{load}) are dominant. Thus, the total output noise power spectral density ($\overline{V_{no}^2}/\Delta f$) can be simplified to equation (33).

$$\overline{V_{no(R_s)}^2}/\Delta f \cong 4kTR_S \times \left(\frac{|R_{BE1}|}{|R_{BE1}+r_{bn1}+R_s|}\right)^2 \times gm_1^2 \times R_{LOAD}^2 \tag{25}$$

$$\overline{V_{no(rbn1)}^2}/\Delta f \cong 4kTr_{bn1} \times \left(\frac{|R_{BE1}|}{|R_{BE1}+r_{bn1}+R_s|}\right)^2 \times gm_1^2 \times R_{LOAD}^2 \tag{26}$$

$$\overline{V_{no(Ibn1)}^2}/\Delta f \cong 2qI_{BQ1} \times \left(\frac{|r_{bn1}+R_s|}{|R_{BE1}+r_{bn1}+R_s|}\right)^2 \times R_{BE1}^2 \times gm_1^2 \times R_{LOAD}^2 \tag{27}$$

$$\overline{V_{no(Icn1)}^2}/\Delta f \cong 2qI_{CQ} \times R_{LOAD}^2 \tag{28}$$

$$\overline{V_{no(rbn2)}^2}/\Delta f \cong 4kTr_{bn2} \times \left(\frac{|gm_2R_{BE2}|}{|r_{o1}(1+gm_2R_{BE2})|}\right)^2 \times R_{LOAD}^2 \tag{29}$$

$$\overline{V_{no(Ibn2)}^2}/\Delta f \cong 2qI_{BQ2} \times \left(\frac{|gm_2r_{bn2}R_{BE2}|}{|r_{bn2}+(r_{o1}(1+gm_2R_{BE2})|}\right)^2 \times R_{LOAD}^2 \tag{30}$$

$$\overline{V_{no(Icn2)}^2}/\Delta f \cong 2qI_{CQ2} \times \left(\frac{1}{|1+gm_2R_{BE2}|}\right)^2 \times R_{LOAD}^2 \tag{31}$$

$$\overline{V_{no_{(R_{LOAD})}}^2}/\Delta f \cong 4kTR_{LOAD} \quad (32)$$

$$V_{no}^2/\Delta f = 2qI_{CQ}R_{LOAD}^2 + 4kTR_{LOAD} \quad (33)$$

As mentioned earlier, the NEP (in $W/Hz^{1/2}$) of a power detector is defined as the ratio of the output noise voltage spectral density (S_{vo}) (in $V/Hz^{1/2}$) to the responsivity (β). If the square root of the total output noise power spectral density ($\overline{V_{no}^2}/\Delta f$) (33) and the responsivity (β) (23) expressions are substituted into the equation of the NEP (24), then the NEP can be expressed by equation (34).

$$NEP = \frac{S_{vo}}{\beta} = \frac{\sqrt{\frac{\overline{V_{no}^2}}{\Delta f}}}{\beta} = \frac{\sqrt{2qI_{CQ}R_{LOAD}^2 + 4kTR_{LOAD}}}{\alpha \frac{I_{CQ}}{V_T^2} R_{LOAD}} = \frac{V_T^2}{\alpha}\sqrt{\frac{2q}{I_{CQ}} + \frac{4kT}{I_{CQ}^2 R_{LOAD}}} \quad (34)$$

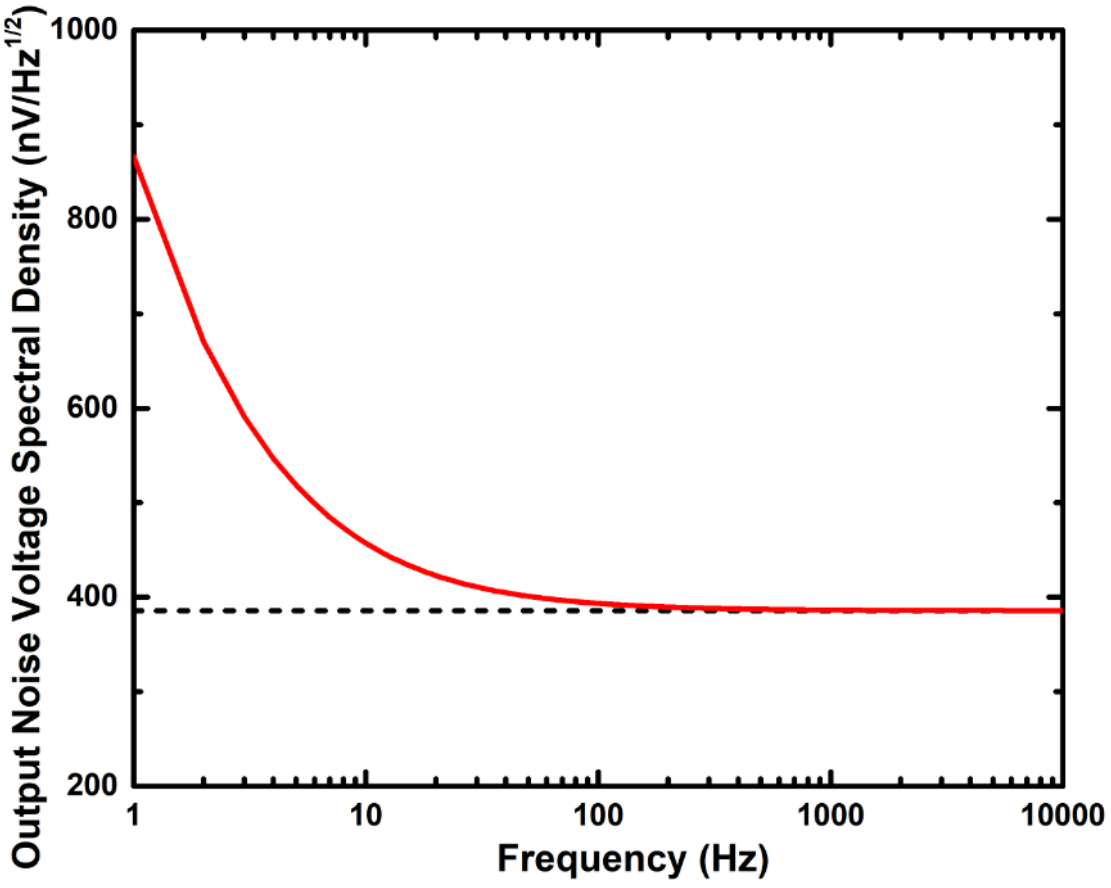

Figure 17 Output noise voltage spectral density of the designed power detector (schematic based result).

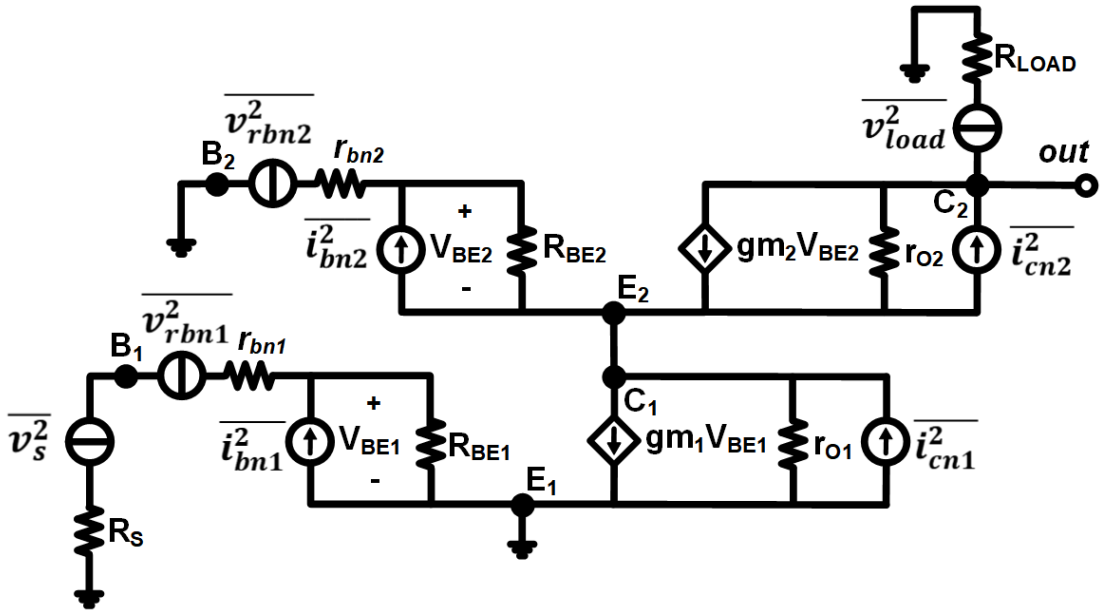

Figure 18 Low frequency small-signal equivalent circuit of the cascode configuration.

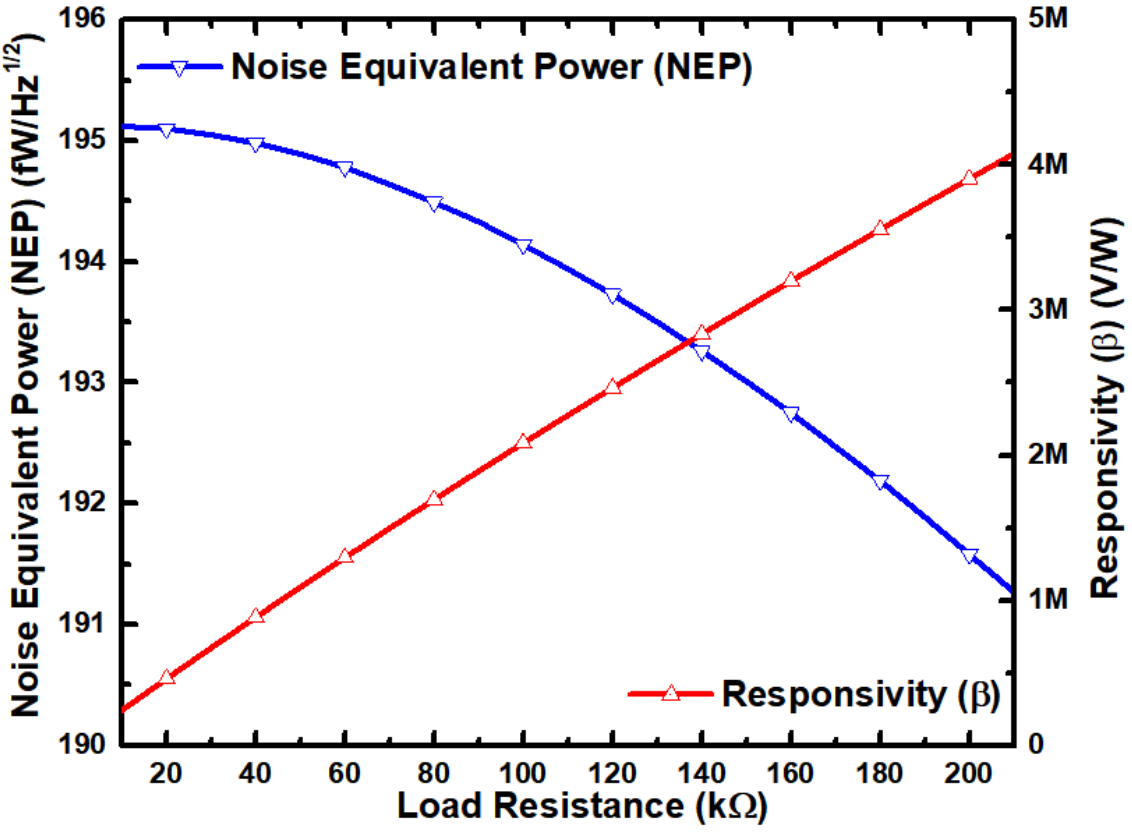

Figure 19 NEP and responsivity (β) versus load resistance (R_{LOAD}) (Loss due to the impedance mismacth between the input of the transistor and the source was de-embedded) (@140 GHz).

As can be seen from (34), the NEP performance of a power detector can be improved by increasing the load resistance (R_{LOAD}) and the quiescent current (I_{CQ}). But this improvement is limited due to two reasons. Firstly, higher quiescent current (I_{CQ}) and larger load resistance (R_{LOAD}) will cause a significant voltage drop between the supply voltage (V_{CC}) and the collector of the CB transistor (Q2), and it would saturate the both transistors. Even though this problem will be able to be solved by increasing the supply voltage (V_{CC}) to a voltage level that will not damage the transistors, a small increase of the amplitude of the input signal (V_{in}) would cause a significant voltage drop again. The second reason is that the maximum current values which can flow through high value resistances in semiconductor technologies are very limited. For the used semiconductor process (IHP's SG13G2), the highest value resistor material, which is made by p-doped gate polysilicon, can drain a maximum 0.15 mA current, for a width of 0.5 μm.

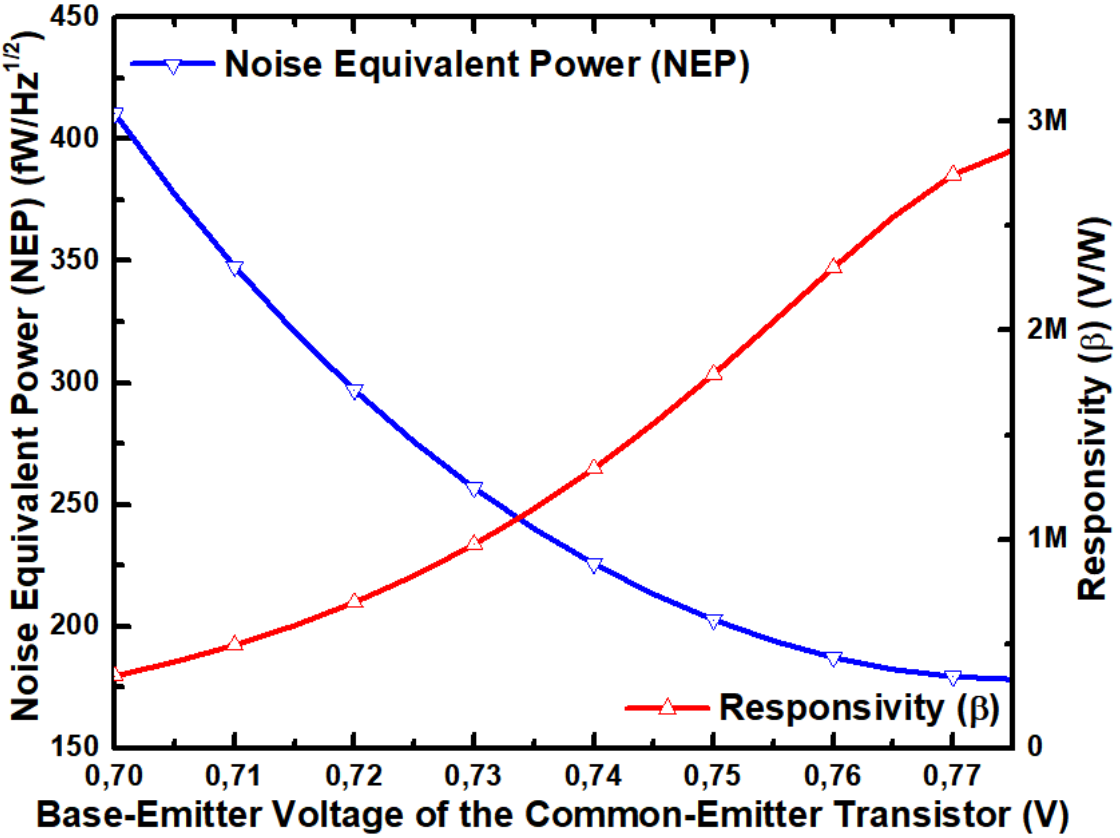

Figure 20 NEP and responsivity (β) versus the base-emitter voltage of the CE transistor (Loss due to the impedance mismacth between the input of the transistor and the source was de-embedded) (@140 GHz).

The dependence of the NEP performance on the load resistance (R_{LOAD}) is shown in Figure 19 for same quiescent current and the same quiescent voltage value at the collector of the CB transistor. As expected from the equations derived for the NEP and the responsivity (β), the performance of the power detector circuit increases with increasing load resistance (R_{LOAD}). Figure 20 shows the dependence of the NEP performance on the quiescent current (I_{CQ}) while using same load resistance (R_{LOAD}) and having the same quiescent voltage value at the collector of the CB transistor. The quiescent current (I_{CQ}) was increased up to the allowed maximum current value for the used resistor material. The trade-offs and aforementioned limitations were carefully evaluated, and a higher load resistor (R_{LOAD}) was chosen instead of higher quiescent current value (I_{CQ}) to minimize NEP of the power detector. In order to improve NEP, the responsivity (β) of the circuit should be increased, i.e. the second-order dc response of the CE transistor (Q1) should be enhanced as possible. Therefore, the transistor size should be as small as possible, as verified by the simulation result shown in Figure 21.

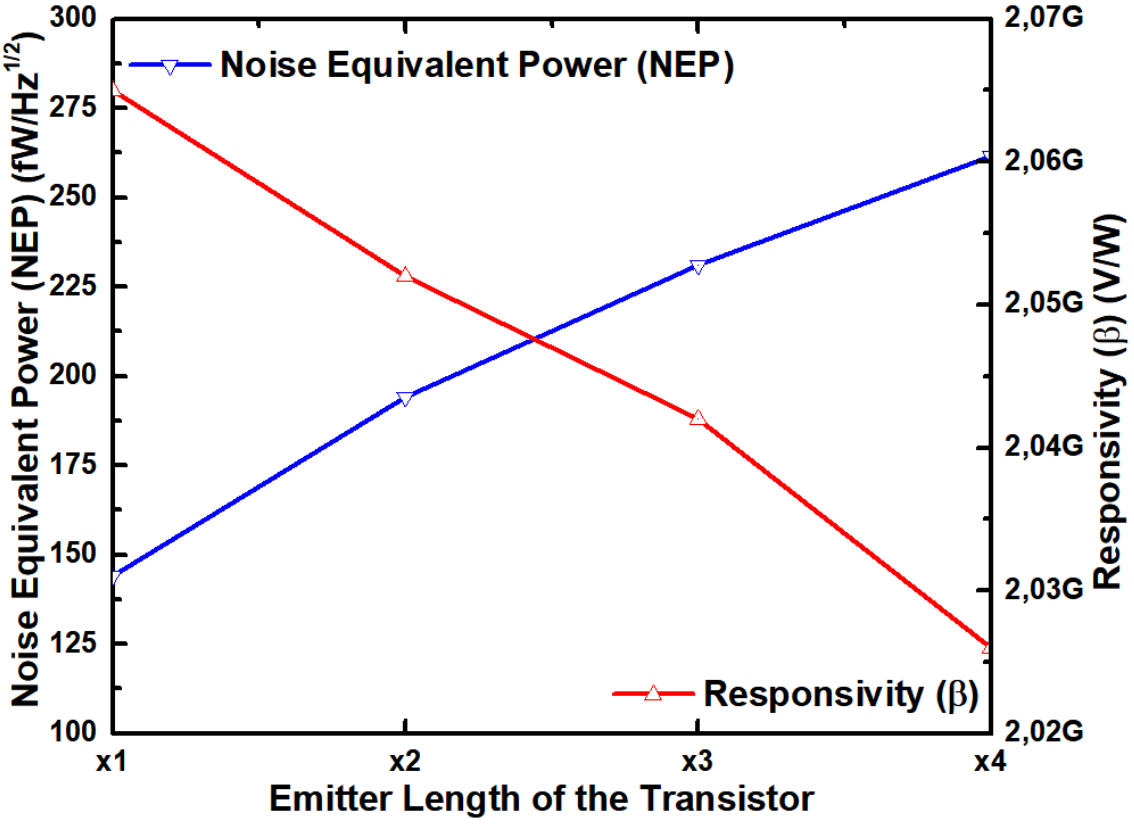

Figure 21 NEP and responsivity (β) versus the emitter length of the transistor (Loss due to the impedance mismacth between the input of the transistor and the source was deembedded) (@140 GHz)

The available power at the input of the power detector should be transmitted to the input of the first transistor (Q1) without having losses due to the impedance mismatching to not degrade the responsivity (β). Thus, the impedance matching between the input of the power detector and the input of the first transistor (Q1) have a significant effect on the responsivity (β), so also on the NEP performance of the power detector. It is very important to have a low NEP value across a broadband frequency range to mimize the NETD value of the radiometer. As explained before, if the transistor size is set to minimum value, the NEP performance is obtained. But this results in narrowband impedance matching because of the very large input impedance of the transistor.

After all these design guidelines had been taken into account and evaluated, the quiescent current (I_{CQ}) was set to 50 μA, a 100 kΩ load resistance (R_{LOAD}) was used, and the emitter size of the transistor was chosen to be 2x unit.

The transmission line based T-type matching network was used to perform the impedance matching between the input of the power detector circuit and the input of the first transistor (Q1). All the transmission lines were implemented as microstrip lines with Top Metal 2 – Metal 1 configuration and all of them were meandered to reduce the chip area. A MIM capacitor of 200 fF was employed to perform DC blocking, as well as to contribute to the input impedance matching slightly. Parasitic capacitance due to the RF pad was not included in the input impedance matching. Instead, a Through-Reflect-Line (TRL) de-embedding fixture was utilized to de-embed the effect of RF-pad and shift the reference plane. The collector of the CE transistor (Q1) was shunted by a MIM capacitor of 340 fF to remove the fundamental signal component, and to isolate the input impedance of the CE transistor (Q1) from the rest of the circuit. The load resistance of 100 kΩ was realized by a p-doped gate polysilicon. Full-chip electromagnetic (EM) simulations were performed by ADS Momentum. The 3D layout view taken from the electromagnetic simulation setup of the D-band power detector is shown in Figure 22.

An ideal bias network should provide a very good AC grounding for all frequencies, but this is not practically possible. For this reason, at least, the bias line network should provide a very good AC grounding for the frequency range of interest. A capacitor has a self-resonance frequency (SRF) depending on its geometrical structure and its size. For instance, the SRF of the 340 fF capacitor which was on the base-bias line is 140 GHz in the used process technology (IHP's SG13G2), and it can just provide an acceptable AC

grounding between 100 GHz and 180 GHz. Another bypass capacitor should be placed on the base-bias line to ground smaller frequencies, but if it is connected in parallel to the first bypass capacitor, their parasitics will be added up, and it would result in unexpected and undesired frequency response. Therefore, a small value resistor should be placed on the bias line, between these two-bypass capacitors. That is why a double RC section was utilized on the base-bias line, as presented in Figure 14.

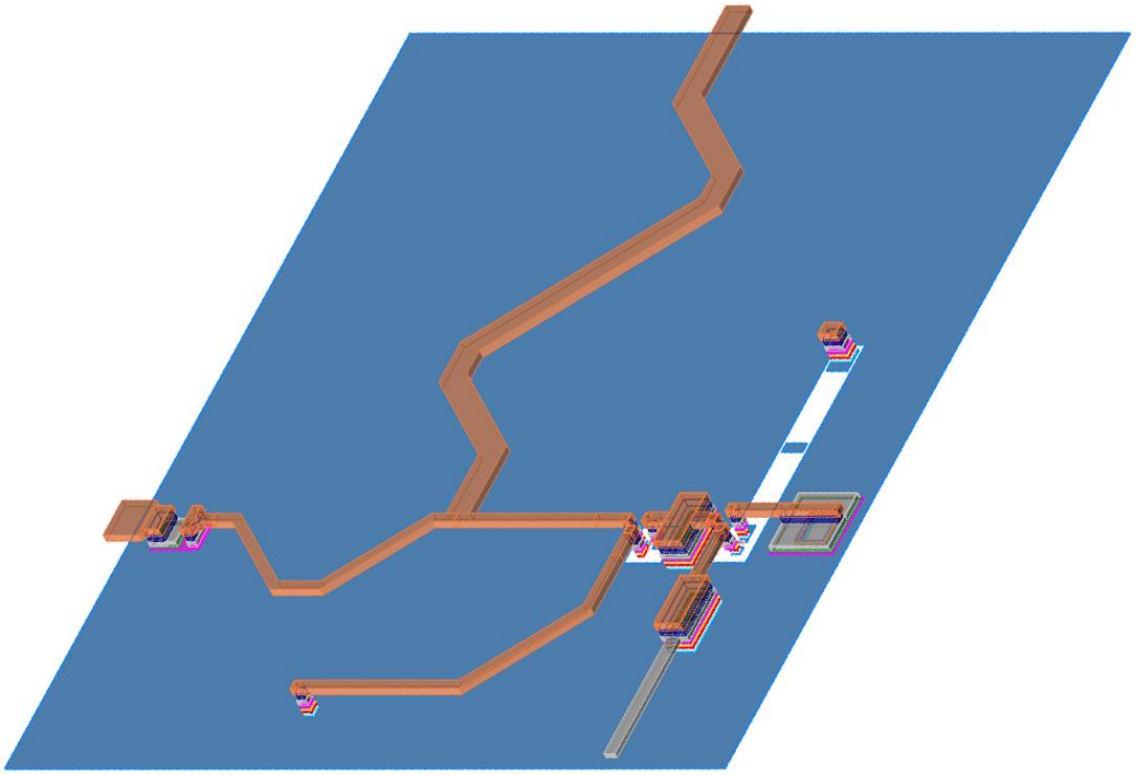

Figure 22 3D layout view taken from the electromagnetic simulation setup of the D-band power detector.

2.2.2 Simulation and Measurement Results

The chip microphotograph of the designed power detector is shown in Figure 23. The effective chip area excluding the pads and de-embedding lines is 0.18 mm^2, and the total area of the integrated circuit is 0.32 mm^2. The total quiescent power consumption is 0.43 mW.

S-parameters of the power detector were measured by Keysight N5224A PNA whose frequency extended to 110-170 GHz using a Virginia Diodes Inc. (VDI) WR6.5 frequency extension module. One-port SOL calibration was performed by an ISS from Cascade-Microtech to move the reference plane to the probe tip. The power at the probe

tip was set to be less than -40 dBm along the D-band to guarantee that the power detector is operating in the square-law region. Later, one-port SOL de-embedding algorithm on Cascade WinCal XE software was performed using the data obtained from on-chip de-embedding structures to remove the parasitic effects of the RF pad. Figure 24 shows the simulated and measured s-parameters of the power detector. As can be seen from Figure 24, there is a quite good agreement between the simulated and measured s-parameter results. The return loss of the power detector is better than 10 dB between 123 and 170 GHz with the RF-pad, and better than 10 dB along the D-band without the RF-pad.

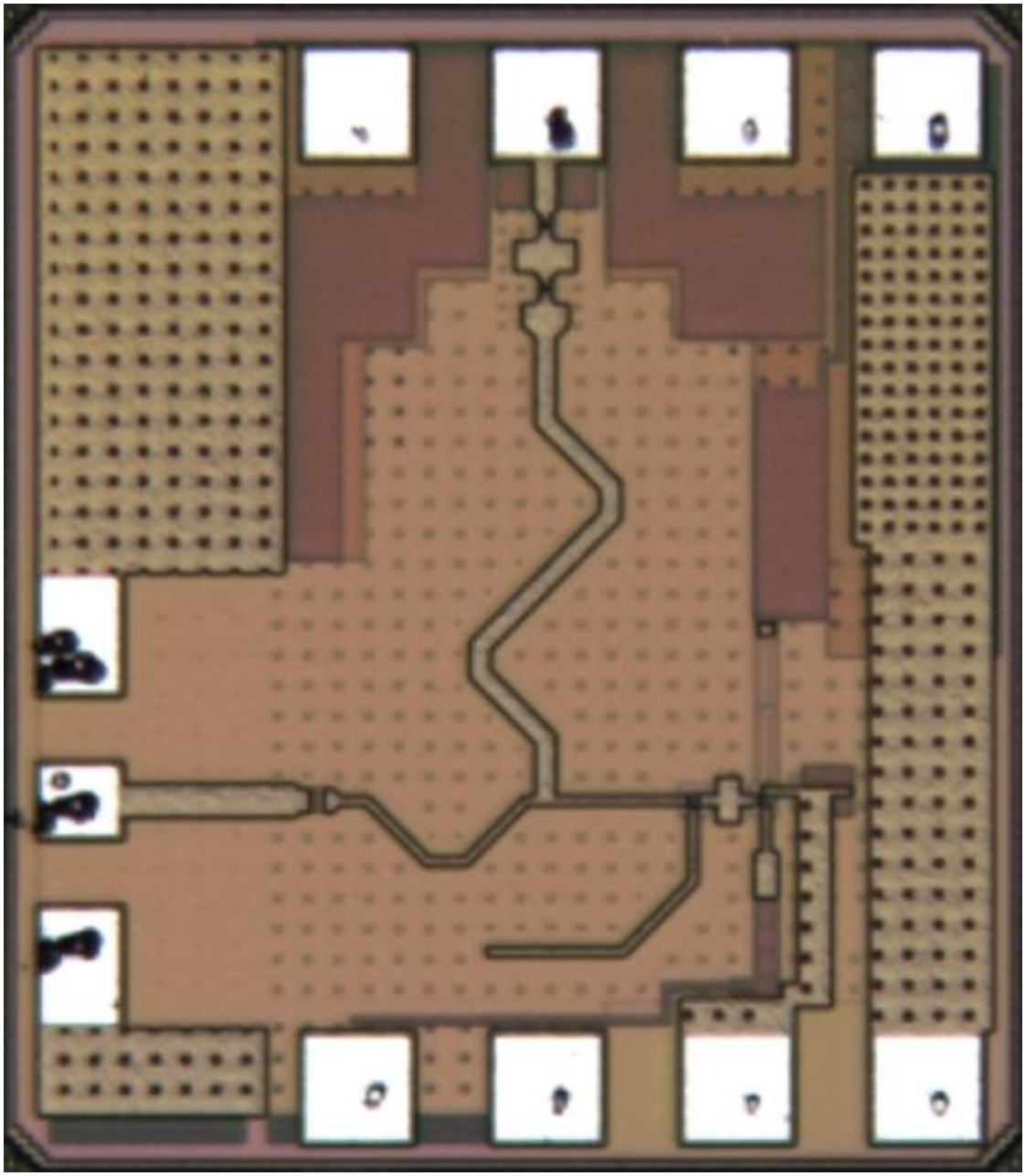

Figure 23 Chip microphotograph of the designed power detector (0.53 mm × 0.61 mm).

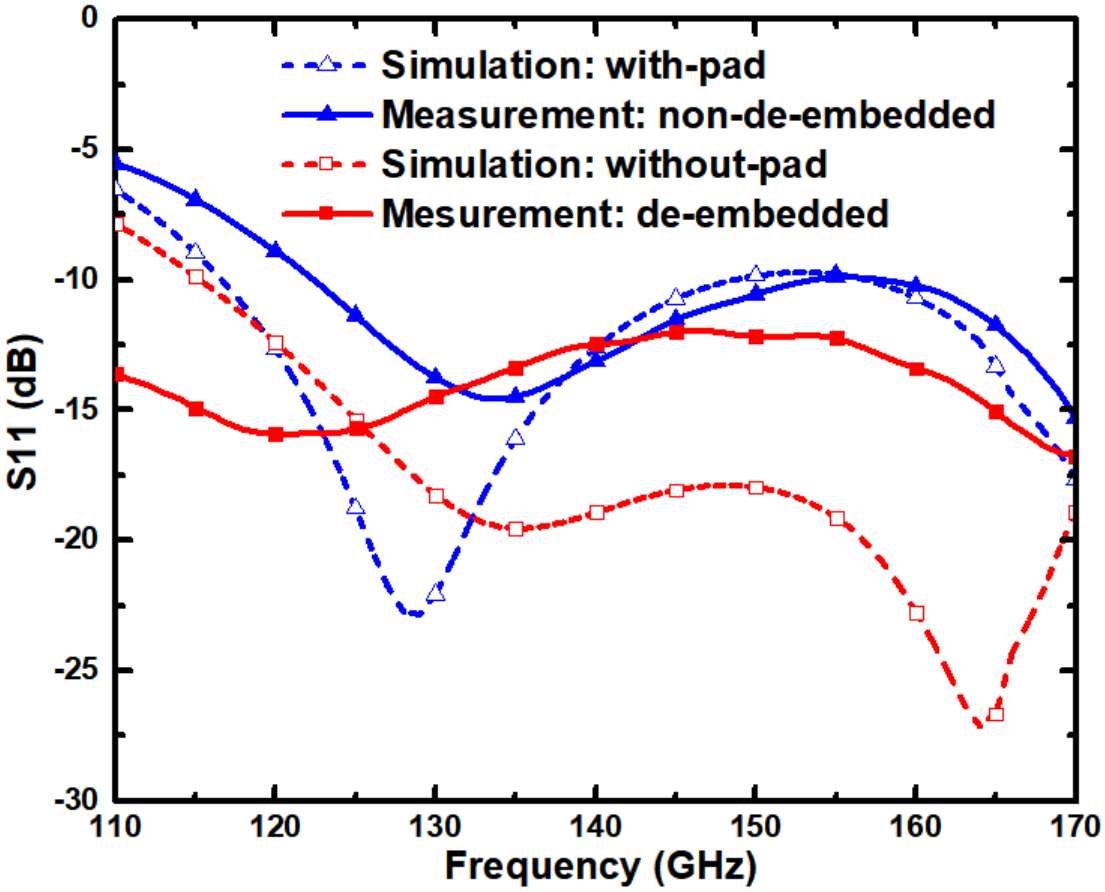

Figure 24 Simulated and measured s-parameter results of the power detector.

An experimental test setup, which is shown in Figure 25, was set to measure the 1/f flicker noise of the power detector. The input of the power detector was externally terminated by a WR6.5 waveguide 50Ω load. The noise voltage at the output of the power detector was amplified by an external low-noise pre-amplifier (SR-550) and then measured by Keysight 35670A dynamic signal analyzer between 1 Hz and 10 kHz. Later, the gain of SR-550 was de-embedded from the measurement.

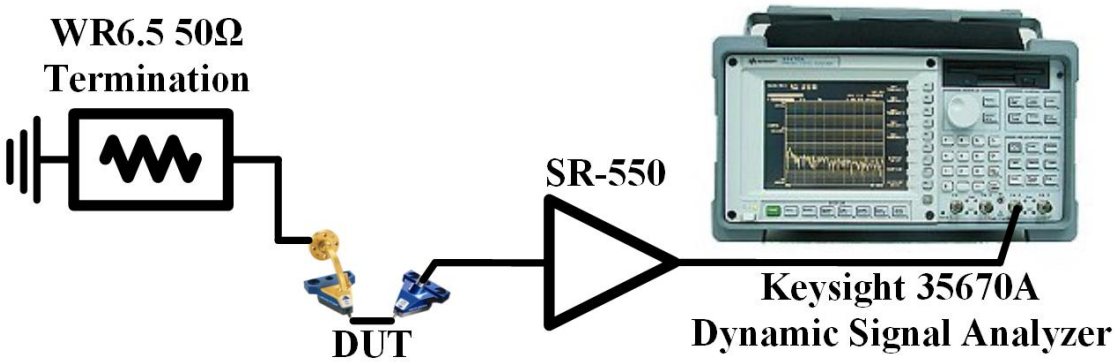

Figure 25 Experimental setup for the measurement of the 1/f flicker noise of the power detector.

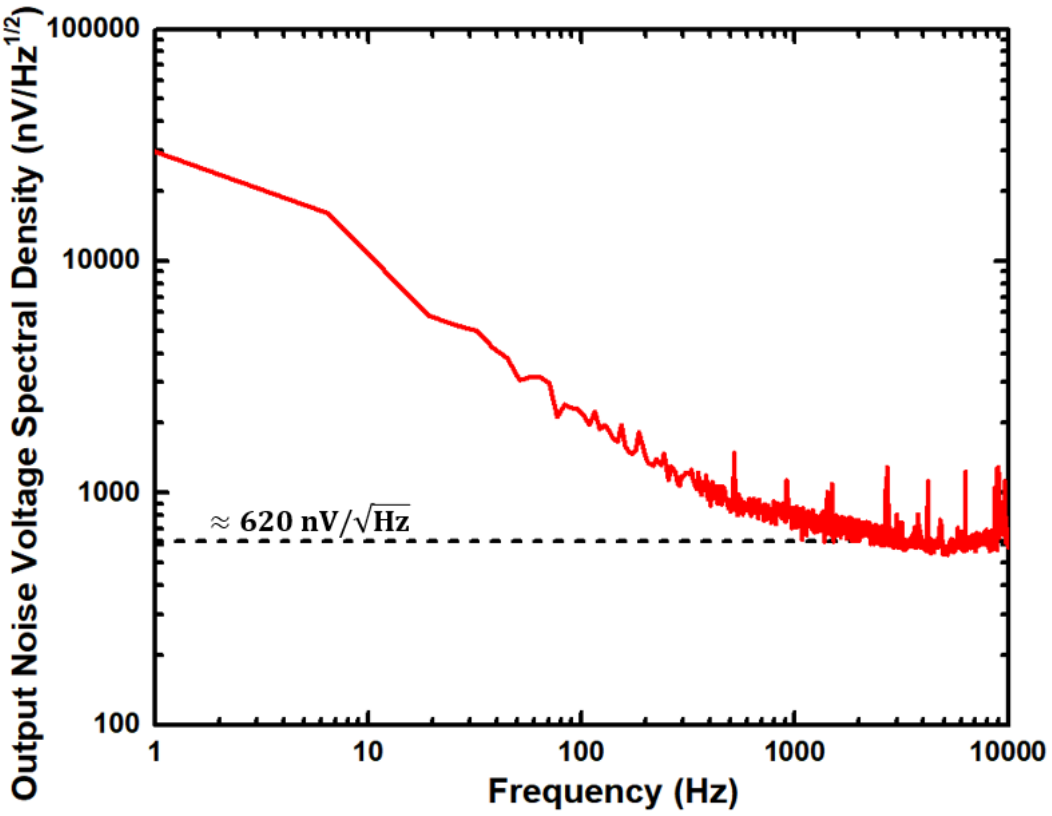

Figure 26 Measured $1/f$ flicker noise of the power detector.

The measured low-frequency output noise voltage spectral density of the power detector is presented in Figure 26. The output noise voltage spectral density is almost constant (620 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$) above 2 kHz which can be also considered as the $1/\mathrm{f}$ corner frequency of the power detector. As mentioned earlier, the Dicke switching frequency should be set to be far away from 2 kHz. Therefore, the output noise voltage spectral density (S_{vo}) was taken as 620 $nV/\sqrt{Hz}$ in the noise equivalent power *(NEP)* calculations.

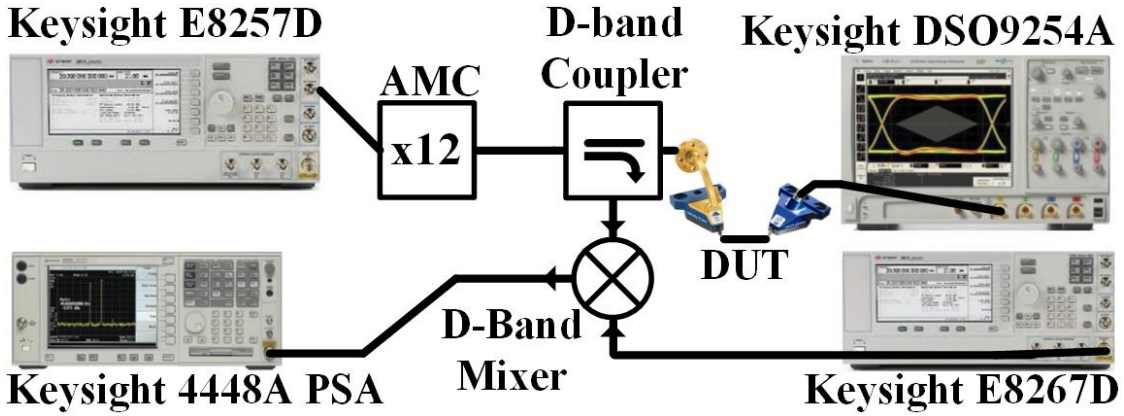

Figure 27 Experimental test setup for the measurement of the output voltage waveform and the responsivity of the power detector.

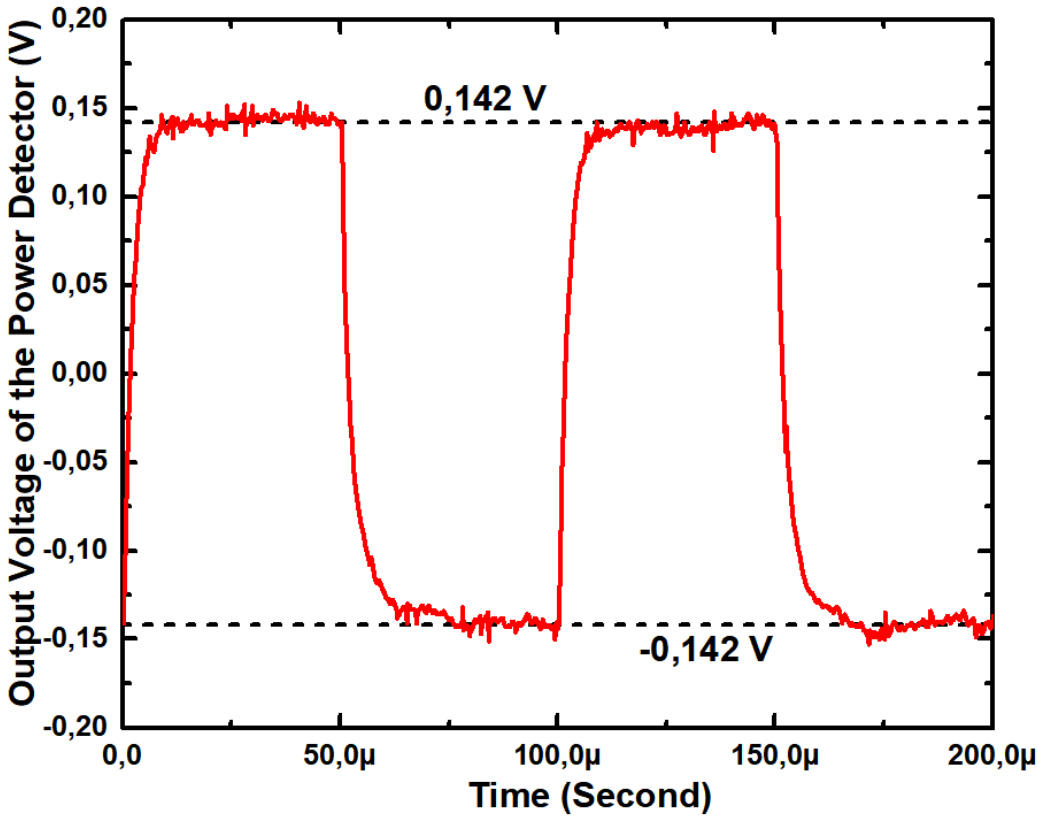

Figure 28 Measured output voltage waveform of the power detector (@140 GHz).

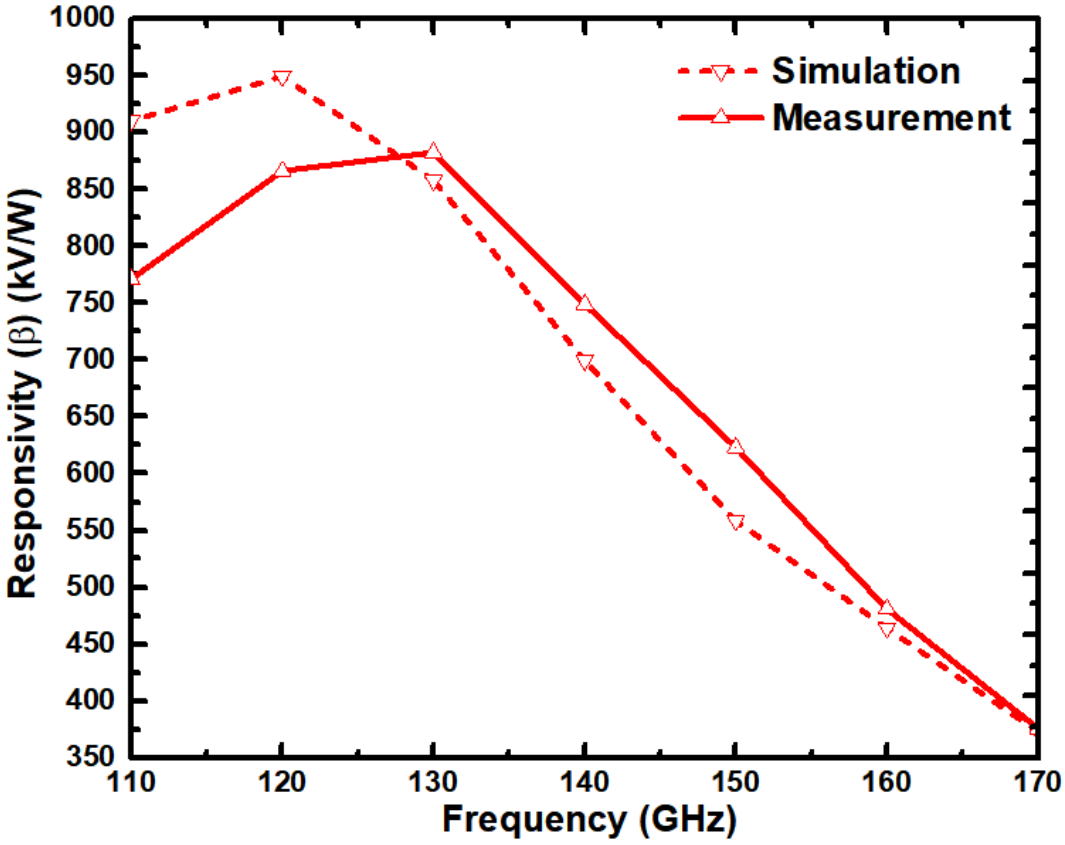

Figure 29 Simulated and measured responsivity of the power detector.

Figure 27 shows the experimental test setup which was used to observe the output voltage waveform and to measure the responsivity of the power detector. It is very important to know exactly the power at the probe tip at the input of the power detector to measure the responsivity correctly. Therefore, first, the conversion loss between the "a" port of the D-band directional coupler and the IF port ("b") of the D-band direct down-conversion mixer was measured by connecting a D-band power meter to the "a" port of the D-band directional coupler. It was verified that this conversion loss is constant for all power levels that would be used during the responsivity measurements. Second, a second probe, which is identical to the presented probe (at left in the figure), was connected to the D-band power meter, and in this way, the total insertion loss of the two s-bend waveguides and two probes was measured using a small through-line on the ISS. By dividing this value by half, the insertion loss between the "a" port of the D-band directional coupler and the probe tip was found. The insertion losses figured out above were taken into account while measuring the responsivity of the power detector.

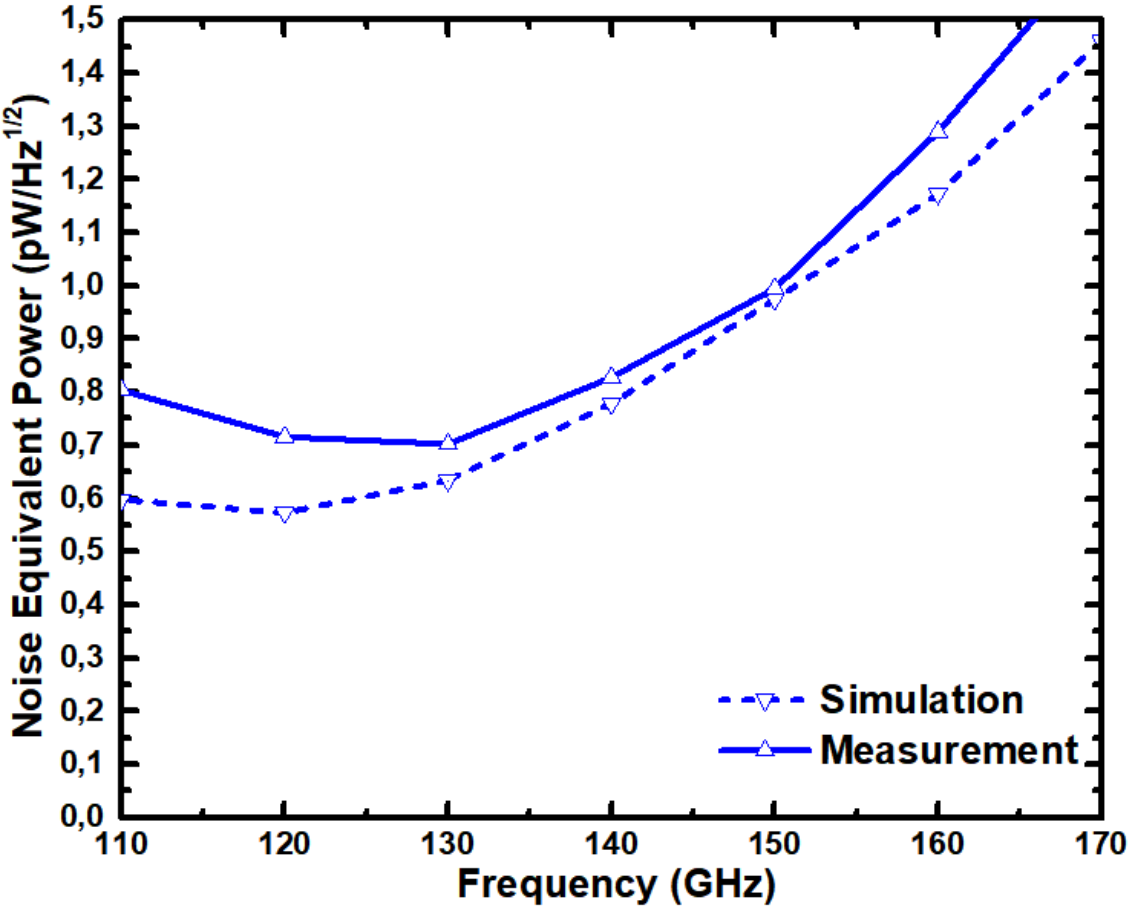

Figure 30 Simulated and measured NEP of the power detector.

An input signal to the input of the power detector which was AM modulated at 10 kHz with a modulation depth of %100 was applied to emulate the impact of the Dicke switch. Figure 28 shows the measured output voltage waveform of the power detector while the power of the input signal varies from -34.2 dBm to -60 dBm at 140 GHz. As mentioned earlier and presented in equation (23), the responsivity can be calculated by dividing the change in dc output voltage by the change in input power. This procedure was repeated with 10 GHz step-size between 110 and 170 GHz. The simulated and measured responsivity results of the power detector are presented in Figure 29. As can be seen from the figure, the measured curve matches well with the simulated result. The measured peak responsivity value of the power detector is about 883 kV/W at 130 GHz. It gradually decreases after 130 GHz, and its minimum value is about 373 kV/W at 170 GHz.

The NEP of the power detector was calculated by dividing the output noise voltage spectral density by the responsivity. Figure 30 shows the simulated and measured NEP of the power detector. The measured NEP is better than 1 $pW/Hz^{1/2}$ over 110-150 GHz frequency range, and its minimum value is about 0.7 $pW/Hz^{1/2}$ at 130 GHz. The slight discrepancy between the simulation and measurement results above 120 GHz can be attributed to that the measured responsivity value is slightly better than the simulation in at the same frequency range.

2.2.3 Comparison

The performance comparison of the power detector with previously reported D-band power detectors implemented in silicon technologies is summarized in Table 3. The NEP performance of a power detector is the most important parameter, which is also considered as the figure-of-merit (FoM) of the power detectors in the passive imaging systems. The designed power detector achieves the best noise equivalent power performance compare to previously reported D-band power detectors implemented in silicon technologies. Moreover, the designed power detector has the highest responsivity among the other silicon-based studies in the literature, thanks to higher value load resistor. Even though the use of high resistance results in a lower power compression point of approximately -30 dBm, it is not a priority performance criterion for the passive imaging applications. These results point that the D-band power detector shows the state-of-the-art performance and emphasize the suitability of the power detector for mm-wave passive imaging systems to achieve excellent NETD performance.

Table 3 Summary of performance comparison of the D-band power detector with previously reported D-band power detectors implemented in silicon technologies.

	Technology	**NEP ($pW/Hz^{1/2}$)**	**Responsivity (kV/W)**	**R_{LOAD} ($k\Omega$)**	**S11 <-10 dB (GHz)**	**Area ($mm2$)**
[42]	*45nm* CMOS SOI	8	3	1	167-194	0.20
[43]	*90nm* SiGe BiCMOS	2.7	10	1	125-170	0.21
[44]	*90nm* SiGe BiCMOS	0.7	11	0.6	145-170	0.05*
[44]	*90nm* SiGe BiCMOS	1.25	14.5	1	N/A	0.02*
[45]	*0.13µm* SiGe BiCMOS	10	10	1	-	N/A
This Work	***0.13µm* SiGe BiCMOS**	**0.7**	**883**	**100**	**110-170**	**0.18***

* Excluding the pads

2.3. Low-Noise Amplifier

2.3.1 Circuit Design and Implementation

The circuit schematic of the designed LNA is shown in Figure 31. The designed LNA consists of four cascode stages. In order to reduce the noise contribution of the CB transistor, a shunt inductor was placed between the CE and CB transistors, which is based on the technique proposed in [46] for WLAN applications and CMOS technology. The effect of this shunt inductor on the noise figure performance of the cascode configuration was analyzed for the SiGe HBT technology. Furthermore, a Butterworth approximation based staggered tuning technique was utilized to enhance the bandwidth and improve the gain flatness of the LNA.

The amplitude of the signal collected by the antenna is expected to be very low, around -100 dBm, as analyzed in Section 2.1. A high-gain LNA is required to amplify the signal collected by the antenna and to suppress the noise of the power

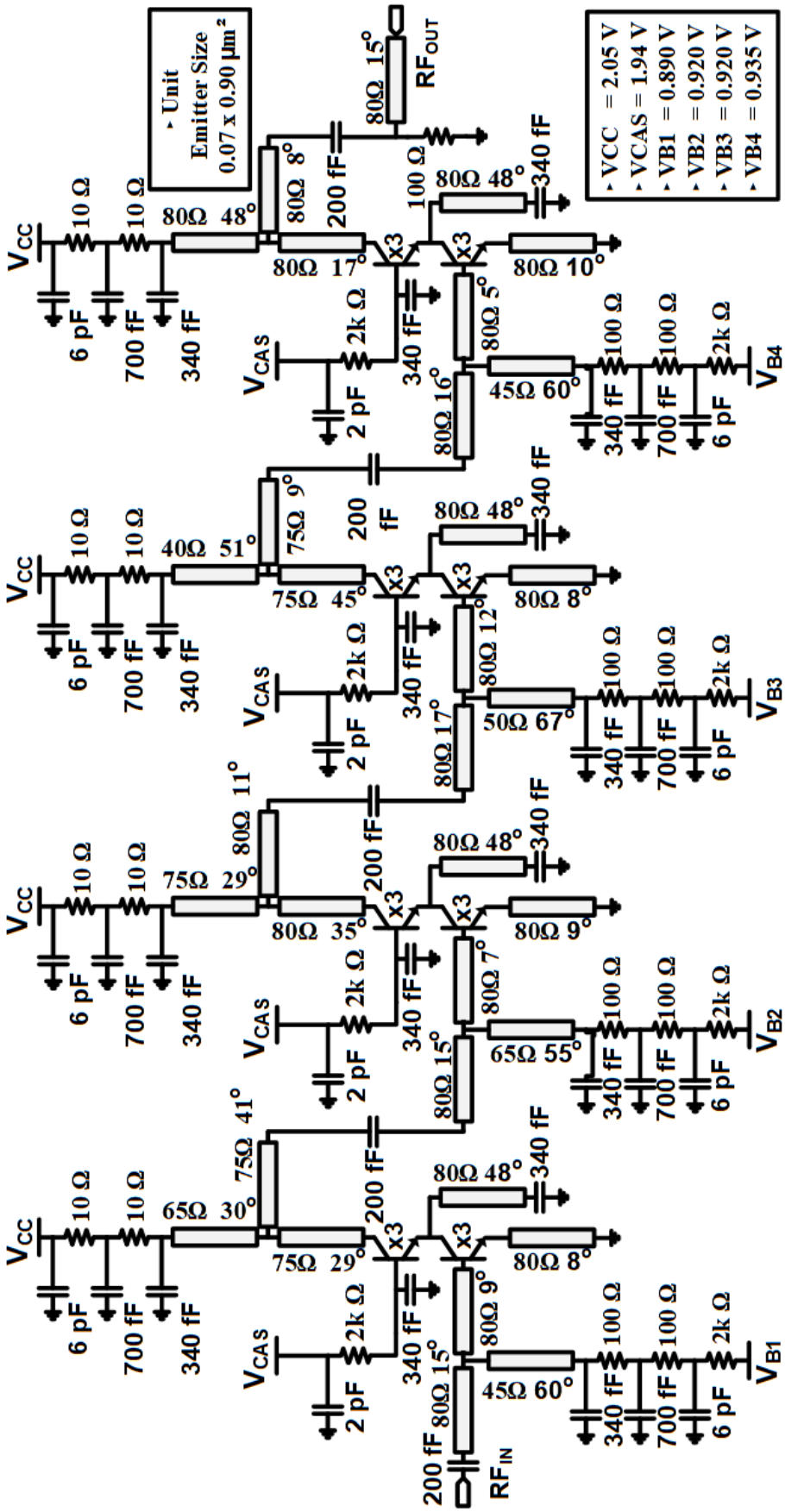

Figure 31 Circuit schematic of the designed D-band LNA (Electrical lengths of the transmission lines are given for 140 GHz).

detector. Assuming a bandwidth of 40 GHz, an integration time of 30 ms, a NEP of 0.8 $pw/Hz^{1/2}$ for the power detector, and an insertion loss of 2.5 dB for the SPDT switch, the dependence of the NETD performance of the Dicke radiometer architecture on the gain and noise figure of the LNA is demonstrated in Figure 32. As could be seen in the Figure 32, the noise figure of the LNA should be as low as possible, and the LNA should have a gain of at least 30 dB to suppress the noise of the power detector enough under aforementioned assumptions. The MATLAB code that was used to figure out the effect of the gain and noise figure of the LNA on the NETD of the radiometer is given in Appendix A.

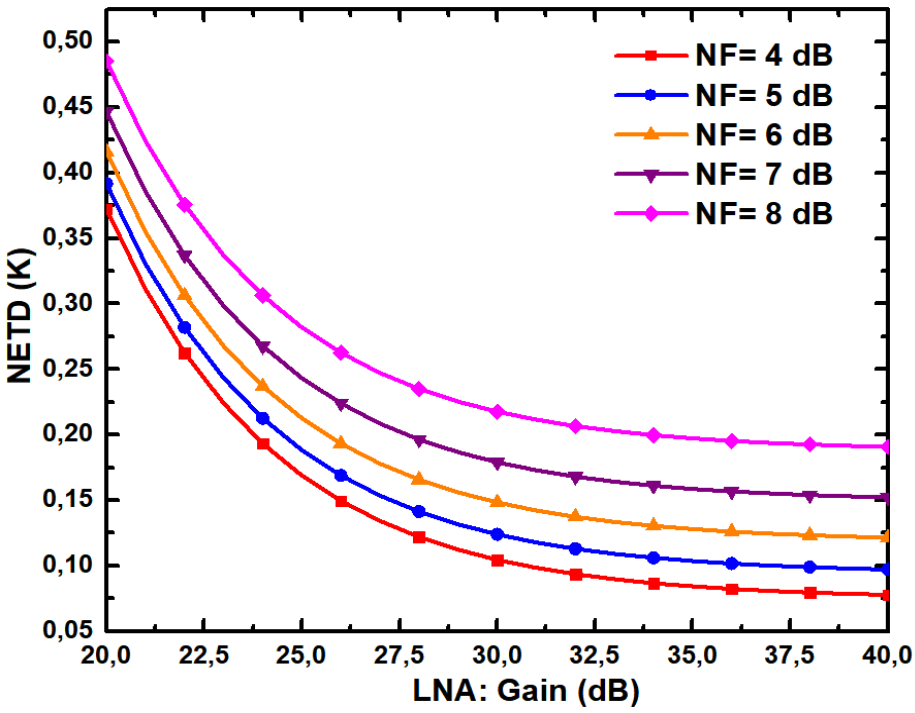

Figure 32 Calculated NETD versus the gain of the LNA for various NF values.

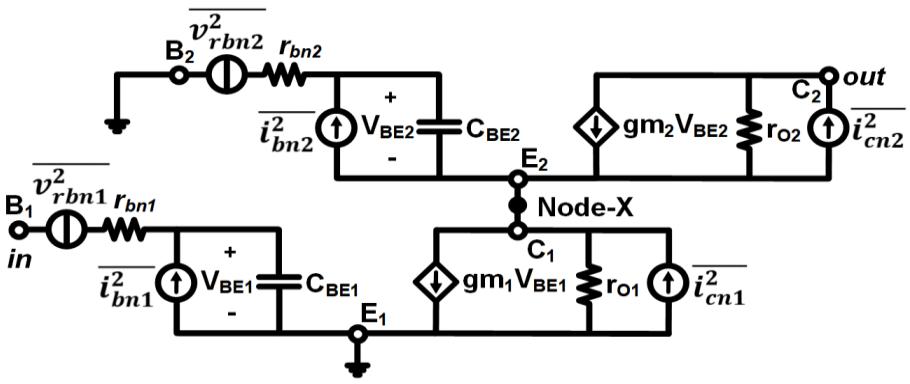

Figure 33 High-frequency small-signal equivalent circuit of the cascode topology including major noise sources.

The CE topology comes out with better noise performance while the cascode configuration comes to the forefront with higher gain performance. The total noise figures of the cascaded two identical stages for both CE and cascode topologies were calculated to figure out which one is appropriate to obtain better noise figure performance, assuming that each stage provides its maximum available gain and minimum noise figure values and they are operating at the optimum bias point for minimum noise figure without trading off too much gain. The result of this calculation is that the gain of the CE is not enough to suppress the following stage. Therefore, it was decided to use the cascode configuration. Ulusoy *et al.* [47] presented a gain-boosting technique to enhance the gain performance of the SiGe HBT cascode configuration operating at D-band. This gain-boosting technique can be used to enhance the gain so that the noise contribution from the following stages can be suppressed better. However, it does not cope with the noise contribution of the CB transistor which leads to trouble in terms of the noise figure, especially for above 100 GHz. In order to figure out how to reduce the noise contribution of the CB transistor, the noise figure of the cascode topology was analyzed including the major noise sources and parasitics in a SiGe HBT.

There are three major noise sources at high-frequencies in a SiGe HBT: the thermal noise of the parasitic base resistance (V_{rbn}), the base shot noise (i_{bn}), and the collector shot noise (i_{cn}). The high-frequency small-signal equivalent circuit of the cascode configuration including the major noise sources is shown in Figure 33. It should be highlighted here that the base-emitter and collector output resistances ($\mathrm{r_{be}}$ and r_o) represent real parts of impedances without having thermal noise and, the collector-base capacitance was omitted for simplification. In Figure 34, $\mathrm{C_x}$ represents all parasitic capacitances between the node-X and the ground such as the collector-emitter and collector-substrate capacitances of the CE transistor, and the base-emitter and emitter-substrate capacitances of the CB transistor.

The method presented in [48] was used to derive the noise factor equation of the cascode topology. The superposition theorem was applied to calculate the total output noise current power spectral density ($\overline{I_{no}^2}/\Delta f$) since the correlation between the presented noise sources could be ignored for simplification. The output noise current power spectral density terms due to each noise source were derived by considering Figure 33 and Figure 34, as presented in equations (35-(41), where k is the Boltzmann constant, T is the

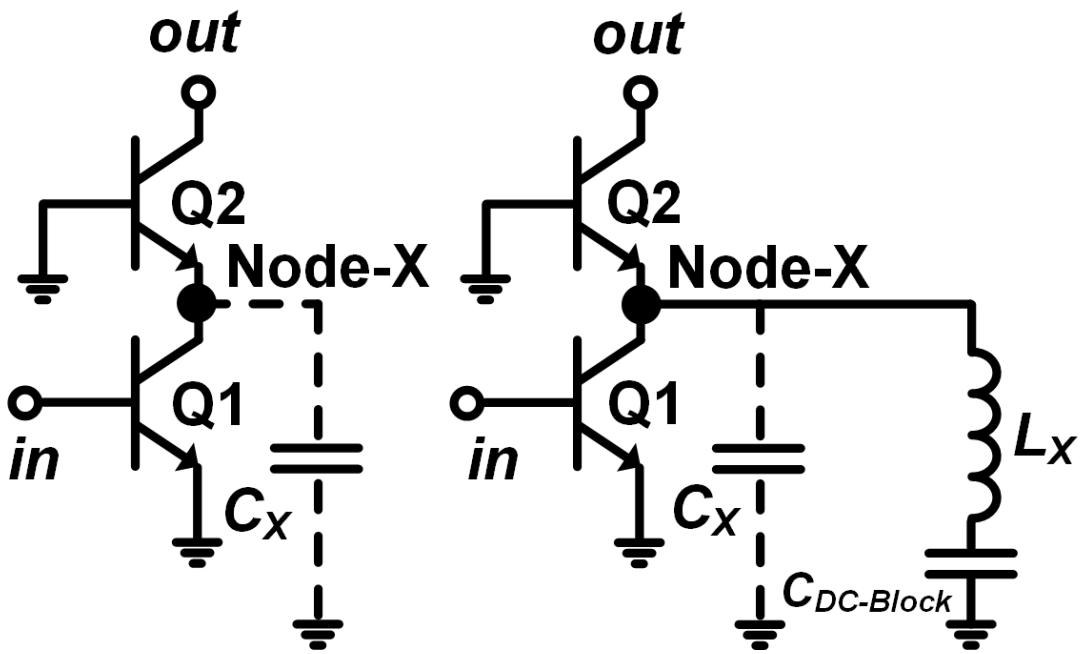

Figure 34 Conventional cascode topology (left) and modified cascode topology with the shunt-inductor L_x (right).

temperature, I_{BQ} is the quiescent base current, I_{CQ} is the quiescent collector current, and R_s is the source resistance. The total output noise current power spectral density ($\overline{I_{no}^2}/\Delta f$) is equal to the sum of all these terms. Consequently, the noise factor equation of the conventional cascode topology (F_a) can be found out by dividing the total output noise current power spectral density ($\overline{I_{no}^2}/\Delta f$) by the output noise current power spectral density due to the source ($\overline{i_{no_{(source)}}^2}/\Delta f$), as presented in equation (42). At this step, the noise factor terms were called like as shown in equation (42) to highlight the parts related with the capacitance C_x in order to focus its effect on the noise factor. $F_{r_{bn1}}, F_{i_{bn1}}, F_{i_{cn1}}, F_{r_{bn2}}, F_{i_{bn2}}$, and $F_{i_{cn2}}$ are the noise factor terms due to the thermal noise voltage of the parasitic base resistances and the shot noise currents of the CE and CB transistor, respectively. As can be seen from equation (42), the noise contribution of the collector shot noise of the CB transistor escalates as frequency increases, and the capacitance C_x has a significant contribution to this undesired effect.

$$\overline{I_{no_{(source)}}^2}/\Delta f \cong 4kTR_S \times \left(\frac{|Z_{\pi 1}|}{|R_s+Z_{\pi 1}|}\right)^2 \times g_{m1}^2 \times \left(\frac{g_{m2}}{\left|g_{m2}+\frac{1}{Z_x}\right|}\right)^2 \quad (35)$$

$$\overline{I_{no_{(rbn1)}}^2}/\Delta f \cong 4kTr_{bn1} \times \left(\frac{|Z_{\pi 1}|}{|R_s+Z_{\pi 1}|}\right)^2 \times g_{m1}^2 \times \left(\frac{g_{m2}}{\left|g_{m2}+\frac{1}{Z_x}\right|}\right)^2 \quad (36)$$

$$\overline{I_{no(Ibn1)}^2}/\Delta f \cong 2qI_{BQ1} \times \left(\frac{R_S}{|R_S+Z_{\pi1}|}\right)^2 \times |Z_{\pi1}|^2 \times g_{m1}^2 \times \left(\frac{g_{m2}}{\left|g_{m2}+\frac{1}{Z_x}\right|}\right)^2 \quad (37)$$

$$\overline{I_{no(Icn1)}^2}/\Delta f \cong 2qI_{CQ} \times \left(\frac{g_{m2}}{\left|g_{m2}+\frac{1}{Z_x}\right|}\right)^2 \quad (38)$$

$$\overline{I_{no(rbn2)}^2}/\Delta f \cong 4kTr_{bn2} \times \left(\frac{|gm_2Z_x|}{|(r_{o1}(1+gm_2Z_x)|}\right)^2 \quad (39)$$

$$\overline{I_{no(Ibn2)}^2}/\Delta f \cong 2qI_{BQ2} \times \left(\frac{|gm_2r_{bn2}Z_x|}{|r_{bn2}+(r_{o1}(1+gm_2Z_x)|}\right)^2 \quad (40)$$

$$\overline{I_{no(Icn2)}^2}/\Delta f \cong 2qI_{CQ} \times \left(\frac{1}{|1+gm_2Z_x|}\right)^2 \quad (41)$$

$$F_a \cong 1 + F_{r_{bn1}} + F_{i_{bn1}} + F_{i_{cn1}} + F_{r_{bn2}} + F_{i_{bn2}} + F_{i_{cn2}}\left(\frac{\omega C_x}{g_{m2}}\right)^2 \quad (42)$$

In order to remove the effect of the capacitance C_x on the noise figure performance, a shunt inductor L_x is placed to parallel to C_x as shown in Figure 4(b). The noise factor equation of the modified topology with the shunt inductor L_x was derived by following the procedure which is presented above for the conventional topology. In this way, the noise factor of the modified topology (F_b) can be expressed by equation (43). As can be seen from equation (43) if the value of the shunt inductor L_x is set to resonate with the capacitance C_x at the operating frequency, the collector shot noise of the CB transistor which is the dominant noise source can be removed completely. Figure 35 compares the simulated maximum stable gain (MSG) and minimum noise figure (NF_{min}) of the conventional and modified cascode topologies (within the typical case). As seen, this noise reduction technique reduces the minimum noise figure ($NFmin$) about 0.5 dB across whole D-band frequency range. However, the maximum stable gain (MSG) remains same for both topologies.

$$\boldsymbol{F_b \cong 1 + F_{r_{bn1}} + F_{i_{bn1}} + F_{i_{cn1}} + F_{r_{bn2}} + F_{i_{bn2}} + F_{i_{cn2}}\left(\frac{1-\omega^2 C_x L_x}{g_{m2}\omega L_x}\right)^2} \quad (43)$$

Another important performance specification that determines the noise equivalent temperature difference performance of the radiometer is the bandwidth. Bi *et al.* [49] used a staggered tuning technique based on Chebyshev distribution at W-band to obtain broad bandwidth and thus to improve the noise equivalent temperature difference of the radiometer. Even though it provides broad bandwidth, it has not flat-gain which is another important performance criterion for the radiometers. The

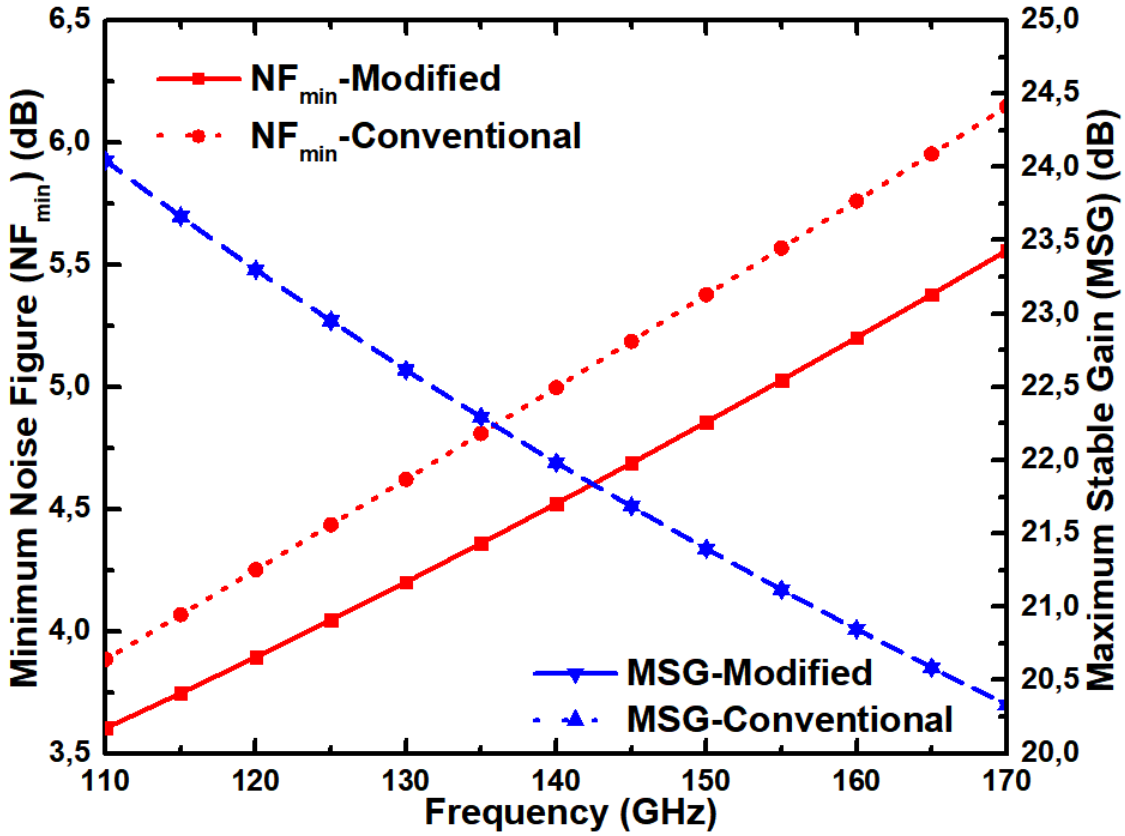

Figure 35 Comparison of the conventional and modified cascode topologies in terms of the minimum noise figure (NF_{min}) and maximum stable gain (MSG).

staggered tuning technique based on Butterworth distribution provides the maximally flat gain response. Therefore, the staggered tuning technique based on Butterworth distribution was employed to obtain broad bandwidth and flat-gain over the frequency of interest in this work.

It is known from the classical filter theory that the number of dominant poles and their relative positions to each other determine the bandwidth and characteristics of the transfer response. In order to have Butterworth distribution, the dominant poles of the transfer function must be on a semicircle with the center at ω_0 on the imaginary axis of s-plane, as depicted in Figure 36. The diameter length of this circle determines the bandwidth of the transfer function in terms of the angular frequency. The dominant pole of a cascode configuration is mainly determined by its output network that determines the gain-peaking frequency and 3-dB bandwidth of the cascode stage [50].

The first three stages were designed by obeying the gain-peaking frequencies and 3-dB bandwidths which are determined by the Butterworth distribution to have a 40 GHz 3-dB bandwidth with a center frequency of 140 GHz in total. The last stage of the low-noise

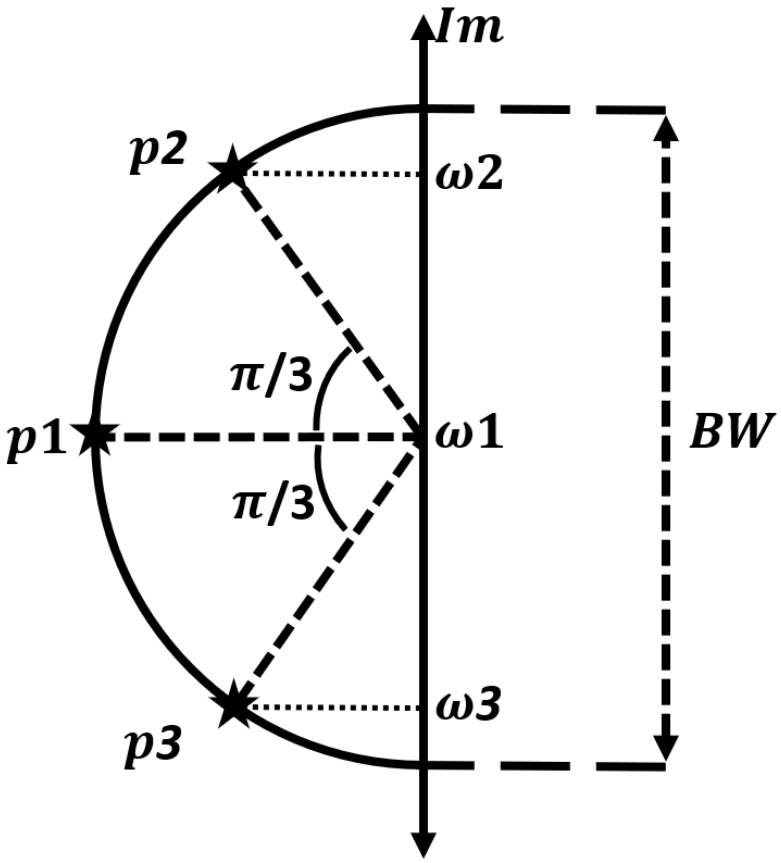

Figure 36 Positions of the poles of Butterworth distribution on the s-plane (for 3-poles).

amplifier was designed to provide wideband output matching without disturbing the Butterworth characteristic as much as possible. According to Figure 36, the gain-peaking frequencies of the staggered tuned stages should be 122.7, 140 and 157.3 GHz, and each stage should have a 3-dB bandwidth of 20 GHz. The gain-peaking frequency of the first stage was set to 140 GHz to have a noise figure as minimum as possible at the center of the frequency range. The gain-peaking frequencies of the second and third stages were optimized to 157.3 and 122.7 GHz, respectively. This order was chosen to avoid a sharp increase in noise figure as frequency increases. If the second stage had been peaked at 122.7 GHz, the total gain of the first two stages would have been not sufficient to suppress the noise of the following stages at the higher frequencies since the noise figure naturally increases with the frequency. Also, the peak-gain of each stage should be the same to each other to not disturb the Butterworth response. Figure 37 shows the simulated gain of each stage and the simulated overall gain.

The collector current of the first stage was optimized to obtain a good compromise between the noise figure (NF) and the maximum available gain (MAG) for the unit emitter size. The emitter area of the CE transistor ($Q1$) was chosen to enable

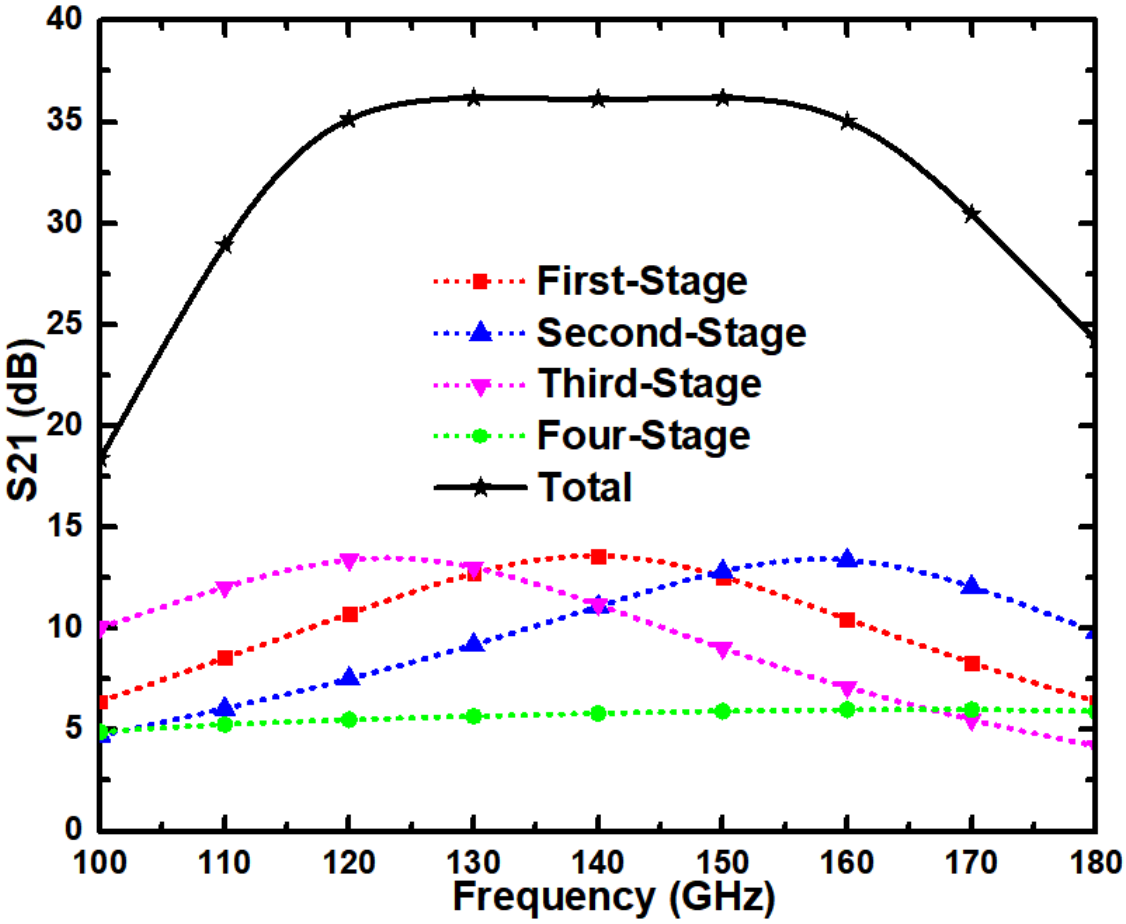

Figure 37 Schematic based simulations of each stage and overall amplifier.

simultaneous input power and noise matching. The inductive emitter degeneration technique was used to keep the peak-gain value same for each stage. If the emitter degeneration had been used to set the real part of the input impedance to 50Ω as in the conventional design approach, it would have resulted in different peak-gains for each stage so that the Butterworth response would have been disturbed. That's why the transmission line based T-type matching network was used to perform the input impedance matching. The electrical lengths and the characteristic impedances of the transmission lines which are used at the output network were set to have peak-gain at 140 GHz with the calculated 3-dB bandwidth for the Butterworth characteristic. The second and third stages were designed in the same way but for different peak-gains, and the collector currents of these stages were increased to allow larger output voltage swing to achieve better linearity performance.

All the transmission lines were implemented as microstrip lines with Top Metal 2 – Metal 1 configuration and all of them were meandered to reduce the chip area. Parasitic capacitances due to the RF-pads were not included in the input and output impedance

matchings. Instead, a TRL de-embedding fixture was used to de-embed the effect of RF-pad and shift the reference plane to the input of the LNA. The MIM capacitors were employed to perform DC-blocking and AC-grounding. The SRF of the 340 fF capacitor which was used at the bias networks to perform AC-grounding is 140 GHz in the used process technology (IHP's SG13G2), and it can just provide an acceptable AC grounding between 100 GHz and 180 GHz. Another bypass capacitor should be placed on the bias line to ground smaller frequencies, but if it is connected in parallel to the first bypass capacitor, their parasitics will be added up, and it would result in unexpected and undesired frequency response. Therefore, small value resistors were placed on the bias lines, between two bypass capacitors as shown in Figure 31, and by this way, these R-C sections on the bias lines help to enhance the low-frequency stability and to improve the insulation between the stages. ADS momentum was used to perform the full-chip electromagnetic (EM) simulations. Figure 38 shows the 3D layout view taken from the electromagnetic simulation setup of the D-band LNA. Isolation walls shown in Figure 38 were employed between the stages to prevent possible unwanted signal leakage between the stages through the SiO_2 layers and the Si-substrate.

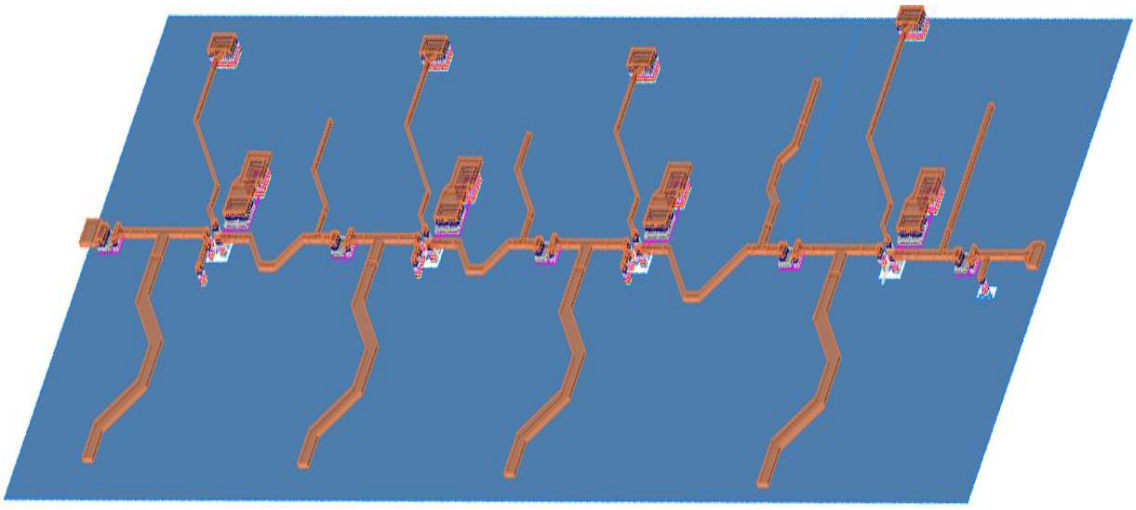

Figure 38 3D layout view taken from EM simulation setup of D-band low noise amplifier.

2.3.2 Simulation and Measurement Results

The chip microphotograph of the designed D-band LNA is shown in Figure 39. The total area of the integrated circuit is 1.0 mm^2 (1.25 mm × 0.8 mm). The effective chip area, excluding the pads and lines placed for de-embedding, is 0.6 mm^2. The total quiescent power consumption is 28 mW.

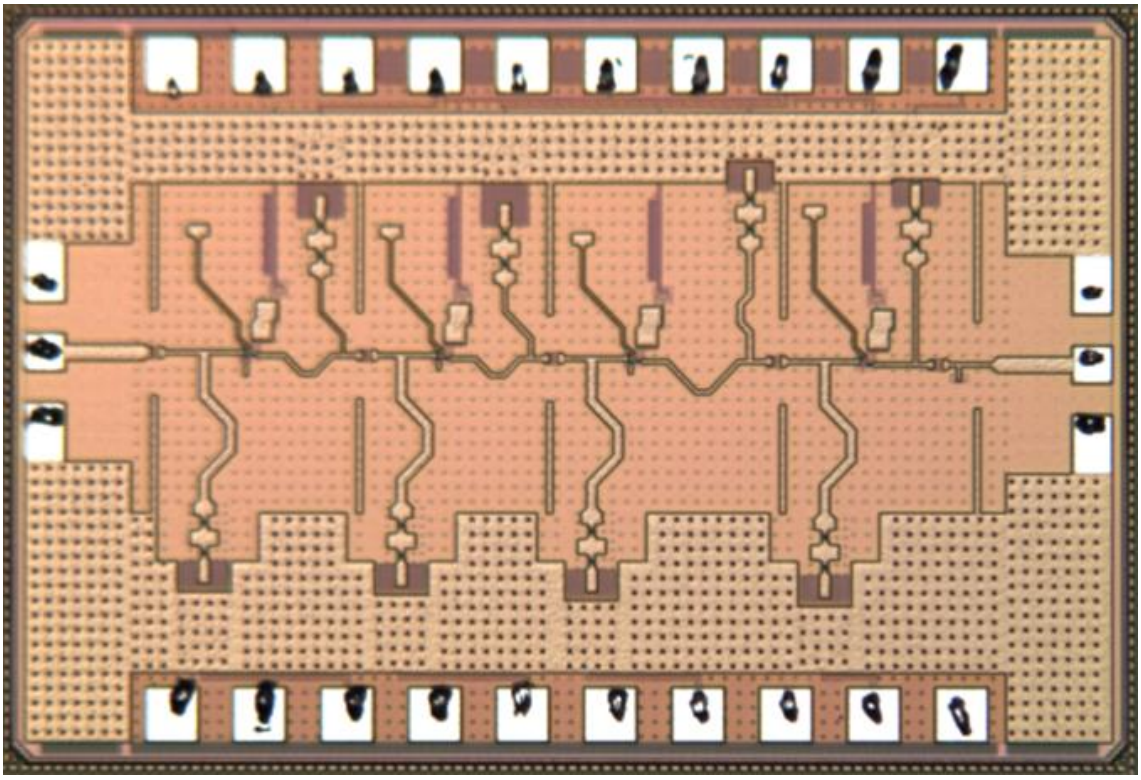

Figure 39 Chip microphotograph of the designed D-band LNA (1.25 mm × 0.8 mm).

S-parameters of the designed D-band LNA were measured by the Keysight N5224A PNA whose frequency extended to 110-170 GHz using VDI WR6.5 frequency extension modules. Two-port SOLT calibration was performed by an ISS from Cascade-Microtech to move the reference plane to the probe tips. The power at the probe tip was set to be less than -40 dBm over the D-band to ensure that the designed low-noise amplifier is operating in the linear region. After that, two-port TRL de-embedding algorithm on Cascade WinCal XE software was performed using the data obtained from on-chip de-embedding structures to remove the parasitic effects of the RF pads. The simulated and measured s-parameter results of the designed low-noise amplifier, including the effects of the RF-pads, is presented in Figure 40. Figure 41shows the de-embedded simulated and measured s-parameters of the low-noise amplifier. As can be seen from Figure 41, there is a quite good agreement between the simulated and measured s-parameter results of the designed D-band low-noise amplifier. The peak gain of the LNA was measured to be 33.1 dB at 147 GHz, and the 3-dB bandwidth of the designed LNA is 42 GHz.

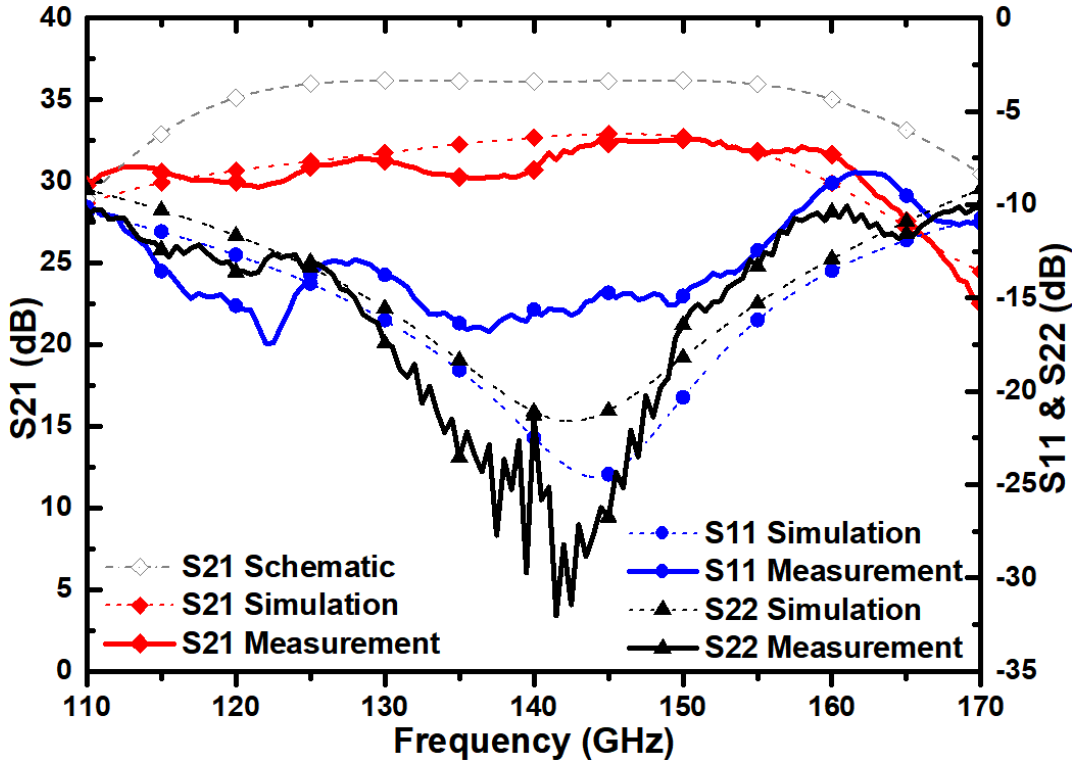

Figure 40 Simulated and measured s-parameter results of the designed LNA, including the effects of the RF-pads.

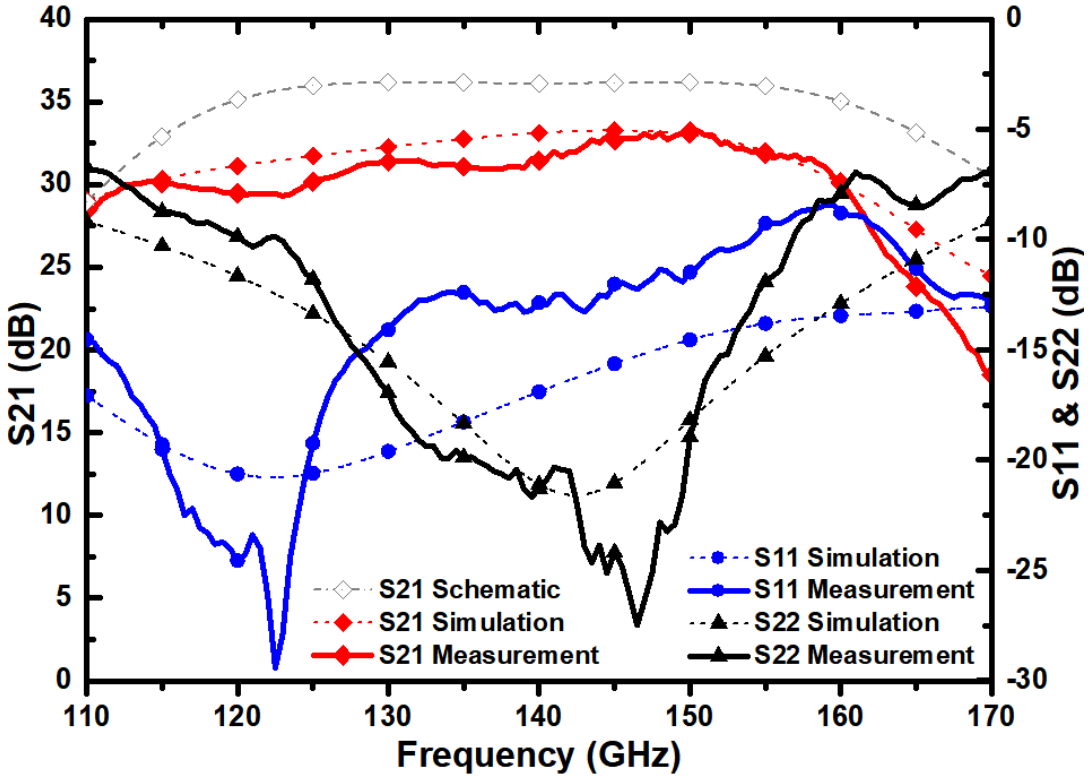

Figure 41 De-embedded simulated and measured s-parameter results of the designed LNA.

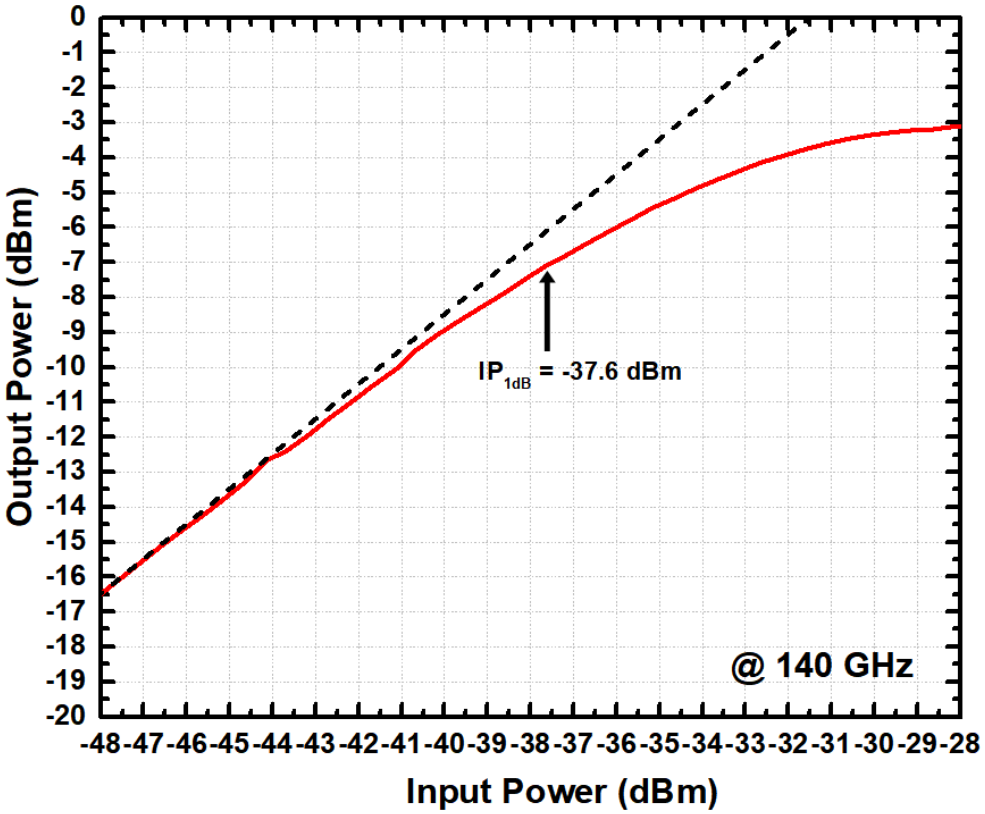

Figure 42 Measured input referred 1-dB compression point of the LNA.

Figure 42 shows the measured 1-dB compression point. The input referred 1-dB compression point (IP_{1dB}) was measured to be -37.6 dBm by applying a 140 GHz single-tone sinusoidal signal to the input of the LNA.

Noise figure measurement of the designed LNA was performed using the experimental test setup shown in Figure 43. As can be seen from the figure, the input of the LNA was driven by a D-band ELVA-1 noise source that has an excess-noise-ratio (ENR) of 12-dB. A D-band faraday isolator was used to avoid the measurement errors that would arise due to the mismatch between the output of the noise source and the input of the LNA. The output signal of the LNA was down-converted to an IF frequency by a D-band direct-down conversion mixer driven by an active multiplication chain configurated with Agilent E8257C signal generator. The IF signal was amplified by an IF LNA, and then analyzed by Agilent 8973A noise figure analyzer. Figure 44 shows the simulated and measured noise figure measurement of the LNA. The extremely low-value points were not included in the fitted curve. The fitted noise figure is better than 6.1 dB along the D-band, and the minimum noise figure value of the LNA is 4.8 dB at 127 GHz.

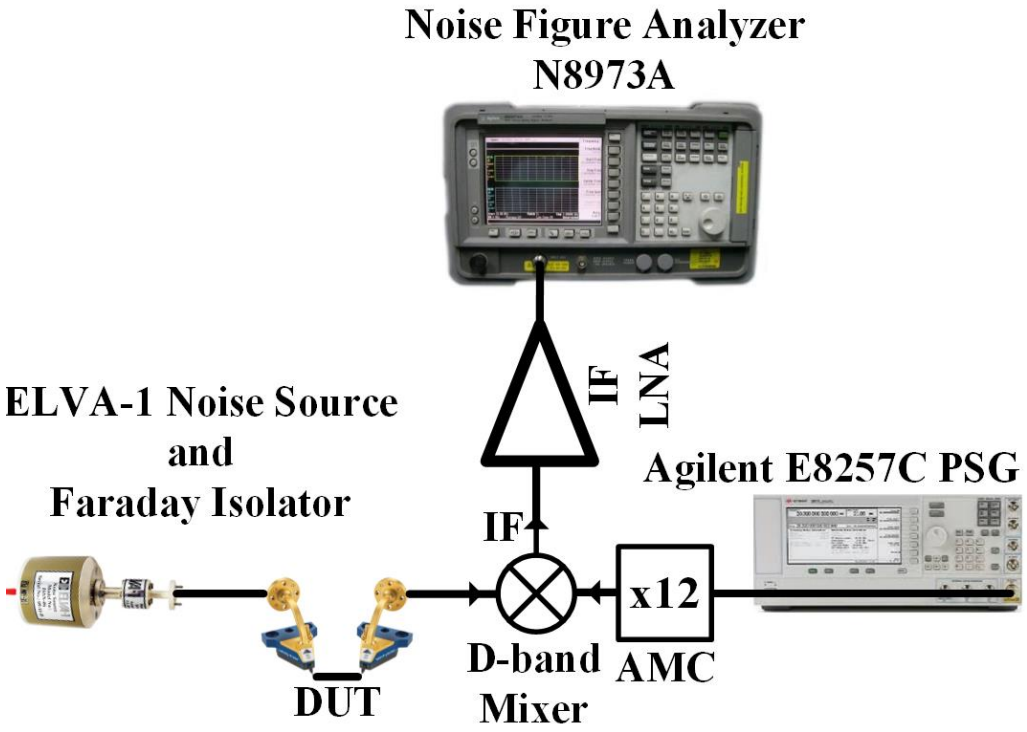

Figure 43 Experimental test setup to measure the noise figure of the LNA.

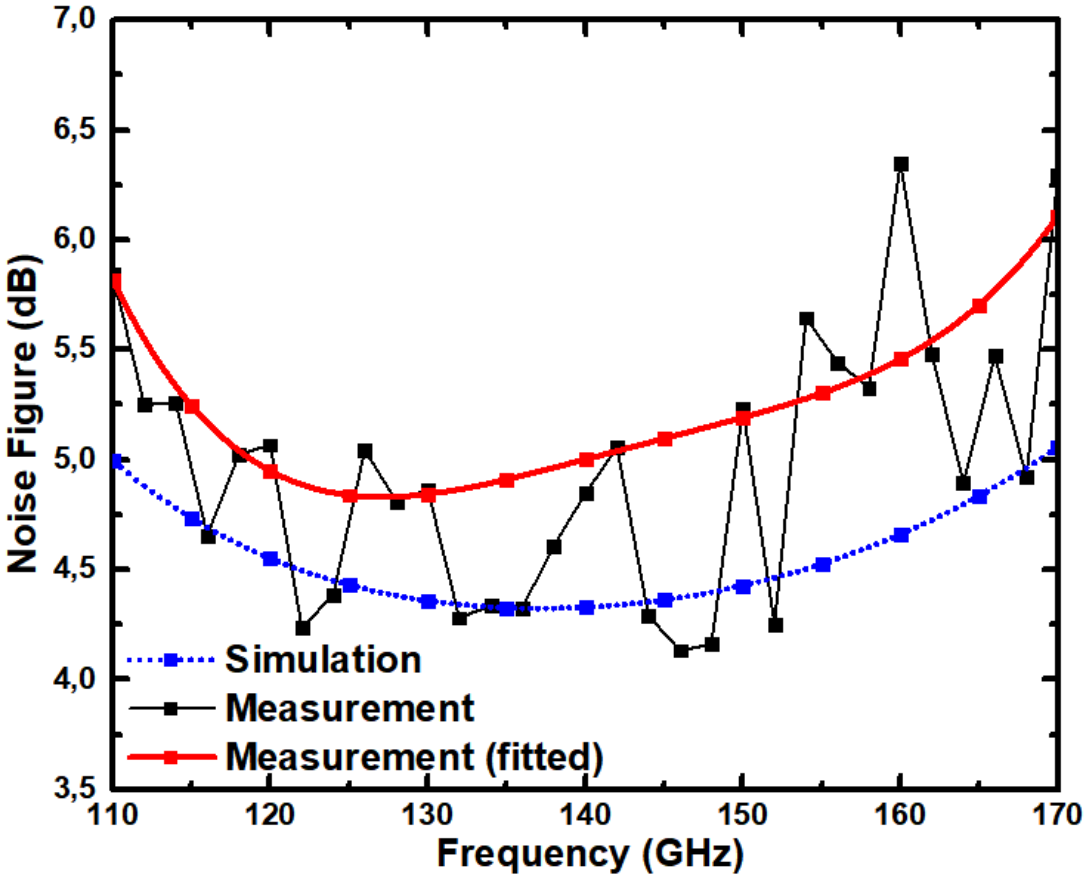

Figure 44 Simulated and measured noise figure performances of the designed LNA.

2.3.3 Comparison

The performance comparison of the designed LNA with reported D-band LNAs implemented in silicon technologies is summarized in Table 4. The figure-of-merit (FoM) described by equation (44) was used to assess the performance of the LNA.

$$FoM = 1000 \times \frac{G \cdot IP_{1dB}[mW] \cdot BW_{3dB}[GHz]}{(F-1) \cdot P_{DC}[mW] \cdot f_{center}(GHz)} \quad (44)$$

The designed LNA achieves the minimum noise figure, and widest 3-dB bandwidth compare to previously reported D-band LNAs implemented in silicon technologies. These results point that the designed D-band LNA shows the state-of-the-art performance, and it is suitable to be employed in millimeter-wave passive imaging systems to achieve excellent noise equivalent temperature difference.

Table 4 Summary of performance comparison of the designed D-band LNA with previously reported D-band LNAs implemented in silicon technologies.

	Tech.	**Peak Gain (dB)**	**Peaking Freq. (GHz)**	**3-dB BW (GHz)**	**NF (dB)**	**IP_{1dB} (dBm)**	**P_{DC} (mW)**	**FoM**
[51]	*65nm* CMOS	13.8	113.7	11.2	10.8	-26.8	40	0.01
[52]	*90nm* SiGe BiCMOS	36	138	5.5	*N/A*	*N/A*	45	--
[43]	*90nm* SiGe BiCMOS	30	140	25	6.2	*N/A*	15	--
[45]	0.13μm SiGe BiCMOS	35	164	8	11	*N/A*	*92*	--
[47]	0.13μm SiGe BiCMOS	27.5	126	18	5.5-6.5	-33	12	1.32
[53]	0.13μm SiGe BiCMOS	24.1	158	40	8.2	-25.9	28	1.07
This Work	0.13μm SiGe BiCMOS	33	147	42	4.8-6.1	-37.6	28	1.78

2.4. SPDT Switch

2.4.1 Circuit Design and Implementation

SPDT switch is one of the important sub-blocks in the Dicke radiometer architecture. Because its insertion loss directly contributes to the overall noise figure of the radiometer since there is no amplification block before the SPDT switch. At millimeter-wave frequencies, the quarter-wave shunt switch topology is commonly preferred to avoid the parasitics of the series devices since these parasitics, especially the parasitic shunt capacitances, become very costly in terms of the insertion loss performance as frequency increases. Furthermore, Schmid *et al.* [54] presented a new mode of operation, which is named as reverse saturation, that improves the switching performance of the HBT.

The circuit schematic of the designed SPDT based on the quarter-wave shunt switch topology is shown in Figure 45. When the V_{cont} is applied, the Q2 is turned "on" and the Q1 is turned "off". Thus, the Q2 provides a low impedance ($R_{on-state}$ and $C_{on-state}$), and the quarter-wave ($\lambda/4$) transmission line transforms this approximate short-circuit to an open-circuit. In the meantime, Q1 acts as an open-circuit because of the very high off-state impedance ($R_{off-state}$ and $C_{off-state}$). In this way, the RF Power at the wanted input is directed to the output. It should be highlighted here that the length of the transmission line could be smaller than the quarter-wave length to compensate the non-ideal short-circuit provided by the on-state-HBT. In addition, an inductive shunt stub is placed parallel to HBT device to improve the insertion loss performance by resonating the off-state capacitance ($C_{off-state}$) at the center of the frequency range of interest. Thence, the dominant term is the off-state resistance ($R_{off-state}$), which determines the insertion loss of the SPDT. Besides, the inductive shunt stub provides the DC-ground for the collector of the HBT, and also contributes to input impedance matching.

The size of the HBT is the main parameter that determines the insertion loss and isolation performances of the SPDT. The use of smaller HBT device enables to provide higher off-state resistance ($R_{off-state}$) which provides better insertion loss performance. However, smaller device inherently brings higher on-state resistance ($R_{on-state}$) which reduces the isolation performance of the SPDT. Therefore, there is a trade-off between the insertion loss and isolation performances of the SPDT, due to the size of the HBT. Consequently, the main challenge in the SPDT design using the quarter-wave shunt switch topology is finding out the optimum device size. The main approach should be to

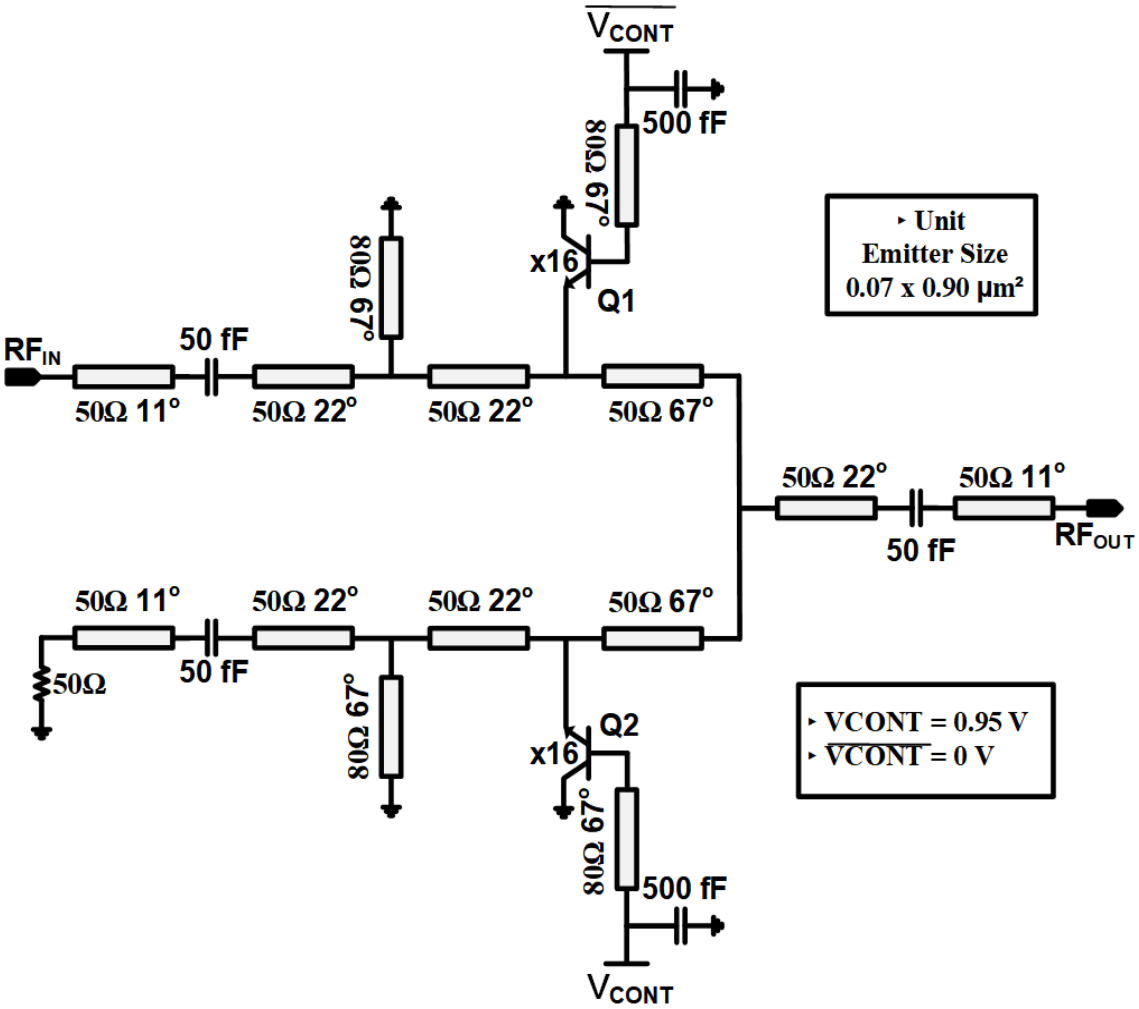

Figure 45 Circuit schematic of the designed D-band SPDT switch (Electrical lengths of the transmission lines are given for 140 GHz).

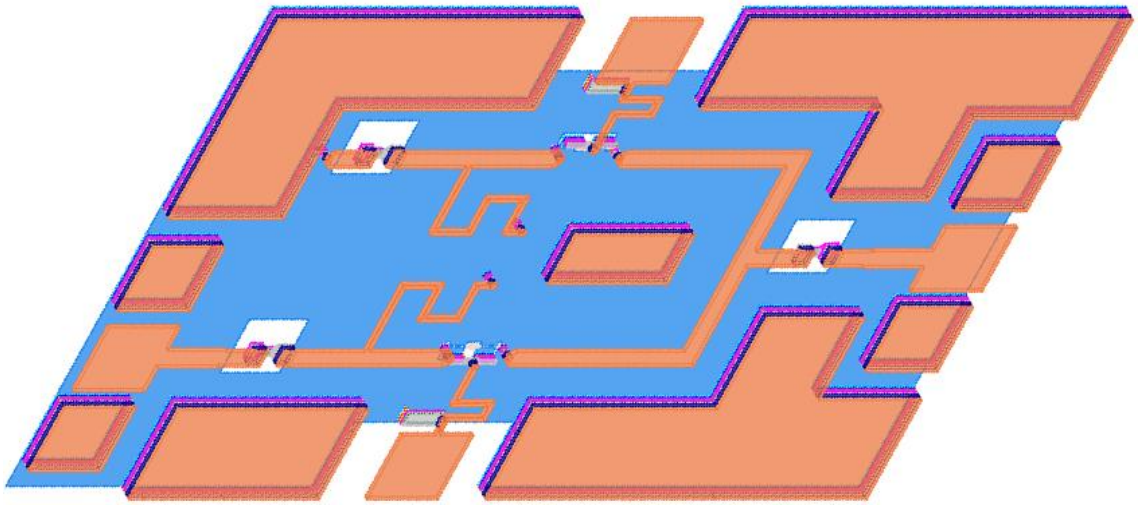

Figure 46 3D layout view taken from EM simulation setup of D-band SPDT switch.

find a way that increases the off-state resistance ($R_{off-state}$) without increasing the on-state resistance ($R_{on-state}$) to break this trade-off. There are three different ways to use

an HBT as an electrical switch: diode-connected, forward-saturation mode, and reverse-saturation mode. Ulusoy *et al.* [55] have shown that the HBT operating in forward-saturation mode achieves superior performance compare to the diode-connected (base and collector terminals connected) HBT. Because the parasitic capacitances, C_{CB} and C_{CE}, are parallel connected in the diode-configuration while they are series connected in the forward-saturation mode. Furthermore, Schmid *et* al. [56] have revealed that for a same on-state resistance ($R_{on-state}$) value, the HBT configurated in the reverse-saturation mode provides a very higher (about eight times larger) off-state resistance ($R_{off-state}$) than the forward-saturated HBT. This improvement enables to build SPDTs that have lower insertion loss but also higher isolation performance, by breaking the trade-off between the insertion loss and isolation performances.

After all aforementioned design guidelines had been taken into account and evaluated, the HBTs were configurated in the reverse-saturation mode, and the emitter size of the transistor was chosen to be 16x unit. The transmission line based T-type matching network was used to perform the impedance matching between at the input of the SPDT switch. All the transmission lines were implemented as microstrip lines using Top Metal 2 – Metal 1 configuration, and they were meandered to reduce the area. The DC-blocking capacitors were implemented by the MIM capacitor of 50 fF. It contributes to the input impedance matching slightly, as well. Parasitic shunt capacitances due to the RF pads were not taken into account. Instead of this, a Through-Reflect-Line (TRL) de-embedding fixture was utilized to de-embed the effect of RF-pad and to shift the reference plane. The self-resonated bypass capacitors of 500 fF were placed on the bias lines to provide an AC-grounding as well as possible. Full-chip electromagnetic (EM) simulations were performed by ADS Momentum. The 3D layout view taken from the electromagnetic simulation setup of the D-band SPDT switch is shown in Figure 46.

2.4.2 Simulation and Measurement Results

The die microphotograph of the designed SPDT switch is shown in Figure 47. The effective chip area excluding the pads and de-embedding lines is 0.16 mm^2. The overall integrated circuit occupies an area of 0.33 mm^2. The total quiescent power consumption is 5.3 mW.

S-parameters of the SPDT switch were measured by Rohde&Schwarz ZVA24 vector network analyzer whose frequency extended to 110-170 GHz using Rohde&Schwarz

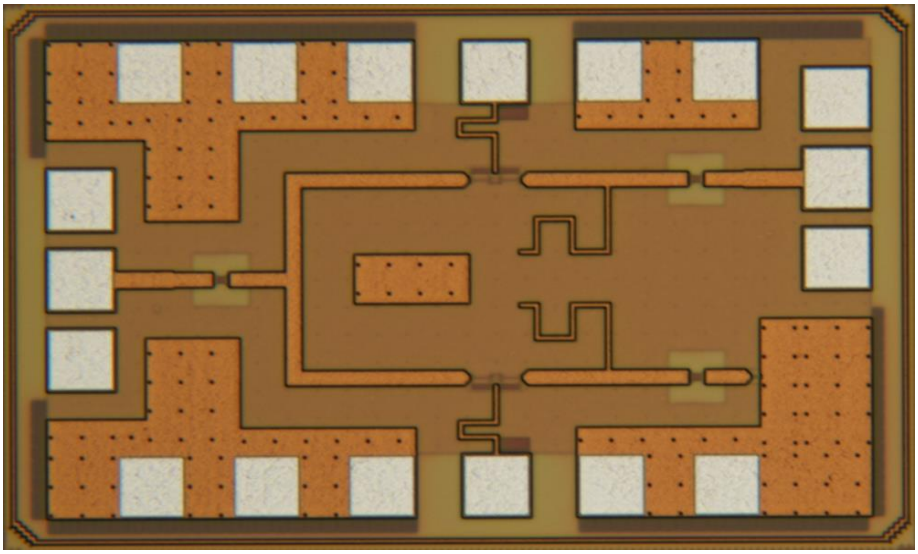

Figure 47 Die microphotograph of the designed SPDT switch (0.46 mm × 0.71 mmm).

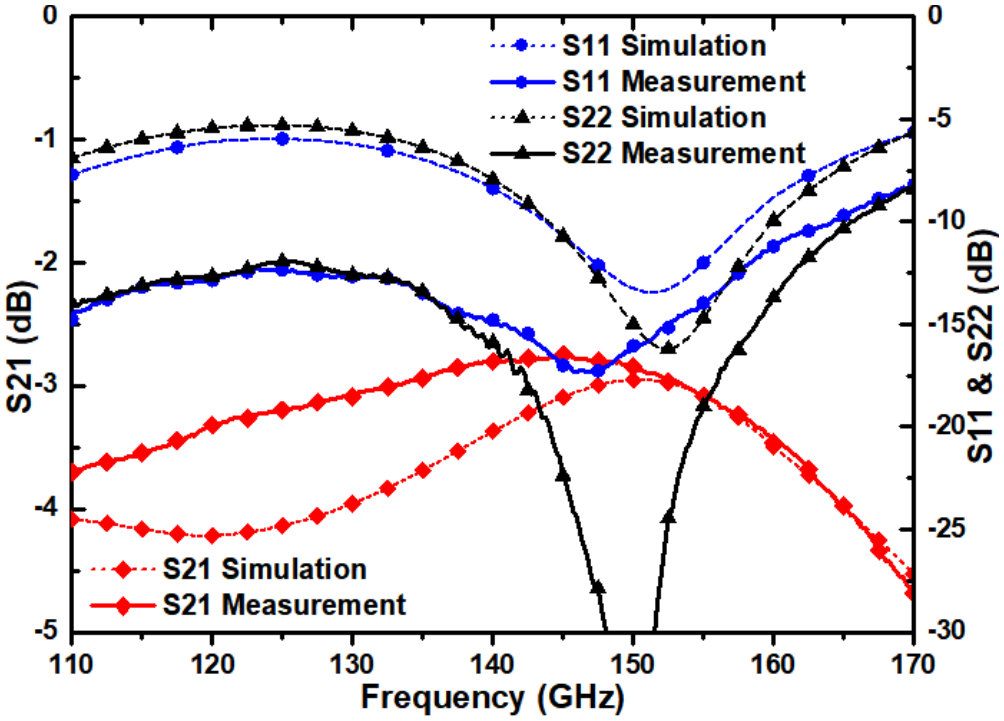

Figure 48 Simulated and measured s-parameter results of the designed SPDT switch, including the effects of the RF-pads (except isolation performance).

ZC170 frequency extension modules. Two-port line-reflect-reflect-match (LRRM) calibration was performed using ISS 138-356 from Cascade-Microtech to move the reference plane to the probe tip. The power at the probe tip was set to be less than -30 dBm along the D-band to guarantee that the SPDT switch is not compressed. Then, two-port thru-open-load (TRL) de-embedding algorithm on Cascade WinCal XE software was run using the measurement data obtained from on-chip de-embedding structures to

remove the parasitic effects of the RF pads. Figure 48 shows the simulated and measured s-parameters of the designed SPDT switch, including the effects of the RF-pads. The de-embedded simulated and measured s-parameters of the designed SPDT switch are presented in Figure 49. As can be observed from the results, there is a little discrepancy between the simulations and measurements. This discrepancy can be attributed to that the simulation program does not solve the full-chip layout of the designed SPDT accurately. The input and output return losses of the SPDT switch are better than approximately 10 dB over the D-band. The de-embedded insertion loss result is better than 4 dB along the D-band, and its minimum value is about 2.6 dB at 125 GHz. Figure 50 shows the simulated and measured isolation results of the SPDT switch, with and without RF-pads. The de-embedded measurement isolation value is better than 25 dB across the entire D-band, and its maximum value is 30 dB.

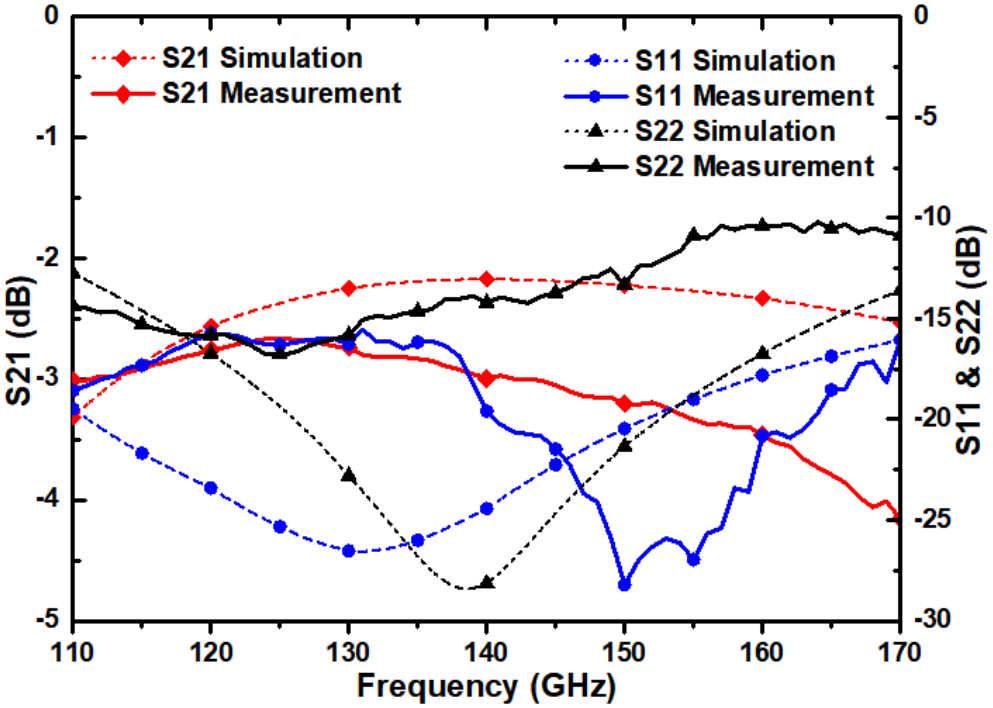

Figure 49 De-embedded simulated and measured s-parameter results of the designed SPDT switch (except isolation performance).

2.4.3 Comparison

The performance comparison of the SPDT switch with previously reported D-band SPDT switches implemented in silicon technologies is summarized in Table 5. The designed SPDT switch shows the minimum insertion loss performance with the highest isolation compared to the other studies implemented in silicon technologies. These results promise

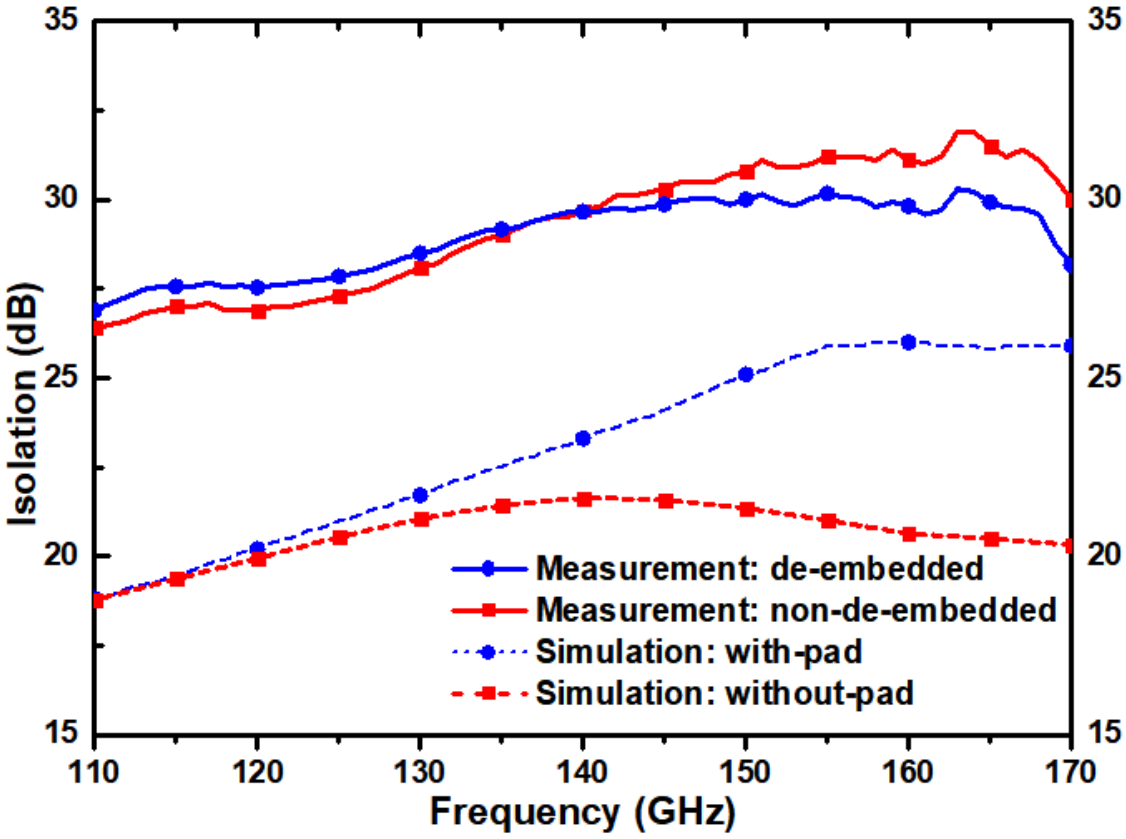

Figure 50 Simulated and measured isolation results of the designed SPDT switch.

a state-of-the-art operation, and the designed SPDT switch is adequate to be used in millimeter-wave radiometer applications to accomplish a superior noise equivalent temperature difference performance.

Table 5 Summary of performance comparison of the designed D-band SPDT switch with previously reported D-band SPDT switches implemented in silicon technologies.

	Technology	**Topology**	**Insertion Loss (dB)**	**Isolation (dB)**	**P_{DC} (mW)**	**Area (mm^2)**
[57]	*32nm* CMOS SOI	Single-shunt	2.6	22	0	0.21
[58]	*65nm* CMOS	Magnetically Switchable Artificial Resonator	3.3	23.7	0	0.004*
[55]	0.13μm SiGe BiCMOS	Double-shunt Saturated HBTs	2.6	29	6	0.36
This Work	**0.13μm SiGe BiCMOS**	**Reverse-saturated Shunt HBTs**	**2.6**	**30**	**5.3**	**0.16***

* Excluding the pads

2.5. Total Power and Dicke Radiometers

2.5.1 Implementation

The advantages and disadvantages of the direct detection radiometer architectures are discussed in Section 2.1.2. Within the scope of this thesis study, the direct detection architectures were used to build the total power and Dicke radiometers. As presented in Section 2.1.2, a typical total power radiometer consists of an LNA to amplify the weak signal collected by the antenna, and a power detector to convert the RF power information to DC-voltage. The noise equivalent temperature difference (NETD) performance of the total power radiometer is significantly degenerated by the gain-fluctuation of the LNA. The effect of the gain-fluctuation of the LNA on the noise equivalent temperature difference (NETD) of the radiometer can be eliminated by using the Dicke switch. Therefore, a typical Dicke radiometer includes an SPDT switch before the LNA in addition to the total power radiometer topology. The performances of the presented sub-blocks such as SPDT switch, LNA, and power detector were found to be suitable to build radiometer systems. The layout view of the implemented Total Power and Dicke radiometers are shown in Figure 51 and Figure 52, respectively. No impedance matching network was used between these sub-blocks because all of them were designed to match 50Ω. All sub-blocks were placed as close together as possible to keep the insertion losses due to the interconnection transmission lines as minimum as possible. In this way, the loading effects of the sub-blocks on each other were kept minimum for both of the radiometer systems.

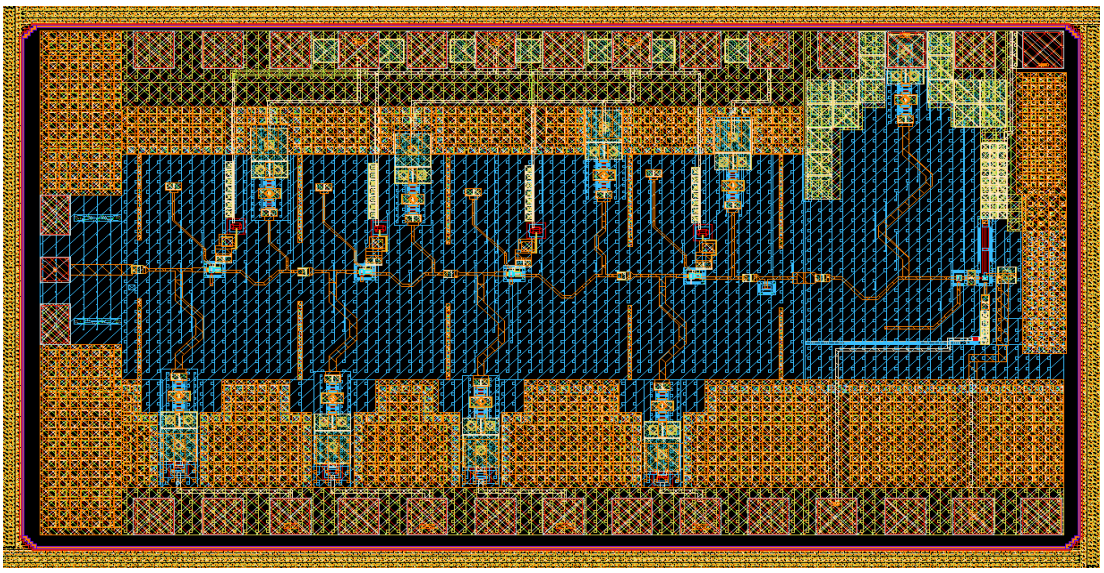

Figure 51 2D layout view of the D-band Total Power Radiometer.

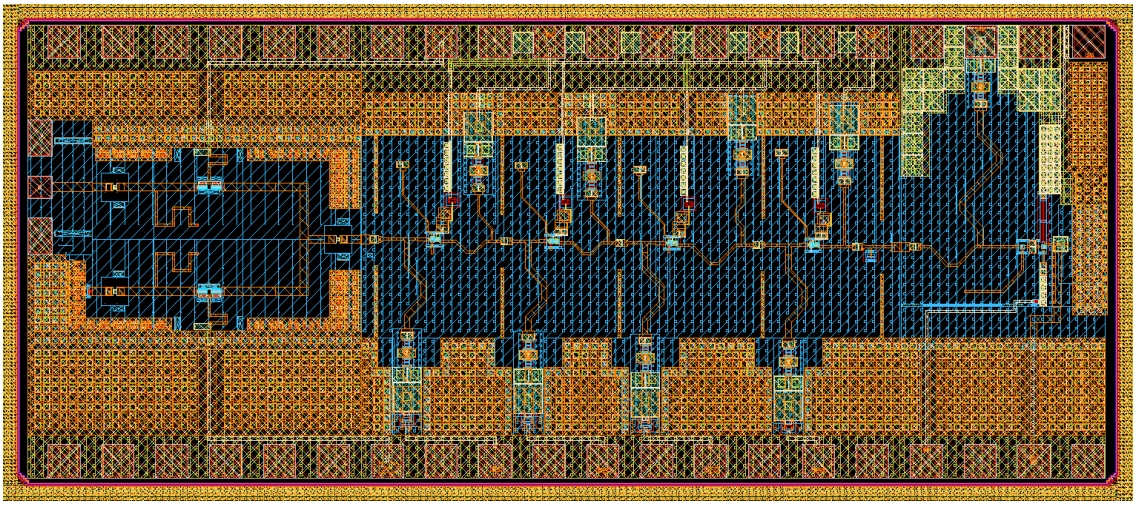

Figure 52 2D layout view of the D-band Dicke Radiometer.

2.5.2 Measurement Results

The chip photos of the total power and Dicke radiometers are shown in Figure 53 and Figure 54, respectively. The total chip area of the total power radiometer is 1.3 mm^2 (1.55 mm × 0.84 mm), and the Dicke radiometer occupies a chip area of 1.7 mm^2 (2.04 mm × 0.84 mm). The total quiescent power consumption of the total power radiometer is 28.53 mW. The Dicke radiometer consumes a DC power of 33.82 mW in quiescent operation. One-port s-parameter measurements of the total power and Dicke radiometers were performed by Keysight N5224A PNA whose frequency extended to D-band using a Virginia Diodes Inc. (VDI) WR6.5 frequency extension module. One port short-open-load (SOL) calibration was done by an ISS from Cascade-Microtech to move the reference plane to the end of the probe. Figure 55 shows the measured input return losses of the total power and Dicke radiometers. The input return loss of the total power radiometer is better than 10 dB over the frequency range of 111 to 158 GHz and better than 8.4 dB across the entire D-band. The input return loss of the Dicke radiometer is better than 10 dB from 110 to 153 GHz and better than 7.5 dB along the D-band.

The experimental test setup shown in Figure 25 was used to measure the 1/f flicker noise of the total power and Dicke radiometers. The input ports of the radiometers were connected to a WR6.5 waveguide 50Ω termination. The external low-noise pre-amplifier (SR-550) was used to amplify the output noise voltage signals of the radiometers. The amplified signals were then measured by Keysight 35670A dynamic signal analyzer operating between 1 Hz and 10 KHz. Later, the gain of the pre-amplifier was subtracted from the measurements.

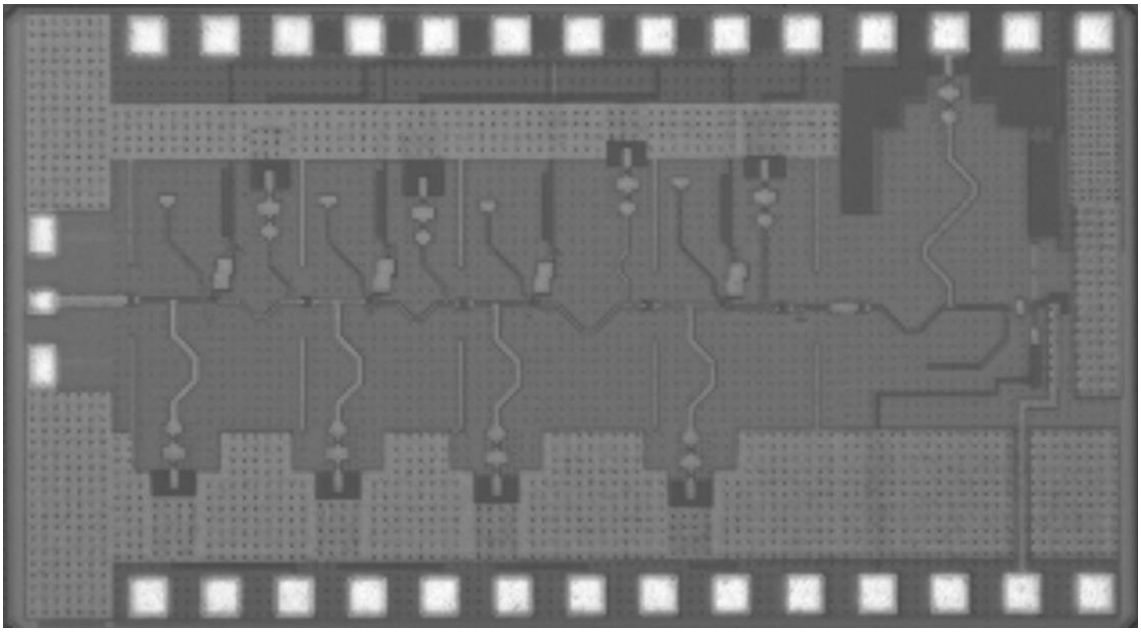

Figure 53 Chip micrograph of the total power radiometer (1.55 mm × 0.84 mm).

Figure 56 shows the measured low-frequency output noise voltage spectral density of the radiometers. The output noise voltage spectral density of the total power radiometer is almost constant (6.6 $\mu V/\sqrt{Hz}$) above 1 kHz which can be also considered as the $1/f$ corner frequency of the total power radiometer. On the other hand, the output noise voltage spectral density of the Dicke radiometer remains approximately constant (6.4 $\mu V/\sqrt{Hz}$) after 1 kHz which can be also considered as the $1/f$ corner frequency of the Dicke radiometer. As mentioned earlier, the Dicke switching frequency should be set to be far away from 2 kHz. Therefore, the output noise voltage spectral density (S_{vo}) was taken as 6.4 $\mu V/\sqrt{Hz}$ in the noise equivalent power (NEP) calculations of the radiometer.

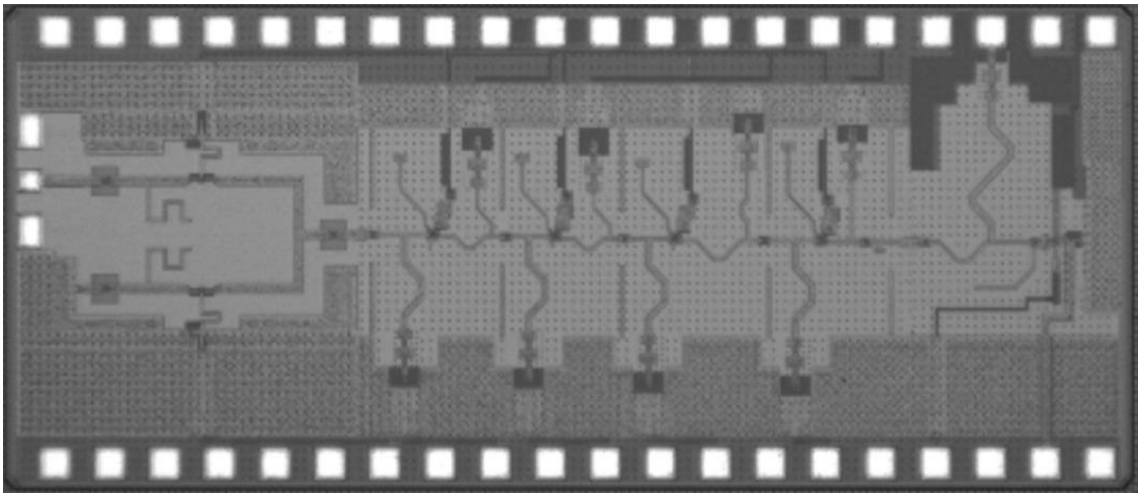

Figure 54 Chip micrograph of the Dicke radiometer (2.04 mm × 0.84 mm).

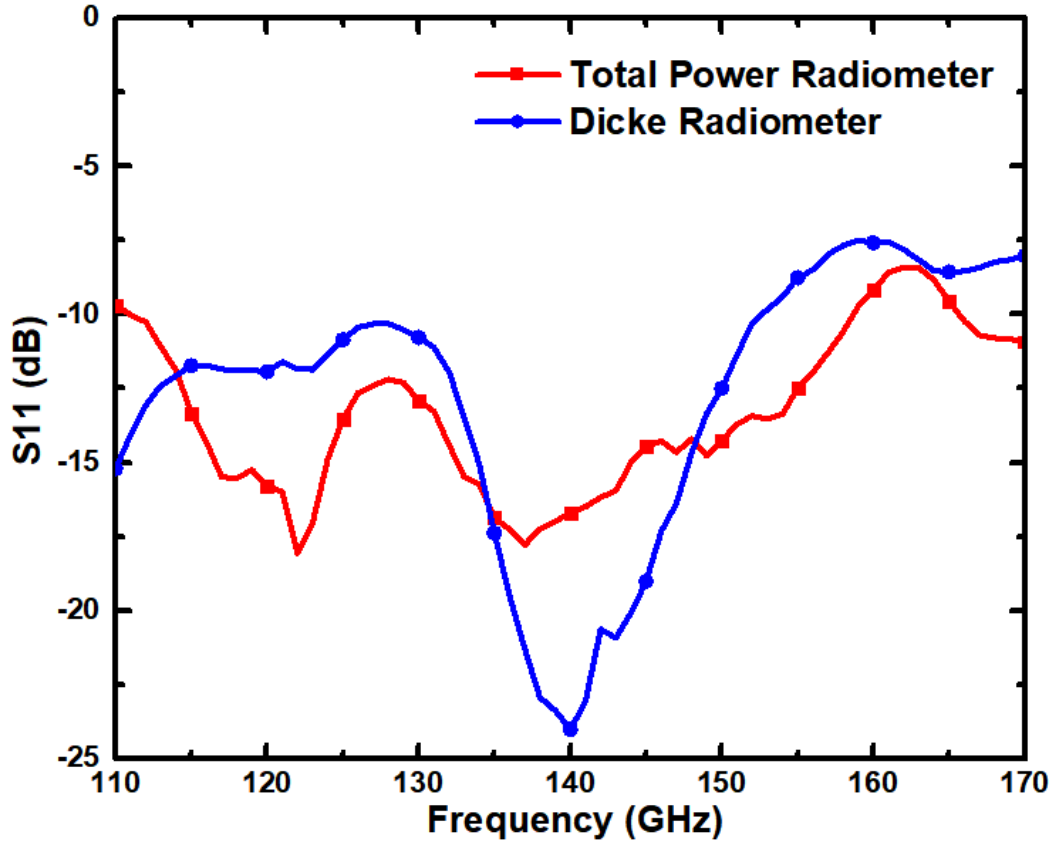

Figure 55 Measured input return losses of the radiometers.

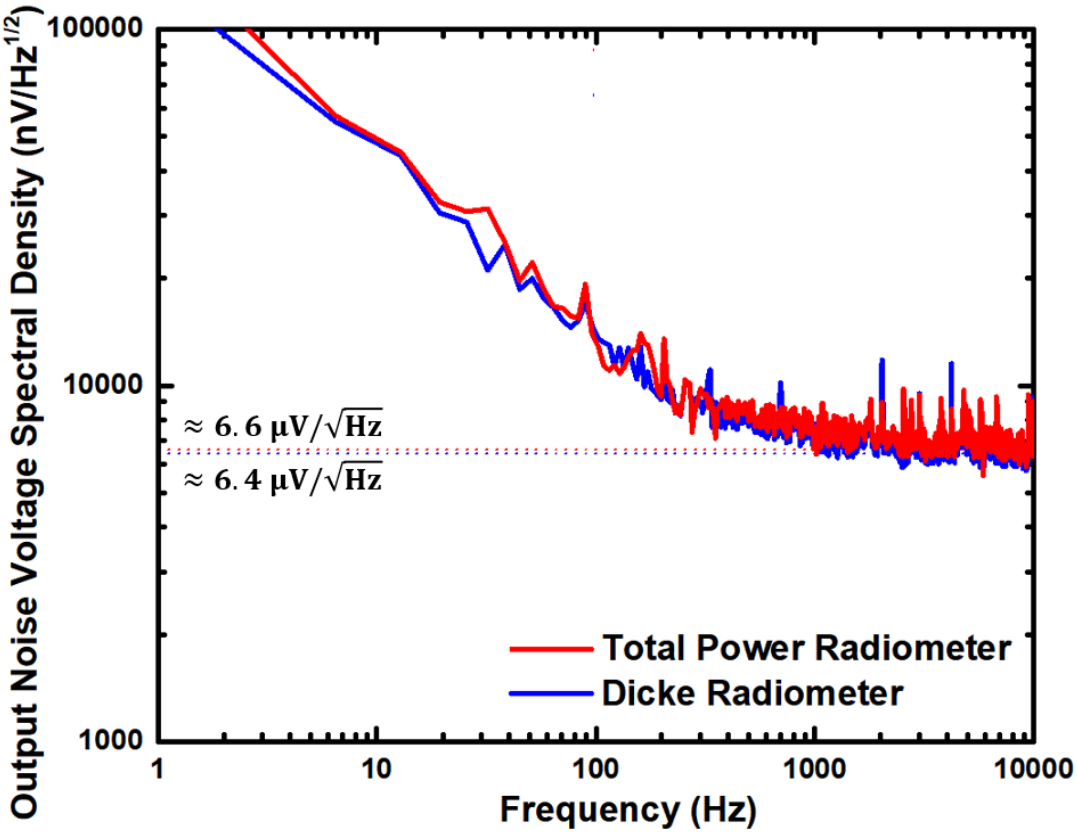

Figure 56 Measured $1/f$ flicker noise of the radiometers.

The experimental test setup shown in Figure 27 was used to measure the responsivities of the radiometers. The power calibration and measurement procedures presented in Section 2.2 was followed in the same way to figure out the responsivity performances of the radiometers. However, the maximum input power was set to -66 dBm and -62 dBm for the total power radiometer and the Dicke radiometer, respectively, to ensure that they are operating in the square-law region. Figure 57 shows the measured responsivity performances of the radiometers. The peak responsivity value of the total power radiometer was measured to be about 1377 MV/W at 130 GHz, and it is higher than 750 MV/W over the frequency range of 110 to 155 GHz. Therewithal, the peak responsivity of the Dicke radiometer is 688 MV/W at 130 GHz, and it is minimum value is about 82.6 MV/W at 170 GHz. As can be observed from the figure, the difference between these two curves is about 3 dB at the center of the frequency range of interest, and it is almost 3.8 dB at the end of the D-band. This difference can be attributed to the insertion loss of the SPDT switch. The observed difference is between the raw and de-embedded insertion loss performances of the SPDT switch. This is already expected because one of the RF-pads is included into the responsivity measurement of the Dicke radiometer.

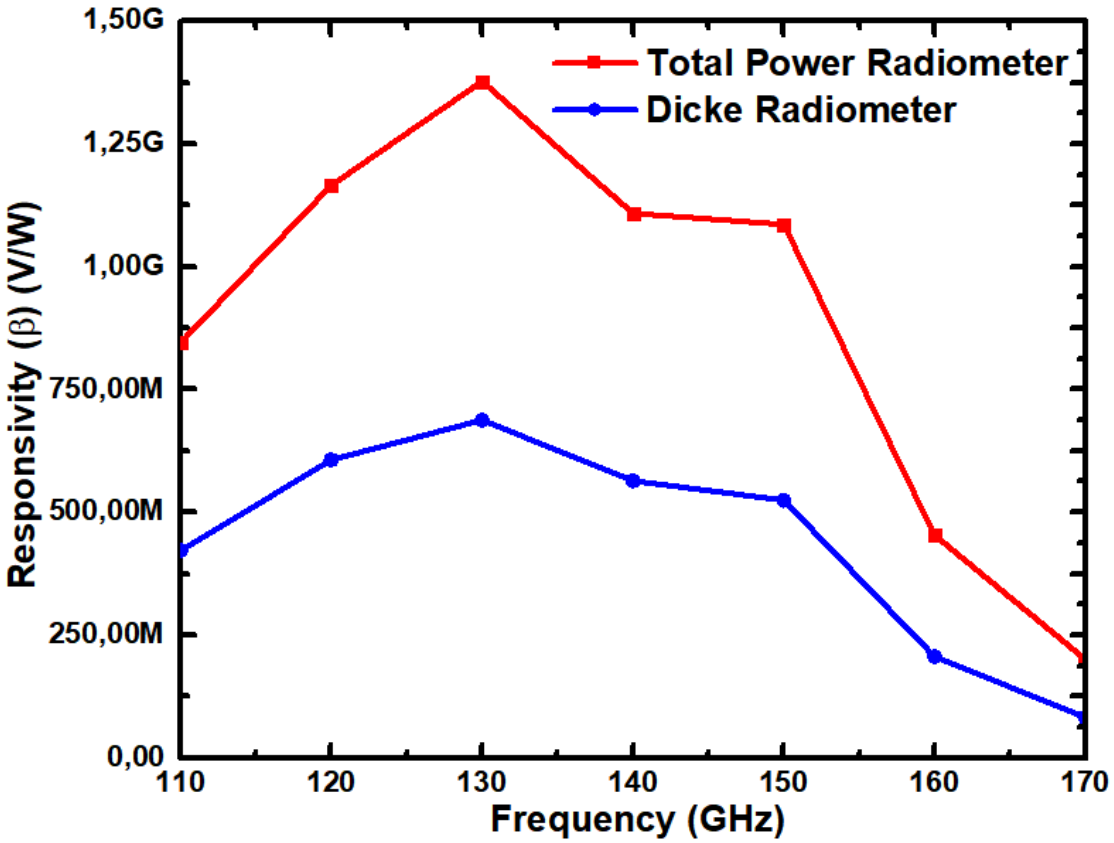

Figure 57 Measured responsivities of the total power and Dicke radiometers.

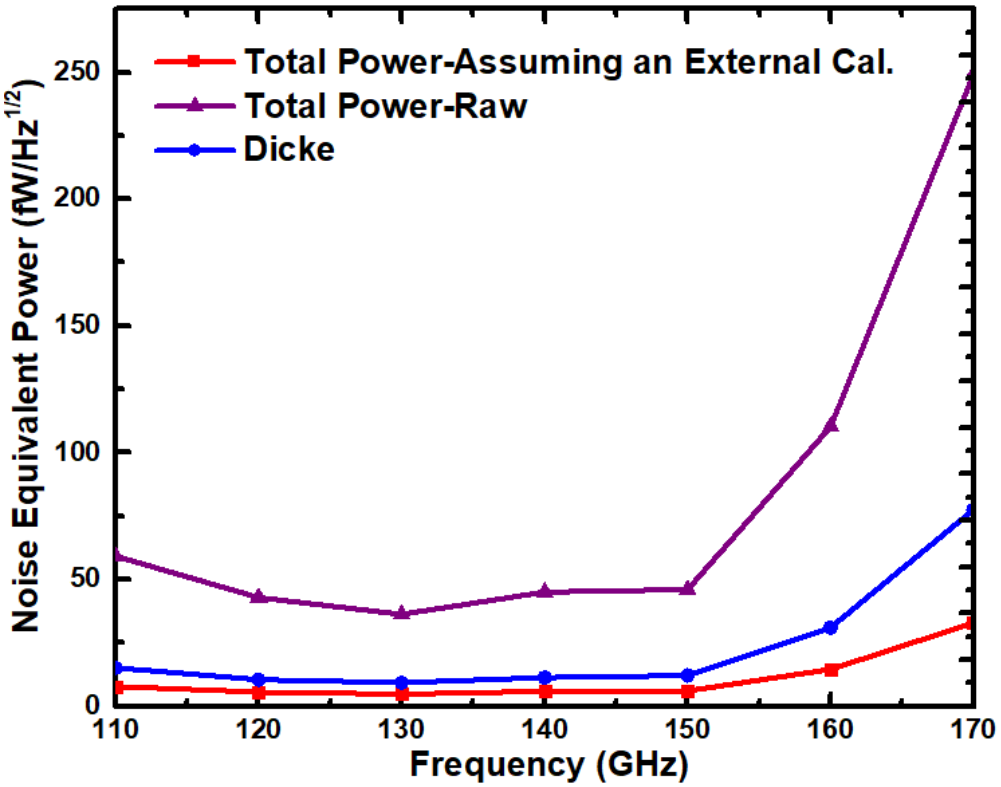

Figure 58 Measured NEP of the total power and Dicke radiometers.

The measured noise equivalent power performances of the radiometers are illustrated in Figure 58. Assuming an external calibration technique that completely eliminate the effect of the gain-fluctuation, the NEP of the total power radiometer is better than 10 $fW/Hz^{1/2}$ from 110 to 155 GHz, and it is much less than 30 $fW/Hz^{1/2}$ along the entire D-band. Its minimum value was found to be about 4.8 $fW/Hz^{1/2}$ at 130 GHz. In addition, the NEP of the total power radiometer was determined including the effect of the gain-fluctuation which arises due to the 1/f noise. In this case, the NEP of the total power radiometer is higher than 36 $fW/Hz^{1/2}$ over the W-band. On the other hand, the noise equivalent power of the Dicke radiometer remains below 20 $fW/Hz^{1/2}$ at the frequency range of 110-155 GHz, and its minimum value is about 9.3 $fW/Hz^{1/2}$ at 130 GHz.

The effective RF noise bandwidth (B_{RF}) of a radiometer can be found by equation (45) using the measured responsivity (β) performance of the radiometer itself [36]. In this way, the effective RF noise bandwidths were calculated to be 52.3 GHz and 51.4 GHz for the total power radiometer and the Dicke radiometer, respectively.

$$B_{RF} = \frac{\left[\int_0^\infty \beta\,(f)df\right]^2}{\int_0^\infty \beta^2(f)df} \tag{45}$$

The effective responsivity (β_{eff}) of a radiometer can be calculated by equation (46) using the measured responsivity (β) values of the radiometer itself [59]. Thus, the effective responsivity values were found to be 1093 MV/W and 552 MV/W for the total power radiometer and the Dicke radiometer, respectively.

$$\beta_{eff} = \frac{\int_0^\infty \beta^2(f)df}{\int_0^\infty \beta(f)df} \tag{46}$$

Consequently, the noise equivalent temperature difference (NETD) performance of the total power radiometer was determined by equation (47) as in [60]. It should be noted that the noise equivalent power (NEP) in equation (3) was derived by dividing the output rms noise voltage by the effective responsivity value. The external calibration techniques require a shorter back-end integration time such as 3.125 ms. Therefore, the NETD of the total power radiometer was calculated for a back-end integration time of 3.125 ms. In the NETD calculation of the Dicke radiometer, the integration time was taken to be 30 ms which is a typical value for the passive imaging systems. In addition, the NETD value for the total power radiometer was calculated assuming an external mechanical switching. Therefore, the penalty factor of 2 was included to account either for mechanical (total power radiometer) and electrical (Dicke radiometer) switching, as presented in equation (48). Moreover, the NETD of the total power radiometer was also calculated for different normalized gain-fluctuation values, using equation (7). Figure 59 shows the NETD performance of the total power radiometer respect to various normalized gain-fluctuation values.

$$NETD = \frac{NEP}{kB_{RF}\sqrt{2\tau}} \tag{47}$$

$$NETD = 2\frac{NEP}{kB_{RF}\sqrt{2\tau}} \tag{48}$$

Finally, the NETD of the total power radiometer was found to be 0.11K, assuming an external calibration technique and a back-end integration time of 3.125ms. The NETD of the total power radiometer was also calculated to be 1.3K, assuming a gain-fluctuation of %0.1. In addition, the NETD of the total power radiometer was found to be 0.07K, assuming a mechanical switch that has no insertion loss. On the other hand, the NETD of the Dicke radiometer was determined to be 0.13K for a back-end integration time of 30 ms.

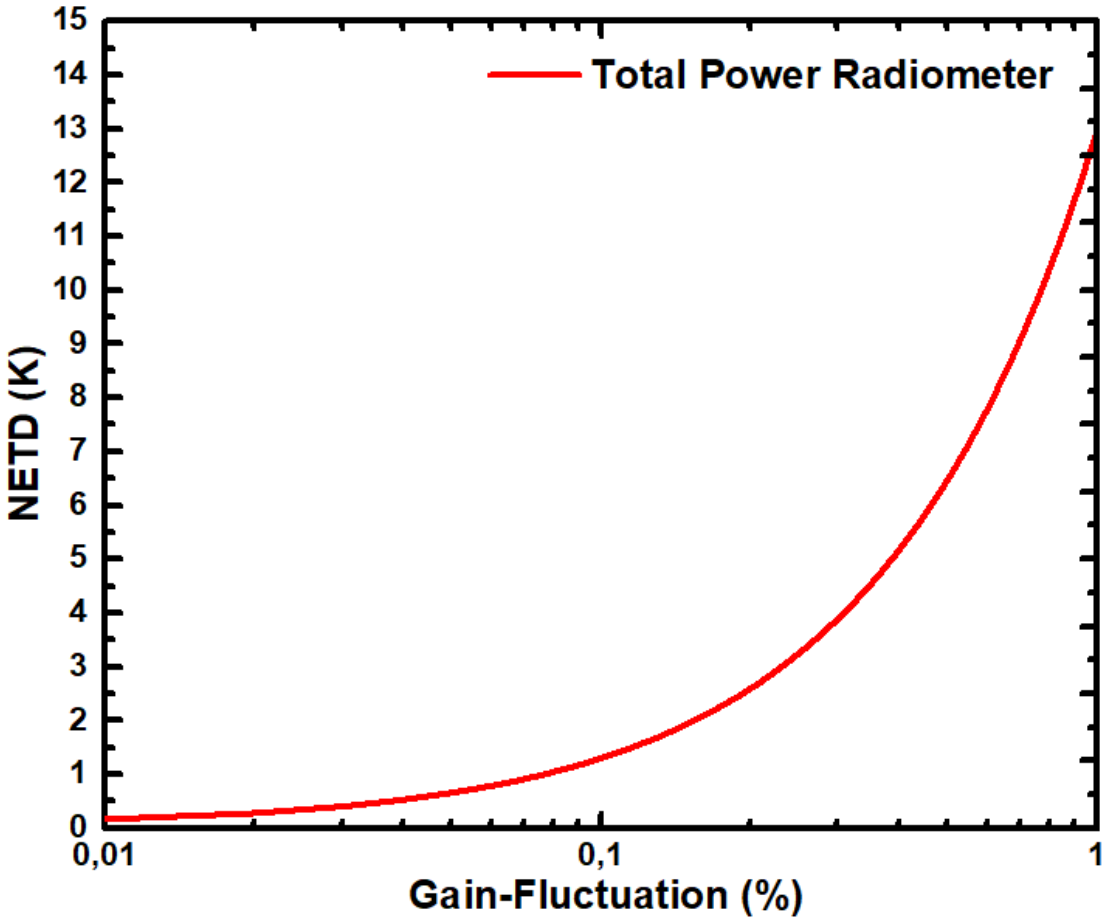

Figure 59 NETD of the total power radiometer for various gain-fluctuation ratios.

2.5.3 Comparison

Table 6 summarizes the performance comparison of the implemented radiometers with previously reported millimeter-wave radiometers. To the authors' best knowledge, the implemented radiometers achieve the best noise equivalent temperature difference (NETD) performances and widest effective RF noise bandwidths in the literature, even better than the millimeter-wave radiometers implemented in III-V semiconductor technologies. The key factor in achieving such a high NETD performance is to be having widest effective RF noise bandwidth which is almost twice that of the nearest study. Therefore, it should be also noted that this study highlights the superior potential of the Butterworth staggered-tuning technique for the millimeter-wave radiometers. Consequently, the implemented total power and Dicke radiometers show the state-of-the-art performances, and they are suitable to be employed in millimeter-wave passive imaging systems by integrating with on-chip or external antennas, and specifically designed baseband parts.

Table 6 Summary of performance comparison of the implemented radiometers with previously reported millimeter-wave radiometers.

	Technology	**Top.**	**Center Freq.** GHz	**NETD** K	B_{RF} GHz	τ ms	NEP $fW/Hz^{1/2}$	β MV/W	P_{DC} mW	**Size** mm^2
[61]	InP HEMT	TPR	92	**0.45**$^{\alpha}$ **0.30**$^{\beta*}$	29	3.125 30	N/A	18	40	N/A
[62]	InP HEMT	TPR	94	**0.29**$^{\alpha}$ **0.18**$^{\beta*}$	28	3.125 30	0.9	4.5	N/A	N/A
[63]	InAlGaAs	Dicke	94	**0.32**	N/A	N/A	N/A	N/A	N/A	N/A
[7]	65nm CMOS	TPR	85	**1**	10	30	8.8$^{\pm}$	16.1	93.2	3
[64]	65nm CMOS	Dicke	86	**1.1**	18	30	36$^{\pm}$	0.666¶	110	0.41
[60]	0.13μm SiGe BiCMOS	TPR	90	**0.69***	15	30	20	4.4	34.8	N/A
[60]	0.13μm SiGe BiCMOS	Dicke	90	**0.83**	15	30	21	4.9	34.8	0.4
[67]	0.18μm SiGe BiCMOS	Dicke	94	**0.48**	10	30	8.1$^{\pm}$	285	197	2.6
[65]	0.18μm SiGe BiCMOS	Dicke	85	**0.4**	26	30	10	43	200	3.1
[68]	0.13μm SiGe BiCMOS	TPR	97.5	**0.45*** **0.37**$^{\beta*}$	21	20 30	0.28	1150	225	N/A
[69]	0.13μm SiGe BiCMOS	Dicke	92	**0.78**	15	30	37$^{\pm}$	27	75	0.32
[70]	0.13μm SiGe BiCMOS	Dicke	90	**0.21**	8	30	1.9 2.7$^{\pm}$	240 166.1¶	28.5	3.42
[66]	65nm CMOS	Dicke	140	**1.5**	21	30	26	1.2	152	N/A
[4]	SiGe (270/330 GHz f_t/f_{max})	TPR	165	**0.35**$^{\alpha}$ **0.23**$^{\beta*}$	10	3.125 30	14	28	95	0.4
[52]	90nm SiGe BiCMOS	TPR	136	**0.25**$^{\alpha}$ **0.16**$^{\beta*}$	11.8	3.125 30	1.4	52	47.2	0.5
This Work	0.13μm SiGe BiCMOS	TPR	130	**0.11** **1.3**$^{\gamma}$ **0.07***	52.3	3.125 3.125 30	4.8 6$^{\pm}$	1377 1093¶	28.5	1.3
This Work	0.13μm SiGe BiCMOS	Dicke	130	**0.13**	51.4	30	9.3 11.6$^{\pm}$	688 552¶	33.8	1.7

* Assuming an external mechanical switching with a penalty factor of 2.
$^{\pm}$ Derived NEP value by using the effective responsivity value (or average NEP).
¶ Effective (Average) responsivity value.
$^{\alpha}$ Assuming a calibration without reducing the observation time.
$^{\beta}$ Recalculated system performance for 30ms back-end integration time.
$^{\gamma}$ Assuming a gain-fluctuation of %0.1.

3. W-Band Frequency Extension Module for VNAs

In this chapter, first, the fundamental operating principle of a VNA, and its basic architectures are presented. Then, the frequency extension concept and the architecture of the single-chip frequency extension module are depicted. After that, the design methodologies, implementation methods, and measurement results of the sub-blocks are presented. In addition, the comparisons of the significant sub-blocks (down-conversion mixer and frequency quadrupler) with the previously reported studies are briefly summarized. Finally, the characterization and the experimental results of the implemented single-chip frequency extension module are presented.

3.1. S-Parameter Measurements Using Frequency Extension Modules

3.1.1 Network Analyzer

Network Analyzer is the basic measurement equipment which is mostly used for characterization of RF, microwave and millimeter-wave electronic networks. A network analyzer measures S-parameters which are capable to completely describe the small-signal properties of electronic circuits such as active circuits, passive components, and sensors. SNAs are capable to measure only amplitude qualities of the incident, reflected, and transmitted waves. In other words, it is not possible to acquire the phase information of the signals by using an SNA. However, VNAs can also measure the phase relationships between the incident, reflected, and transmitted signals in addition to the amplitude properties. Therefore, VNAs have tremendous advantages over SNAs to completely and precisely figure out the small-signal behaviors of the electronic networks.

A simplified block diagram of a typical two-port SNA is illustrated in Figure 60. As can be seen from the figure, it uses the amplitude detectors to measures the incident, reflected and transmitted signals so that it misses the phase relationships between the signals. Assume that the s-parameters of a device under test are being measuring, as illustrated in Figure 60. First, the RF signal is directed to the port-1 by the port switch. The RF signal is sampled by the first directional coupler, and its amplitude (a1') is measured by the amplitude detector labeled as “reference-1”. At the same time, the reflected signal is sampled by the second directional coupler, and its amplitude (b1') is measured by the amplitude detector labeled as “test-1”. In fact, the magnitude of the S11 of the device under test is found by dividing the amplitude of the reflected signal (b1) by the amplitude

of the incident signal (a1), as presented in equation (49). Therefore, an error correction, which is termed as calibration, should be performed, as discussed later. After that, the amplitude of the transmitted signal (b2') is determined by the test-2 amplitude detector, and the amplitude of the incident signal (a1') continues to be measured simultaneously. In the same way, a calibration should be done because of the fact that the S22 of the device under test is equal to the quotient of the actual amplitude of the transmitted signal (b2) and the actual amplitude of the incident signal (a1), as described in equation (50).

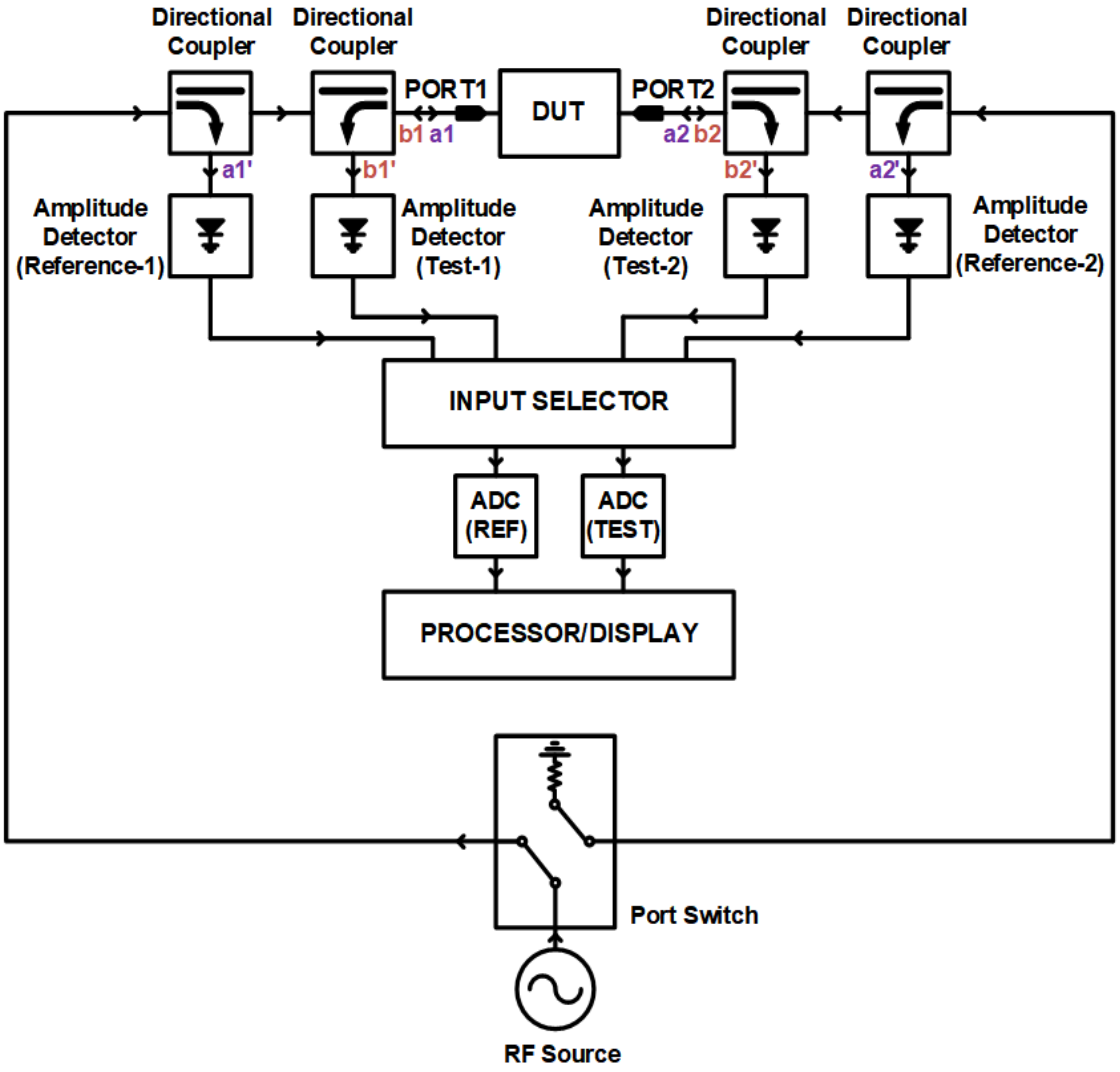

Figure 60 Simplified block-diagram of a typical two-port scalar network analyzer.

$$|S11| = \left.\frac{|b1|}{|a1|}\right|_{a2=0} \tag{49}$$

$$|S21| = \left.\frac{|b2|}{|a1|}\right|_{a2=0} \tag{50}$$

Figure 61 presents a simplified block diagram of a typical two-port VNA. VNAs are operating as like described above for SNAs. However, as can be seen from the figure, it employs down-conversion mixers instead of amplitude detectors so that the incident, reflected, and transmitted signals are down-converted to IF signals. These IF signals are converted into digital domain by analog-to-digital converters (ADCs), and then divided to I and Q signals by processing with digital IQ-demodulators. Later, these I and Q signals are converted to magnitude and phase information for further signal processing. In practice, multiple frequency down-conversion process might be performed before ADCs.

As can be seen from Figure 61, a two-port VNA comprises two front-end circuits, which is termed as a reflectometer, that consist of basically two directional couplers, two down-conversion mixers, and a power divider. In essence, the reflectometers can be considered as the hearts of the VNAs since they dominantly determine the main performance specifications of the VNAs such as frequency range, input impedance, dynamic range, noise floor, etc. In addition, the directivity and the input impedance of the reflectometers dominate the measurement uncertainty of the performed measurement.

Figure 62 shows the flow graph of the 3-term error model of the one-port s-parameter measurement which is performed by a VNA, where e_{00} is the error that arises due to the finite directivity of the reflectometer, e_{11} is the error due to the port matching, and e_{10} and e_{01} are the tracking errors (insertion losses etc.). The actual reflection coefficient of the device under test, which is equal to S11 of the device under test when the other ports are terminated with match load if they exist, can be determined by dividing the *b1* (reflected wave) by the *a1* (incident wave), as described in equation (51). However, the measured reflection coefficient is equal to the division of *b0* by *a0*, as shown in equation (52). Therefore, an error correction should be performed to remove the errors such as e_{00}, e_{01}, e_{10}, and e_{11}.

$$\Gamma_{11} = \frac{b1}{a1} \tag{51}$$

$$\Gamma_{11-M} = \frac{b0}{a0} \tag{52}$$

The actual reflection coefficient (Γ_{11}) can be expressed in terms of the measured reflection coefficient (Γ_{11-M}), the directivity error (e_{00}), the port match error (e_{11}), and the overall tracking error ($e_{01}e_{10}$) by considering the flow-graph of the one-port three-term error model shown in Figure 62, as described by equation (53). This equation can be rewritten

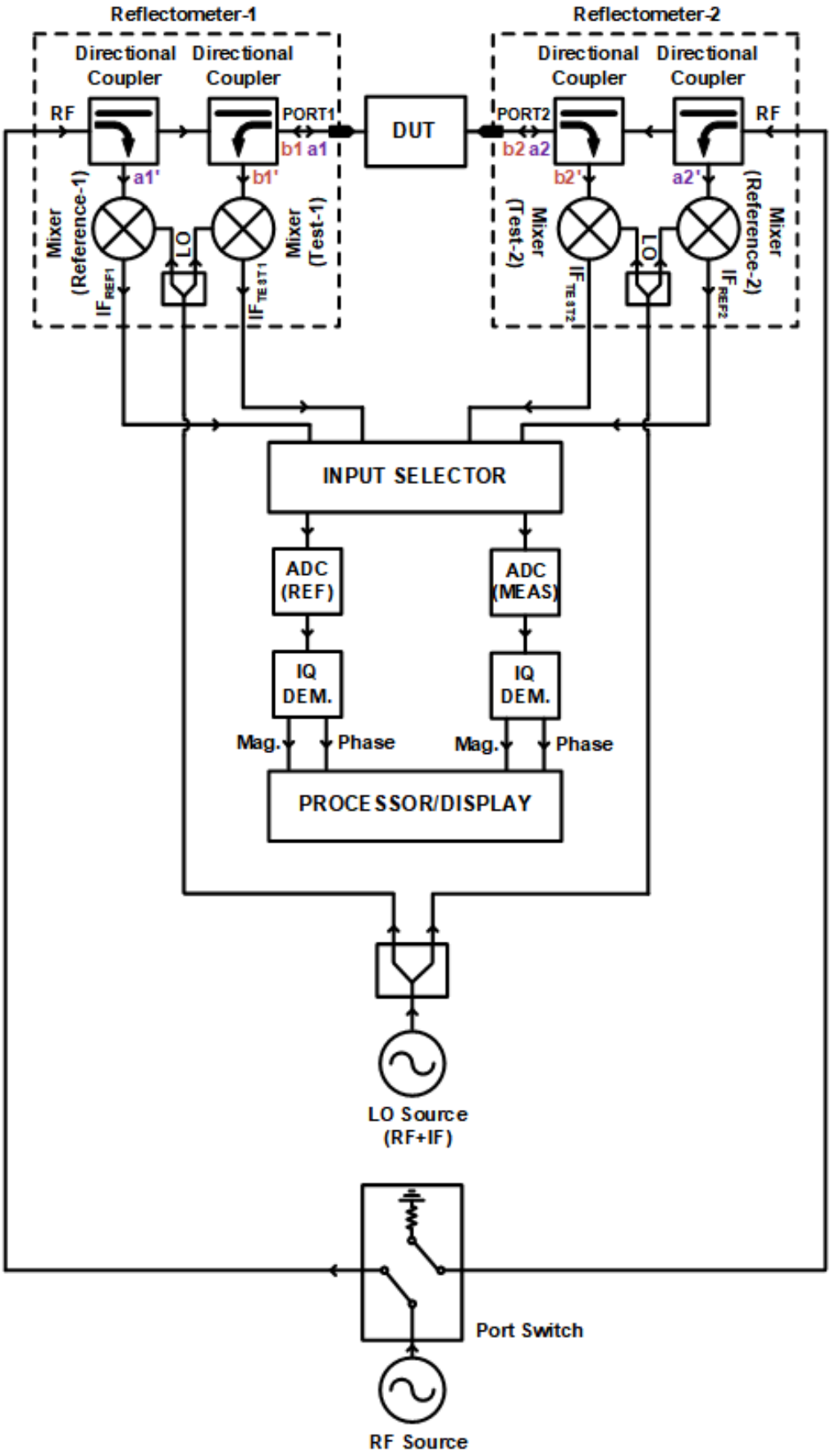

Figure 61 Simplified block-diagram of a typical two-port vector network analyzer.

as shown in equation (54) by leaving the actual reflection coefficient (Γ_{11}) alone on the left side. The product of e_{10} and e_{01} can be considered as one term for the ratio measurements. That is also why this error model is named as "three-term error model".

$$\Gamma_{11-M} = e_{00} + (e_{10}e_{01}) \times \frac{\Gamma_{11}}{1 - e_{11}\Gamma_{11}} \tag{53}$$

This equation can be rewritten as shown in equation (53) by leaving the actual reflection coefficient (Γ_{11}) alone on the left side and taking the product of e_{10} and e_{01} as one term which is named as the overall tracking error (e_T).

$$\Gamma_{11} = \frac{\Gamma_{11-M} - e_{00}}{e_T + \Gamma_{11-M}e_{11} - e_{00}e_{11}} \tag{54}$$

As can be seen from the equation, there are three unknown terms, and it means that we need to have three independent equations at least to find the actual reflection coefficient. For this reason, three different measurements must be performed with three independent standards such as short ($\Gamma_{11} = -1$), open ($\Gamma_{11} = 1$), and match load ($\Gamma_{11} = 1$) to make error correction (calibration). In fact, this works for any three independent linear measurement, not just for short-open-load (SOL), but these three standards are very suitable to build for all frequency range.

The flow graph of the six-term forward error model of the two-port s-parameters measurement is presented in Figure 63, where e_{00} is the error that arises due to the finite directivity of the reflectometer of the port-1, e_{11} is the error due to the port-1 matching, e_{10} and e_{01} are the reflection tracking errors (insertion losses etc.), e_{22} is the port-2's matching error, e_{30} is the error because of the signal leakage from the port-1 to the port-2, and e_{10} and e_{01} are the transmission tracking errors. Solving the flowgraph of the two-port six-term forward error model shown in Figure 63 yields measured S11 (S11m) and S21 (S21m) as described in equation (55) and equation (56), respectively, in terms of the errors mentioned above and the actual s-parameters of the device under test ($S_{11}, S_{12}, S_{21}, S_{22}$), where $\Delta_s = S_{11}S_{22} - S_{21}S_{12}$.

$$S_{11M} = \frac{b_0}{a_0} = e_{00} + (e_{10}e_{01})\frac{S_{11} - e_{22}\Delta_s}{1 - e_{11}S_{11} - e_{22}S_{22} + e_{11}e_{22}\Delta_s} \tag{55}$$

$$S_{21M} = \frac{b_3}{a_0} = e_{30} + (e_{10}e_{32})\frac{S_{21}}{1 - e_{11}S_{11} - e_{22}S_{22} + e_{11}e_{22}\Delta_s} \tag{56}$$

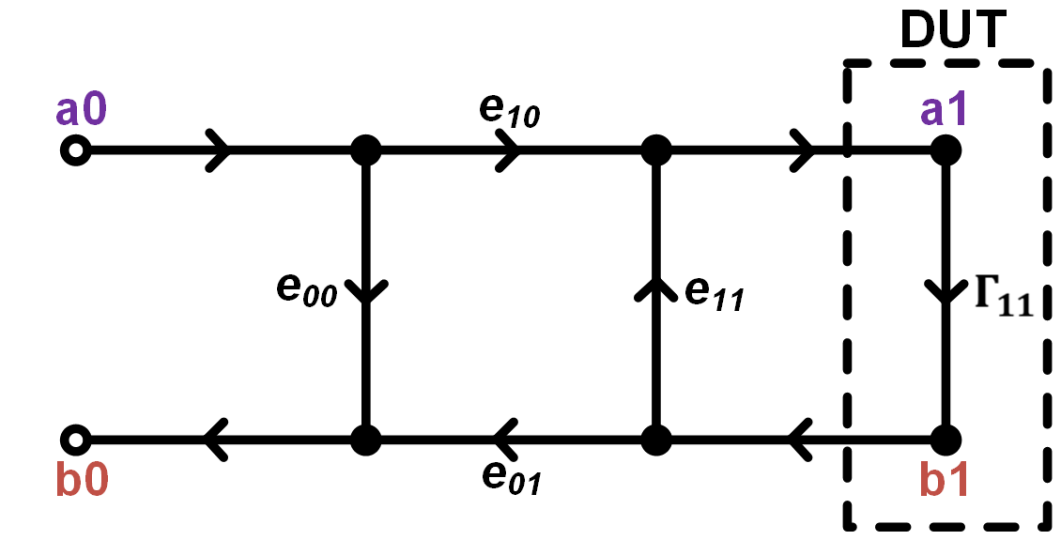

Figure 62 One-port three-term error model for the s-parameter measurement.

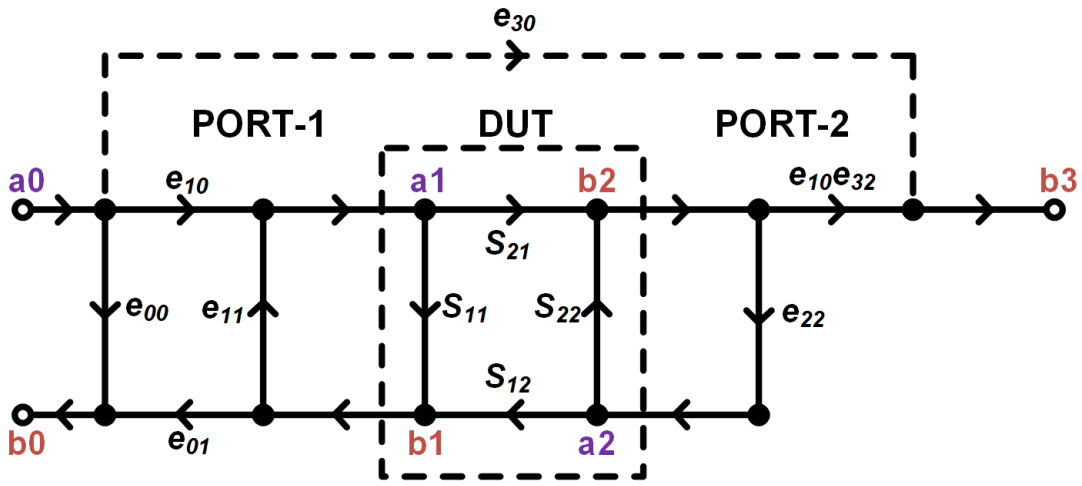

Figure 63 Two-port six-term forward error model for the s-parameter measurements.

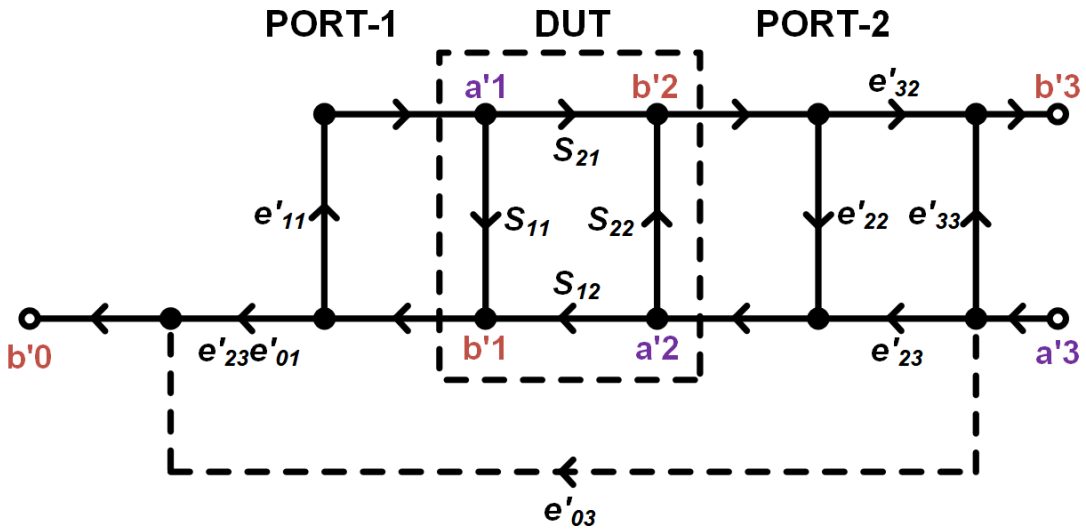

Figure 64 Two-port six-term reverse error model for the s-parameter measurements.

Two-port s-parameters measurement requires a second error model which is the six-term error mode for the reverse operation. Figure 64 shows the flow graph of the six-term reverse error model of the two-ports s-parameters measurement, where e'_{33} is the error because of the finite directivity of the port-2's reflectometer, e'_{11} is the error due to the port-1 matching, e'_{10} and e'_{01} are the reflection tracking errors (insertion losses etc.), e'_{11} is the port-1's matching error, e'_{03} is the error because of the signal leakage from the port-2 to port-1, and e'_{23} and e'_{32} are the transmission tracking errors.

Considering the flowgraph of the two-port six-term reverse error model shown in Figure 64, the measured S22 (S22m) and S12 (S12m) can be expressed by equation (57) and equation (58), respectively, in terms of the errors mentioned above for the reverse operation, and the actual s-parameters of the device under test ($S_{11}, S_{12}, S_{21}, S_{22}$), where $\Delta_s = S_{11}S_{22} - S_{21}S_{12}$.

$$S_{22M} = \frac{b'_3}{a'_3} = e'_{33} + (e'_{23}e'_{32})\frac{S_{22} - e'_{11}\Delta_s}{1 - e'_{11}S_{11} - e'_{22}S_{22} + e'_{11}e'_{22}\Delta_s} \quad (57)$$

$$S_{21M} = \frac{b'_0}{a'_0} = e'_{03} + (e'_{23}e'_{32})\frac{S_{12}}{1 - e'_{11}S_{11} - e'_{22}S_{22} + e'_{11}e'_{22}\Delta_s} \quad (58)$$

The four equations derived above ((55-(58) for the forward and reverse measurement operations comprise the four-actual s-parameters of the device under test, and total 12 error terms (6+6=12). It should be highlighted here that either the product of e_{10} and e_{01}, and the product of e'_{23} and e'_{32} is taken as individually one term because of the ratio measurements. If these 12 error terms are figured out, the equation system that includes these four equations can be solved in order to acquire the actual s-parameters of the device under test. Even though, there are total twelve unknown terms, we have just four equations. It means that eight more independent linear equations are required to solve the equation system completely. Therefore, the six error terms in the forward operation are solved, and then the other six error terms in the reverse operation are figured out using the same procedure which is used in the solution of the forward equation system.

Let's start with the error correction of the forward mode. First, the directivity error (e_{00}), the port-2 matching error (e_{11}), and reflection tracking error ($e_{10}e_{01}$) are determined using the same error correction procedure predefined for the one-port three-term error model (i.e., short-open-load for the port-1). Second, the leakage from the port-1 to the port-2 (e_{30}) is found by taking the measurement while connecting the match load to each of the ports. Third step is to figure out the match error of the second port (e_{22}) by

measuring directly by the reflectometer of the first port which is already calibrated at the first step. Lastly, the overall transmission tracking ($e_{10}e_{32}$) is measured by connecting the ports to each other.

The procedure which is described for the six-term error correction of the forward mode can be followed for the reverse mode as well to figure out the six error terms mentioned before. In this way, total twelve-terms of the two-port error model is determined.

3.1.2 Frequency Extension Module

The main limiting factors that determine the upper-frequency edge of a VNA are the frequency ranges of the reflectometers and RF&LO sources. Even though there is an effort to extend the frequency ranges of the reflectometers and RF&LO sources, the trend is not to integrate them with the base units of the VNAs. Instead, the frequency extension modules that consist of reflectometers and frequency multiplication components are employed to extend the frequency range of the s-parameter measurements. The simplified block diagram of a frequency extension module configured with a VNA is presented in Figure 65.

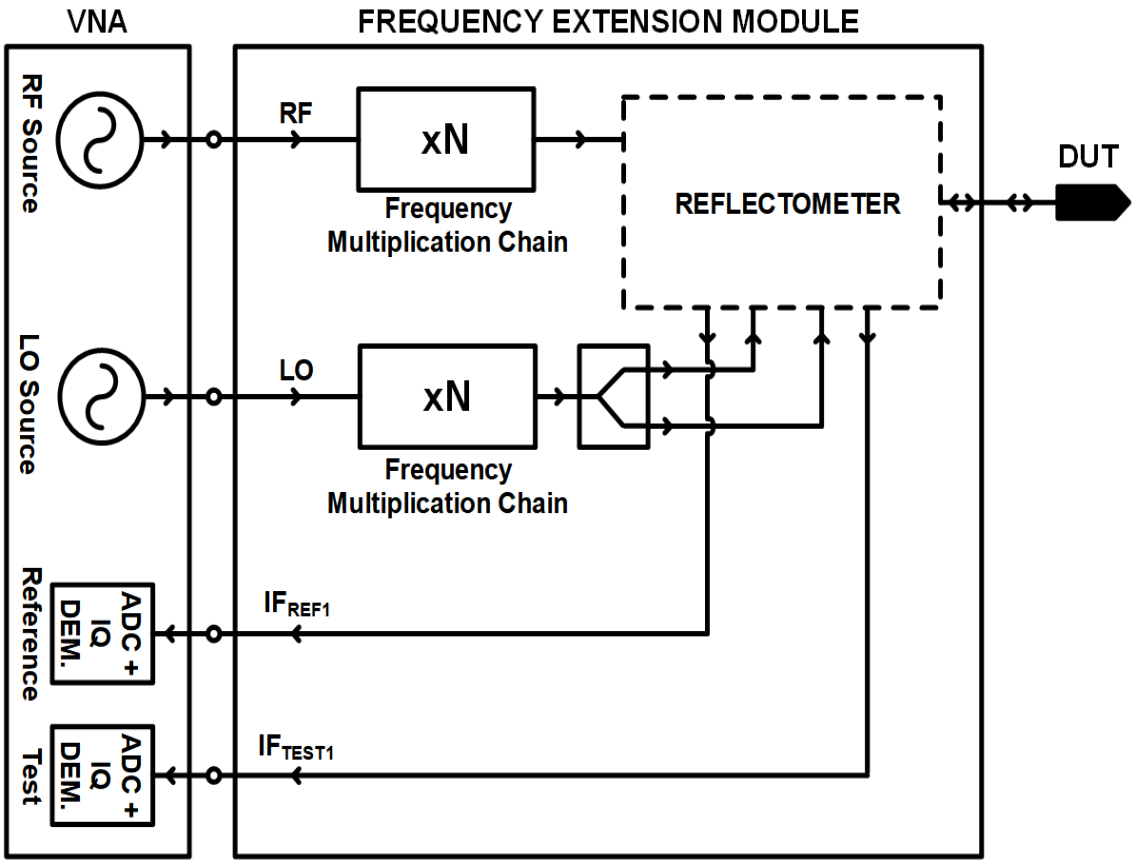

Figure 65 Simplified block diagram of a frequency extension module.

There are several significant reasons of using the frequency extension modules instead of extending the frequency ranges of the base units of VNAs. First, the existing coaxial cables and connectors in the market do not work properly above 110 GHz. However, 0.8mm coaxial cables and connectors, which are capable of operating up to 145 GHz, have recently begun to appear on the market [71]. Therefore, using the rectangular or circular waveguides for above 145 GHz measurements is still an imperative, and thereby it is not possible to manage the connections between the outputs of a VNA and the ports of a device under test, because of the waveguide's rigidity structures. Second, the free-space wavelengths of the signals above 75 GHz are extremely small (<4mm) respect to the required lengths of the cables that should use to connect the ports of the device under test to the output connectors of the VNA. It results in intolerance to even small changes in the positions of the cables that would significantly degrade the accuracy of the measurement due to severe phase changes. For this reason, the output of the reflectometer should be as close as possible to the ports of the device under test. Last, there are already many vector network analyzers available in the customer's hands which are compatible with the configuration with frequency extension modules. Thus, many customers tend to extend the frequency range of their measurement systems by using the frequency extension modules to avoid high costs of having a new VNA.

Although there are many advantages of using frequency extension modules to extend the frequency range of the measurements, the frequency extension modules have many significant drawbacks. First of all, a typical frequency extension module built with waveguide components may weigh about 2.5 kg or even more, and its physical dimensions might be as much as 18 cm × 7 cm × 24 cm [71]. It leads to difficulties in placing the frequency extension modules near to the device under test, and this has a negative impact on the performance of the measurement. In addition, they need specially designed holders and positioners which are compatible to integrate with the probe station because of the bulky and heavy structures of the frequency extension modules, and this increases costs. Second, the interior height and width sizes of the waveguides which are compatible with such a frequency extension module are typically a few millimeters or even less (see Table 7). Discontinuities and erosions at the connection interfaces due to usage would significantly deteriorate the accuracies of the measurements [72]. In addition, misalignments at the connections of two waveguides might considerably cause systematic errors in the error corrections (calibration) of the measurements [73]. Finally,

but most importantly, as can be seen from Table 7 and approximately described in equations (59) and (60), where c is the speed of the light in the free-space, and a is the physical dimension of the width of the waveguide, for the air filled rectangular waveguides, the waveguides have both lower and upper cut-off frequencies that determines their operating frequency range. For this reason, the frequency extension modules can operate in only the frequency range that they are specifically aimed. In addition, the frequency extension modules require the waveguide input wafer probes specially designed for each waveguide frequency band for the on-wafer measurements. Whereas, the coaxial cables have just one cut-off frequency that determines the upper limit of their frequency ranges, as described in equation (61) for the air-filled cables so that they can operate from DC to their cut-off frequencies. Therefore, the frequency extension modules with the coaxial outputs (1 mm up to 110 GHz and 0.8 mm up to 145 GHz) have recently begun to take place in the market (Anritsu ME7838E/D [74], Keysight N5290A [75], Rohde&Schwarz [76]). They provide a very broad frequency range such as from DC to 110 or 145 GHz. Nevertheless, the usage of the coaxial output is not an ultimate solution for the higher frequencies.

Table 7 Millimeter-wave rectangular waveguides' physical dimensions and operating frequency bands.

Waveguide Standard Code (EIA)	**Recommended Frequency Band (GHz)**	**Lower Cutoff Frequency (GHz) (for lowest order)**	**Higher Cutoff Frequency (GHz) (for lowest order)**	**Interior Width (mm)**	**Interior Height (mm)**
WR22	33-50	26.346	52.692	5.6896	2.8448
WR19	40-60	31.391	62.782	4.7752	2.3876
WR15	50-75	39.875	79.75	3.7592	1.8796
WR12	60-90	48.373	96.746	3.0988	1.5494
WR10	75-110	59.015	118.03	2.54	1.27
WR8	90-140	73.768	147.536	2.032	1.016
WR6.5	110-170	90.791	181.583	1.651	0.8255
WR5	140-220	115.714	231.429	1.2954	0.6477
WR4	170-260	137.243	274.485	1.0922	0.5461
WR3	220-330	173.571	347.143	0.8636	0.4318

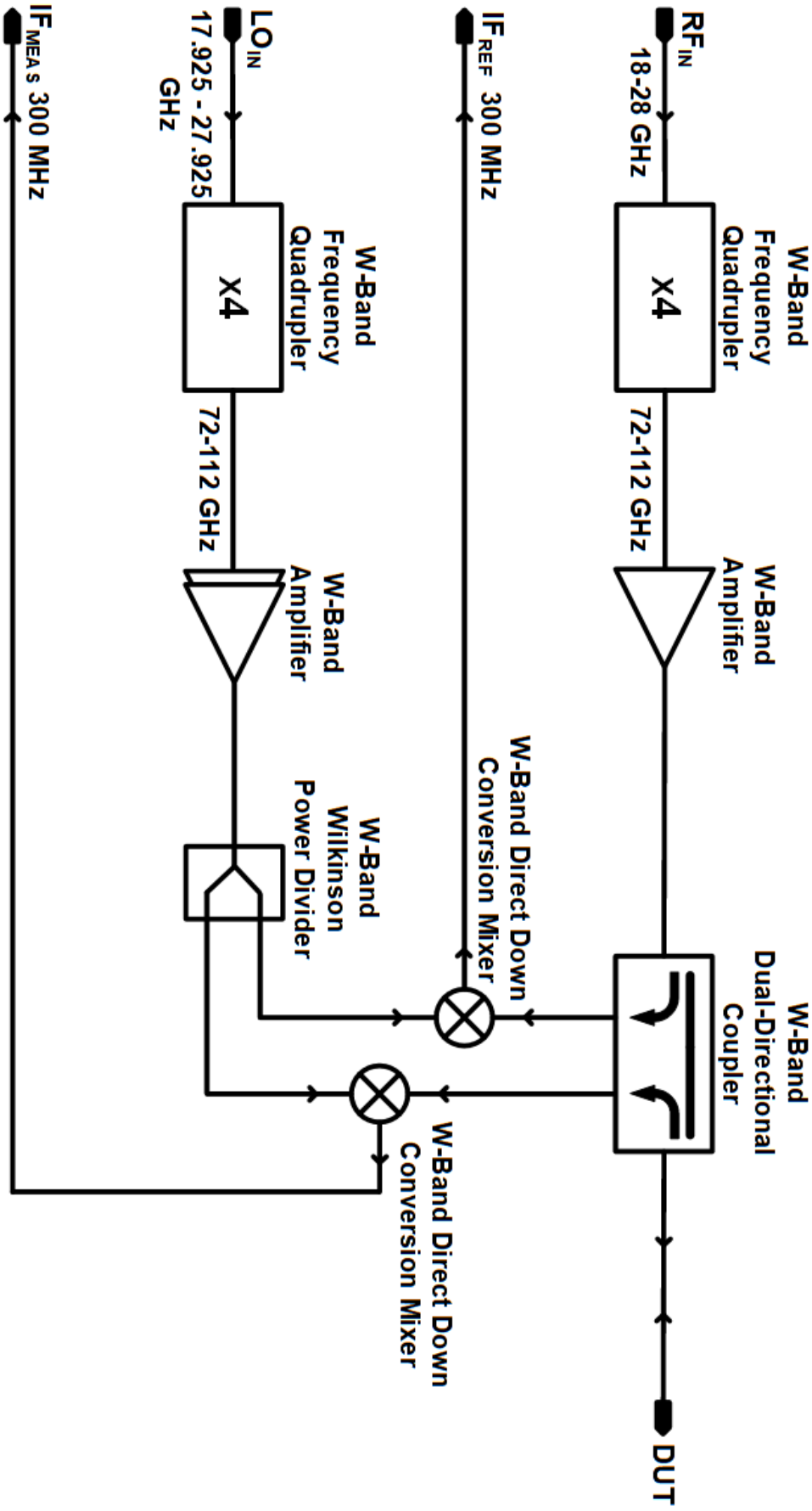

Figure 66 Detailed block diagram of the designed single-chip frequency extension module.

$$f_{lower-cutoff} = \frac{c}{2a} \tag{59}$$

$$f_{upper-cutoff} = \frac{c}{a} \tag{60}$$

$$f_{cutoff} = \frac{c}{\pi(\frac{D+d}{2})\sqrt{\mu_R \epsilon_R}} \tag{61}$$

3.1.3 Single-Chip Frequency Extender and System Simulations

The detailed block diagram of the designed W-band single-chip frequency extension module for VNAs is presented in Figure 66. As can be seen from the figure, the fully integrated frequency extension module, which receives RF (18-28 GHz) and LO (17.925-27.925 GHz) signals from the VNA and sends two IF (MHz) signals (reference and test signals) to the VNA, consists of two single-balanced W-band down-conversion mixers, two balanced frequency quadruplers (K-band to W-band), two W-band amplifiers, a W-band Wilkinson power divider, and a W-band dual directional coupler. In essence, the frequency extension module can be considered as a superheterodyne transceiver that can simultaneously receivers and transmits through single-port.

Assuming an ideal power splitter with an insertion loss of 3 dB and an isolation of 25 dB, a dual directional coupler with a coupling of 10 dB and a directivity of 45 dB, two direct down-conversion mixers with a conversion loss 7 dB and a LO-to-RF isolation of 40 dB, two frequency quadrupler with a conversion loss of 10 dB for even harmonics and a conversion loss of 30 dB for odd harmonics, the system simulations were performed using harmonic balance simulations through ADS. A 3-dBm RF input signal sweeping from 18.75 GHz to 27.5 GHz and a 3-dBm LO input signal sweeping from 18.675 GHz to 27.425 GHz were applied through 50Ω power terminals.

The amplitude ratio and the phase difference of the 300 MHz IF reference and test signals were tracked as the outputs of the systems. The measured reflection coefficient (Γ_{11-M}), which is described in equation (53) for the three-term error model of the one-port s-parameter measurement, is equal to phasor division of the IF test signal by IF reference signal. In this way, a SOL error correction is virtually performed using short, open, and load standards through the MATLAB. Finally, an impedance (10-45j Ω) was connected to DUT port, and it was verified by the MATLAB code which gives us 10.1232-45.2538j Ω at 90 GHz. The MATLAB code which was used to perform the virtual short-open-load (SOL) calibration is given in Appendix B.

Figure 67 and Figure 68 depict the representative 2D and 3D models of the proposed active probe, respectively, which utilizes the designed single-chip frequency extension module for the VNAs. In this way, the output of the frequency extension module can be placed as close as possible to the device under test so that it helps us to avoid the performance degeneration of the measurement due to the long distance, which is detailly explained above (in Section 3.1.2). Furthermore, this approach overcomes the frequency band limitations of the waveguides.

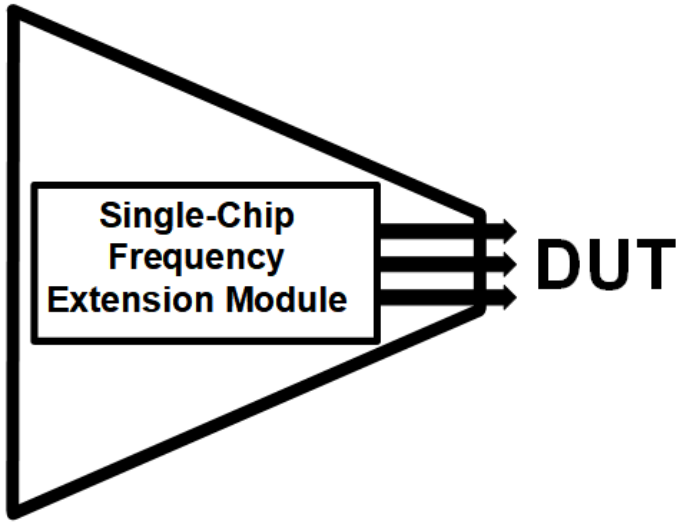

Figure 67 2D representative model of the proposed active probe.

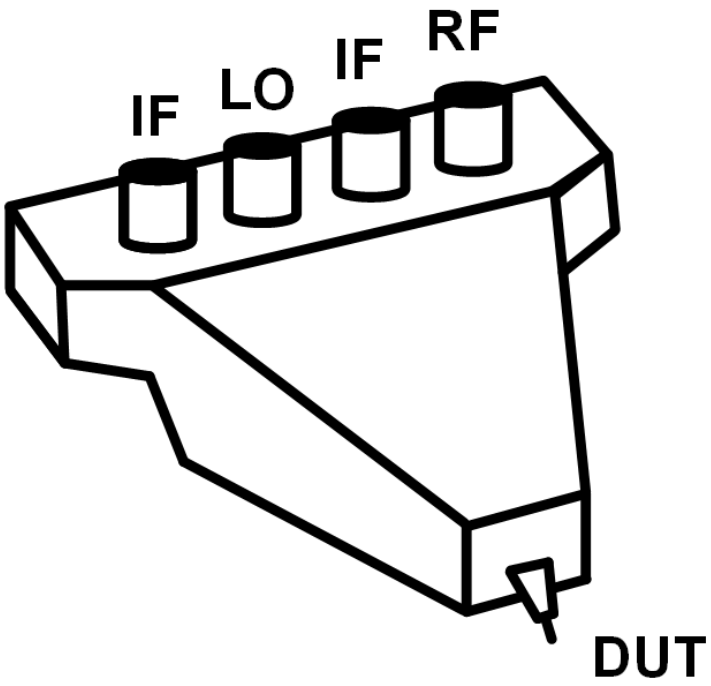

Figure 68 3D representative model of the proposed active probe.

3.2. Down-Conversion Mixer

3.2.1 Circuit Design and Implementation

The mixer is one of the basic RF circuits, which performs the down-conversion and up-conversion by multiplying two different signals. There are three basic configurations of active mixers: single-ended, single-balanced, and double-balanced [77]. These three mixer topologies have their advantages and disadvantages. The single-ended configuration comes to the forefront with features such as lower power consumption, less LO power requirements, and design simplicity. However, it suffers from some performance deficiencies, in particular, a lack of isolations between the RF and LO ports, the LO and IF signals, and the RF and IF ports. On the contrary, the double-balanced mixer topology has significant drawbacks, including the higher power consumption and the design complexity, although it is capable to completely solve the isolation deficiencies that cannot be handled by the single-ended configuration. In addition, the double-balanced mixer configuration requires two baluns that convert the input RF and LO signals to balanced RF and LO signals. The single-balanced mixer can be considered in the middle of these two topologies, in terms of the RF performances and the requirements. For instance, its power consumption and LO power requirement are less than the double-balanced mixer, but more than the single-ended mixer. Furthermore, it needs just one balun, which is employed to convert the unbalanced LO input to the balanced signal for the switching LO pair. Moreover, it significantly suppresses the signal leakages from LO port to RF port as in the double-balanced configuration.

In essence, s-parameter measurement can be considered as a kind of single-tone test. Therefore, there must be a single signal coming into the port of the device under test. In addition, the LO-to-RF leakage of the mixer would degrade the accuracy of the measurement since the leakaged LO signal would produce an undesired IF signal in the other receiver in the reflectometer [78]. For this reason, it is very significant to suppress the leakage between the LO and RF ports of the mixer. With all these considerations in mind, the single-ended topology was chosen to perform down-conversion. The detailed circuit schematic of the designed W-band single-balanced down-conversion mixer is shown in Figure 69. The designed circuit includes a Marchand balun and an off-chip wideband discrete IF 3:1 transformer (WBC-3TL) in addition to the single-balanced core.

The tail transistor (Q1), which is the CE driver stage, converts the incoming RF voltage signal into a current signal, and then the switching differential pair multiplies this current signal by the incoming LO signal. Thence, the conversion gain of the mixer strongly depends on the transconductance and the parasitic capacitances (C_π and C_μ) of the tail transistor. Therefore, the transistor was biased where its f_t is maximum. The optimum number of the transistor was found by considering the input matching of the driver stage (RF input). The tail transistor was degenerated by an inductive impedance to set the real part of its input impedance to 50Ω, and also this inductive degeneration improves the linearity.

On the other hand, the LO switching transistors were biased at the Class-B point to perform switching as ideal as possible [77]. The optimum LO power was found to be -4 dBm to acquire better conversion gain performance. The number of the transistors were optimized to provide better LO input matching. The inductive emitter degenerations were utilized to set the real part of the input impedance of each switching transistor (Q2, Q3) to 25Ω thanks to that the collector node of the driver stage is the virtual ground for the switching differential pair.

The leakages of the LO and RF signals to IF ports were eliminated by placing a shunt-capacitor of 550 fF at the output of each switching transistor. The supply voltage (V_{CC}) was supplied through the resistors of 250Ω instead of the inductors. Because, tens of nHs are required to provide high impedance at the IF frequency of 300 MHz, and an on-chip inductor of around these values would occupy an incredibly large area with respect to the mixer itself. However, the resistive load would dramatically reduce the 1-dB compression point of the mixer. Therefore, the resistors of 250Ω were employed to avoid significant voltage drop, considering also the output impedance matching. The differential IF output was converted to single-ended output using an off-chip 3:1 wideband transformer. However, the IF output was taken single-endedly in the frequency extension module, as depicted in Figure 70, to avoid large areas of passive baluns and the high-power consumptions of the active baluns, and meanwhile the other IF output was terminated with an on-chip resistor of 50Ω. The LO signal was supplied into the switching differential pair transistors by the designed Marchand balun that consists of two quarter wave coupled line pairs. Figure 71 shows the simulated EM results of the amplitude and phase balances of the designed Marchand balun. The amplitude balance is better than 1 dB and the phase balance is less than 2° over the W-band.

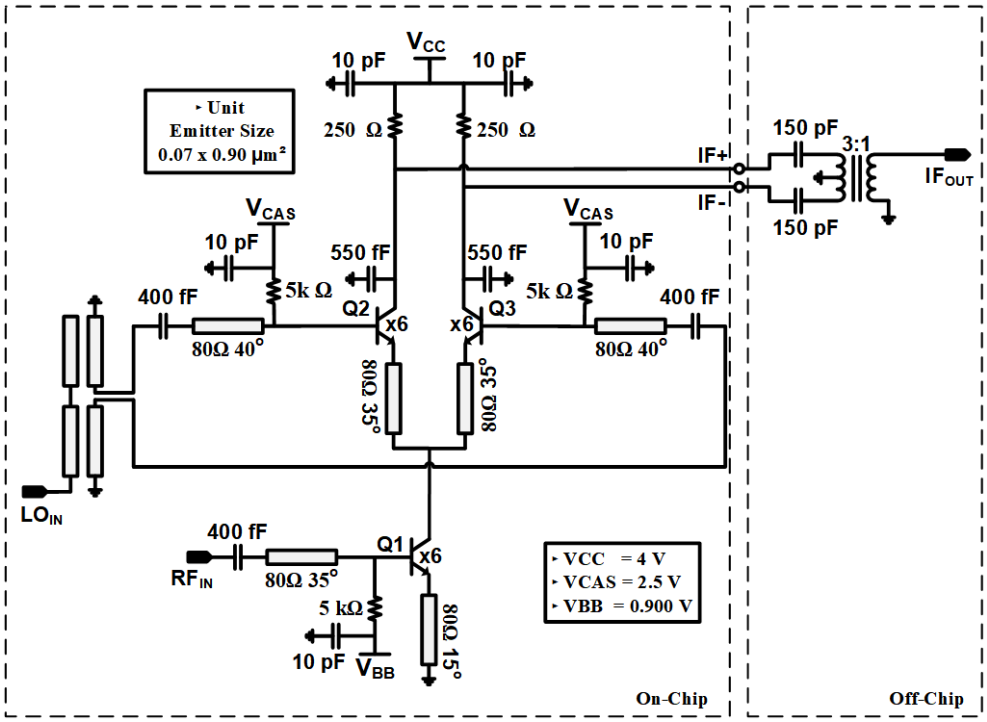

Figure 69 Detailed circuit schematic of the w-band direct down-conversion mixer (Electrical lengths of the transmission lines are given for 94 GHz).

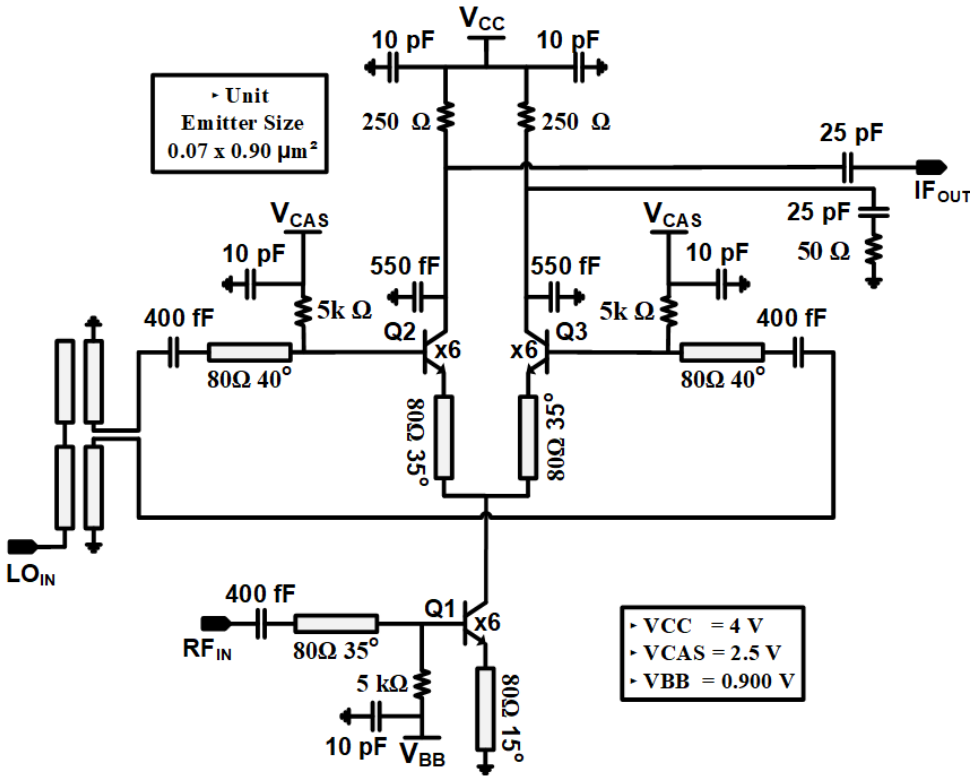

Figure 70 Detailed circuit schematic of the W-band direct down-conversion mixer inserted into the frequency extension module (Electrical lengths of the transmission lines are given for 94 GHz).

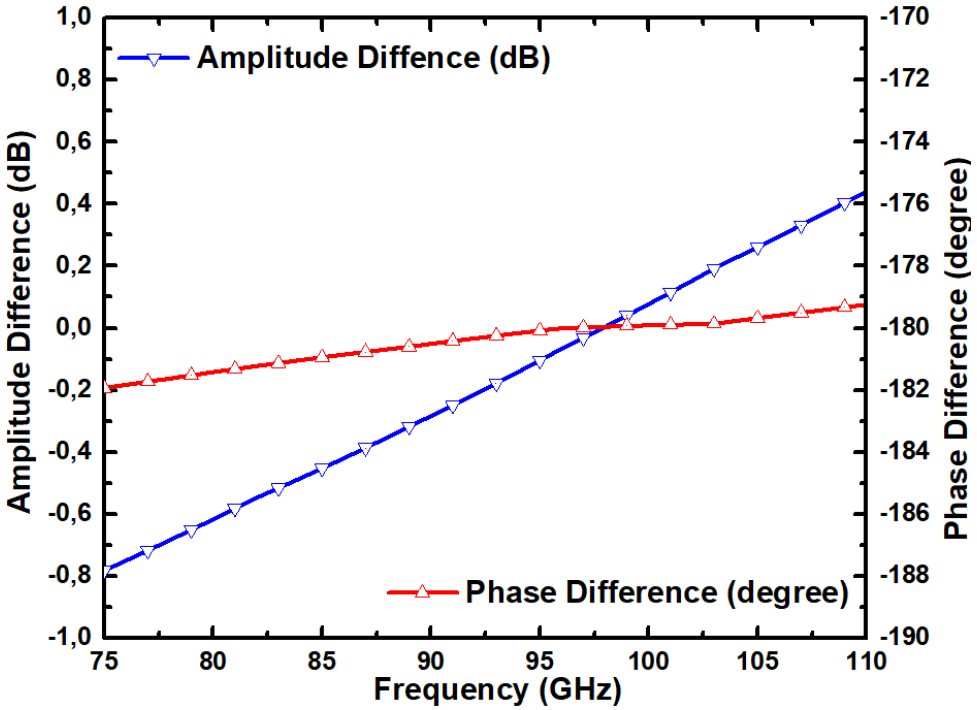

Figure 71 Simulated amplitude and phase balances of the designed Marchand balun.

All the transmission lines were implemented as microstrip lines with Top Metal 2 – Metal 1 configuration. Parasitic capacitances due to the RF pads were included in the RF and LO ports' input impedance matchings. Full-chip electromagnetic (EM) simulations were performed by ADS Momentum. The MIM capacitors were utilized to perform DC-blocking and AC-grounding. The 3D layout view taken from the electromagnetic simulation setup of the W-band single-balanced down-conversion mixer is shown in Figure 72.

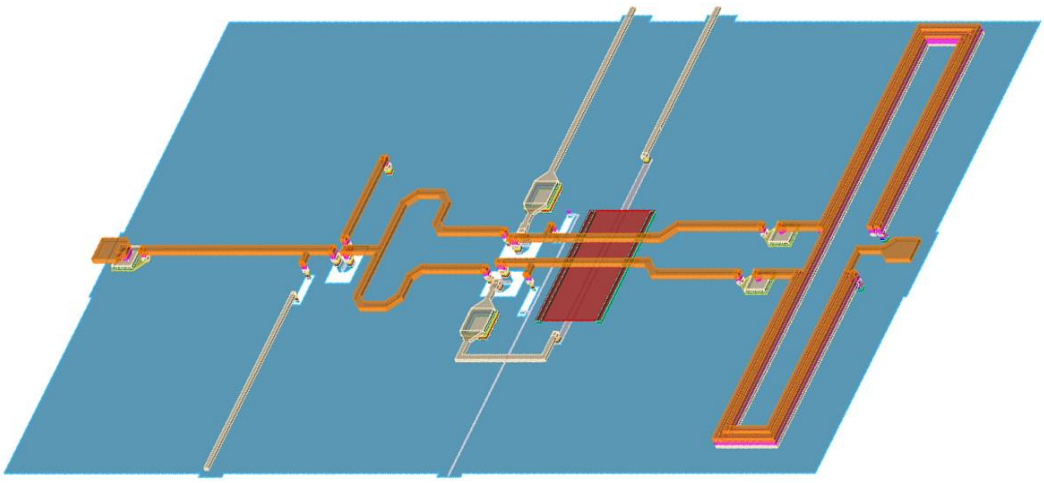

Figure 72 3D layout view taken from EM simulation setup of W-band single-balanced down-conversion mixer.

3.2.2 Simulation and Measurement Results

The chip photo of the designed W-band single-balanced down-conversion mixer is shown in Figure 73. The overall integrated circuit occupies an area of 0.54 mm^2 (0.94 mm × 0.57 mm), the effective chip area, excluding the pads, is 0.37 mm^2 (0.82 mm × 0.45 mm). The total quiescent power consumption is 13.8 mW. As depicted in Figure 69 and Figure 70, two different PCB boards were fabricated. An off-chip wideband (0-1 GHz) IF 3:1 transformer (WBC-3TL) was mounted to one of these and the measurement was taken in this way. On the other PCB board, one of the outputs of the mixer was terminated by discrete 50Ω so that the IF output was measured single-endedly. Figure 74 shows the experimental test setup for the measurements of the W-band down-conversion mixer. Two VDI WR10 frequency extension modules were employed to perform the frequency multiplications of RF and LO signals. In the meantime, Keysight N5224A VNA configurated with these frequency extension modules was used to track the power level at the RF and LO ports of the designed mixer. Since the number of the VNA's signal sources is not enough to perform the measurement of the mixer, an external signal generator, which is Keysight E8257D, was configurated with the VNA using the GPIB interfaces. By this way, the mixer was fed with continuously and simultaneously RF and LO signals. Also, the Keysight E4448A spectrum analyzer was used to determine the power level at the IF output of the designed mixer.

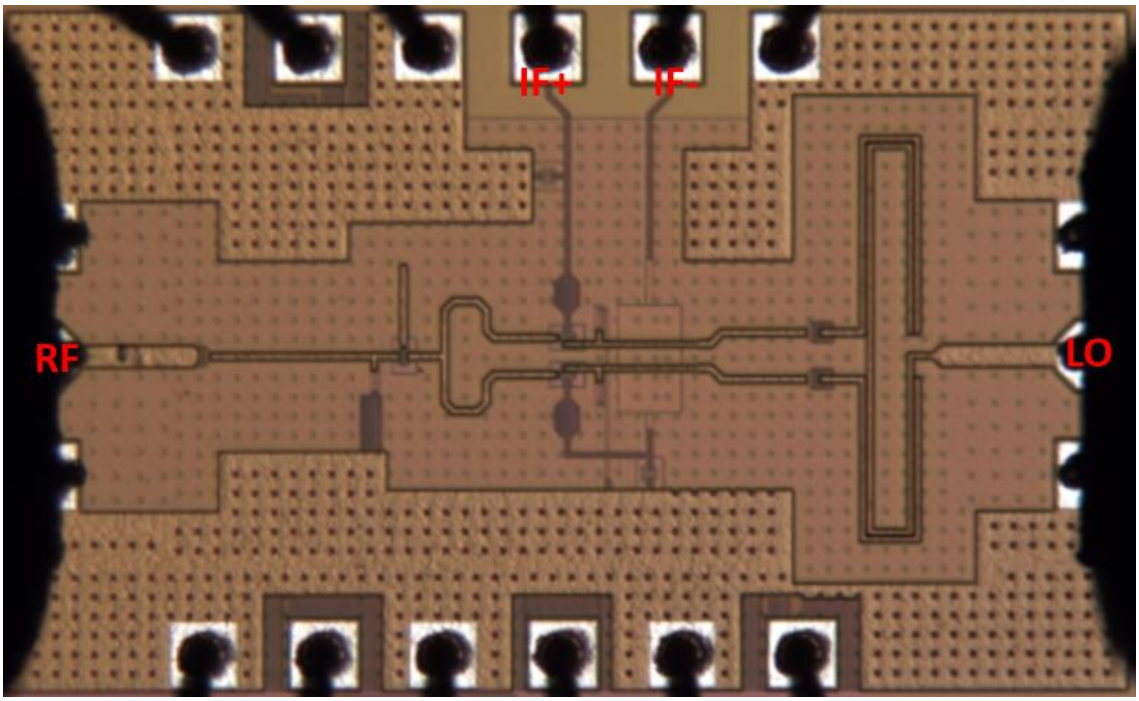

Figure 73 Chip microphotograph of the designed W-band mixer (1.25 mm × 0.8 mm).

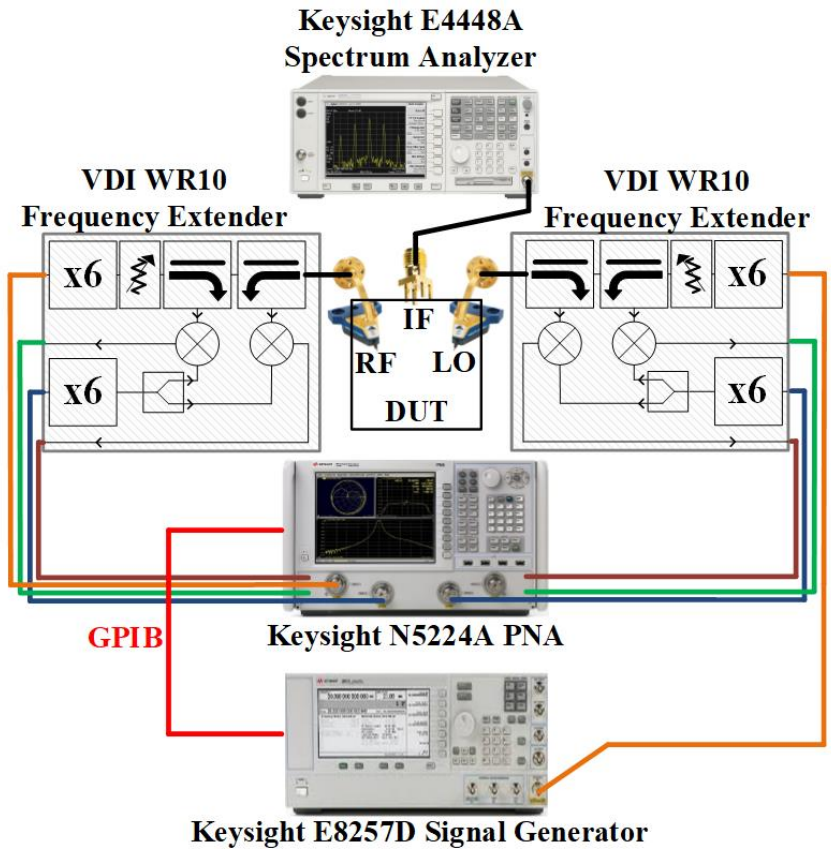

Figure 74 Experimental test setup for the measurements of the designed W-band mixer.

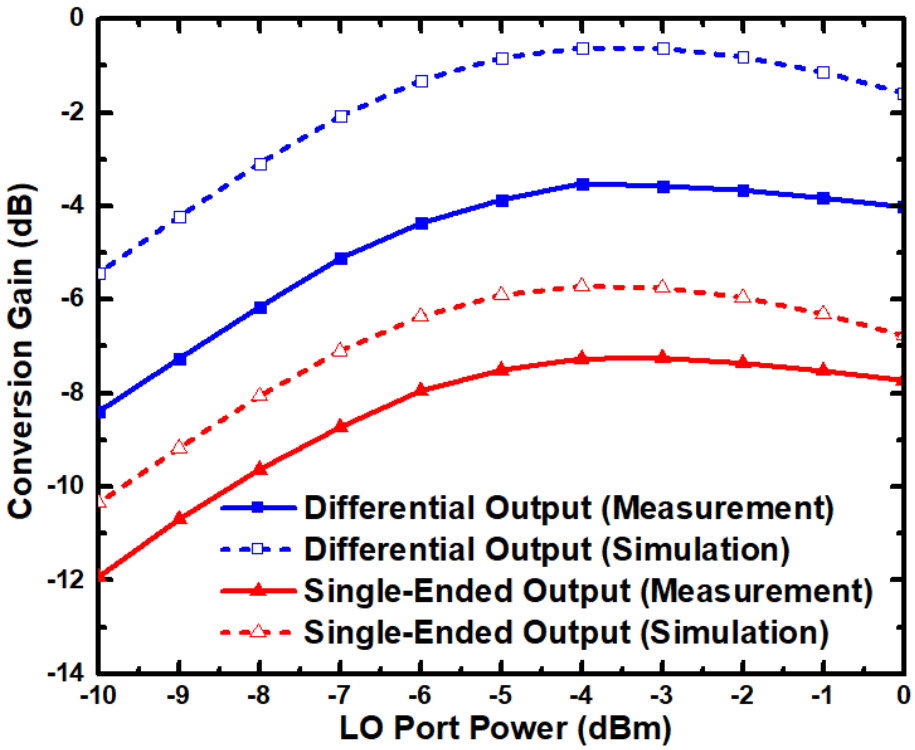

Figure 75 Simulated and measured conversion gains versus LO port power (IF fixed at 300 MHz, and RF fixed at 92.5 GHz).

First, the effect of the LO port power on the conversion gain was examined to find the optimum LO power level of the designed mixer. The frequencies of the RF and LO signals were fixed 92.5 GHz and 92.2 GHz, respectively, to set the IF frequency to be 300 MHz. The power at the LO port of the designed mixer was swept from -10 to 0 dBm with 1 dB steps. Figure 75 shows the simulated and measured conversion gains versus LO port power. The conversion gain steadily increases until the LO power of -4 dBm. The optimum LO power level was found to be -4 dBm for both single-ended and differential output. The conversion gain remains almost constant for the LO power levels of higher than -4 dBm. As can be seen from Figure 75, for single-ended, the difference between the simulated and measured results is about 1.5 dB. This difference can be attributed to the losses of the bond-wire of 5 mm in the package, the SMD dc-blocking capacitor, and the board-to-connector transition. This difference is about 2.8 dB for the differential output, and the difference of 1.3 dB with respect to single-ended version is most likely due to the insertion loss of the used transformer.

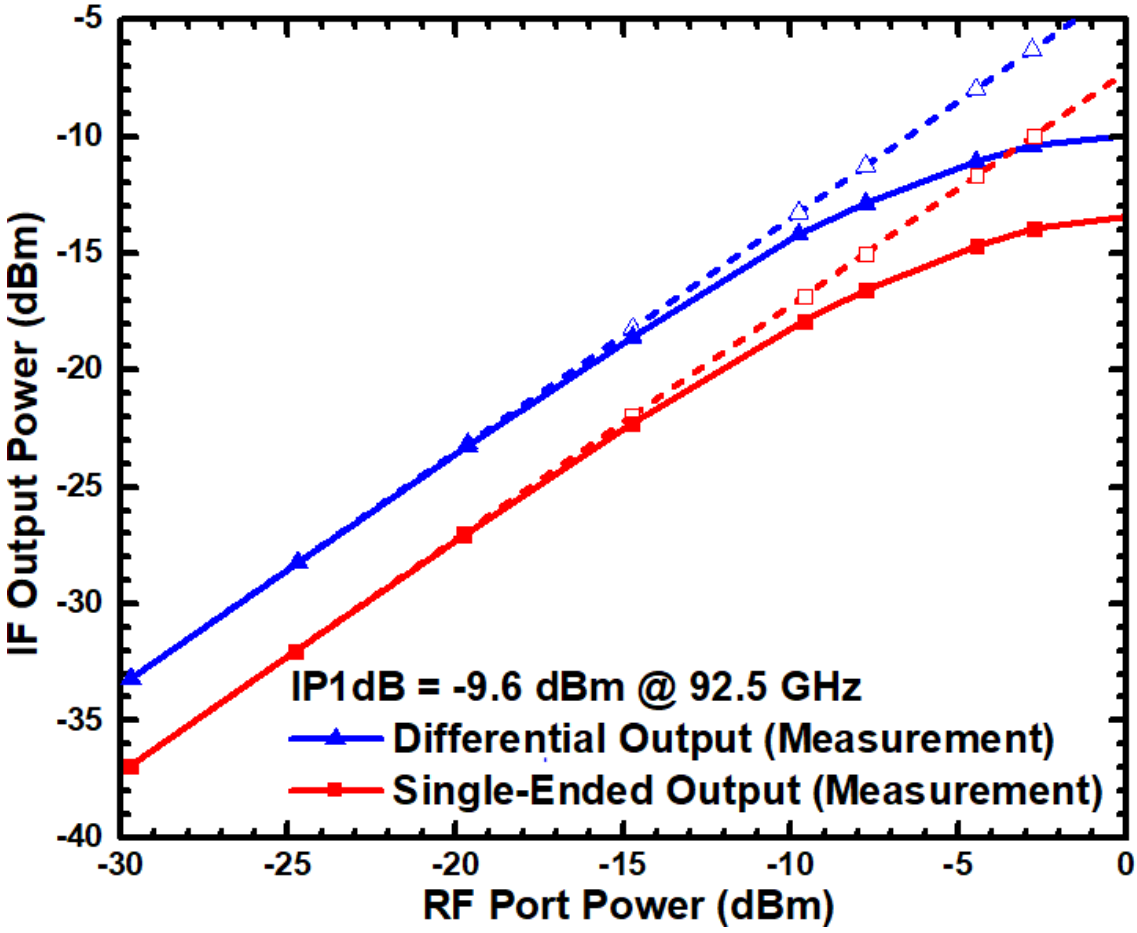

Figure 76 Measured IF output power versus RF port power (IF fixed at 300 MHz, RF fixed at 92.5 GHz, and LO power fixed at -4 dBm).

Second, the input referred 1-dB compression point of the designed mixer was tested. The frequencies of the RF and LO signals were fixed 92.5 GHz and 92.2 GHz, respectively, and the LO port power was fixed to be -4 dBm. Figure 76 shows the measured IF output power versus RF port power. The measured input referred 1-dB compression points of the single-ended and differential output mixers were found to be -9.6 dBm, and it is same for both versions as expected. Third, the difference between the RF and LO frequencies was set to 300 MHz, and the LO port power was fixed to -4 dBm. The RF port power was set to be less than -20 dBm along the W-band to ensure that the mixer does not compress. Figure 77 shows the simulated and measured conversion gain performances across the entire W-band. The measured maximum conversion gains were found to be about -2 dB and -5.7 dB at around 84.5 GHz for the differential output and single-ended mixers, respectively. The conversion gains of them remain above -4.8 dB and -8.2 dB across the whole W-band. It means that both of them achieve a 3-dB bandwidth of at least 35 GHz.

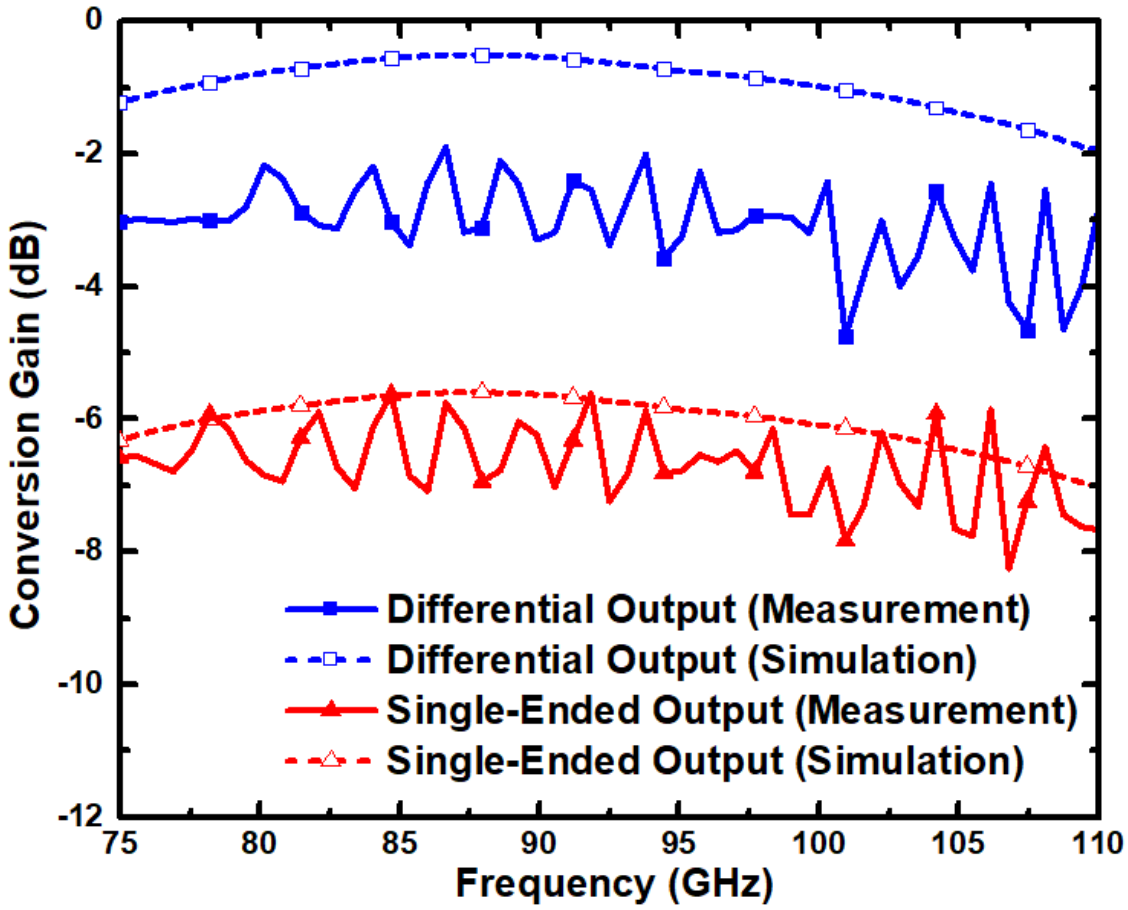

Figure 77 Simulated and measured conversion gains versus RF Frequency (IF fixed at 300 MHz, and LO power fixed at -4 dBm).

S-parameter measurements of the designed W-band down-conversion mixer were performed by Keysight N5224A PNA whose frequency extended to 75-110 GHz using VDI WR10 frequency extension modules, as can be seen from the Figure 74. Two-port SOLT error correction was done using a Cascade-Microtech ISS (138-357) to shift the reference plane to the ports of the designed mixer. The power at the RF input port of the mixer was set to be less than -20 dBm over the W-band to guarantee that the mixer is not compressed, and the LO port power was fixed to be -4 dBm. Also, the frequency of the IF output was fixed to 300 MHz. Figure 78 shows the simulated and measured s-parameters of the input ports of the designed mixer. As can be seen from Figure 78, there is a good match between the simulated and measured s-parameter results of the mixer. The measured return loss of the RF input port of the mixer is better than 10 dB across the W-band. Also, the measured return loss of the LO port is greater than 10 dB in the frequency range of 78 GHz to 110 GHz.

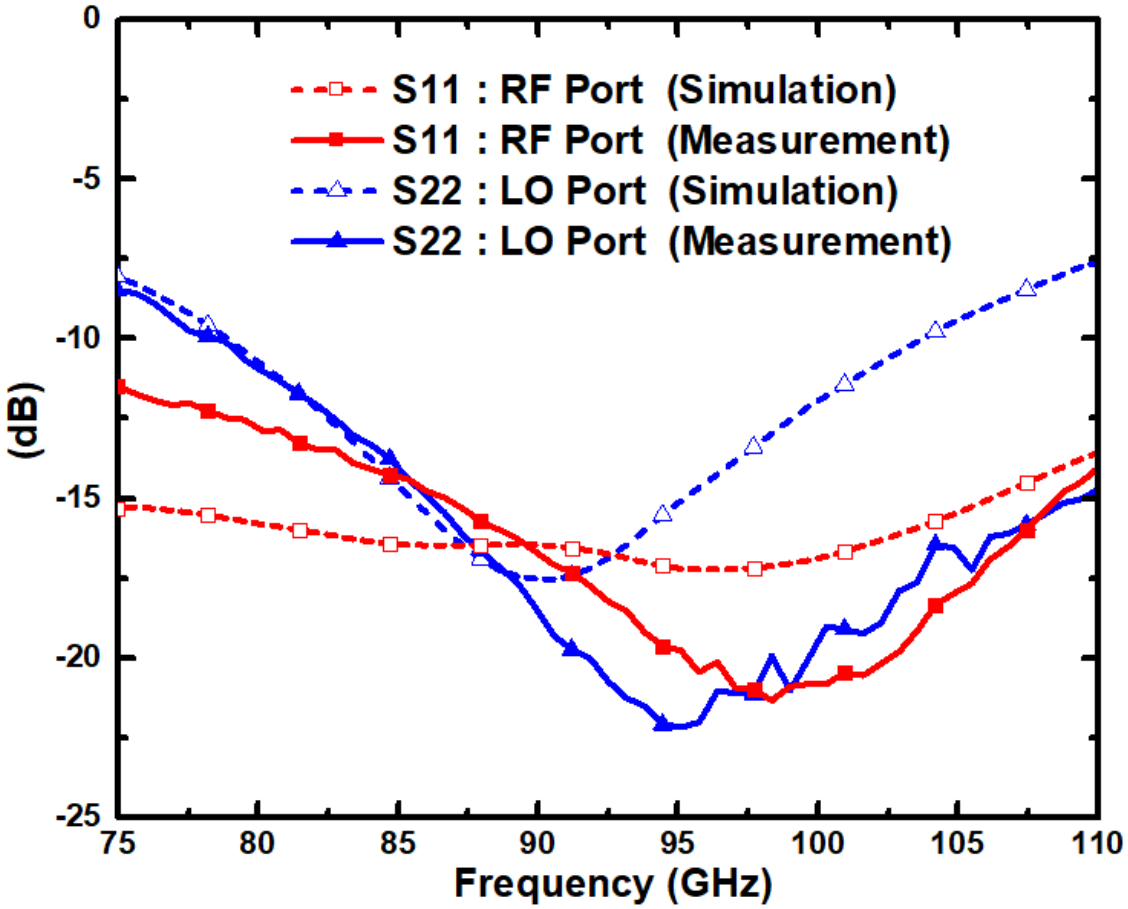

Figure 78 Simulated and measured s-parameters of the input ports of the designed mixer. (IF fixed at 300 MHz, and LO power fixed at -4 dBm).

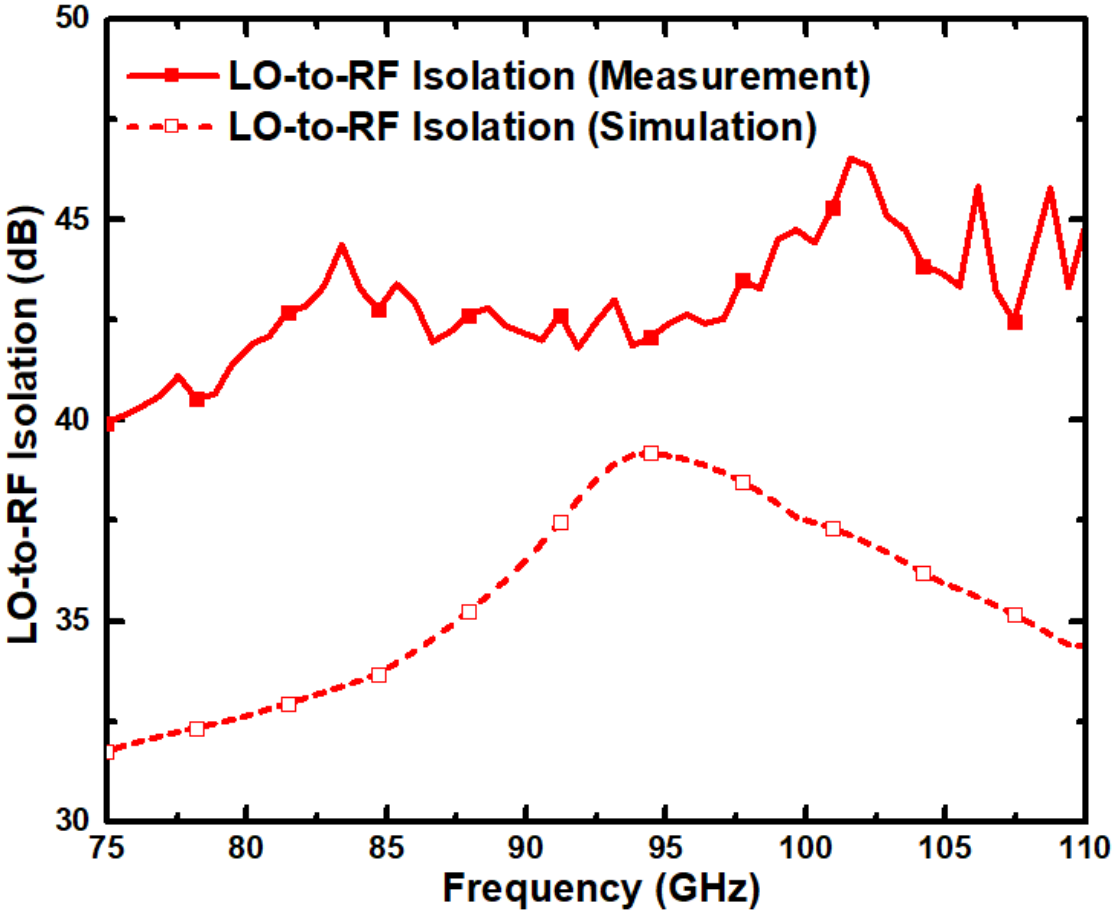

Figure 79 Simulated and measured LO-to-RF isolation of the designed mixer. (IF fixed at 300 MHz, and LO power fixed at -4 dBm).

The simulated and measured LO-to-RF isolation results are presented in Figure 79. The measured LO-to-RF isolation of the mixer is better than 40 dB over the W-band. This discrepancy can be attributed to that the simulation program does not solve the 3D structure of the designed Marchand balun accurately.

3.2.3 Comparison

Table 8 presents the summary of the performance comparison of the designed mixer with previously reported W-band mixers implemented in silicon technologies. All of the published studies, which are included in the comparison, consists of the mixer cores and IF buffer amplifiers. This results in higher conversion gain performance, but it also reduces the input referred 1-dB compression point or increases the DC power consumption. The designed W-band single-balanced down conversion mixer achieves a 3-dB bandwidth of 35 GHz. To the author's best knowledge, the designed mixer is the single work that completely covers whole W-band frequencies.

Table 8 Summary of performance comparison of the designed mixer with previously reported W-band down-conversion mixers implemented in silicon technologies.

	Tech.	**Center Freq. (GHz)**	**Conv. Gain (dB)**	**3-dB BW (GHz)**	**IP_{1dB} (dBm)**	**P_{DC} (mW)**	**P_{LO} (dBm)**
[79]*	0.13μm SiGe BiCMOS	77	0.7	6	-8	22	10
[80]*	0.13μm SiGe BiCMOS	80	3.9	N/A	N/A	2.2	-7
[81]*	0.13μm SiGe BiCMOS	77	20	N/A	-14.7	9.6	-4
[81]*	0.13μm SiGe BiCMOS	94	15	N/A	-10.7	9.6	6
[82]*	0.13μm SiGe BiCMOS	85	10.8	4	N/A	57	-3
This Work	**0.13μm SiGe BiCMOS**	**84.5**	**-2$^{\pm}$ -5.7¶**	**35**	**-9.6**	**13.8**	**-4**

* Including IF buffer amplifier.
± Including off-chip 3:1 transformer.
¶ Single-ended, one of the outputs is terminated by 50Ω.

3.3. Frequency Quadrupler

3.3.1 Circuit Design and Implementation

Frequency multipliers, which perform the frequency multiplication operations, are one of the essential blocks in the RF front-end circuits. The detailed circuit schematic of the designed frequency multiplier is presented in Figure 80. An active balanced frequency multiplier configuration was utilized to perform the multiplication of the frequency of the input signal by four. That is also why it is termed as "frequency quadrupler". The designed frequency quadrupler, which consists of a transformer based passive balun and differential transistor pair, receives the signals between 18 and 28 GHz (K-band) and then produces signals between 72 and 112 GHz (W-band) using their fourth harmonics. Therefore, the input part of the circuit was optimized for the K-band, and the output part of the circuit was designed for the W-band. The unbalanced input signal is converted to a balanced signal through the transformer based passive balun. The 3D layout view of the

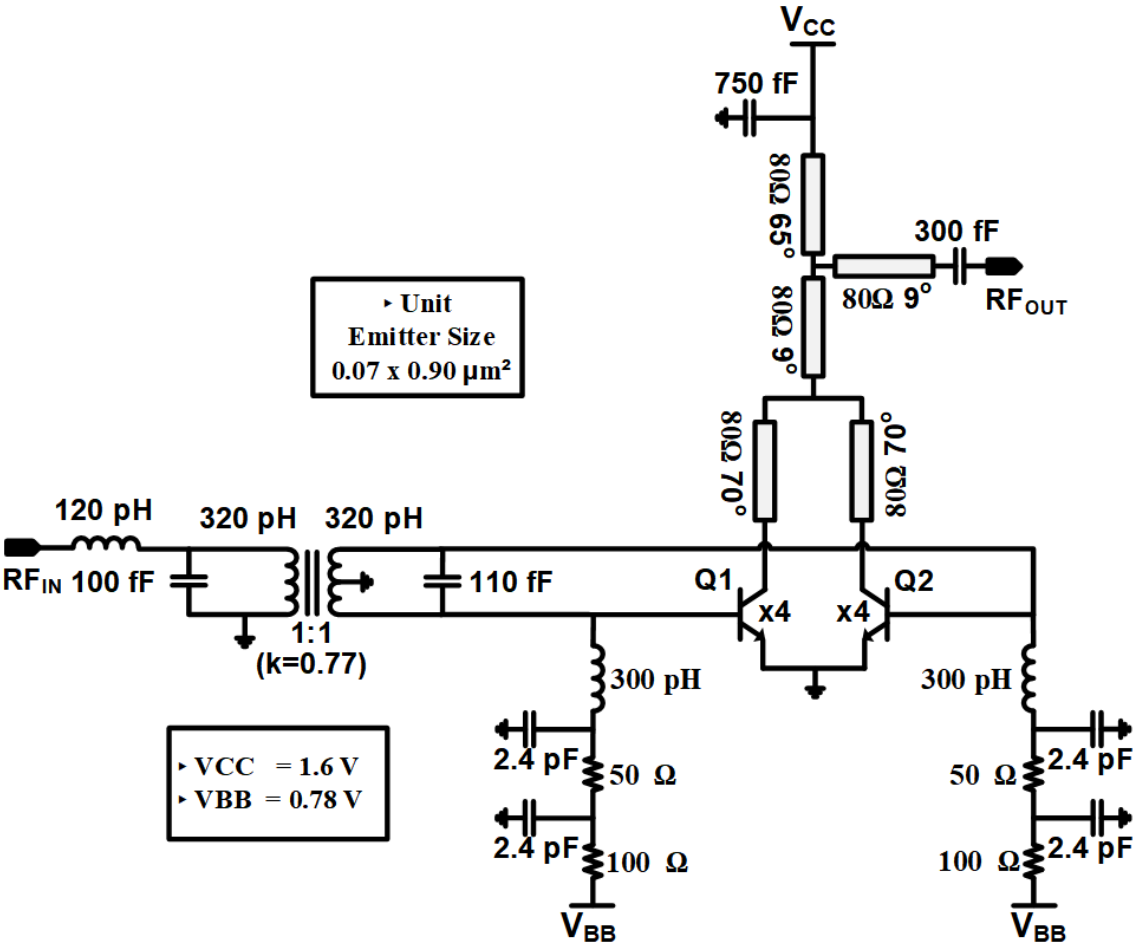

Figure 80 Detailed circuit schematic of the designed frequency quadrupler (Electrical lengths of the transmission lines are given for 94 GHz).

designed balun is shown in Figure 81. Two different conductor layers (Top Metal-2 and Top Metal-1 for the primary and secondary windings, respectively) were utilized to implement the overlay transformer with a k-factor of 0.77 [83]. The self-inductances of the primary and secondary windings are approximately 320 pH so that the turn ratio of the transformer is unity (1:1). Figure 82 shows the EM simulation results of the amplitude and phase differences of the transformed. The amplitude difference is less than 0.25 dB, and the phase difference is approximately 180° across the entire the frequency range of 18 to 28 GHz with an error of less than 0.5°. The transistors in the quadrupling stage (Q1 and Q2) were biased at the Class-B bias point to enrich their output currents in terms of harmonic contents [84]. The number of the transistors were determined to be x4 by considering the output power and the input matching. The optimum power value of the input signal was found to be 5 dBm, taking the loss of the passive balun into account. The collector nodes were connected to each other to combine the even harmonics, and this

node will be virtual ground for the odd harmonics so that the odd harmonics can be significantly suppressed [85]. The third and fifth harmonics of the frequency qudrupler would cause significant degradation in the accuracy of the measurement that would be performed by the frequency extension module since they will also be in the frequency range of interest. Therefore, the elimination of the odd-harmonics is very important to reduce the systematic errors in the s-parameter measurement. This is also the most important reason for choosing the balanced configuration in the frequency multiplication.

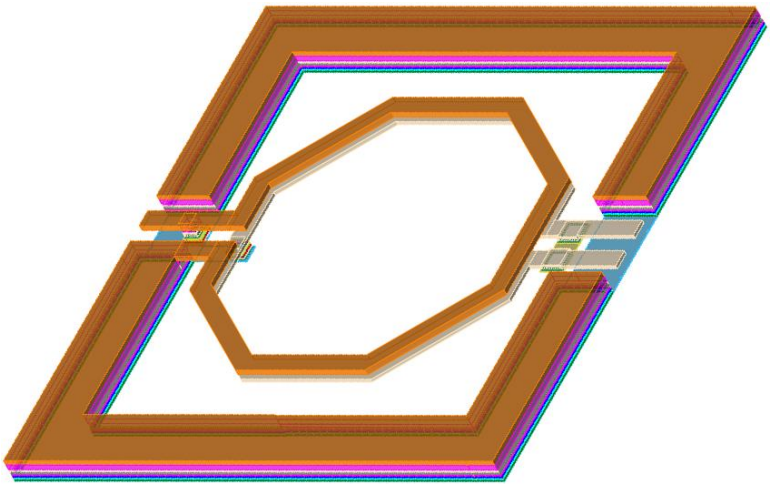

Figure 81 3D layout view taken from EM simulation setup of the designed K-band transformed based balun.

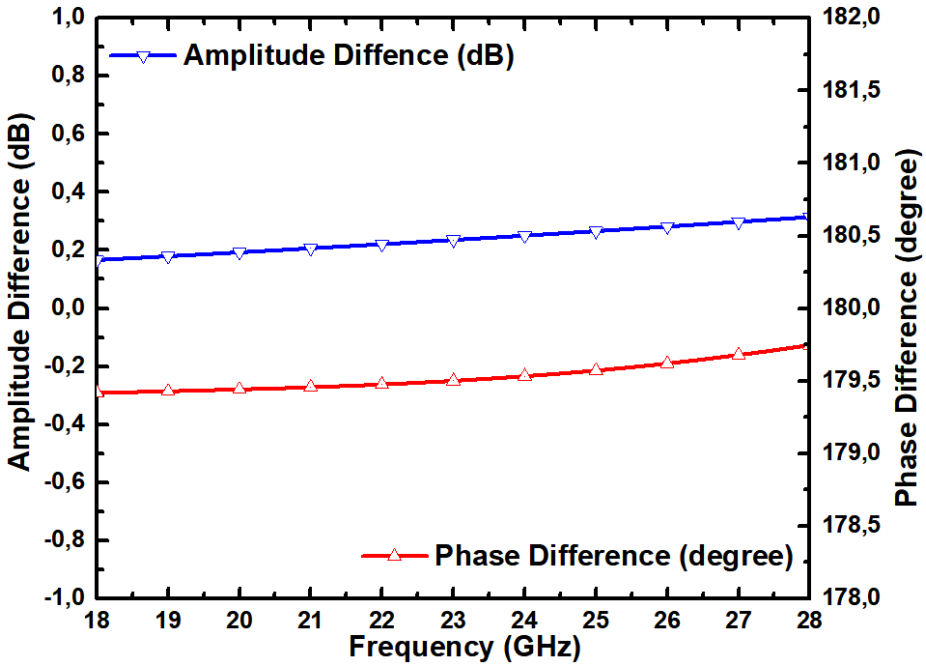

Figure 82 Simulated amplitude and phase balances of the designed K-band transformed based balun.

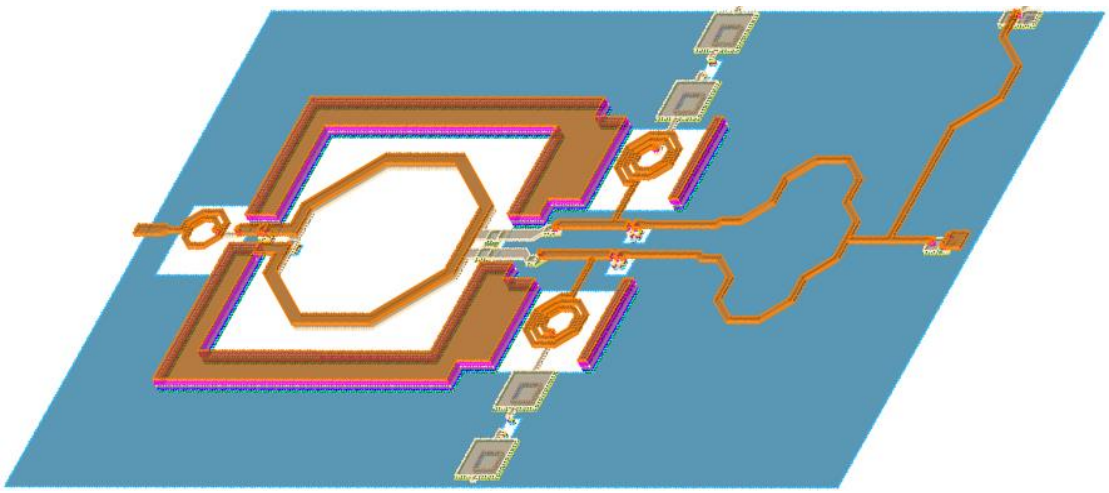

Figure 83 3D layout view taken from EM simulation setup of the frequency quadrupler.

Efforts were made to ensure that the circuit is as symmetrical as possible throughout the design of the frequency quadrupler circuit. All the transmission lines were implemented in microstrip from with a Top Metal 2 – Metal 1 configuration. Parasitic capacitances due to the RF pads were included into the input and output impedance matching networks. Full-chip electromagnetic (EM), harmonic-balance and transient simulations were performed on ADS Momentum. The MIM capacitors were used to perform DC-blocking on the signal paths and bypassing on the feed lines. The 3D layout view taken from the electromagnetic simulation setup of the designed balanced frequency quadrupler is shown in Figure 83.

3.3.2 Simulation and Measurement Results

Figure 84 shows the micrograph of the designed frequency quadrupler circuit. The total IC occupies an area of 0.56 mm^2, and the effective area is 0.41 mm^2, excluding the pads. The total power consumption is 44.8 mW while applying an RF input signal of 5 dBm. S-parameter measurement of the frequency quadrupler circuit was performed by Keysight N5224A PNA. One-port SOL calibration was performed by as ISS from Cascade-Microtech to move the reference plane to the probe tip. The power at the probe tip was set to be approximately 5 dBm at the center of the W-band. The simulated and measured s-parameters of the frequency quadrupler circuit were presented in Figure 85. The measured S11 is better than -5 dB along the entire W-band. The simulated and measured output powers (4^{th} harmonic) of the frequency quadrupler were shown in Figure 86. The measured peak output power is about 1.5 dBm at 95 GHz, and it is greater than -6 dBm over the W-band. Figure 87 shows the simulated and measured harmonic levels relative to the 4^{th} harmonic signal. The second, third and fifth harmonics could not be measured

since our measurement setup does not cover the frequency ranges of these harmonics. The fundamental signal is suppressed better than 28.5 dB along the W-band.

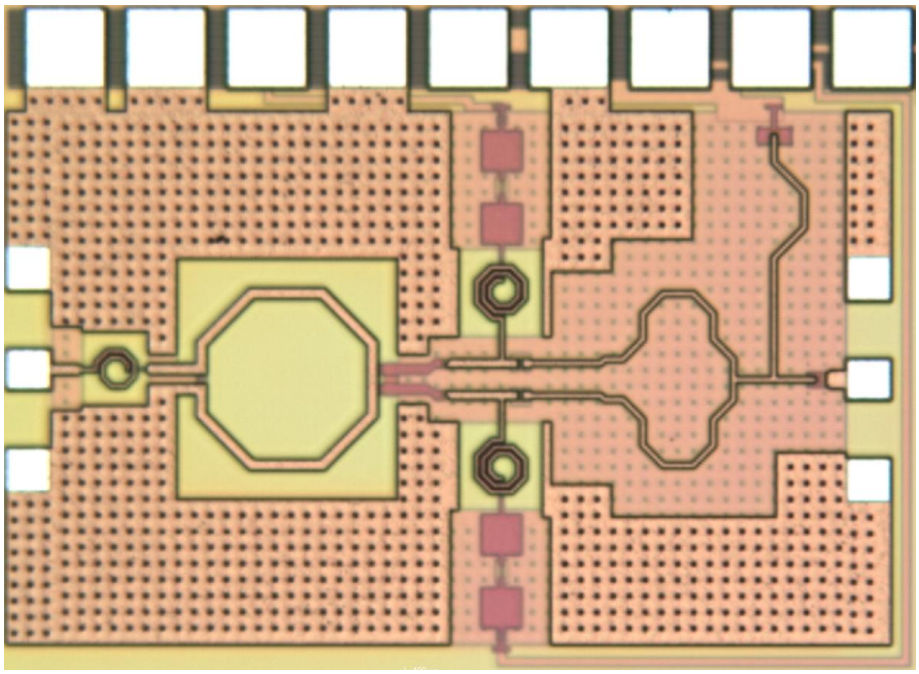

Figure 84 Chip micrograph of the designed frequency quadrupler circuit (0.89 mm × 0.63 mm).

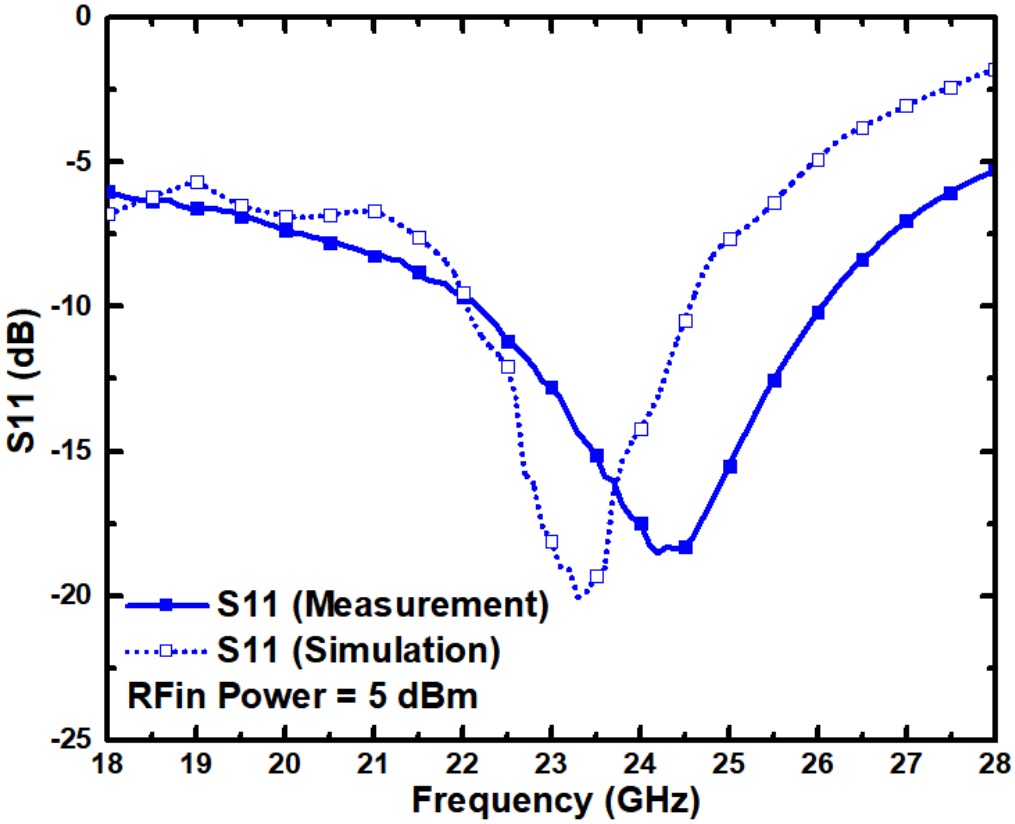

Figure 85 Simulated and measured s-parameter results of the frequency quadrupler.

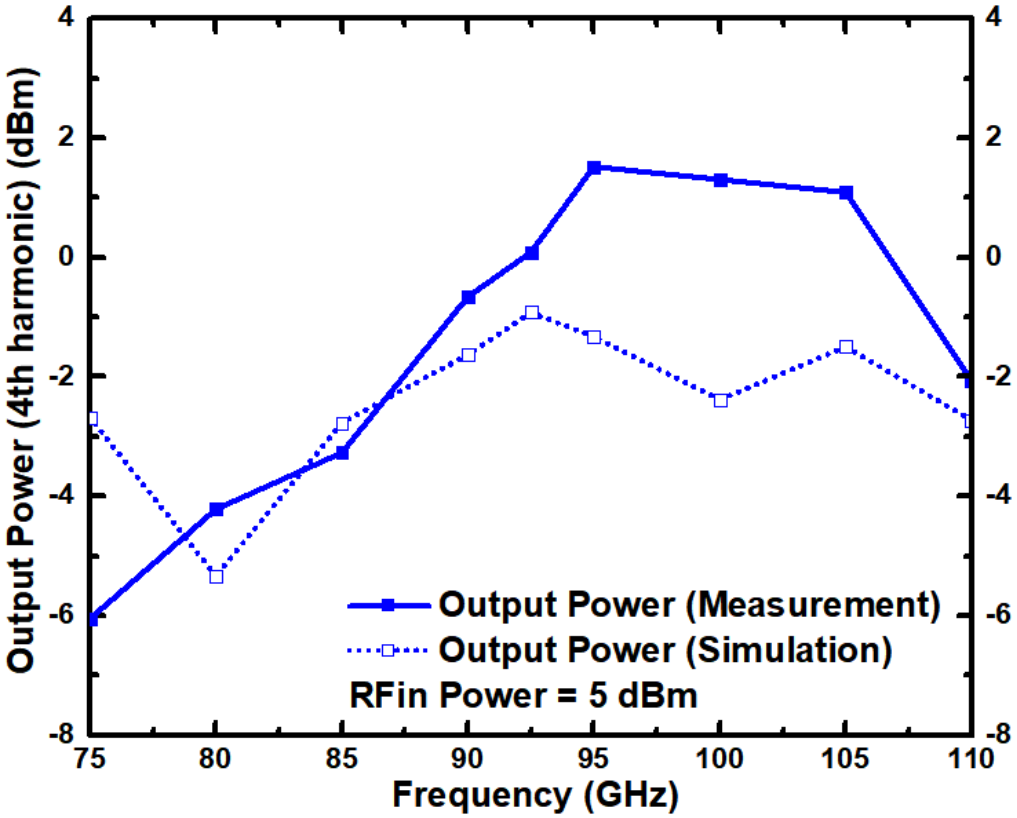

Figure 86 Simulated and measured output power of the frequency quadrupler.

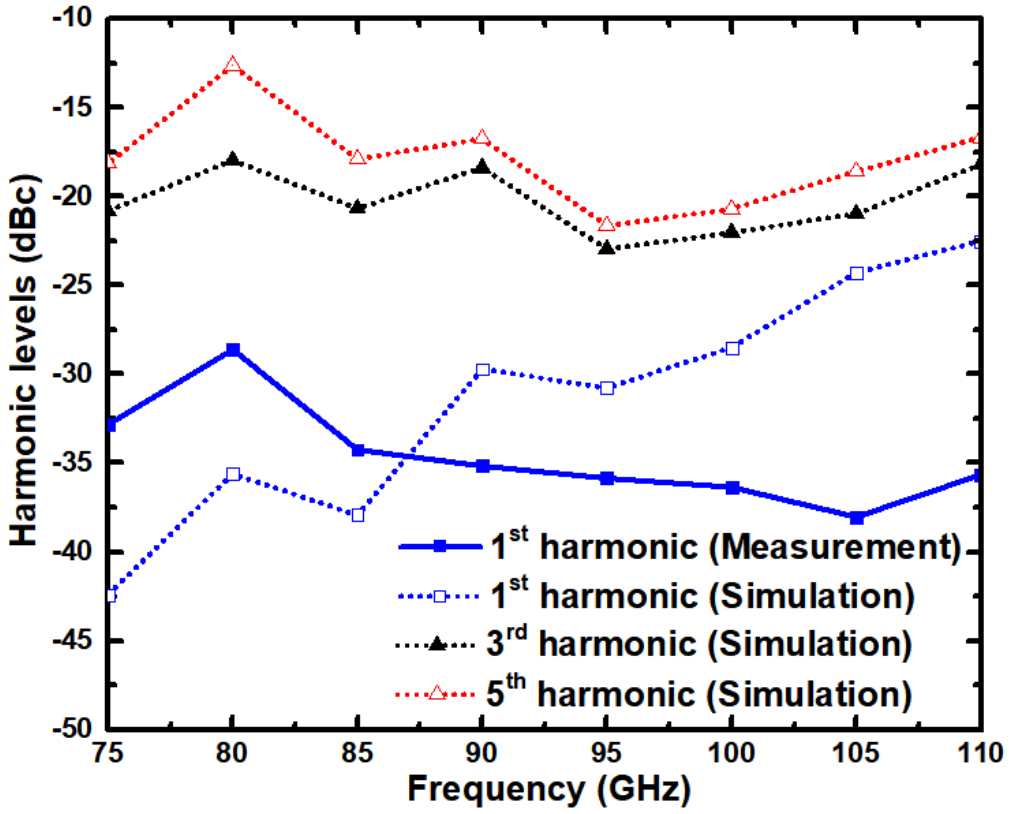

Figure 87 Simulated and measured output harmonic levels of the frequency quadrupler.

3.3.3 Comparison

The performance comparison of the designed frequency quadrupler with previously reported W-band frequency multipliers implemented in silicon technologies is summarized in Table 9**.** It achieves the maximum output power compared to other frequency multiplier circuits implemented in silicon technologies.

Table 9 Summary of performance comparison of the designed frequency quadrupler with previously reported W-band frequency multipliers implemented in silicon technologies.

	Tech.	**Freq. (GHz)**	**xN**	**P_{in} (dBm)**	**P_{out} (dBm)**	**f_0 sup. (dB)**	**P_{DC} (mW)**
[86]	65nm CMOS	73-88	x2	-4	-3.2∼-8.2	>19	14
[87]	65nm CMOS	75-110	x2	5	-11	>20	13.8
[88]	65nm CMOS	75-110	x4	10	-14.3	>30	16
[89]	0.18μm SiGe BiCMOS	80-100	x3	0	-10.5	>20	78
This Work	**0.13μm SiGe BiCMOS**	**75-110**	**x4**	**5**	**1.5∼-6**	**>28.5**	**44.8**

3.4. Buffer Amplifiers

3.4.1 Circuit Design and Implementation

The input impedance of the following stage of the frequency quadrupler has a significant impact on the output power of the frequency quadrupler circuit. This would significantly reduce the accuracy of the s-parameter measurement since the input impedance of the device under test would change the output power of the frequency quadrupler at the RF path of the frequency extension module. Therefore, an amplifier with high reverse isolation was employed as a buffer stage to eliminate the dependence of the output power of the frequency quadrupler on the input impedance of the following stage. A cascode configuration was utilized to acquire high reverse isolation performance since the cascode transistor reduces the effect of the C_μ the capacitance of the CE transistor on the overall transfer function of the amplifier.

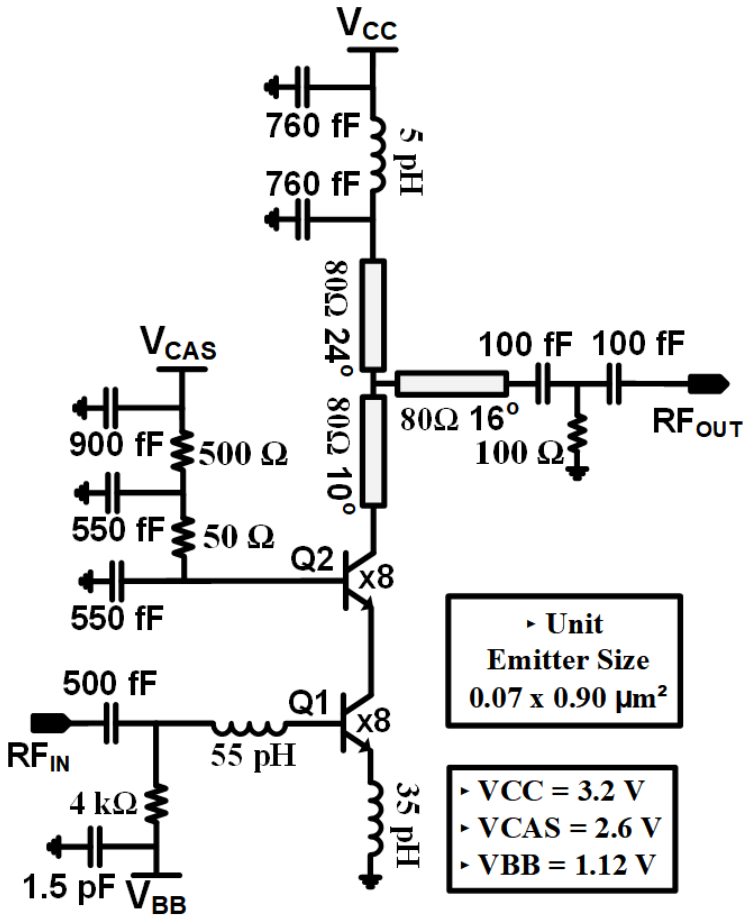

Figure 88 Detailed circuit schematic of the single-stage W-band buffer amplifier, which is at the RF path. (Electrical lengths of the transmission lines are given for 94 GHz).

Figure 88 shows the detailed circuit schematic of the designed single-stage W-band amplifier which is used at the RF path. As presented in Section 3.3, the simulation results show that the average output power of the frequency quadrupler circuit is around -3 dBm over the W-band. A power of 0 dBm at the output of the frequency extension module was aimed to achieve a high dynamic range. Therefore, assuming an insertion loss of 2 dB for the dual-directional coupler, the amplifier should have a gain of 5 dB with an input 1-dB compression point greater than -3 dBm. For this reason, the collector current was set to provide the required input 1-dB compression point and required gain, and it was also optimized to not increase the noise figure too much for the unit emitter size. The number of the transistor was found to be x8 considering the required output power level. The inductive emitter degeneration (35 pH) was utilized to set the real part of the input impedance to 50Ω. The imaginary part of the input impedance was canceled out using a series inductor of 55 pH at the base of the CE transistor. It should be also noted that the

designed amplifier behaves as a band-pass filter for W-band. By this way, the second harmonics of the frequency quadrupler (36-56 GHz) are suppressed.

As stated in Section 3.2, the optimum power of the LO signal of the designed mixer was found to be -4 dBm, according to simulation results, and the conversion gain of the mixer remains almost constant for LO power of greater than -4 dBm. Assuming an insertion loss of 3.5 dB for the power divider which is at the LO path of the frequency extension module, and an insertion loss of 2 dB due to the interconnection transmission lines, the output power of the buffer amplifier at the LO path must be at least 1.5 dBm across the entire W-band.

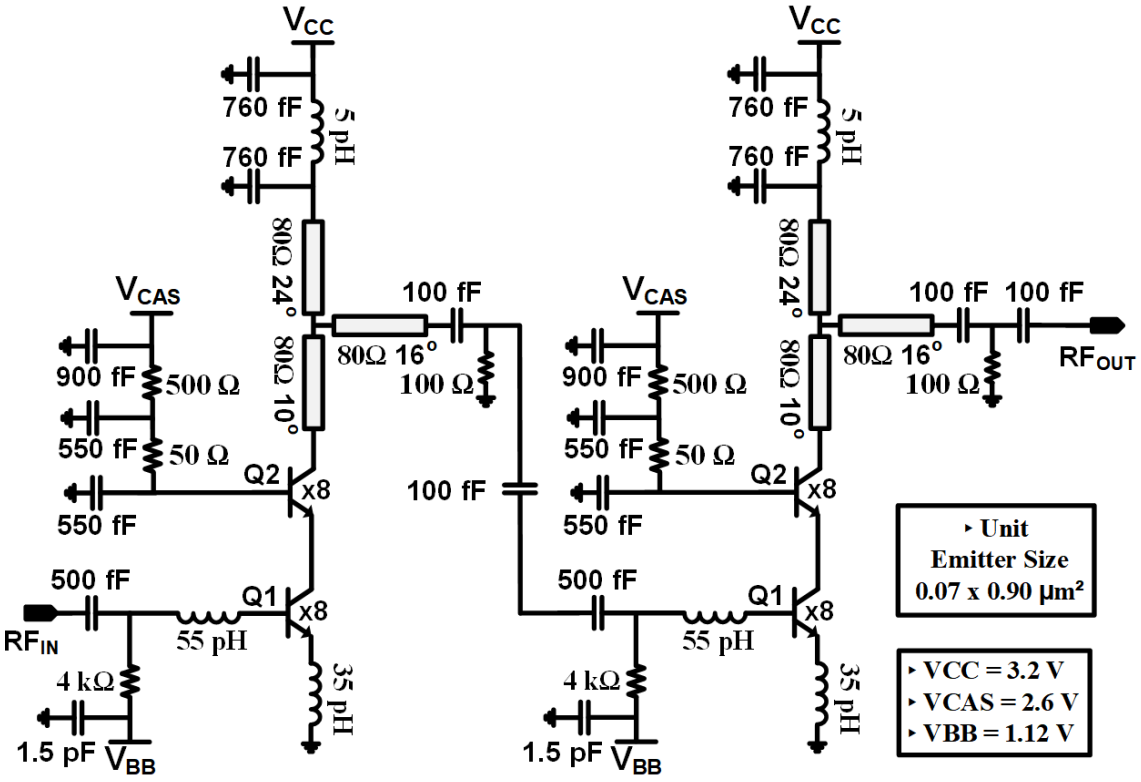

Figure 89 Detailed circuit schematic of the double-stage W-band buffer amplifier, which is at the LO path. (Electrical lengths of the transmission lines are given for 94 GHz).

The simulation results of the frequency quadrupler show that the minimum output power is around -4.5 dBm across the W-band. Therefore, the buffer amplifier should have a minimum gain of 6 dB and an output 1-dB compression point greater than 1.5 dBm. Taking into account a deviation of 2 dB which may occur in these performance specifications after fabrication, a double-stage buffer amplifier was designed by cascading the single-stage amplifier which is used at the RF path. Figure 89 shows the

circuit schematic of the double-stage buffer amplifier which is used at the LO path of the frequency extension module.

All the transmission lines were implemented in microstrip form with Top Metal 2 – Metal 1 configuration and all of them were meandered to reduce the chip area. The inductors were implemented using the Top Metal 2 layer. Parasitic capacitances due to the RF-pads were included in the input and output impedance matchings. The MIM capacitors were used to perform DC-blocking and AC-grounding. ADS momentum was used to perform the full-chip electromagnetic (EM) simulations. Figure 90 shows the 3D layout view taken from the electromagnetic simulation setup of the designed single-stage amplifier.

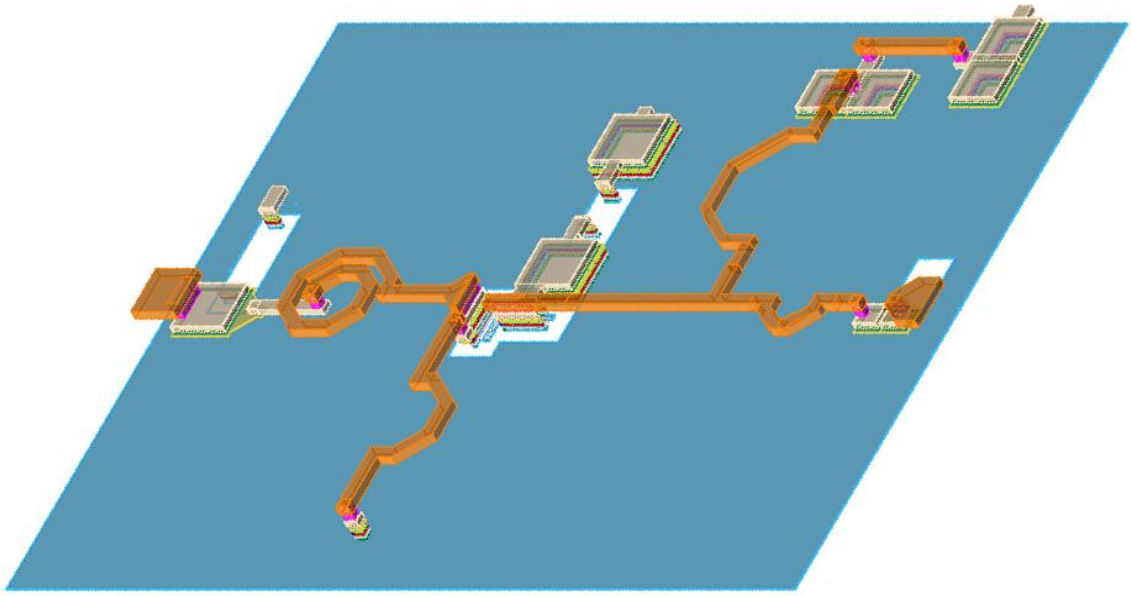

Figure 90 3D layout view taken from EM simulation setup of the single-stage W-band buffer amplifier.

3.4.2 Simulation Results

Figure 91 shows the simulated s-parameter results of the single-stage W-band buffer amplifier. The maximum gain is approximately 5.8 dB at 100 GHz, and its minimum value is 4.5 dB across the W-band. The input return loss is better than 12 dB over the whole W-band, and the output impedance matching can be considered as an acceptable level. The reverse-isolation is about 32 dB along the frequency range of interest thanks to that the cascode topology eliminates the effect of the CB capacitance of the CE transistor. The relationships between the input and output power of the single-stage and double stage amplifiers are depicted in Figure 92. As can be seen from the figure, both amplifiers have a saturated output power of 6 dBm. The input referred 1-dB compression

points of the single-stage, and double-stage amplifiers are -1.5 dBm and 6.5 dBm, respectively.

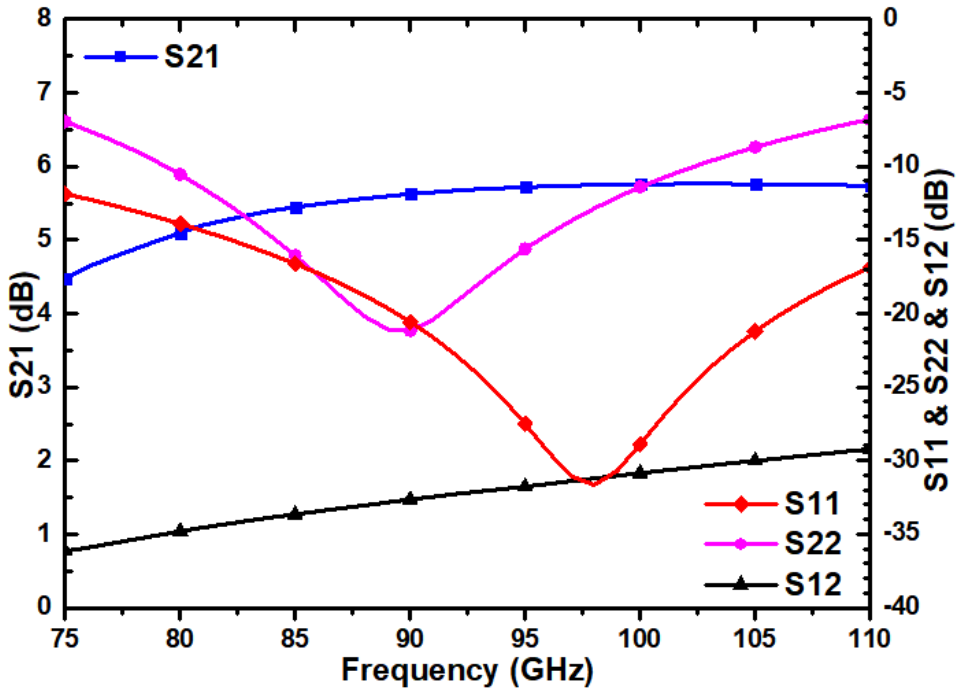

Figure 91 Simulated s-parameter results of the single-stage buffer amplifier.

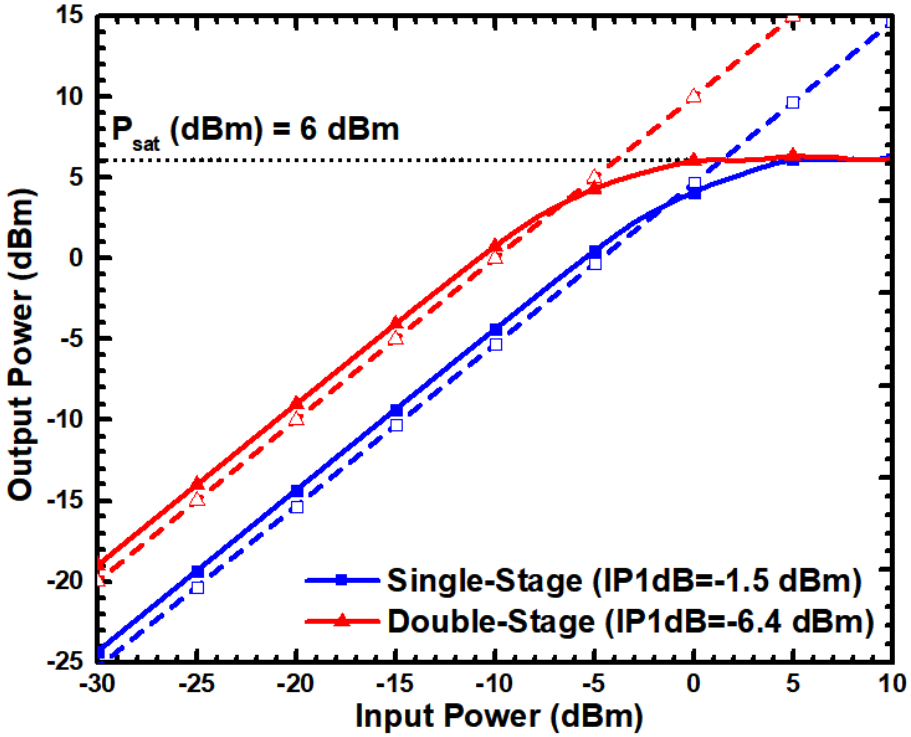

Figure 92 Simulated input power versus output power of the single-stage and double-stage amplifiers.

3.5. Dual-Directional Coupler

3.5.1 Circuit Design and Implementation

A directional coupler is a four-port passive circuit that samples the incident wave to the coupling port. The directivity of the coupler, which is used in the reflectometer part to sample transmitted and reflected signals, has a significant impact on the accuracy of the s-parameter measurement [90].

As shown in Figure 93, a quarter-wave coupled transmission line can be utilized to build a directional coupler by terminating the isolated port (4^{th} port) with a 50Ω impedance, but it allows sampling only in one direction. On the other hand, a quarter-wave coupled transmission line can be also employed to sample both forward and reverse directions simultaneously. However, in this configuration, the isolation, hence directivity, of the coupler depends on the impedance matchings at the coupling ports. An impedance mismatch at the coupling ports would significantly degrade the directivity of the coupler. For this reason, two directional couplers were connected back to back by terminating their isolation ports with on-chip resistors of 50Ω in order to eliminate the dependence of the directivity on the port matchings, and this coupler configuration is known as dual-directional coupler.

The even and odd characteristic impedances of the coupled lines were determined to obtain a coupling of 10 dB [91]. The 3D layout model of the implemented dual-directional coupler is presented in Figure 94. The coupled transmission lines were implemented using microstrip lines with Top Metal 2 and Metal 1 configuration, and they were meandered to reduce overall area. Full-chip electromagnetic (EM) simulations were done using ADS Momentum.

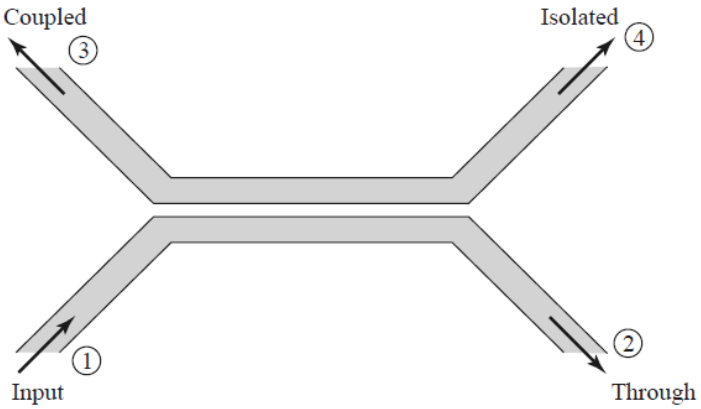

Figure 93 A single-section coupled-line based directional coupler [91].

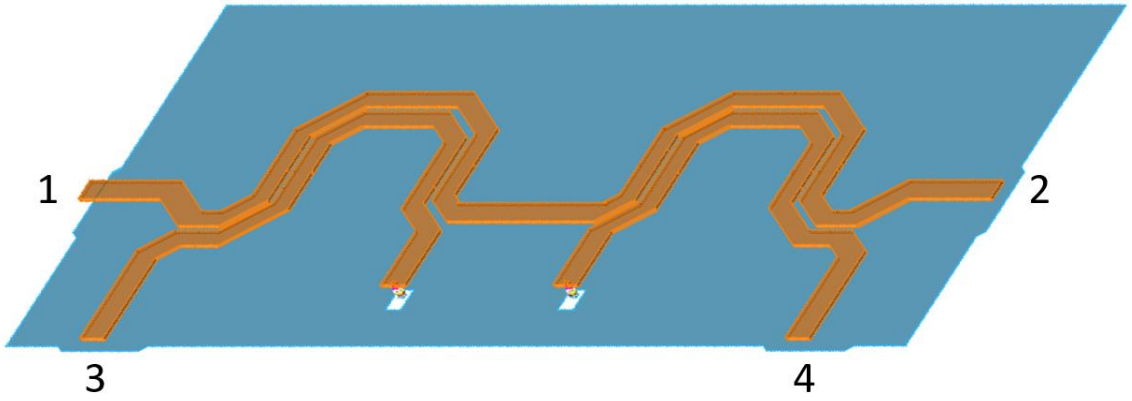

Figure 94 3D layout view taken from EM simulation setup of the W-band dual-directional coupler.

3.5.2 Simulation Results

The simulated insertion loss and coupling values of the designed dual-directional coupler is presented in Figure 95. The insertion loss is about 1.7 dB, and the average coupling value is approximately 10.2 dB across the W-band. Figure 96 shows the isolation and directivity of the designed dual-directional coupler. The directivity is around 20 dB over the W-band.

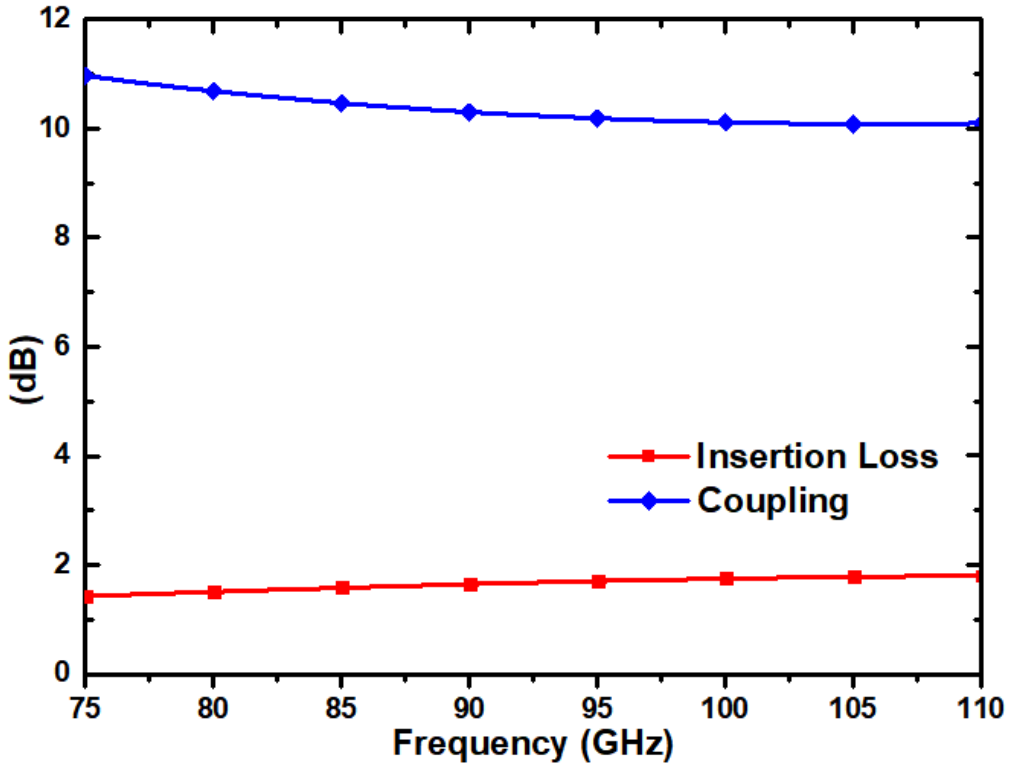

Figure 95 Simulated insertion loss and coupling performances of the dual-directional coupler.

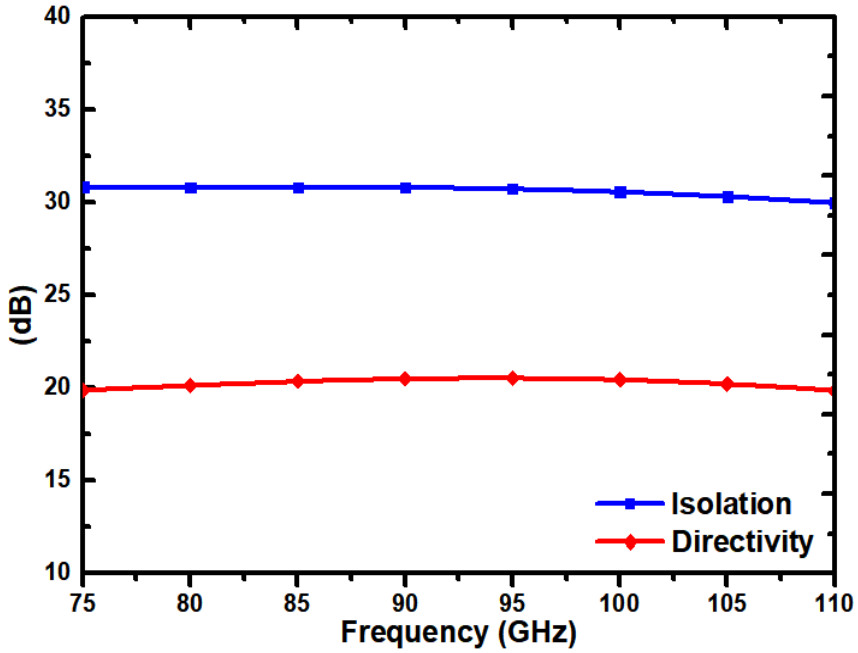

Figure 96 Simulated isolation and directivity results of the dual-directional coupler.

3.6. Wilkinson Power Divider

3.6.1 Circuit Design and Implementation

A Wilkinson power divider is a three-port passive circuit that splits the incident wave into two equal-phase output waves. The Wilkinson power divider can be also utilized to split the incoming signal into different amounts [91], but an equal division was utilized for this design. s powers arbitrary. It consists of two quarter-wave transmission line transformers and a resistor of 100Ω between the output ports.

Figure 97 shows the circuit schematic of the designed W-band Wilkinson power divider. The 3D layout model of the implemented power divider is shown in Figure 98. quarter-wave transmission lines were implemented using microstrip lines using Top Metal 2 and Metal 1 configuration, and they were meandered to avoid the large area. Full-chip electromagnetic (EM) simulations were performed using ADS Momentum.

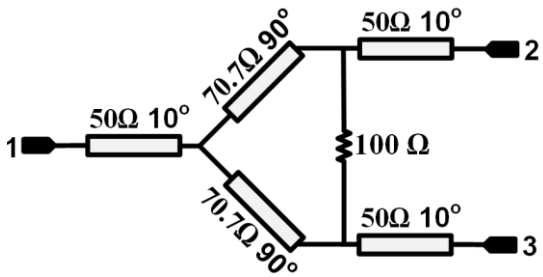

Figure 97 Circuit schematic of the designed Wilkinson power divider.

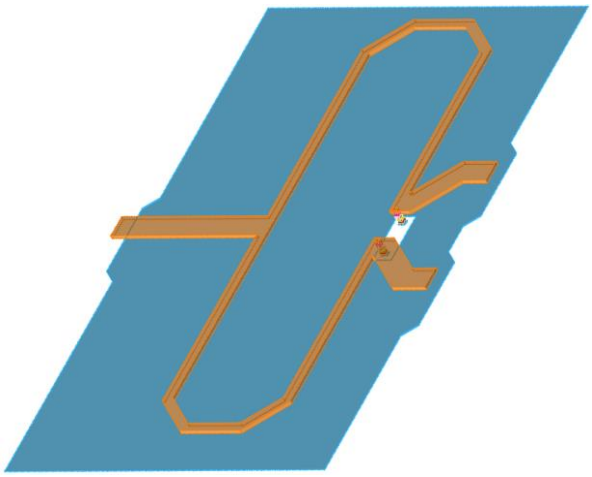

Figure 98 3D layout view was taken from the EM simulation setup of the W-band dual directional coupler.

3.6.2 Simulation Results

Figure 99 shows the simulated insertion losses and isolation results of the W-band Wilkinson power divider. The insertion loss is approximately 3.45 dB across the whole W-band, and as can be seen, the power split ratio is almost the same. The maximum isolation was found to be almost 33 dB, and its minimum value is 18.5 dB at the lower edge of the frequency range of interest. As can be seen from the Figure 100, which presents the simulated return losses performance of the power divider, the port impedances pretty match to 50Ω.

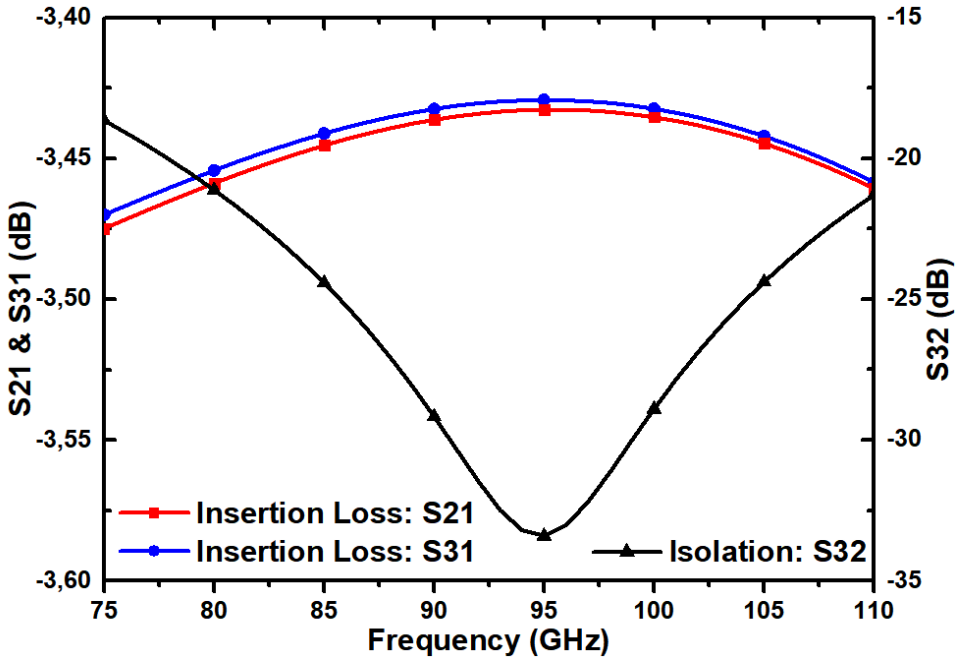

Figure 99 Simulated insertion losses and isolation results of the designed power divider.

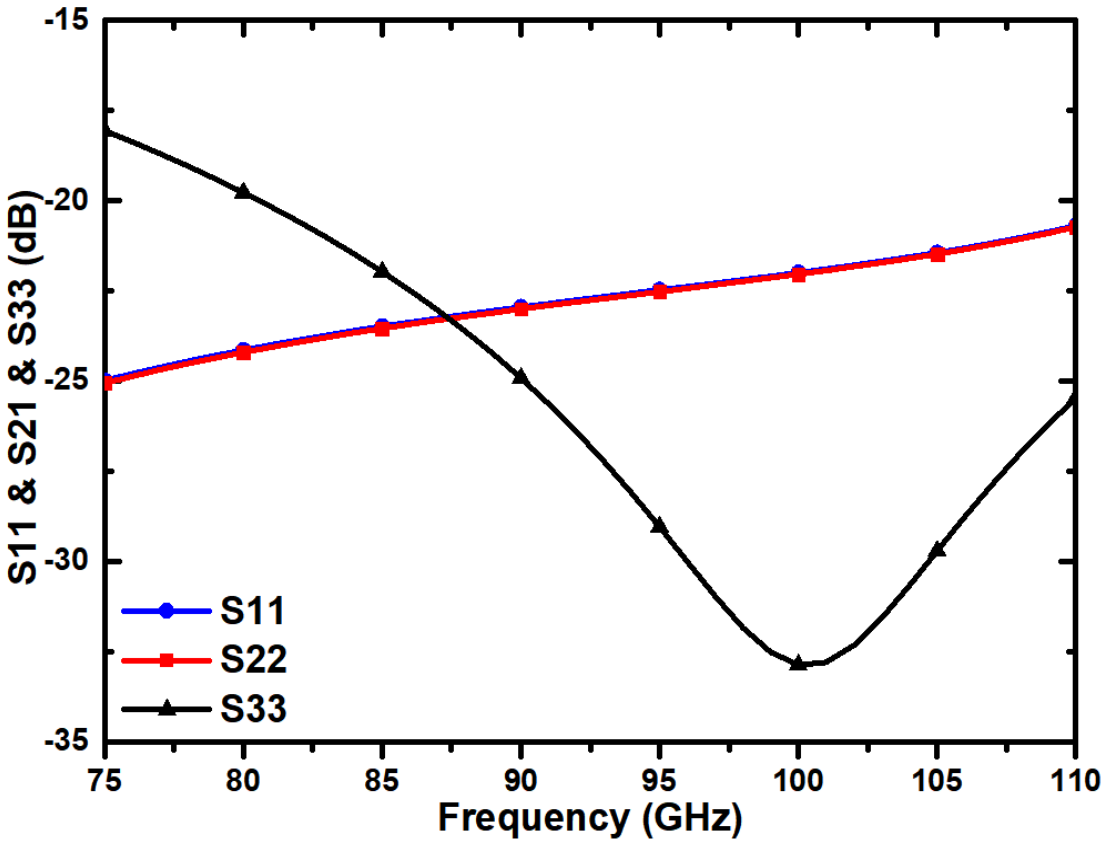

Figure 100 Simulated return losses of the designed power divider.

3.7. Frequency Extension Module

3.7.1 Implementation

The designed sub-blocks (down-conversion mixer, frequency quadrupler, buffer amplifier, dual-directional coupler, and Wilkinson power divider) were assembled to build a frequency extension module whose detailed block diagram is shown in Figure 66. The 2D layout view of the implemented frequency extension module is presented in Figure 101. The transmission lines which are used to carry RF signals between the sub-blocks were implemented as grounded coplanar transmission lines that configurated as follow: Top Metal 2 for top lines, Metal 3 for ground, and with via-walls from Metal 3 to Top Metal 2. This enabled to use Metal1 and Metal 2 layers for DC routings. In order to reduce the insertion losses of the interconnection transmission lines, sub-blocks were located as close as possible to each other. Since the inputs and outputs of the sub-blocks were matched to 50Ω, any impedance matching network between the sub-blocks was not used.

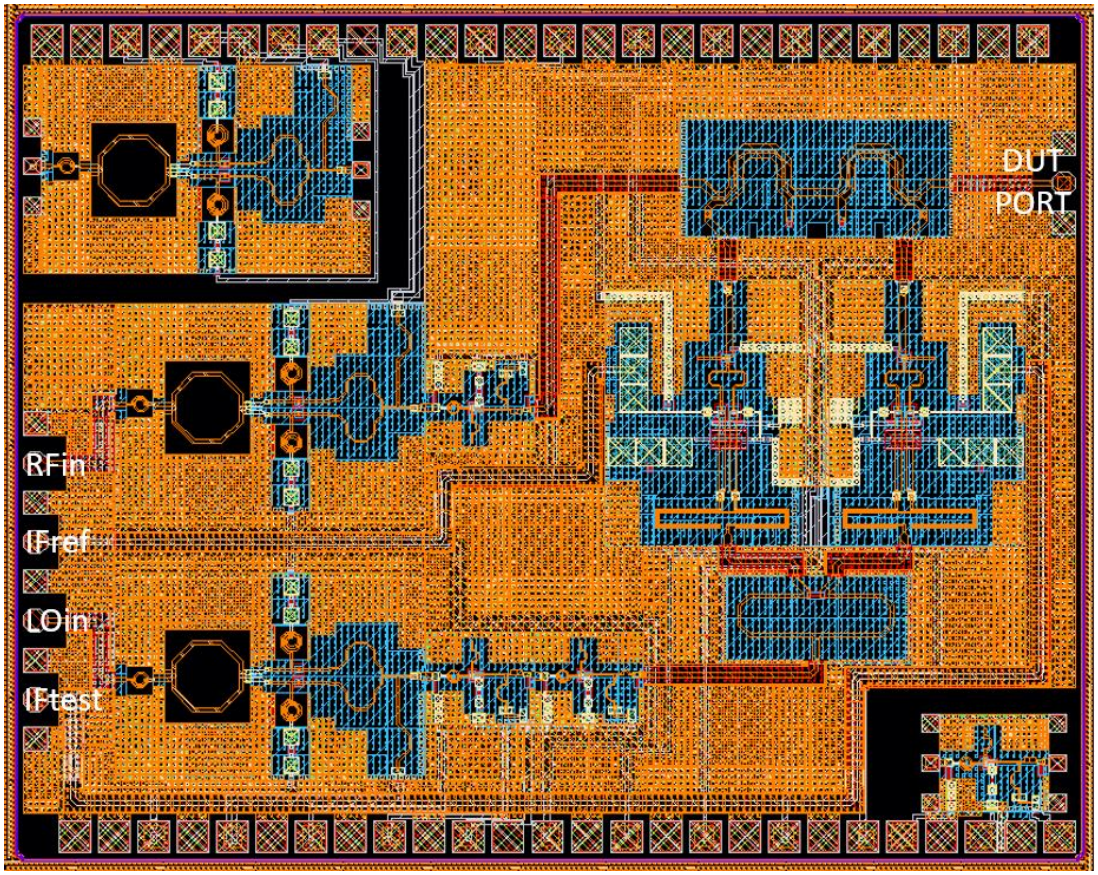

Figure 101 2D layout view of the implemented W-band frequency extension module for VNAs.

3.7.2 Characterization

Figure 102 shows the chip micrograph of the frequency extension module designed for VNAs. The total chip occupies an area of 5.9 mm^2, including the other designs. The total power consumption is approximately 410 mW while applying both RF and LO input signals. A quad-probe (GSGSGSGSG, DC-to-40 GHz) which is custom manufactured by Cascade Microtech to characterize the single-chip frequency extension module was used either to apply the RF and LO input signals (RFin and LOin) and to measure the IF reference and test signals (IFref and IFtest). The DUT port was connected to the measurement instruments or the DUTs by the WR10 GSG probe.

The experimental test setup which was used to determine the output power of the designed frequency extension module is depicted in Figure 103. The RFin (18.75-27.5 GHz) and LOin (18.675-27.425 GHz) signals were applied by Keysight N5224A PNA. The output power was down-converted by a W-band down-converter mixer which is configurated with an active multiplication chain (AMC) and Keysight E8257D signal generator. The

down-converted signal was measured using the Keysight E4448A spectrum analyzer. Figure 104 shows the measured output power of the designed frequency extension module. The maximum output power is -0.3 dBm at 95 GHz, and it is greater than -4.25 dBm across the W-band. The average noise floor of the DUT port was found to be -110 dBm for an IF resolution bandwidth (RBW) of 10 Hz. Consequently, the designed frequency extension module achieves a dynamic range of 105-110 dB over the W-band.

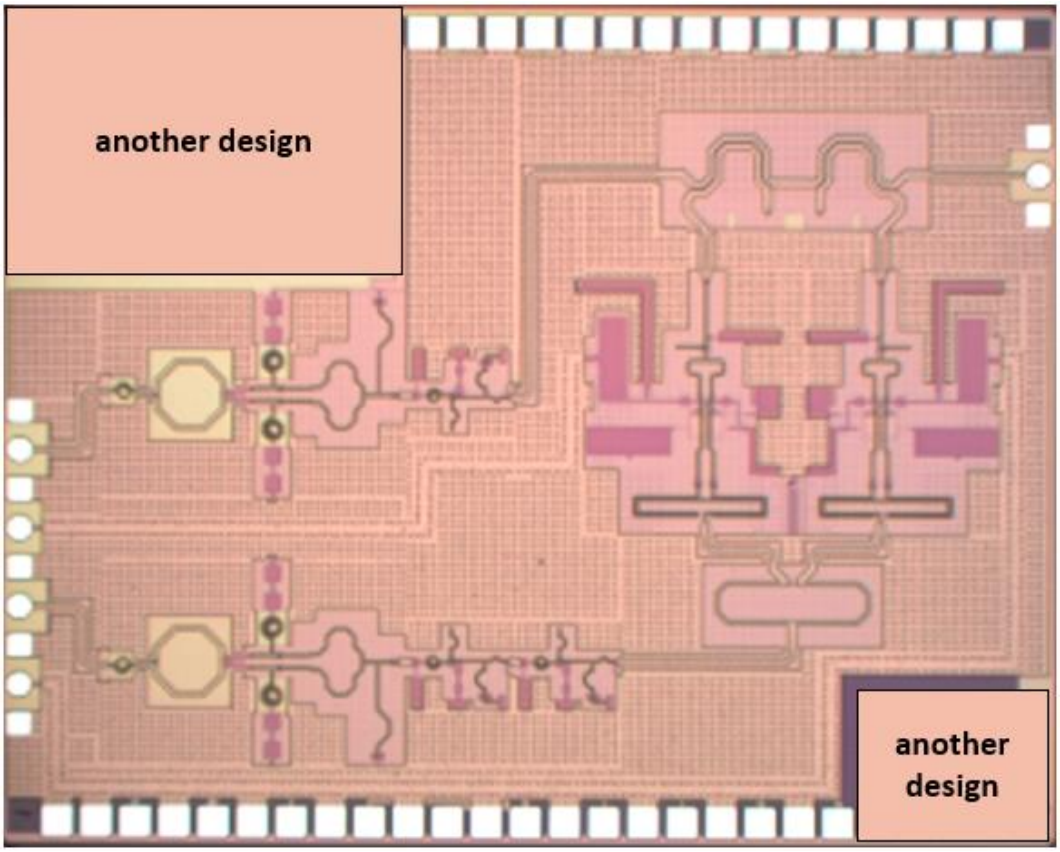

Figure 102 Chip micrograph of the frequency extension module (2.75 mm × 2.15 mm).

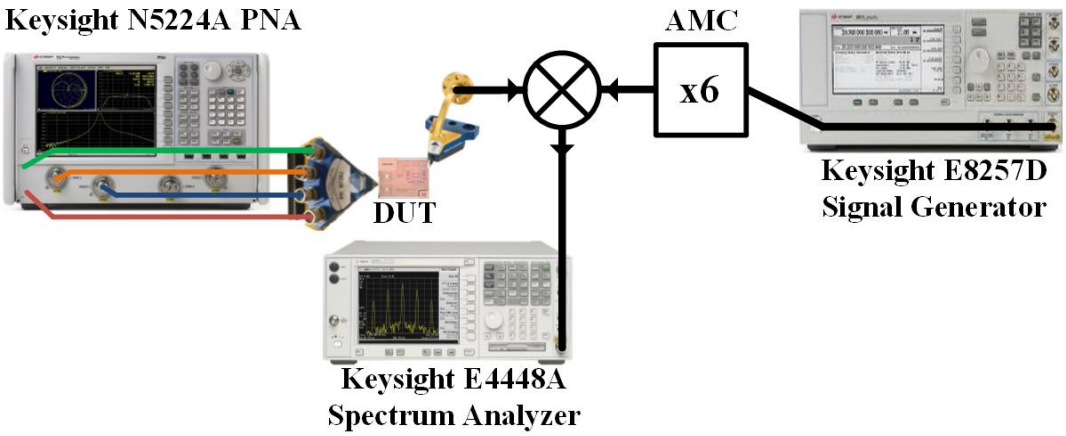

Figure 103 Experimental test setup to measure the output power of the designed frequency extension module.

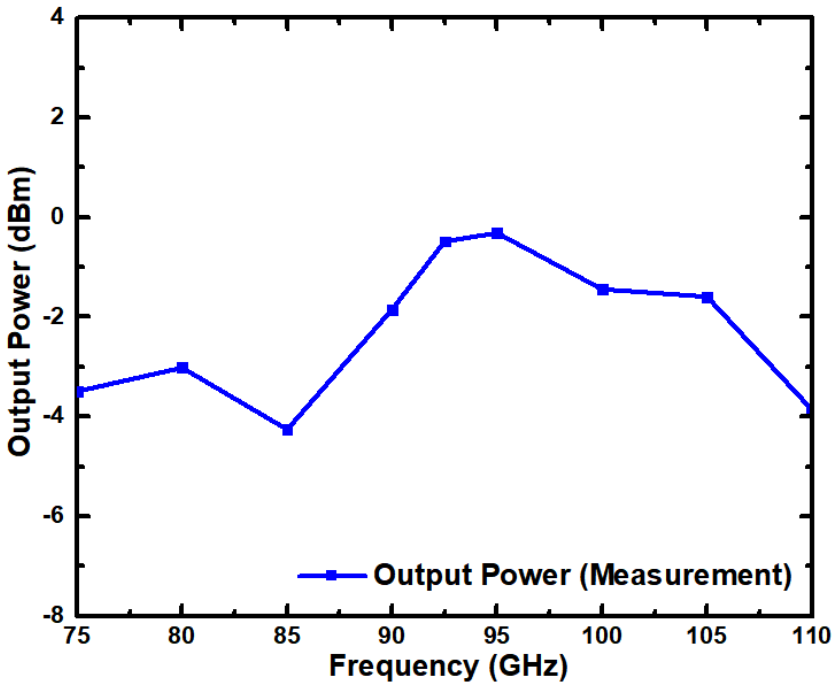

Figure 104 Measured output power of the designed frequency extension module.

Figure 105 depicts the experimental test setup which is used to determine the input referred 1-dB compression point of the designed frequency extension module. A 92.5 GHz, the center of the frequency range of interest, the signal was applied to the DUT port of the frequency extension module. This applied signal was sampled and then down-converted to IF signal to determine its power. In the meanwhile, the IF test signal of the designed frequency extension module was observed by the IF receiver of the VNA. The relationship between the power of the DUT port and the power at the IFmeas port is shown in Figure 106. The measured IP1dB was found to be about 1.9 dBm.

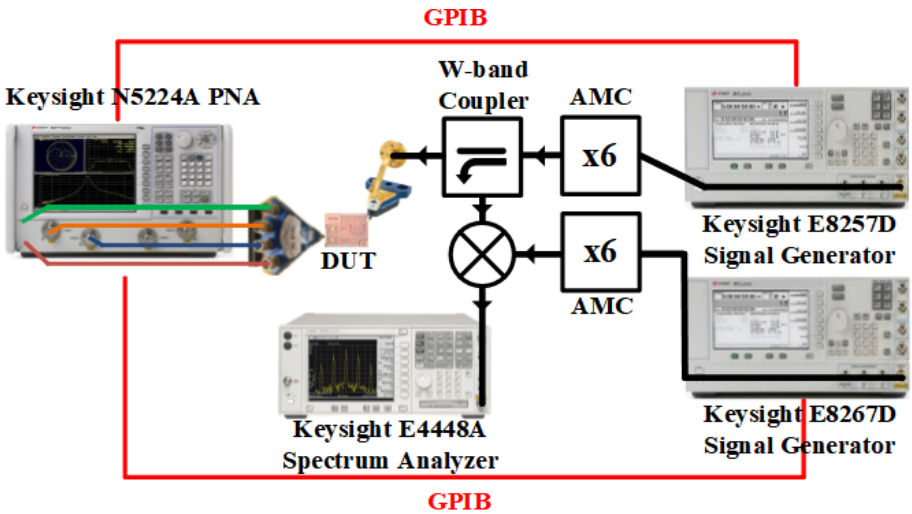

Figure 105 Experimental test setup to measure the input referred 1-dB compression point of the designed frequency extension module.

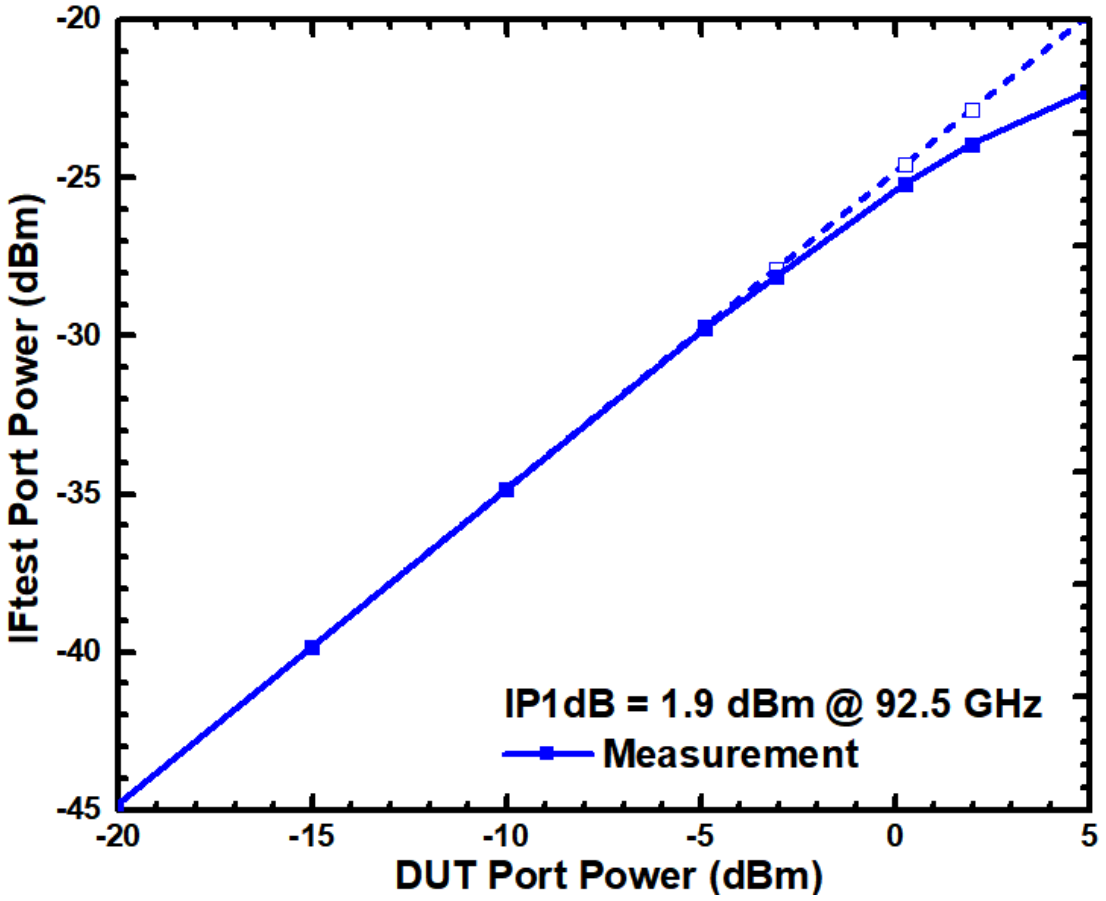

Figure 106 Measured power of the IFtest port versus the power of the DUT port.

The directivity of the designed frequency extension module was determined as follow. First, the DUT port was terminated with an open circuit using the WR10 calibration kit, and the IF reference and test signals of the designed frequency extension module were measured. The power difference between the IF reference and test signals gives us to the conversion gain difference between the reference and test receiver channels of the designed frequency extension module. After that, the match load (50Ω) from the WR10 calibration kit was connected to the waveguide interface of the WR10 probe, and the power of the IF reference and test signals were measured again. Consequently, the directivity can be found by de-embedding the conversion gain difference from the power difference at the second configuration (match load). Figure 107 shows the measured directivity of the designed frequency extension module. The peak value of the directivity is about 23 dB, and it remains above 10 dB across the W-band. The degradation in the directivity of the single-chip frequency extension module relative to the directivity of the dual-directional coupler can be attributed to the mismatching which might arise due to the used WR10 probe and the parasitic capacitances of the pads of the DUT port.

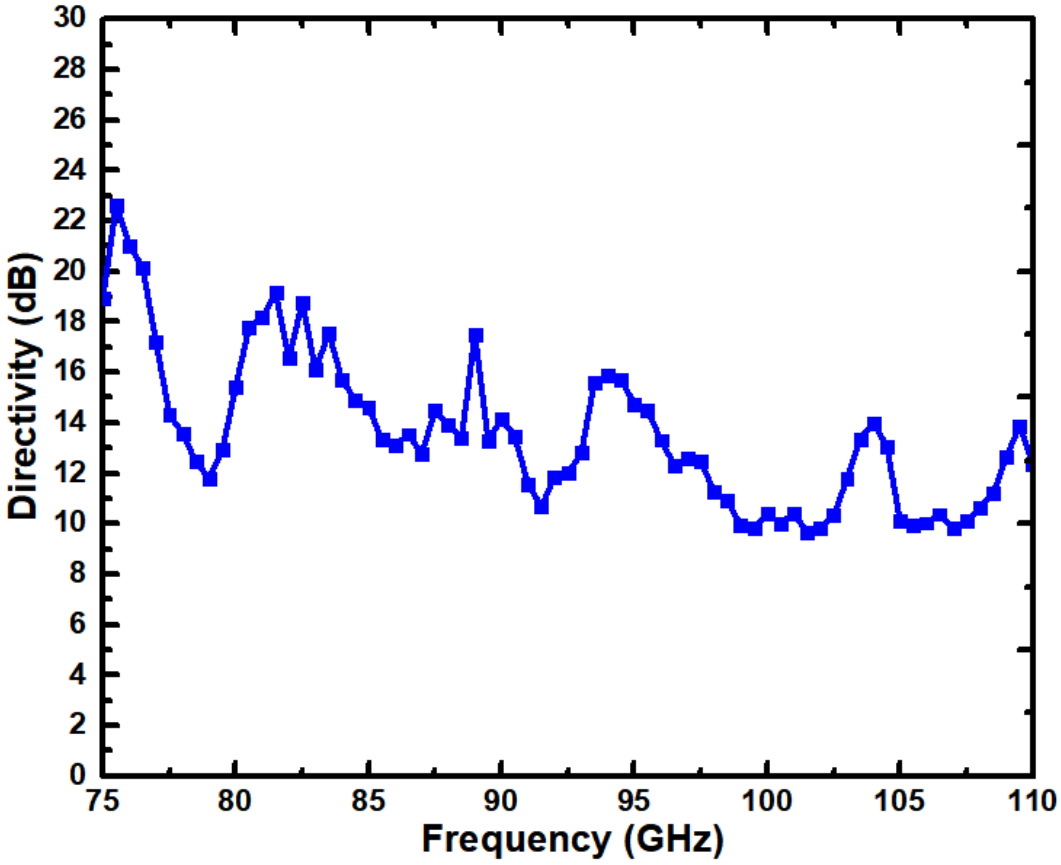

Figure 107 Measured directivity of the single-chip frequency extension module, including the WR10 probe.

3.7.3 Measurement Results

Figure 108 depicts the experimental test setup which is used to perform one-port s-parameter measurements by the designed single-chip frequency extension module. The single-chip frequency extension module was configurated with Keysight N5224A PNA through the quad probe, and the DUT port was connected to the calibration standards and the DUTs using the WR10 probe. One-port short-open-load (SOL) calibration was performed by a WR10 calibration kit, and IF resolution bandwidth was set to 10 Hz.

S-parameters of a W-band horn-antenna was measured using both the designed single-chip frequency extension module and a commercial frequency extension module, under the same conditions such as IF resolution bandwidth, a number of points, sweep time, etc. The amplitudes of the measured S11 of the W-band horn-antenna is shown in Figure 109. Figure 110 presents the phases of the measured S11 of the W-band horn-antenna. As can be seen from the figures, there is a pretty good agreement between the results. However, there are some noticeable discrepancies, even between two different measurements which

are performed by the same commercial frequency extension module due to the misalignments of the waveguide interfaces during the measurements and the calibrations. In addition to these misalignments, the considerable part of the discrepancies between the commercial and designed frequency extension modules arise because of the low directivity of the single-chip frequency extension module. The directivity of the single-chip frequency extension module can be significantly improved using the shielded coplanar lines instead of the microstrip lines.

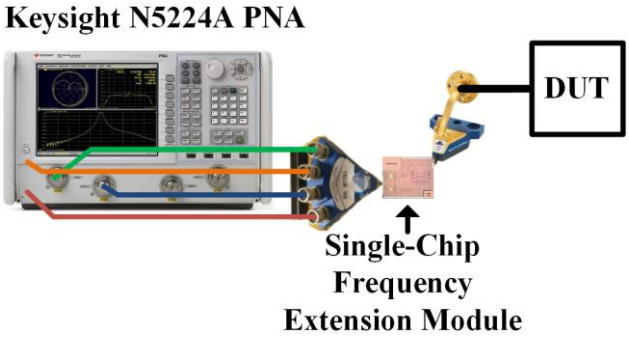

Figure 108 Experimental test setup to measure the one-port DUT by the designed frequency extension module.

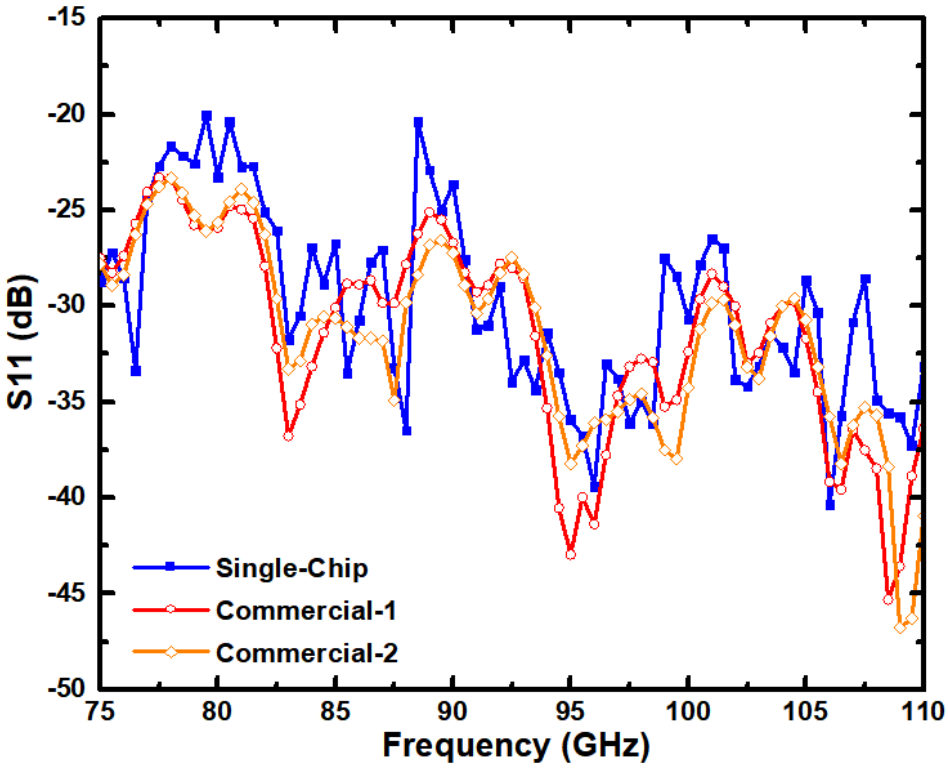

Figure 109 Measured amplitudes of S11 of a W-band horn-antenna using the designed single-chip frequency extension module and a commercial WR10 frequency extension module.

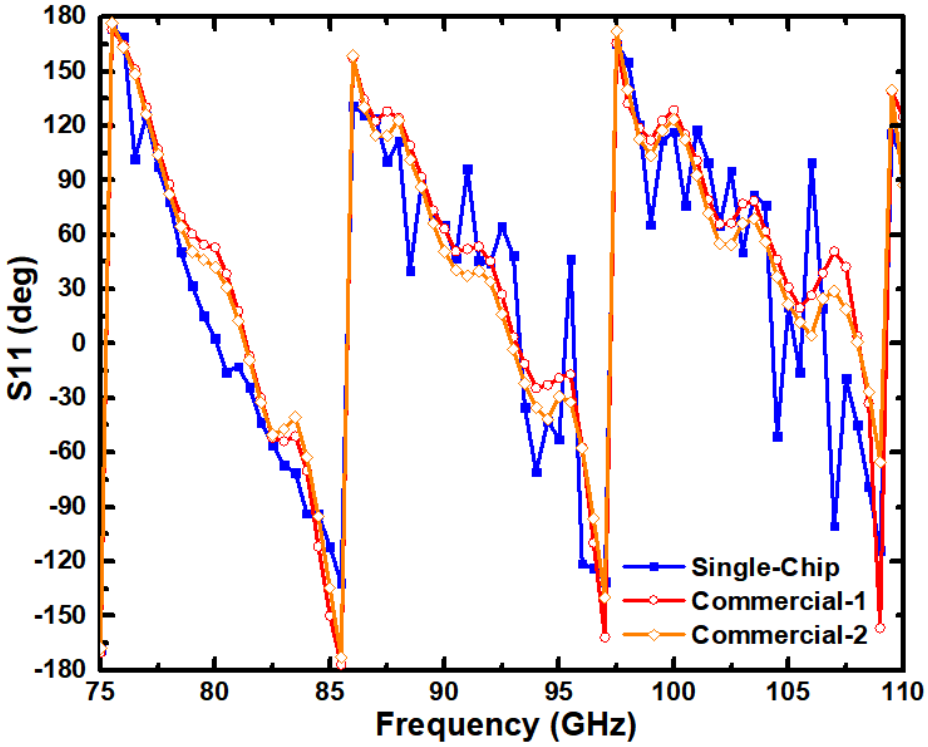

Figure 110 Measured phases of S11 of a W-band horn-antenna using the designed single-chip frequency extension module and a commercial WR10 frequency extension module.

4. Conclusion & Future Work

4.1. Summary of Work

Latest developments in silicon-based semiconductor technologies have led to an important research interest in the field of millimeter-wave systems. There are a few significant low-atmospheric attenuation windows in the millimeter-wave spectrum (35, 77, 94, 140, 220 GHz). These low-atmospheric attenuation windows make the millimeter-wave domain appropriate and attractive for many various applications such as automotive RADARs, passive imaging systems, high-speed point-to-point wireless communication links, and radar sensors.

SiGe BiCMOS technology provides the integration of the high-speed SiGe HBTs and the Si CMOS transistors on single-chip. Recently, the RF performances, f_t and f_{max}, of the SiGe HBTs have caught up those of III-V counterparts. Therefore, SiGe HBT BiCMOS technology have enabled to build low-cost and fully-integrated single-chip millimeter wave systems that include the RF front-end and baseband parts together.

In this thesis, two single-chip D-band front-end receivers for passive imaging systems and a single-chip W-band frequency extension module for VNAs are presented. These systems are implemented in IHP's 0.13µm SiGe BiCMOS process, SG13G2, featuring HBTs with $f_t/f_{max}/BV_{CEO}$ of 300GHz/500GHz/1.6V. This thesis can be summarized under two main groups as D-band radiometers and W-band frequency extension module.

Under the chapter of D-band radiometers, first, the designs, implementations, and measurements of the sub-blocks of the radiometers (SPDT switch, LNA, and power detector) are presented. After that, the implementation and experimental test results of the total power and Dicke radiometers are demonstrated. The total power radiometer attains an NETD of 0.11K, assuming an external calibration technique. The NETD of the total power radiometer is 1.3K for a gain-fluctuation of %0.1. The Dicke radiometer shows an NETD of 0.13K for a Dicke switching of 10 kHz. These implemented radiometers show the state-of-the-art operations with respect to the previously reported radiometers implemented in either silicon-based technologies and III-V group semiconductor technologies.

In the other main chapter, named as W-band frequency extension module for VNAs, first, the design methodologies, implementation methods, and experimental results of the sub-blocks (down-conversion mixer, frequency quadrupler, Wilkinson power divider, and dual-directional coupler) are presented. Then, the implementation, characterization and experimental results of the single-chip W-band frequency extension module are demonstrated. The maximum output power of the designed frequency extension module is -0.3 dBm at 95 GHz, and it remains above -4.25 dBm along the entire W-band. The average noise floor of the DUT port is -110 dBm for an IF resolution bandwidth of 10 Hz. Thence, the designed frequency extension module has a dynamic range of 105-110 dB across the W-band. The measured input referred 1-dB compression point of the single-chip frequency extension module is approximately 1.9 dBm. One of the most critical performance criteria of a frequency extension module is the directivity. The maximum value of the directivity of the designed frequency extension module is about 23 dB, and it is greater than 10 dB over the W-band. Lastly, the measurement results of a W-band horn antenna, performed using the single-chip frequency extension module and a commercial frequency extension module, are demonstrated. It is observed that there is a good agreement between these measurements. Consequently, this thesis highlights the potential of the SiGe BiCMOS technology in the field of millimeter-wave passive imaging systems and the measurement instruments.

4.2. Future Work

As a short-term future work for the D-band radiometers, an on-chip antenna and a baseband part need to be designed on the same chip and to be implemented together. After that, suitable packaging is required for the DC supply connections and the output signal. Finally, a focal-plane array needs to be implemented to obtain the image of the scene using the designed single-pixel radiometers.

On the other hand, the performance of the single-chip frequency extension module should be improved to obtain more accurate results. Within this scope, the directivity of the frequency extension module can be significantly improved using the shielded coplanar transmission line based directional coupler instead of the microstrip line based coupler. Moreover, the transmission lines of the coupler were meandered to reduce the chip area, but it considerably reduces the isolation of the dual-directional coupler so that the directivity of the frequency extension module is dramatically degraded. Therefore, the priority should be given to achieving high isolation rather than reducing the chip area. In

addition, the gain of the double-stage amplifier at the LO channel of the frequency extension module is too much so that it is compressed for the fourth harmonic (actual operating signal of the frequency extension module) of the frequency quadrupler. Thence, it would result in the degradation of the harmonic suppression performance. For this reason and considering the current performance of the system, a single-stage amplifier would be enough instead of the double-stage amplifier. After the proposed performance improvements, an electrically controlled attenuator can be placed after the single-stage amplifier at the RF channel to enable the control of the output power of the frequency extension module. The final step of the frequency extension module work is to integrate into a suitable RF probe, as proposed in Section 3.1.2.

APPENDIX

A. Appendix

```
k= 1.38 * 10^-23; %boltzmann's constant (J/K)
T0= 290; %Temperature (K)
B= 15*10^9; %bandwidth (GHz)
NEP=0.43*10^-12; %NEP of PD

G1_dB=-2.1; %S21 of the SPDT
G2_dB=22.5; %S21 of the LNA
G1=10.^(G1_dB/10);
G2=10.^(G2_dB/10);

NF1_dB=-G1_dB %NF of the SPDT
NF2_dB= 4.4 %NF of the LNA
F1=10.^(NF1_dB/10);
F2=10.^(NF2_dB/10);
F3=1+(NEP/(k*T0*sqrt(B)));; %noise factor of the PD

TE1= T0*(F1-1); %the equivalent noise temperature of the SPDT
TE2= T0*(F2-1);%the equivalent noise temperature of the LNA
TE3= T0*(F3-1)%the equivalent noise temperature of the PD

T_R= TE1 + (TE2./G1) + (TE3./(G1.*G2));%the equivalent noise temperature of the receiver
T_A=T0; ; %The equivalent noise temperature of the antenna
T_S=T_R+T_A; %the system noise temperature

tau= 30*10^-3 ;%back-end integration time
NETD=2 .*(T_S)./sqrt(B*tau); %the noise equivalent temperature difference (K)

plot (G2_dB, NETD)
hold on
```

B. Appendix

```
R1= 0.902768;
theta1 = deg2rad(-25.807768);
GM1 = R1.*exp(i*theta1) % GM1 = measured short
R2 =0.628266;
theta2 = deg2rad(170.674668);
GM2 = R2.*exp(i*theta2) % GM2 = measured open
R3 =0.153073;
theta3 = deg2rad(247.575889);
GM3 = R3.*exp(i*theta3) % GM3 = measured 50ohm
GA1 = -1; %short
GA2 = 0.8181818182; %open 500ohm
GA3= 0; %load
syms a b c
eqn1 = GA1 * a + b - GA1 * GM1 * c == GM1;
eqn2 = GA2 * a + b - GA2 * GM2 * c == GM2;
eqn3 = GA3 * a + b - GA3 * GM3 * c == GM3;
S= solve (eqn1, eqn2, eqn3)
S= [S.a S.b S.c]
d=double (S);
am=d(1)
bm=d(2)
cm=d(3)
R4= 0.467042;
theta4 = deg2rad(70.697597);
GM4 = R4.*exp(i*theta4) %GM4 = measured reflection coefficient - DUT
syms GA4
eqn4 = GA4 * am + bm - GA4 * GM4 * cm == GM4;
Sol = solve(eqn4)
e=double(Sol)
ZL=50*((1+e)/(1-e))
```

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