High Dynamic Range Smart Pixel Architecture for Infrared Focal Plane Arrays

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***Abstract*—This paper focuses on achieving high dynamic range pixel by using multiple pre-amplifiers in the pixel. There are two input circuits which are optimized for different signal levels inside the pixels. A smart circuit mechanism, inside each pixel, decides the best input circuit according to the incoming light level. In short, an individual pixel has the ability to select the best input amplifier circuit that performs the best SNR for the incoming signal level. A prototype chip is designed in 0.18 um CMOS technology. Pixel can achieve minimum 8.6 e- input referred noise and 98.9 dB dynamic range. In room temperature, power consumption of 2.8 uW is measured for the pixel.**

I. Introduction

First and second generation FPAs are defined based on their array formation. However, the third generation promises more on-chip functionality, capability, and performance for pixels such as analog to digital conversion inside a pixel instead of column level, very large number of pixels (2048x2048), usage of dual or multi color detectors, some pre-processing functionalities within a pixel and utilization of cheap uncooled technologies [1].

New generation ROICs have been developed over the last decade to meet the performance requirements of the third generation FPAs. Digital integrated readout of circuits (DROICs) promise very large charge handling capacities around Ge^{-} range, high SNR values with high-resolution conversion capabilities and low power consumption [2]–[4]. DROICs are mostly suitable for LWIR and MWIR due to high current levels. There are some drawbacks associated with DROICs such as high cost due to the usage of advanced technology node. Another approach is developing smart ROICs that includes on-chip processing capabilities and functionalities to reduce the overhead or improve performance [5]–[10]. Pitch sizes of these ROICs are bigger than conventional ROICs, due to the extra added functionalities into pixel structure. Finally, another popular trend for the third generation FPAs is dual or multi-color imaging systems or detectors [11]–[15].

In this work, a smart solution for improving SNR is demonstrated for third generation detectors. This smart solution is found within pixel structure of a ROIC and includes two input amplifiers and a mechanism which selects the best performing input amplifier automatically according to the incoming illumination level. This solution is compatible with both high dynamic range SWIR and dual-band, multicolor detectors.

II. Architecture

Conventionally, single input amplifier is used inside each unit cell. Instead, two input pre-amplifiers which are optimized for low and high photon flux levels are utilized in the smart pixel architecture. Fig. 1 represents the conventional and smart pixel architecture in a simple manner. The smart pixel diverges from the usual structure with additional amplifier and in-pixel smart control circuit. The control mechanism selects the best optimized input amplifier according to the incoming flux level. The smart control mechanism consists of latches and switches which occupy small pixel area. This mechanism activates two-step integration scheme. Basically, in this control mechanism some latches are pre-configured in the beginning of the first integration. According to illumination level, control circuit switches between CTIA (Capacitive TransImpedance Amplifier) and SFD (Source Follower per Detector) for the actual integration.

The working principle of the smart light detection mechanism is based on two-level integration which is simply shown in Fig. 3. In this scheme, before regular integration (second integration) there is a very short integration time. This very short integration time will be used to determine the flux level. In the SWIR imaging, the integration time is in the millisecond range due to the low photon flux as opposed to MWIR and LWIR bands. Even in the near infrared region typical integration time is around 100 ms range. The first integration can be negligible and very short compared to the actual integration. Users have the option to adjust the duration of the first integration using a digital control interface. Flow chart of the pixel operation is shown in Fig. 2.

A register inside the control mechanism activates the CTIA in the first integration by default (S2 switch is selected by default). Then, CTIA is configured to start as a comparator (deactivating C_f integration capacitor by a switch which is not shown in Fig. 4) and compares the integrated charge with V_{ref} which is a user defined voltage level for determining the light level. If integrated charge exceeds the threshold level, comparator activates the SFD for actual integration. Otherwise, CTIA continues the integration (C_f will be activated). Either S1 or S2 switches are activated by the control circuit to select between the SFD and the CTIA. S3 switch is used for resetting the node for V_{res} during reset period. At the end of integration, the register provides a 1-bit information regarding the selected amplifier along with an analog output; logic 0 for the CTIA

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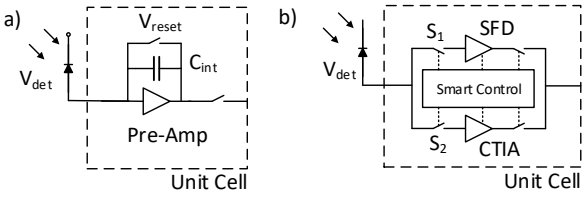

Fig. 1. a) Standard pixel structure b) smart pixel architecture

and logic 1 for the SFD. 1 bit digital information is useful for post-processing purposes such as non-uniformity correction. First and second integration time durations are controlled by the central digital control circuit.

CTIA and SFD input amplifiers, which respectively cover low and high illumination levels, are used in the smart pixel design. The choice of CTIA for the low illumination level is based on its injection efficiency of very low currents (low photon flux) and its low noise characteristic with the choice of small integration capacitance. The integration capacitance of CTIA can be very small unlike other topologies because the output of the unit cell is connected to the amplifier output which is a low impedance node. This yields great low noise performance compared to large integration capacitance [16].

The input referred noise of the CTIA is given by:

$$N^2_{white} = \frac{kT}{q^2}\left[\left(\frac{2T_{int}}{R_o}\right) + \left(\frac{C_{int}+C_d}{C_L + \frac{C_{int}C_d}{C_{int}+C_d}}\right)\left(C_{int} + \frac{C_{int}+C_d}{A_{vo}}\right)\right] \quad (1)$$

$$N^2_{1/f} = \frac{2T^2_{int}}{q^2}\left[S_{fd}\ln\left(\frac{1}{\pi f_{sat} T_{int}}\right) + \left(\frac{f_s}{f_a}\right)^2 S_{fa}\left(\frac{C_{int} + \frac{C_{int}+C_d}{A_{vo}}}{C_L + \frac{C_{int}C_d}{C_{int}+C_d}}\right)^2 \ln\left(\frac{11.8 f_a}{f_s}\right)\right] \quad (2)$$

in which S_{fa} and S_{fd} respectively stand for amplifier and detector 1/f noise current power spectral densities at 1 Hz. f_{sat} is the saturation frequency which is related with integration capacitance (C_{int}), detector capacitance (C_{det}), load capacitance of the amplifier (C_L), detector impedance (R_o), integration time (T_inT) and gain of the amplifier (A_v0). Finally, f_a is the cutoff frequency of the CTIA amplifier and f_s is the sampling frequency.

1 and 2 do not include kTC noise component as it can be eliminated with correlated double sampling (CDS). The input-referred noise can be made small by choosing a small integration capacitance (C_{int}) and using a high gain amplifier. Also, increasing the load capacitance reduces the noise bandwidth.

Source follower per detector consists of an integration capacitor, a reset transistor and a source follower transistor.

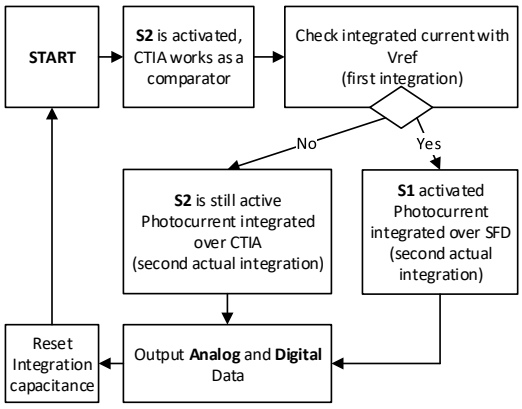

Fig. 2. Flow chart of the pixel operation.

The total integration capacitance can be calculated by adding the integration capacitor and the source follower input capacitance. While the signal is integrating on to the capacitance, detector bias changes, since the signal is integrated directly on the same node as the detector, unlike CTIA which keeps the detector voltage constant. Nevertheless, due to its simple structure, SFD provides noise performance is better than other preamplifier such as CTIA and SFD.

The primary source of white noise in the SFD is the source-follower transistor itself. Additionally, SFD is very susceptible to flicker noise. Slightly large integration capacitance is used in SFD design to cover high photon flux.

Input-referred white noise electrons for the SFD is given by [17]:

$$N_{sf} \approx \frac{\sqrt{2}}{S_V}\left[\int_0^{\triangle f} V_n^2(f)\frac{(1-\cos 2\pi f t)}{[1+(2\pi f T_D)]} d_f\right]^{1/2} \quad (3)$$

which S_V equals:

$$S_V = \left(\frac{C_{int} A_{v0}}{q}\right)^{-1} \quad (4)$$

in which A_v0 is the gain of the amplifier, C_inT integration capacitance and T_D is the time constant for CDS.

In both preamplifier topology, noise contribution of the input multiplexer (S1 and S2 switches) is common and it is not eliminated by CDS. General form of the noise contribution is as follows [17]:

$$\sigma^2_{mux,ir} = \frac{1}{A_v^2} kTC_{bus}\Delta f \quad (5)$$

Direct Injection (DI) topology can be an alternative to SFD if very high flux levels are expected. DI features a single MOS whose source is modulated directly by a detector. For the high flux levels, detector bias stability and injection efficiency are very high because it depends on transconductance and detector resistance. In the case of the low photocurrents, the

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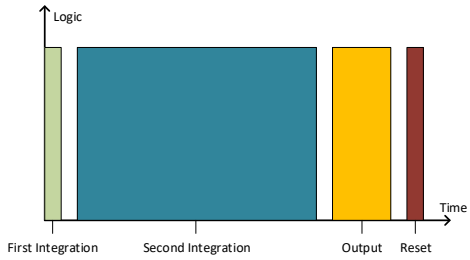

Fig. 3. Timing diagram for the two-step integration. First integration is for detecting light level second one is actual integration of light

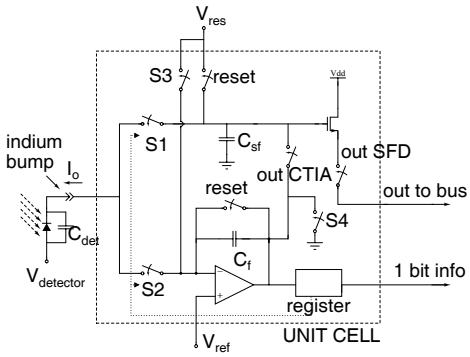

Fig. 4. Schematic of the smart pixel.

transconductance drops due to the change in the operating region of MOS. In the sub-threshold region, g_m of the MOS is very small.

III. Implementation

A ROIC test chip with smart pixels is designed and fabricated using 0.18μm XFAB technology. The ROIC includes pixels, current sources, a multiplexer, an output amplifier and some test circuits such as individual CTIA and SFD amplifiers. In this chip, current sources are used instead of an infrared detector. The designed current source is compensated for process and mismatch variations and capable of providing current from 10pA to 3nA. Its architecture is based on [18], to reduce the footprint of the current source, some optimizations are performed such as getting rid of the temperature optimization part. Unlike a detector, the current sources are not hybridized to the ROIC chip. Thus the detector bonding area inside the pixel is utilized for the current sources.

Fig. 4 and Fig. 5 present schematic and layout of the smart pixel, respectively. It consists of a CTIA, a SFD, and a smart control register. In this structure, the CTIA amplifier is designed as the differential input instead of a single-input common-source structure which is commonly used in conventional CTIA cells. This differential structure provides an extra feature that the CTIA can be utilized as a comparator. 6 fF and 40 fF are selected as an integration capacitance for CTIA and SFD, respectively. 6 fF is minimum drawable capacitance in this technology.

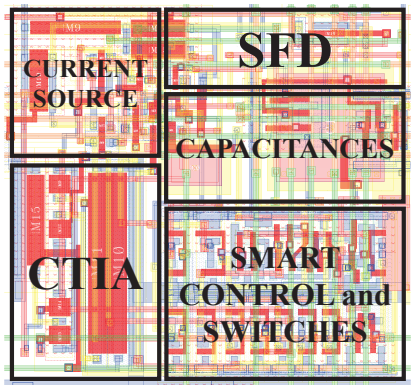

Fig. 5. Layout of the smart pixel (22.5x22.5 μm^2)

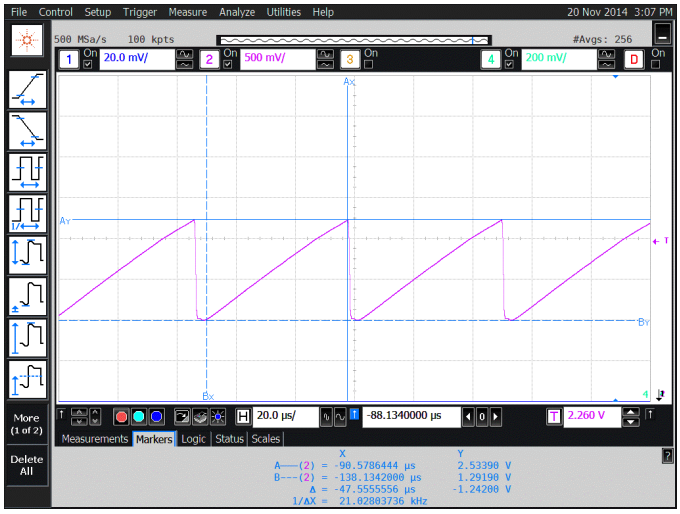

Fig. 6. 50 μs integration time, 2.714V bias voltage, and 1.24V integrated charge.

IV. Measurements

Measurements were performed using Keysight 16702B Logic Analyzer, MSO 9254A Digital Storage Oscilloscope and Agilent DC power supplies. Logic Analyzer provides the digital control and clock signals for the chip. The oscilloscope is used for sampling the analog data. PCB test card which includes BNC connections for dc cables, coupling capacitances and switches are designed for the test.

First, single amplifier response is measured. For instance, Fig. 6 shows 50 μs integration of SFD with 2.714V bias voltage (approximately 1 nA current) of current source. SFD is integrated 1.24V charge.

Reset noise is measured and extracted from measurement results to calculate input referred noise for the both amplifiers. Since the architecture does not include CDS, subtraction is done manually with two consecutive measurements. Keysight MSO 9254A oscilloscope is used to sample the data. 128 consecutive measurements are performed. Extracted data is processed using MATLAB.

Fig. 7 shows SNR performances of CTIA and SFD amplifiers. As expected SNR performance of CTIA is superior

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TABLE I
COMPARISON

	This Work	[19]	[20]	[21]	[22]	DROIC [2]
Pixel Size (μm^2)	22.5x22.5	50x50	30x30	15x15	N/A	30x30
Input Stage	CTIA, SFD	BDI	DI	SFD	CTIA	DI
Input Current	15 pA - 3 nA	20 nA - 112 nA	2 pA - 10 nA	astronomy	VLWIR	20 nA
Charge Handling Capacity (e^-)	45 K (CTIA), 764.4 K (SFD)	N/A	9.8 M	120 K	11 M	2.3 G
Power/Pixel	2.8 μW	1 μW w/o 14 bit ADC	800 nW	3.6 nW	11 μW	1 μW
Operating Temperature (K)	300	77	77 - 300	80 - 140	1.8 - 3	77 - 300
Readout Noise	8.6 e^-(CTIA), 252 e^-(SFD)	205 μV	350 e^-	6 e^-	1000 e^-	161 e^-
Dynamic Range (dB)	98.9	95.8	88.9	86	80	132
CMOS Technology	0.18 μm	0.35 μm	0.18 μm	0.35 μm	0.5 μm	90 nm

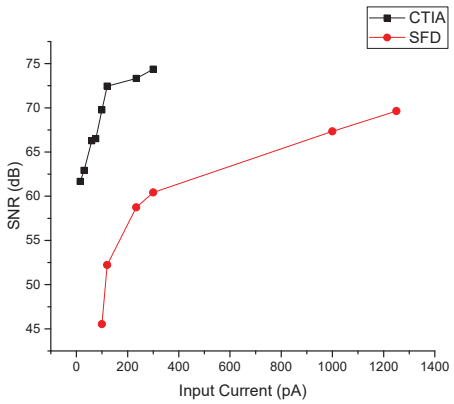

Fig. 7. SNR vs Input Current of CTIA and SFD amplifiers

due to low integration capacitance and high gain. Reasonable SNR performance obtained from SFD amplifier with its 40 fF integration capacitance. In this measurement integration time is increased until integration capacitance reaches in saturation. Just before saturation, maximum SNR values are observed. CTIA and SFD have reached 74.3 dB and 69.6 dB SNR respectively. 8.6 e^- noise is measured from CTIA amplifier with 45 K e^- charge handling capacity.

Table I demonstrates the comparison of the measured pixel performance with literature. [19] and [20] are high dynamic range ROIC examples which were designed for high photocurrent levels and SWIR, respectively. [21] and [22] are using SFD and CTIA respectively. Finally, [2] is provided to compare the analog and digital ROICs. Digital ROICs are superior regarding charge handling capacity and dynamic range. Hence, they are costly regarding technology node (90nm or lower CMOS technology), and their SNR levels are comparable to analog ROICs [2].

Dynamic range is the best among analog ROICs in the literature with respect to the table. The ROIC has reasonable charge handling capacity for SWIR. The noise floor is again competitive among its rivals.

Regarding dynamic range [19] is quite a close competitor. [19] uses unique multiple sampling method and background suppression to reach 95.4 dB dynamic range. That architecture is inefficient for high speed and big arrays. Also, 50 μm pixel size is quite large compared to this work. [19] can use for a certain range of detectors.

[21] has a low readout noise (6 e^-) due to minimal integration capacitance and operating temperature. It is designed for astronomy measurements. Thus it has a slow frame rate (2 Hz) and low charge handling capacity (120 Ke^-). It operates cryogenic temperatures. Due to very slow frame rate pixel per power consumption is extremely low (3.6 nW).

Regarding temperature, current range, dynamic range and technology, [20] performs closely to this work. Nevertheless, this work exceeds concerning dynamic range and input referred noise level but [20] has enormous charge handling capacity and low power. Another point should be taken into consideration is [20] designed for quantum dot (QDIP) detector. That is why [20] can utilize DI and handles very wide input current level (2 pA - 10 nA).

[22]'s work is similar to [21] with respect to an application. Both are designed for astronomical observations. Due to expected high dark current levels and to be able to achieve long integration times charge handling capacity is very high (11 Me^-). Moreover its the only competitor that utilizes CTIA for High Dynamic Range.

V. CONCLUSION

In this paper a novel pixel architecture for the third generation infrared detectors is demonstrated. The idea is based on the detection of the incoming flux and choosing the best input amplifier. One input amplifier is optimized for low flux levels (CTIA), and another one is optimized for the high flux levels (SFD) of SWIR.

A prototype chip is designed in 0.18 μm XFAB technology and measured to demonstrate the idea. Instead of a detector, process and mismatch tolerant current sources are used to mimic a wide-range SWIR detector. 98.9 dB dynamic range is achieved with a minimum 8.6 e^- input referred noise with CTIA amplifier and 764.4 Ke^- charge handling capacity with SFD.

ACKNOWLEDGMENT

The authors would like to thank Ministry of Science, Industry and Technology (Project no: 1250.STZ.2012-1) for the financial support.

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