A Novel Approach to Noise Shaping in Digital Pixels for Infrared Imagers using Over-Integration

Shahbaz Abbasi, Atia Shafique, Omer Ceylan, Melik Yazici, Yasar Gurbuz
Faculty of Engineering and Natural Sciences
Sabanci University
Istanbul, Turkey
shahbazabbasi@sabanciuniv.edu

Abstract— **Digital readout integrated circuits (DROICs) for small pitch infrared focal plane arrays (IR-FPAs) suffer from low in-pixel resolution owing to the limited pixel real estate. To this end, a new technique to improve the resolution of pulse frequency modulation (PFM) based pixels, using quantization charge noise shaping, is presented. Multiple integration operations are performed in a single frame and the quantization error from each integration phase is retained and effectively induced into the next integration phase. The result is a high pass noise transfer function (NTF) equivalent to what is obtained in a first order sigma delta modulator. Along with a theoretical analysis of the technique, a prototype based on a single pixel and a 2nd order decimation filter is developed to demonstrate the performance of the proposed technique. With an in-pixel circuitry generating 5 bits, a resolution of 11 bits (65 dB) is achieved with an over-integration ratio of 64. With a 100 Hz frame rate and 64 integration operations per frame, a readout noise of 1100e- is measured at full-well fill from the test pixel fabricated in a 90nm CMOS process.**

Keywords— Digital Readout Integrated Circuit (DROIC), Pulse Frequency Modulation (PFM), Focal Plane Array (FPA), Oversampling, Noise Shaping

I. INTRODUCTION

Infrared imaging systems with above-megapixel formats find applications in missile warning systems, optical thermography and infrared astronomy [1]. The requirement of compact pixel sizes in these systems poses crucial challenges for the readout circuits in terms of the achievable signal-to noise ratio (SNR) and dynamic range. The photo-charge handling capacity is reduced, thereby degrading readout performance. Analog pixels are usually preferred under these constraints owing to their superior fill factor [2]. However, they impose the need for either chip level or column level analog to digital converters (ADCs) to quantize the entire charge well. Moreover, they suffer from reduced SNR. Digital pixels, on the other hand, provide a direct digital output and can significantly improve the charge handling capacity [2]. In addition, in-pixel parallel conversion of the photodetectors allows the transmission of digital levels, eliminating the need for high performance analog transmission lines. The proximity between the photodetector and the analog to digital converter reduces power consumption and reduces the noise introduced by the commutations of the analog multiplexer circuits. Despite the superior SNR of digital pixels, their noise performance at low illumination levels, which is dominated by the digital resolution, deteriorates when the pixel real estate is limited. Thus, there is a need to develop digital readout integrated circuits (DROICs) for imaging systems with megapixel formats that can provide adequate noise performance throughout the pixel's dynamic range.

Pixel-parallel readout approaches have been reported in recent years that employ digital pixels based on pulse frequency modulation (PFM) [2-4]. While such pixels provide supply-independent dynamic range, a direct digital output and a better signal integrity compared to analog pixels, a large pixel size is inevitable if high SNR is desired. The DROIC reported in [2], for instance, has a 15-bit ADC inside a 30μm×30μm pixel, whereas in [3], in-pixel extended counting has been employed to reduce readout noise, however, it requires additional counters and memories inside the pixel's real estate. Both implementations are not scalable with pixel dimensions. In [4], a CMOS pixel based on PFM has been reported. The SNR in that work has been improved by utilizing different sampling periods according to the intensity of illumination. This approach also utilizes an additional counter. A partially pixel parallel DROIC designed in [5], performs column parallel analog to digital conversion on the PFM residue and therefore doesn't take full advantage of the low noise digital realization.

Oversampling is a promising way of boosting the noise performance with little in-pixel area overhead. An oversampling PFM pixel reported in [6] samples the free-running photocurrent-controlled oscillator in each pixel at a constant frequency and implements a pixel-parallel first-order sigma-delta-type analog-to-digital converter. This approach requires a clock signal going to each pixel and could, therefore, pose implementation challenges in large format arrays. To this end, a novel method to oversampling and noise shaping, for PFM pixels, is proposed in this work, that doesn't require clocked in-pixel operation. By performing over-integration (integration on multiple charge packets in a single frame) and bypassing reset at the end of each integration, a high pass first order noise transfer function can be obtained. Off-pixel lowpass decimation filters, implemented in MATLAB, are used to downsample the output and filter out high frequency noise. In this way, increased resolution imaging arrays can be enabled without any additional in-pixel area and power overhead. A rigorous theoretical treatment of this technique has been carried out and included in Section II. Furthermore, measurement

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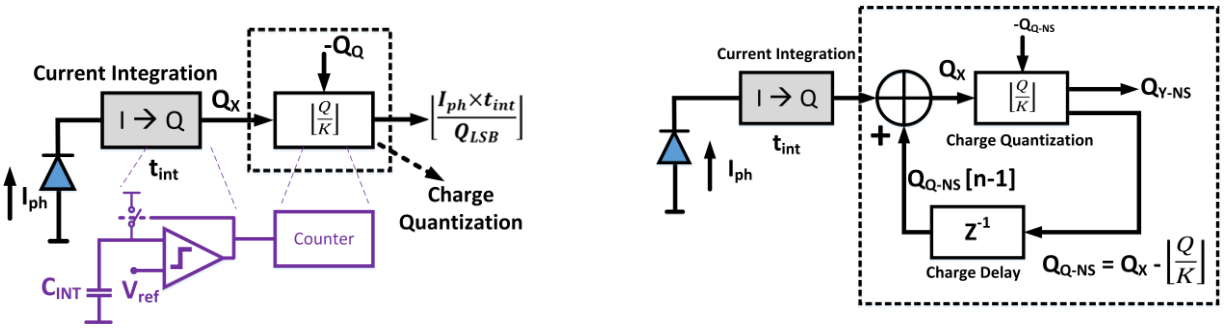

Fig. 1 Block Diagram of (a) Conventional PFM ADC (b) PFM ADC employing noise shaping

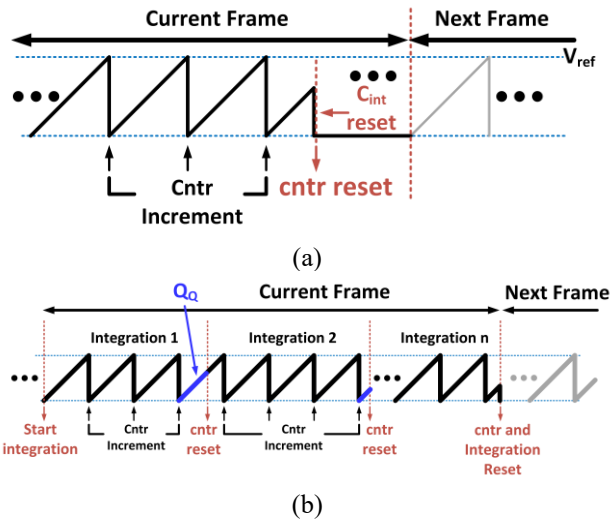

Fig. 2 Integration timing diagram of (a) Conventional PFM operation (b) PFM with over-integration

results showing the obtained readout noise can be found in Section IV.

II. Noise Shaping Using Over-Integration

In PFM based pixels, the information about pixel illumination is encoded in the instantaneous frequency of digital pulses. As shown in Fig. 1(a), these pixels typically consist of a photocurrent controlled oscillator circuit comprising a comparator, reset switch and an integration capacitor (C_{int}). When operation begins, the integration capacitor fills at a rate proportional to the photocurrent (Iph), and the progression of charging and resetting generates a pulse train whose frequency is proportional to the photocurrent. The pulse train is input to the counter, which increments its contents with each pulse until the integration ends, at which point the contents of the counter represent a quantized digital well [3].

From a mathematical viewpoint, this current-to-digital operation can be broken down into integration and floor division (integer division) denoted by the $\lfloor x \rfloor$ symbol in Fig. 1(a). Integration is performed on the input I_{ph} for an adjustable time duration t_{int}. The resulting charge (Q_X) is integer divided by the LSB charge packet (Q_{LSB}). For a comparator reference voltage of V_{ref}, Q_{LSB} can be expressed as

$$Q_{LSB} = C_{int} \times V_{ref} \tag{1}$$

The counter contents (D_{PFM}) and the equivalent quantized charge (Q_Y) at the end of integration can be written as

$$D_{PFM} = \left\lfloor \frac{I_{ph} \times t_{int}}{Q_{LSB}} \right\rfloor = \left\lfloor \frac{I_{ph} \times t_{int}}{C_{int} \times V_{ref}} \right\rfloor \tag{2}$$

$$Q_Y = (I_{ph} \times t_{int}) - Q_Q \tag{3}$$

which is essentially a digital representation of the incident photon flux. Consequently, the resulting charge quantization error (Q_q) at the end of integration is

$$Q_q = I_{ph} \times t_{int} - D_{PFM} \times Q_{LSB} \tag{4}$$

To increase the resolution of a PFM ADC under tight area constraints, the idea of oversampling and noise shaping is exploited in this work. The basic concept is that by performing over-integration (multiple integration operations in each frame) and reusing the quantization error charge and holding onto it till the next integration operation, a high pass noise transfer function can be obtained. The block diagram shown in Fig. 1(b) illustrates this approach. In conventional PFM operation, after the incident photo charge is quantized by a counter, the remaining charge on the integration capacitor is drained out before integration starts for the next frame. In the proposed PFM pixel, this residue charge ($Q_{Q\text{-}NS}$ in Fig. 1(b)) is retained and effectively added to the next photo charge sample within the same frame. The resulting counter contents ($D_{PFM\text{-}NS}$) and the corresponding quantized charge ($Q_{Y\text{-}NS}$) can be written as

$$D_{PFM-NS} = \left\lfloor \frac{I_{ph} \times t_{int} + Q_{Q-NS}(n-1)}{Q_{LSB}} \right\rfloor \tag{5}$$

$$Q_{Y-NS} = (I_{ph} \times t_{int}) + Q_{Q-NS}(n-1) - Q_{Q-NS}(n) \tag{6}$$

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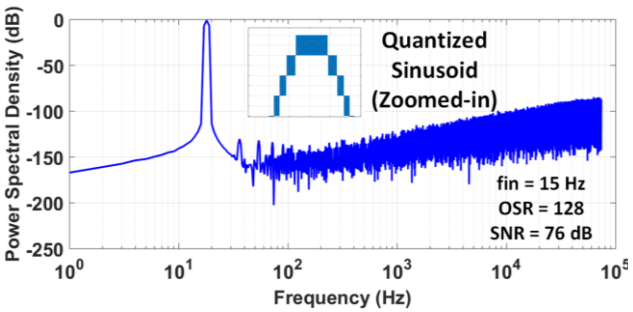

Fig. 3 Simulated PSD plot with a 12 Hz sine wave input test current

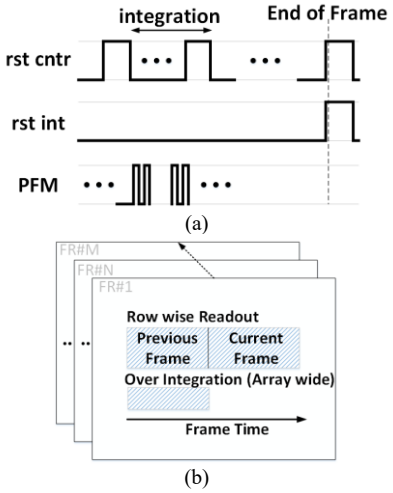

Fig. 5 (a) Pixel Timing Diagram (b) Frame-wise read out process

where Q_X is essentially the sum of the input charge and the quantization charge from the previous integration sample. The first term in (6) is the incident charge packet whereas the second and third terms form a differentiated version of the quantization error. This differentiation results in a high pass filter response that suppresses quantization noise at low frequencies and shapes it in a similar way as seen in a first order delta sigma modulator.

Fig. 2(a) depicts the integration timing diagram of a conventional single sample/frame PFM pixel. At the end of integration, both the counter contents and the integration capacitor are reset. This way, the digital resolution is limited by the counter size. On the other hand, the proposed mechanism of conveying residue charge to the next integration phase, illustrated in Fig. 2(b), provides the benefits of oversampling as well as high pass noise shaping. Instead of resetting the quantization error charge at the end of integration, it is preserved till the next integration starts. Consequently, this residue charge adds to the total incident charge being quantized (as shown through (6)).

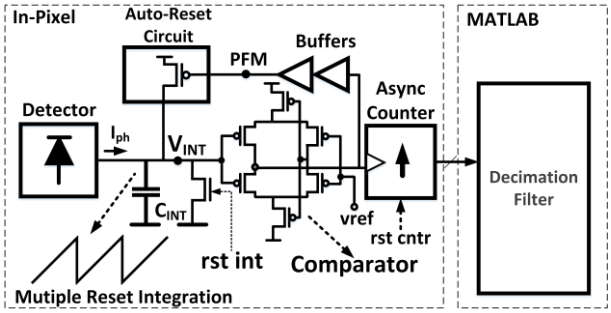

Fig. 4 Pixel Schematic

Furthermore, to validate the theoretical basis established for the proposed noise shaping in (1)-(6), a PFM ADC model was developed. The PFM model has 5 bits of in-pixel resolution. A sinusoidal test current was injected into the model and an over-integration ratio of 128 was used. The resulting power spectral density with the input bin at 15 Hz is shown in Fig. 3. An SNR of 76 dB (≈5+7.5 = 12.5 bits) was obtained that falls in the expected range.

III. Design Considerations

Given the area/complexity constraints on in-pixel circuitry, it is imperative to consider the realization cost of the proposed over-integration technique. The timing illustrated in Fig. 2(b) provides an idea about the deviation needed from the normal pixel operation. For instance, the integration capacitor is drained out at the end of the last integration within a frame instead of every integration. This means that the counter contents at the end of each integration need to be read out and passed through an off-pixel decimation filter. This can be a problem in high frame rate applications and can set an upper limit on the frame rate. To overcome this, either a fast readout clock can be employed or the residue charge at the end of integration can be held for some time before the start of next integration to spare some margin for readout.

Furthermore, choosing the optimal number of bits for the in-pixel circuitry is also crucial. While this decision largely depends on the area constraint, it also affects the noise performance of the pixel [5]. The off-pixel bits, resulting from the over-integration process, are decided based on the frame rate specifications. In the proposed design, there are 5 bits coming from the in-pixel ADC, whereas a 64 times over-integration rate allows a total of 11 bits of resolution.

Fig. 4 shows the pixel circuit. The corresponding timing control signals are depicted in Fig. 5(a). Though the pixel design is largely driven by the area constraint, the various circuit blocks have been optimized for speed and power as well. The comparator, counter and a memory circuit (not shown in Fig. 3(a)) dictate the area consumption requirement of the pixel. A compact, self-biased topology has been opted for the comparator which is based on the complementary self-biased

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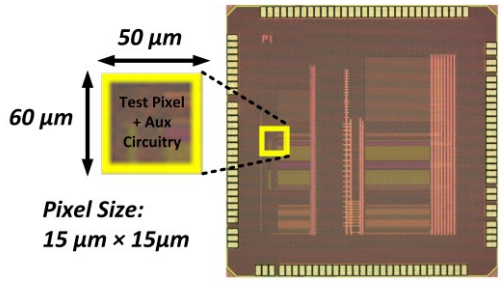

Fig. 6 Die photo with zoomed-in test pixel

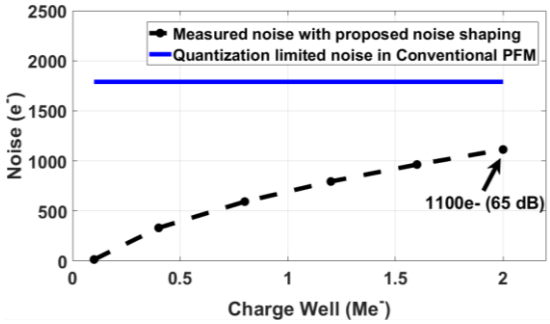

Fig. 8 Measured noise comparison with quantization limited noise in a 5-bit PFM pixel

differential amplifier architecture [7]. This topology provides switching currents higher than its quiescent current, making the PFM loop faster in high illumination conditions. The counter and memory circuits are based on static logic and their transistors have been sized for the maximum and minimum PFM frequency dictated by the test current dynamic range. Fig. 5(b) gives an indication of how an imaging array would function with the proposed method of over-integration.

IV. Experimental Results

The proposed pixel circuit is fabricated using a 90 nm 8-metal CMOS process. The pixel size is 15µm×15µm with analog buffers and digital control circuitry placed outside the pixel. A PMOS device mimics the infrared detector providing current in the medium-wave infrared detector range (300pA – 3nA). Fig. 6 shows a micrograph of the chip. The chip has been measured at room temperature and works with a 1.2 V power supply. Fig. 7 shows the measurement waveforms taken from a logic analyzer. With a fixed input test current, the serial data is read out for many frames. The signals DW, Reset Cap and Shift Enable correspond to pixel data write, capacitor reset at the end of a frame and shift enable of an output data serializer respectively. These measurements have been taken at different input test currents (not shown) with a fixed integration time. This data has been used to characterize the pixel in terms of its readout noise. With an integration capacitor (C_{INT}) of 20 fF, V_{ref} of 0.5 V, an over-integration ratio of 64, and 5 bits of in-pixel resolution, the readout noise in terms of electrons has been measured and calculated. Fig. 8 shows the plot of readout noise vs charge well fill. A worst-case readout noise of 1100e- at the full well capacity is measured. This noise has been compared with the quantization noise dominant noise of a conventional 5-bit PFM pixel. The reduction in the readout noise in this work is due to the noise shaping operation that takes the pixel outside

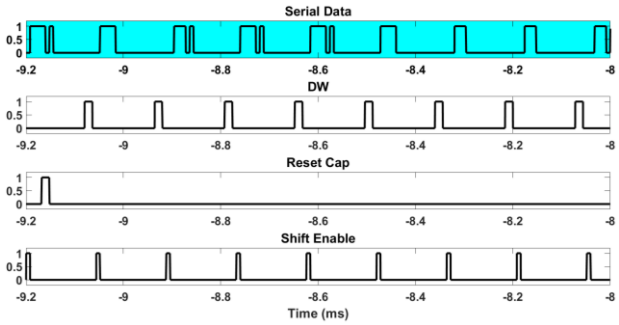

Fig. 7 Measured pixel data at mid-range input current

of the quantization noise limited regime. Finally, the measured power is 100 nW with an over-integration ratio of 64. Table I summarizes the main specifications and compares this work with previously reported readouts employing PFM based pixels. The figure of merit (FOM) for the prototype pixel (defined in [3]) is 488 fJ/conv. Note that for a fair comparison, power consumption of off-pixel circuits is not included in FOM computation. Performance comparable to Nyquist readouts [2], [5] is obtained. While the fully pixel parallel architecture of [2] achieves a better SNR, the presented oversampling based design offers the potential for higher SNR by increasing the over-integration ratio. Thanks to a low pixel power consumption accompanied by a competitive SNR, the proposed noise shaping technique achieves a better FOM.

TABLE I. Comparison with state of the art

	This work	**[2] (2009)**	**[5] (2017)**
Pixel Pitch	15 µm	30 µm	15 µm
Readout Noise	1100e- (65 dB)	(73 dB)	1500e- (62 dB)
Resolution	11 bits	15 bits	16 bits
Pixel power	100 nW	500 nW	100 nW
Frame Rate	50 Hz	100 Hz	400 Hz
FOM	488 fJ/conv	558 fJ/conv	520 fJ/conv

V. Conclusion

A method to shape the quantization noise of PFM pixels is presented in this paper. The proposed technique is targeted at large format imaging arrays. A test pixel prototype has been designed and fabricated in a 90nm CMOS process. By employing oversampling and time-based quantization charge transfer between successive charge packets, a reduced readout noise has been demonstrated. The proposed approach circumvents the inevitable large area requirement of digital pixels, which is expected to persist in advanced technology nodes. With a simple pixel structure, the proposed oversampling architecture promises improved digital resolution and an effectively lower readout noise owing to the improvement in the resulting quantization noise. With a 100 nW/pixel power consumption, the presented digital pixel architecture serves as a potential enabler of imaging systems demanding a small pixel pitch.

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