7-bit Phase Shifter using SiGe BiCMOS Technology for X-band Phased Array Applications

by

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Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of
Master of Science

Sabancı University

Summer, 2017

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for X-band Phased Array Applications

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DATE OF APPROVAL: 01/08/2017

Acknowledgements

First and foremost, I would like to thank my advisor Prof. Yaşar Gürbüz, for his invaluable advice and support during my undergraduate and master's studies in Sabanci University. I would not be at this stage of my career without his support and endless motivation.

I also would like to thank Assoc Prof. Meriç Özcan and Asst. Prof. Erdinç Öztürk for taking their precious time to serve in my thesis committee and for their valuable comments and feedback.

I am very thankful to my friends and colleagues, Eşref Turkmen and İlker Kalyoncu for always helping me along the way our research, their patience answer to my endless questions. I also would like to thank my companions in the SU Microsystems group, Dr. Melik Yazıcı, Dr. Ömer Ceylan, Alper Güner, Murat Davulcu, Emre Can Durmaz, Elif Gül Özkan Arsoy, Atia Shafique, Arman Galioğlu, Can Çalışkan, and Shahbaz Abbasi for creating such a friendly working environment, including the past members Barbaros Çetindoğan, Berktuğ Üstündağ, and Emre Özeren. I am happy to be a part of this group. I thank the laboratory stuff Ali Kasal and past member Mehmet Doğan for their help and support.

In addition, thanks to Ahmet Can, Alican, Didem, Emre, Metin, Onur, Ozan, Recep and many others for your dear friendship during my college and high school years.

Finally, but most importantly, I would like to thank my parents Huriye and Erdal, my sister Betül, and my fiancee Betül for their unconditional love and endless support. I would not come that far without their support and the sacrifices they made.

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EE, Master's Thesis, 2017
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Keywords: Phased Array RADAR, Phase Shifter, T/R module, SiGe BiCMOS, X-Band Integrated Circuits.

Abstract

Phase array T/R modules achieve high performance with III-V technologies. However, the cost of III-V technologies is high. Recent developments in SiGe BiCMOS technology show us that III-V technology can be replaced with SiGe BiCMOS. Moreover, thanks to the integration of the CMOS, digitally controlled T/R modules can be realized with that technology. Power dissipation, area, and integration complexity can be reduced with SiGe BiCMOS technology. Also, the number of radiating elements and the cost of T/R module can be reduced with phase shifters with high phase resolution. In the light of these trends, this thesis presents a 7-bit low insertion-loss SiGe X-band (8-12 GHz) passive phase shifter, realized in IHP 0.25-μm SiGe BiCMOS process.

The phase shifter is based on high-pass/low-pass filter topology with a new proposed switching technique. This technique decreases the number of series switch by dividing each phase into 4 arms instead of two arms. Also, in this technique, instead of using two single pole switches consecutively, multiple pole switches are realized. Thanks to the IHP SiGe BiCMOS technology, isolated NMOSs are used which improve insertion-loss of the phase shifter. The overall phase shifter is composed of BALUN, SP4T, DP4T, 4P4Ts, and phase blocks to create a phase shift for achieving 7-bit phase resolution. The return loss of each state is better than 10 dB and the phase shifter has an average of 14.5 dB insertion loss. Minimum 1° RMS phase error is obtained at 10 GHz. RMS phase error is better than 6° at 9-11 GHz band. The phase shifter occupies an area of 6 mm^2 and it has no DC power consumption.

The thesis also summarizes the work that was contributed as part of the complete TR Module generation. These include active and passive gain equalizers that are utilized in the Module to generate desired slope in the receiver / transmitter chain.

X-band Faz Dizinleri için SiGe BiCMOS 7-bit Faz Kaydırıcı

Abdurrahman Burak
EE, Yüksek Lisans Tezi, 2017
Tez Danışmanı: Prof. Dr. Yaşar GÜRBÜZ

Anahtar Kelimeler: Faz Dizinli RADAR, Faz Kaydırıcı, Alıcı/Verici Modülü, SiGe BiCMOS, X-Bandında entegre devre.

Özet

III-V teknolojisi ile faz dizinli alıcı/verici (T/R) modüllerinden yüksek performans elde edilir. Buna rağmen, III-V teknolojilerinin maliyeti yüksektir. SiGe BiCMOS teknolojisindeki son gelişmeler, III-V teknolojisinin SiGe BiCMOS ile yer değiştirebileceğini göstermektedir. Dahası, CMOS'un entegrasyonu sayesinde dijital olarak kontrol edilebilir T / R modüller bu teknoloji ile gerçekleştirilebilir. SiGe BiCMOS teknolojisiyle güç dağıtımı, alanı ve entegrasyon karmaşıklığı azaltılabilir. Üstelik, yüksek bit çözünürlüklü faz kaydırıcılar ile radyasyonlu elemanların sayısı ve T/R modüllerin maliyeti azaltılabilir. Bu eğilimler ışığında, bu tezde, 7 bitlik düşük araya yerleştirme kaybına sahip SiGe BiCMOS teknolojisinde gerçekleştirilmiş Xband(8-12GHz) pasif faz kaydarıcı sunulmaktadır.

Faz kaydırıcı, yeni önerilen anahtarlama tekniğiyle beraber yüksek geçiren / düşük geçiren süzgeç topolojisine dayanmaktadır. Bu teknik, her fazı ikiye bölmek yerine dörde bölerek seri switch sayısını azaltmaktadır. Dahası, bu teknikte, ard arda tek bitişli anahtarlar kullanmak yerine çok bitişli anahatlar gerçekleştirilmiştir. IHP SiGe BiCMOS teknolojisi sayesinde, faz kaydırıcının araya yerleştirme kaybını geliştiren izole NMOSlar kullanıldı. Bu method faz kaydırıcının araya yerleştirme kaybını geliştirmektedir. 7-bit faz çözünürlüğünü elde etmek için faz kaydırıcı BALUN, SP4T, DP4T, 4P4T ve faz bloklarından oluşmaktadır. Her durumun geri dönüş kaybı 10 dB'den daha iyi, ve faz değiştirici ortalama 14.5 dB araya yerleştirme kaybına sahiptir. 10 GHz'de minimum RMS faz hatası 1 ° olarak elde edilmiştir. RMS faz hatası, 9-11 GHz bantında 6 ° ' den daha iyidir. Güç tüketmeyen faz kaydırıcı 6 mm^2 alana sahiptir.

Tezde, tamamlanmış T/R modül üretimine katkı sağlayan çalışmaları da özetlemektedir. Bunlar, alıcı / verici zincirinde istenen eğimi oluşturmak için modülde kullanılan aktif ve pasif kazanç edengeleyicileri içerir.

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List of Abbreviations

AF	Array Factor
AM	Amplitude Modulation
BALUN	Balanced to Unbalanced
BV_{CEO}	Collector-Emitter Breakdown Voltage
BV_{CBO}	Collector-Base Breakdown Voltage
CB	Common-Base
CCB	Constant Current Biasing
CE	Common-Emitter
CVB	Constant Voltage Biasing
DBF	Digital Beam Forming
DE	Drain Efficiency
EIRP	Equivalent Isotropically Radiated Power
FM	Frequency Modulation
FOM	Figure-of-Merit
GaAs	Gallium-Arsenide
HP	High Pass
IC	Integrated Circuit
IF	Intermediate Frequency
IL	Insertion Loss
InP	Indium phosphide
iNMOS	Isolated NMOS
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Pass
MEMS	Microelectromechanical System
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuits
mm-Wave	Millimeter-wave
MOS	Metal-Oxide-Semiconductor
OAE	Overall Efficiency
PA	Power Amplifier
PAE	Power-Added-Efficiency
PAWS	Phased Array Warning System
PS	Phase Shifter
RADAR	Radio Detecting And Ranging
RF	Radio Frequency
RMS	Root Mean Square
RX	Receiver
SiGe	Silicon-Germanium
SPDT	Single-Pole Double-Throw
SP4T	Single-Pole Four-Throw
DP4T	Double-Pole Four-Throw
4P4T	Four-Pole Four-Throw
T/R	Transmit/Receive
TX	Transmitter
VGA	Variable-Gain Amplifier

1 Introduction

1.1 A Brief History of Radar

Radio Detection and Ranging (Radar) is a system for detecting the current information such as direction, distance and speed of the aircraft, ships, and other objects. Radars detect objects by sending out radio waves from a source which are reflected off the object back to the source. A radar uses electromagnetic radiation at high radio frequency in order to detect and locate remote reflecting objects. Then, the radiation is sent out in pulse form with a few second duration and these pulses are separated with "silent" intervals. Pulses which are sent out from the receiver are returned from the detected objects to the receiver. The detected objects are displayed by the receiver. The distance of the detected object is measured thanks to the speed of wave multiplied by the duration of the returned pulse signals from "target". The direction of the detected object is determined by use of highly directive radio antennas [9].

The history of the Radar begins with the invention of "Telemobiloskop" which is a device operating at 650 MHz by the German Cristian Hülsmeyer in May 1904 . This device is capable of detecting the presence of ships but it cannot detect the movement and distance of the ships. In 1914, Nikola Tesla introduced the idea of radar. In 1922, a lecture on the principle of radar was delivered by Guglielmo Marconi. In 1934, cargo ship Oregon and the ocean liner Normandie used the radar system which was installed by the French Emilie Girardeu [10].

During the World War II, radars played an important role to win the war. Mechanically scanned radars achieved hundreds scans per minute and they help to increase the visible area. The mechanically scanned radar system is replaced with the electronically scanned arrays, which is called as "phased arrays". This way of scanning achieved hundreds of scans per second and therefore they are commonly used in the military applications[11].

1.2 Phased Array Radars

Today, phased array radar technology is used in both military and civilian applications. The number of civilian applications is increasing and we can see some

examples from the civilian applications such as 5G, automotive radar, weather monitoring and radio astronomy. By placing a phased array into the automobile, collision avoidance is provided by measuring the distance between the placed car and an obstacle [12]. 5G systems are the great solution for boosting user data rates to accommodate rapidly increasing traffic demands of the user in the future in cellular technology [13]. In order to detect the place of storms, atmospheric and airborne hazards, phased arrays are used to monitor the results [14]. Sensitive phased arrays receive signals from the sky and detect gas, or other objects in the sky [15].

Although many examples are shown in civilian applications, phased array systems are mainly used in military applications. Fig.1a is one of the examples of the surface radar which is produced in the United States and called as AN/TPS-75 [1]. Fig. 1b is an example of ballistic missile warning radar system which is used for detecting missiles from the long-range and creates an early warning [2]. This radar is called as AN/FPS-132 and it is produced in the United States.

Phased array systems have more advantage than the conventional radar applications. Conventional radar applications are steering the beam by rotating the antenna mechanically. The mechanical rotation creates a reliability problem and a rotation time is needed to beam towards a single target. Phased array systems eliminate the reliability problem of the mechanical part and beam positioning does not need a mechanical rotation. Therefore, it takes less time than the conventional radar applications. Phased array systems can provide multi-target operation by targeting different frequencies at once. As a result, a multi-channel operation is created and it can increase data rates in communication application.

In phased arrays, the number of radiating elements directly increase the spatial resolution. Transmit/receive modules form the radiating elements and, phase and amplitude of the signal are controlled inside these modules. Today, GaAs, InP or SiGe are used for realizing these modules.

1.3 Phased Array Operating Principles

The block diagram of the phased array system in a receiver mode is shown in Fig. 2. Assume that the distance between each antenna is d, the θ is the angle where the signal comes from a targeted source, the distance to reach the signal at

Figure 1: AN/TPS-75 [1] (a) and AN/FPS-132 [2] (b) phased array radars

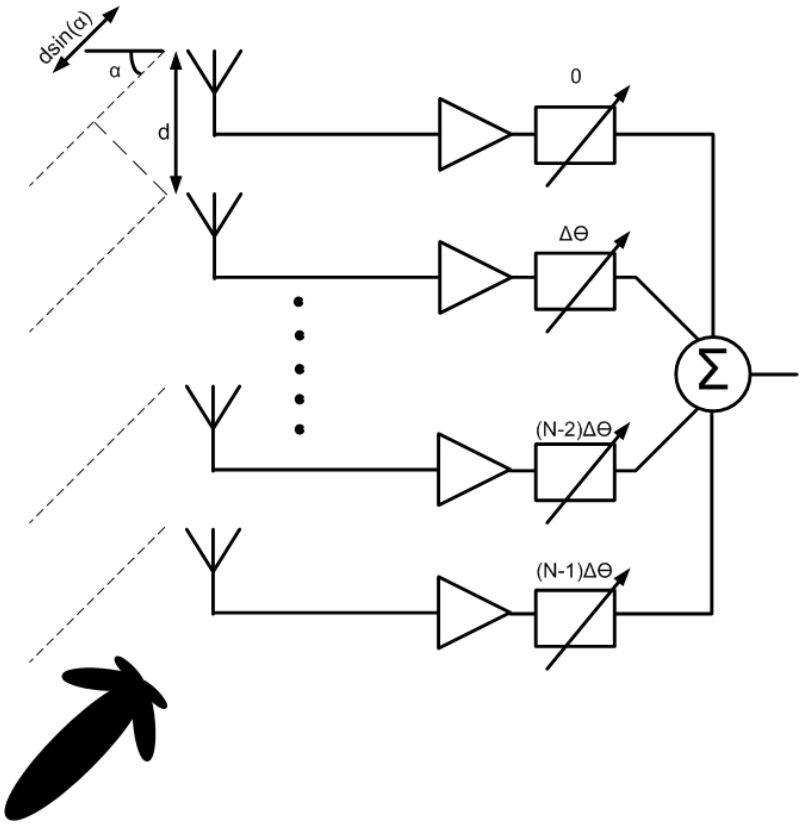

Figure 2: Basic receiver block diagram of a phased array system

i_{th} element can be found from

$$\delta d_i = id \sin\theta \tag{1}$$

The travel differences to each antenna element create a progressive time delay and phase difference. The comparison of the phased arrays based on time delays and the phase shift is provided in the following section.

1.3.1 Time Delay vs Phase Shift

In order to find the time delay of the radiating element, the travel distance of each antenna is divided by the speed of the light. From this division, time delay of the i_{th} element is found as $\frac{id\sin\theta}{c}$. In order to find the phase difference of the radiating element, a carrier frequency is multiplied with the time delay. From this multiplication, the phase difference of the i_{th} element is found as $w_c\frac{id\sin\theta}{c}$. This can be rewritten as

$$\Delta_\phi = 2\pi\frac{d\sin\theta}{\lambda} \tag{2}$$

These time delay and phase difference will be used in defining the receiving signal. Generally, the k_{th} radiating element receive the signal as shown in (4).

$$S_0(t) = A\cos(\omega t + \phi_0(t)) \tag{3}$$

$$S_k = S_0(t - k\Delta_\phi) \tag{4}$$

$$S_k = A\cos(w(t - k\Delta_t) + \phi(t - k\Delta_\phi)) \tag{5}$$

These equations are also valid for transmitter part of the radar systems because they are reciprocal. From these equations, depending on the control mechanism, timed-arrays and phased-arrays mechanisms are appeared as a solution. Due to the independence from the frequency of timed-arrays, they provide a much wider solution. However, due to the insertion-loss, noise, and nonlinearity of building blocks, it is hard to implement timed-arrays, especially for RF applications [16]. Consequently, in order to control the electronic beam, phase shifters draw the attention on employing the antenna system. As a result, phased array radars consist of thousands of radiating elements and by controlling the phase and amplitude of each element, the effective radiation pattern is created in the desired direction [17].

1.3.2 Beam Steering and Array Factor

In phased array systems, by adjusting the phase shift and amplitude of the system in each transmitter/receiver channel, the main beam direction can be steered.

The angle between main beam direction and the array normal is dependent on the distance between each antenna element and incremental phase shift of each channel. This dependency can be found from (6) which is the rewritten version of (2).

$$\theta = \sin^{-1}\left(\frac{\lambda}{2\pi d}\Delta\phi\right) \tag{6}$$

From this equation, the beam direction has a dependency only to the distance between each antenna elements and incremental phase shift value of each channel. When the distance between each antenna is increased, the beam width gets smaller, consequently, it increases the directivity of the antenna. However, after some point, increasing the spacing between each antenna creates grating lobes which make the phased array system more sensitive to interferer signals. The general distance between each antenna is chosen as $\frac{\lambda}{2}$.

When the array factor and antenna element is multiplied, the radiation pattern of an array is found[18]. Normalized array factor of a long(L>>λ) and uniform linear antenna array is given as

$$AF = \frac{\sin\left(N\frac{\psi}{2}\right)}{N\sin\left(\frac{\psi}{2}\right)} \tag{7}$$

where N is the number the antenna elements. This equation gives us, more antenna number will provide narrower main beam. As a drawback, more side lobe levels appear in the one period of ψ. Normalized array pattern of a linear array with $\frac{\lambda}{2}$ spacing with a different number of antenna is given in Fig. 3. From this figure, we can see that when the number of the antenna increases, the narrower main beam appears.

1.3.3 Phased Array as a Receiver and Transmitter

A phased array system needs to receive the signal with a low noise value from each channel. Assume that the number of phased array is N, the summed power of the received signal with N radiating element can be found as

$$S_{sum} = n^2 G S_{in} \tag{8}$$

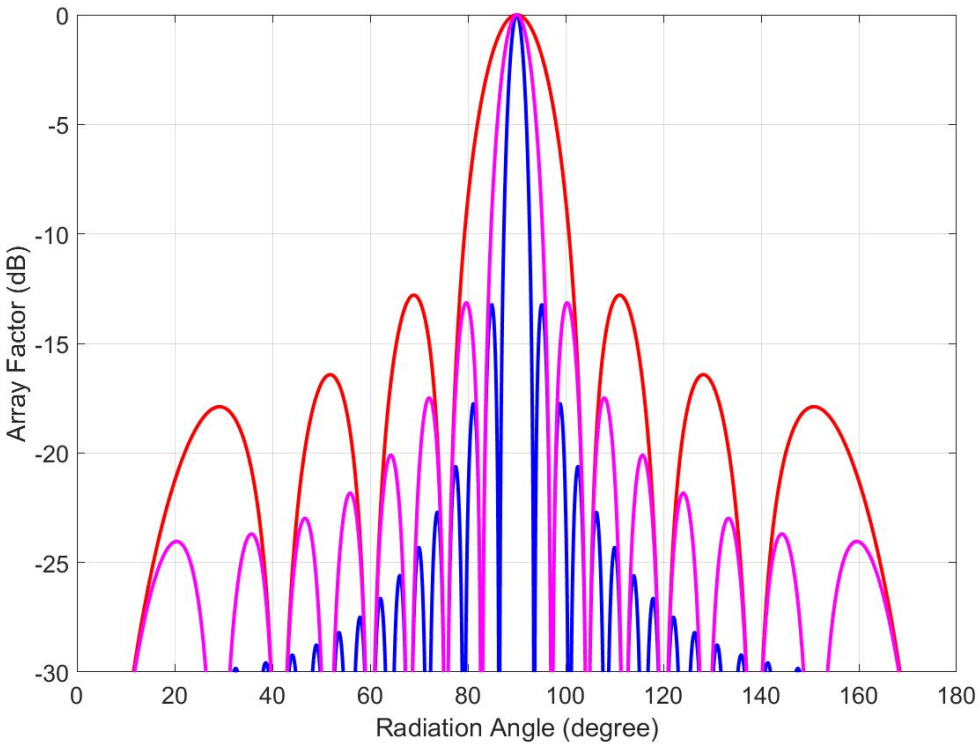

Figure 3: Normalized array pattern of a linear array with $\lambda/2$ spacing for (red) N=8 (magenta) N=16 (blue) N=32 antenna elements

where S_{in} is the input power in each receiver channel, G is the power gain of each receiver channel, n is the number of channels or antenna elements, and S_{sum} is the summed signal power at the receiver output.

Assuming that noise contributions of different receiver channels are uncorrelated, their signal powers (not voltages) are added at the receiver output, which can be written as

$$Noise_{sum} = nG\left(N_{ant} + N_{rec}\right) \tag{9}$$

where N_{rec} is the noise power added by each receiver channel, N_{ant} is the noise power feeding from an antenna, and $Noise_{sum}$ is the combined noise power at the receiver output. Signal to noise ratio is found from the ratio of (8) and (9). From this ratio, we can see that the antenna element is directly proportional with the SNR. In order to improve the SNR of the system, the more antenna can be used. The drawback of using more antenna in the system is the cost and power consumption.

Using multiple channels also increases the radiated power in the main beam

direction [19]. The overall radiated antenna can be found from the multiplication of the square of the antenna number with the power of each radiating element. From this multiplication, the effective isotropic radiated power (EIRP) of an N-element active phased array in the main beam direction is N^2P watt [20]. This equation can be interpreted as the more antenna element will result as the more radiated power in the main beam direction. This ability can handle the drawback of the less output power of SiGe based power amplifiers due to the low-breakdown voltages with respect to III-V technologies.

1.4 Phased Array Architectures

Phased array systems feed the antenna in two ways. The first way is feeding the antenna with a single high-performance low-noise amplifier(LNA) in receiving side and single high-performance power amplifier(PA) in transmitting side. Both sides is connecting to the multiple phase shifters and antennas. This approach is called as passive phased arrays. The second way is feeding each antenna with each low noise amplifier, power amplifier, and phase shifter separately. This approach is called as active phased arrays.

The way the phase shifting functionality is realized is another categorization type of the phased array systems. In this context, phased arrays divided into four groups, RF phase shifting, IF phase shifting, LO phase shifting and digital beam forming.

1.4.1 Passive Phased Arrays

Block diagram of the passive phased arrays is shown in Fig.4. As we can see from the figure, passive phased arrays consist of a very high output power PA in transmit mode and very high noise performance LNA in receiver mode. These modes are connected to multiple passive phase shifters and radiating elements through a circulator. Since all elements are passive and using one LNA and one PA in this architecture, power consumption is low. Moreover, this architecture can be used in high power applications. One of the examples of using this architecture is showed in Fig. 5 is AN/FPQ-16 which is introduced in 1975 in United States [3].

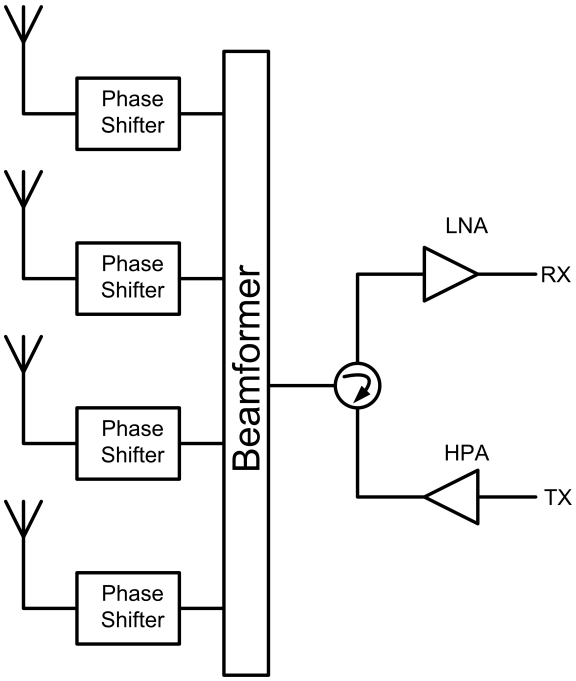

Figure 4: Block diagram of passive phased array

Figure 5: Passive Phased array example: AN/FPQ-16 [3]

1.4.2 Active Phased Arrays

Block diagram of the active phased arrays approach is shown in Fig.6. As we can see from the figure, each antenna element has its own active transmit/receive (T/R) module. Inside this module, PA, LNA, phase shifters and switches are used. One of the examples that uses this architecture is shown in Fig. 7, SAMPSON which is introduced in United Kingdom [4].

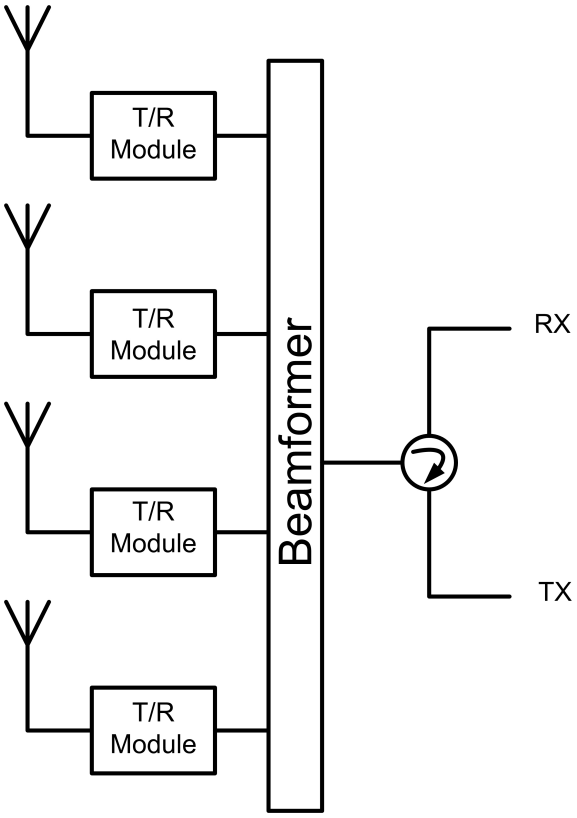

Figure 6: Block diagram of active phased array

Figure 7: Active phased array example: SAMPSON[4]

Active phased arrays consume high power and cannot deal with high power

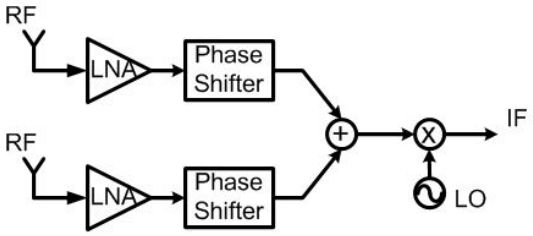

Figure 8: RF phase shifting Phased array architectures

applications. However, this architecture is more reliable since each element has its own LNA and PA. In passive phased array structure, if one failure occurred in LNA or PA whole structure will fail. In this architecture, if one LNA or PA fail, only this part of the whole structure will fail. In receiving part, LNA is the first block in the active phased array structures. In passive phased array structures, antenna, phase shifter, and circulator receive the signal before the LNA. These blocks create a loss on the signal path. As a result, the noise performance of the active phased arrays is better than the passive phased arrays. These passive structures are also placed after PA in transmit mode. Therefore, due to this loss, output power performance of the active phased arrays is better than the passive phased arrays.

1.4.3 RF phase shifting(All RF Transmit/Receive)

Fig. 8 shows the RF phase shifting(All RF Transmit/Receive) approach. RF phase shifting is the most dominant approach since it is the most compact approach than other phase shifting types. A single mixer is used after the RF combining part in this approach. The advantage of using a single mixer is that LO distribution network is not necessary.

1.4.4 IF phase shifting

Fig. 9 shows the IF phase shifting approach. In this approach, phase shifters are realized in IF domain. Because passive component values are inversely proportional with frequency, passive component values are high in this approach. Moreover, in this approach, each radiating elements has its own mixer. Consumed power is increasing in this approach because of individual mixer components.

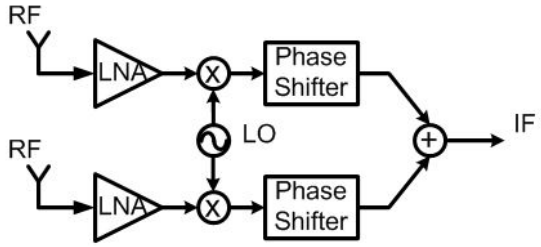

Figure 9: IF phase shifting Phased array architectures

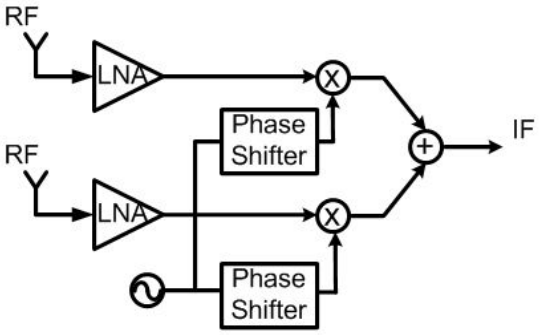

Figure 10: LO phase shifting Phased array architectures

1.4.5 LO phase shifting

Fig. 10 shows the LO phase shifting approach. In this approach, a single mixer is used for each radiating element. However, phase shifters are no longer exist in RF part of phased array. Therefore, the drawbacks of the phase shifter are eliminated with this approach such as insertion-loss, noise figure, and noise. The problem with this approach is that due to the realization of phase shifters in LO part, the distribution network is required for this part. As a result, a more complex system is required in this approach.

1.4.6 Digital beam forming

Fig. 11 shows the digital beam forming phase shifting approach. In this approach, phase shifting is performed in digital domain instead of analog or RF domain. The advantage of this approach is that a large number of beams is synthesized by using a digital signal processor (DSP)[21]. The disadvantage of this approach is interference rejection only occurs after signal combining. Therefore, the dynamic range requirement of mixers increases, consequently, power consumption of mixers increases. This approach also needs separate ADC for each radiating element. It

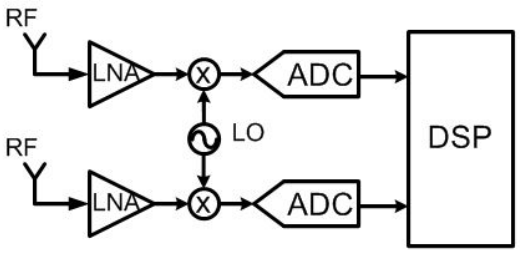

Figure 11: Digital beam forming Phased array architectures

also increases the power consumption of the phased array.

1.5 All RF Transmit/Receive Module

As explained in previous section, all RF T/R module has compact design and does not need LO distribution network. This architecture enables the phase shift in RF front end structure. RF front end phase shifting enables high phase resolution with low area and, consequently, it decreases the required number of element for each phased arrays. Due to the tendency for higher phase resolution, low area and low cost all RF T/R module is selected as a T/R module structure. The performance of active phased arrays strongly depends on the performance of transmit/receive (T/R) modules. In T/R modules, several blocks are realized. In order to amplify the received signal from the environment, low noise amplifier (LNA) is used. In order to transmit the signal to the environment with a high power, a power amplifier (PA) is used. Transmit and receive parts of a module has to be isolated from each other. LNA and PA need to be switchable in the module. This ability is provided with single-pole-double-throw (SPDT) switches. Phase shifters(PS) and variable gain amplifiers(VGAs) determine the performance parameter of T/R module. The aim of PS is to change the angle of the signal without changing the amplitude of the signal. The aim of the VGA is to change the amplitude of the signal without changing the phase of the signal.

In Fig. 12, different approaches on system-level architectures for all T/R modules is shown. Fig. 12.a shows that transmit and receive part of T/R module is separated from each other and high isolation can be achieved with this approach. However, the number of PS and VGA increases in this approach. As a result, the power consumption of this approaches increases.

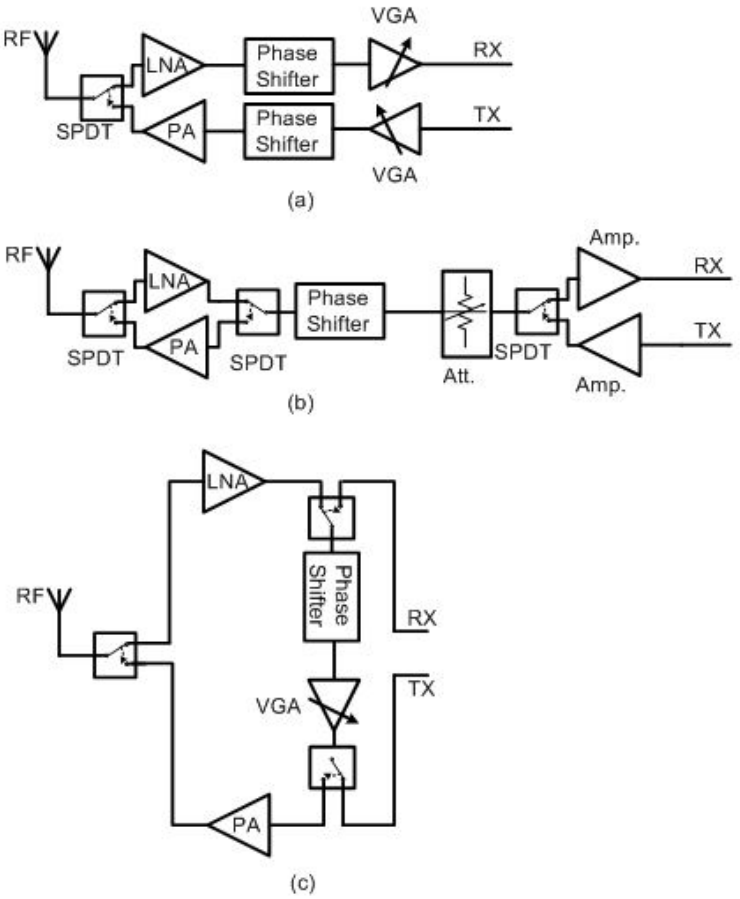

Figure 12: Several system level architectures for RF transmit/receive modules

Fig. 12.b shows that PS and VGA must be bidirectional because, in both modes of T/R module, these blocks are used on two sides. Therefore, passive phase shifter and attenuator must be used in this approach. By using passive elements with this approach, the gain requirement of PA and LNA increase to compensate the losses from these sub-blocks. Additional SPDT also increases the loss on the signal path.

Fig. 12.c shows the solution for the direction problem of previous approaches. Moreover, with this approach isolation requirement of the SPDTs decreases. Thanks to the direction solution single direction of sub-blocks can be used in this approach. Active phase shifters and VGAs decrease the gain requirement of amplifiers.

1.6 SiGe BiCMOS Technology

In RF applications, III-V, RF BiCMOS and RF CMOS technologies play an important role in realizing T/R modules for phased array applications. III-V tech-

nologies have the best performance parameters with respect to others. However, integration problems and high product cost are drawbacks of this technology. Recent advances in RF CMOS technologies show us high f_t, f_{max} and low f_{min} values are achieved with low cost and easy integration. However, the layout of the RF CMOS changes these parameters. In other words, parasitic resistances and capacitances create a reliability problem on this technology. Today, SiGe BiCMOS enables to realize T/R modules for phased array applications without performance sacrifice when compared with III-V technologies and with less parasitic dependence with respect to RF CMOS. Thanks to this technology, the advantages of Si can be used with the same speed and performance with respect to the III-V technologies.

f_t is the cutoff frequency where the current gain of transistor β becomes unity. f_{max} is the maximum oscillation frequency where the power gain of a transistor becomes unity. These two parameters are important in RF engineering because the highest they are, the larger gain they can achieve and the lower noise figure can achieve. The relationship between minimum noise figure level and f_t is shown in 10

$$NF_{min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_c}{V_t}\left(r_e + r_b\right)\left(\frac{f^2}{f_t^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}} \tag{10}$$

As we see from the equation, f_t is inversely proportional with NF_{min}. In order to increase the f_t of the transistor, Ge is used with Si. In bipolar transistors, SiGe alloys are grown as base part of the transistor. Si has a band-gap of 1.12 eV and Ge has a bandgap of 0.66 eV. By combining Si with Ge enables injecting more electrons and as a result, current gain, β, of the transistor increases. Moreover, adding Ge to the base of a transistor increases the speed of carriers. This leads a decrement of the base transit time τ_b. The relationship between f_t and τ_b is shown in

$$f_T = \frac{1}{2\pi}\left(\tau_b + \tau_c + \frac{1}{g_m}\left(C_\pi + C_\mu\right) + \left(r_e + r_c\right)C_\mu\right)^{-1} \tag{11}$$

where τ_c is the transit time in collector region, g_m is the transconductance, C_π and C_μ are base-emitter and base-collector junction capacitances, r_e and r_c are emitter and collector resistances [8]. The g_m of the transistor is increased by increasing β_{DC} of the transistor. The higher f_T for the transistor is achieved via τ_b and g_m.

As mentioned before, another important parameter of the transistor is f_{MAX},

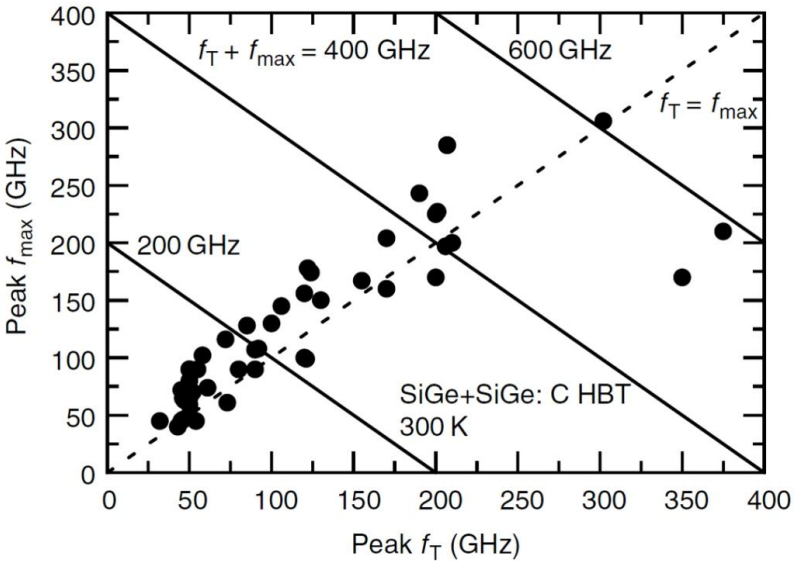

Figure 13: (f_T) and (f_{MAX}) for different SiGe HBT technologies. [5]

where is shown as

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}} \tag{12}$$

where r_b is intrinsic base resistance. Another advantage of Ge with Si instead of pure Si, while adding doping into the base of the transistor, the current gain of the transistor does not reduce. In Si based and SiGe based transistors, the increment of doping reduces r_b. Without reducing current gain of transistor enables high noise performance without gain loss of transistor.

Adding Ge doping in the base region, all important high-frequency parameters increase. Fig. 13 shows reported f_T and f_{MAX} values for different SiGe HBT technologies.

The most important advantages of SiGe over other its III-V counterparts is the ability to integrate with CMOS. III-V technologies still achieve the highest output power level and the lowest noise figure level but the advancements on SiGe BiCMOS offers a competitive solution. Moreover, the cost and yield performance is increased with this technology. Furthermore, digital baseband and RF front-end blocks can be easily integrated into SiGe BiCMOS. A comparison between SiGe HBTs with alternative technologies is presented in Table 1.

Today, ultrahigh performance phased arrays which are mainly used in military applications can be realized in III-V technologies. However, SiGe technologies can

Table 1: Relative performance comparison of different IC technologies (Excellent: ++; Very Good: +; Good: 0; Fair: –; Poor: – –) [8]

Performance Metric	SiGe HBT	SiGe BJT	Si CMOS	III-V MESFET	III-V HBT	III-V HEMT
Frequency Response	+	0	0	+	++	++
1/f and Phase Noise	++	+	–	– –	0	– –
Broadband Noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output Conductance	++	+	–	–	++	–
Transconductance	++	++	– –	–	++	–
Power Dissipation	++	+	–	–	+	0
CMOS Integration	++	++	N/A	– –	– –	– –
IC cost	0	0	+	–	–	– –

be used instead of these technologies in both military applications and civilian applications due to the low-cost, fully-integrated structure, less area, and system-on-chip solutions for microwave and millimeter wave phased array applications.

1.7 Motivation

Phase array T/R modules achieve high performance with III-V technology. However, the cost of III-V technologies is high. Recent developments in SiGe BiCMOS technology show us III-V technology can replace with SiGe BiCMOS. Moreover, thanks to the integration of the CMOS, digitally controlled T/R modules can be realized with that technology. Power dissipation and integration complexity can be reduced in SiGe BiCMOS. On the other hand, the limited breakdown voltage, the high noise levels reduce the performance of phased arrays with SiGe BiCMOS. Therefore, low sensitive receiver chain and low output power transmitter can be realized with SiGe BiCMOS. Taking everything into account, SiGe technologies can be used in phased arrays instead of III-V technologies with same performance parameters.

The objective of this thesis is to design integrated electronic phase shifter, the most important element in phased arrays, for- X-band. Passive phase shifter based on III-V technologies can achieve low insertion-loss with the conventional design techniques due to the high-quality passive components. Low-insertion-loss can also

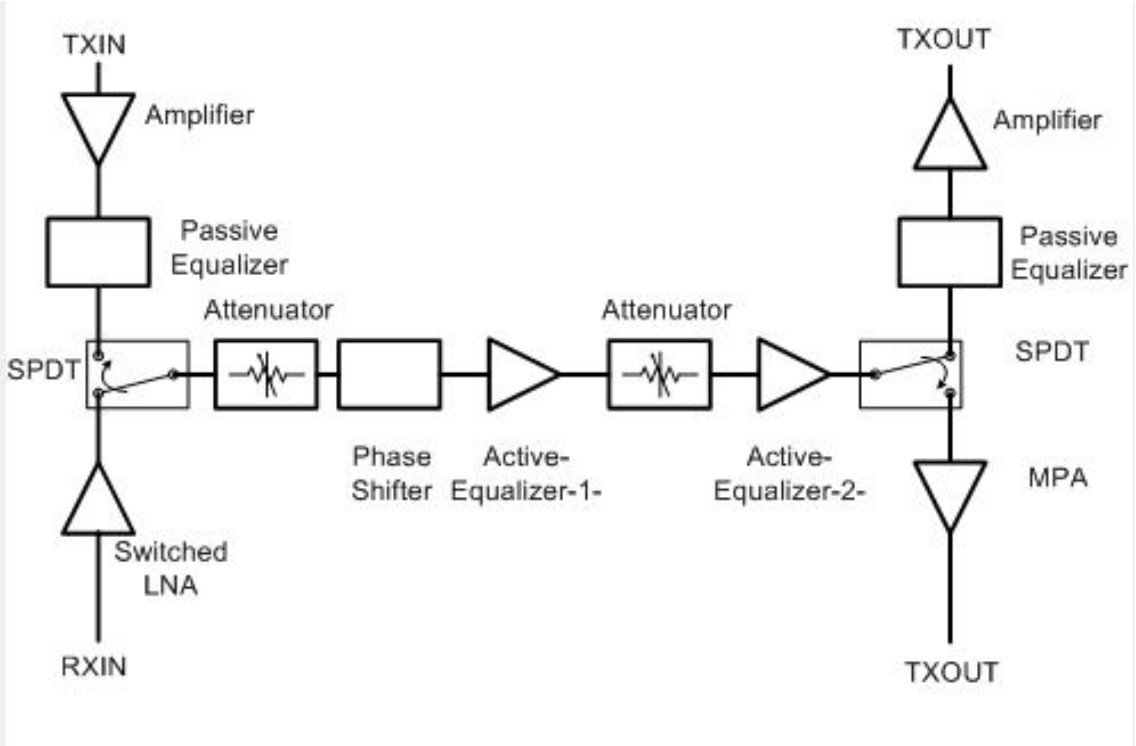

Figure 14: SiGe X-band all-RF T/R module block diagram and component specifications

be achieved with the reduction of the series switches on the passive phase shifter. In order to improve the insertion-loss aspect of the passive phase shifter, in this thesis, new switching methodology is employed and this thesis is devoted to the development of phase shifter designs utilizing passive approaches rather than active topologies. Moreover, in collaboration with my colleagues, in T/R module 3-dB positive slope gain is aimed. In order to achieve this gain-behavior, on T/R module which is shown in Fig. 14, two positive slope gain behavior passive gain-equalizers and two positive slope gain behavior amplifiers are presented to balance the negative slope gain-behavior previously designed amplifiers.

1.8 Organization

This thesis includes five chapters which are organized as follows. Chapter 2 introduces the different approaches on the phase shifter and compares the different topologies of the phase shifters. This chapter continues with the explanation of the advantages of using passive phase shifters instead of active phase shifters.

Chapter 3 begins with the design of high-performance low insertion-loss 7-bit

passive phase shifter. Specifically, approach on the passive phase shifter is explained the simulation result of the 7-bit passive phase shifter is depicted in this chapter.

Chapter 4 expresses the design considerations for achieving positive slope gain T/R Module. Specifically, measurement and simulation results of two active gain-equalizers and two passive gain-equalizers are demonstrated to achieve this gain behavior.

Chapter 5 concludes the thesis with the summary of work and provides information on possible future studies.

2 Fundamentals of Phase Shifters

2.1 Introduction

In this chapter, fundamentals of phase shifters will be covered. This chapter begins with a brief description of the phase shifter. Then, categorization of the phase shifters will be done with different approaches. Important performance parameters of the phase shifter will be explained. In order to achieve the best performance, how different topologies performed the phase shift operation is discussed in the following section. At the end of the chapter, the effect of quantization error is discussed.

2.2 A Brief Description of Phase Shifter

In phased array systems, the phase control of the signal is utilized by phase shifters. They are used to change the transmission phase angle, in other words, phase of S21, of a network. The phase shift is achieved in a controlled way. Ideally, this block varies the phase between 0 and 360 degrees without creating an insertion-loss. Moreover, the insertion-losses of each phase state are the same. The important and challenging parameters of the phase shifters are phase resolution, RMS phase error, RMS amplitude error, bandwidth, chip size, linearity, and power dissipation.

2.3 Classification of Phase Shifters

Phase shifters can be controlled in two ways: Analog and Digital. Analog phase shifters vary the phase between 0 and 360 degrees in a continuous way. Digital phase shifters vary the phase between 0 and 360 degrees in a discrete way.

Analog phase shifters achieve the continuous phase shift generally with a voltage control. Varactor diodes have the dependency on the voltage. By changing the voltage, the capacitance of the diode changes, as a result, continuous way phase shift is achieved.

Digital phase shifters achieve the discrete phase shift by “bits”. Each bit has at least two states. One of the states of the “bit” is called as an “ON” and other states of the “bit” are called as an “OFF”. The phase differences between the “ON” state and “OFF” state is called as an achieved phase shift. In digital phase shifters, MSB,

most significant bit, is defined as the largest bit and LSB, least significant bit, is defined as the lowest bit. Assume that the range of the phase shifter is between 0 and M, in the N bit phase shifter, MSB is found as $M/2$ and LSB is found as $M/2^N$. For example, assume that phase shifter covers between 0 and 360 degrees, if the bit number of the phase shifter is 3, the LSB of the phase shifter is 45 degrees. If the bit number of the phase shifter is 6, the LSB of the phase shifter is 5.62 degrees. In both cases, the MSB of the each phase shifter is 180 degrees.

Between these two approaches, digital phase shifters are more common due to the immunity to the noise contribution of the voltage lines. In analog phase shifters, voltage lines lead the noise contribution on the block.

2.4 Important Performance Metrics of the Phase Shifter

In RF-IC blocks, performance parameters are the key part of the designs. The comparison between each block is decided with respect to these results. In general, input and output return loss, noise; insertion-loss or gain, power consumption, linearity, chip size, bandwidth, and stability are common key parameters for all RF-IC blocks. Specifically, in phase shifters, RMS phase error, RMS amplitude error, and an effective number of bits determine the performance of the phase shifter. In this section, we focus on the performance metrics which are specific for phase shifters.

2.4.1 RMS Phase Error

In the phase shifter, there is always an error between the desired phase shift value and the obtained phase shift value. These phase errors are different for each phase state and these values are changing with the frequency. In order to describe the errors of the phase shifter, root-mean square of each phase state is found. To find this value, the phase error between each phase state and the desired phase shift is found. These errors are summed up for each frequency and defined as a common error. This common error is added to each phase state. The error between the desired phase states and the phase states with an addition of common error is found. The standard deviation of these errors is defined as RMS phase error. The formula of the RMS phase error is defined as:

$$\theta_{\Delta,rms}(f) = \sqrt{\frac{\sum_{i=2}^{2^N} |\theta_{\Delta_i}(f)|^2}{2^N - 1}} \tag{13}$$

Where $\theta_{\Delta i}$ denotes the phase error between the desired phase shift and the obtained phase shift at the i_{th} state and N is the number of bits of the phase shifter. Generally, RMS phase error is the minimum at the center frequency and increases for higher and lower frequencies.

2.4.2 RMS Amplitude Error

An ideal phase shifter changes the phase of the transmission angle without changing the amplitude of transmission. However, in real life, it is not practicable. Amplitude error occurs in phase shifter because while changing the phase of the transmission, the amplitude of the transmission also varies. RMS amplitude error is defined with respect to the average amplitude of the phase shifter. In order to define the amplitude error of the phase shifter, RMS amplitude error can be expressed as

$$A_{\Delta_{rms}}(f) = \sqrt{\frac{\sum_{i=1}^{2^N} \left(\Delta A_i(f)\right)^2}{2^N}} \tag{14}$$

where ΔA_i is the error between the amplitude of the i_{th} state and the average amplitude. N is the number of bits of the phase shifter.

2.4.3 Effective Number of Bits

The effective number of bits determines the useful bandwidth of the phase shifter. If the phase shifter has N bits in terms of an effective number between two frequencies, the useful bandwidth of the phase shifter is called as the between these two frequencies.

During the design period of the phase shifter, N bit performance is aimed and therefore N stage has "ON" and "OFF" states. However, due to the RMS phase error of the phase shifter, an effective number of bits is defined in a different way. In order to have N effective number of bits, the RMS phase error must be lower than LSB/2 for that specific N. For example; a phase shifter who has 5-bit operation has LSB value 11.25 degree. Therefore, RMS phase error must be lower than 5.62.

2.5 Phase Shifter Topologies

Phase shift operation is realized with different topologies. These topologies can be grouped into two main categories: Passive phase shifter and active phase shifter. An active phase shifter consumes power during the phase shift operation and generally provides gain. A passive phase shifter does not consume power during the phase shift operation. Due to the passive networks, this type of phase shifter generally introduces attenuation.

On the one hand, active phase shifters have better insertion-loss, better noise figure value, wider bandwidth operation, and smaller size than the passive phase shifters. On the other hand, passive phase shifters have better linearity, less power consumption. Common passive phase shifter topologies are switched-line, loaded-line, reflection-type, and switched-filter. Common active phase shifter topology is the vector modulator.

2.5.1 Switched-Line Phase Shifter

As shown in Fig. 15, switched line phase shifter operates as a true time delay element. This delay is determined by the difference of two path lengths. Ideally, phase shifter based on time delay operation gives the wide-band solution. However, practically, the time delay is not the same different frequencies. Moreover, additional path causes an additional loss and therefore amplitude error of the phase shifter increases. In this type of phase shifter, SPDTs degrade the performance of the phase shifter. This type of phase shifter cannot reach high bit resolution in wide-band operation region and RMS amplitude error of this phase shifter is high. We can see some switched-line type phase shifter examples in literature[22][23][24].

2.5.2 Loaded-Line Phase Shifter

As shown in Fig. 16, in loaded-line phase shifters, $\lambda/4$ transmission line is connected with either inductance or capacitances. By changing the load of the transmission line, the line characteristic changes. The advantage of this topology consumes less area than switched-line topology. The disadvantage of this topology is return loss depends on the desired phase shift. This dependency may lead an amplitude difference while combining next stage. Due to the dependency on λ, this

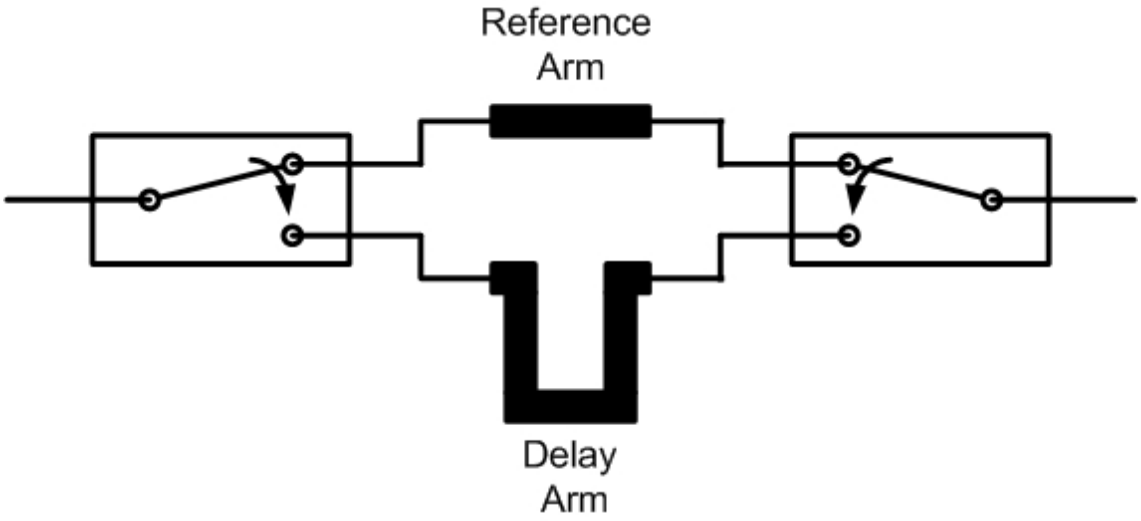

Figure 15: General diagram of the bit of the switched-line phase shifter

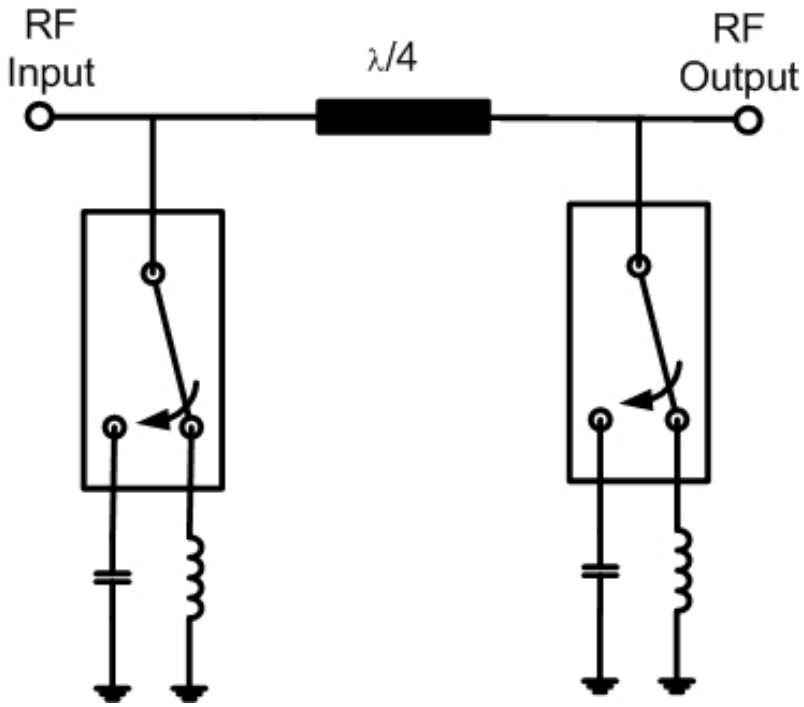

Figure 16: General diagram of the bit of the loaded-line phase shifter

type of phase shifter still has narrow-band operation problem and cannot reach high bit resolution [25].

2.5.3 Reflection-Type Phase Shifter

As shown in Fig. 17, a reflection type of phase shifters perform the phase shift operation using a circulator or coupler. RF input is directly connected to one port of the coupler, RF output is directly connected to another port of the coupler. Last

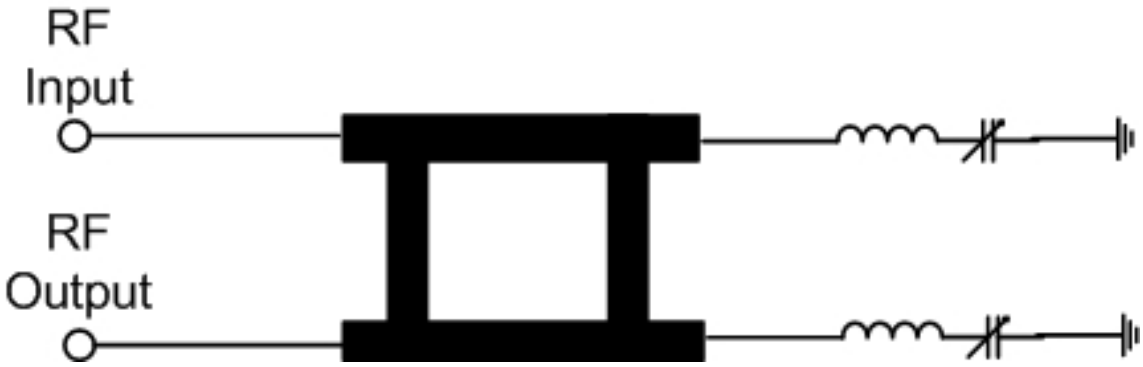

Figure 17: General diagram of the bit of the reflection-type phase shifter

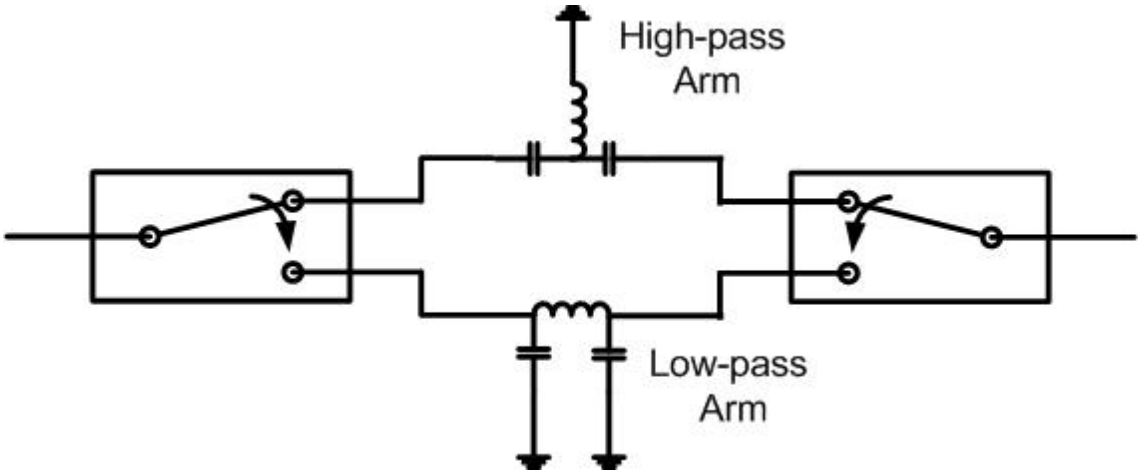

Figure 18: Switched-filter topology with tee networks

two ports of the coupler are terminated with variable loads. These loads generate the desired phase shift. These type of phase shifters use in millimeter-wave. The advantage of this type of phase shifters is better insertion-loss and better return loss performances due to the isolation between ports. However, this type of phase shifters cannot reach 360 degrees cover range[26] [27] [28] [29].

2.5.4 Switched-Filter Phase Shifter

As shown in Fig. 18, switched-filter type phase shifters have a high-pass filter or low-pass filter networks to achieve phase shift operation. In one arm, these filters can achieve 90-degree phase shift. By using one type of filter in one arm and using another type of filter in the reference arm, the 180-degree phase shift can be achieved. Ideally, this type of phase shifter achieves desired phase shift at the center frequency. Practically, due to the passive components, RMS phase error degrades dramatically due to narrow-band operation.

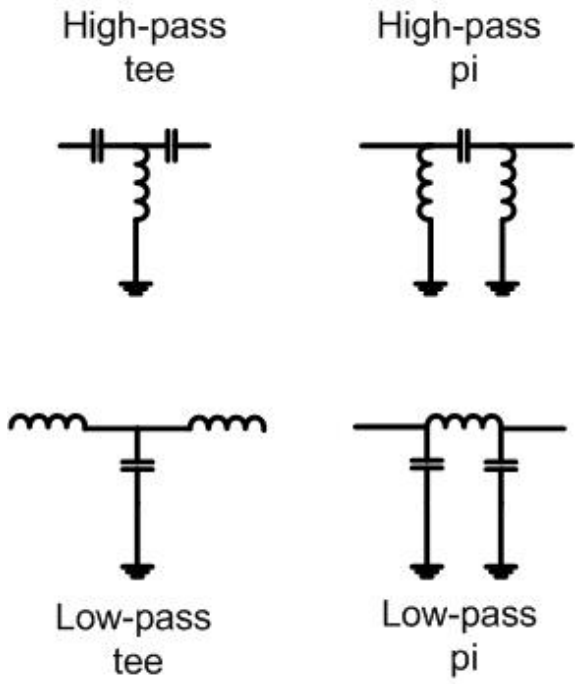

Figure 19: Tee and pi filter networks

In this topology, Π and T type of filters can be used in arms. Equations for ideal lumped elements are shown in the formula in this order: High-pass tee, Low-pass tee, High-pass pi, Low-pass pi [30]. These networks are shown in Fig. 19.

$$L_1 = \frac{Z_0}{2\pi f \sin(\phi)} \quad \& \quad C_1 = \frac{\sin(\phi)}{2\pi f Z_0 (1-\cos(\phi))} \tag{15}$$

$$L_2 = Z_0 \frac{(1-\cos(\phi))}{2\pi f \sin(\phi)} \quad \& \quad C_2 = \frac{\sin(\phi)}{2\pi f Z_0} \tag{16}$$

$$L_3 = \frac{Z_0 \sin(\phi)}{2\pi f (1-\cos(\phi))} \quad \& \quad C_3 = \frac{1}{2\pi f Z_0 \sin(\phi)} \tag{17}$$

$$L_4 = Z_0 \frac{\sin(\phi)}{2\pi f} \quad \& \quad C_4 = \frac{(1-\cos(\phi))}{2\pi f Z_0 \sin(\phi)} \tag{18}$$

Some examples of high-pass/low-pass filter based phase shifter can be seen in the literature. Although, achieving phase shift operation without consuming power, they have narrow-bandwidth operation and large size [31] [32].

2.5.5 Vector Modulator Phase Shifter

The figure of the vector modulator type phase shifter depicts in Fig. 20. By using all-pass RLC filters or hybrid couplers, the input signal is divided into four quadra-

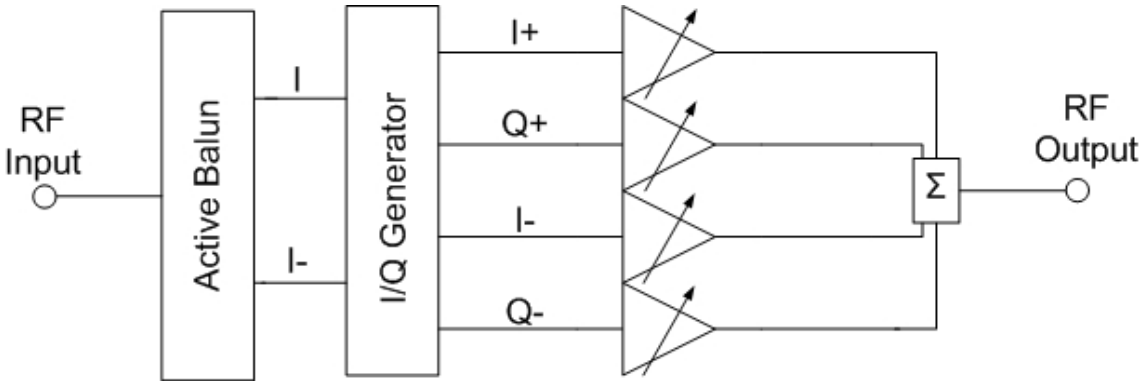

Figure 20: Block diagram of a typical vector sum type phase shifter

ture vector: in-phase plus($I+$), quadrature-phase plus($Q+$), in-phase minus(I-), quadrature-phase minus(Q-). These vectors are amplifying by VGAs and adding these signals to create the output of the phase shifter. VGAs determine the amplitude of each quadrature vector and in order to achieve desired phase shift, gain setting of each VGAs is determined. High phase resolution, less area, low RMS phase error can be achieved with this type of phase shifter. However, power consumption, omnidirectional structure, and linearity are the drawbacks of vector modulator phase shifter[33] [34] [35].

2.6 Quantization Loss of the Phase Shifter

Due to the discrete phase shift operation of the digital phase shifter, it can change the phase of transmission with constant pre-defined values. For instance, if the phased array wants to steer the beam in $\theta = 63$ degrees, and as we found in previous sections, $\lambda/2$ spacing is required for antenna spacing, Δ_θ must be 153 degrees. Since digital phase shifter cannot operate this operation in a continuous way, 153 degrees will be provided with the closest phase shift value. If the phase shifter has 5 bits, this value is 157.5 degrees. The difference between the desired phase shift and required phase shift creates a quantization error. This quantization error degrades the overall performance of the phased array systems.

3 A 7-bit X-band Switched Filter Phase Shifter in SiGe BiCMOS

3.1 Introduction

In this chapter, design and analysis of 7-bit X-band switched-filter based phase shifter will be covered. In section 3.2 the requirement of a designed phase shifter is discussed. Then, in section 3.3, the analysis on the pi and tee networks will be given. The methodology used in phase shifter design is explained in detail in section 3.4. At the end of the chapter, the simulation results of the phase shifter are shown.

3.2 Phase Shifter Requirements

Phase shifter requirements can be listed as: Bit-resolution, RMS phase error, power dissipation, and insertion-loss. As shown in Fig. 21 the improvement of the bit resolution of the phase shifter decreases the number of the required antenna element to satisfy the same side-lobe level [6]. 7-bit is required to decrease the number of radiating elements. T/R modules should have the capability of adjusting the phases correctly for not inhibiting the performance degradation of the receiver sensitivity and output power of the transmitter. Therefore, low RMS phase error is required. Two important building blocks of a T/R module are phase shifters and attenuators. The phase shifter determines the phase resolution of the T/R module and the attenuator provides the amplitude control of the T/R module. Since these blocks are used in all T/R module arrays, the power consumption of the whole module is linearly proportional to the power dissipation of these blocks. In the light of the discussion in Chapter 2, switched-filter topology is chosen to meet the bit resolution, RMS phase error, and power dissipation requirements. In order to handle the insertion-loss problem of this type of phase shifter, new switching networks are employed.

3.3 High-Pass and Low-Pass Pi and Tee Networks

Switched-filter based phase shifters are based on high-pass/low-pass Π and T networks. Schematic views of these networks are shown in Fig. 19. As shown in the

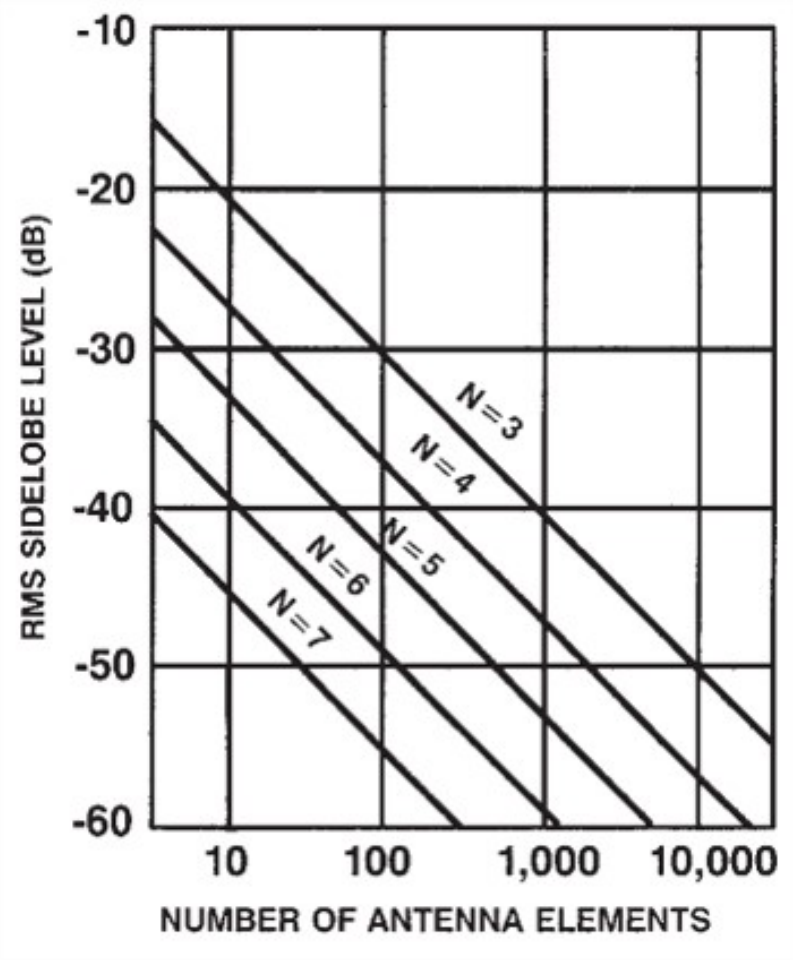

Figure 21: Required antenna number to reach the same RMS side-lobe level with different phase resolutions [6]

figure, high-pass tee and low-pass pi networks provide the phase shift operation with one inductance while other two networks perform the phase shift operation with two inductances. Due to the large size of the inductances, high-pass tee and low-pass pi networks are generally chosen. The analysis of each network will be provided in this section.

These networks are the core part of the phase shift operation in this type of phase shifter. During the phase shift operation, two requirements must be satisfied: Input and output parts must be matched to 50Ω and the phase of S21 must be equal to the desired phase shift.

These networks can be represented as an ideal transmission-line because both of them has the same properties such as they are matched to 50Ω and they have ideal phase shift. Due to this likeness, these networks are represented with ABCD parameters and equalized to the well-known transmission line as shown in following

matrix:

$$\begin{bmatrix} cos(\theta) & jZ_0 sin(\theta) \\ jY_0 sin(\theta) & cos(\theta) \end{bmatrix}$$

3.3.1 High-pass Tee Network

High pass tee network has two series capacitances and a parallel inductance in between. ABCD matrix for the series capacitance can be written as:

$$\begin{bmatrix} 1 & \frac{1}{jwC_1} \\ 0 & 1 \end{bmatrix}$$

ABCD matrix for the parallel inductance can be written as:

$$\begin{bmatrix} 1 & 0 \\ \frac{1}{jwL_1} & 1 \end{bmatrix}$$

In order to find ABCD matrix of the overall system, ABCD matrix of the series capacitance is multiplied with ABCD matrix of the parallel inductance and finally this result is multiplied with the ABCD matrix of the series capacitance again. The result of the first multiplication is:

$$\begin{bmatrix} 1 - \frac{1}{w^2 C_1 L_1} & \frac{1}{jwC_1} \\ \frac{1}{jwL_1} & 1 \end{bmatrix}$$

This result is multiplied with the series capacitance and result of the second multiplication is:

$$\begin{bmatrix} 1 - \frac{1}{w^2 C_1 L_1} & \frac{2}{jwC_1} - \frac{1}{jw^3 C_1^2 L_1} \\ \frac{1}{jwL_1} & 1 - \frac{1}{w^2 C_1 L_1} \end{bmatrix}$$

This matrix is equalized to the ABCD matrix of the transmission line. From this equation derivation of L_1 and C_1 values is shown in (19 - 23).

$$\frac{1}{jwL_1} = jY_0 sin(\theta) \tag{19}$$

$$L_1 = \frac{Z_0}{wsin(\theta)} \tag{20}$$

$$1 - \frac{1}{L_1 C_1 w^2} = cos(\theta) \tag{21}$$

$$1 - \frac{1}{\frac{Z_0}{sin(\theta)} C_1 w} = cos(\theta) \tag{22}$$

$$C_1 = \frac{sin(\theta)}{wZ_0(1 - cos(\theta))} \tag{23}$$

3.3.2 Low-pass Tee Network

Low pass tee network has two series inductances and a parallel capacitance in between. ABCD matrix for the series inductance can be written as:

$$\begin{bmatrix} 1 & jwL_2 \\ 0 & 1 \end{bmatrix}$$

ABCD matrix for the parallel capacitance can be written as:

$$\begin{bmatrix} 1 & 0 \\ jwC_2 & 1 \end{bmatrix}$$

In order to find ABCD matrix of the overall system, ABCD matrix of the series inductance is multiplied with ABCD matrix of the parallel capacitance and finally this result is multiplied with the ABCD matrix of the series inductance again. The overall result of the these multiplications is:

$$\begin{bmatrix} 1 - w^2 L_2 C_2 & 2jwL_2 - jw^3 L_2^2 C_2 \\ jwC_2 & 1 - w^2 L_2 C_2 \end{bmatrix}$$

This matrix is equalized to the ABCD matrix of the transmission line. From this equation derivation of L_2 and C_2 values is shown in (24 - 27).

$$jwC_2 = jY_0 sin(\theta) \tag{24}$$

$$C_2 = \frac{sin(\theta)}{wZ_0} \tag{25}$$

$$1 - w^2 L_2 C_2 = cos(\theta) \tag{26}$$

$$L_2 = \frac{Z_0(1 - cos(\theta))}{wsin(\theta))} \tag{27}$$

3.3.3 High-pass Pi Network

High pass pi network has two parallel inductances and a series capacitance in between. In order to find ABCD matrix of the overall system, ABCD matrix of the parallel inductance is multiplied with ABCD matrix of the series capacitance. Then, this result is multiplied with the ABCD matrix of the parallel inductance again. The overall result of the these multiplications is:

$$\begin{bmatrix} 1 - \frac{1}{w^2 L_3 C_3} & \frac{1}{jwC_3} \\ \frac{2}{jwL_3} - \frac{1}{jw^3 C_3 L_3^2} & 1 - \frac{1}{w^2 L_3 C_3} \end{bmatrix}$$

This matrix is equalized to the ABCD matrix of the transmission line. From this equation derivation of L_3 and C_3 values is shown in (28 - 31).

$$\frac{1}{jwC_3} = jZ_0 sin(\theta) \tag{28}$$

$$C_3 = \frac{1}{wZ_0 sin(\theta)} \tag{29}$$

$$1 - \frac{1}{w^2 L_3 C_3} = cos(\theta) \tag{30}$$

$$L_3 = \frac{Z_0 sin(\theta)}{w(1 - cos(\theta))} \tag{31}$$

3.3.4 Low-pass Pi Network

Low pass pi network has two parallel capacitances and a series inductance in between. In order to find ABCD matrix of the overall system, ABCD matrix of the parallel capacitance is multiplied with ABCD matrix of the series inductance. Then, this result is multiplied with the ABCD matrix of the parallel capacitance

again. The overall result of the these multiplications is:

$$\begin{bmatrix} 1 - w^2 L_4 C_4 & jwL_4 \\ -w^2 C_4^2 + w^4 L_4 C_4^3 & 1 - w^2 L_4 C_4 \end{bmatrix}$$

This matrix is equalized to the ABCD matrix of the transmission line. From this equation derivation of L_4 and C_4 values is shown in (32 - 35).

$$jwL_4 = jZ_0 sin(\theta) \tag{32}$$

$$L_4 = \frac{Z_0 sin(\theta)}{w} \tag{33}$$

$$1 - w^2 L_4 C_4 = cos(\theta) \tag{34}$$

$$C_4 = \frac{1 - cos(\theta)}{w Z_0 sin(\theta)} \tag{35}$$

All these equations can be summed up as

$$L_1 = \frac{Z_0}{w \sin(\phi)} \quad \& \quad C_1 = \frac{\sin(\phi)}{w Z_0 (1 - \cos(\phi))} \tag{36}$$

$$L_2 = Z_0 \frac{(1 - \cos(\phi))}{w \sin(\phi)} \quad \& \quad C_2 = \frac{\sin(\phi)}{w Z_0} \tag{37}$$

$$L_3 = \frac{Z_0 \sin(\phi)}{w (1 - \cos(\phi))} \quad \& \quad C_3 = \frac{1}{w Z_0 \sin(\phi)} \tag{38}$$

$$L_4 = Z_0 \frac{\sin(\phi)}{w} \quad \& \quad C_4 = \frac{(1 - \cos(\phi))}{w Z_0 \sin(\phi)} \tag{39}$$

These equations will be used in the calculation of the desired phase value of each bit of the phase shifter.

3.4 Circuit Design

The conventional schematic of the phase shifter based on high-pass/low-pass filters is depicted in Fig. 22. Generally, this network is based on two passive filter networks and two SPDT switches for each bit. When SPDTs are switched to up, high-pass arm shifts the phase of the signal. When SPDTs are switched to low, low-pass arm shifts the phase of the signal. Ideally, these high-pass and low-pass

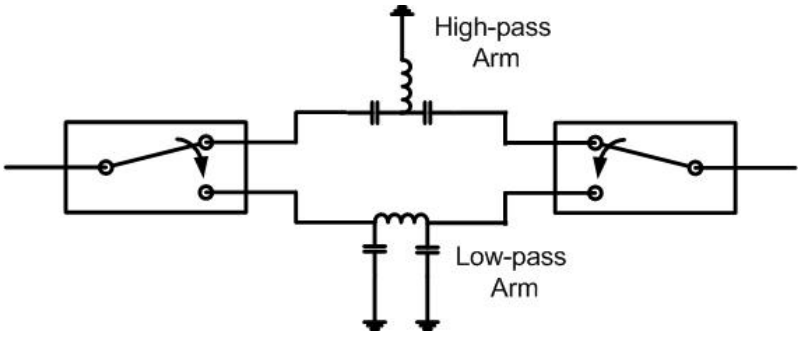

Figure 22: Schematic view of high-pass/low pass type phase shifter

networks shift the phase without changing the amplitude of the signal. However, due to the loss of the switches and the parasitics of the lumped components insertion-loss occurs.

In order to decrease the insertion-loss of the phase shifter, the number of used switches can be decreased. Two methods are proposed to decrease the number of switches: Number of the arms are increased from two to four in the first proposed method. Since the number of arm is increased to four, SP4Ts are employed instead of SPDTs. Each SPDT or SP4T has one series switch which is the main reason of the insertion-loss of the switched-base phase shifter. The overall series switch number of the phase shifter is decreased by increasing the number of arms. Consequently, the insertion-loss of the phase shifter decreases with this method.

The second proposed method improves the insertion-loss of the phase shifter by using 4P4Ts instead of cascading two SP4Ts. This method also decreases the number of series switch of the phase shifter. From one bit to another, two series switches are used when two cascaded SP4Ts are used. From one bit to another, one series switch is used when 4P4T is used. The overall number of the series switch is decreased from 6 to 4 with this method.

In order to realize switches, the isolated NMOS transistors offered by IHP 0.25-μm BiCMOS technology is used. The cross section of the isolated NMOS is shown in Fig. 23. Moreover, body floating technique is used in isolated NMOS. The body of the transistor is floated with connecting 10K Ω to the ground. Isolated NMOS and body floating technique implemented on the transistors improve the insertion-loss of the switches and increase the linearity of the switches.

Only the phase shifters with even number of bits can be designed by cascading each arm with 4P4Ts. In order to obtain 7-bit operation, one of the bits should

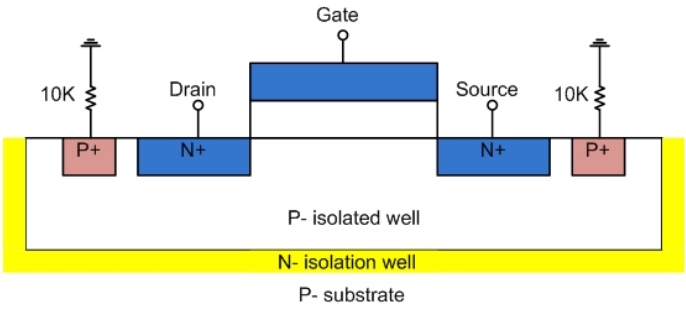

Figure 23: Cross section of typical isolated NMOS transistor and body floating technique

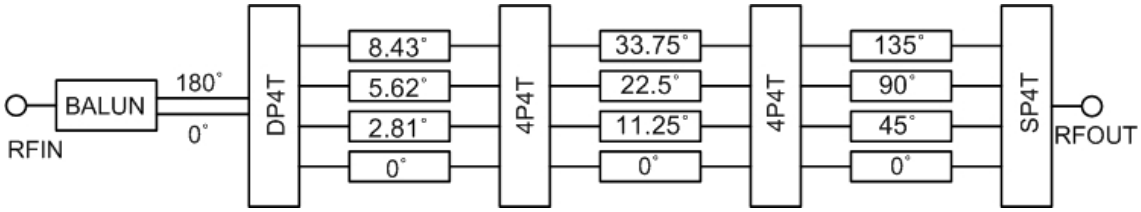

Figure 24: Block diagram of 7-bit passive phase shifter

be connected with two arms. Passive phase shifters cannot achieve high phase degrees with low phase errors. Two arms are connected with 180 degrees in order to reduce the phase error of the phase shifter. Moreover, in that part, BALUN is used for decreasing the phase error of the phase shifter. In this way, 180 degrees phase difference is obtained with ±0.5 dB phase error which is better result than the conventional high-pass/low-pass arm.

Block diagram of the designed phase shifter is depicted in Fig. 24. Two outputs of the BALUN is connected to 4 arms with DP4T switch. These four arms are connected with 4P4T to another four arms. The second 4P4T is used for connecting the third part of the phase shifter to fourth part of the phase shifter. Lastly, SP4T is used to connect the four arms to the output. Overall 7-bit phase shifter block is employed with 3 series switches instead of 14 series switches. Consequently, a low-insertion-loss is achieved with this switching technique.

The drawback of this design is having more complex structure in the digital part. In the conventional 7-bit passive phase shifter, the 7-bit digital control unit is directly connected with the switches in order to obtain the desired phase. The number of switches increases with the proposed switching method. Therefore, The phase of the block is controlled by the 7-bit digital control unit with multiplexers. As a result, digital part of the phase shifter becomes more complex.

Table 2: Ideal lumped element values for X-band 7-bit phase shifter

	Tee Network		Pi Network		Tee Network		Pi Network	
	High-pass		High-pass		Low-pass		Low-pass	
	L_1	C_1	L_2	C_2	L_3	C_3	L_4	C_4
	nH	pF	nH	pF	nH	pF	nH	pF
180 degree	0.795	0.318	0.795	0.318	0.795	0.318	0.795	0.318
90 degree	1.125	0.768	1.921	0.45	0.329	0.225	0.562	0.131
45 degree	2.079	1.6	4	0.831	0.158	0.121	0.304	0.063
22.5 degree	4.079	3.231	8.079	1.631	0.078	0.062	0.155	0.031
11.25 degree	8.118	6.479	16.198	3.247	0.039	0.31	0.077	0.015
5.62 degree	16.217	12.966	32.416	6.487	0.019	0.015	0.039	0.007
2.81 degree	32.431	25.941	64.853	12.972	0.009	0.007	0.019	0.003

3.4.1 Ideal Lumped Element Values of 7-bit Phase Shifter

The conventional method of designing passive phase shifter based on high-pass/low-pass filter chooses one arm with a high-pass filter and chooses the other arm with a low-pass filter. Positive phase shift is provided by the arm with high-pass filter. Negative phase shift is provided by the arm with low-pass filter. The difference between these two phase shifts gives the desired phase shift of one bit. For example, if a bit is designed to perform 90° phase shift, ideally the arm with high-pass filter shifts the phase by +45° and the arm with low-pass filter shifts the phase by −45°. The difference between these two arms gives the 90° phase shift.

The values of the ideal lumped elements can be calculated by using the (36). The desired frequency of the phase shifter is 10 GHz. The ideal lumped element values for designing 7-bit conventional X-band high-pass/low-pass filter based phase shifter is shown in Table 2.

As shown in the Table 2, 4.079 nH inductance is required in order to obtain 22.5-degree phase shift. In practice, this value of inductance cannot be obtained at X-band because of the self-resonance of the inductance. Even if it is achieved, the size of the inductance will be huge. Because of the same reasons, 11.25 degrees, 5.62 degrees, and 2.81 degrees phase shifts cannot be obtained using this configuration.

For low phase shift degrees, same type of filters are used. For example, two different low-pass filters should be used in order to obtain 2.81-degree phase shift between two arms.

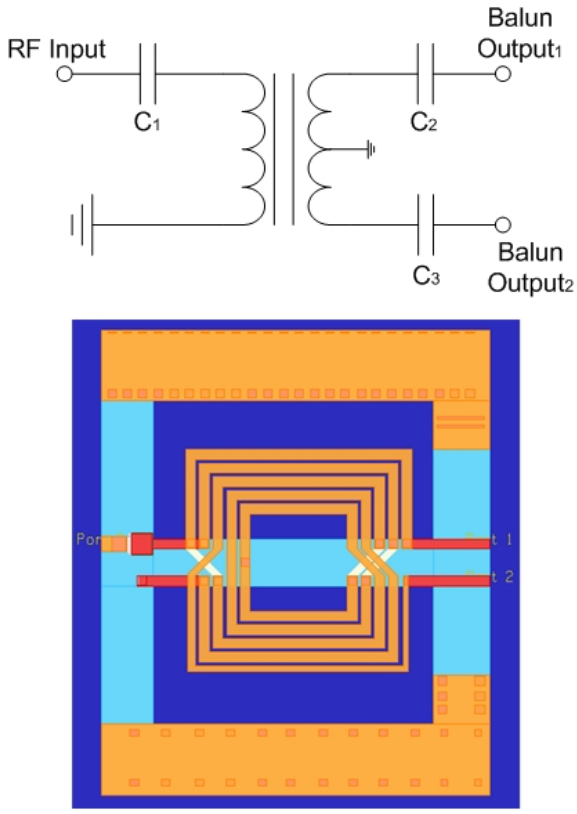

Figure 25: Schematic and Layout of the Transformer

3.4.2 BALUN Design

The first bit of the phase shifter will shift the signal either 180° or 0°. This part can be designed using high-pass/low-pass switched type phase shifter. However, the phase error of this bit is huge. In order to minimize the phase error of this bit, a transformer balun topology is selected for implementation.

Transformers convert signals from single ended to differential-end and two signals are generated in this way. Each of these signals has a 180° phase difference. In order to create two signals differentially, one of the windings at the electrical center or center tap is grounded. Schematic and layout of the transformer are depicted in Fig. 25.

While providing the 180°, transformers instead of high-pass/low-pass based filters, provide the phase difference in wide-band. This wide-band phase shift operation prevents the performance degradation of the phase shifter which can be caused by a 180° bit. However, due to the transformer, the insertion-loss of the 180° bit increases.

The transformer balun is designed using ADS Momentum. Since the signal is

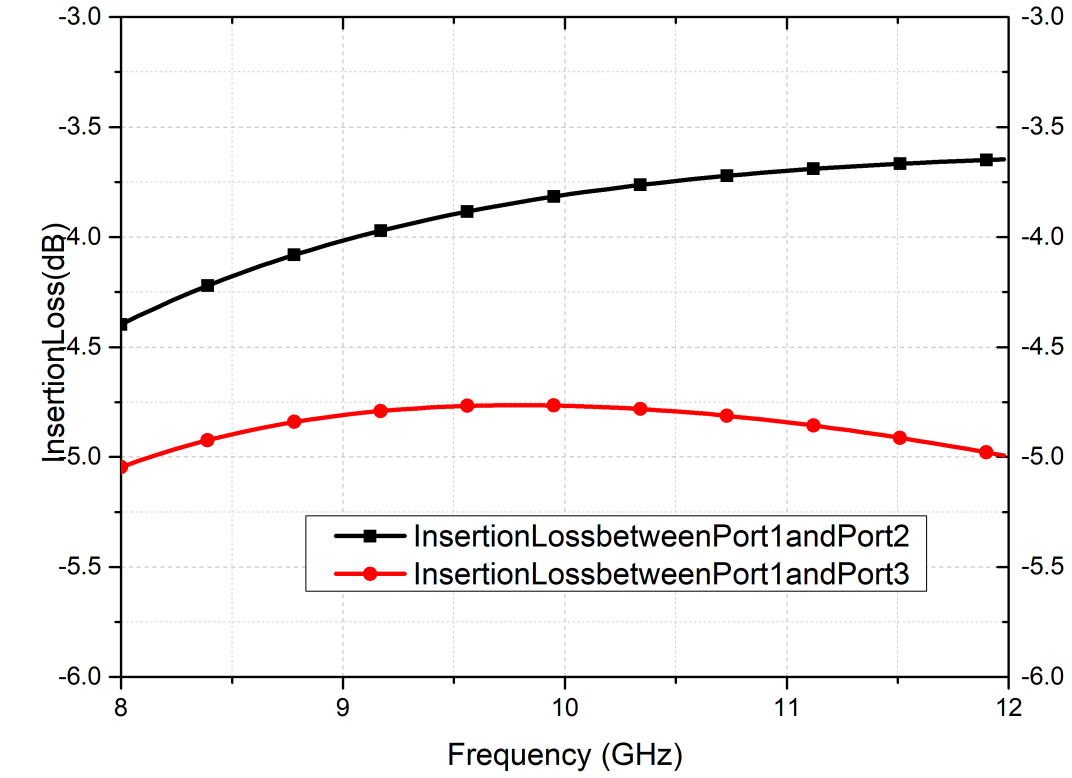

Figure 26: Simulation result of the insertion-loss between each output and input

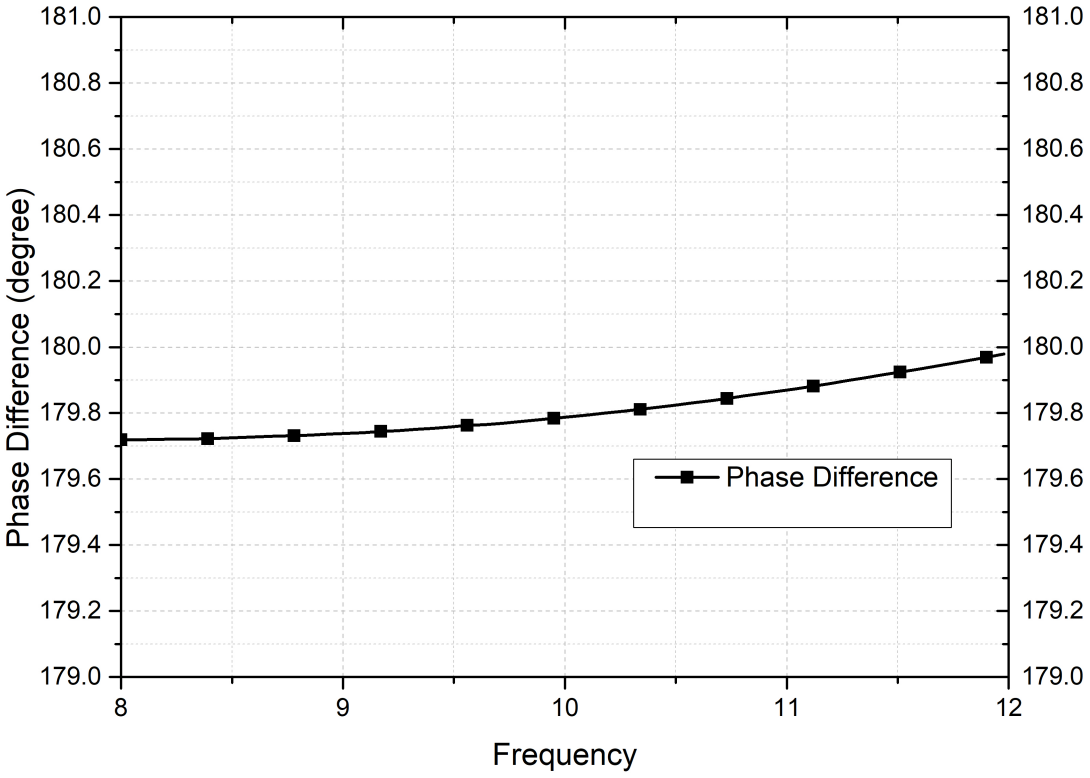

Figure 27: Simulation result of the phase difference between each output of the transformer

divided into two signals, the insertion-loss of an ideal transformer is 3 dB. Fig. 26 shows that the insertion-loss of the balun is <5dB. We can say that this transformer adds extra 2dB insertion-loss to the system. The amplitude error of the balun is <1.3 dB. Fig. 27 shows that the phase difference between the outputs is <0.3°.

3.4.3 Phase Values of Each Arm and Ideal Component Values

As shown in Table 2, the ideal component values of conventional type high-pass/low-pass based passive phase shifter cannot be realized. In order to achieve the phase difference as shown in Fig.24, same type of filters is chosen for each bit.

Inductance is used for matching each switch to 50 ohm, which will be explained in the next section. It means that the output of the switch ends with the inductance. If the filter type chosen begins with inductance, the area of the phase shifter reduces. Consequently, low-pass tee network is chosen for the first and the second bits.

In the first bit, 22.5°, 25.31°, 28.12°, 30.93° are chosen as a desired phase shift of the low-pass tee network for supplying 2.81° phase difference between each arm. In the second bit, 15°, 26.25°, 37.5°, 48.75° are chosen as a desired phase shift of the low-pass tee network for supplying 11.25° phase difference between each arm.

The phase difference between each network increases from 11.25° to 45°. Therefore, the same network cannot be used to obtain this phase difference. High-pass pi and low-pass pi networks are used to obtain the desired phase difference. The first arm of the third bit employs 33.75° phase shift with a high-pass pi network. Other arms employ the phase difference with low-pass pi networks. The desired phase values of networks of the second, third and fourth arms are 11.25°, 56.25°, and 101.25° respectively.

These values are optimized after combining all bits together to get low RMS phase values. Table 3 shows the comparison of the degree values after combining all bits. Ideal component values are calculated using the (36).

3.4.4 SP4T Design

The insertion-loss of the SP4T and the phase difference between each throws and pole are the main design considerations of the SP4T. Therefore, the design is optimized for minimum insertion-loss and phase difference between each throws and

Table 3: Phase values of designed phase shifter

Bit Number	Arm Number	Network Type	Ideal Phase Value	Optimized Phase Value
1	1	Low-pass tee	22.5	22.5
	2		25.31	25.65
	3		28.12	28.85
	4		30.93	31.7
2	1		15	15
	2		26.25	23.85
	3		37.5	33.2
	4		48.75	43.55
3	1	High-pass pi	33.75	33.75
	2	Low-pass pi	11.25	9.7
	3		56.25	57.65
	4		101.25	101.65

pole.

Designed phase shifter has four arms. The output of the phase shifter is connected to four arms over SP4T. The schematic of the SP4T is depicted in Fig. 28. R is selected as 10 kΩ. L_1, L_2, L_3, L_4, L_5, L_6, L_7, and L_8 are selected as 450 pH. Control voltages represented as $V_{c_{1-8}}$ have the connection from the digital control part of the phase shifter. When the width of the transistors increases, the insertion-loss of the switch decreases. The insertion-loss of the SP4T increases after some point due to the oxide capacitance of the transistor. The optimum point is chosen for the best insertion-loss.

SP4T is based on series-shunt switch topology. When the first voltage is high, M_1 , M_6, M_7, and M_8 operate in deep triode region while M_2 , M_3, M_4, and M_5 operate in cut-off region. This voltage connects the first arm to the output. When the second voltage is high, M_2 , M_5, M_7, and M_8 operate in deep triode region while M_1 , M_3, M_4, and M_6 operate in cut-off region. This voltage connects the second arm to the output. When the third voltage is high, M_3 , M_5, M_6, and M_8 operate in deep triode region while M_1 , M_2, M_4, and M_7 operate in cut-off region. This voltage connects the third arm to the output. When the fourth voltage is high, M_4 , M_5, M_6, and M_7 operate in deep triode region while M_1 , M_2, M_3, and M_8 operate in cut-off region. This voltage connects the fourth arm to the output.

Since the phase error of each bit plays an important role at the performance of

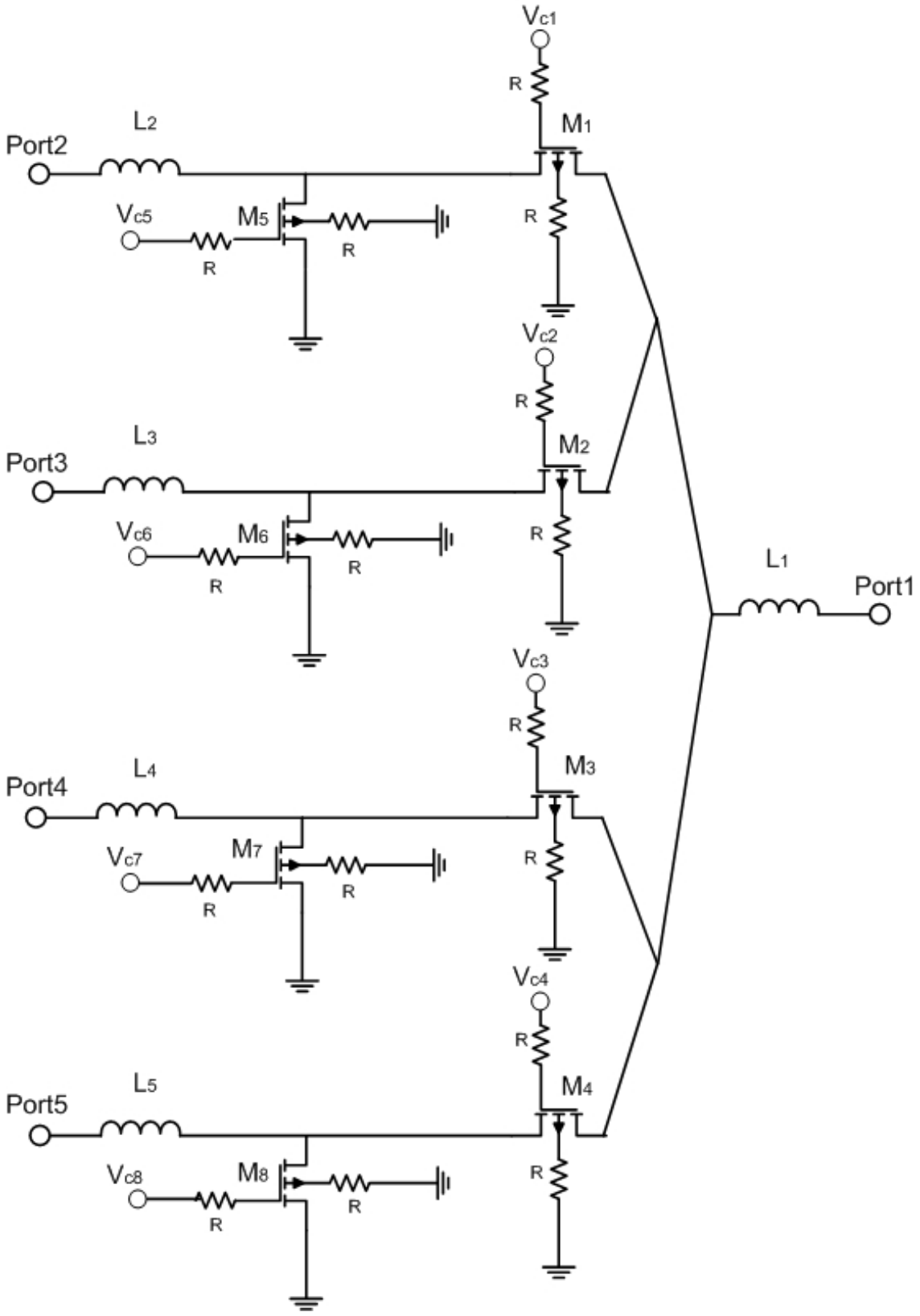

Figure 28: Schematic of the SP4T

the phase shifter, the phase difference between each arm to the output must be low. In order to decrease the phase difference from each arm to the output, the layout of

the SP4T is designed symmetrical.

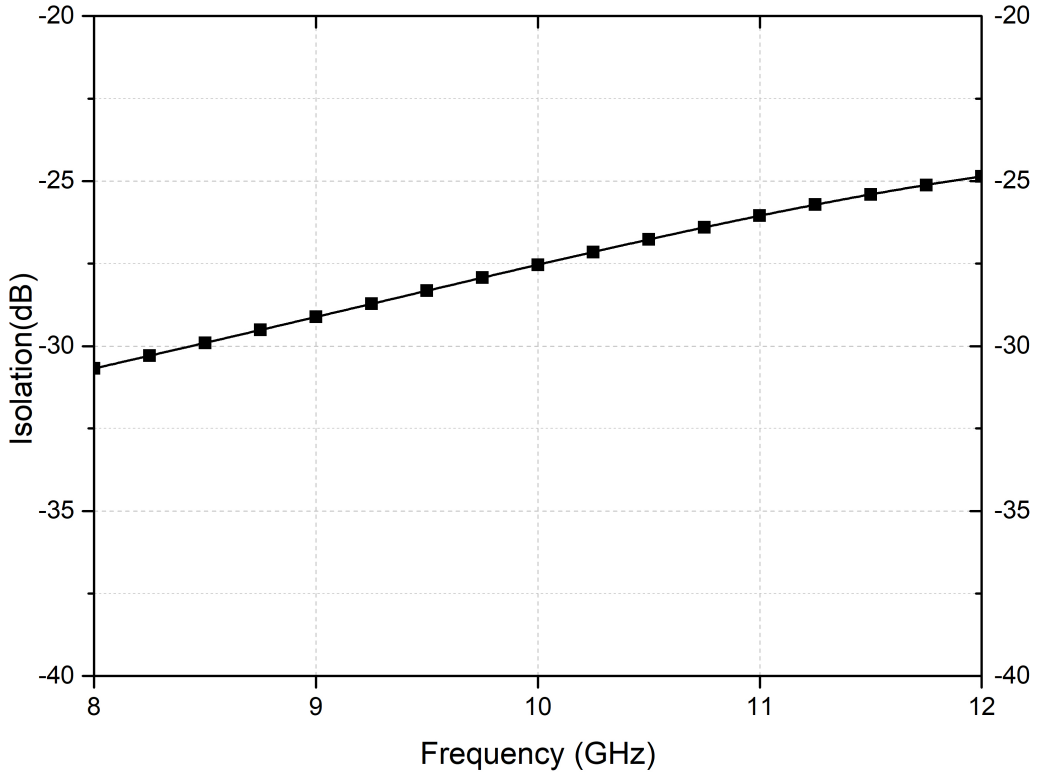

Figure 29: Simulation result of the isolation of the SP4T

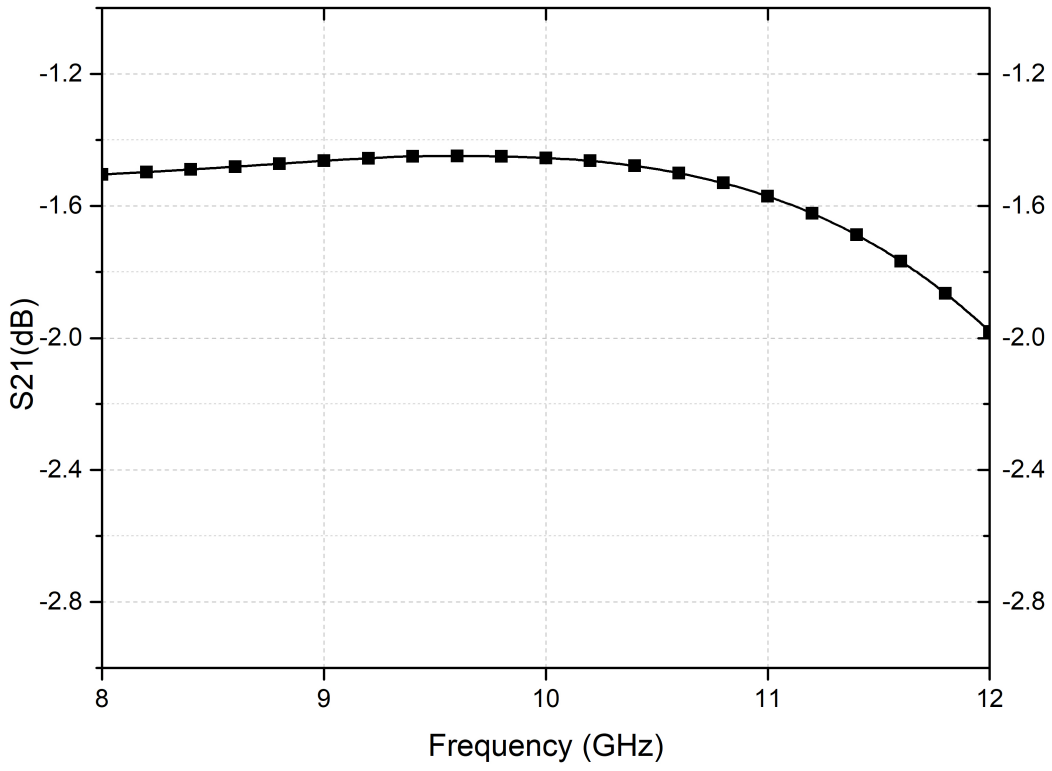

Figure 30: Simulation result of the insertion-loss of the SP4T

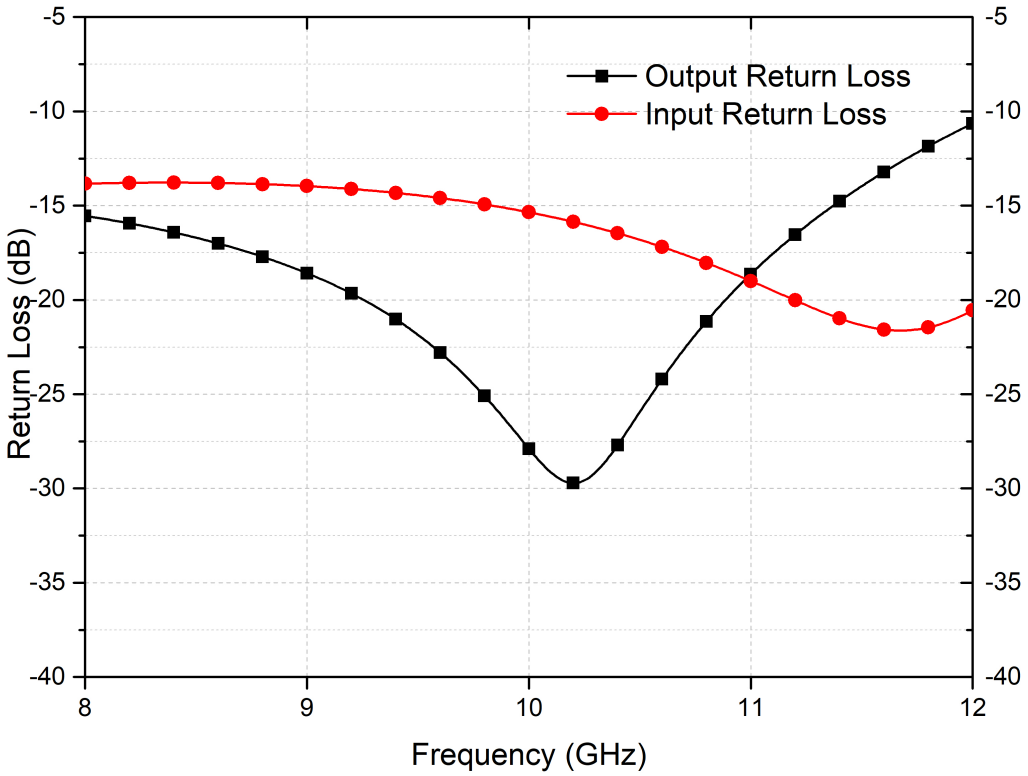

Figure 31: Simulation result of the return losses of the SP4T

As shown in Fig.30, SP4T achieves 1.5-2 dB insertion-loss. This value is the optimized insertion-loss value for the SP4T. Since the minimum insertion-loss is aimed for the phase shifter, design has sufficient performance for phase shifter.

The isolation between each port is 25-30 dB as shown in Fig.29. The isolation between each arm should be as high as possible to not interfere to the other arms. This isolation value is enough for handling the interference problem between each arm.

Fig. 31 depicts that return loss of each port is below from -10 dB which,will not cause an overall matching problem. Moreover, return loss of each port can be improved at using different inductance values for each arm. However, this will cause an additional phase error to the system. Therefore, best return loss value with the same inductance value is achieved in that design.

3.4.5 DP4T Design

The insertion-loss of the DP4T and the phase difference between each throws and each poles are the main design considerations of the DP4T. Therefore, the design

is optimized for minimum insertion-loss and phase difference between each throws and each poles.

The first bit the designed phase shifter is the BALUN, which is creating 180-degree phase shift between two arms. These two arms are connected to four arms over the DP4T. The schematic of the DP4T is depicted in Fig. 32. R is selected as 10 kΩ. L_1, L_2, L_3, L_4, and L_5 are selected as 500 pH. Control voltages represented as $V_{c_{1-14}}$ have the connection from the digital control part of the phase shifter. When the width of the transistors increases, the insertion-loss of the switch decreases. The insertion-loss of the DP4T increases after some point due to the oxide capacitance of the transistor. The optimum point is chosen for the best insertion-loss.

DP4T is based on series-shunt switch topology. To summarize, first connection is explained in detail. When the first voltage is high, M_1, M_{10}, M_{11}, M_{12}, and M_{14} operate in deep triode region while M_2 , M_3, M_4, M_5, M_6, M_7, M_8, M_9, and M_{13} operate in cut-off region. This voltage connects the first arm of the BALUN to the first arm of the second phase shift block.

Since the phase error of each bit plays an important role at the performance of the phase shifter the layout of the DP4T is designed symmetrical.

As shown in Fig.34 DP4T achieves 1.8-2.1 dB insertion-loss. This design is optimized for the insertion-loss value of the DP4T. Therefore, best insertion-loss value is achieved in that design.

The isolation between port1 - port2, port1 - port4, and port2 - port 3 are below 24 dB shown in Fig.33. All these isolation value is sufficient for handle the interference problem between each arms.

Fig. 35 depicts that return loss of each port is below from -10 dB. The return losses of this block can be improved. However, in order to match the circuit better, different inductance values are needed. This will cause phase difference between arms. Therefore, best matching with the same component value is achieved in that design.

3.4.6 4P4T Design

The insertion-loss of the 4P4T and the phase difference between each throws and each poles are the main design considerations of the 4P4T. Therefore, the design is

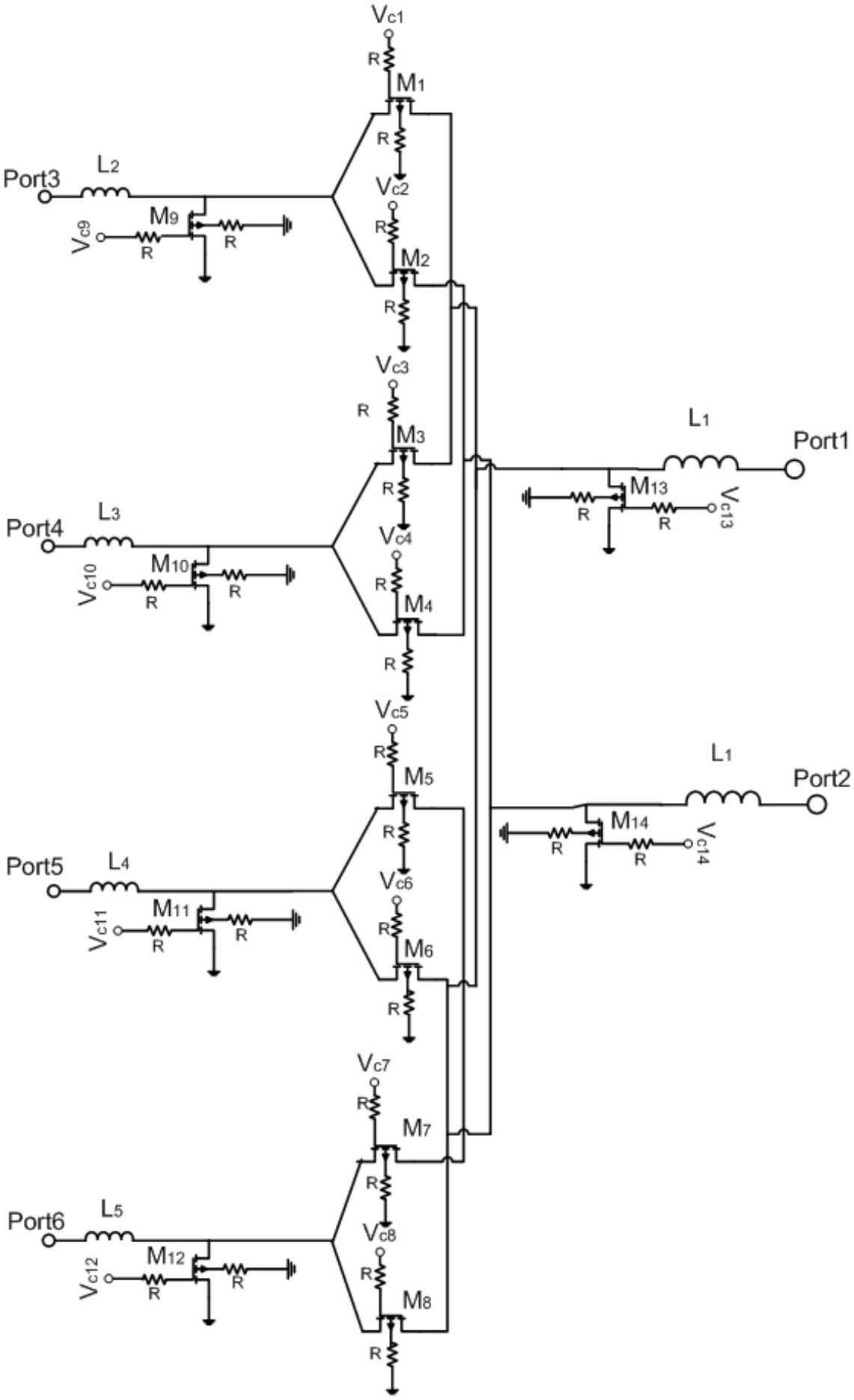

Figure 32: Schematic of the DP4T

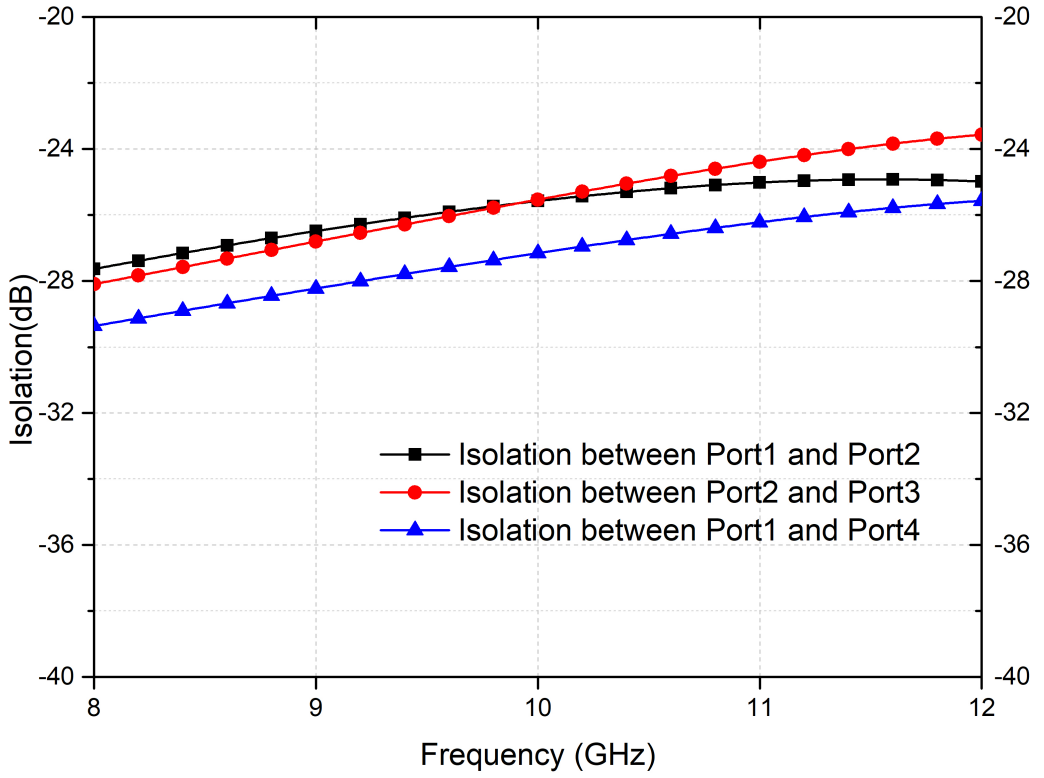

Figure 33: Simulation result of the isolation of the DP4T

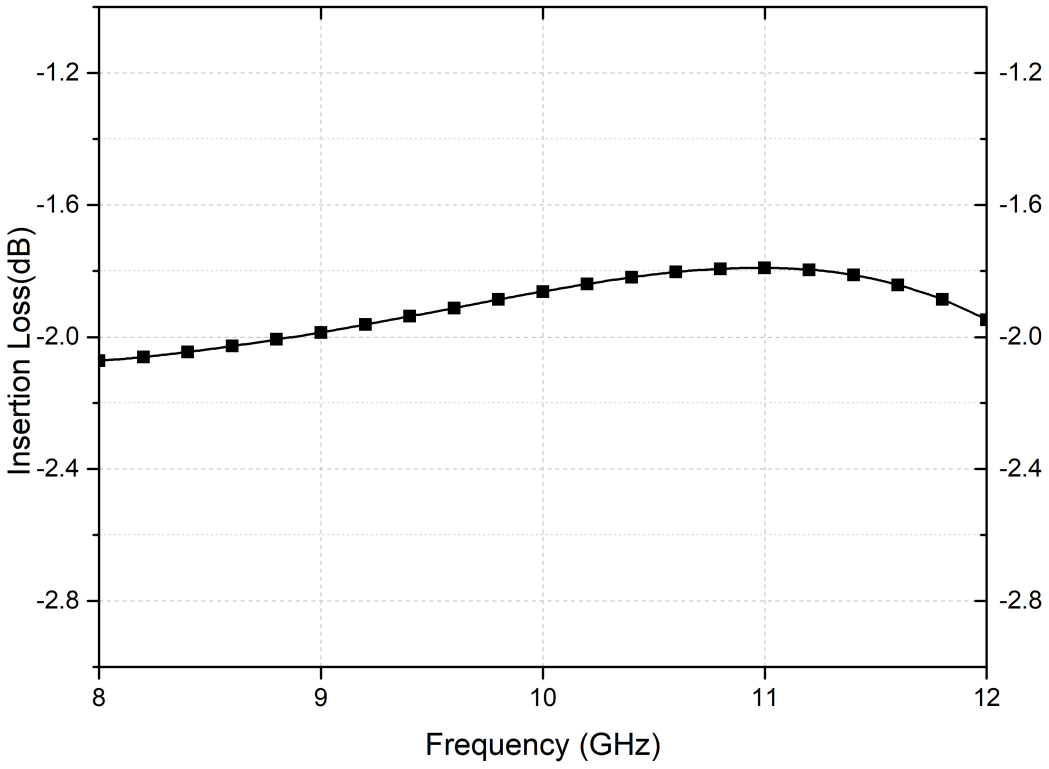

Figure 34: Simulation result of the insertion-loss of the DP4T

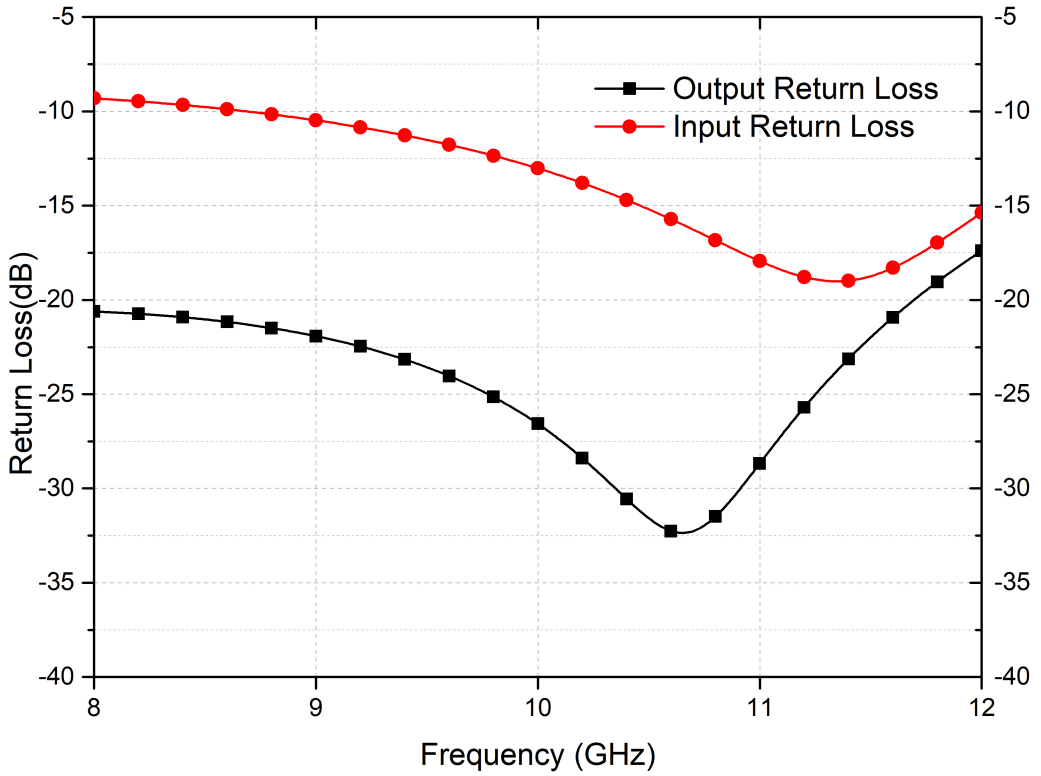

Figure 35: Simulation result of the return losses of the DP4T

optimized for minimum insertion-loss and phase difference between each throws and each poles.

While connecting the second and third bit of the phase shifter and the third and the fourth bit of the phase shifter, 4P4T is employed. The schematic of the 4P4T is depicted in Fig. 36. R is selected as 10 kΩ. L_1, L_2, L_3, L_4, L_5, L_6, L_7, and L_8 are selected as 425 pH. Control voltages represented as $V_{c_{1-24}}$ have the connection from the digital control part of the phase shifter. Four arms of each bit are connected to the four arms of the following bit individually. The optimum width of the transistor is chosen for the best insertion-loss performance.

4P4T is based on series-shunt switch topology. To summarize, first connection is explained in detail. When the first voltage is high, M_1 , M_{18}, M_{19}, M_{20}, M_{22}, M_{23}, and M_{24} operate in deep triode region while M_2 , M_3, M_4, M_5, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{18}, M_{19} , M_{20}, M_{22}, M_{23}, and M_{24} operate in cut-off region. This voltage connects the first arm of the second phase shift block to the first arm of the third phase shift block.

Since the phase error of each bit plays an important role at the performance of

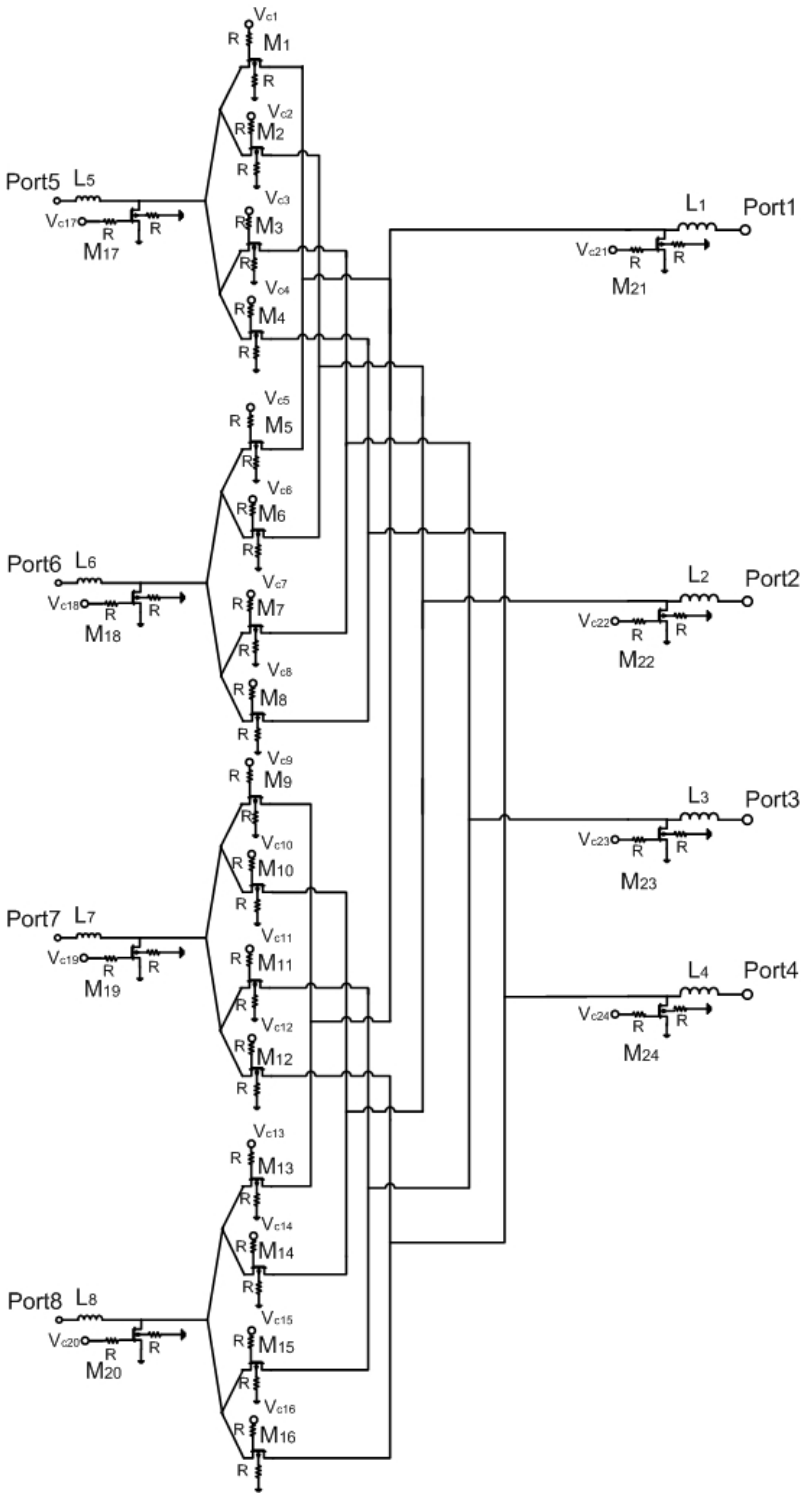

Figure 36: Schematic of the 4P4T

the phase shifter the layout of the 4P4T is designed symmetrical.

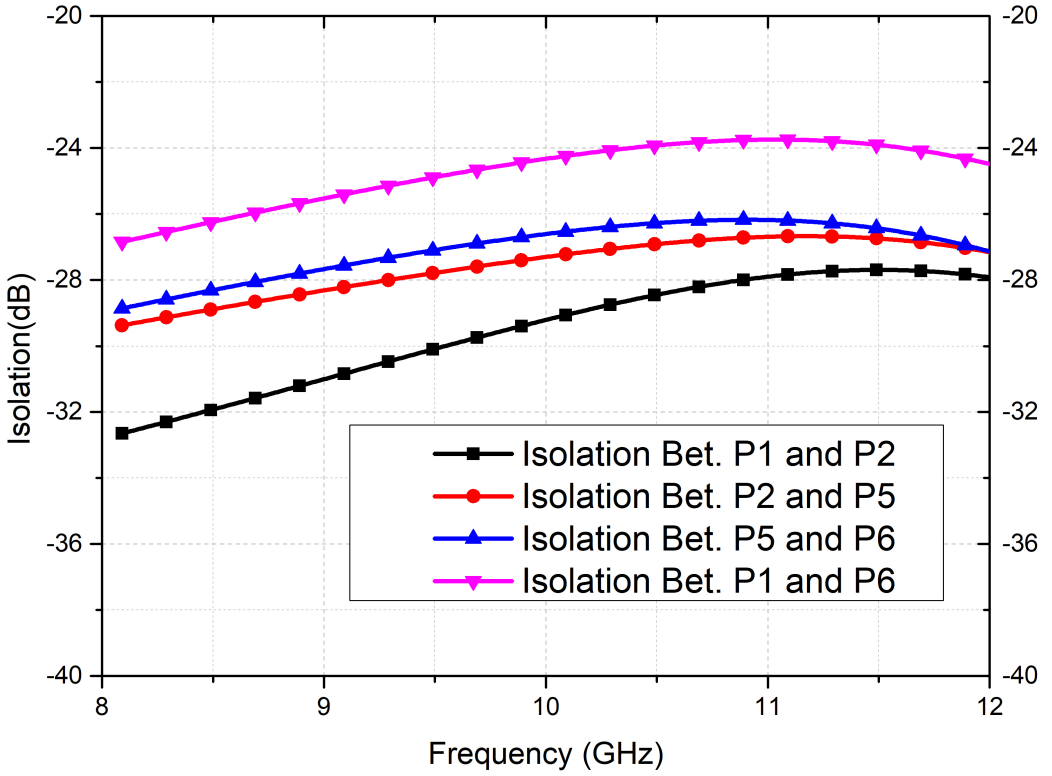

Figure 37: Simulation result of the isolation of the 4P4T

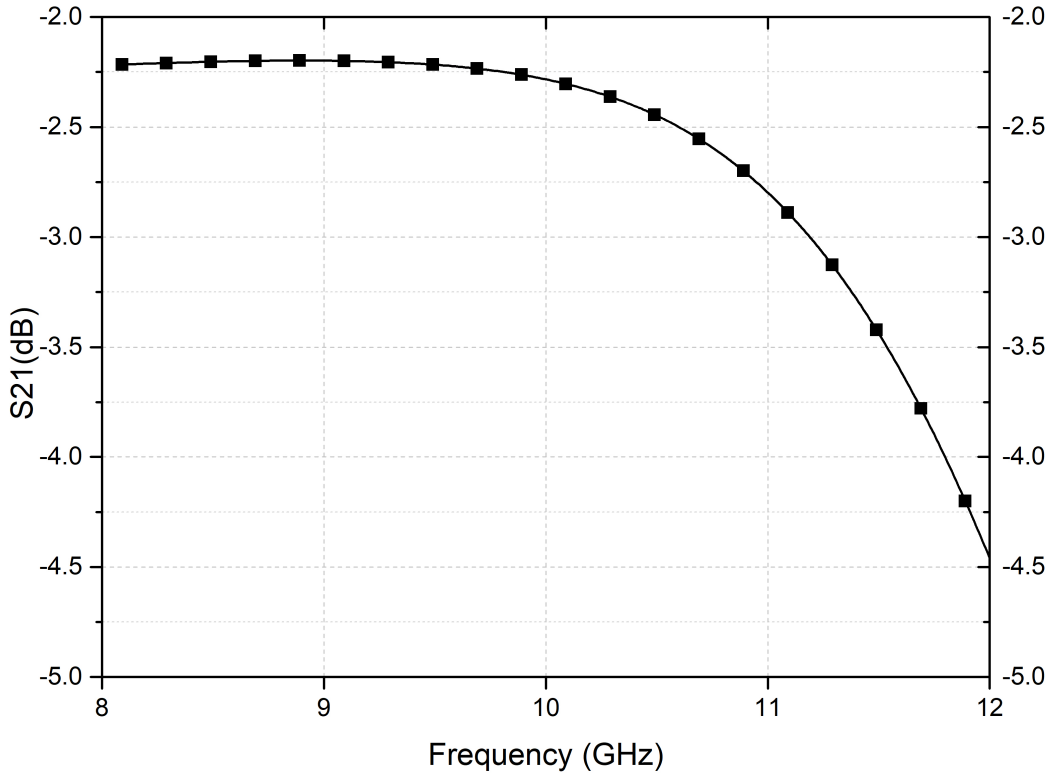

Figure 38: Simulation result of the insertion-loss of the 4P4T

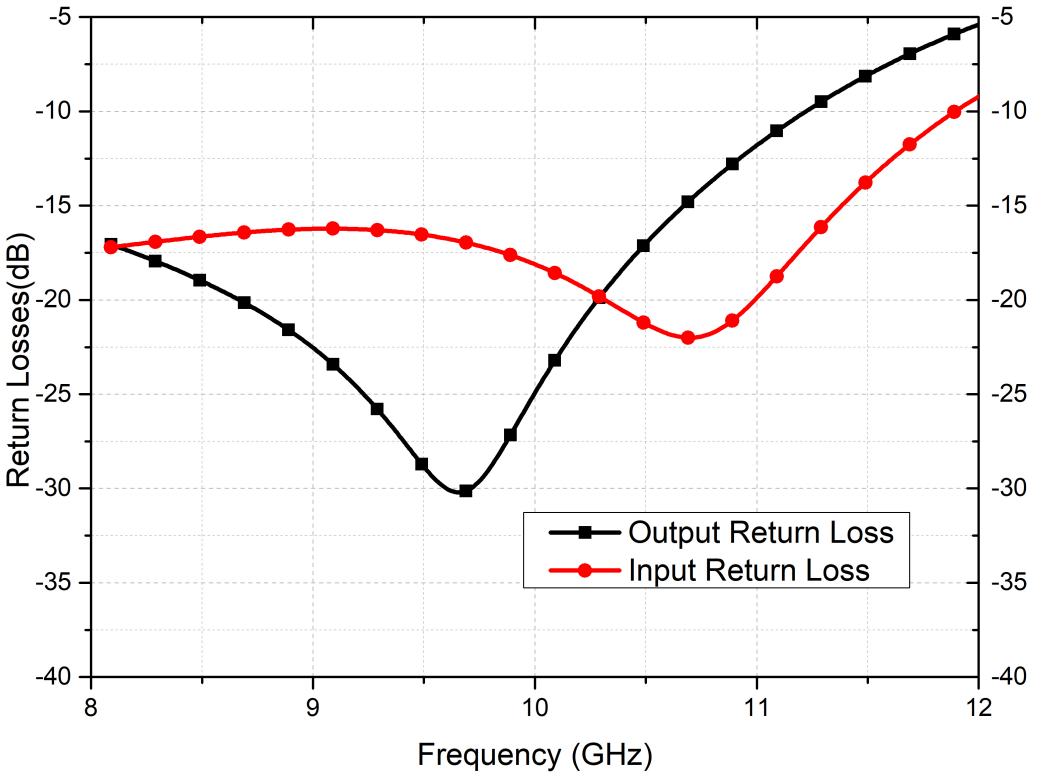

Figure 39: Simulation result of the return losses of the 4P4T

As shown in Fig.38 4P4T achieves 2.2-4.5 dB insertion-loss. The insertion-loss of the 4P4T increase dramatically after 11 GHz. This insertion-loss increases due to the bad matching of the 4P4T after 11 GHz. This can be improved in the future works. Between 8 GHz and 11 GHz 4P4T achieves 2.2-2.7 dB insertion-loss and this value still improve the insertion-loss of the phase shifter when we look at the overall performance of the phase shifter.

The isolation between port1 - port2, the isolation between port2 - port 5, the isolation between port 5 - port6, and the isolation between port1- port 6 are below -24 dB as shown in Fig.37. All these isolation value is sufficient for handle the interference problem between each arms.

Fig. 39 depicts that return loss of each port is below from -10 dB between 8 GHz and 11 GHz. The output return loss of 4P4T is worse than 10 dB between 11 GHz and 12 GHz. This matching problem causes an additional insertion-loss. This property needs to be improved in the next design.

3.5 Simulation Results of the Phase Shifter

The designed X-band phase shifter is designed using a high performance 0.25μm SiGe BiCMOS process (SG25H3) offered by IHP Microelectronics. Total die area is 4.9 x 1.2 mm^2. The EM simulation of the whole chip is performed in Advanced Design System (ADS) EM tool. Pad-to-pad S-parameter simulation results are shown in following sections.

3.5.1 Return Loss

Return losses of the phase shifter play an important role when integrating this block in T/R Module. S_{11} and S_{22} simulation results are shown in Fig.40 and Fig.41, respectively. As we can see from figures, S_{11} of the phase shifter is better than -10 dB at X-band and S_{22} of the phase shifter is better than 10 dB at X-band. We can say that the input and output of the phase shifter match 50 Ω.

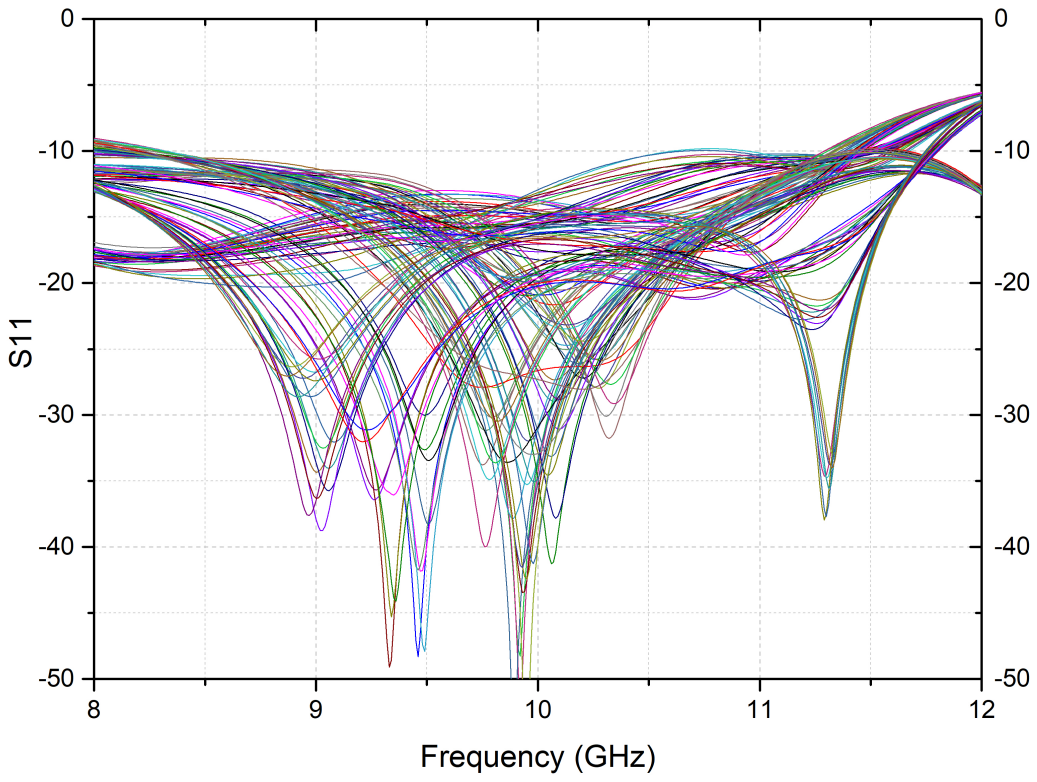

Figure 40: Simulation result of the input return losses of all states of the designed phase shifter

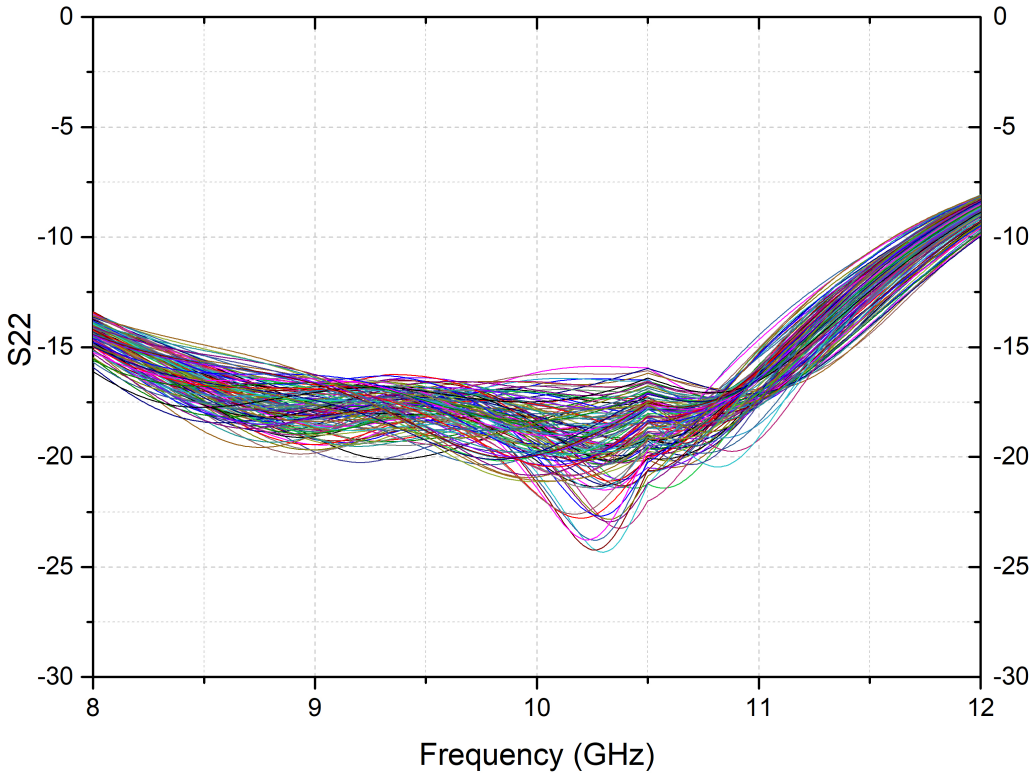

Figure 41: Simulation result of the output return losses of all states of the designed phase shifter

3.5.2 Insertion Loss

The most important improvement of the proposed phase shifter is the low insertion-loss. Fig. 42 shows the insertion-loss of the phase shifter. Due to the reduction of the number of the series switch, insertion-loss performance of the phase shifter is improved. The designed phase shifter achieves minimum 15 dB insertion-loss. Due to the poor performance of the 4P4T, the insertion-loss of the phase shifter increases between 11 GHz and 12 GHz. This will be improved in the next design.

3.5.3 Phase and Amplitude Performance

Phase and amplitude error of the BALUN is minimum at X-band. First and second sub-blocks show quite a good phase and amplitude performance. However, third sub-block which shifts the phase 45°, 90°, and 135° degrades the performance of the phase shifter.The phase shift operations of 45°, 90°, and 135° match well around 10 GHz. However, their phase shift values change too much with respect to frequency. This performance determines the performance of the phase shifter.

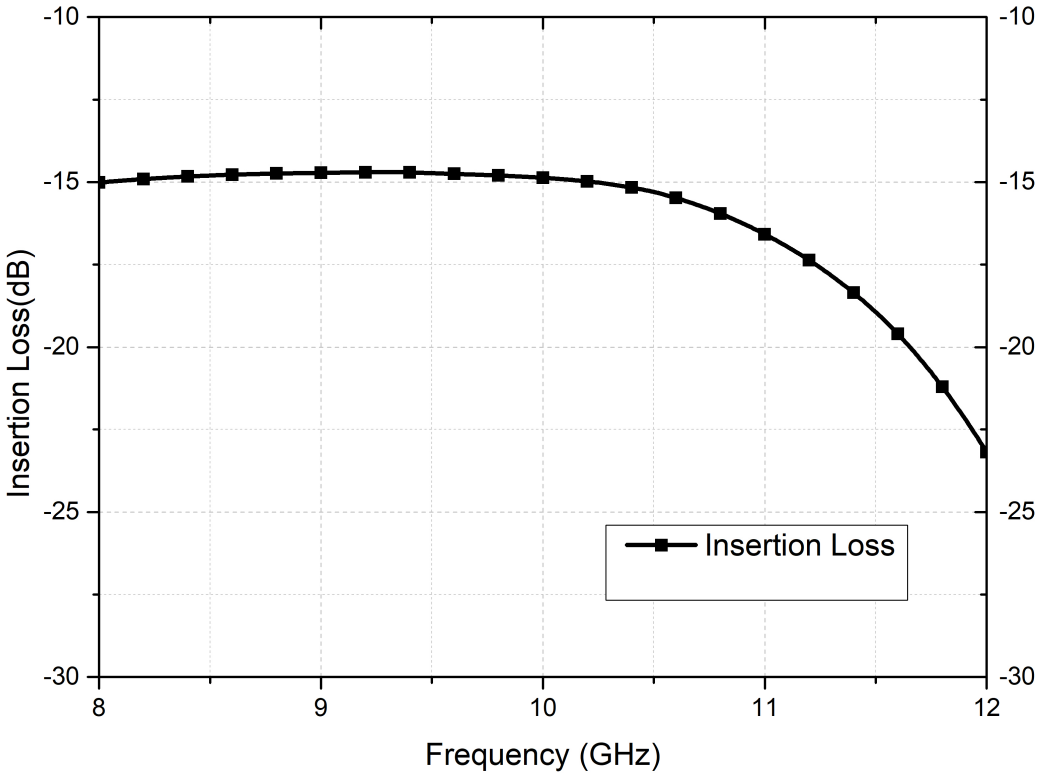

Figure 42: Simulation result of the insertion-loss of the designed phase shifter

Fig. 43 shows the amplitude response of phase states and Fig. 44 shows the RMS amplitude error of the overall 7-bit phase shifter. RMS amplitude error calculation is done by using (14). The lowest RMS amplitude error is achieved at 8.6 GHz with 0.25 dB.

Fig. 45 shows the each phase step of the phase shifter. As we can see from (36), inductance and capacitance values are depended on sine and cosine as function of phase shift value, respectively. Sine and cosine functions change more in value near 45 degrees. Therefore, these changes lead high phase errors. In the third sub-block of the phase shifter, 33.75 degrees and 56.25 degrees are used. These degrees lead overlaps and missing states in the phase shifter.

Finally, Fig 46 shows the RMS phase error of the overall 7-bit phase shifter. RMS phase error calculation is done using (13). Lowest RMS phase error is achieved at 10 GHz with 1°. RMS phase error of the phase shifter is lower than 2.8° between 9.5 GHz and 10.5 GHz.

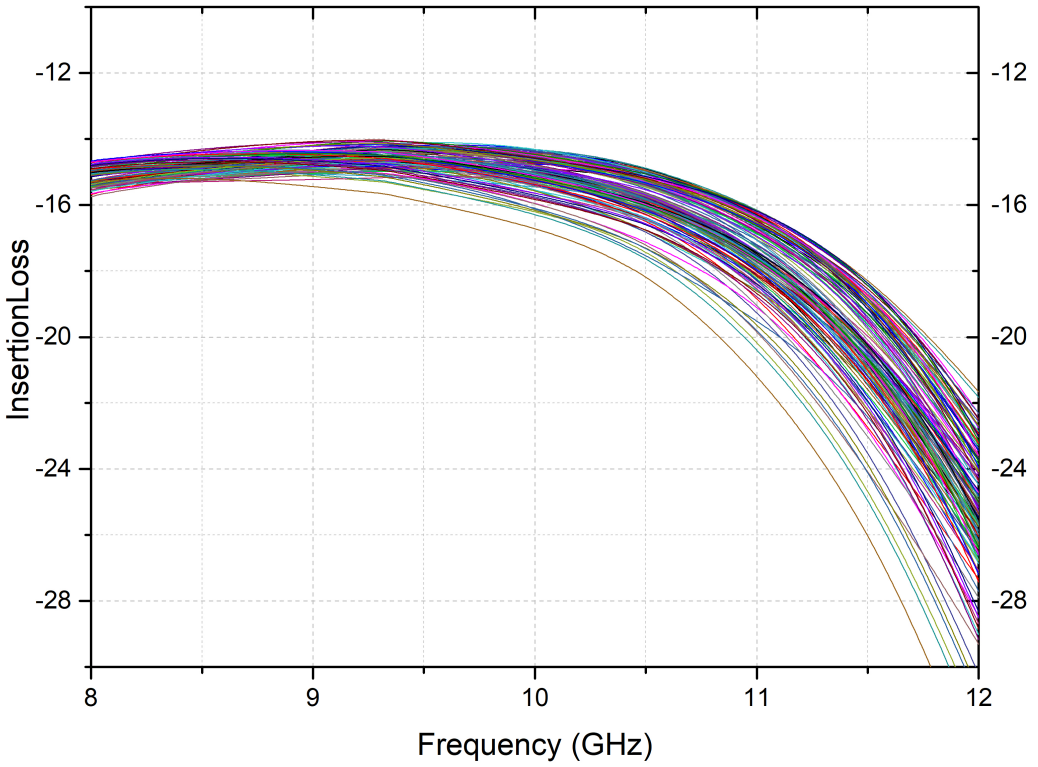

Figure 43: Simulation result of the amplitude response of each state of the designed phase shifter

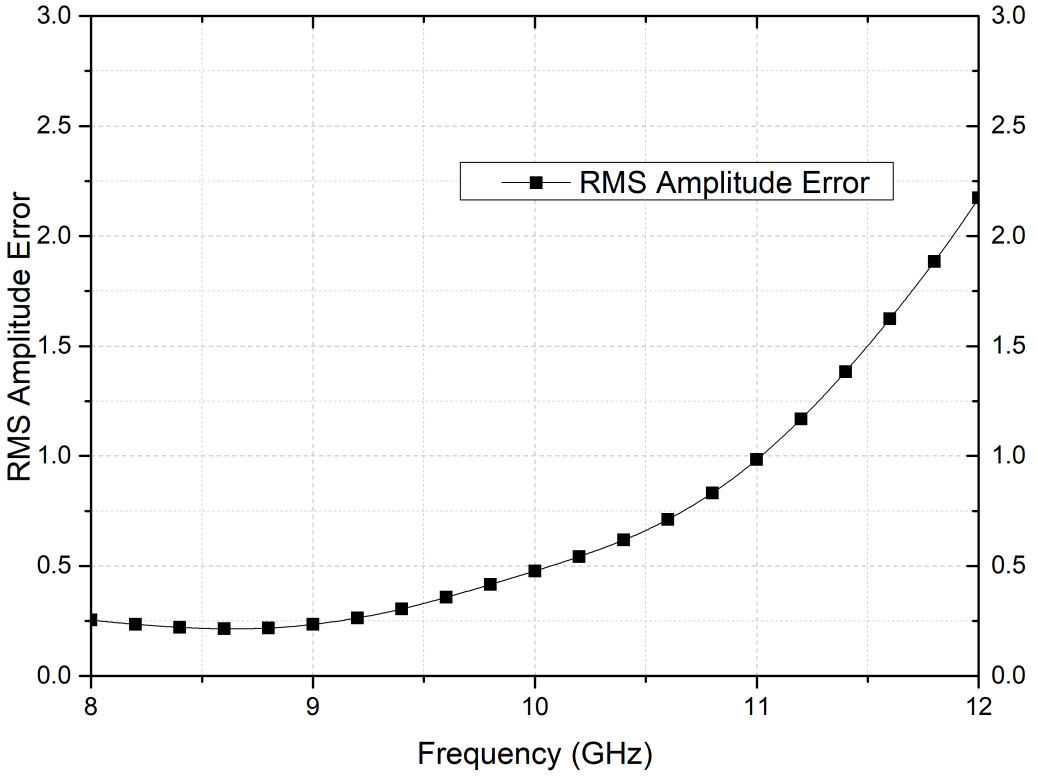

Figure 44: Simulation result of the RMS amplitude error of the designed phase shifter

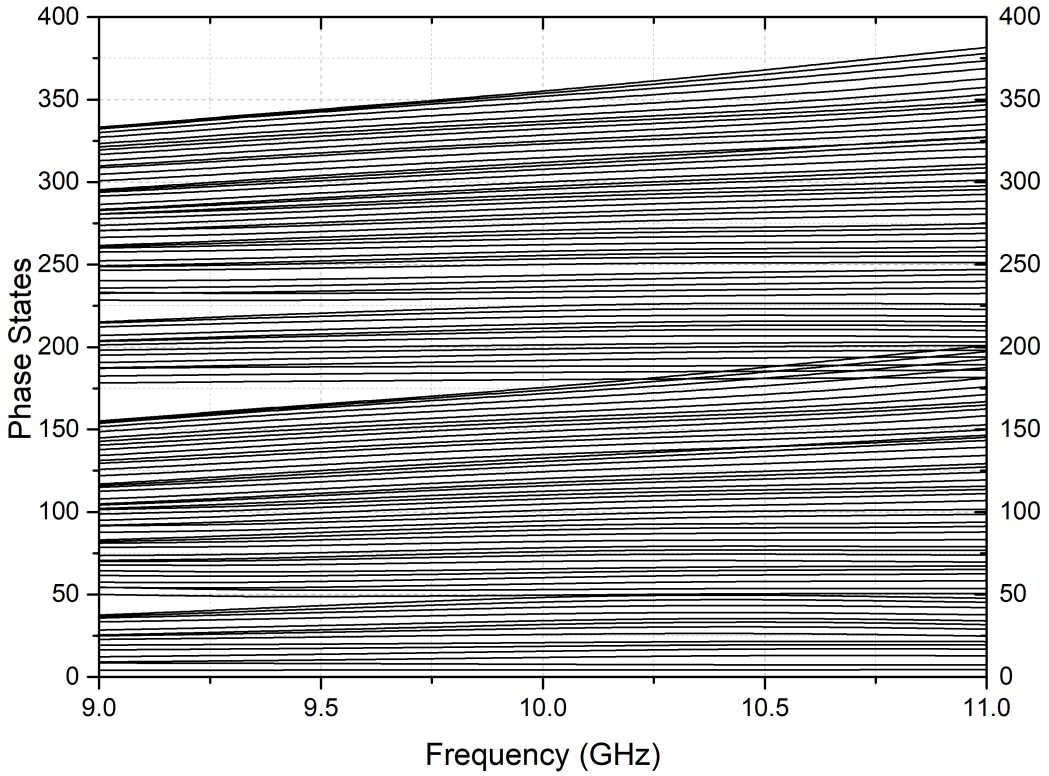

Figure 45: Simulation result of the phase states of the designed phase shifter

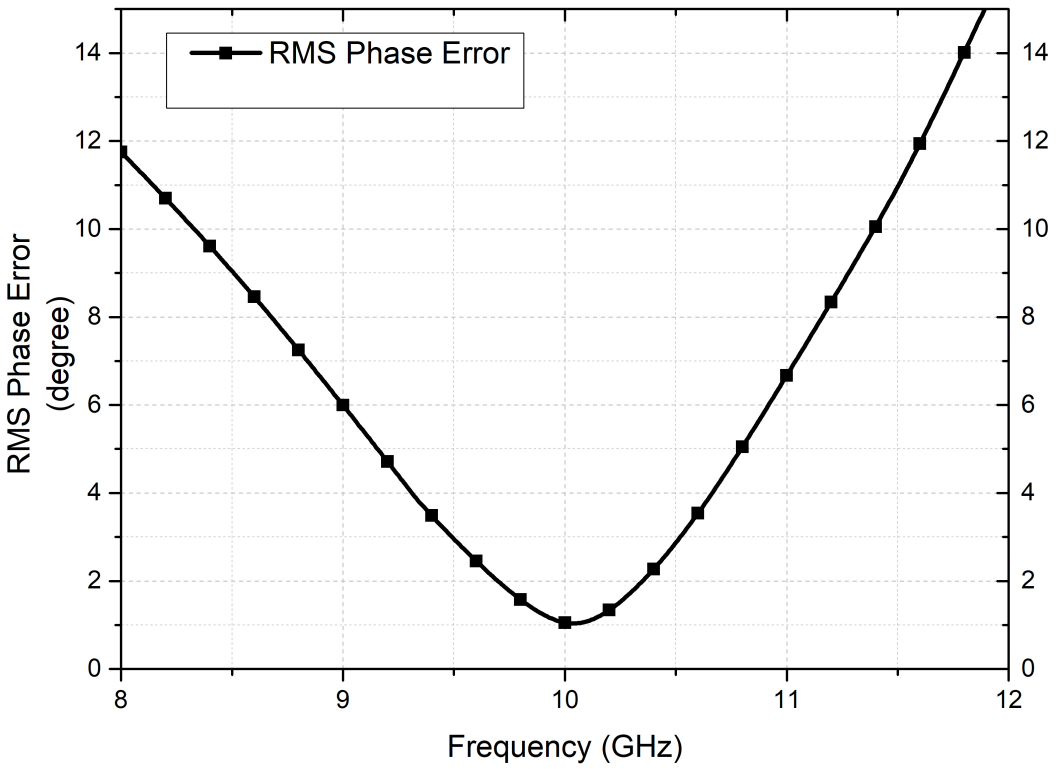

Figure 46: Simulation result of the RMS phase error of the designed phase shifter

3.6 Comparison

Table 4 shows the comparison between the proposed low insertion-loss 7-bit SiGe X-band phase shifter and the similar works in the literature. The proposed work achieves a significant reduction in the insertion-loss ,as proposed, with respect to other high-pass/low-pass topologies while achieving the highest bit resolution. Due to the passive configuration, the designed phase shifter achieves low bandwidth with respect to active phase shifters. Also, due to the performance degradation caused by 4P4Ts and 3_{rd} bit of the phase shifter, the bandwidth of the phase shifter becomes narrower. Active phase shifters achieve low-RMS phase error than this phase shifter. However, they consume power.

In the next phase shifter work, the bandwidth of the phase shifter will be improves by using 4P4Ts with a better performance in terms of insertion-loss and return-loss. Moreover, wide passive filter types will be replaced to increase the bandwidth of the phase shifter.

Table 4: Comparison of 7-bit SiGe X-band phase shifters with reported works

Frequency (GHz)	Num. of bit	RMS Phase Error (deg)	Gain (dB)	RMS Gain Error (dB)	Power Diss. (mW)	Chip Size (mm^2)	Topology	Process	Ref.
9 – 11	7	1-6	<-15.5	<0.7	0	6	Switched Type	0.25-μm SiGe (CMOS)	This work
8–12	5	<6.5	-11	<0.5	0	0.9	Switched Type	0.18-μm SiGe (SOI)	[31]
8 – 12	5	<9.1	<-20	N/A	<1	4.8	Switched Type	0.13-μm SiGe (HBT)	[32]
6 – 18	5	<5.6	<19.5	<1.1	61	0.9	Vector Sum	0.18-μm SiGe (HBT)	[33]
8 – 12	6	<6.4	<-2.5	<2	110	1.65	Vector Sum	0.25-μm SiGe (HBT)	[36]
9.2-10.8	4	3-11	<-10	2	0	0.9	Switched Type	0.25-μm SiGe(HBT)	[37]

4 Performance Summary of Other Building Blocks of T/R Module including Passive and Active Gain-Equalizers

4.1 Introduction

Throughout my master education, I was also a part of team which builds sub-blocks to design a complete T/R module. In this chapter, the design and specifications of T/R module designed by our group will be presented. Then, this section will emphasize the design and implementation of an X-Band SiGe passive gain-equalizers designed by myself with the collaboration of Eşref Türkmen and active gain-equalizers designed by myself with the collaboration of Can Çalışkan, two members of our group. These equalizers are part of the fully integrated single-chip 6-bit phase and 6-bit amplitude controllable T/R module providing 3-dB positive slope gain. Generally, T/R modules are integrated with III-V low-noise amplifiers or power amplifiers to increase the sensibility and output power of the whole system. The gain of these amplifiers decreases with the increase in frequency. In other words, these amplifiers have negative slope with respect to the frequency. When the T/R module is integrated with these amplifiers, the negative slope of the overall gain increases. In order to compensate this negative slope, between T/R module chip and III-V amplifiers, discrete gain equalizers are utilized. Due to the discrete off-chip solution, the area of overall chip will be huge.

In order to handle this gain and area problems due to integration problem, the gain behaviour of the T/R module should have the positive gain slope with respect to frequency. However, amplifiers, switches, phase shifters, and attenuators inside T/R module have negative gain-slope due to the same reason aforementioned for III-V amplifiers. In order to have positive gain-slope, passive or active equalizers needs to be integrated with the blocks which have negative gain behaviour.

Active and passive gain-equalizers are realized in SiGe BiCMOS process technology in order to integrate these blocks with T/R module. The utilized process is IHP 0.25 μm SiGe BiCMOS technology. In this process, RF blocks are realized with three different transistor types which are high-performance for low noise level

values, high-voltage for high output power levels, and mid-voltage for the performances in the middle of noise and output power. Moreover, CMOS can be used in this process. Generally, CMOSs are used in RF switching and digital control part of the T/R module.

T/R module is the most important part of the phased arrays because it determines the performance of the phased arrays by controlling the phase and amplitude. The designed T/R module consists of a 6-bit active phase shifter, a 6-bit attenuator, a switched LNA, two passive gain-equalizers, two high linearly-gain SPDT switches, middle power amplifiers, driver amplifier, and two active gain-equalizers. System level circuit diagram of the designed amplifier is shown in Fig. 47. The explanations of each block are presented in the following section.

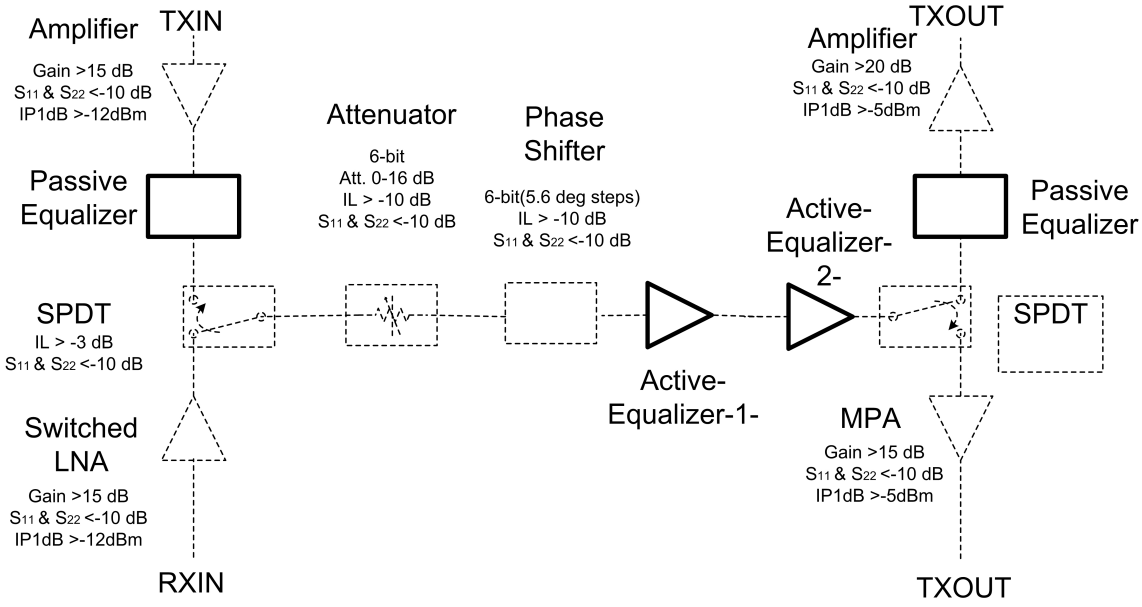

Figure 47: SiGe X-band all-RF T/R module block diagram and component specifications

4.2 System and Previously Designed Sub-Blocks

In the proposed T/R module, system configuration shown in Fig.47 is selected for reducing the cost and compactness. By selecting this configuration, the same phase shifter and attenuator are utilized for transmitter and receiver path. This configuration enables to use the omnidirectional phase shifter. Therefore, power cost is reduced using this configuration. The isolation between the transmitter and receiver is also high with this configuration. Amplifiers are used for obtaining the

3-dB gain slope and counteracting the insertion loss of the switches, passive gain-equalizers, phase shifter and attenuator.

The aim of T/R module is to achieve phase and amplitude control with a 3-dB positive overall gain slope. 3-dB positive gain slope can be obtained by designing sub-blocks based on the insertion-loss of phase shifter and attenuator. The main purpose of phase shifter and attenuator is not a gain behaviour. They need to achieve desired amplitude or phase control on T/R module. Therefore, firstly, phase shifter and attenuator are designed. Then, the sub-blocks are used to meet the gain behaviour requirement.

4.2.1 A 6-bit Active Phase Shifter

In the designed T/R module, an active 6-bit vector sum type phase shifter is used for obtaining the phase control of T/R module [36]. The designed phase shifter based on vector-sum topology. In order to obtain 90-degree phase shift between I± and Q± networks, passive balun and RCPPF based quadrature generator is utilized. These reference quadrature vectors are amplified by 6-bit digitally controlled VGAs. The output of the VGAs is summed up and given as an output.

4.2.2 A 6-bit Attenuator

In the proposed T/R module, an attenuator is used for obtaining the 6-bit amplitude control of T/R module [38]. The fully passive attenuator is achieved with pi and tee type of networks. In these networks, the attenuation steps are achieved by either bypassing the state or attenuating the state. In order to obtain the lowest insertion loss, the width of each transistor is chosen carefully. 16-dB attenuation is covered with 0.25 dB amplitude step.

4.2.3 CMOS SPDT Switches

In the proposed T/R module, linearly gain slope CMOS based SPDT switches, designed by Eşref Türkmen, my colleague in RF-IC laboratory, are used. The realized SPDT uses series-shunt based topology. When the first control voltage is high, the first input is connected to the output. The second input is grounded to increase the isolation between input ports. When the second control voltage is high,

the second input is connected to the output and the first input is grounded. The insertion loss of SPDT is inversely proportional to the width of the series transistors. When the width of transistor increases, the insertion loss of the SPDT is improved. However, this improvement does not continue linearly. Consequently, the best width of the transistor is chosen.

4.2.4 Switched LNA

In the proposed T/R module, switched LNA is designed by Eşref Türkmen. Switchable LNA is used to obtain the signal in the receiver path with low noise or switching the amplifier to get the signal with high power without concerning about linearity. Cascode configuration is used in the LNA. In this configuration, emitter inductance is employed to increase the linearity and match the input of the circuit. Moreover, RF feed inductance also plays an important role in input matching. The switch part creates a feedback system between the input and output.

4.2.5 MPAs

In the proposed T/R module, two proposed middle-PAs, designed by Can, my colleague in RF-IC laboratory, are employed. Two different middle-PAs are used with the same schematic to obtain high output power at both transmitter and receiver part of the T/R module. Two stage cascode configuration is used in both amplifiers. The difference between these two blocks is that MPA which is used in transmitter path of the system has high output resistance value to obtain higher output power and higher gain. As a result of higher output resistance and higher gain, the output return loss of this amplifier is worse than the MPA used in receiver path.

4.2.6 Driver Amplifier

The proposed driver amplifier, designed by Eşref, is used to amplify the signal at the input part of the transmitter in T/R module. Single stage cascode configuration is used in this block. Emitter inductance is employed to increase the linearity performance of the driver amplifier.

4.2.7 Equalizer Requirements

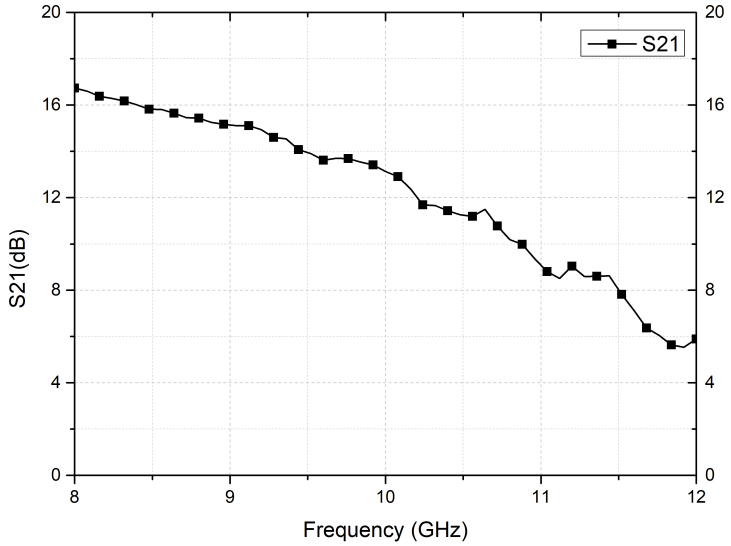

Figure 48: Overall S21 result of the designed T/R module blocks for RX chain

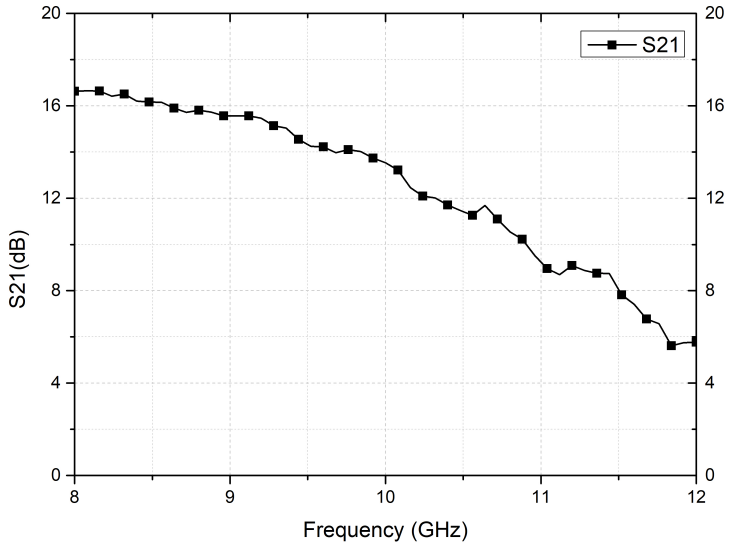

Figure 49: Overall S21 result of the designed T/R module blocks for TX chain

As shown in Fig. 48 and Fig. 49, these designed blocks create approximately 11-dB negative gain slope with respect to the frequency. In order to have 3-dB positive gain behaviour with respect to the frequency, positive sloped gain equalizers are needed. Passive gain equalizers can create less positive slope than the active gain equalizers. However, they do not suffer from the linearity and they do not consume power. Therefore, one passive gain equalizer for each chain and two active equalizers for common chain are employed to achieve 3-dB positive slope gain. Approximately,

without considering the decrease of the gain due to the mismatches, 14 -dB positive slope gain is aimed for these gain-equalizers. The explanations of these blocks, designed by myself, are presented in the following section.

4.3 Active and Passive Equalizers

As initial step to design an equalizer for the overall system, circuit topology of the equalizer must be selected by considering the specifications and trade-offs. There are two main configurations for equalizer design: Passive equalizers and Active equalizers. This categorization is done considering their power consumption.

Passive equalizers create a ramp with a positive slope without consuming power. These networks immune to the temperature variations because the whole network does not depend on the active networks. Moreover, they have high linearity. However, these networks cannot create ramps with a high slope in small frequency intervals. They have high insertion loss. Moreover, whenever a new sub-block is added the system, the gain behaviour changes a lot due to isolation.

Fig.50 shows the example schematics of the equalizer circuits. Equalizer in Fig.50a uses parallel connection of the capacitance and resistance. Equalizer in Fig.50b uses the series connection of the inductance and resistance in parallel with the input and the output port. Equalizer in Fig.50c connects a capacitance in the parallel with the resistance. Two frequency dependent component increase the controllability of the gain vs. frequency of the gain-equalizer. Equalizer in Fig.50d employs series RLC filter. Equlizer in Fig.50e is the conventional type passive gain-equalizer. Parallel $\lambda/4$ grounded transmission-line connections and series LC filter connection determines the peak gain point of the gain-equalizer. Resistance is used for the matching of the network. The gain vs. frequency slopes of these equalizers are shown in Fig. 51. In this figure C_1 is selected as 1pF, R_1 is selected as 50Ω, R_2 is selected as 25Ω, L_1 is selected as 1 nH, R_3 is selected as 25Ω, C_2 is selected as 1pF, L_2 is selected as 1nH, R_4 is selected as 25Ω, L_3 is selected as 1nH, C_3 is selected as 1pF, R_5 is selected as 50Ω, R_6 is selected as 85Ω, L_4 is selected as 2.25 nH, and C_4 is selected as 0.45 pF. From this figure, Fig.50e is selected as the schematic of the gain-equalizer in order to increase the controllability of the slope of the gain vs. frequency.

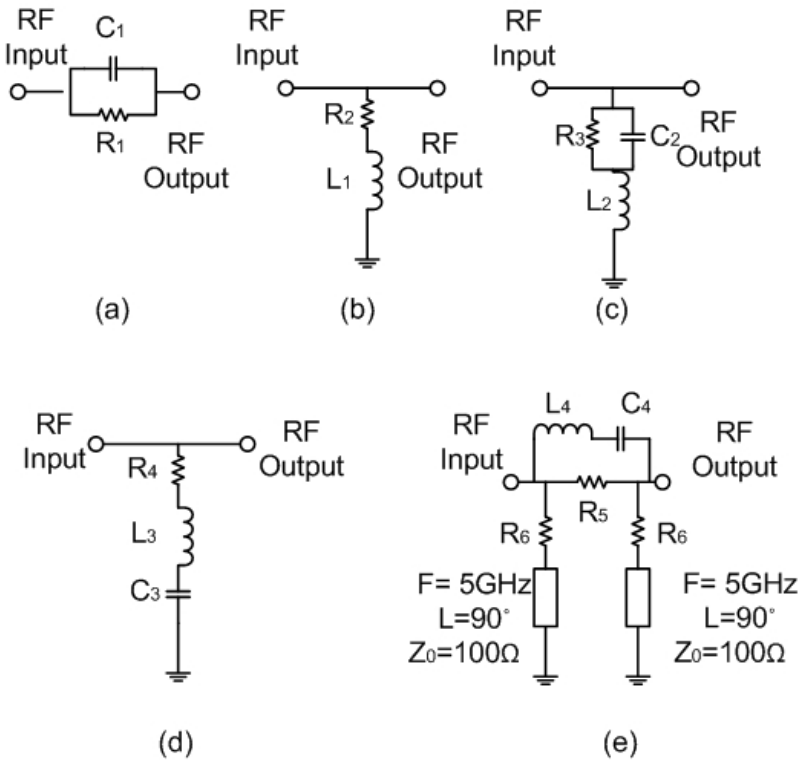

Figure 50: Examples of the schematic of passive gain-equalizers

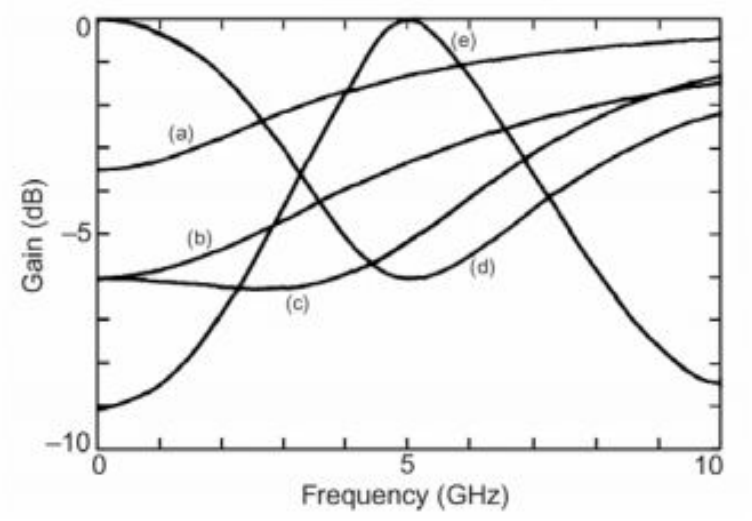

Figure 51: The gain vs. frequency for the five example gain-equalizers[7]

4.3.1 A Conventional Type Passive Gain-Equalizer

Fig.50e shows the conventional type of passive gain-equalizer. The slope of gain vs. frequency can be adjusted by changing the series connection between L and C of the gain-equalizer. Series resistance and $\lambda/4$ also adjust the slope of the gain vs. frequency but they are not the main determinant of the slope of the gain vs. frequency.

The aim of the first gain-equalizer is that provides a 3 dB gain vs. frequency slope. The minimum attenuation of the gain equalizer is aimed at 12.5 GHz. Therefore, the frequency of the $\lambda/4$ is aimed for 12.5 GHz. Different LC values are select for different slopes for the gain vs. frequency of the gain-equalizer.

Series resonance of the L-C part is calculated using formula 40. The series capacitance value is swept from 500fF to 200fF with 100 fF intervals. In the first ideal gain equalizer, the series capacitance is used as 500fF, consequently, the series inductance is used as 324 pH. In the second ideal gain equalizer, the series capacitance is used as 400fF, consequently, the series inductance is used as 405 pH. In the third ideal gain equalizer, the series capacitance is used as 300fF, consequently, the series inductance is used as 540 pH. In the fourth ideal gain equalizer, the series capacitance is used as 200fF, consequently, the series inductance is used as 811 pH. S21 graphs of ideal gain-equalizers are depicted in Fig. 52. The desired aim is 3dB. Therefore, 300fF is selected as the capacitance value of the series resonance and 540 pH is selected as the inductance value of series resonance. In order to match the network to 50Ω, series resistance is selected as 50Ω and parallel resistance is selected as 235Ω.

$$2\pi f = \frac{1}{\sqrt{LC}} \tag{40}$$

The schematic of the conventional type passive gain equalizer with component values is shown in Fig.53. This passive gain-equalizer is fabricated in IHP 0.25 μm SiGe BiCMOS technology. Fig. 54 depicts the micrograph of the conventional type of gain-equalizer.

Sonnet EM simulation tool is used as design environment. Since the whole block has passive components, detailed full-chip simulations are performed. Both

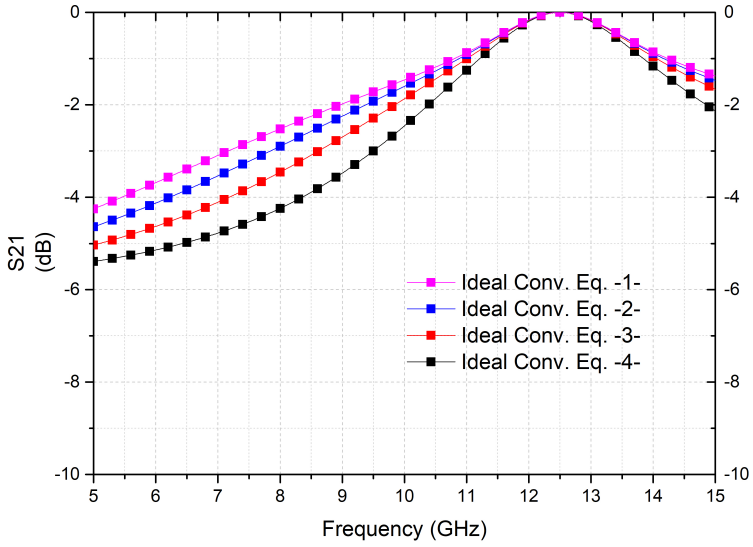

Figure 52: The gain vs. frequency for four example conventional gain-equalizers

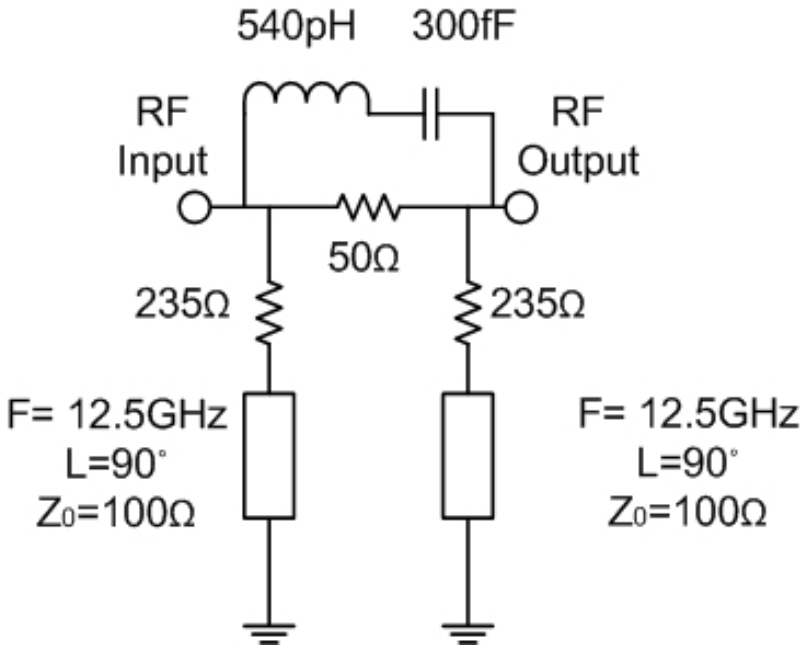

Figure 53: The schematic of designed conventional type gain-equalizer

simulation and measurement results of S_{11},S_{22}, and S_{21} are given in Fig.55.

4.3.2 A New Compact Passive Gain-Equalizer

Fig.56 shows a new compact passive gain-equalizer designed by myself in collaboration with Eşref Türkmen, my colleague in RF-IC group. In this design, the slope of gain vs. frequency can be adjusted by changing the series connection between L and C of the gain-equalizer. In this design, instead of using and $\lambda/4$, parallel LC resonance is employed. Series resonance and parallel resonance are employed at the

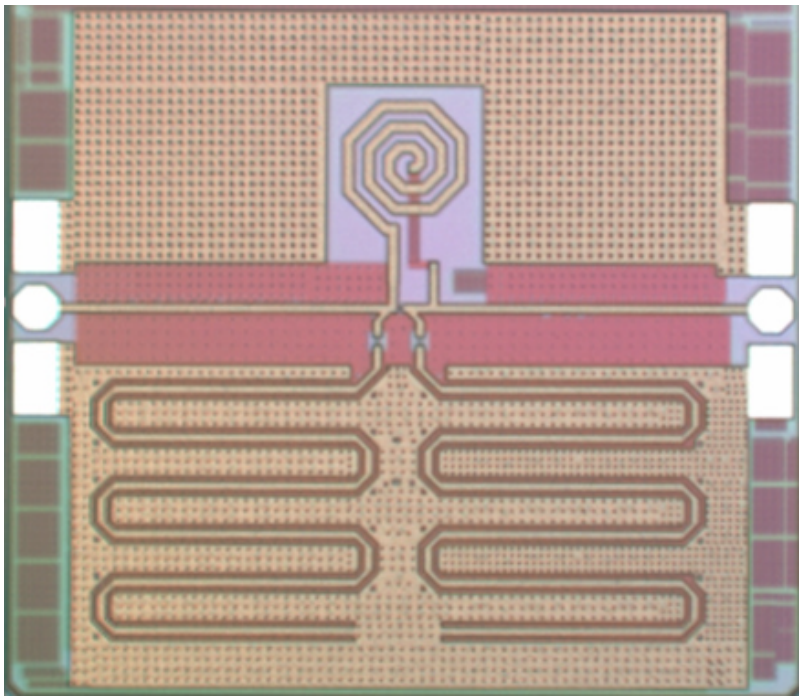

Figure 54: The micrograph of designed conventional type gain-equalizer

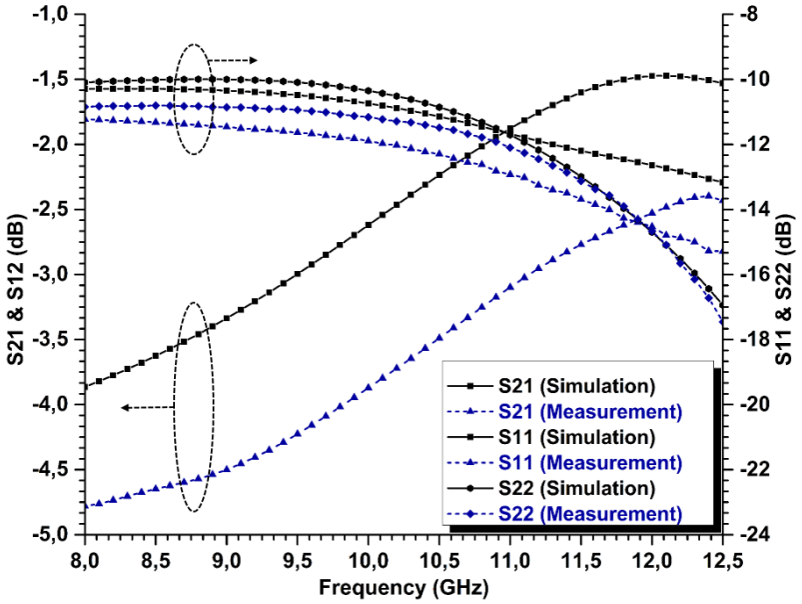

Figure 55: Simulation and measurement results of designed conventional type gain-equalizer

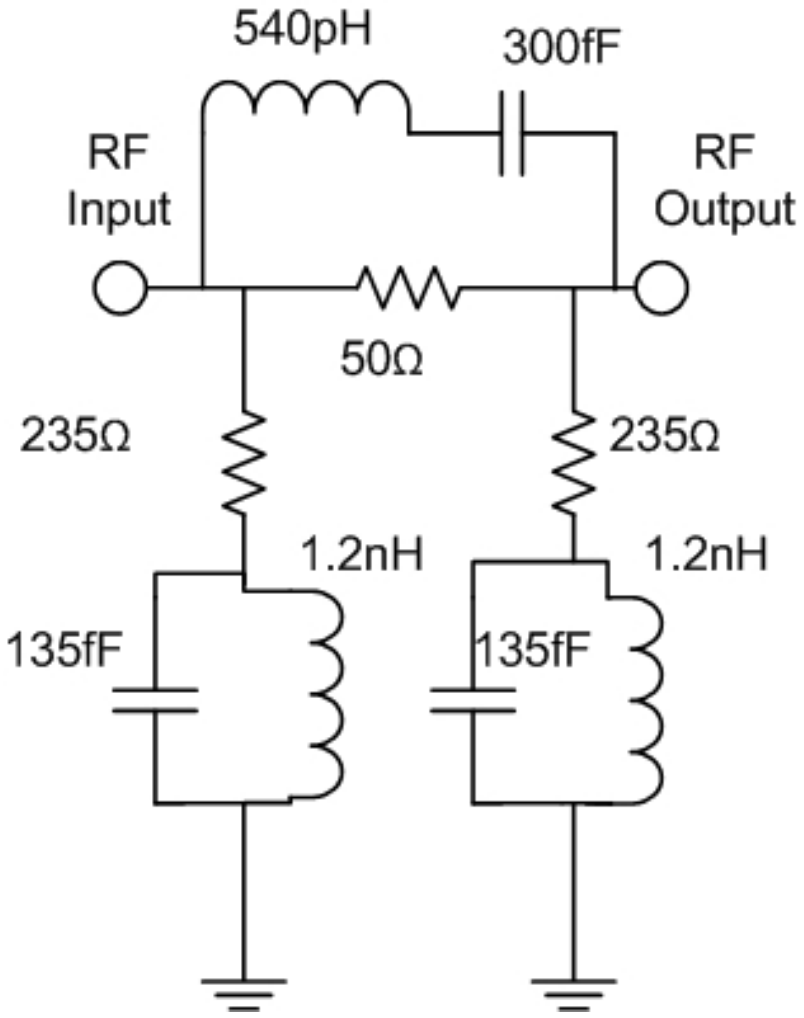

Figure 56: The schematic of designed a new compact type gain-equalizer

same frequency.

The aim of the new compact gain-equalizer is to provide a 3 dB gain vs. frequency slope. The minimum attenuation of the gain equalizer is aimed at 12.5 GHz. Therefore, the frequency of the series resonance and parallel resonance are aimed at 12.5 GHz. Series L and C values are determined in a conventional type gain equalizer. The value of the parallel resonance values is selected as 1.2nH and 135fF.

The new compact gain equalizer reduces the area of the block from 1.96 mm^2 to 0.33 mm^2. Due to the employing the parallel resonance instead of $\lambda/4$, the transmission line length is reduced at the input part of the network. Therefore, this new chip also reduces the insertion-loss. This passive gain-equalizer is fabricated in IHP 0.25 μm SiGe BiCMOS technology. Fig. 57 depicts the micrograph of the conventional type of phase shifter.

Sonnet EM simulation tool is used as design environment. Since the whole

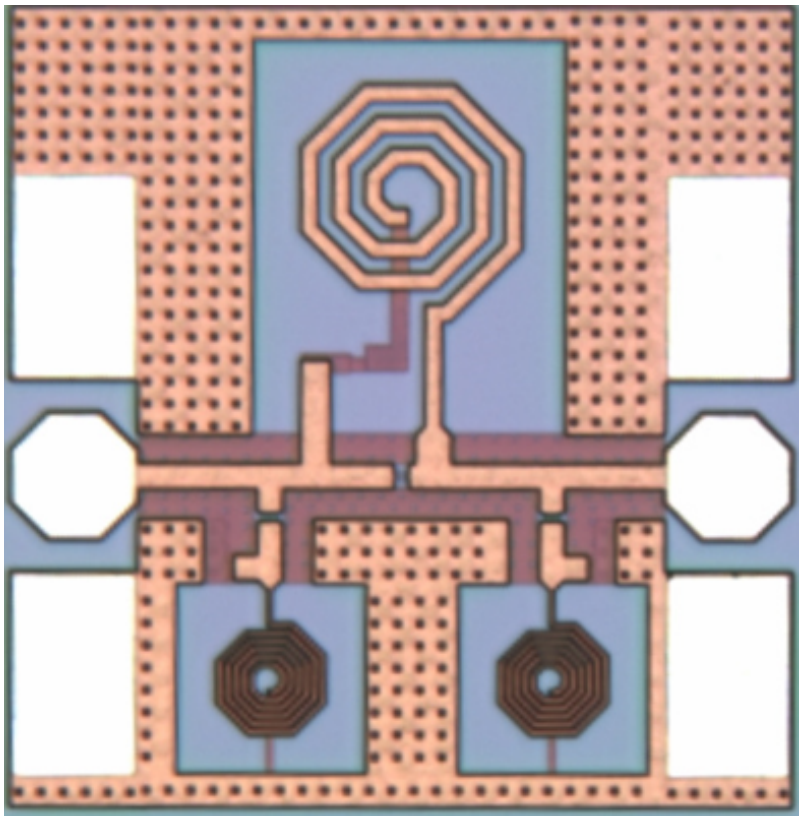

Figure 57: The micrograph of designed a new compact type gain-equalizer

block has passive components, detailed full-chip simulations are performed. Both simulation and measurement results of S_{11},S_{22}, and S_{21} are given in Fig.58.

As we can see from measurement results, this new compact gain-equalizer has less insertion-loss than the conventional type of gain-equalizer. Moreover, the compact gain equalizer occupies 1/6 ratio of the conventional type of equalizer. Due to these advantages, the new compact gain-equalizers are used in T/R Module to provide positive 3 dB slope for the whole block.

4.3.3 Passive Gain-Equalizers for T/R Module

In order to provide 3-dB positive slope gain in T/R module, passive and active gain-equalizers are used. The beginning point of obtaining this behaviour is the gain-behaviour of the phase shifter and attenuator. Since these blocks are designed regardless of their gain-behaviour, the aim of the gain-equalizers is that reform the gain-behaviour of these blocks. Moreover, MPAs are also designed regardless of their gain-behaviour because the main aim of these blocks provides high output power. All these blocks have gain behaviour in a negative slope. In order to flatten

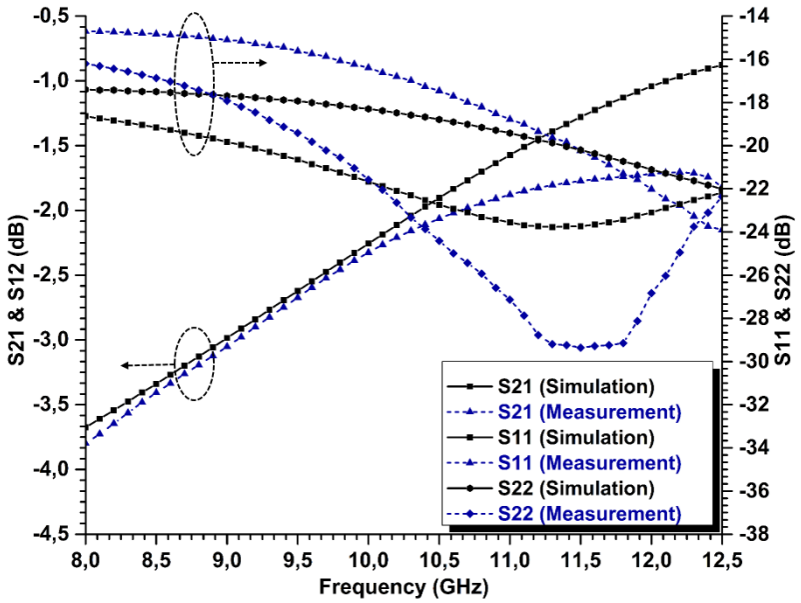

Figure 58: Simulation and measurement results of designed a new compact type gain-equalizer

the gain behaviour of the whole system, two passive gain-equalizers and two active equalizers are designed. Active gain-equalizers are used in common path, one passive gain-equalizer is used in RX chain and one passive gain-equalizer is used in TX chain.

A compact type passive gain-equalizers are used in T/R module. The difference between these two equalizers is the desired positive slope and the desired minimum attenuation frequency. The value of the capacitance and the inductance lead different positive slope in the passive gain-equalizer. These blocks are integrated with T/R module. Therefore, these blocks have a connection to another block before the gain-equalizer and after the gain-equalizer. These blocks are not matched 50Ω perfectly. This matching difference leads different matching criteria for this network. As a result, resistance values which are mainly used for matching the block to 50Ω are also different.

Fig.59 shows the S_{11} and S_{22} measurement result of the gain-equalizer which is used in RX chain. Insertion-loss graph of this gain-equalizer depicts in Fig.60.

Fig.61 shows the S_{11} and S_{22} measurement result of the gain-equalizer which is used in TX chain. Insertion-loss graph of this gain-equalizer depicts in Fig.62.

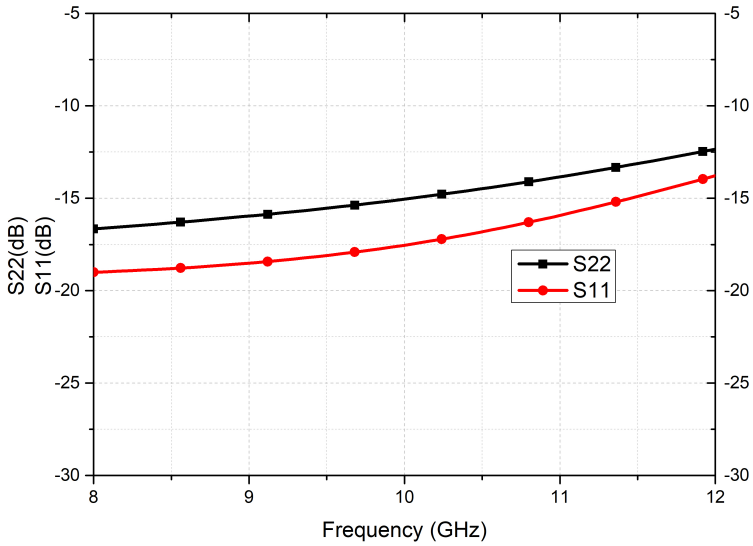

Figure 59: S11 and S22 measurement results of designed compact type gain-equalizer for RX chain

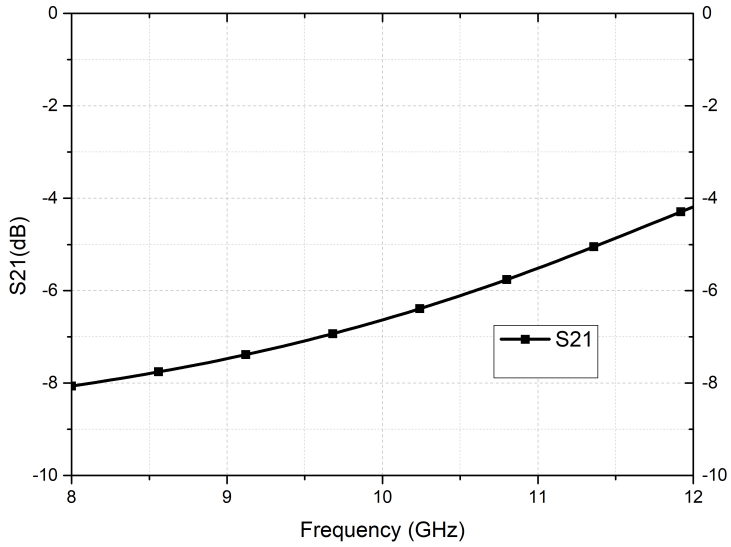

Figure 60: S21 measurement results of designed compact type gain-equalizer for RX chain

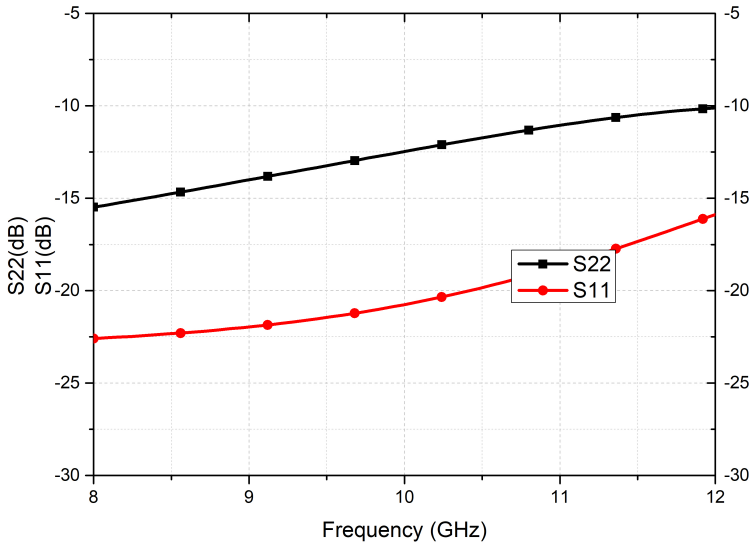

Figure 61: S11 and S22 measurement results of designed compact type gain-equalizer for TX chain

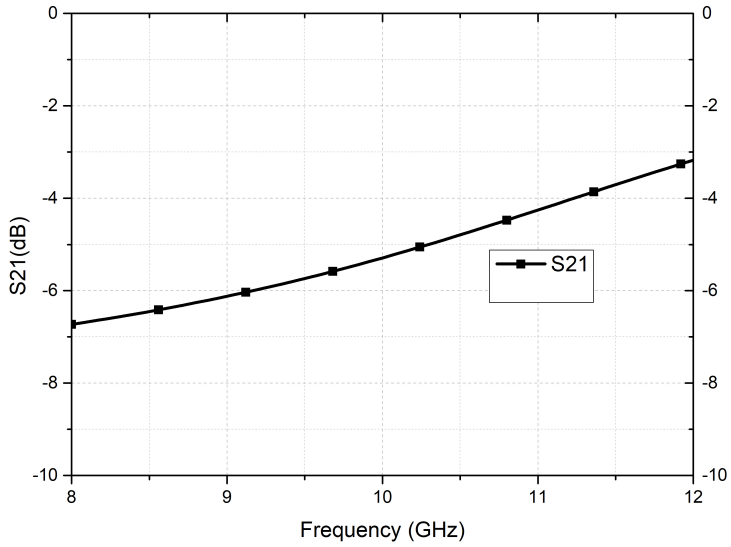

Figure 62: S21 measurement results of designed compact type gain-equalizer for TX chain

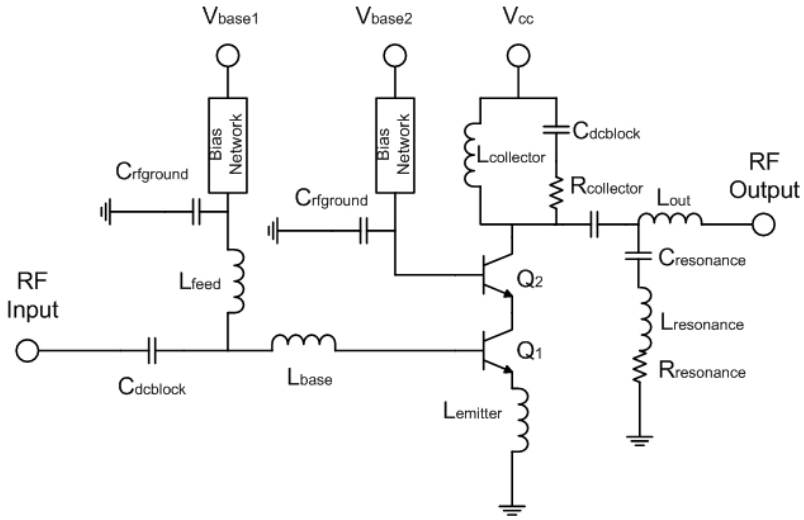

Figure 63: Schematic of an active gain-equalizer

4.3.4 Active Gain-Equalizers for T/R Module

Fig.63 depicts the schematic of the active gain-equalizers which are designed by myself in collaboration with Can, my colleague in RF-IC group. These equalizers are employed in common chain of T/R Module. Single stage cascade topology selects in this topology. As a different from an amplifier design, transistor numbers are chosen for providing positive gain-slope.

Input part of the active equalizer is used for matching to 50Ω. $L_{emitter}$,L_{feed}, and L_{base} form the input matching of the gain-equalizer. $L_{emitter}$ is also used for increasing the linearity of the amplifier.

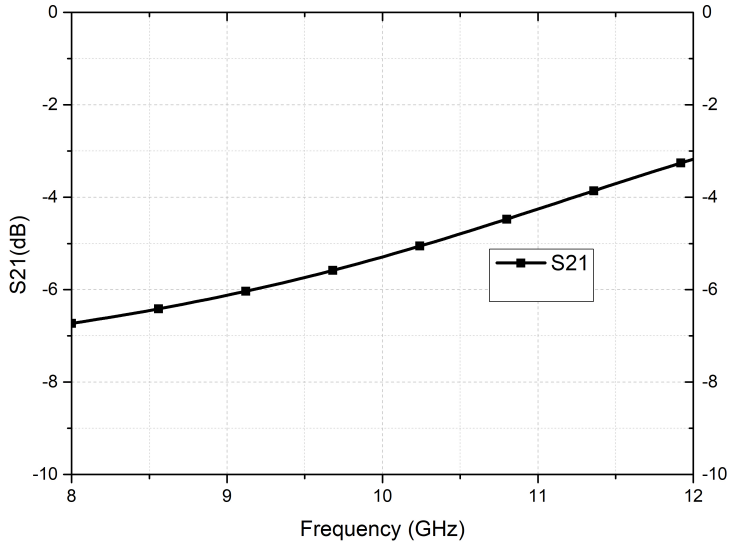

Figure 64: S11 and S22 measurement results of designed first active gain-equalizer

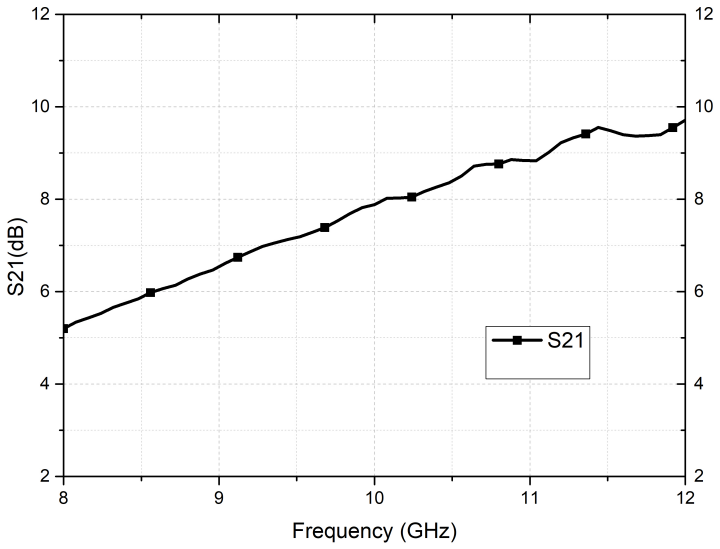

Figure 65: S21 measurement results of designed first active gain-equalizer

The output part of the active equalizer is used for creating the positive gain-slope vs frequency and matching the network to 50Ω. $L_{collector}$ and $R_{collector}$ is the conventional output matching network with the output capacitance. After this matching network, RLC resonance network is added for increasing the positive slope of the amplifier. The effect of RLC network is shown in Fig.51d. L_{out} is employed for matching this block to 50Ω.

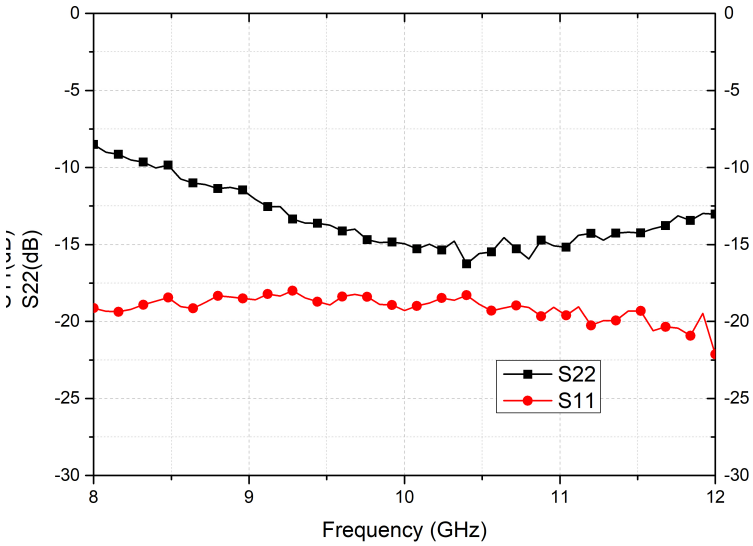

Figure 66: S11 and S22 measurement results of designed second active gain-equalizer

Two different active equalizers are employed in order to provide different positive gain-slope vs. frequency. Fig.64 shows the S_{11} and S_{22} measurement result of the

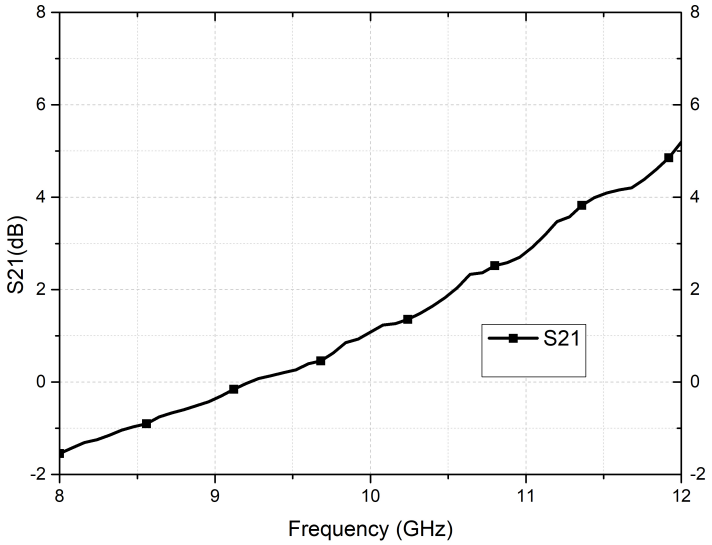

Figure 67: S21 measurement results of designed second active gain-equalizer

gain-equalizer which is used in TX chain. Insertion-loss graph of this gain-equalizer depicts in Fig.65.

Fig.66 shows the S_{11} and S_{22} measurement result of the gain-equalizer which is used in TX chain. Insertion-loss graph of this gain-equalizer depicts in Fig.67.

4.4 T/R Module overall gain behavior

IHP 0.25-μm SiGe BiCMOS technology is utilized for the realization of this T/R module. The sub-blocks of T/R module construct the whole system. While combining each block, transmission lines with 50Ω are utilized. The width of the transmission line is 16 μm. The signal line is drawn with top-metal-2 and ground line is drawn with metal-1. Each block is placed to the close the other block to prevent the degradation of the 3-dB positive slope gain.

The overall T/R module achieves 3 dB positive slope gain with respect to the frequency in transmitter path and in receiver path. Fig. 68 shows gain vs. frequency slope in TX mode and Fig. 69 shows gain vs. frequency slope in RX mode.

By achieving this slope, the core T/R module chip can integrate with III-V technology without adding extra discrete component to shape the gain behaviour of T/R module.

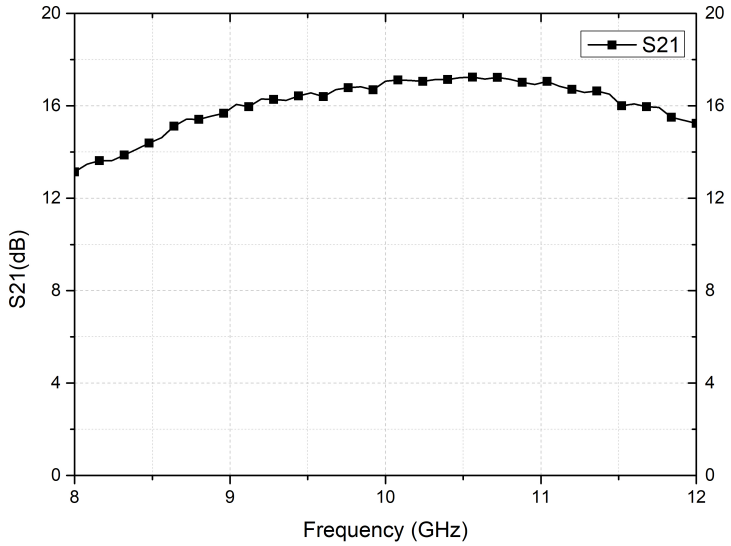

Figure 68: S21 measurement result of TX chain of T/R Module

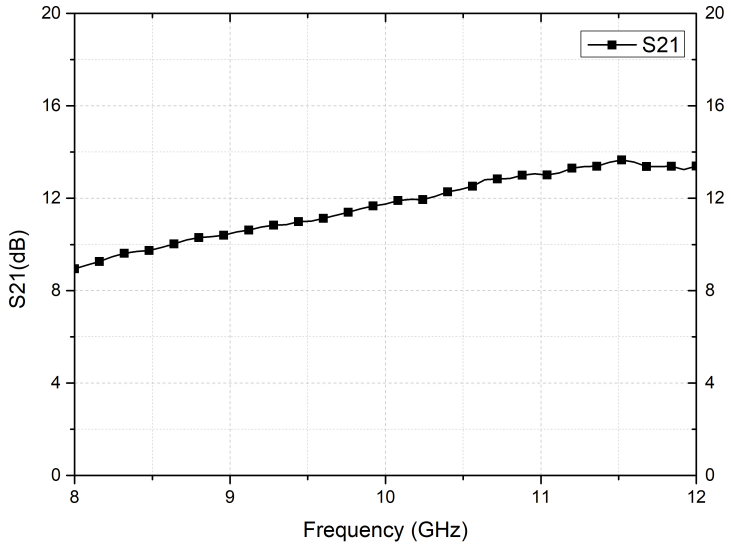

Figure 69: S21 measurement result of RX chain of T/R Module

5 Conclusion & Future Work

5.1 Summary of Work

Modern phased array radar systems consist of thousands of radiating elements, T/R modules, to adjust the angle of the overall antenna to achieve fast beam scanning. Phased arrays play an important role in the performance of T/R modules. The cost of these modules is also a critical issue. With the recent developments in SiGe BiCMOS technology, these modules are realized in SiGe BiCMOS technology with low cost to achieve high-performance T/R modules.

A 7-bit low insertion-loss high phase resolution passive X-band phase shifter and passive and active gain-equalizers which are realized in SiGe BiCMOS technology for modern phased arrays are realized. After the introduction of the phased array modules, phase shifter fundamentals and phase shifter topologies are discussed. High-pass /low-pass passive phase shifter is chosen to achieve high phase resolution without consuming power. New switching technique is applied in order to decrease the insertion-loss.

The low insertion-loss high phase resolution switched filter based 7-bit passive phase shifter for modern X-band phased arrays in a SiGe BiCMOS technology is presented in the following chapter. This phase shifter achieves $< 6^{\circ}$ RMS phase error with $< 0.7dB$ RMS amplitude error between 9-11 GHz. To the best knowledge of the authors, this phase shifter achieves highest phase resolution with a low insertion-loss at X-band. The overall phase shifter occupies 6 mm^2 area, has no DC power consumption.

Positive gain sloped passive and active gain-equalizers for modern X-band phased arrays in a SiGe BİCMOS technology is demonstrated in the last part of the thesis. These equalizers are realized for positive slope gain behavior with respect to the frequency at X-band. At the end of this part, T/R module achieves positive slope gain with respect to the frequency.

5.2 Future Work

As a short-term future work, the simulation results of the passive 7-bit phase shifter needs to be verified with measurement results. After the measurement ver-

ification of the phase shifter, the bandwidth of the phase shifter can be increased with new techniques to overcome high RMS phase error values at the edge of the X-band. Also, after the verification, this phase shifter can be integrated into the T/R module to decrease the power consumption of the whole system.

Passive gain-equalizers can be improved to get the higher positive slope. These equalizers can be employed instead of using active gain-equalizers. Moreover, the overall gain behavior of T/R module is different from the 3-dB positive slope. In order to achieve this behavior, active equalizers can be updated.

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