HIGH RESOLUTION, PROCESS AND TEMPERATURE COMPENSATED PHASE SHIFTER DESIGN USING A SELF GENERATED LOOK UP TABLE

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ABSTRACT

HIGH RESOLUTION, PROCESS AND TEMPERATURE COMPENSATED PHASE SHIFTER DESIGN USING A SELF GENERATED LOOK UP TABLE

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PhD Dissertation, August 2016

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Phase resolution is one of the most important parameters in phased array RADAR determining the precision of antenna beam direction and side-lobe level. Especially, in tracking applications the antenna directivity should be high and side-lobe levels must be low in order to abstain from the signals of Jammers. Phase shifters (PS) set phase resolution and directivity; therefore, they are the key components for phased arrays.

Among the PS topologies, vector sum type comes forward due to its significant advantage over the other design techniques, in terms of insertion loss, phase error, area and operation bandwidth. However, in design of vector sum type PS, phase and amplitude errors in vectors, and phase insertion of variable gain amplifiers degrades the phase resolution performance of the PS.

In order to overcome these issues and improve bit resolution (reduced phase step size and lower phase error while covering 360° phase range), and improve the tolerance on process - temperature variations, the proposed solution in this thesis is the design of a calibration circuit consisting of Power detector (PD), Analog to Digital Converter (ADC) and a Digital Processing Unit (DPU). The main objective of the calibration loop is the generation of a Look up Table (LUT) for target frequency band and at operating temperature. With this technique, the first 7-bit Phase shifter is designed in SiGe-BiCMOS technology, which also has highest fractional bandwidth in literature.

ÖZET

KULLANDIĞI DOĞRULUK TABLOSUNU KENDİSİ OLUŞTURARAK SICAKLIK VE ÜRETİM KAYNAKLI FAZ HATALARINI AZALTAN, YÜKSEK ÇÖZÜNÜRLÜKLÜ FAZ KAYDIRICI TASARIMI

EMRE ÖZEREN

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Faz çözünürlüğü, anten huzme yönü hassasiyetini ve kenar lobu seviyesini belirlemesi sebebiyle faz dizili RADAR'ın en önemli performans parametrelerinden birisidir. Özellikle, iz takip etme uygulamalarında frekans bozucuların sinyallerinden kaçabilmek için anten huzme yönünün hassaslığı yüksek ve kenar lob seviyesi düşük olmalıdır. Faz kaydırıcılar (FK) yön hassasiyetini ve faz çözünürlüğünü belirleme özellikleriyle faz dizili sistemler için anahtar bileşenlerdir.

Vektör toplama tekniği; kayıp seviyesi, faz hatası, alan ve frekans aralığı açısından FK tasarım yöntemleri arasında öne çıkmaktadır. Öte yandan, vektör toplama tipi FK tasarımlarında, vektörlerin faz - genlik hataları ve ayarlanabilir kazançlı kuvvetlendiricilerin faz eklemesi sebebiyle, faz çözünürlüğü performansı düşmektedir.

Bahsi geçen sorunların üstesinden gelinmesi, çözünürlüğün arttırılması (yani 360 derecelik faz aralığını kapsayacak şekilde, faz adımlarının küçültülmesi ve faz hatasının azaltılması) ve üretim-sıcaklık varyasyonlarına toleransın arttırılması amacıyla, bu tez kapsamında, güç algılayıcısı, analog-sayısal çevirici ve sayısal işlem ünitesi içeren bir kalibrasyon devresi önerilmiştir. Kalibrasyon döngüsünün temel amacı hedeflenen frekansta ve bulunulan sıcaklıkta doğruluk tablosu üretmektir. Bu yöntemle, Si-Ge BiCMOS teknolojisiyle tasarlanmış literatürdeki ilk 7-bit faz kaydırıcı gerçeklenmiştir. Bu devre aynı zamanda hedeflenen frekans bandlarındaki, band aralığı oranı en geniş devredir.

To my wife, Hatice and to my son, Mehmet

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This dissertation would never have been completed without my wife Hatice, whose love has been an inspiration. Thank you for every day.

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LIST of ABBREVIATIONS

ANT	Antenna
APAR	Active Phased Array RADAR
ADC	Analog-to-Digital Converter
AAW	Anti-Air force Warfare
BALUN	BALanced UNbalanced
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BP	ByPass
BP-LP	ByPass-Low Pass
BJT	Bipolar Junction Transistor
CB	Common-Base
CE	Common-Emitter
CR	Capacitor-Resistor
DAC	Digital-to-Analog Converter
DC	Direct Current
DBF	Digital Beam Forming
DPU	Digital Processing Unit
DTI	Deep Trench Isolation
EIRP	Equivalent Isotropic Radiated Power
FT	Cut-off frequency
FOM	Figure-of-Merit
FPGA	Field Programmable Gate Array
GCR	Gain Control Range
Ge	Germanium
HB	High Breakdown-voltage
HBT	Heterojunction Bipolar Transistor
HFET	Heterojunction Field Effect Transistor
HEMT	High Electron Mobility Transistor
HP	High Performance
HP-LP	High Pass-Low Pass
HPF-LPF	High Pass Filter-Low Pass Filter
IF	Intermediate Frequency
IL	Insertion Loss
I	Inphase
I/Q	Inphase/Quadrature
iNMOS	Isolated NMOS
LCQAF	Inductor capacitor resonance based quadrature all pass filter
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Pass
LSB	Least Significant Bit
LUT	Look Up Table
MESFET	Metal Semiconductor Field Effect Transistor
MEMS	MicroElectroMechanical System
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuits
mPA	Medium Power Amplifier
MSB	Most Significant Bit

NMOS	N-channel Metal Oxide Semiconductor
NF	Noise Figure
OPAMP	OPeration AMPlifier
P1dB	1dB Compression Point
PA	Power Amplifier
PAWS	Phased array warning system
PD	Power Detector
PMOS	P-channel Metal Oxide Semiconductor
PPF	Poly Phase Filter
PS	Phase Shifter
RADAR	Radio Detecting And Ranging
RC	Resistor-Capacitor
RCPPF	Resistor-Capacitor Poly Phase Filter
RF	Radio Frequency
RL	Return Loss
RMS	Root-Mean-Square
RS	Serial Resistance
RTPS	Reflection Type Phase Shifter
RX	Receiver
Q	Quadrature
S	Sum (vector)
SAR	Successive Approximation Register
SiGe	Silicon-Germanium
SNR	Signal to Noise Ratio
SPDT	Single-Pole-Double-Throw
TLQG	Transmission Line Based Quadrature Generator
T/R	Transmit/Receive
TX	Transmitter
VGA	Variable Gain Amplifier

1. INTRODUCTION

1.1. Phased Array RADAR

RADAR (RAdio Detecting and Ranging) is a substance detection scheme, that resolves the distance, direction, speed, and more features of both mobile and immobile substances through the utilization of electromagnetic waves. The first establishment date of RADAR backs to the first World war, and its progress has developed to more and more complicated schemes. The first antenna array is introduced by Fris in 1937, which has enhanced directivity that maintains an advancement in signal to noise ratio (SNR) [1]. Despite the mechanical adjustment, it was the earliest prototype of the modern phased arrays. In this system, the numerous dipole antennas are located in $\lambda/4$ separation and in parallel position. The direction of the highest power wavefront is dictated through adjusting the phase of each radiating element and utilizing the constructive and destructive interference. The highest power wavefront could be turned to any specific location through a matrix of radiating elements. The conventional view range has the form of a cone with a central angle around 90-120°. Higher directivity and enhanced resolution can be maintained through the higher number of elements in the array. Enhanced resolution is required to distinguish numerous objects which are in adjacency to each other and far away from the RADAR. Electronically steered array was evolved, close to the end of second World War [2].

The competence to dictate the beam without utilization of mechanical schemes, is the most important superiority of phased array over conventional systems. This competence maintains following assets [3]:

- Higher reliability
- Higher data rates
- Immediate beam positioning
- Removal of mechanical errors
- Operation in numerous approaches
- Capability of aiming numerous targets

The disadvantages of phased array radar in comparison with the conventional radar are

- The resolution is reliant on the quantity of radiating element and resolution of the phase shifter
- High quantity of antennas and T/R modules are needed for phase and amplitude control

These modules consist of individual chips for power amplifier (PA) and low noise amplifier (LNA- typically GaAS or InP) and individual chips for switches and phase shifters (typically p-i-n diodes). Various examples can be found in literature [4] [5] [6] [7] [8] [9]; however, in evolution of low prized– high performance phased arrays, the area consumption and expense of these modules are still important issues.

In contemporary implementations, particularly military missile defense systems, phased array radar is the preference. For instance, the Patriot system has phased array radar, which served in The Gulf War [10] . The system is portable and moveable, and combined to a missile firing platform [11] . The competence of aiming numerous targets is enhanced by the fast scanning of phased array radar. Phased array warning system (PAWS) is an additional instance for phased array radar applications [12].

Construction of a low prized phased array radar module operating at 35 GHz (the expense is $30/element) is enabled through the evolution of monolithic microwave integrated circuits (MMIC) [13]. In addition, one of the main targets of phased array is to be able to integrate as much RF front-end blocks as possible into a single solid-state chip, with the ultimate goal of wafer scale phased arrays [14]. Moreover, digital control of phase and

amplitude for each antenna element (which is called digital beam forming-DBF) is attainable because of the developments anticipated by the Moore's law [15]. Furthermore, developing and merging miscellaneous digital and non-digital capabilities (such as Microelectromechanical systems and 3D integration) to semiconductor components is enabled through the new plan, More than Moore [13] .

1.2 Phased Array Principles

In consideration of manipulating the orientation of the complete antenna beam electronically, multiple antenna phased arrays can be employed [16]. The radiation shape and the gain of the array can be manipulated through shifting the phase of currents in every element separately. Phased array transmitters and receivers are constructed by multiple antennas and signal paths, in which the signals transmitted or received by every antenna element are processed (by meaning of phase shifting or delay and amplification) and combined. Regarding to the application, the antenna elements of a phased array system can be ordered in one two or three dimensions [17]. A simplified n-element phased array receiver is demonstrated in Fig. 1. With the following assumptions: the signal for each element is *s(t)*, the target radiation angle is θ, the delay for each gradual element is τ; the combined signal, *S(t)*, is [13]

$$S(t)=\sum_{k=0}^{n-1} s\left(t-k\tau-(n-1-k)\frac{d\sin\theta}{c}\right) \tag{1}$$

This formula shows that, for target radiation angle, the signals from the whole quantity of array elements are accumulated coherently in which, *d* corresponds the spacing among the array elements, and *c* corresponds the velocity of the light. Therefore, gain of the array is strengthened in a desired direction and silenced in other directions called beam nulls, as shown in Fig. 1. (1) also shows that, for a transmitter of N-element phased array, antenna gain of the array will be N, and equivalent isotopically radiated power (EIRP) in the main beam direction will be N^2 times higher than the radiated power of a single element, with following assumptions. First, radiated power of each element is equal. Second, the array elements are isotropic, and weighted by linear

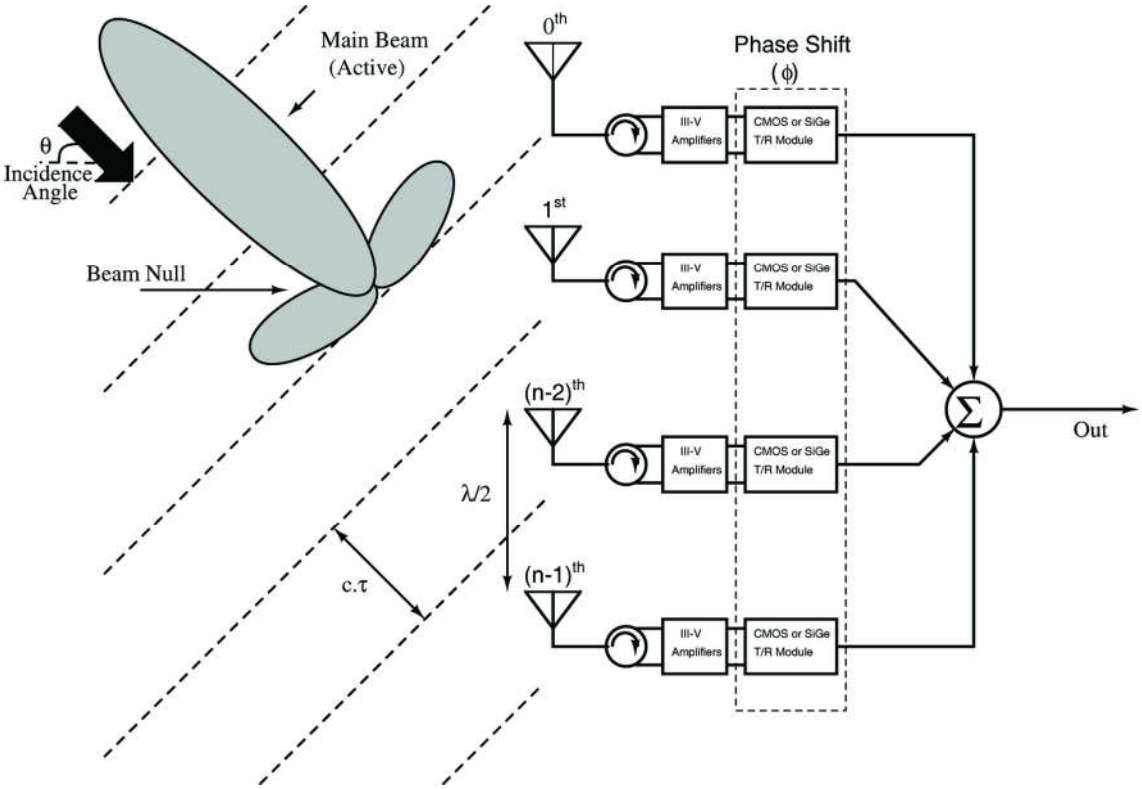


Fig. 1: Typical block diagram of the active electronically scanned phased-array radar system.

amplitudes. For instance, for a 10 element phased array with 15 dBm of radiated power from a single element, the EIRP of the system is 35 dBm (10 dB by antenna gain, and 10 dB by overall transmitted power). For a phased array in which thousands of elements are combined, this expansion in the signal power will be much more significant.

In receiver side, each array element receives the radiated signals from the aimed object at different instant. The incidence angle can be directed to target angle through appropriate phase shift and separation among the elements. Received signal power is reinforced in the incidence angle, and weakened in other directions. Suppression of these interferences is not the only benefit of phased array, which also maintains enhanced sensitivity at receiver [18].

1.3 Phased Array Architectures

Transistor speed and breakdown voltage, losses of the passive components, low power budget, and low circuit area are the essential restraints which have significant effect on

complete system performance. For silicon based phased array schemes, various architectures are proposed in consideration of meeting these requirements [19], [20], [21].

Gain variations for different time delays, and different frequencies; delay variations for different array element causes incorrect information data about the aimed object. Therefore, phase shift can be implemented at different stages of the phased array receiver. The phase shift can be applied at RF stage (All-RF architecture), at baseband (or IF) stage, at local oscillator (LO) stage, or in digital domain. The trade-off in power consumption, cost and area determines the architecture selection.

Excessive amount of mixers are employed in IF and LO phase shifting architectures, which consume significant die area and power. Allocation of the LO signal is another difficulty of these architectures in addition to the demand of extremely high performance of phase noise (for a 10 GHz carrier, -133 dBc/Hz at 10 MHz offset [22]). This demand can be met through employing external oscillators solely, which causes higher cost and area. Moreover, IF phase shifters are employed in these architectures, which are not appropriate for phased array implementations [23]. For this reason, the trend in phase shifter design is to operate at high frequency [24], [25]

In digital phase shifting architectures, for the sake of avoiding the distortion in processing of all of the approaching signals, a high dynamic range analog-to-digital converter (ADC) is necessary. In these architectures, phase shift is applied in digital domain, therefore, high-speed and excessive amount of A/D converters are demanded, which causes significantly higher area and power consumption.

Due to the employment of only one mixer and LO for down conversion to IF stage, the all RF architecture is the most condensed and appropriate architecture in consideration of silicon based integrated phased array systems. In addition to the other benefits of all RF architectures, the interference can be considerably restrained prior to the consecutive building blocks of the receiver because the output signal is processed subsequent to the RF combiner. Therefore, the linearity specifications of consequent building blocks are relaxed. However, the loss of phase shifters is the most important challenge for these architectures, which needs to be compensated by additional amplifiers.

1.4 Building Blocks of T/R Module

In this work, All-RF phased-array architecture is chosen, rather than IF or LO phase shifting architectures, due to its higher pattern directivity, and higher interferer rejection capability [26]. In addition, All-RF phased array architecture does not require integrated high performance local oscillators, and complex LO distribution networks which consumes significant die area especially for large arrays with hundreds of elements [26]. Fig. 2 shows the block diagram of proposed X-band phased array T/R module core chip, with block level target specifications. The benefit of this architecture is to share phase shifter and attenuator in both of the transmit (TX) and receive paths (RX), which saves the chip area and power consumption [27], [28]. In addition, bi-directional functionality for phase shifters and amplifiers is not a must for this architecture, which allows active structures for phase shifters, such as Vector Sum structure. On the other hand, for path selection, three SPDT switches are used which a have limited (around 30 dB for a typical switch) isolation performance. If the gain requirement of a T/R module core chip (typically 25 dB) is covered with only PA, LNA, or the amplifiers at the common path (which are connected to shared PS and Att), due to low isolation performance of the switches, the RX_{in}-TX_{out} isolation performance becomes strictly limited. As an improvement to the well-known *All-RF* architectures in literature [26], [28], in our work, two linear amplifiers are connected to TX/RX SPDT as depicted at Fig. 2. With using these amplifiers, gain requirement for LNA and PA are reduced, and, therefore, RX_{in}-TX_{out} isolation performance is improved in architectural level.

The core chip is composed of SPDT switches, phase shifter, attenuator, Low noise amplifier, linear amplifiers, and power amplifier. HBTs are used for the amplifiers for their high f_T, and low noise. In addition, we have also used HBTs in design of attenuator and SPDT due to their low insertion loss.

In this subsection, the reasons behind the specifications of the building blocks (which are depicted at Fig. 2) are clarified, whereas the function of these building blocks

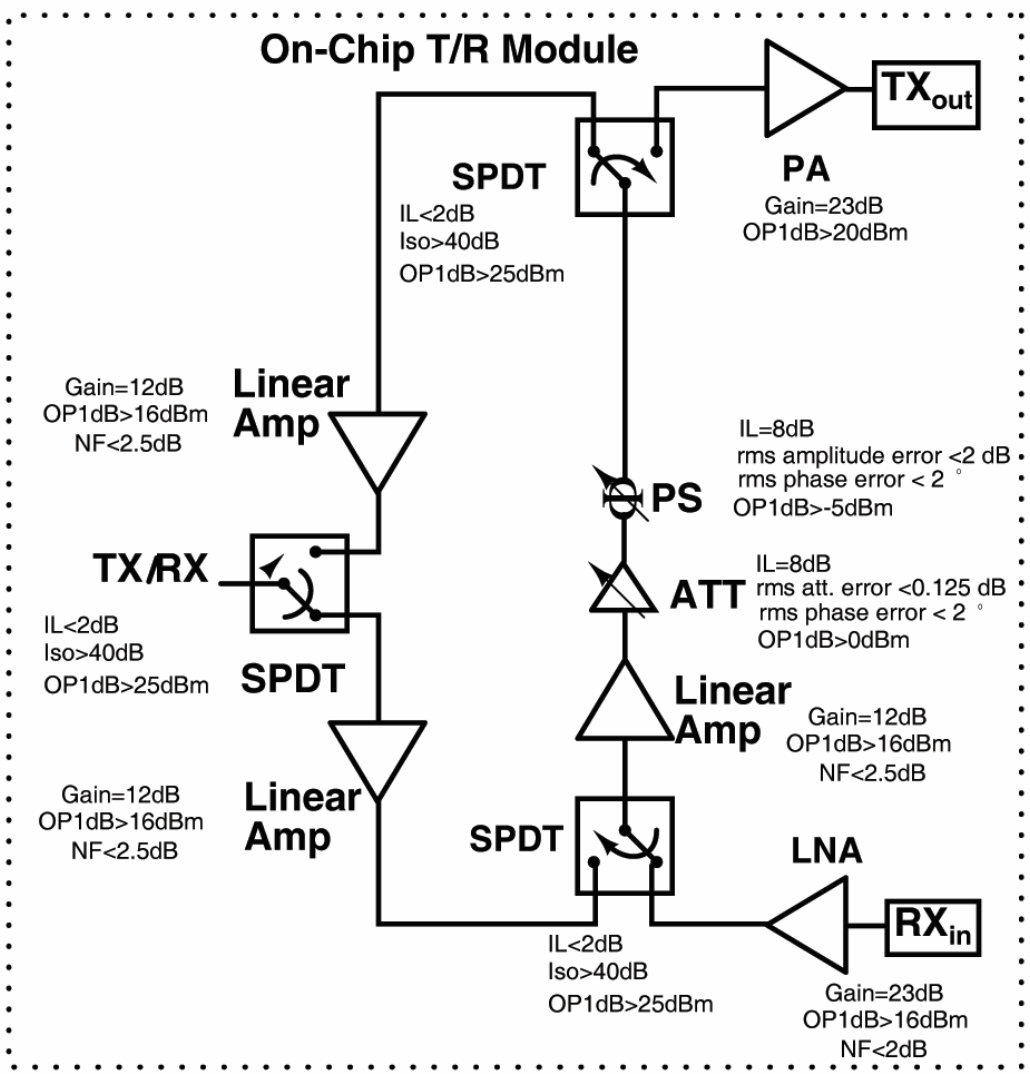


Fig. 2: Block diagram of proposed X-band phased-array transmit/receive core chip.

are epitomized. In addition, at the end of this subsection, the function and the impact of phase shifter on phased array radar is explained in detail. Three SPDTs are employed in this T/R module core chip; therefore, the IL of this block must be as low as possible in order to achieve high gain from the module. In addition, isolation performance is important to reduce the leakage from the output of transmitter to input of receiver. In comparison with other performance parameters of a typical SPDT, (such as power handling capability, and operation bandwidth) insertion loss (IL) and isolation have more significance. Because 4 GHz of operation bandwidth is not a challenging specification for SPDT, and maximum 0 dBm of signal power will be applied on these building blocks. Regarding these considerations (IL < 2 dB and isolation > 40 dB), and the SPDT switch is designed using quarter wave double shunt switch topology, and employing HBTs in reverse saturation configuration.

LNA has high significance for T/R module due to determining the noise figure of the receiver. Regarding the performance of state of the art T/R modules in literature ([29], [30], [27]), overall noise figure target is selected as 5 dB. Because of employing noisy components such as PS and attenuator, high gain and low NF is crucial for LNA. Although more than 33 dB of gain is applied before the attenuator (as depicted in Fig. 2), 3 dB of NF comes from cascaded PS and attenuator, and NF of LNA must be lower than 2 dB. Targeting more than 25 dB of gain in a single building block increases the risk of oscillation; for this reason, 35 dB of gain is shared between the linear amplifier and LNA. 23 dB of gain is aimed for the first stage. However, applying high gain in first stages degrades the linearity performance of the whole module. For this reason, minimum 16 dBm of OP1dB performance is aimed in this block.

As depicted in Fig. 1, the core chip is designed to be cascaded to III-V amplifier blocks which have capability of delivering high output power such as 36 dBm. For the sake of reaching this power level, T/R module core chip needs to have the capability of delivering around 10 dBm of signal power to III-V blocks. Considering the linearity issues, at least 20 dBm of OP1dB compression point performance is required at (medium) power amplifier stage (mPA). mPA is designed to be employed as an intermediate component between III-V based RF blocks and Si-based IF blocks, thus, its requirements are not as harsh as a traditional PA. However, obtaining high output power with a flat gain response at wide bandwidth is challenging. Concerning these specifications, a two-stage cascode topology is chosen.

Resolution of the attenuator is a significant performance parameter for a T/R module because it determines gain control capability. On the other hand, from noise perspective, the loss of this passive block must be as low as possible because it is cascaded to an active phase shifter which has high noise figure. For minimum attenuation state, 8 dB of loss is specified for this building block, considering 6 cascaded attenuation blocks. 31.5 dB of attenuation range will be covered with 6-bit digital control, and LSB is 0.25 dB. Therefore, 0.125 dB of rms amplitude error is aimed in this block. Insertion phase of this block varies for different attenuation states, root-mean-square of this variation must be lower than 2° concerning phase performance of the system. Regarding these considerations, HBTs are chosen rather than MOS devices and reverse saturated configuration can be preferred. In

this design, combination of cascaded switched Pi-type and T-type attenuator blocks can be utilized in order to achieve 6-bit operation.

The role of phase shifter is to introduce progressive phase difference (Φ) at antenna elements for changing the direction of antenna beam. The relationship between direction of antenna beam and phase difference is [31].

$$\theta = \sin^{-1}\left(\frac{\lambda}{2\pi d}\phi\right) \tag{2}$$

Here λ is wavelength, d is the spacing between antennas and θ is the incidence angle, as previously depicted at Fig. 1. (2) shows that, an accurate phase shifter is required for accurate Φ which is required to control the direction of antenna beam, θ, precisely. A digital phase shifter with N bits has 2^N phase states divided by phase steps of $2\pi/2^N$. This discretization allows only a staircase approximation of the continuous progressive shift required for the array. The staircase phase front results in a periodic triangular phase error. If the mean square of this error is calculated in one half of the phase step, phase quantization error variance is [32],

$$\overline{\phi^2} = \frac{1}{3}\frac{\pi^2}{2^{2N}} \tag{3}$$

Expression (3) is important to show the impact of phase shifter resolution on quantization error. Quantization error is added from phase shifter, and it has two important impact on phased array RADAR; reduced Directivity (and gain) and increased side lobe level. If there is amplitude error and phase error, the directivity is [33],

$$\frac{D}{D_0} = \frac{1}{1+\overline{\phi^2}+\overline{\delta^2}} \tag{4}$$

In this formula, $\overline{\delta^2}$ is the normalized amplitude error variance, and D_0 is the directivity without the quantization error. (3) and (4) shows that, as the resolution of phase shifter increases, quantization error decreases and directivity increases.

The average side lobe level, far from the beam peak and normalized to the peak, is a constant given by [33]

$$SL_{dB} = 10\log\overline{\sigma^2}\text{, and, } \overline{\sigma^2} = \frac{\overline{\phi^2} + \overline{\delta^2}}{N\varepsilon_A} \tag{5}$$

Where, ε_A is the aperture efficiency. The formulas (3) and (4) refer to linear and planar arrays. The element pattern gain has been taken away from these formulas because they are normalized to the beam peak. Expression (5) shows that, quantization error of phase shifter, $\overline{\phi^2}$, and phase shifter resolution, N, have direct impact on side-lobe level. For instance, side-lobe level of a phased array radar can be reduced 10 dB through the reduction of rms-phase error from 10° to 3.2°, and reduction of rms-amplitude error from 1.5 dB to 0.5 dB (these values can be achieved through simultaneous control of attenuator and phase shifter) [33]. High phase shifter resolution is also significant for reduction of the cost of a phased array radar. For instance, considering the same side lobe levels, 100 antenna elements with 7-bit phase shifters can be used rather than 5000 antenna elements with 4-bit phase shifters [33].

In addition to these system level benefits, high resolution phase shifters can also be used to compensate phase error resulting from the building blocks of T/R modules such as attenuators, variable gain amplifier, etc. For these reasons, designing a 7-bit phase shifter with rms phase error lower than 2° is aimed for the proposed T/R module. Around 8 dB of insertion loss of PS can be compensated with other building blocks. OP1dB compression point of is -5 dBm is aimed for this project. However, it is not a strict requirement, because, as previously mentioned in mPA section, around 10 dBm of signal power will be delivered to III-V blocks.

1.5 Selected Technology: SiGe BiCMOS

In design and realization of T/R modules for phased array RADAR, III-V technologies are generally preferred, such as GaAs and GaN [34]. As a result of the developments in SiGe bipolar complementary metal oxide semiconductor (SiGe BiCMOS) technologies, heterojunction bipolar transistors (HBT) in this technology shows a comparable

performance with their III-V substitutions. Therefore, realization of single chip T/R modules for microwave and millimeter wave implementations is feasible.

The advancements in RF performance of SiGe HBT is significant for phased arrays, however, the integration capability of this technology with CMOS is a more important superiority over its III-V substitutions. In addition, yield, cost and manufacturing assets of silicon CMOS fabrication also serve to this technology. Moreover, combining the RF and microwave circuits with digital circuits is not complicated in this technology. In Table 1, other technologies are collated with SiGe HBTs.

III-V technologies are generally used in fabrication of phased arrays with ultimate specifications demanded by military implementations. Essential utilization area of SiGe technology is the profitable implementations, for instance, RFID, short range movable RADAR, weather RADAR, radio astronomy, satellite communications, biomedical implementations, and short range indoor communications. To sum up, SiGe BiCMOS is a preferable technology, in realization of completely integrated, inexpensive, featherweight transmit – receive modules and system-on-chip solutions utilized in microwave and millimeter wave phased array implementations.

Table 1: Respective performance collation of IC technologies
(Excellent: ✓✓; Very Good: ✓; Good: 0; Fair: -; Poor: - -) [35]

Performance Metric	**SiGe HBT**	**SiGe BJT**	**Si CMOS**	**III-V MESFET**	**III-V HBT**	**III-V HEMT**
Frequency Response	✓	0	0	✓	✓✓	✓✓
1/f and Phase Noise	✓✓	✓	-	- -	0	- -
Broadband Noise	✓	0	0	✓	✓	✓✓
Linearity	✓	✓	✓	✓✓	✓	✓✓
Output Conductance	✓✓	✓	-	-	✓✓	-
Transconductance	✓✓	✓✓	- -	-	✓✓	-
Power Dissipation	✓✓	✓	-	-	✓	0
CMOS Integration	✓✓	✓✓	N/A	- -	- -	- -
IC cost	0	0	✓	-	-	- -

1.7 Thesis Objectives

This thesis is written on phase shifter design for phased array RADAR with improved bit resolution (reduced phase step size and lower phase error while covering 360° phase range) and tolerance on process - temperature variations. Among the PS topologies, vector sum type comes forward due to their significant advantages over the passive PS (RTPS, switched line, loaded line, HPF/LPF switching based PS) in terms of insertion loss, phase error, area and operation bandwidth. However, in vector sum type PS, it is not possible to create two signals with 90° out of phase without amplitude and phase errors in a wideband operation. In addition, variable gain amplifiers are utilized to control amplitude of the vectors, and they cause additional phase error. Moreover, both I/Q vector generation circuits and amplitude control circuits have less tolerance on process and temperature variations. The main objective is to answer these issues and to create circuit approaches that are applicable to the design of PS for phased array RADAR.

In order to overcome these issues, the proposed solution is the design of a calibration circuit consisting of an on-chip measurement circuit, an analog to digital converter (ADC), and a digital processing unit (DPU). Calibration module and core circuit are separated with a single pole double throw (SPDT) switch. When the calibration mode is on, output of the VGA of the PS is connected to the power detector which measures amplitude of the vector. This measurement will be converted to digital with an ADC. The DPU is used for the control of the PS, calculation of phase error and generating the look up table (LUT). The system will act as PS, when the calibration mode is off, and the self-generated LUT will be used in this PS. Function of the digital circuit can be summarized as:

1- Controlling PS for measurement of I and Q vectors for all possible vector magnitudes and all of the magnitude combinations of I and Q vectors which forms S (sum) vector, and recording this data in register arrays

3- Calculation of phase error for each phase state and for all possible vector pairs, using the cosine formula and the magnitude data in I, Q and S register arrays

4- Determining the optimum vector pairs (which have minimum phase error) for each of the phase states,

5- Saving this vector pair control data in a LUT which controls PS when the calibration mode is off.

The impact of this technique can be summarized as:

- I/Q amplitude mismatch will be reduced significantly due to on-chip measurement of I and Q.
- VGA phase error will be reflected to S vector, and it will be measured in power detector and considered in calculations; therefore, this error will also be reduced.
- The circuit will generate its own LUT after fabrication. Therefore, tolerance on process variations will be higher.
- The circuit will generate its own LUT at operating temperature. If the temperature change is discerned, user can recalibrate the circuit for the purpose of generating a new LUT for that temperature.

1.8 Thesis Overview

The thesis is organized as six chapters. Following chapter is a review for phase shifters. Active and passive phase shifter topologies are presented and their performances are compared. It is shown that vector sum topology offers highest phase resolution, lowest phase error, lowest insertion loss and highest operation bandwidth. In this chapter, design challenges of vector sum technique are also explained.

In third chapter, the proposed solution for these design challenges is introduced. In this chapter feasibility of the system is also investigated and idea is tested with using a matlab script. Design requirements of the building blocks are derived using matlab level simulations.

In chapter 4, design and implementation of the building blocks are described. In this chapter, especially, novel design methodologies for power detector is explained in detail. Design details, simulation and measurement results of coupler, amplifier, ADC and DPU are also discussed in this chapter.

In chapter 5, simulation challenges and solution techniques are disclosed. The first version of the system, consisting of the RF front end circuits such as phase shifter, LNA,

PD and coupler, is presented. In this chapter, the second version of the system consisting of integrated baseband and RF circuits is also introduced. Moreover, measurement plan and setup is also described. The simulation and measurement results of the first version and second version of the calibration system are demonstrated.

Chapter 6 concludes the thesis with some additional discussion on the problems encountered throughout the thesis and provides information on possible future studies.

2. REVIEW OF PHASE SHIFTER DESIGN TECHNIQUES

In this section the literature review for Phase Shifter (PS) types is presented. There are two categories for phase shifters; Passive PS and Active PS. Passive PS uses passive circuit for phase shifting, such as inductances, capacitances and transmission lines. These PS are bi-directional, highly linear (in terms of IP1dB) and they do not consume power. However, their insertion loss is significantly high, hence power hungry amplifiers are required. In addition, they consume a large area. There are five types of passive PS; switched-line PS, loaded line PS, reflection type PS, switched filter type PS, and PS with distributed active switches. Vector - sum type PS are categorized as active PS, which use active circuits such as BALUN, variable gain amplifiers and summation circuits for phase shifting purpose. They have significant power consumption and their linearity is limited. However, higher phase resolution and lower phase error can be achieved in lower die area with smart design techniques.

2.1. Passive Phase Shifters

Switched-Line phase shifting is the most straightforward approach. The operation is based on true time delay difference of two paths with different lengths, as shown in Fig. 3. The delay is depending on λ (c/f), therefore, it is a narrowband solution. In addition, in order to provide a high phase difference such as 180°, long path lines are required which increases the chip area and loss significantly. Moreover, two SPDT switches per bit are required which increases insertion loss (around 2 dB per switch). Furthermore, as path length changes, attenuation of the path also changes, which causes amplitude errors. In literature, due to high insertion loss (more than 2dB insertion loss per bit) of this

technique, GaAs or SOI technologies are preferred [36], [37]. In addition, due to low fractional bandwidth (lower than 0.1) and high area (higher than 0.5 mm^2 per bit), only one or two-bit PS are designed with this technique, [36] [37] [38].

In *Loaded-Line PS* phase difference is achieved by changing the line characteristics by changing the loading of the line, as shown in Fig. 3b. In this approach, one path and two different loads are utilized; therefore, the area is smaller than switched line. In addition, the switches are not series to the signal path; therefore, loss per switch is lower. However, similar to the switched line approach, for higher phase resolution, higher number of phase bits and switches are required. Therefore, insertion loss is still very high. The phase difference in this approach is also dependent on λ, therefore it is also a narrowband operation. In addition, the return loss strongly depends on phase shift, allowing only small phase shifts to be realized. [39] is a good example in the literature, and two PS are designed with this technique. The First PS is designed for minimum phase error, and achieved 2° rms phase error, 1.2 dB rms phase error. Second PS is designed for minimum gain error and achieved 0.5 dB gain error and 3.2° phase error. 1mm x 0.01 mm area is consumed in low loss and high cost 32nm SOI technology. These PS achieve good phase and amplitude error performances; however, only 3 bits of phase control is achieved in a low phase range (180°) and the fractional bandwidth is very low (0.17). State of the art switched line and loaded line type phase shifters are shown at Table 2.

Table 2: Comparison of Switched line and loaded line type phase shifters.

Ref	Process	Design technique	Freq. GHz	Frac. BW	Ph. Err. (°)	Gain Err. (dB)	Gain (dB)	Phase range	OP1dB (dBm)	Area mm^2	Pow. mW
[36]	GaAs pHEMT	Switched Line and RTPS	60	0,17	N/A	N/A	-9,10	360° (analog)	N/A	N/A	8,00
[37]	180 nm SOI	Switched Line	18	0,06	N/A	N/A	-3,00	360° (1 Bit)	11,00	N/A	0
[38]	130nm CMOS	Switched Line	57-64	0,12	N/A	N/A	-9,00	360° (2 Bit)	N/A	0,50	0
[39]	32 nm SOI	Loaded Line	60	0,17	2.0 / 3.2	1.2 / 0.5	-5.3 / -6.8	180° (3 Bit)	10,00	0.073 / 0.099	0

In *Reflection Type PS,* 90° hybrid coupler, or a 180° rat-race coupler (or a circulator) is used as shown in Fig. 3c. Two ports are terminated with variable loads which can be tunable passives (for instance varactors) or diodes and the other two ports are RF input and output. With tuning the impedance, the phase shift is acquired. In this type of PS, return loss performance is better than its alternatives due to the high isolation between the coupler ports. State of the art reflection type phase shifters are compared at Table 3. This type of PS is widely used at millimeter waves ([36], [40], [41], [42]) however they have significant disadvantages. First of all, analog control is applied which requires a high resolution DAC for digital control. In addition, for each chip DACs have to be calibrated. Secondly, this type of PS cannot cover 360° ([36], covers 180°, [40] covers 250°, [41] covers 190° and [42] covers 180°). Moreover, as the increase of operating frequency, quality factor of tunable loads decreases significantly, as well as insertion loss and phase performance.

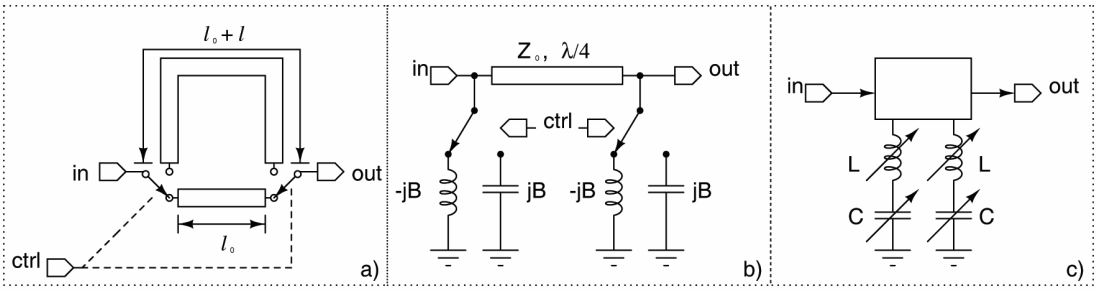


Fig. 3: a) Switched line phase shifter, b) Loaded line phase shifter, c) Reflection type phase shifter.

Table 3: Comparison table for Reflection type phase shifters

Ref	Process	Design technique	Freq GHz	Frac. BW	Ph. Err. (°)	Gain Err. (dB)	Gain (dB)	Phase range	OP1dB (dBm)	Area mm^2	Pow. mW
[40]	130nmCMOS	RTPS	60	0,23	N/A	1,70	-6,40	250° (2Bit)	N/A	0,20	0,00
[41]	90nm CMOS	RTPS	60	0,17	N/A	1,50	-9,30	190° (analog)	N/A	0,027	0,00
[42]	90nm CMOS	RTPS	23	Single Freq.	N/A	0,60	-13,00	275° (analog)	N/A	0,450	0,00

In *switched filter type PS*, similar to the switched line PS, path selection is used. However, instead of transmission lines, LC based filters which have different phase responses are used. There exist mainly two ways of creating phase difference between states with using filter type topology; HP-LP filter type [43] [44], and Bypass (BP)-LP [44]- [45] filter type. An example of high-pass/low-pass PS is in Fig. 4, where the signal path is swapped between high-pass and low-pass Π-network. Up to 90° phase shift can be maintained in a High pass or Low pass Π- or T-network. As a result of swapping between two different filter types, up to 180° phase shift can be maintained. Around center frequency two filters have almost parallel phase vs. frequency slopes, therefore fractional bandwidth of this type of PS is much more than its previous alternatives. For a HP-LP filter type PS each phase selection bit, two SPDTs are required. Under these conditions, BP /LP filter type PS can be a good candidate because each phase selection bit can be realized with only a single series switch. However, this type of PS is capable of providing up to 90° phase shift, and in a narrowband operation. State of the art switched filter type PS are presented at Table 4. Combination of HP/LP and BP/LP type PS are widely used in literature [44]- [45]- [46]. However, these type of PS have significant disadvantages. First of all, due to the lack of very low insertion loss RF switches in SiGe technology, high resolution passive PS topologies have significantly high insertion loss. For a 5-bit PS this loss can be up to 20 dB [46]. In addition, as resolution of PS increases, area consumption also increases. Moreover, these type of PS provide very narrowband solutions. For instance, [44] is a 6-bit PS designed for 7-12 GHz. This PS has 7.5° rms phase error in this bandwidth which is 34% more than its LSB (5.6°).

Active switches are also used in PS in order to use phase selection, [47]- [48]. A 3-bit PS using distributed active switches is presented in Fig. 5 which consists of eight stage of cascaded ladder network with series inductors and shunt capacitances. The phase shift per section can be derived as $\Delta\varphi \approx \omega\sqrt{LC}$, [49], and for a 4-bit PS L and C values are optimized in order to provide 22.5° phase shift for each step. Due to keeping the switches in active region, the loss per switch reduces significantly. However, for N bit PS 2^N L-C sections are required, which consumes significant area. For instance, a 6-bit PS requires 64 L-C sections. In addition, coupling between the inductances are very significant and electromagnetic simulations are very complex. Moreover, phase shift per section is frequency dependent and very narrowband. Performance of PSs using distributed active switches is summarized at Table 5.

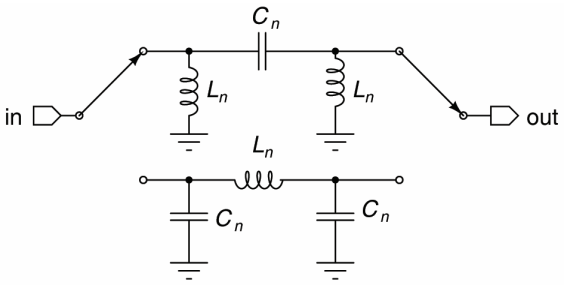


Fig. 4: High-pass/Low-pass phase shifter.

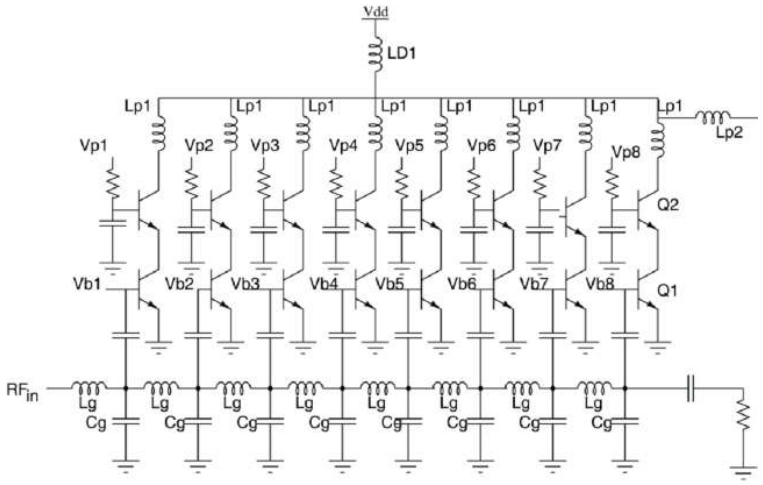


Fig. 5: 3-bit phase shifter using distributed active switches [47].

Table 4: Comparison table for Switched filter type phase shifters.

Ref	Process	Design technique	Freq GHz	Frac. BW	Ph. Err. (°)	Gain Err. (dB)	Gain (dB)	Phase range	OP1dB (dBm)	Area mm^2	Pow. mW
[43]	90nm CMOS	BP/LP	60	0,17	N/A	1,30	-15,60	360° (4-Bit)	N/A	0,280	0,00
[44]	180nm CMOS	HP/LP/BP	7 -12	0,67	7,50	1,10	-15,70	360° (6-Bit)	N/A	1,900	0,00
[45]	180 nm CMOS	HP/LP/BP	2,8	0,25	2,00	1,50	-13,00	360 (6-Bit)	-11,00	4,160	0,00
[46]	130 nm SiGe	Passive HP/LP/BP	8-12	0,40	9.1		-20,00	360° (5-Bit)	-12,6	4,86	1,00
SU RFIC [50]	250 nm SiGe	Passive HP/LP/BP	9.2-10.8	0.16	11.5	1.8	14±1	360° (4- Bit)	1	1.84	0

Table 5: Comparison table for phase shifters using distributed active switches.

Ref	Process	Design technique	Freq GHz	Frac. BW	Ph. Err. (°)	Gain Err. (dB)	Gain (dB)	Phase range	OP1dB (dBm)	Area mm2
[47]	180 nm CMOS	Distributed Active switches	11,6-12,6	0,08	5,5	1,2	3,5	360° (4 Bit)	-5,5	1,7
SU RFIC [48]	250 nm SiGe	Distributed Active switches	9,5-10,5	0,1	5,8	0,3	7	360° (4 Bit)	-8	2,2

2.2. Active Phase Shifters: Vector Sum Methodology

Recently, respectable amount of research has been done on active phase shifter topologies utilizing vector-sum method [51], [52], [53]. Remarkable phase resolution and higher gain can be achieved in a smaller area in vector-sum architectures in comparison with passive PS. Thus, in contemporary phased-arrays vector-sum architecture is a prominent competitor to be realized.

Fundamental idea of vector-sum method is generation of the desired phase by combining the amplitude modulated reference in-phase and quadrature vectors, [51], [52], [53]. The block diagram of a recently implemented (at SU-RFIC laboratories) phase shifter is presented in Fig. 6. The first step is the generation of in-phase (***I***) and quadrature (***Q***) reference vectors. Amplitude equivalence, and accuracy in 90° phase difference in a wide bandwidth are critical objectives for this step. For this reason, an active Balun and a polyphase filter type ***I/Q*** network are utilized. The second step is amplification or attenuation of these vectors. For this purpose, digitally controlled variable gain amplifiers (VGA) are used. A decoder based control circuit is used to set amplitude weightings of the reference vectors for the desired phase state. Finally, the sum of the reference vectors provides the phase shift. Assuming the input signal of the Vector SUM circuit is,

$$RF_{in} = \cos\left(\omega t + \phi\right) \tag{6}$$

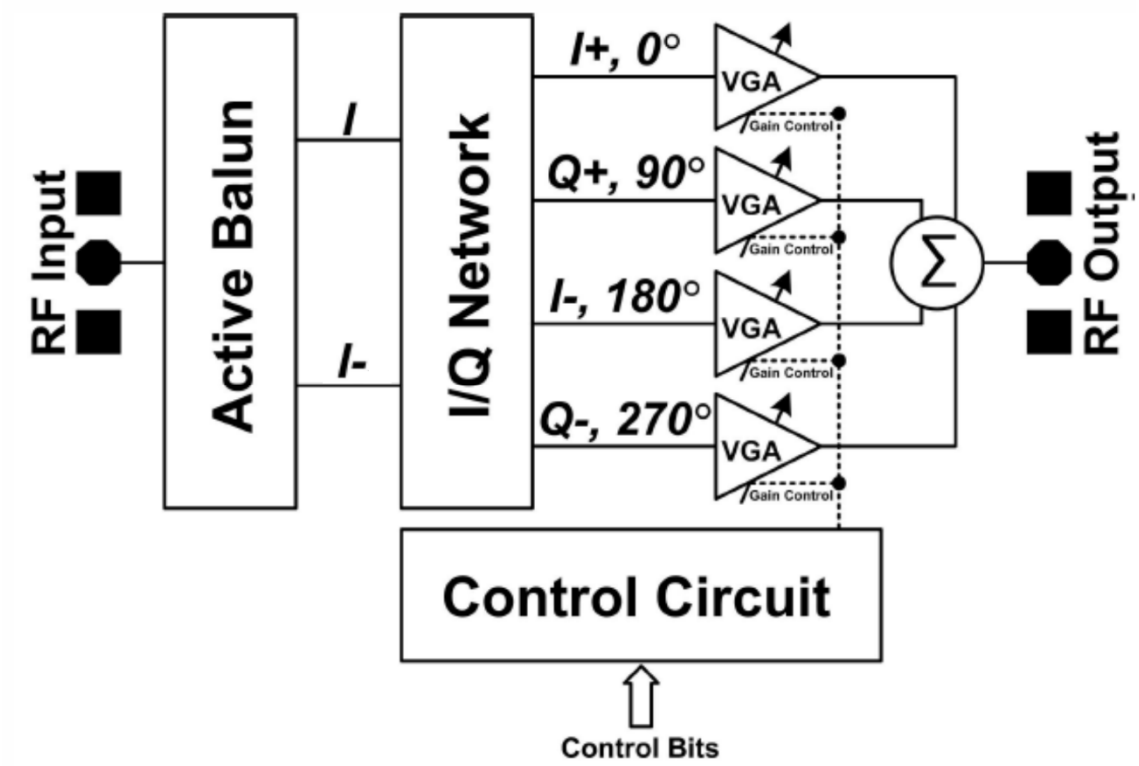


Fig. 6: Block diagram of vector sum type phase shifter.

Corresponding signals at the output of the active BALUN will be,

$$I = \cos(\omega t + \phi) \text{ and } I^{-} = \cos(\omega t + \phi + 180°) \tag{7}$$

For the input signal (6), corresponding output signals of the I/Q network will be,

$$I^{+} = \cos(\omega t + \phi) \tag{8}$$

$$Q^{+} = \cos(\omega t + \phi + 90°) \tag{9}$$

$$I^{-} = \cos(\omega t + \phi + 180°) \tag{10}$$

$$Q^{-} = \cos(\omega t + \phi + 270°) \tag{11}$$

Four VGA will be used with corresponding gains as G_1, G_2, G_3 and G_4. Finally, the outputs of VGAs are connected to a common load and reference vectors are added in current domain. The output of vector sum circuit will be,

$$RF_{out} = G_1 \cos(\omega t + \phi) + G_2 \cos(\omega t + \phi + 90) + G_3 \cos(\omega t + \phi + 180) + G_4 \cos(\omega t + \phi + 270) \tag{12}$$

For desired phase, one of in-phase vectors (I^+ or I^-) and one of Quadrature (Q^+ or Q^-) are amplified and added, the other vectors will be attenuated. For instance, in order to acquire a phase shift between 0° and 90°, A_3 and A_4 must be negligible in comparison with A_1, and A_2. With these assumptions,

$$RF_{out} = G_1 \cos(\omega t + \phi) + G_2 \cos(\omega t + \phi + 90) \tag{13}$$

$$= \mathrm{Re}\left\{ e^{i\omega t+\phi} \left(G_1 + G_2 e^{i90} \right) \right\} = \mathrm{Re}\left\{ e^{i\omega t+\phi} \left(G_1 + G_2 i \right) \right\} \tag{14}$$

$$= \mathrm{Re}\left\{ e^{i\omega t+\phi} \left(\sqrt{G_1^2 + G_2^2} \right) e^{i \arctan\left(\frac{G_2}{G_1}\right)} \right\} \tag{15}$$

$$= \sqrt{G_1^2 + G_2^2} \cos\left(\omega t + \phi + \arctan\left(\frac{G_2}{G_1} \right) \right) \tag{16}$$

The gain of the vector sum circuit is,

$$K = \sqrt{G_{1,3}^2 + G_{2,4}^2} \tag{17}$$

Acquired phase shift is, $\alpha_{desired}$,

$$\alpha_{desired} = \angle \arctan\left(\frac{G_{2,4}}{G_{1,3}} \right) = \angle \arctan\left(\frac{G_Q}{G_I} \right) \tag{18}$$

Expression (18) shows that, in ideal case, the acquired phase difference is inverse tangent function of the ratio of amplitudes of quadrature and in-phase vectors. For instance, if the desired signal is 37° the ratio between quadrature and in-phase vectors must be 3/4. Expression (18) also shows that, for a vector sum based phase shifter, it is not necessary to measure the phase. Measuring size of the vectors is enough to estimate acquired phase difference.

Table 6 shows the performance summary of the state of the art phase shifters. For switched line PS [36] [37] [38], phase resolution is very low (up to 2 bits), fractional bandwidth is very limited (0,12-0,17) and loss is very high (3-4.5 dB per section). Loaded

line PS, for instance [39], have very low phase resolution, low fractional bandwidth, and low phase range. Reflection type PS, [40] [41] [42], have analog control, therefore DAC requirement and calibration problems are important. In addition, phase range is also limited. On the other hand, PS using distributed active switches do not have insertion loss. However, other performance parameters such as phase resolution, fractional bandwidth, phase error, and gain error, are much lower than its alternatives. If the objective is the design of a phase shifter achieving high performance in terms of fractional bandwidth, phase resolution, phase range, and phase error, there are two important alternatives: Switched filter type and Vector sum type. Switch filter type PS do not have power consumption; however, they have significant insertion loss (up to 20 dB) which has to be compensated with an amplifier. In addition, for a high phase resolution objective such as 7 bit, all of the 7 phase shifter stages have to be cascaded. Therefore, insertion loss and area consumption is directly related with phase resolution. Moreover, fractional

Table 6: Comparison table of state of the art phase shifters

Ref	Process	Design technique	Freq. GHz	Frac. BW	Ph. Err. (°)	Gain Err. (dB)	Gain (dB)	Phase range	OP1dB (dBm)	Area mm^2	Pow. mW
[44]	180nm CMOS	HP/LP/BP	7 -12	0,67	7,50	1,10	-15,70	360° (6 Bit)	N/A	1,900	0,00
[46]	130 nm SiGe	Passive HP/LP/BP	8-12	0,40	9.1		-20,00	360° (5 Bit)	-12,6	4,86	1,00
[47]	180 nm CMOS	Distributed Active switches	11,6-12,6	0,08	5,5	1,2	3,5	360° (4 Bit)	-5,5	1,7	26,6
[51]	180 nm SiGe	Vector Sum	6-18	1,00	5.6	1	18±1.5 **	360° (5 Bit)	-20	0.18	62**
[52]	130 nm SOI	Vector Sum	23-23,4	0,06	2,8	0,5	14*	360° (6 Bit)	-15,00	0.87	45*
[53]	65 nm CMOS	Vector Sum	50-66	0,28	11	1,7	-6	360° (4Bit)	-2,00	1,60	30,00
SU RFIC [54]	250 nm SiGe	Vector Sum	9 - 12	0,285	5	2	-5,00	360° (6Bit)	-11,00	1,65	110,00

bandwidth of this type of PS is also limited. As a result, vector sum type PS has highest phase resolution (higher than 6-bit design is possible), lowest insertion loss (around 5-6 dB [53]), highest fractional bandwidth (around 1 at [51]), low area (less than 1.7 mm^2) and reasonable power consumption. OP1dB performance of this type of PS is the weak point and needs to be improved.

2.3.Vector Sum Design Challenges

In the above sections, it is shown that the highest phase resolution, the lowest insertion loss, the highest fractional bandwidth can be achieved with vector sum type phase shifters. However, this technique still needs improvements. The state of the art vector sum in literature, as shown in Table 6, can achieve up to 6-bit phase shift, in a limited fractional bandwidth. This literature search also shows that, as operation bandwidth increase, phase error increase and phase resolution significantly decreases. In addition, OP1dB compression points of this type of PS are much lower than their alternatives. There are two important reasons of these limitations; I - Q nonideality and VGA nonideality.

2.3.1 I-Q Nonideality

Generation of in-phase and quadrature reference vectors is the first step of phase shift operation, therefore, it has a significant importance on performance of phase shifter. Without any phase or amplitude correction circuit, phase error and gain error of this stage is reflected to output rms phase and amplitude error [53]. Assuming G_0 is a constant, representing the gain of the phase shifter, and α is desired phase shift, as previously derived in (18),

$$\alpha_{desired} = \angle \arctan\left(\frac{G_Q}{G_I}\right) \Rightarrow \frac{G_Q}{G_I} = \frac{\sin\alpha}{\cos\alpha} \tag{19}$$

$$G_Q = \sin\alpha G_0 \tag{20}$$

$$G_I = \cos\alpha G_0 \tag{21}$$

Output of the vector sum circuit can be expressed as,

$$V_{out} = \left(G_I + jG_Q\right)V_{in} \tag{22}$$

Assuming ε is the gain error, β is the phase error at Q path, output of the vector sum circuit will be:

$$V_{out} = \left[G_I + G_Q\left(1-\varepsilon\right)e^{j\left(\frac{\pi}{2}-\beta\right)}\right]V_{in} \approx \left[\left(G_I + \beta G_Q\right) + G_Q\left(1-\varepsilon\right)\right]V_{in}$$
$$= \left[\cos(\alpha) + \beta\sin(\alpha) + j\sin(\alpha)\left(1-\varepsilon\right)\right]G_0 V_{in} \tag{23}$$

Achieved phase shift, $\alpha_{achieved}$ will be

$$\alpha_{achieved} = \arctan\frac{\sin\left(\alpha\right)\left(1-\varepsilon\right)}{\cos\left(\alpha\right)+\beta\sin\left(\alpha\right)} \tag{24}$$

Therefore, the phase error, Δα will be,

$$\Delta\alpha = \alpha_{achieved} - \alpha_{desired} = \arctan\frac{\sin\left(\alpha\right)\left(1-\varepsilon\right)}{\cos\left(\alpha\right)+\beta\sin\left(\alpha\right)} - \arctan\left(\frac{G_Q}{G_I}\right) \tag{25}$$

$$= \arctan\left[\frac{-\frac{\beta}{2}-\frac{\varepsilon}{2}\sin\left(2\alpha\right)+\frac{\beta}{2}\cos\left(2\alpha\right)}{1-\frac{\varepsilon}{2}+\frac{\beta}{2}\sin\left(2\alpha\right)+\frac{\beta}{2}\cos\left(2\alpha\right)}\right] \tag{26}$$

$$\approx -\frac{\beta}{2}-\frac{\varepsilon}{2}\sin\left(2\alpha\right)+\frac{\beta}{2}\cos\left(2\alpha\right) \tag{27}$$

The RMS phase error will be

$$\Delta\alpha_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\alpha_{achieved}-\alpha_{desired}\right)^2 d\alpha} \approx \sqrt{\frac{3}{8}\beta^2+\frac{1}{8}\varepsilon^2} \tag{28}$$

The gain of the phase shifter will be $G_{achieved}$,

$$G_{achieved} = G_0\sqrt{\left(\cos(\alpha)+\beta\sin(\alpha)\right)^2+\sin^2(\alpha)(1-\varepsilon)^2} \approx G_0\sqrt{(1-\varepsilon)+\beta\sin(2\alpha)+\varepsilon\cos(2\alpha)} \quad (29)$$

RMS gain error, $\Delta G_{RMS,dB}$ will be,

$$\Delta G_{RMS,dB} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(G_{achieved,dB}-G_{0,dB}\right)^2 d\alpha} \approx 8.7\sqrt{\frac{1}{8}\beta^2+\frac{3}{8}\varepsilon^2} \quad (30)$$

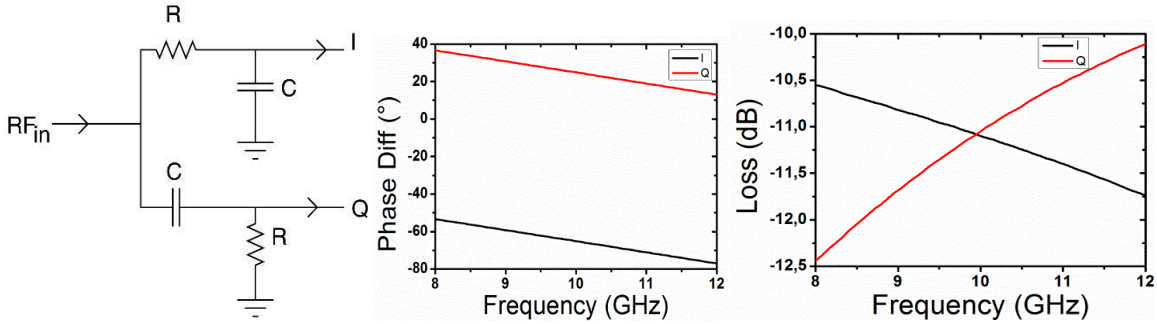
In order to design a 4-bit phase shifter with less than 11.25° phase and 1.7 dB amplitude errors, using (28) and (30) it can be calculated that $\beta < 0.28$ (equivalent to 16°) and $\varepsilon <$ 0.28 (equivalent to 2.8 dB) are required. In other words, phase error must be smaller than 16° for the angle between I and Q reference vectors, and amplitude mismatch must be smaller than 2.8 dB for I and Q amplitudes, [53]. Similarly, for a 6-bit phase shifter with less than 2.8° phase and 0.4 dB amplitude errors, I – Q generator can have maximum 4° phase and 0.6 dB amplitude errors.

Four quadrature generation techniques can be implemented on PS; Transmission line based quadrature generator (TLQG), RC-CR network, RC-polyphase filter (RCPPF) and LC resonance based quadrature generator (LCQAF).

TLQG is quadrature generation technique that shifts the phase of one of the two signal paths by $\frac{\pi}{2}$ with using a transmission line, hence its bandwidth is very limited. In [53], 9° phase error is obtained in 20% fractional bandwidth. Therefore, it is not very useful for the systems targeting 40% or more fractional bandwidth and high phase resolution.

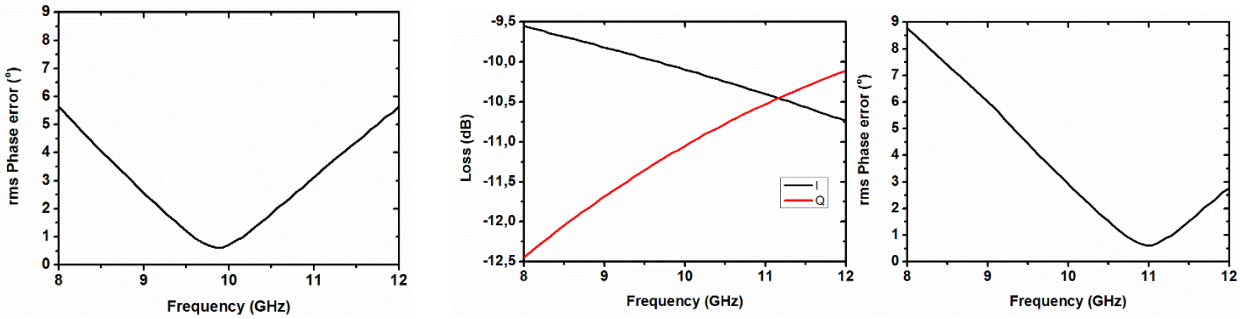
In RC-CR (R-resistor, C-capacitor) network the phase of two signal paths are shifted by $+\frac{\pi}{4}$ and $-\frac{\pi}{4}$ respectively [55]. As shown in Fig. 7a, a low-pass filter and a high-pass RC filter are placed in two signal paths. With this technique 90° phase difference between I and Q vectors is achieved for all frequencies as shown in Fig. 7b [56]. However, the amplitudes of the reference vectors are equal only at the corner frequency of the RC filter, that is $\omega = \frac{1}{RC}$, as shown in Fig. 7c. In addition, the corner frequency varies due to the

variation of R and C with temperature and process; it is thus impossible to get a robust quadrature signal in CMOS or BiCMOS technologies by using RCCR networks. Moreover, for both of two quadrature outputs, a good matching performance can only be achieved on the corner frequency of this RC-CR network with a very narrow band. For that reason, this technique is not suitable for wideband operation. With using this technique [56] achieved less than 5.6 ° phase error in 8-12 GHz band (in simulation level), as shown in Fig. 8a. However, the correlation between I-Q imbalance (shown in Fig. 7c) and rms phase error (shown in Fig. 8a) is very critical. In order to investigate this correlation, an ideal amplifier with 1dB gain is added to I path. With this modification, minimum rms phase error frequency (ω_1) is shifted from 10 GHz to 11 GHz, as shown in Fig. 8c. This simulation shows that, if the gain imbalance between I and Q reference vectors is minimized, rms phase error is also minimized. In addition, through controlling R or C to shift $\omega_1 = \frac{1}{RC}$, rms phase error performance of a phase shifter can also be controlled.



(a) (b) (c)

Fig. 7: a) RC-CR network b) phase difference c) S21 variation of I and Q.



(a) (b) (c)

Fig. 8: a) rms phase error with using an RC-CR network at [56] b) simulation result for S21 variation after 1 dB gain improvement at I path, c) rms phase error after this improvement.

In order to generate quadrature signals without amplitude imbalance in radio, Polyphase filters (PPFs) were established by Gingell [57] in 1971. Integrated PPFs were utilized first time as a valuable RF quadrature generation technique in CMOS technology by Steyaert [58] in 1994. The topology of PPF is presented in Fig. 9, and it is formed as cascaded 'n'stages of RC networks [58]. Each stage consists of four equal resistors and four equal capacitors. Different size of resistors and capacitors are selected for each stage. In Fig. 9, the differential inputs are presented as in^+ and in^-, differential outputs of the I path are presented as I^+ and I^-, and differential outputs of Q path are presented as Q^+ and Q^-. The basis of PPFs is a stated as 'stagger tuning' technique [58], which is the utilization of two or more cascaded stages of RC-CR networks minimizes the amplitude imbalance and enhances the bandwidth of the quadrature signal generated. The advantages of RCPPF over conventional quadrature generation techniques are [59]:

- Due to utilization of only resistors and capacitors, the design is simple.
- Due to utilization of stagger-tuning technique, process variation tolerance is improved and other sophisticated tuning circuitries are left out. °
- They are strongly adapted for wideband quadrature signal generation.

A two stage RCPPF is embedded in design of Vector sum in SU-RFIC [54] as a replacement of RC-CR network. In this 0.1dB amplitude error, and 1° phase error is observed at quadrature signals, rms phase error of the phase shifter is reduced from 5.6° (presented at [56]) to 1.4° in simulation level.
Although RCPPFs are strongly adapted as RF quadrature signal generator, they have the consecutive disadvantages:

- RC-PPFs have insertion loss of 3 dB/stage (considering parasitic R and C in layout of RC-PPF this insertion loss per stage can be much higher). For high accuracy, multiple cascaded stage is used, and additional power hungry amplifiers are required for compensation of this loss.
- If RC-PPF s are utilized in signal path, they decrease NF performance of the receiver.
- PS are generally used after LNA due to their high NF, therefore, insertion loss of RC-PPF deteriorates IP1dB and IIP3 performance of receiver.

L–C resonance technique is important method for generation of Quadrature signals with lower insertion loss which is shown in Fig. 10a for the single-ended and differential versions [60] (where $R = \sqrt{L/C}$ nad $Q = \frac{\sqrt{\frac{L}{C}}}{R} = 1$). In comparison with a second order RC-PPF, L-C based quadrature all pass filter (LC-QAF) has 6 dB higher voltage gain and similar phase error performance. However, if the loading effect is considered, where the loading capacitance can be comparable with C (at Fig. 10) which causes significant I/Q amplitude and phase error. Minimizing this amplitude and phase error is possible with inserting a serial resistances (R_S) to C and L, which causes 6 dB loss. With using

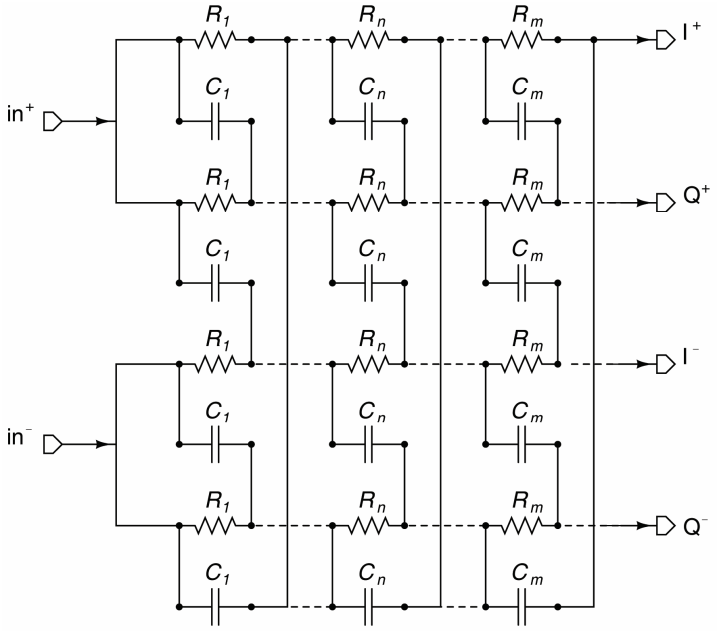


Fig. 9: Polyphase filter as a quadrature generator.

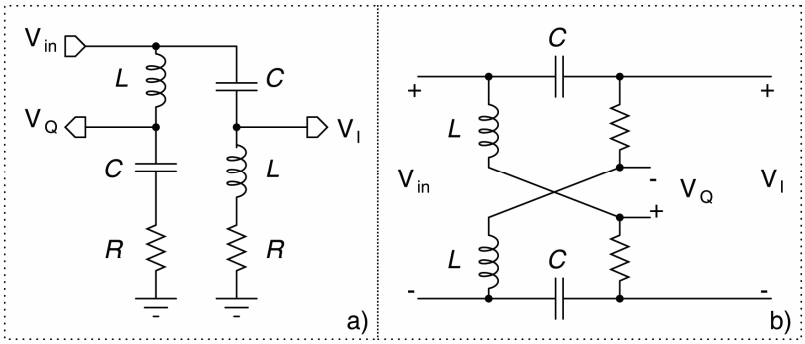


Fig. 10: L–C resonance-based quadrature all pass filters (LCQAF), a)Single ended, b) differential.

LCQAF loaded with R_S (R_S/R=0.67), quadrature signals are generated (including the loading effect) with less than 9.5° phase error and 0.5 dB amplitude error in 55-78.5 GHz band allowing the design of 5-bit PS [60]. However, this performance is not sufficient in design of PS with phase resolution of 6 bit or higher.

2.3.2 VGA Nonideality

After generation of reference I and Q vectors, Variable gain amplifiers (VGA) are used for weighting and summation of these vectors. In design of VGAs, first of all, the variation of input return loss of VGA for different gain states must be minimal in order to obtain phase shift which can be anticipated with (12). Secondly, gain control range (GCR) of VGA must be sufficient for synthesizing the minimum phase step ($\alpha_{min}=360/2^n$) of *n* bit phase shifter. If there is an amplitude mismatch, ε, between I and Q signals,

$$\left|\mathrm{I}_{max}\right| = \left|Q_{\max}\right| + \varepsilon \tag{31}$$

In order to generate same phase difference between 0° to α_{min}, and to 90° to 90+ α_{min} to (18) can be re-arranged as;

$$\frac{\left|\mathrm{I}_{max}\right|}{\left|Q_{\min}\right|} = \frac{\left|Q_{\max}\right|}{\left|\mathrm{I}_{\min}\right|} = \frac{1}{\tan\left(\alpha_{\min}\right)} \tag{32}$$

$$\left|I_{\min}\right| = \left|Q_{\min}\right|\frac{\left|Q_{\max}\right|}{\left|I_{max}\right|} = \left|Q_{\min}\right|\frac{\left|Q_{\max}\right|}{\left|Q_{\max}\right| + \varepsilon} \tag{33}$$

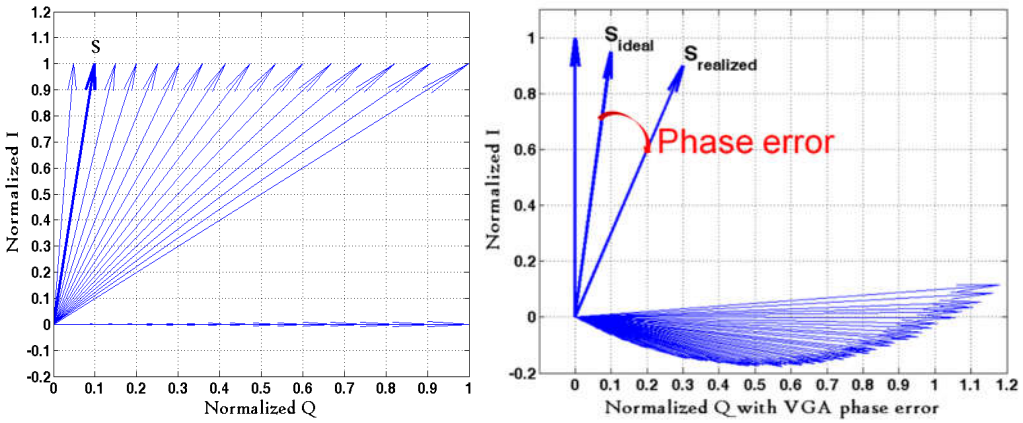
$$GCR = 20\log\left(\frac{\left|I\right|_{max}}{\left|I\right|_{\min}}\right) = 20\log\left(\frac{1}{\tan\left(\alpha_{\min}\right)}\right) + 20\log\left(\frac{\left|Q_{\max}\right| + \varepsilon}{\left|Q_{\max}\right|}\right) \tag{34}$$

With using expression (34), it can be calculated that, in order to design a 7-bit phase shifter with 2.8° of minimum phase step, and 3 dB of gain mismatch between I and Q signals, 29.2 dB of gain control range is required. Moreover, maximum phase variation ($\Delta\alpha_{VGA}$) of VGA between its highest and lowest gain states must be minimum. $\Delta\alpha_{VGA}$ is a significant design criterion which creates significant phase error at output as depicted at Fig. 11. In order to synthesize an example *S* vector at output of PS, amplitude of Q must be 1/10 of I vector as represented at Fig. 11.a. However, modulating the amplitude

of Q vector without adding phase error is not possible as represented at Fig. 11.b, where VGA phase error is represented at x-axis. Furthermore, considering the requirement of four VGAs in a PS, achieving gain control in a single stage is very important for minimization of area and power consumption. In addition, summation function can also be achieved in current domain, at VGA stage. The state of the art VGA are based on cascode configuration due to its high isolation between input and output. For gain control, two important methodologies come forward; *bias voltage adjustment* [61], [62], [63], and *current steering* [64], [65], [66].

In *bias voltage adjustment* method, base (or gate) voltage of driver transistor (common emitter) or cascoded (common base) transistor is adjusted in order to control gm and gain of the VGA. In order to compensate phase variation, capacitor at base (or gate) of the cascoded transistor is minimized [61] or a varactor is connected to this node [62]. This method is simple to implement, however, bias voltage and current of driver transistor changes (for some gain states operation region of transistor has to change) for each gain state. Therefore, parasitic capacitances and input return loss of the amplifier changes significantly, and for this reason phase error performance of PS degrades. Performance of the state of the art VGA are summarized at Table 7. Although GCR is lower than 15dB, a significantly high phase variation (5-8.9°) is measured at [62] and [63].

In *current steering* method, in contrast with *bias voltage adjustment method*, bias voltage and current of driver transistor remains constant and the gain of VGA is controlled with



a) b)

Fig. 11: a) Vector sum with ideal vectors, b) Vector sum including VGA phase error. VGA phase error in this figure is imported from post layout simulations.

a variable current source which is connected to collector (or drain) node of driver transistor. This variable current source modulates current of cascoded transistor and controls gm of to control gain. Input return loss of the amplifier remains unchanged. Higher GCR (15.5 dB) can be achieved with lower phase variation (6.6 °) [64]. At SU-RFIC laboratories this type of VGA is utilized at PS, and post layout simulations show that if 29.5 dB of GCR is aimed, phase variations reach to 31°.

Highest GCR and lowest phase variation performance is achieved in topologies with two or more stage cascaded VGA [65] - [66]. In first stage current steering method is applied, in second stage bias voltage adjustment method is applied. First stage and second stage have opposite trend slope of phase performance; hence the phase compensation is achieved by combination of these two techniques. 33 dB gain control range with 7° phase variation performance is significant, however this type of VGA cannot be used in PS because of following the reasons. First, for each VGA one separate DAC is required for bias voltage adjustments, which increase complexity of the system. Secondly, considering the requirement of VGA for a PS, as number of cascaded stages increase, area and power consumption also significantly increase.

Table 7: Performance summary of the state of the art VGAs

Ref	GCR (dB)	$\Delta\theta_{VGA}$ (°)	OP1dB (dBm)	P(mW)	tech
[61]	6.20	1.86	-4.00	31.20	bias adjustment. optimized cascode gate termination
[62]	13.00	5.00	N/A	240	bias adjustment. cascode gate varactor controlled
[63]	14.50	8.90	-7.00	25.70	bias adjustment. optimized cascode gate termination
[64]	15.50	6.60	4.00	36.00	current steering optimized gate termination
[65]	33.00	7.00	-4.00	10.90	three stage cascaded - bias adjustment and current steering.
[66]	22.00	7.50	N/A		double stage cascaded VGAs with bias adjusting and current steering

3. SELF GENERATED LOOK UP TABLE for PHASE CORRECTION in VECTOR SUM METHODOLOGY

Before the introduction of proposed design method, it is useful to restate some important remarks from the previous section, in which the advantages and challenges of vector sum technique are explained in detail.

- Vector sum type PS has the highest phase resolution, the lowest insertion loss, the highest fractional bandwidth, the lowest area and acceptable power consumption.
- However, it is not possible to create I and Q vectors without amplitude errors and phase errors in a wideband operation.
- Variable gain amplifiers are utilized to control amplitude of the vectors, and they cause additional phase error.
- I/Q vector generation circuits and amplitude control circuits have less tolerance on process and temperature variations.

Remarks and problems listed above are the main motivation for this thesis. The aim is to lower the phase error of PS, and increase phase resolution. To be more specific, the intention is to introduce a self-calibration circuit to minimize phase error resulting from I/Q imbalance, I/Q phase inaccuracy and phase insertion of VGA.

Assuming the I vector (which will be the reference of the circuit) is

$$I = |I| \cos(\omega t) \tag{35}$$

Due to I/Q phase inaccuracy and phase insertion of VGA, there will be a phase error, β. The amplitude error due to process variations and model inaccuracies will be included to the amplitude of the |Q|, therefore, the quadrature vector will be,

$$Q = |Q|\cos(\omega t + 90 + \beta) \tag{36}$$

The vector-sum circuit will provide the output as,

$$S = |S|\cos(\omega t + \alpha) \tag{37}$$

These signals can be represented using the vectors as demonstrated in Fig. 12a. Using the cosine formula in basic geometry, we know that

$$|Q|^2 = |S|^2 + |I|^2 - 2|I||S|\cos(\alpha) \tag{38}$$

$$\alpha = \arccos\frac{|S|^2 + |I|^2 - |Q|^2}{2|I||S|} \tag{39}$$

Therefore, (39) shows that the phase shift acquired in vector sum circuit can be calculated using the amplitude information of I, Q and S vectors. On the other hand, (12) can be reorganized to show the output of the Vector-Sum circuit as,

$$RF_{out} = G_1 I^+ + G_2 Q^+ + G_3 I^- + G_4 Q^- \tag{40}$$

The digitally controlled variable gain amplifiers in vector sum circuit determines G_1-G_4. These variable gain amplifiers can be controlled in such a way that; the output of vector

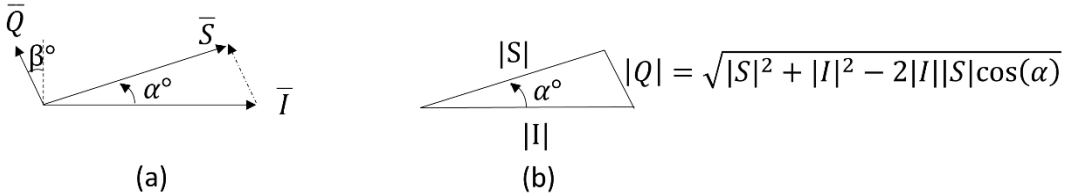


Fig. 12: a) Vector representation, b) Geometric approximation

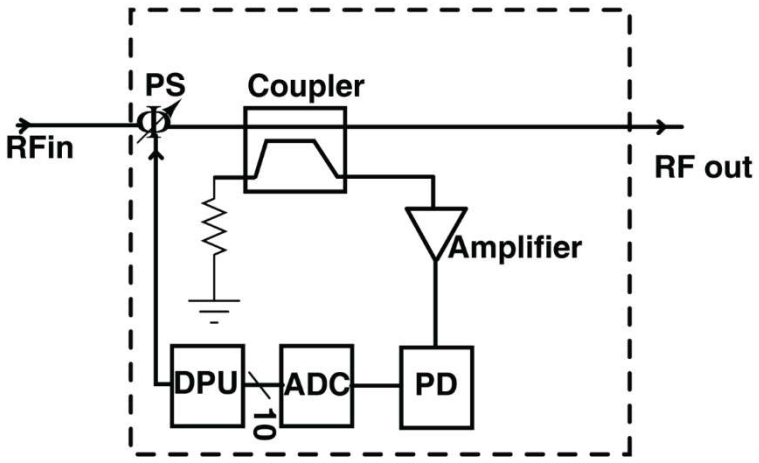


Fig. 13: Block diagram of the proposed self-calibration circuit.

sum circuit can be one of the reference vectors, or combination of two vectors. For instance, if G2, G3, and G4 are set to zero, the output of the vector sum circuit will be, $RF_{out} = G_1 I^+$.

Proposed idea is to design a calibration circuit which measures all possible amplitudes of I, Q and S vectors and estimates the relative phase shift for these vectors. A portion of these (I, Q) vector pairs will provide S vectors that have accurate relative phase shift. Digital control data of variable gain amplifiers in vector sum circuit (which are utilized in generation of accurate S vectors) will be recorded in a LUT. When the calibration is ended, this LUT will be used in control of the phase shifter.

The block diagram of the proposed calibration circuit is demonstrated in Fig. 13. A Power detector (PD) will be used for measurement of I and Q vectors. Output of PD will be converted to digital for calculations. A digital processing unit (DPU) with a small memory will be used for calculations and generation of LUT. Calibration module will be cascaded to a phase shifter, which will be used in a T/R module as represented at Fig. 14. Transmitting - receiving path and calibration path are connected with a coupler. When the calibration mode is on, an input signal with a certain power (for instance -12 dBm) at target frequency (for instance 10 GHz) will be requested for the input of the phase shifter.

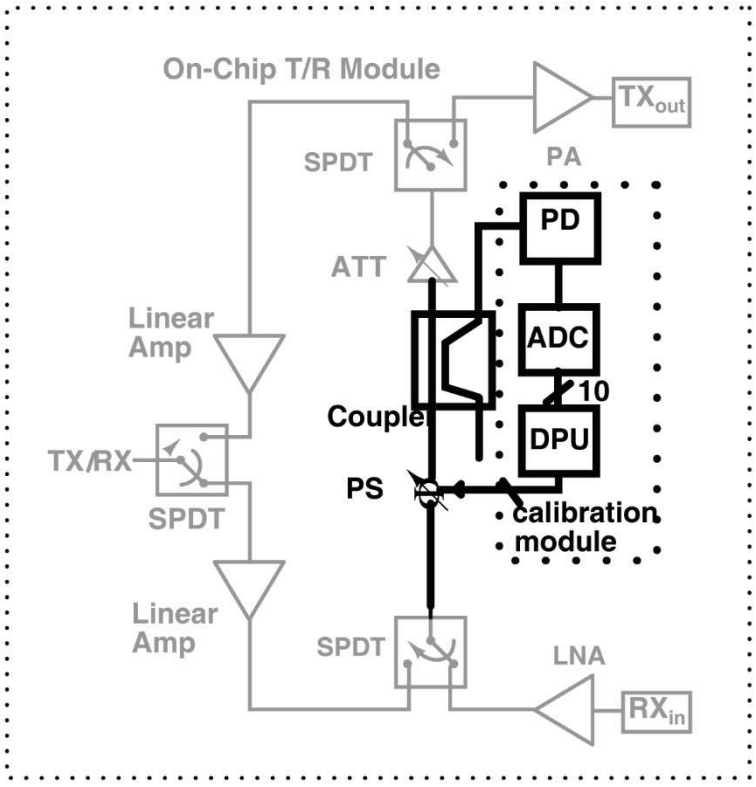


Fig. 14: Integration of the calibration module to T/R module.

3.1 Proposed Self-Calibration Algorithm

The first step of the algorithm is to control the phase shifter to generate the minimum amplitude. This means, a control signal will be send to all of the VGAs and they will be turned off. In order to generate minimum amplitude, G_1-G_4 must be as low as possible. Assuming current steering type VGA are utilized, all of the switches at steered currents must be on state in order to minimize the gain. For a phase shifter with four 6 bit VGAs, the control signal will be 111111-111111-111111-111111 (first 111111 is for I^+, second 111111 is for I^-, third 111111 is for Q^+ and fourth 111111 is for Q^-). This will be the reference state, and the other vector sizes will be calculated based on this reference. The power detector measures the output of the PS, and for this reference state maximum possible voltage will be read at the output of power detector, and the ADC converts this data to digital. The DPU records this data at its register bank.

The second step of the calibration algorithm, is the measurement of vector magnitudes for I^+, I^-, Q^+ and Q^- states and recording this data to register arrays. This will be possible

through sending a control sequence to the VGA of corresponding vector (for instance I), which sweeps amplification ratio of target vector (G_1) while keeping the amplitude of other vectors (G_2-G_4) at minimum. Assuming VGA is 6 bit, 64 different control signals will be applied in a sequence. For instance, the control signal sequence for sweeping the I vector will be ([0:1:63] - 111111-111111-111111).

The third step of the calibration algorithm is the measurement of *Sum* vectors for all possible vector pairs of *I* and *Q*, and recording the data in corresponding register arrays. In the first version of the code, one of the vectors are kept at maximum and the others are swept from minimum to maximum. For instance, the control signal sequence for sweeping I^+ vector with a fixed maximum Q+ vector will be ([0:1:63] - 111111-000000-111111).

After finishing all of the measurements, calculation sequence starts. For each desired angle, $\alpha_{desired}$, the code takes a reference vector, and seeks an orthogonal vector such that, the angle between the reference vector and sum vector ($S_{\alpha desired}$) is $\alpha_{desired}$. In other words, the code has the information of magnitude of reference vector and the information of desired angle. The code searches the optimum orthogonal vector and corresponding Sum vector. For instance, if $\alpha_{desired}$ is between 0-45°, the reference vector is I, and the orthogonal vector will be Q. The code will have the information of I_{max} and $\alpha_{desired}$, and it searches the optimum Q vector, Q_{opt}, from all possible magnitudes of the Q vectors, which provides the S_{opt} vector. (25) can be reorganized such that,

$$\left|Q_{opt}\right|^2 = \left|S_{opt}\right|^2 + \left|I_{ref}\right|^2 - 2\left|I_{ref}\right|\left|S_{\alpha_{desired}}\right|\cos\left(\alpha_{desired}\right) \tag{41}$$

Implementation of inverse trigonometric function of (26) in a digital circuit is unnecessarily complicated, therefore rather than using (26) an error function is defined. For a 6 bit VGA, there will be 64 different Q vectors, all of these vectors cause error for target $\alpha_{desired}$, $Error_{phase}$ as,

$$Error_{phase} = \left|S\right|^2 + \left|I_{ref}\right|^2 - 2\left|I_{ref}\right|\left|S\right|\cos\left(\alpha_{desired}\right) - \left|Q\right|^2 \tag{42}$$

Optimum orthogonal vector, is the vector which creates minimum $Error_{phase}$. Optimum vector pair, is the pair of the vectors, consisting of optimum vector and reference vector. For each desired $\alpha_{desired}$, $\cos(\alpha_{desired})$ values are included as constants in the code of DPU. Floating point multiplication techniques are applied for this calculation. The objective of the code is to find the optimum vector pair for each angle, and to record the corresponding control signal data in another register array which forms the LUT.

When the calibration sequence is finished, final form of the LUT will be generated. This LUT provides digital control signals of VGA for each phase state. For instance, for a 7-bit phase shifter, in order to create a phase shift of 8.4°, user enters 0000011 and output of the LUT will be 000000-111111-110100 -111111 (this code means that, VGA of Q^+ is partially open, VGA of I^- and Q^- are completely closed, and VGA of I^+ is operating at maximum amplification). The summary of this algorithm is shown at Fig. 15. Measurement sequence will be completed in 768 cycles. The calculation sequence will be done in 64x128 cycles. Maximum measurement cycle can be as long as 1ms, and calculation cycle can be as long as 50ns; with these assumptions, the basic calibration can be finished in 768.4 ms. Considering that, the calibration is a onetime process, time consumption less than 1s is acceptable.

In conventional phase shifters, the LUT is generated from the data based on post layout simulations, and it cannot be changed after post layout simulations. On the other hand,

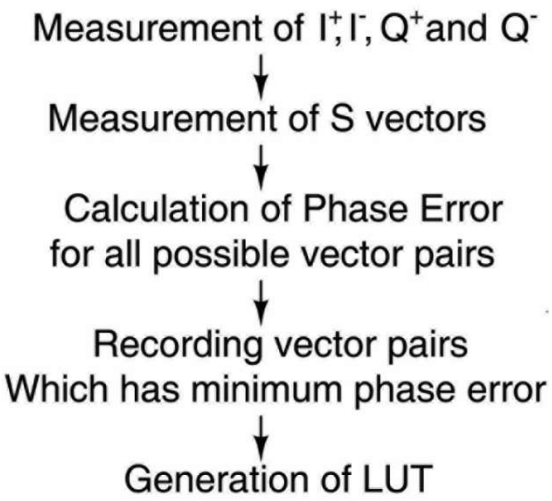


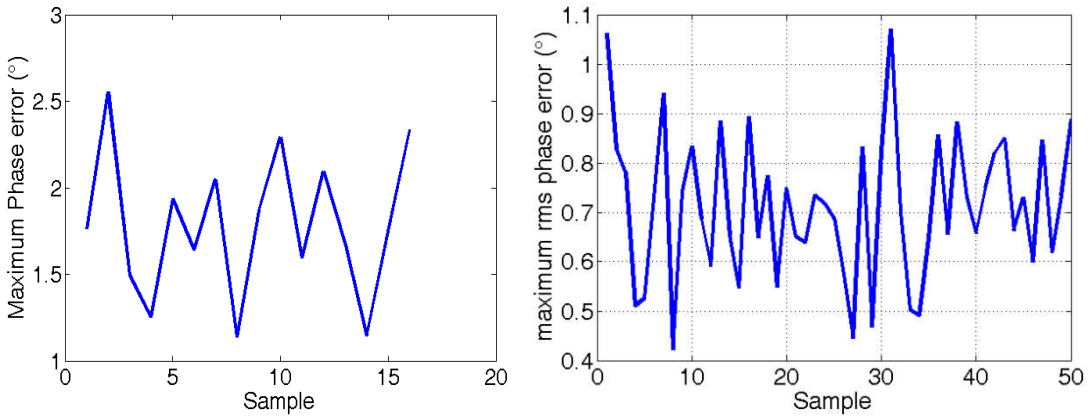
Fig. 15: Summary of proposed calibration algorithm.

the self-generated LUT is generated after fabrication, therefore it has more tolerance to process variations of I/Q generator and VGA. This performance enhancement can be explained with an example. For instance, 45° of relative phase shift is aimed, which requires equal amplitudes of ***I*** and ***Q*** vectors. In conventional LUT, VGAs will be set to symmetric amplification for I and Q vectors. Due to process variations or model inaccuracies (in I/Q generator or VGA) there can be 2 dB amplitude difference, which causes a significant phase error. With this new technique, the LUT will be generated based on on-chip measurements of I and Q vectors, therefore this 2 dB amplitude difference will be covered with asymmetric VGA control. In addition, due to process variations, phase error coming from VGA can be more than expected. This phase error will be observed at $Error_{phase}$ calculations at DPU, and a more proper amplitude set will be selected for vector pairs.

In addition, the self-generated LUT has more tolerance on temperature variations. LUT generated at 27 °C will be adapted to this temperature. If the temperature decreases to -10 °C, a new calibration cycle can be started and the LUT can be generated to be adopted to -10 °C.

In order to increase operation bandwidth of PS, an advanced calibration is proposed. In this technique, the calibration will be repeated for different frequencies. For instance, X-Band (8-12.5GHz) can be divided to four sections, and four LUT will be generated. For target operation frequency, appropriate LUT will be selected with 2-bit control signals. With these four LUT, RMS phase error will be minimum at the center of frequency sections. Frequency sections will not be wide, hence; phase error performance will not be degraded at corners of frequency sections. The drawback of this operation is the larger memory for LUTs and a more complex PS control.

In order to test the idea a Matlab script is written with the algorithm summarized at Fig. 15. This code can be found in the appendix. In this code, VGA phase error (which is exported from post layout simulations) is included. The code uses VGA phase error data to find optimum vector pairs for each target relative phase shift. In addition, each of the measurement sensitivity and quantization error are taken as 2% of the maximum vector magnitude. The results of these simulations are shown at Fig. 16. In 50 samples, maximum phase error is lower than 2.5° and rms phase error is lower than 1.1°, which is sufficient for 7-bit phase shifter design.



a) b)

Fig. 16: Results of the Simulation in Matlab. a) Maximum phase error b.) rms phase error.

3.2 Design Requirements of Building Blocks

Power detector has three important design specifications: Power range, settling time, and linearity.

1- Power range: In order to synthesize phase shift at minimum phase step, α_{min}, one of the reference vectors (for instance I) must be at the highest possible amplitude, and the other reference vector (Q) must be at the lowest possible amplitude. For this reason, power detector must be capable of measuring both of these vectors. Therefore, power ratio of minimum detectable input power and maximum input power defines the power range of the power detector. Maximum detectable signal amplitude is the maximum value of the Sum vector (S_{max}), which is sum of maximum I vector, I_{max}, and maximum Q vector, Q_{max}. Assuming I_{max} and Q_{max} are equal,

$$S_{max} = \sqrt{2}\, I_{max} \tag{43}$$

On the other hand, minimum input signal amplitude is the amplitude of minimum of I (or Q) vector, I_{min} which is related with minimum phase step. With re-arranging (18) and assuming I_{min} and Q_{min} are equal:

$$I_{min} = I_{max} \tan(\alpha_{min}) \tag{44}$$

Therefore, power range can be calculated as,

$$PowerRange(dB) = 20\log\left(\frac{P_{in\max}}{P_{in\min}}\right) = 20\log\left[\frac{\sqrt{2}\,\mathrm{I}_{max}}{\tan(\alpha_{\min})\,\mathrm{I}_{max}}\right] = 20\log\left[\frac{\sqrt{2}}{\tan(\alpha_{\min})}\right] \quad (45)$$

For a 7-bit phase shifter, α_{min} is 2.8°. Therefore, power range of the power detector must be higher than 29 dB.

2- Settling time: Calibration time is not a strict requirement for this system. One calibration cycle can be completed in 1 ms, therefore, 0.1 ms can be spared for settling time of Power detector.

3- Linearity: Power detector must have high linearity in high power ranges. The nonlinearity of PD results with measurement errors. Calculations in MATLAB with the code attached shows that, the residual error must be lower than 2% of S_{max} in order to have rms phase error less than 1.4°.

ADC design specifications

Calculations in MATLAB with the code in appendix show that, the quantization error must be lower than 2% of S_{max} in order to satisfy rms phase error requirement, which corresponds to a 6-bit requirement.

On the other hand, ADC must be capable of converting the smallest changes at output of power detector for high input power levels. When synthesizing minimum phase step, amplitude of the sum vector, $S_{\alpha min}$, will be very close to amplitude of one of reference vectors. Therefore, voltage change at output of power detector will be minimum, and ADC must be capable of sensing this voltage difference. Assuming I_{max} and Q_{max} are equal,

$$S_{\alpha_{\min}} = \sqrt{\mathrm{I}_{max}^2 + \left(\mathrm{I}_{max}\tan(\alpha_{\min})\right)^2} = \mathrm{I}_{max}\sqrt{1+\tan^2(\alpha_{\min})} \quad (46)$$

$$\Delta S_{\min} = S_{\alpha_{\min}} - \mathrm{I}_{max} = \mathrm{I}_{max}\left(\sqrt{1+\tan^2(\alpha_{\min})} - 1\right) \quad (47)$$

Assuming α_{min}=2.8 °, ΔS_{min} will be 0.0012 I_{max}. Therefore, LSB must be 1/1000 of ADC input voltage range. For this reason, a 10-bit ADC would be enough for this system.

Assuming that, the 10-bit ADC will convert analog to digital in 10 cycles, and the power detector can settle in 1 cycle. Hence, one measurement duration will be 11 clock period. During the calibration, maximum 16000 measurements will be applied. Therefore, in order to finalize all of the calibration in 100 ms, maximum clock period for the ADC is 0.56 μs.

4 IMPLEMENTATION of BUILDING BLOCKS

Proposed calibration module consists of RF building blocks (such Phase shifter, as coupler, LNA and Power detector) and baseband blocks such as (ADC and DPU). The block diagram of the system with block level specifications are demonstrated at Fig. 17. A phase shifter consisting of four 6 bit digitally controlled variable gain amplifiers is required to be calibrated. Total insertion loss must be lower than 7 dB, and OP1dB must be higher than -10 dBm. The loss of the coupler must be lower than 1.5 dB, which corresponds a coupling factor around -10 dB. The loss of the coupler will be compensated with a LNA, which must have at least 15 dB of gain. As previously

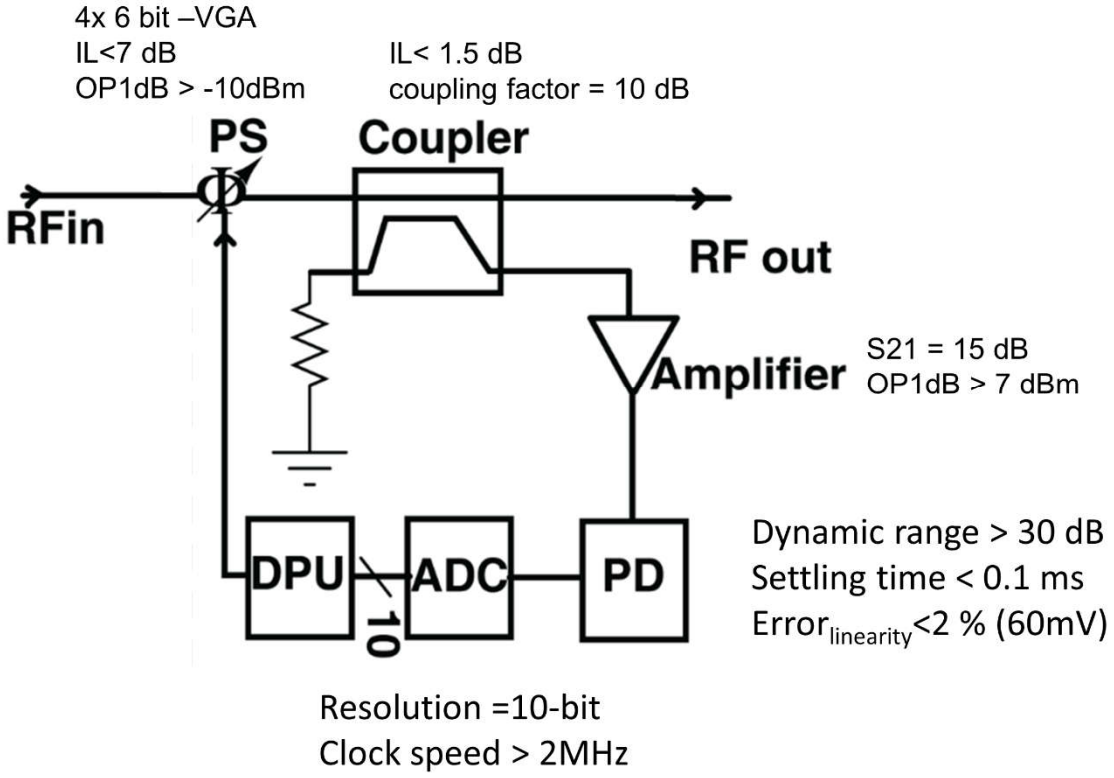


Fig. 17: Proposed system with block level specifications.

mentioned in chapter 3, LNA will be connected to a PD, which must have at least 30 dB of dynamic range, and the linearity error must be lower than 2% in this dynamic range. Reminding from chapter 3, the resolution of the ADC must be at least 10-Bit, and the clock speed must be higher than 2MHz. In his chapter, design of these circuits and measurement results are explained in detail.

4.1 Phase Shifter

A vector sum based phase shifter is designed for this thesis, which is previously published in wireless component letters [54]. PS consists of an active BALUN, a second order RC-Polyphase filter, four current steering type VGA, and a decoder which includes a static Look up table as shown in Fig. 6. The complete circuit schematic of vector sum type phase shifter is shown in Fig. 18.

4.1.1. Principle of the Operation and Circuit Design

Common-base (CB) – common-emitter (CE) based topology is chosen for active BALUN. The circuit is based on the 180° phase difference between CB configuration and CE configuration. Output of CB configuration has the reference state and output of CE stage has 180 ° phase difference. In order to minimize gain mismatch, the same type of transistors (npnH3shp1) are chosen, because in H3 technology, "shp" series HBTs have highest f_T. In npnH3shp1, there is only one HBT, for this reason 3 parallel transistors are utilized for both of the CB and CE amplifiers considering input matching and linearity issues. 1.242 mA of current is consumed from the power supply of CE amplifier (Vcc_{CE} =1.4V). On the other hand, 1.935 mA of current is consumed from the power supply of CB amplifier (Vcc_{CB} =2.4V). The difference in current consumption is also required for minimizing the gain mismatch. C_{block1} is set to 2pF in order to minimize phase imbalance. L_{in1} (675 pH), L_{in2} (665 pH), C_{in1} (450fF), and C_{in2}(450fF) are used for input matching. R_{balun} is set to 219 Ω, which is the optimized value regarding input matching and biasing of CB amplifier. Rbias2 is set to 5 kΩ, and C_{bypass} is set to 12pF for decoupling issues. L_{out1} (1.1 nH), $L_{I/Q}$ (50pH), Cout1(450fF), Cout2 (450fF) and R_{out1} (85Ω) forms the inter-stage matching between the BALUN and poly-phase filter. In bias of base of CE amplifier and VGAs, the bias circuit is utilized, which is shown in Fig. 18. For Q_{bias1}, Q_{bias2}, and Q_{bias3}, npnH3shp2 is chosen. R_{bias1} and R_{bias0} are 800 Ω. Simulation results show that, at

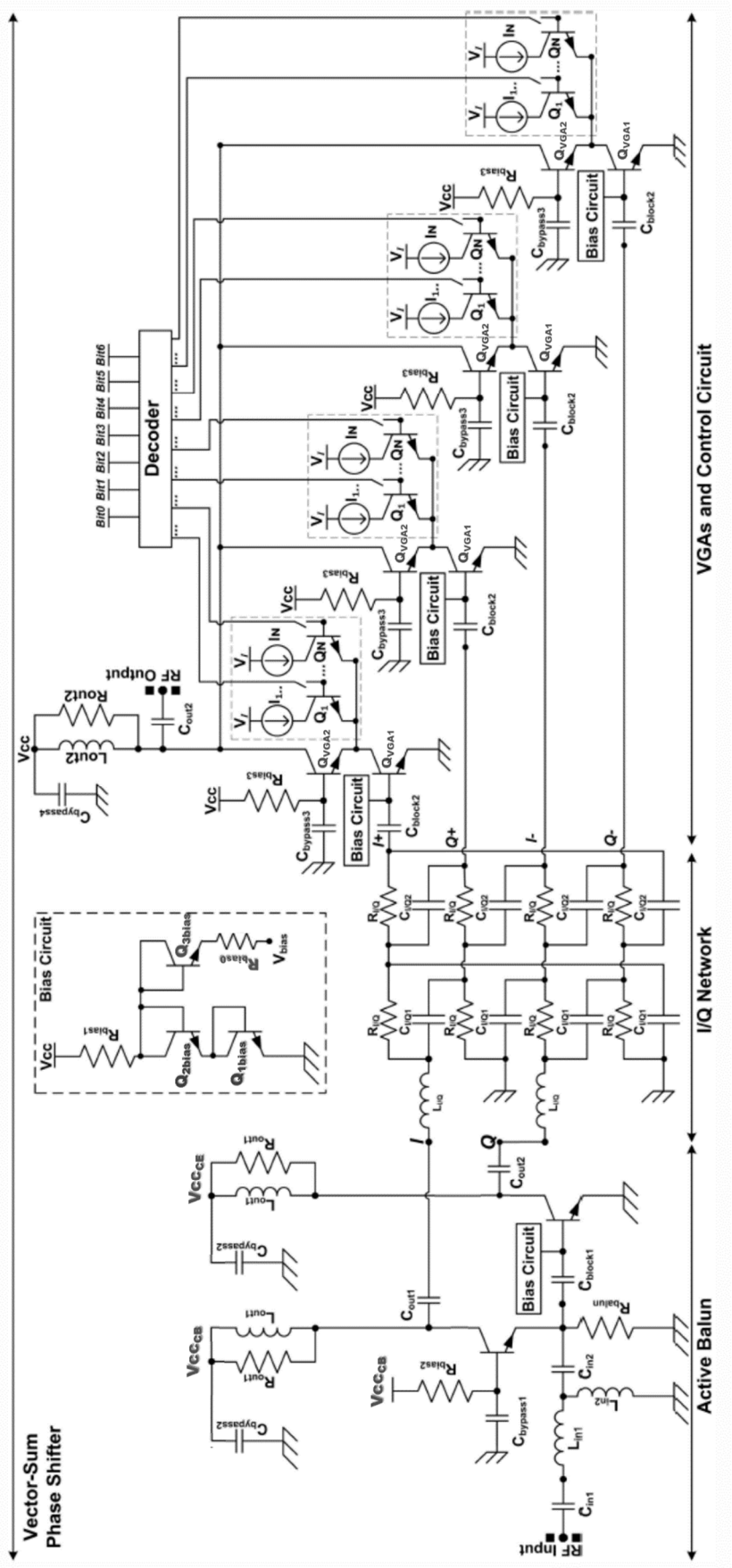


Fig. 18: Complete circuit schematic of Vector-Sum type phase shifter.

output of the BALUN phase error is lower than 0.1°, and amplitude error is lower than 0.1 dB. BALUN is connected to ***I/Q*** network which is used to generate the reference $\boldsymbol{I^{+}}$, $\boldsymbol{I^{-}}$, $\boldsymbol{Q^{+}}$ and $\boldsymbol{Q^{-}}$ vectors. Accuracy of the synthesized phase is significantly sensitive to amplitude and phase error between the reference vectors. In spite of high signal loss, R-C based constant-phase second order poly-phase filter (PPF) is selected due to its higher precision in generation of the reference vectors accurately over a wide frequency band [67]. $R_{I/O1}$(85Ω), $R_{I/O2}$(132Ω), and $C_{I/O1}$ (150fF) forms the RC PPF, as shown in Fig. 18. Simulation results show that, in addition to the accurate phase response in 8-12 GHz, RC PPF has 0.17 dB of amplitude error in this frequency bandwidth.

Four outputs of ***I/Q*** network are connected to four identical VGAs as shown in Fig. 18. Accuracy of the synthesized phase is also sensitive to the input return loss (RL) of VGA. RL of VGA has to be as low as possible and unaffected from the gain change of VGA. For this purpose, cascode configuration (which consists of Q_{VGA1} and Q_{VGA2} as shown in Fig. 18) is selected in design of these amplifiers, and collector current of Q_{VGA1} is kept constant. For the sake of varying the gain of the amplifier, two techniques are applied simultaneously. First, the collector current of Q_{VGA2} (cascoded transistor) is partially or fully directed to current-steering transistors (Q_1-Q_N), and combination of steered current modifies the gain of the amplifier. Second, a low impedance node is generated in collector of Q_{VGA1} through opening current-steering transistors (Q_1-Q_N), and gain of the amplifier is modified through changing the load.

In design of VGA, npnH3shp8 (which consists of 8 parallel HBT) is chosen for Q_{VGA1} and Q_{VGA2}. 7.875 mA of current flows through Q_{VGA1}. As number of devices increase in this structure, the linearity increases. However, the phase insertion of behavior of VGA is dependent to the junction capacitances, therefore there is a significant trade-off between insertion phase and linearity. In order to achieve at least -10 dBm of output referred compression point, at least 8 parallel HBTs are required.

As shown in Fig. 18, each VGA utilizes 6 current steering structures which consist PMOS devices as current source, and HBT devices (Q_1-Q_6) as switches. For HBT switches, Q_1-Q_6, npnH3shp8 are chosen. Generic current source structure is used in this circuit. The current, which is flowing on a 5 kΩ resistance, is mirrored through a diode connected

PMOS device (w=5 µm, l=2.5 µm). The current sources are binary weighted, from LSB to MSB, I_{LSB} to I_{MSB} are 0.125mA, 0.25 mA, 0.5mA, 1mA, 2mA and 4mA, respectively. PMOS widths are also chosen similarly, from LSB to MSB, 6.25 µm, 12.5 µm, 25 µm, 50 µm, 100 µm, and 200 µm respectively. Long channel (l=2.5 µm) PMOS devices are utilized as current sources. For each VGA, there are 6 binary weighted current sources which are connected to HBT switches. Therefore, the gain of VGA is controlled in digital domain, using 6-bit digital control input.

As previously explained in second chapter, the output of phase shifter is

$$RF_{out} = G_1 I^+ + G_2 Q^+ + G_3 I^- + G_4 Q^- \tag{48}$$

Corresponding relative phase shift is

$$\alpha_{desired} = \angle \arctan\left(\frac{G_{2,4}}{G_{1,3}}\right) \tag{49}$$

G_1-G_4 constants are formed using four 6-bit-digitally-controlled-VGA, for this reason, 24-bit digital input is requested. For a 7-bit digitally controlled phase shifter, there will be 128 phase states, and for each phase state, there is a particular 24-bit data. This data is iteratively obtained during the post layout simulations (using Cadence), and it is written to a static LUT. A decoder (which consists the static LUT) is utilized in this phase shifter, which has 7-bit digital input and 24-bit digital output. The digital output of the decoder is connected to the HBT switches (Q_1-Q_6) of four VGA (VGA $_{I+}$, VGA $_{I-}$, VGA $_{Q+}$ and VGA $_{Q-}$).

4.1.2. Measurement Results

IHP SG25H3 technology is utilized in implementation of this PS. The area consumption of the circuit is 1.87mm × 0.88 mm without bonding pads. Die photo of this circuit is shown in Fig. 19. Although a 7-bit digital control is applied, after fabrication 6-bit phase resolution is achieved, because of the previously mentioned challenges in Vector Sum based phase shifter design. Measured relative phase response is demonstrated in Fig. 20. Proposed phase shifter has 2.8 ° of rms phase error in 9.6–11.7 GHz band, and 5.6° of

rms phase error in 8.2-12 GHz, as shown in Fig. 21. On the other hand, rms gain error of proposed phase shifter is measured lower than 2 dB in 8-12 GHz. The total power consumption of active BALUN, four variable gain amplifiers and bias circuits is 110 mW.

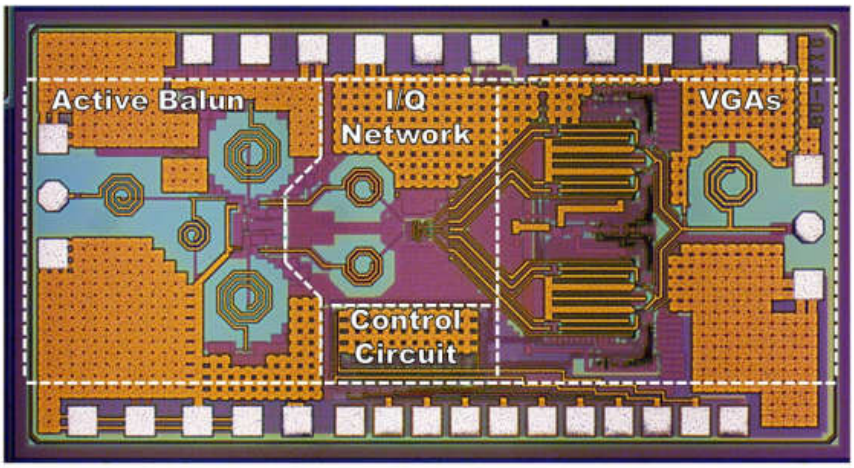


Fig. 19: Die photo of previously fabricated vector sum based phase shifter with static LUT.

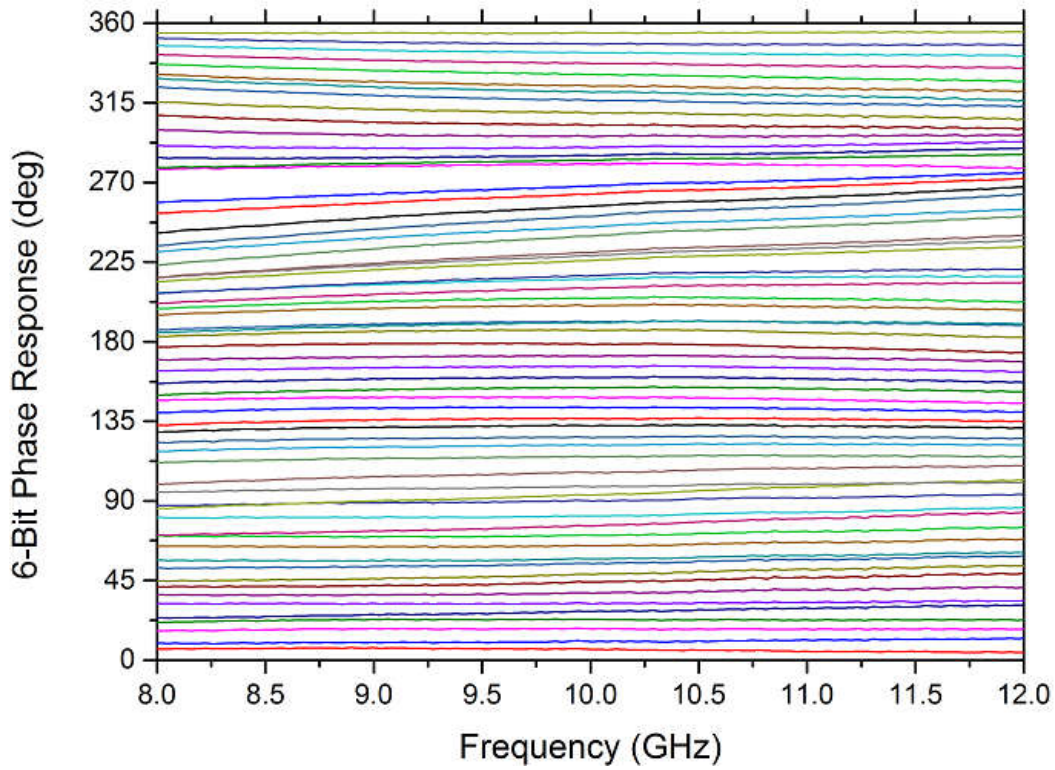


Fig. 20: Measured Relative insertion phase response of previously fabricated vector sum based phase shifter with static LUT.

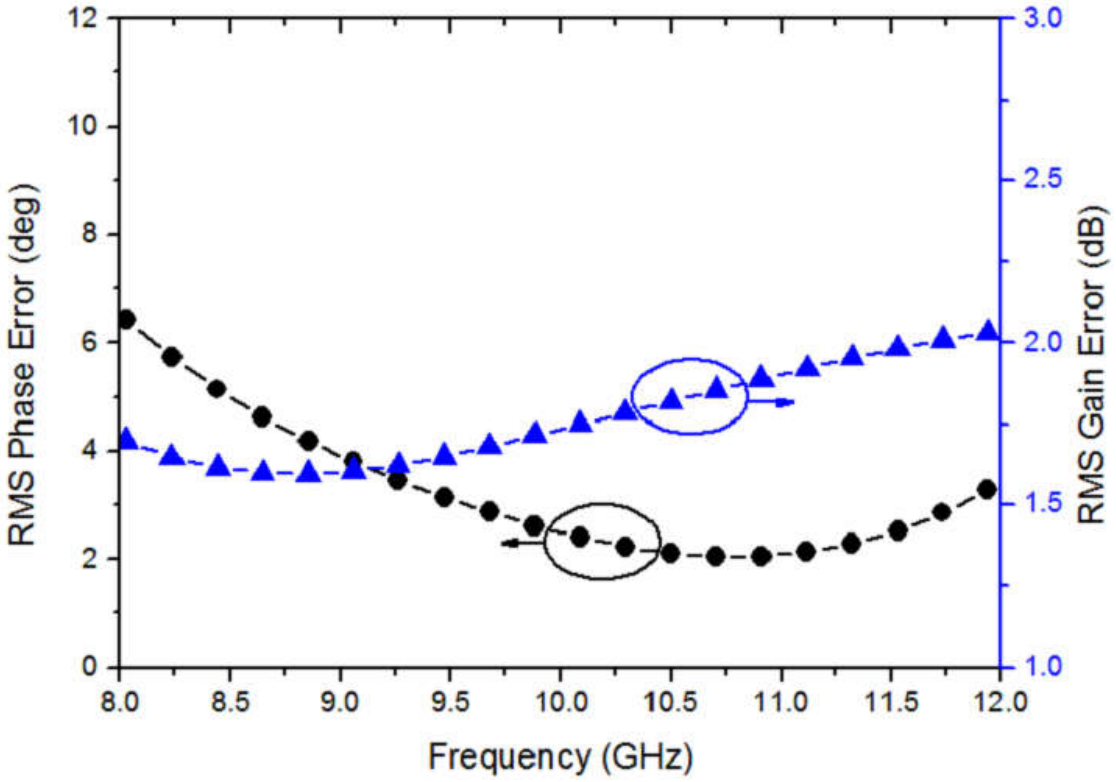


Fig. 21: Measured rms phase and gain error of previously fabricated vector sum based phase shifter with static LUT.

4.2 Power Detector

The self-calibration needs a power detector with very high dynamic range (more than 29 dB) and very high linearity (less than 2%). With using conventional methods, it is not possible to achieve more than 27 dB of dynamic range. Therefore, it is mandatory to propose a new power detector circuit. In this thesis we propose a novel power detector which uses HBT in cascode configuration with a diode connected PMOS load. The cascode topology enables implementation of an input matching network that is independent of input power level by isolating detector output from the input node. The diode connected PMOS load improves the dynamic range of the detector by effectively reducing the load impedance for high DC currents.

4.2.1 Principle of the Operation and Circuit Design

The power detector works in the square-law region, to acquire the power in a target frequency band and transform it to an output voltage. The common emitter configuration is widely utilized in conventional power detectors as depicted in Fig. 22.a. Output DC

voltage is a function of input signal amplitude. Considering a sinusoidal input signal with frequency *f* and amplitude V_i, the output DC voltage can be derived as:

$$v_{be} = V_i \cos \omega t \tag{50}$$

$$v_{BE} = V_{BE} + v_{be} \tag{51}$$

$$i_C = I_S e^{v_{BE}/V_T} \tag{52}$$

$$i_C = i_C(V_{BE}) + i'_c(V_{BE})(v_{BE} - V_{BE}) + \frac{i_c''(V_{BE})}{2!}(v_{BE} - V_{BE})^2 + \ldots \tag{53}$$

$$I_{DC} = i_C(V_{BE}) \tag{54}$$

$$i_C = I_{DC} + \frac{I_{DC}}{V_T} v_{be} + \frac{I_{DC}}{2V_T^2} v_{be}^2 + \ldots \tag{55}$$

$$i_C = I_{DC} + \frac{I_{DC}}{V_T} V_i \cos \omega t + \frac{I_{DC}}{2V_T^2} V_i^2 \frac{1}{2}(1 + \cos 2\omega t) \tag{56}$$

At DC,

$$i_C = I_{DC} + \frac{I_{DC}}{4V_T^2} V_i^2 = I_{DC}\left(1 + \frac{V_i^2}{4V_T^2}\right) \tag{57}$$

$$V_{out} = V_{CC} - I_{DC} R_1 \left(1 + \frac{V_i^2}{4V_T^2}\right) \tag{58}$$

$$V_{diff_{conv}} = Vout(0) - V_{out}(Vi) = I_{DC} R_1 \frac{V_i^2}{4V_T^2} \tag{59}$$

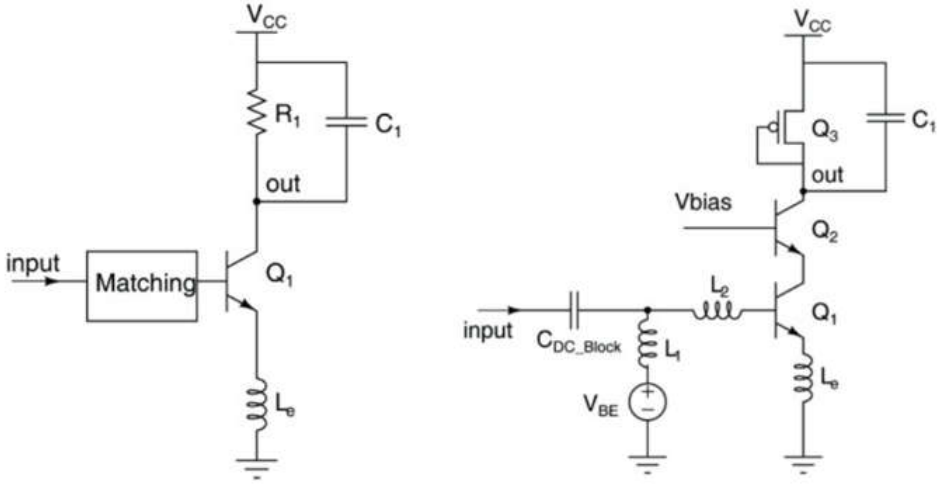


Fig. 22: (a) Conventional power detector. (b) Proposed power detector with increased input power dynamic range.

where I_{DC} is the DC current of HBT when RF signal is not applied to the input, V_T is the thermal voltage and R_l is the load resistor [68]. From (37) it is seen that by using a fixed resistor value, DC voltage drop at the output is linear to the square of the input signal amplitude. Power detectors in this configuration operate in a limited dynamic range (around 27 dB [68], 20dB [69]) and compress in a very low input signal power (around -30 dBm [68], -15dBm [69]).

In this work, a new power detector configuration with a diode connected PMOS load is proposed, as shown in Fig. 22.b. In this configuration, assuming long channel PMOS device, the output DC voltage can be derived as,

$$I_d = \frac{1}{2} K_p \left(\frac{W}{L} \right) \left(|V_{GS}| - |V_{th}| \right)^2 \tag{60}$$

$$V_{out} = V_{CC} - |V_{GS}| = V_{CC} - |V_{th,p}| - \sqrt{\frac{2I_d}{K_p \left(\frac{W}{L} \right)}} \tag{61}$$

$$I_d = i_C = I_{DC} \left(1 + \frac{V_i^2}{4V_T^2} \right) \tag{62}$$

$$V_{out} = V_{CC} - |V_{th,p}| - \sqrt{\frac{2I_{DC}}{K_p \left(\frac{W}{L} \right)}} \sqrt{\left(1 + \frac{V_i^2}{4V_T^2} \right)} \tag{63}$$

$$V_{diff_{\text{Proposed}}} = V_{out}(0) - V_{out}(V_{in}) = \sqrt{\frac{2I_{DC}}{K_p \left(\frac{W}{L} \right)}} \left(\sqrt{\left(1 + \frac{V_i^2}{4V_T^2} \right)} - 1 \right) \tag{64}$$

where, K_p is a process parameter, $V_{th,p}$ is the threshold voltage of the PMOS transistor and W/L is its aspect ratio. In conventional power detectors, as shown in (59) DC voltage drop is proportional to square of the input signal amplitude. However, in proposed configuration, (64) shows that, for large signal amplitudes, DC voltage drop is proportional to input signal amplitude which improves the dynamic range of the power detector. Fig. 23 shows the comparison of (59) and (64). In these calculations, Kp is taken as 65 µA/V^2, I_{DC} is 1mA, R1 is 1200 Ω, w/l is 80, Vth is 0.9V, Vt is 25,9 mV. This figure shows that; 15 dB of improvement is observed at dynamic range.

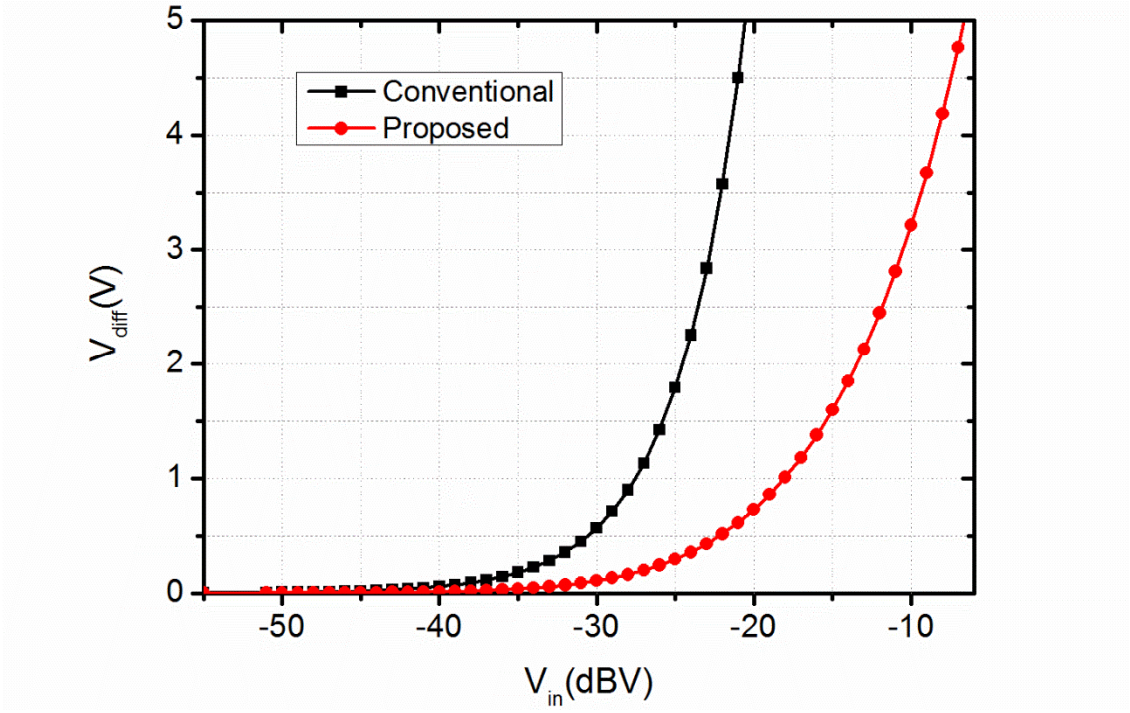


Fig. 23: Theoretical comparison of conventional PD and proposed PD.

On the other hand, in standard CE power detectors output noise power density is expressed as [68]

$$\frac{\overline{V_n^2}}{\Delta f} = 2qI_{DC}R^2 + 4kTR \tag{65}$$

Because of utilization of the diode connected PMOS, as the load, R can be replaced with $1/gm_{PMOS}$ and thermal noise of the resistance can be replaced with thermal noise of PMOS,

$$i_{d,PMOS}^2 = \frac{8kT}{3} g_{m_{PMOS}} \tag{66}$$

The load is $\frac{1}{g_{m_{PMOS}}}$, therefore,

$$v_{d,PMOS}^2 = \frac{8kT}{3g_{m_{PMOS}}} \tag{67}$$

approximately, the final expression will be:

$$\frac{\overline{V_n^2}}{\Delta f} = \frac{2qI_{DC}}{g_{m_{PMOS}}^2} + \frac{8kT}{3g_{m_{PMOS}}} = \frac{q}{K_p \frac{W}{L}} + \frac{8kT}{3\sqrt{2K_p \frac{W}{L} I_{DC}}} \tag{69}$$

The first term in (65) is linearly proportional to DC current of the circuit which underlines a significant tradeoff. If the objective is to create a higher DC voltage drop from the same input signal power, (59) shows that higher $I_{DC}R_L$ multiplication is required which causes higher output noise. On the contrary, in the proposed technique, DC current appears in the second term of (69) while providing an effect in opposite direction and creating more flexibility for a designer.

Using a low pass filter [68], [69], [70], [71] or an integrator [72], [73], [74] cascaded to the rectifier (as C_1 in Fig. 22 a.) is widely utilized in power detectors in order to suppress high frequency signals at output. In conventional CE configuration, the input return loss of the power detector strongly depends on the value of C_1 due to the low isolation from output to input. Hence, because of this capacitive behavior, the input matching becomes narrowband. In addition, as the input signal power changes, the voltage drop across R_1 also changes as well. This results in a change of the collector-base junction capacitance of Q_1. Therefore, the variations in input signal power strongly affects the input matching performance of the power detector causing significant measurement errors.

In order to increase the isolation from the load capacitance to the input, a cascode configuration, which is widely used in LNA's for this purpose [75], is proposed as shown in Fig. 22.b. With this configuration the input of the circuit can be matched to 50 Ω in a wider bandwidth. In addition, in the cascode configuration, the collector voltage of Q1 changes in a logarithmic function of input signal power. Therefore, in this configuration, the variation of CCB (and input return loss) is significantly lower than common emitter configuration. In design of the circuit, length of the diode connected PMOS is set to 8 μm in order to assure the operation in the square law region, while the width is 640 μm. VCC of the circuit is 7V. For this reason, 16 parallel HBTs with high breakdown voltage are chosen as Q2 (npnH3_HV). High performance transistors (npnH3shp) are chosen as Q1 in order to maximize the conversion of input amplitude to output DC current, and eight parallel HBTs are used considering maximum dynamic range. The matching circuit consists of a shunt inductor (L_1=1.36 nH) connected to a serial inductor (L_2=980 pH), which are connected to the base of Q1. On the other hand, grounded co-planar transmission line is used as emitter degenerate inductor (L_e=200pH). Transmission lines and inductors are custom designed using EM simulation tools.

4.2.2 Measurement Results of Power Detector

The X-band power detector has been designed and fabricated in IHP 0.25-μm SiGe BiCMOS process with five metal layers. The 3μm-thick top metal has been used to realize the transmission lines and inductors. Fig. 24 depicts the micrograph of the fabricated 0.52 mm × 0.820 mm chip.

In measurements, Agilent E8267D signal generator is connected to the input of power detector which generates 10 GHz single tone signal while the output is connected to Agilent DSO-X 3012A oscilloscope. Proposed power detector provides a very linear response (error is less than 2%) for the input signal amplitudes between 2.2mV and 280mV as presented in Fig. 25. In this figure, V_{diff} indicates the voltage drop as the result of the input signal amplitude.

The measurement result matches well with (39), as shown in Fig. 26. For this circuit, minimum detectable signal power is limited by the noise performance of the circuit, and it is -45 dBm, which provides 1mV DC voltage change at the output. On the other hand, maximum input signal power is limited by the V_{DS} and V_{GS} breakdown voltages of the PMOS load. Measurement results show that, from -42 dBm to 10 dBm, 1dB power increment provides at least 1mV voltage change at output, therefore, the dynamic range is 52dB. Measurement results for 7 different input power settings are shown in Fig. 27, in which S_{11} is lower than -8 dB for proposed dynamic range from 7 to 20 GHz. Table 8

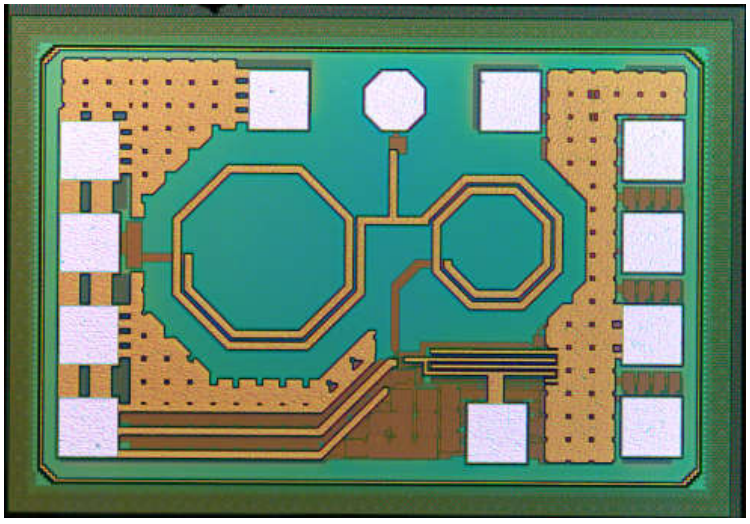


Fig. 24: Die photo of the power detector. Total chip area is 0.42 mm^2, including the pads.

provides a comparison between the measured performances of the proposed detector and the state of art for power detectors fabricated in deep-submicron CMOS and BiCMOS silicon technologies [68] - [74] . In [70] and [72], unbalanced source coupled pairs are used as rectifiers which are cascaded to attenuators [70] or amplifiers [72]. In these circuits, 6-10 dB dynamic range is achieved in one stage, therefore, in order to enhance dynamic range performance, 5-7 stages of rectifier and attenuator (or amplifier) arrays are formed. In [71], active source degenerated common source configuration is proposed, which improves the dynamic range from 10 to 13 dB in one stage. In [69] and [68], conventional common emitter configuration is used. High responsivity performance is achieved in these circuits; however, dynamic range is not higher than 27 dB. In [74], common base configuration with current mirror load is used achieving 30 dB of dynamic range. In literature, maximum 47 dB dynamic range is achieved in single stage, using self-biased power detector with quasi Tcoil matching network [73]. As shown in this table, proposed detector has the highest measured dynamic range with low power, low area and high sensitivity maintaining more than 8 dB return loss in 13 GHz bandwidth.

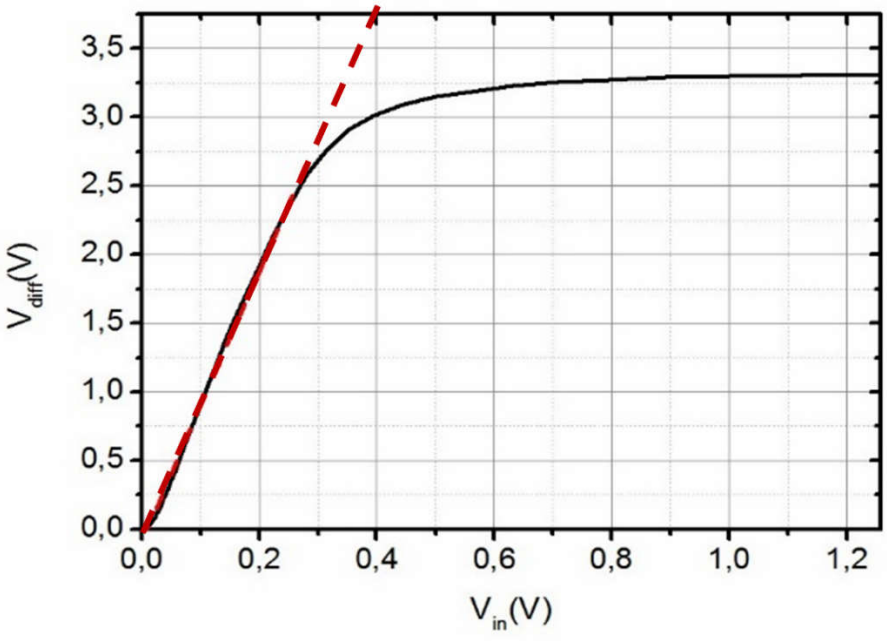


Fig. 25: Output DC voltage vs input signal amplitude. Dashed line shows the linear region.

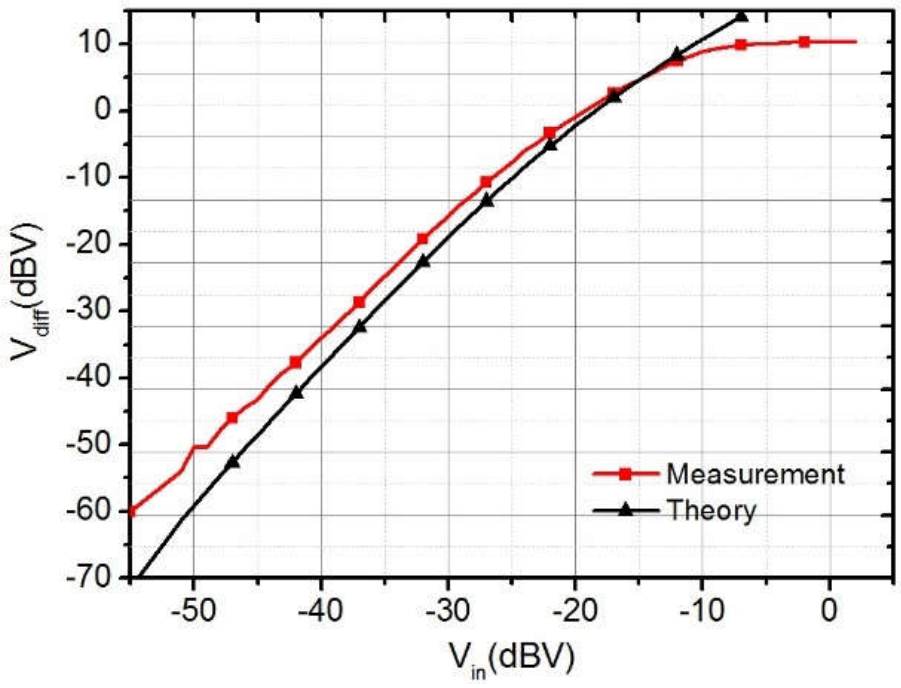


Fig. 26: Logarithmic-Logarithmic plot of output DC voltage change vs input signal amplitude.

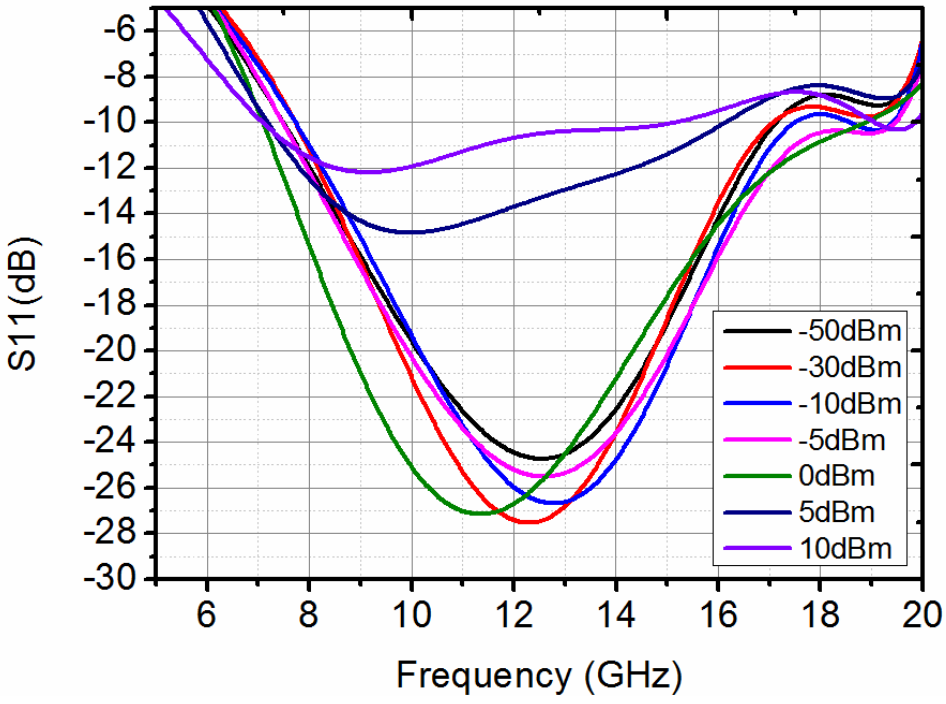


Fig. 27: S-parameter measurement results for 7 different input amplitudes. S11 is lower than -8 dB in 7-20 GHz and 52 dB dynamic range.

Table 8: Performance Comparison with Recently Published Power Detectors

Ref.	Freq. (GHz)	Tech. (nm)	Return Loss (dB)	Dyn. Range (dB)	P_{min} (dBm)	Pow. Cons. (mW)	Area (mm^2)	Technique
[68]	90-102	180 (BiCMOS)	10	20	-52.6	0.075	0.4332	CE with R load
[69]	87-100	120 (BiCMOS)	10	27	-42	0.18	0.14	CE with R load
[70]	0.3-10	180 (CMOS)	N/A	42	-12	0.55	0.113	7 branches of unbalanced source-coupled pairs with cascaded attennuators
[71]	2-16	130 (CMOS)	N/A	50	-30	35	0.75	3 branches of active source degenerated common source configuration with cascaded amplifiers
[72]	DC-8	180 (CMOS)	N/A	40 (8GHz)	-40 (8GHz)	67.2	0.98	5 branches of unbalanced source-coupled pairs with cascaded limiting amplifiers
[73]	0.5-20	130 (CMOS)	14	47	-38	0.1	0.085	self-biased PD with a quasi-T-coil matching network and an embedded am
[74]	50-66	55 (BiCMOS)	N/A	30	-30	0.8	0.0064	CB with current mirror load
This work	7-20	250 (BiCMOS)	8	52	-42	7	0.42	Cascode configuration with diode connected PMOS load

4.2 Amplifier and 10dB-Coupler

In order to use the signal at output of phase shifter in calibration path simultaneously, a 10 dB coupler is cascaded to phase shifter. The layout of the coupler is shown in Fig. 28. EM simulation tools, such as Sonnet and ADS-Momentum are used in design of this component. 3µm-thick top metal 2, is used for the main signal path (width is 14 µm) and 2µm-thick top metal 1 is used for calibration path (width is 8 µm). For both of the signal paths, the total length is 960 µm. Coupler consumes 285µm × 315 µm of die area. Simulation results show that from Rf_{in} port (P_1) to Rf_{out} (P_2) port, IL (P_2/P_1) is around 1.4 dB whereas the coupling factor (P_3/P_1) from P_1 to calibration loop (P_3) is -10 dB. Fourth port is terminated with 50 Ω and isolation (P_4/P_1) is 23 dB. Directivity between P4 and P3 is 13 dB.

Using an SPDT switch in order to route the signal to calibration path from main signal path could have been an alternative approach, however, this component adds around 3 dB of insertion loss to main signal path [76] [77]. On the other hand, the drawback of using coupler is the 10dB of insertion loss in calibration path. In this thesis, the loss in calibration path is preferred to the loss in main signal path because of the following reasons. First of all, the loss in the signal path increases the noise figure. Secondly, vector sum type phase shifter saturates at very low output signal power level (such as -11 dBm [54]), thus, the linearity of this block determines OP1dB compression point of the T/R module. Therefore, insertion loss after this block has to be kept minimum not to reduce linearity of the TR module. In addition, the loss in calibration path can be compensated with an amplifier which will be turned on (and consume power) only when the calibration mode is on. However, the amplifier to be designed to compensate the loss in signal path has to operate and consume continuously. Furthermore, in terms of area consumption, using coupler is significantly better choice in comparison with the SPDT because the area of coupler (which is 0.088mm^2) is significantly lower than the area of SPDT (typically 0.4 - 1 mm^2 [76]).

As mentioned before, phase shifter saturates at -11 dBm of output signal power level,

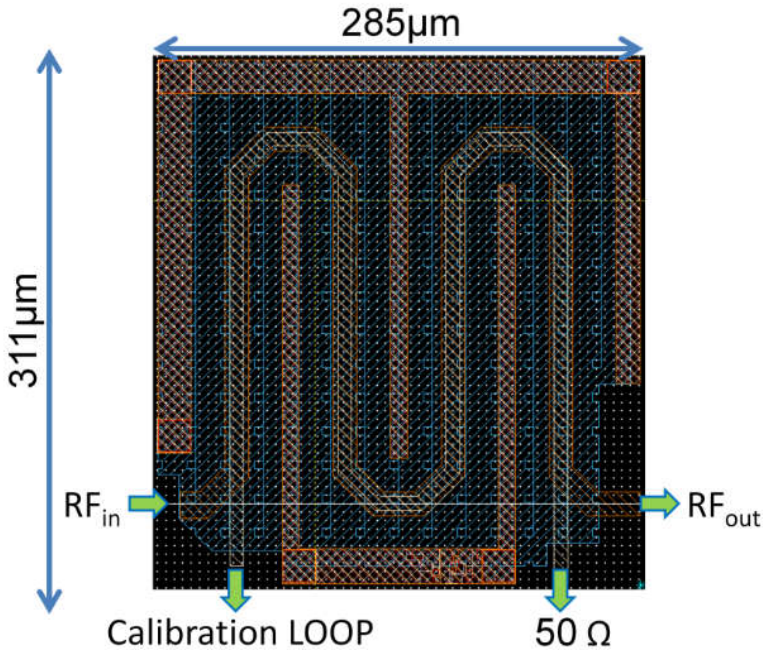


Fig. 28: Layout of the coupler, width of the top M2 is 14 µm, width of the top M1 is 8 µm, length is 960 µm.

and the loss of the coupler is 10 dB. In order to increase the power level of calibration signal to the linear working range of power detector (which is -7 dBm to -37 dBm), an amplifier is required. The amplifier employs a conventional inductively degenerated cascode configuration which is shown in Fig. 29. In addition to its role in matching, L_1 (860 pH) used to increase linearity performance of the amplifier. L_B (250 pH) and L_E(55 pH) are used for matching purposed. L_C (720 pH), R_C (80 Ω) and L_{out} (100 pH) forms the output matching network. Moreover, active bias circuits are used for biasing base nodes of both Q_1 and Q_2 for achieving more power handling capability. In the first bias circuit, (which provides the base current of Q1), R_1 and R_2 are 1.46 kΩ and 100 Ω, respectively. For the first and second bias circuits, npnH3shp8 is used for both of Q_{B1} and Q_{B2}. For the second bias circuit, rather than L_1 inductance, a high resistance (1.6 kΩ) is utilized, which provides higher stability. For this circuit, R_1 and R_2 are 600 Ω and 1.6 k Ω, respectively. Q_1 and Q_2 are selected as high performance HBT (3 parallel npnH3shp8) for low NF. Number of transistors in Q_1 and Q_2, and collector current(8.6mA) are optimized for high linearity and moderate noise figure. Collector voltages are adjusted close to breakdown voltages in order to provide maximum possible voltage swing for the RF signal.

This block is also separately fabricated, and according to measured results, the gain of the amplifier has the peak value of 14.5 dB at 12 GHz where 3dB gain bandwidth is from 7.5 GHZ to 18 GHz. The linear amplifier has average NF of 2.7 dB at X Band. IP1dB of the LNA is 5 dBm where, consequently, output P1dB is measured as 18.5 dBm. LNA consumes 0.32 mm^2 of die area.

Power consumption of the main building blocks of the calibration loop is shown in Table 9. In this table, Phase shifter will be working constantly, however power detector, LNA and ADC will be turned on when the calibration mode is on. Therefore, during the calibration (which will be around a few seconds), the total power consumption will be around the twice of the power consumption of phase shifter. Assuming that, the calibration is one-time-procedure (after calibration phase shifter can operate hours), the power consumption of LNA, PD and ADC are acceptable. To sum up, achieving the linearity performance with relatively low DC power dissipation (54mW) and reasonable NF makes this block as an excellent asset for proposed recalibration system.

Table 9: Power consumption of main building blocks

Phase Shifter	Power Detector	LNA	ADC
110 mW	7 mW	54 mW	61.6 mW

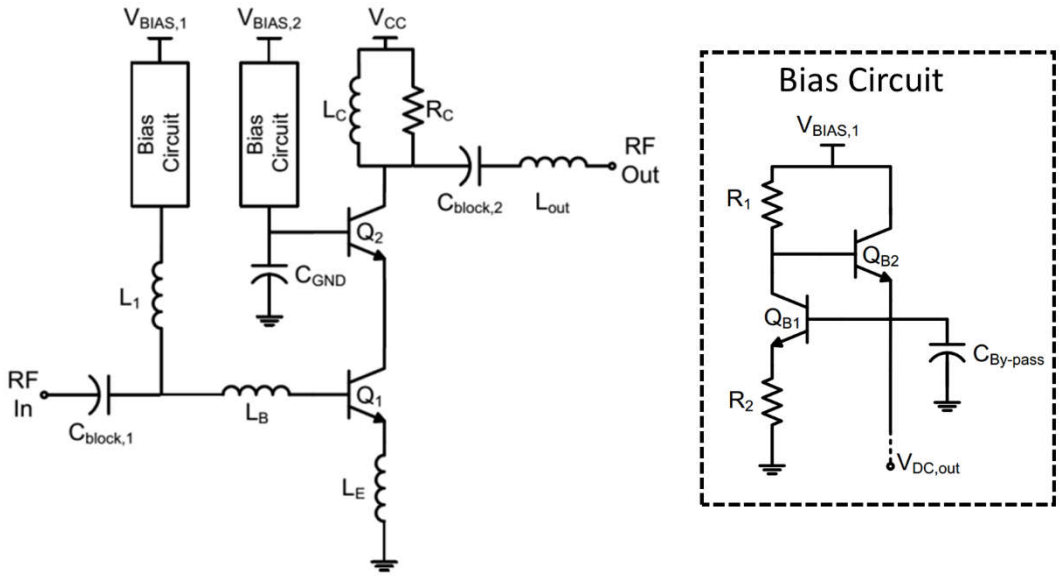


Fig. 29: Schematic of amplifier circuit.

4.3 Analog/Digital Converter Design

Design of a state of the art ADC is not primary purpose of the thesis. The main objective is to meet moderate level of specifications, therefore, straight forward design techniques are applied rather than novel methodologies. Significant specifications are high input voltage range (3V), high resolution (10-bit), low area (<0.1 mm^2) and average clock speed (10 MHz). Clock speed and Power consumption performances do not have important role in demonstration of the main idea of the thesis. Clock speed determines the calibration time which will be one-time procedure for the phased array. On the other hand, there will be only one ADC and this circuit will only consume power during the calibration. From these perspectives, a successive approximation register (SAR) based architecture is selected.

SAR based architecture is depicted at Fig. 30. In this architecture, one analog voltage comparator is used which compares the input signal (the signal to be converted to digital) and internal reference signal which is generated in the circuit. A Digital to analog converter (DAC) is used to generate the reference signal according to the approximate digital code which is generated by the successive approximation register that uses logarithmic search algorithm. Flowchart of the algorithm is illustrated in Fig. 31. In this figure, DAC_{out} is the output of Digital to analog converter, ADCin is the input signal of Analog to digital converter. SAR[N:0] register in Fig. 31, forms the parallel output of the ADC. Proposed 10-bit-ADC, converts analog to digital in 10 cycles.

In design of DAC, R-2R resistive ladder is connected to an operation amplifier (OPAMP) with unity gain buffer configuration. Additionally, in design of OPAMP a two stage miller OTA configuration is used. The schematic of OTA (with optimized transistor geometries and device values) is shown in Fig. 32. Simulation results show that, OTA has 40 dB of gain and 64° of phase margin. The schematic of comparator (with optimized transistor geometries) is given at Fig. 33. In design of this circiuti, the techniques at [78] are applied.

Fig. 34 shows post layout simulation results of ADC, which also demonstrates the operation principle of the circuit. As shown in this figure, 1.92 V of analog DC voltage is converted to digital. In first clock cycle, SAR generates a signal to set the reference voltage to 2.25V which is the middle voltage of the input voltage range (0.5V-4V), and the result of the comparison is **0**. In second clock cycle, the reference voltage is set to 1.375V (=0.5+3.5/4), and the result of the comparison is **1**. At the end of ten clock cycle, the bit sequence of 0-1-1-0-1-0-0-0-0-0 is generated by the ADC, for 1.92 V of analog DC voltage input. Layout of the circuit is depicted at Fig. 35**,** the circuit consumes 235 µm × 215 µm of area, and 61.6 mW of power consumption, when the clock frequency is 10MHz.

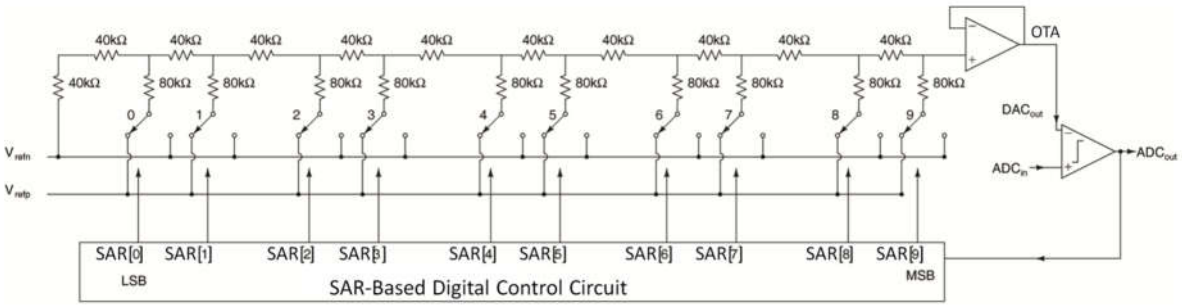


Fig. 30: Block diagram of SAR based ADC.

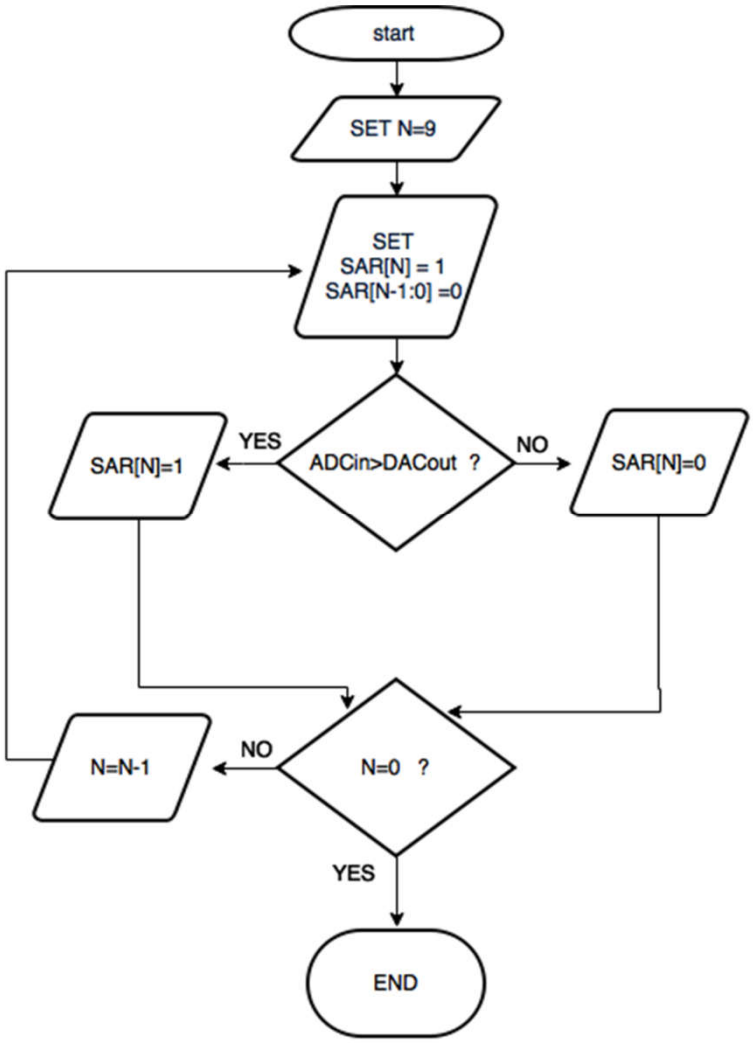


Fig. 31: Flowchart of the SAR algorithm.

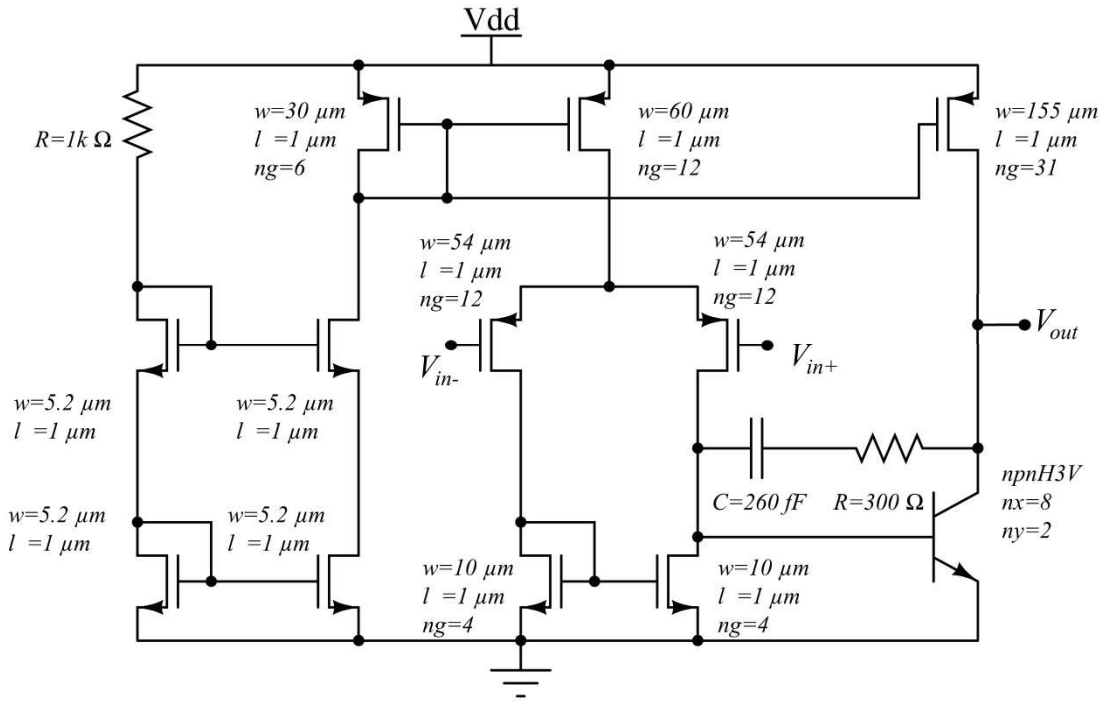


Fig. 32: OTA schematic with optimized transistor geometries.

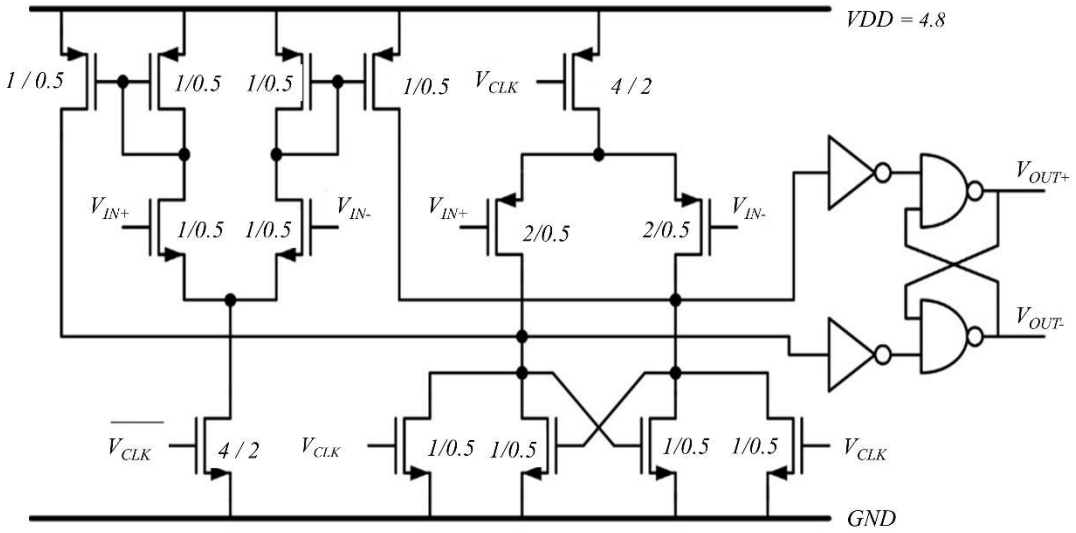


Fig. 33: Comparator circuit with optimized transistor geometries.

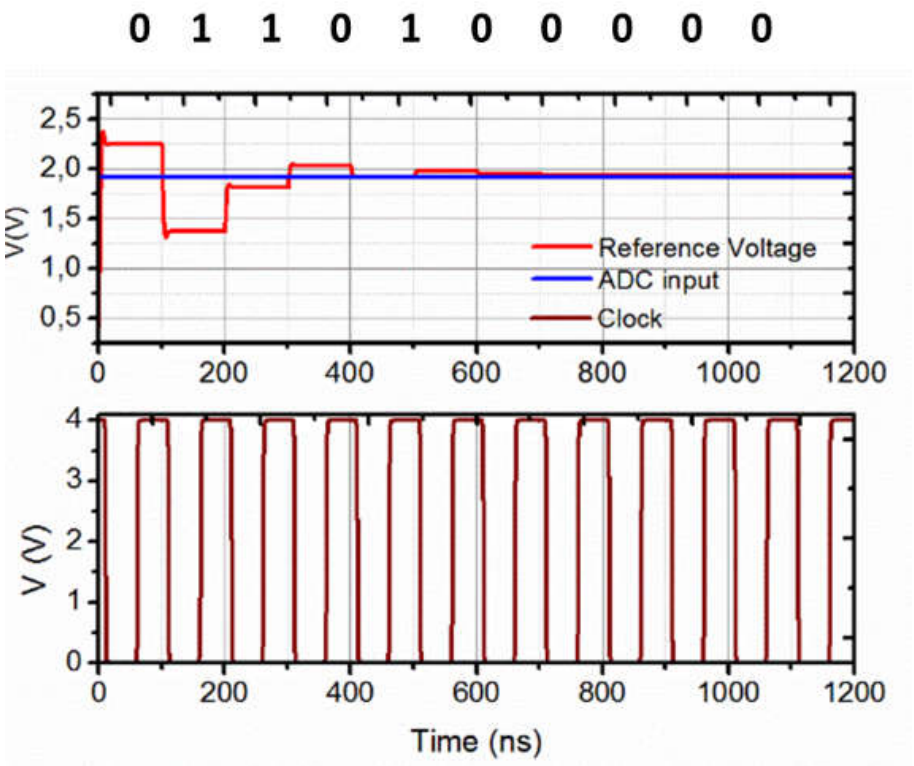


Fig. 34: Post layout transient Simulation Results of ADC.

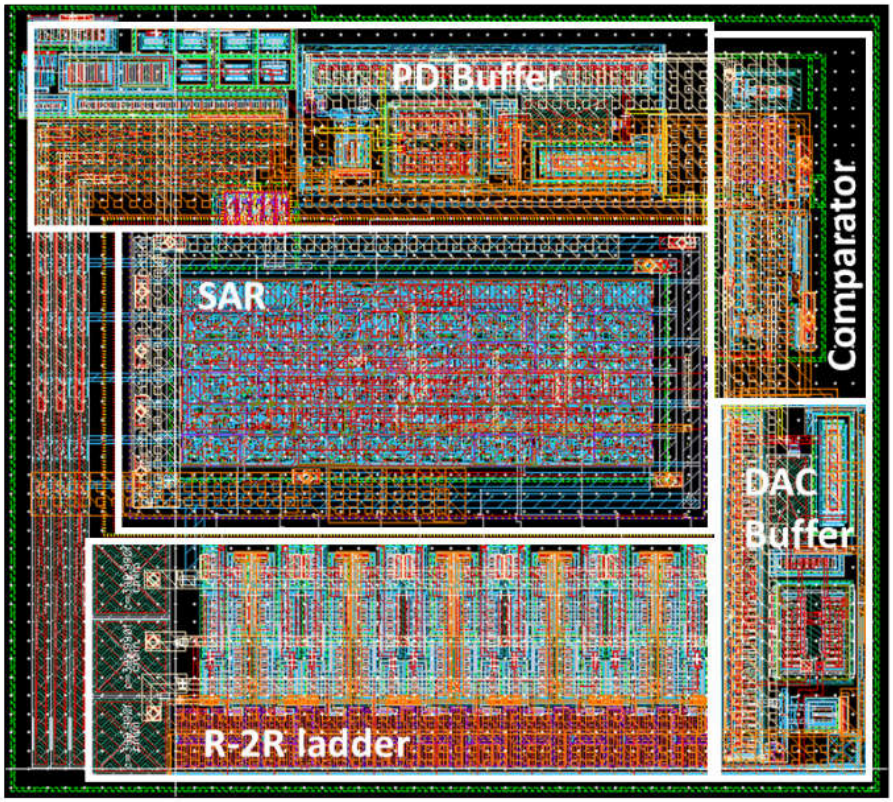


Fig. 35: Layout of the ADC.

4.4 DPU Design

As the first step of the design of the DPU, a verilog code written with the algorithm which is summarized at Fig. 15. The flowchart of the code is illustrated at Fig. 36. The function of the circuit can be reminded as:

1- Measurement, and record of amplitudes of I, Q and S vectors, with 10-bit ADC accuracy (For this reason, there will be 4 register array (12x64) for I-Q vectors, and 8 register array (12x64) for S vectors.)

2- Calculation of the phase error for each phase state ($\cos(\alpha)$ is represented with 15-bit floating number, and floating number multiplication techniques are applied)

3- Finding the optimum vector pair for minimum phase error

4- Generation of LUT in a register array (24x128)

Two different DPU are designed for this thesis. The First DPU is designed to be used in a FPGA, and the second DPU is designed to be completely integrated to the other

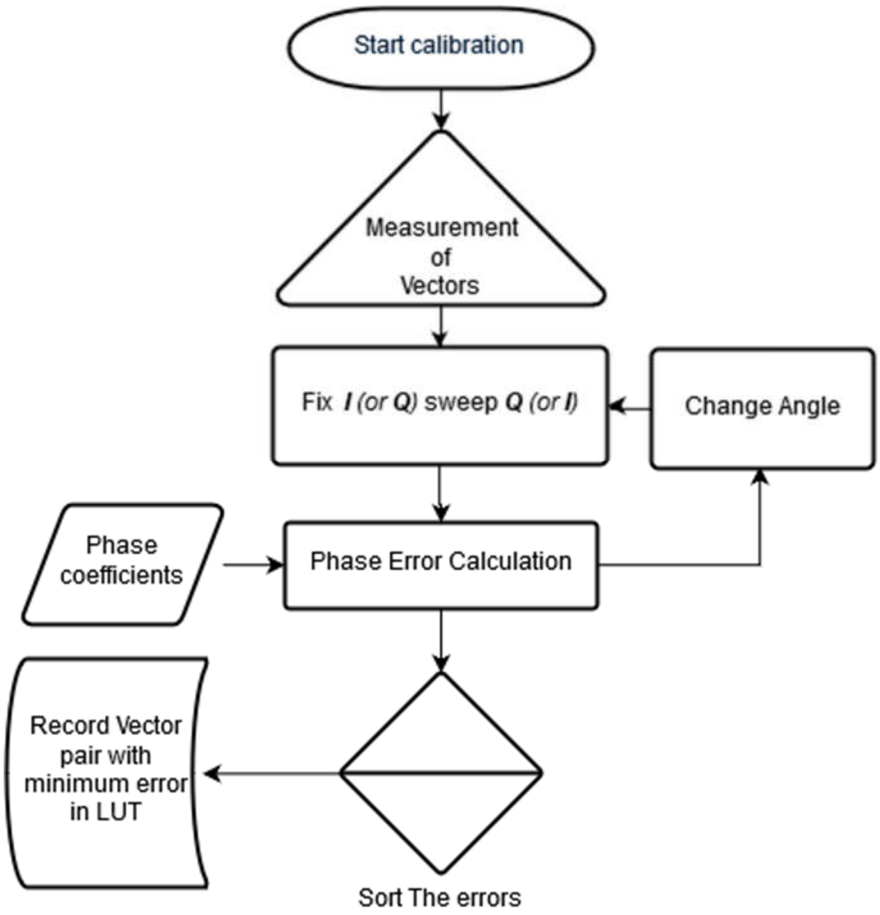


Fig. 36: Flowchart of the proposed digital processing unit.

building blocks of proposed system. The first design relies finishing all of the measurements before calculations. All of the I_p, I_n, Q_p, Q_n vectors and all of their sum combinations are measured in 768 measurement steps, and saved at memory. After these measurements, all of the measurements are finalized in less than 200µs. However, for this operation, significant amount of memory is required for calculations and measurements, which consumes more than 10 mm^2 of digital circuit area for 250 nm IHP technology. For this reason, in second design, the code is changed such that, vector size is measured whenever is it is required during the calculations. With this technique, more than 16000 measurements are required which will be finalized in 10 ms, however, unnecessary memories are removed from the circuit and area consumption is reduced significantly.

The final area of the digital circuit is reduced to 1.3 mm^2 at 250 nm IHP technology. Area consumption of the main building blocks are shown at Table 10. Although the role of the DPU is to assist phase shifter and reduce its phase error, the area consumption of this digital circuit is comparable with the phase shifter itself. However, the proposed calibration idea is still feasible to be applied on advanced technologies because of the following reasons. First of all, proposed circuit is designed in 250nm H3 technology which is not optimized for digital design. Standard-cells consume significant area in this technology. For instance, smallest inverter and flip-flop in this standard-cell library consume 41.8 and 198.6 μm^2, respectively. However, in standard cell library of 130nm IHP-S technology, smallest inverter and flip-flop consume circuits consume 7.1 and 40.4 μm^2, respectively. Secondly, IHP 250nm H3 technology standard cell library does not offer large number of choices for digital gates, flip-flops, multiplexers, etc. For example, there is only one multiplexer which is a 2x1 MUX, and in order to make a selection from 8 input signals, rather than using a single 8x1 MUX, 7 MUX are required. Because of these reasons the digital circuits synthesized in this technology consumes much larger area than the ones which is synthesized in other technologies such as IHP 13S, X-FAB, etc. On the other hand, area reduction effect of using an advanced technology node and miniaturized devices is not 100%correct for RF circuits, in which passive circuits such as inductors and transmission lines dominate the circuit area. In order to compare technology nodes, DPU is synthesized in these technologies and the area consumptions are shown in Table 11. If we apply the idea in 130nm S technology,

Table 10: Area consumption of the main building blocks

Phase Shifter	Coupler	LNA	PD	ADC	ALU
1.8 mm^2	0,09 mm^2	0.32 mm^2	0.4 mm^2	0.05 mm^2	1.3 mm^2

the area of DPU will be less than $1/6^{th}$ of PS. With compact design techniques, and using the area spared for *fillers* (which are used to meet density rules of the technology) the area of DPU will be negligible.

Table 11: Area consumption of DPU in different technology nodes

IHP H3 (250 nm)	IHP S (130 nm)
1.3 mm^2	0.30 mm^2

5 SIMULATION and MEASUREMENT RESULTS

The building blocks of the system can be categorized as RF circuits and baseband circuits. PS, coupler and LNA are RF circuits working at 8-12.5 GHz band. These circuits and PD are fabricated and measured separately. On the other hand, the baseband circuits are ADC and DPU works at low frequency, therefore, it is possible to test the idea using off-chip components for the baseband circuits. In addition, for PD, the input is at 8-12.5 GHz band, and the output is at DC, therefore, the effects of packaging, and bonding is negligible for its output. For these reasons, as the first prototype, PS-Coupler-LNA and Power detector are combined and fabricated. Completely integration of RF circuits with ADC and DPU is finalized in second prototype.

5.1 Simulation Results of the First Prototype

Normally, the plan was to use transient simulations for all of the system, however, it is not possible because of the following reasons. On one hand, PS is operating at 8-12.5 GHz, therefore in transient simulations, maximum time step is in the order of a few ps. On the other hand, digital circuit finishes its operation in around 160 µs (with a behavioral model of ADC). Thus, the simulation time is excessively long. For that reason, I have used another technique for simulation of this system, which can be summarized as:

1- PS is connected to PD, and PD is connected to the 10 Bit ADC. Transient simulation (in cadence) of this system runs for 100ns. Parametric analyze runs for 64 states of each of I_p, I_n, Q_p, Q_n, and all of their sum combinations. The results are written to a .txt file.

2- Verilog code reads this .txt file for measurements and calculations. The LUT is written to another .txt file.

3- In cadence, this .txt file is imported for the settings of PS and s-parameter simulations run for phase error calculations of 128 phase states.

The first prototype consists of PS, coupler, LNA, and power detector. The block diagram is depicted at Fig. 37. The layout of the circuit is given at Fig. 38 which consumes 2.04mm × 1.3 mm of die area.

The building blocks before power detector are RF circuits, therefore, S-parameter simulations before PD are important to show the total gain and maximum possible output signal power. As the first step of the simulation flow, s-parameter simulations are applied to the sub-system which is the combination of PS-coupler-LNA. The results of this simulation are depicted at Fig. 39. This sub-system has two outputs, one of the output forms main signal path (port 3 at simulations), the other output is at calibration path (port2 at simulations). S21 at Fig. 39 (left) shows the signal gain at calibration path, and S31 at this figure shows the signal loss at main signal path. RL performance is also shown at Fig. 39 (right), and is higher than 13 dB for all ports. Maximum -11.5 dBm of input signal can be applied to this circuit, therefore, maximum input signal power for the PD is -7 dBm.

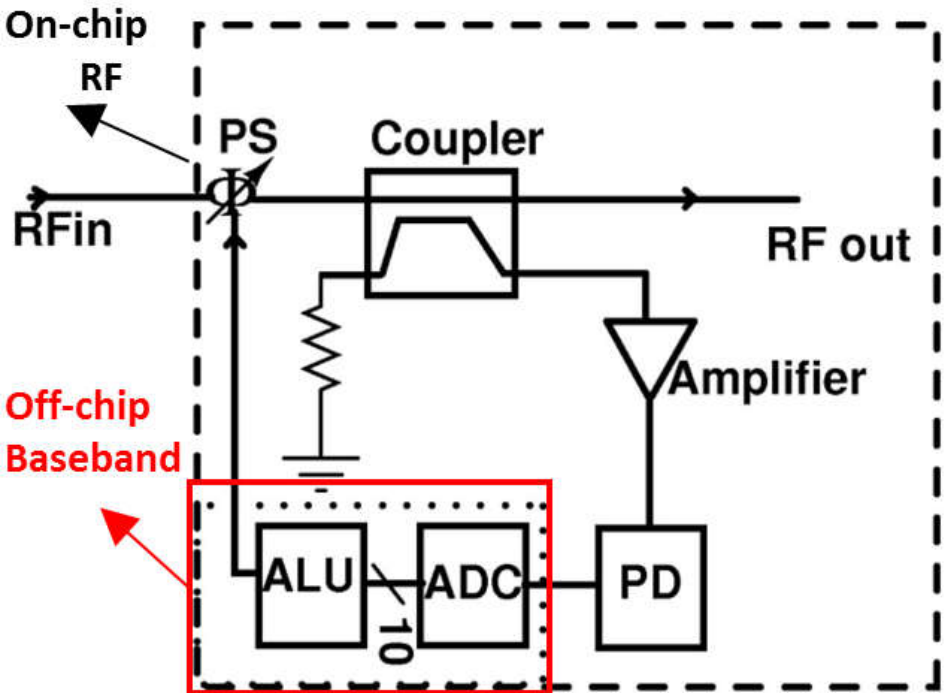


Fig. 37: On-Chip RF circuits and PD are combined in the first prototype. For baseband circuits, off-chip components will be used.

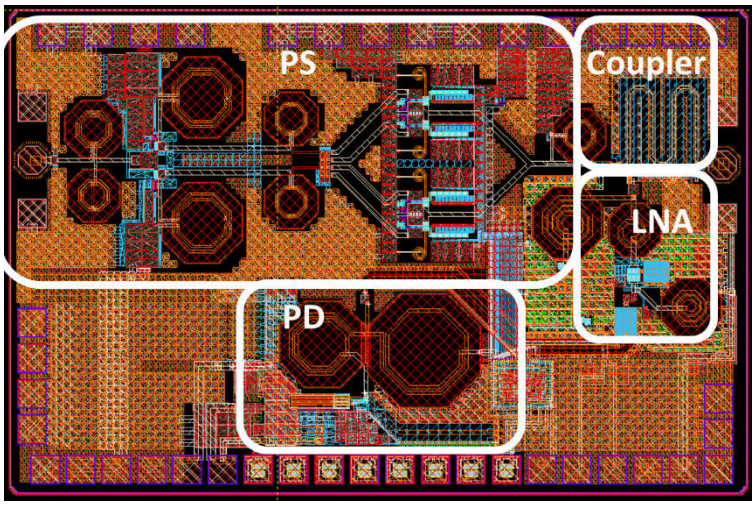


Fig. 38: Layout of the first prototype

As described before, the role of the power detector is to measure the vector sizes, which requires transient simulations. There are 64 different vector sizes for each of the I_n, I_p, Q_n and Q_p vectors, and 8 combination of these vectors. In order to measure vector sizes for all possible combinations (768 measurements are required), as the second step of the simulation flow, a long sequence of transient simulations is applied (a behavioral model of ADC is cascaded to PD in these simulations). The results are exported to a .txt file.

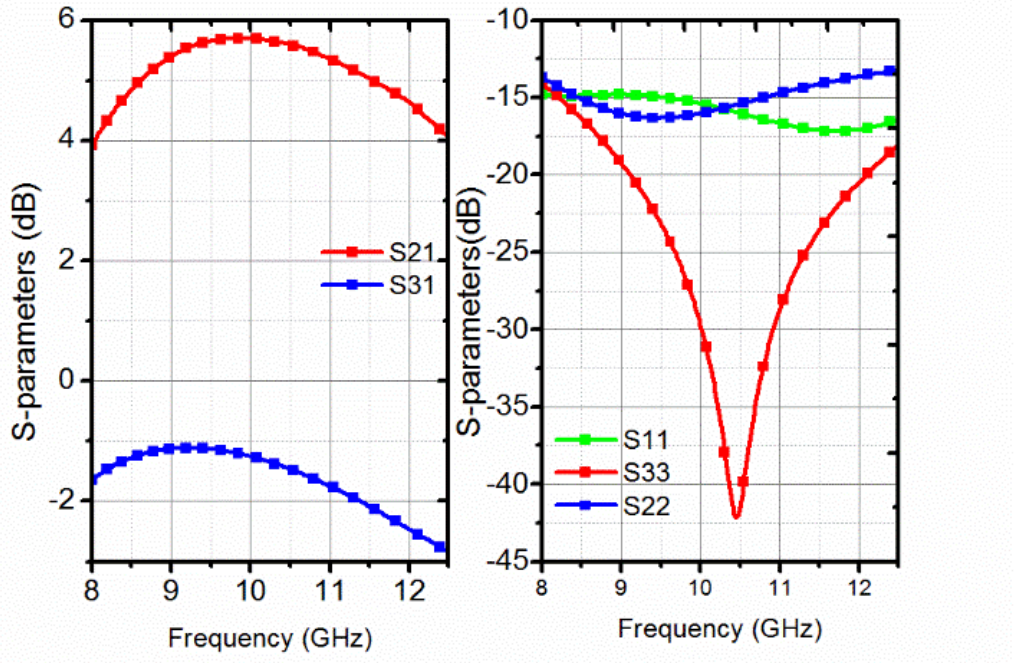


Fig. 39: S-parameter simulation results of the RF circuits before PD, S21 is the gain at calibration path, S31 is the insertion loss at signal path, S11 is the input RL, S22 is the output RL at calibration path, S33 is the output return loss at signal path.

As the third step of the simulation flow, ModelSim is used in order to simulate DPU. The program reads the vector sizes from previously generated .txt files, and applies these values to the digital circuit which generates the LUT. The self-generated LUT is also exported to a LUT.txt file.

As the fourth step of the simulation flow, S-parameter simulations of PS are done separately. An ocean script file is written to import LUT.txt file in S-parameter simulations, and phase response of phase shifter is simulated. Relative insertion phase response of the phase shifter is plotted at Fig. 40. This figure shows that; proposed system works. The LUT generated by the DPU provides appropriate information for accurate phase shift. Especially at 10 GHz, in which calibration signal is applied, most of the phase states are generated without overlapping and intersecting.

In order to show the impact of the proposed self-calibration technique, the performances of two phase shifters are compared. LUT of the first PS, is designed through iterative post-layout simulations. This LUT involves 128 registers for 128 phase state. Each of these registers are 24-bit, which are optimized for corresponding phase state. During the optimizations, post layout simulations are applied in typical conditions, at 27 °C, and typical model libraries are utilized. This PS is previously fabricated, and design details with the measurement results are explained in second chapter, which is also published in [54]. From now on, the performance of this PS (first) is represented with *Static-LUT* in figures. In second phase shifter, the proposed self-calibration technique is applied, and the LUT of this PS generated by DPU. From now on, the performance of this PS (second) is represented with *Self-Generated* in figures.

RMS phase error of these PS is shown at Fig. 41, in this figure, a 10 GHz signal is used for calibration. These simulation results also show that self-calibration technique works, and it has a comparable performance with conventional PS in typical conditions and typical models. With using proposed technique, maximum rms phase error is reduced to 1.7° from 2.2°. There is not a large difference between two phase shifters, because this is the best conditions for the first phase shifter which uses *Static-LUT*.

Normally, phase shifters are designed for a target frequency band, and after fabrication it is not possible to change it. Fig. 42 is very important figure which proves that phase shifter can be recalibrated, using the proposed calibration system, for target frequency band. To the best of authors knowledge, this is a new capability to phase shifters. This capability has more impact especially in transmitter side. If user wants to use RADAR for transmitting the signals at 8GHz, user can recalibrate the phase shifter using an 8 GHz calibration signal and rms phase error. On the other hand, the bandwidth of the RADAR in X band, is not higher than 200 MHz, therefore shifting target frequency band in order of 1 GHz is enough for recalibration. In addition, this capability is still effective in receiver side, because RADAR receives the signals reflected signals, and the frequency of reflected signal will be close to the transmitted signal (in 1 GHz range). In figure Fig. 42, target frequency band is shifted through utilization of three calibration signals, Cal1, Cal2 and Cal3 which are at 9, 10 and 11 GHz, respectively. These simulation results also show that operation bandwidth of the phase shifter can be extended to 6.4 GHZ, using two different calibration signals at 9 and 11 GHz band.

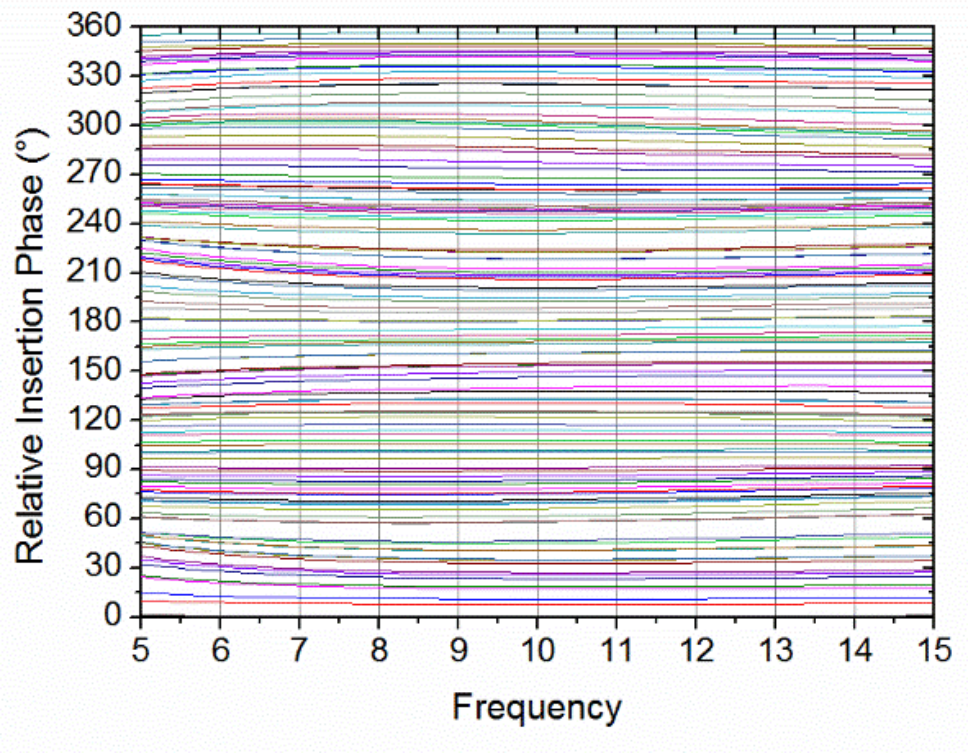


Fig. 40: Relative insertion phase response of phase shifter after calibration.

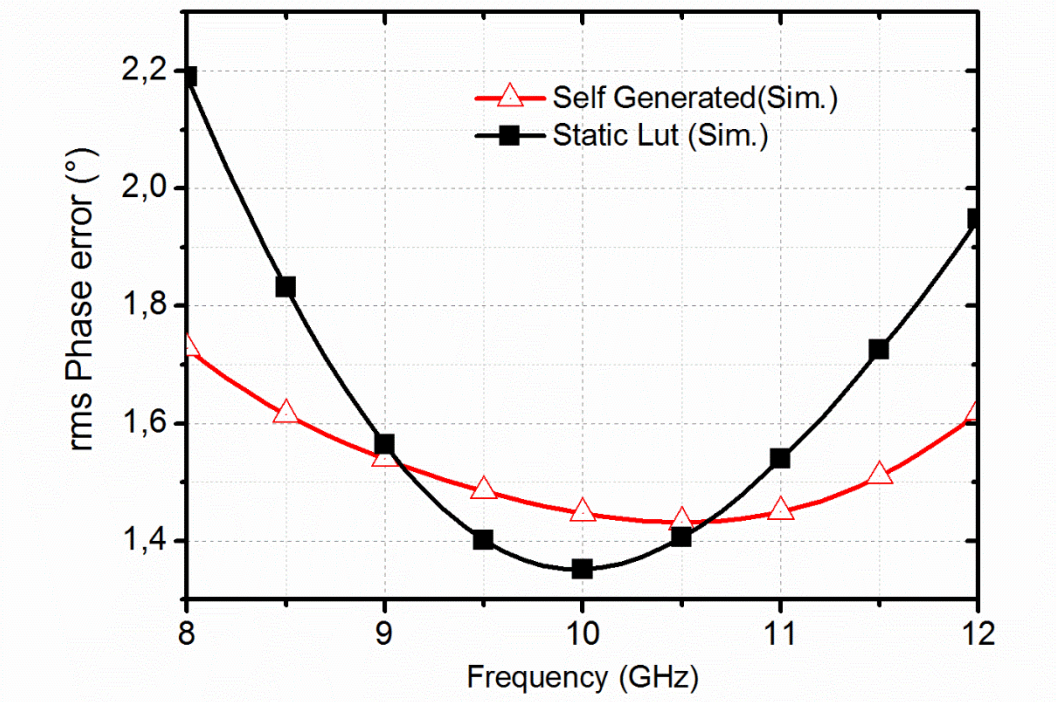


Fig. 41: rms Phase error of phase shifter with and without calibration for typical conditions.

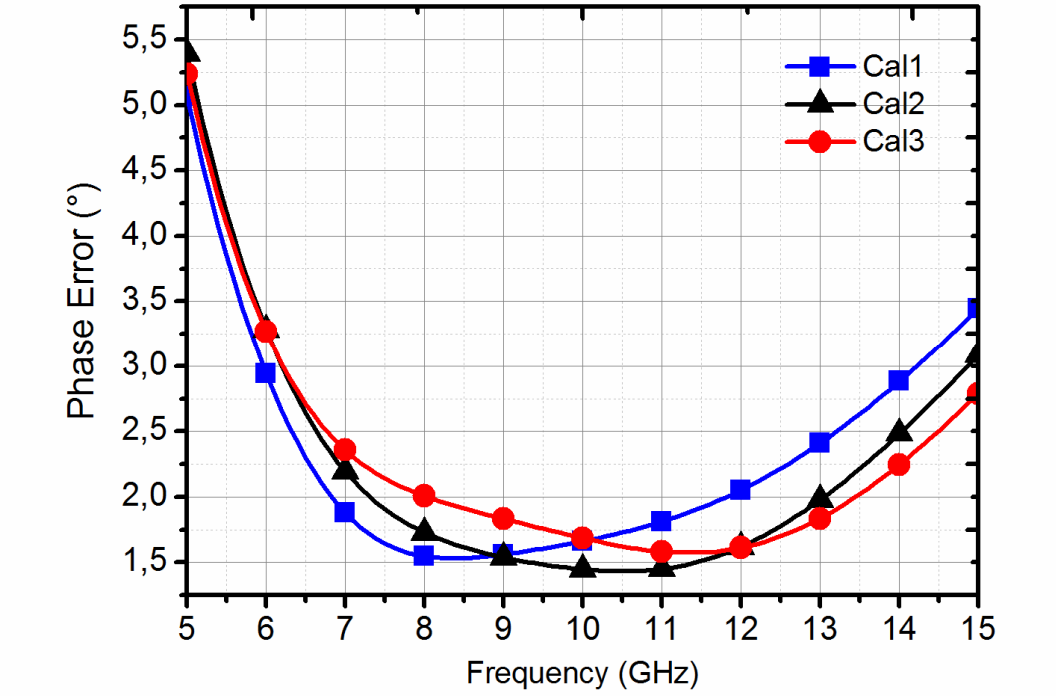


Fig. 42: Simulation results for the comparison of rms phase error of three calibrations. In Cal1, Cal2 and Cal3 calibration signals are sent at 9, 10 and 11 GHz, respectively.

In order to test the tolerance of proposed calibration technique on process variations, corner simulations have been applied and ocean script files have been written for this purpose. Previous simulations have been applied with typical models, and *Static-LUT* has been designed based on these typical models. As the first step of the corner simulations, the model libraries of resistors, capacitors, HBT and CMOS devices are changed to best case models. The simulations run again, in these conditions, maximum rms phase error of the phase shifter with *Static-LUT* increases to 3.38° (which was 2.2° in simulations with TYP model), as shown at Fig. 43. After applying proposed the calibration method, maximum rms phase error decreases to 2.76°.

As the second step of the corner simulations the model libraries of resistors, capacitors, HBT and CMOS devices are changed to worst case models. The simulations run again, in these conditions, maximum rms phase error of the phase shifter with *Static-LUT* increases to 2.38°. After applying the calibration method, the maximum rms phase error of the phase shifter which uses Self-generated LUT, decreases to 2.32°, as shown in Fig. 44. In the worst case corner, the variation from typical condition was not excessively high, and the device models are shifted in the same direction. For this reason, phase error performance of the phase shifter was not worsened further. However, the error of

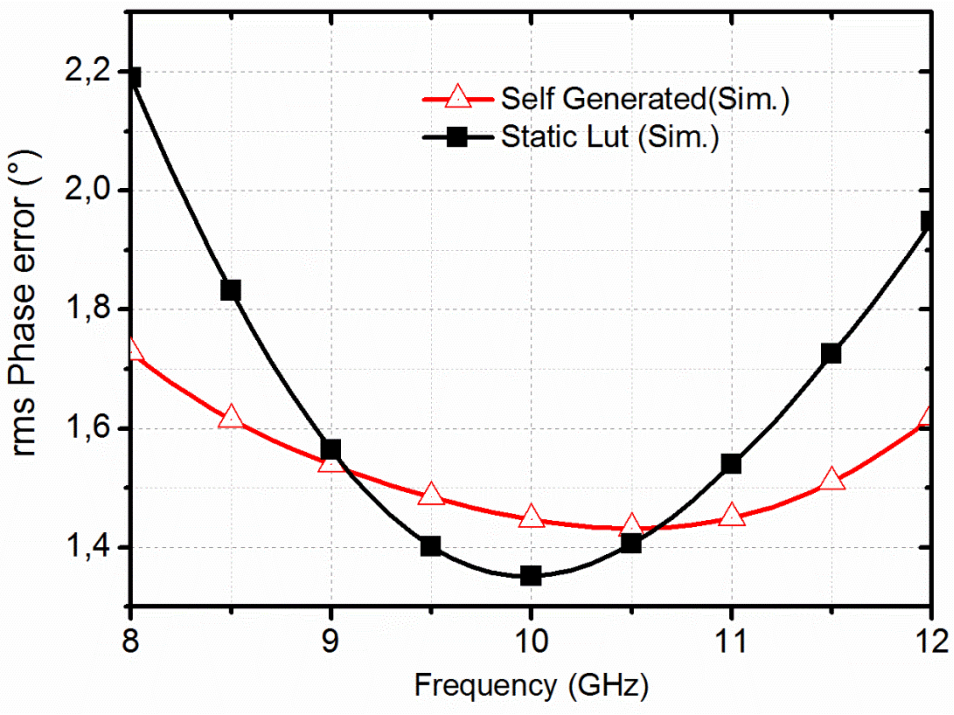


Fig. 43: Effect of the calibration on rms Phase error in process corners – Best Case.

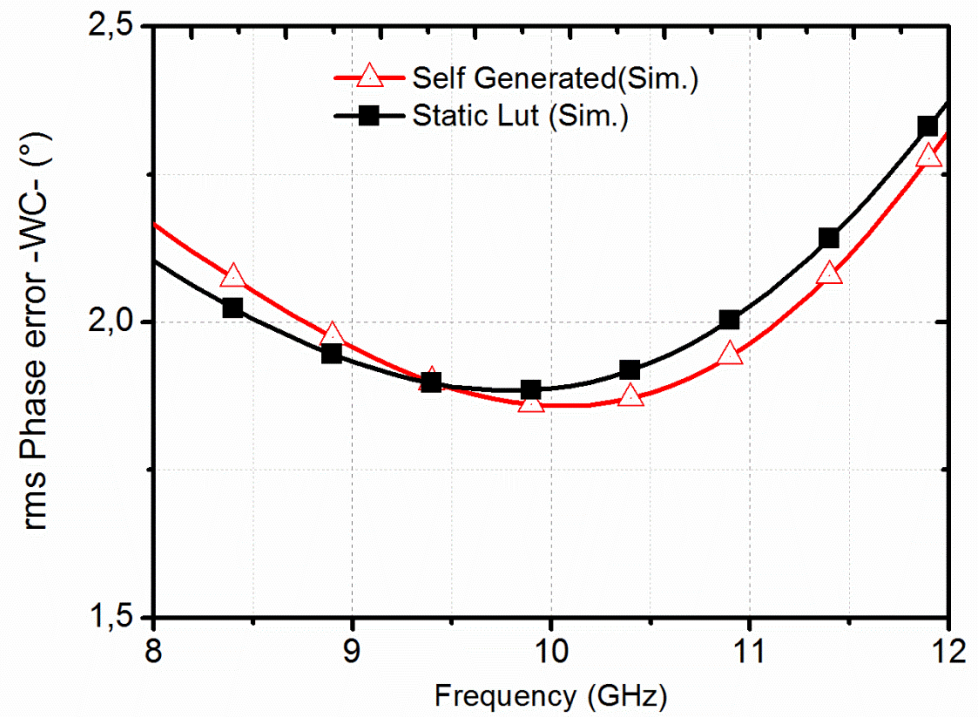


Fig. 44: Effect of the calibration on rms Phase error in process corners – Worst Case.

the power detector in this corner higher. Therefore, the compensation impact of proposed technique is not observed in this simulation. In consideration of analyzing the tolerance of phase shifter to temperature change, simulations have been applied and ocean script files have been written for this purpose. In previous simulations, temperature is set to 27 °C, and *Static-LUT* has been created in this temperature. In the simulations are applied at -40°C maximum rms phase error of the phase shifter with *Static-LUT* increases to 2.61° (which was 2.2° in simulations at 27 °C). After applying the proposed calibration method, the maximum rms phase error decreases to 2.5°, as shown at Fig. 45.

The proposed calibration method has more impact on higher temperatures. If the temperature is set to 85°C, and the simulations are applied, maximum phase error of the phase shifter with *Static-LUT* decreases to 2°, as shown at Fig. 46. After applying the calibration method, the maximum rms phase error decreases to 1.4°.

Corner simulations demonstrated in Fig. 43-Fig. 44, and temperature simulations in Fig. 45-Fig. 46 prove that using a self-calibrated circuit enhances process and temperature tolerations of a vector-sum based phase shifter.

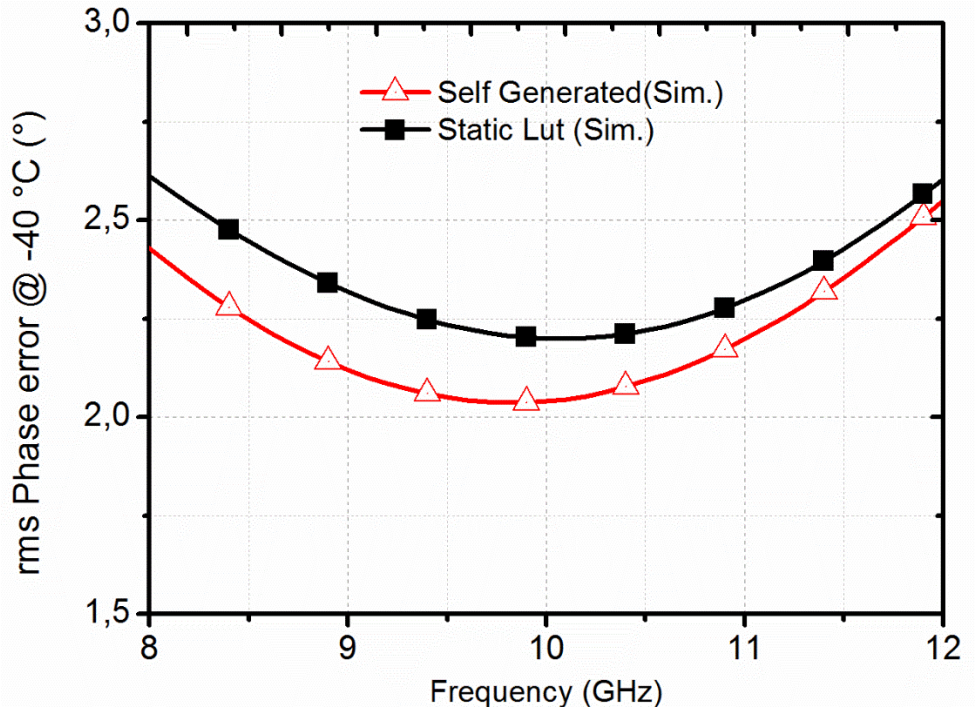


Fig. 45: Effect of the calibration for -40 °C.

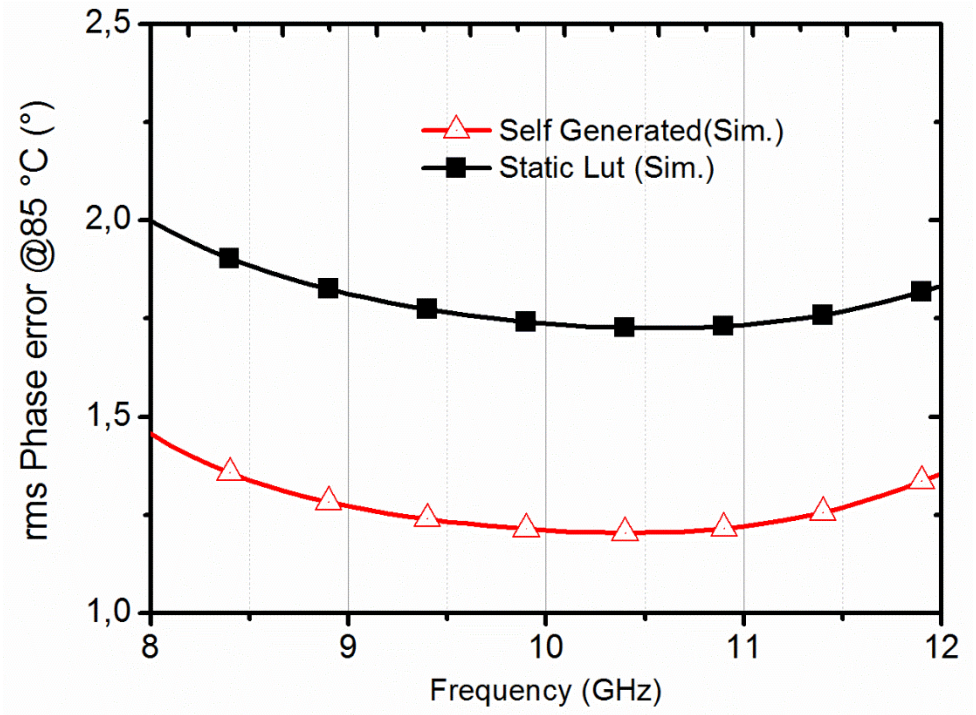


Fig. 46: Effect of the calibration for 85 °C.

A comparison of this work and the state of the art is illustrated in Table 12. Because of the flexibility of tuning the center frequency, operation bandwidth of the phase shifter is significantly extended. If the threshold of rms phase error is set to 2.8°, in which 7-bit operation is achieved, (after two recalibrations with using the signals at 9 GHz and 11 GHz) operation bandwidth will be 6.2-15 GHz, which corresponds 0.8 of fractional bandwidth. On the other hand, the target rms phase error specification for this phase shifter is 2°. Proposed phase shifter achieves this phase accuracy at 6.75 GHz to 13.5 GHz bandwidth, which corresponds 0.66 of fractional bandwidth. To the best of author's knowledge this is the highest fractional bandwidth for a phase shifter with phase resolution of 6-bit or higher in literature. Moreover, the resolution of proposed phase shifter is 7-bit which is the highest resolution in literature, to the best of author's knowledge. On the other hand, Proposed technique does not have additional static power consumption; However, power consumption instantaneously increases during calibration. Proposed technique increases insertion loss, and area of the phase shifter which is not a burden for T/R modules. To conclude, the proposed work is advantageous in terms of bit

Table 12: Comparison of simulation results of this work with state of the art phase shifters

Ref	Process	Design technique	Freq. GHz	Frac. BW	Ph. Err. (°)	Gain Err. (dB)	Gain (dB)	Phase range	OP1dB (dBm)	Area mm^2	Pow. mW
[51]	180 nm SiGe	Vector sum	6-18	1.00	5.6	1	18±1.5 **	360° (5 Bit)	-20	0.18	62**
[52]	130 nm SOI	Vector sum	23-23.4	0.06	2.8	0.5	14*	360° (6 Bit)	-15.00	0.87	45*
[53]	65 nm CMOS	Vector sum	50-66	0.28	11	1.7	-6	360° (4 Bit)	-2.00	1.60	30
SU RFIC [54]	250 nm SiGe	Vector sum	9 - 12	0.30	5	2	-5.00	360° (6 Bit)	-11.00	1.65	110
This Work*[1] (First prot.)	250 nm SiGe	Vector sum with self-calibration	6.2-15	0.8	2.8	1.6	-8.6	360° (7 Bit)	-11.00	2.6	110*[2] 233*[3]

*1: Based on simulation results
*2: After calibration
*3: During the calibration

resolution, phase error, and fractional bandwidth. The power and area consumption of the circuit is at an acceptable level.

5.2 Simulation Results of the Second Prototype

After the design of ADC and ALU, RF and baseband building blocks are combined. As depicted at Fig. 47, the difference between the second prototype and the first prototype is the completely integration of baseband blocks with RF circuits. The second version is important to demonstrate the feasibility of completely integrated version of proposed idea which will be used in phased array radar systems. Final layout of the self-calibration circuit is depicted at Fig. 48, the final area of the circuit is 2.1mm × 2.1 mm. The circuit is sent to fabrication at January 2016.

In simulations of the second prototype, the techniques which are described at section 5.1 are applied. The only difference is rather than using the behavioral model of ADC, post layout simulation results of integrated ADC are utilized. Relative insertion phase of the second prototype is presented at Fig. 49. The calibration circuit could not generate the phases at following intervals: 55° - 75°, 168°-188°, 260°-276°, and 346°-357° because

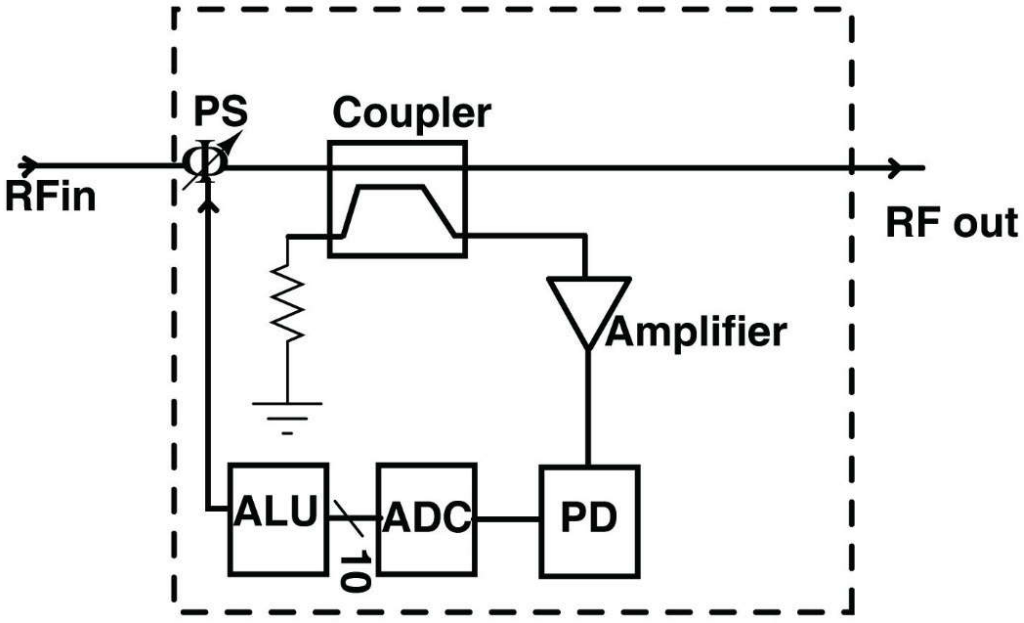


Fig. 47: Block diagram of the second prototype consisting of completely integrated RF and baseband building blocks.

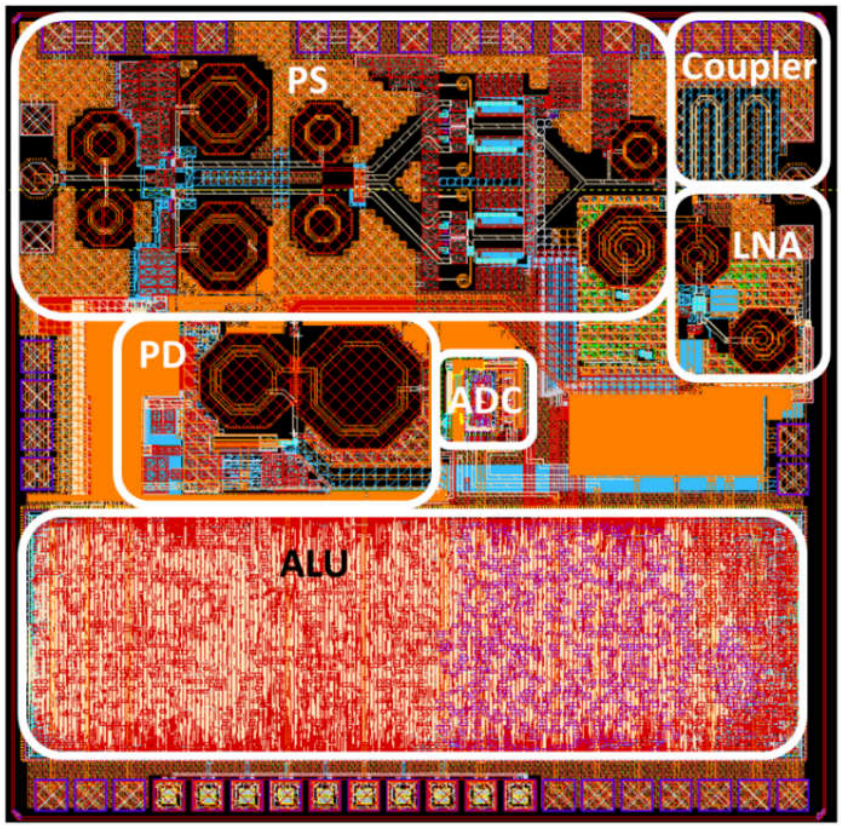


Fig. 48: Layout of the final circuit.

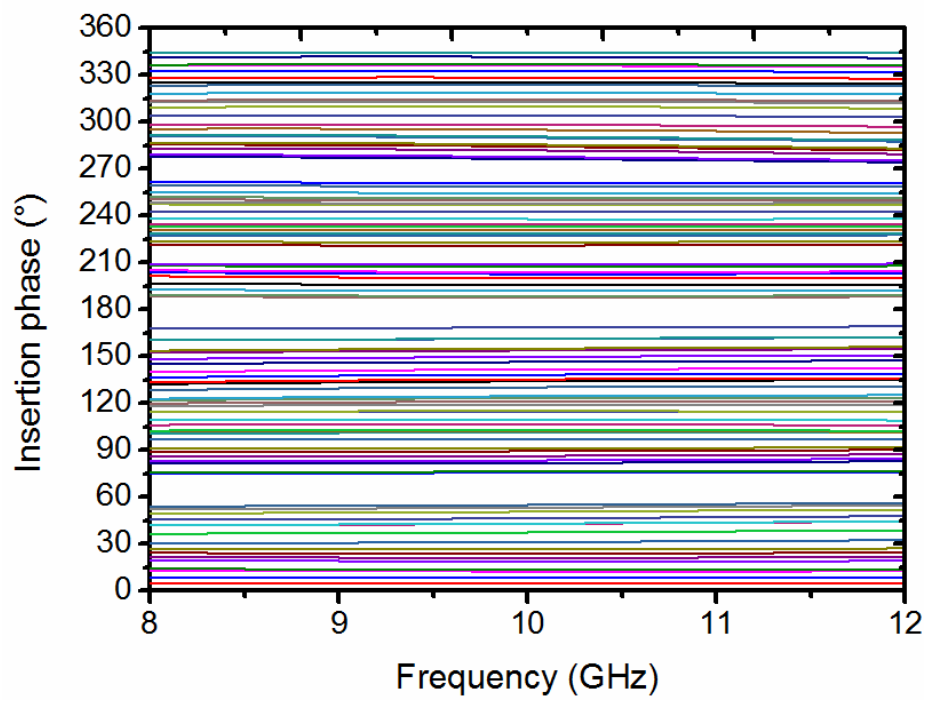


Fig. 49: Relative insertion phase for the second prototype.

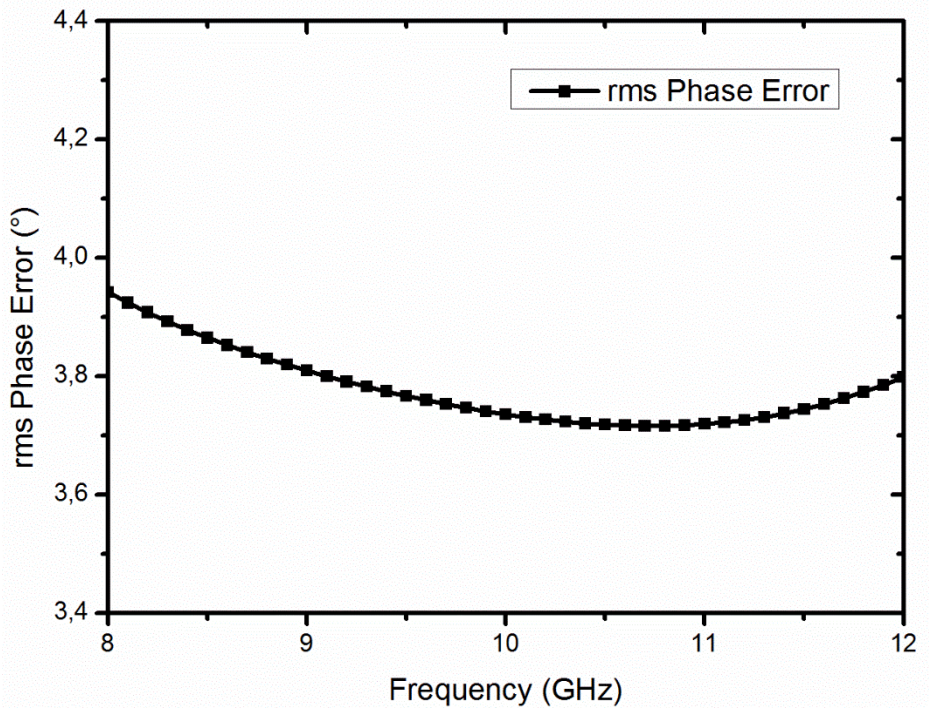


Fig. 50: RMS-phase error for the second prototype.

of the following reasons coming from ADC design. Input voltage range of the ADC is very high (0.5V-4V), and significant conversion errors occur for the input voltages which are very close to negative and positive reference voltage. Secondly, power detector is single ended, for simplicity single ended ADC design is preferred. However, the circuit suffers from clock feed-through which generates conversion errors. In addition to these errors, the mismatch at the input of comparator is also significant. These conversion errors, returns as measurement errors especially for very small and very large vector sizes. Because of these reasons, accuracy of the phase shifter is reduced, and maximum RMS-phase error is increased to 3.9° as shown at Fig. 50.

5.2 Measurements of the first prototype

The first prototype consisting of PS, Coupler, LNA and PD is fabricated in 0.25 µm SiGe BiCMOS technology. The micrograph of the chip is shown in Fig. 51, which occupies 2.04mm × 1.3 mm including all the pads. On wafer S parameter measurements of the core chip have been done using both R&S ZVL and Agilent 8720ES Network Analyzer. On the other hand, Agilent 8267D Vector Signal Generator is used for generation of single tone signal during the calibration. Measurement plan and measurement setup of the first prototype are depicted at Fig. 52 and Fig. 53, respectively.

As it is stated previously, power detector operation range is higher than 52 dB; however, its linear operation range is around 35 dB. On the other hand, maximum vector power is 30 dB higher than the minimum vector power. All possible vector powers must be in the linear operation range of the power detector; therefore, input signal power has significant role during the calibration. Moreover, optimum bias points of the active BALUN and VGA of the phase shifter are significantly different from the post-layout simulations.

During the optimization of bias points of active BALUN, first of all, FPGA is programmed to generate reference quadrature vectors. At target center frequency, (10 GHz) bias points of the BALUN is optimized to provide minimum phase and amplitude errors for these reference quadrature vectors. Measurement of the first prototype is completed after optimization of bias points and signal power at signal generator. During measurements -11.5 dBm of signal is applied.

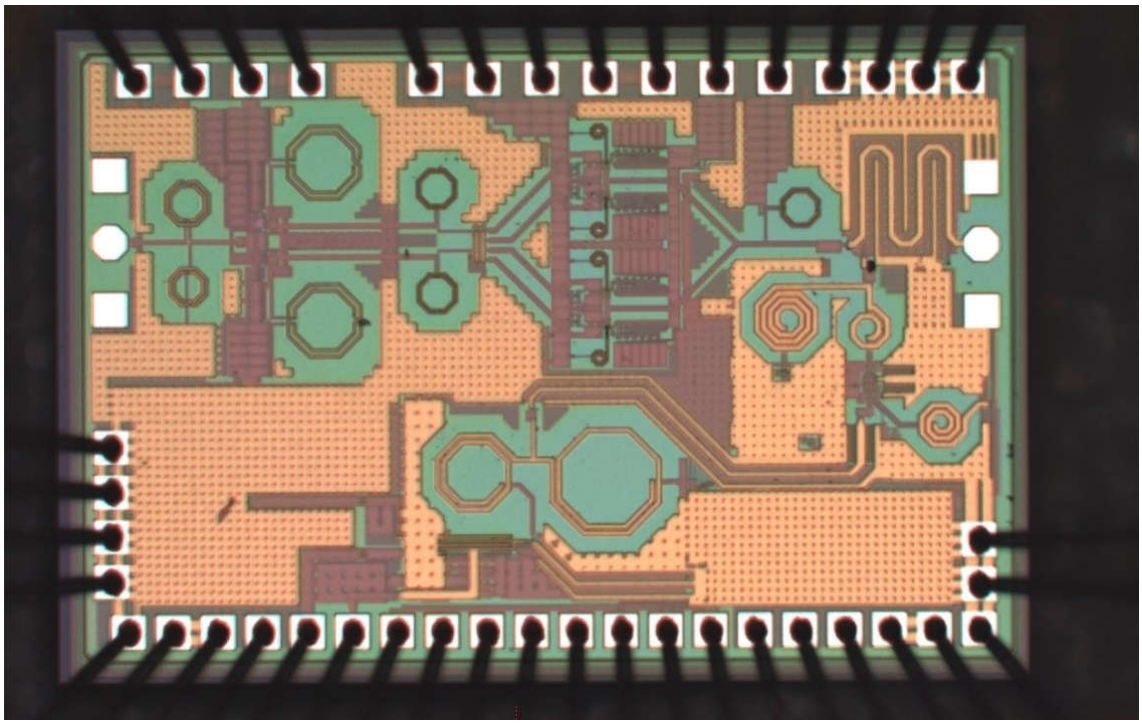


Fig. 51: Die photo of the first prototype consisting of Phase shifter, coupler, amplifier and power detector.

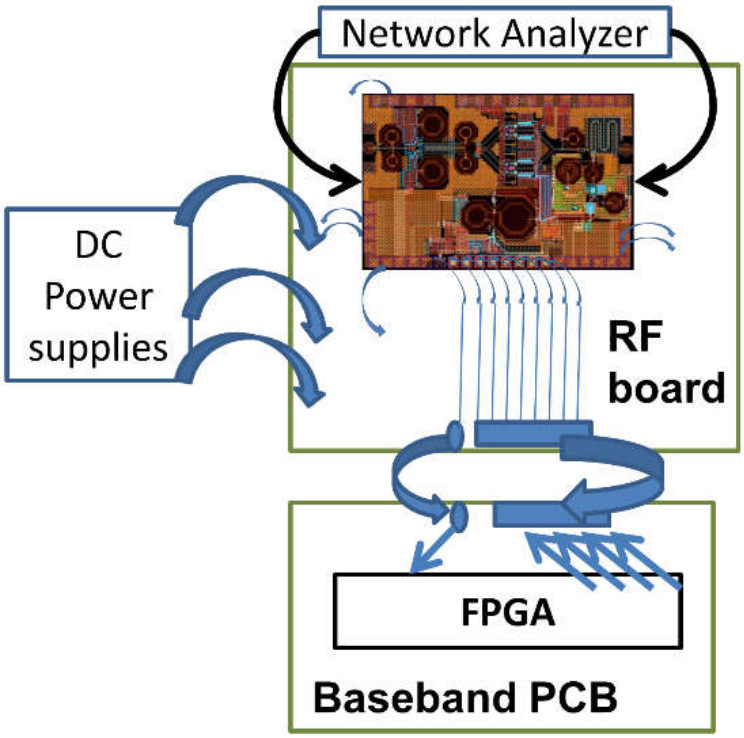


Fig. 52: Measurement plan of the first prototype.

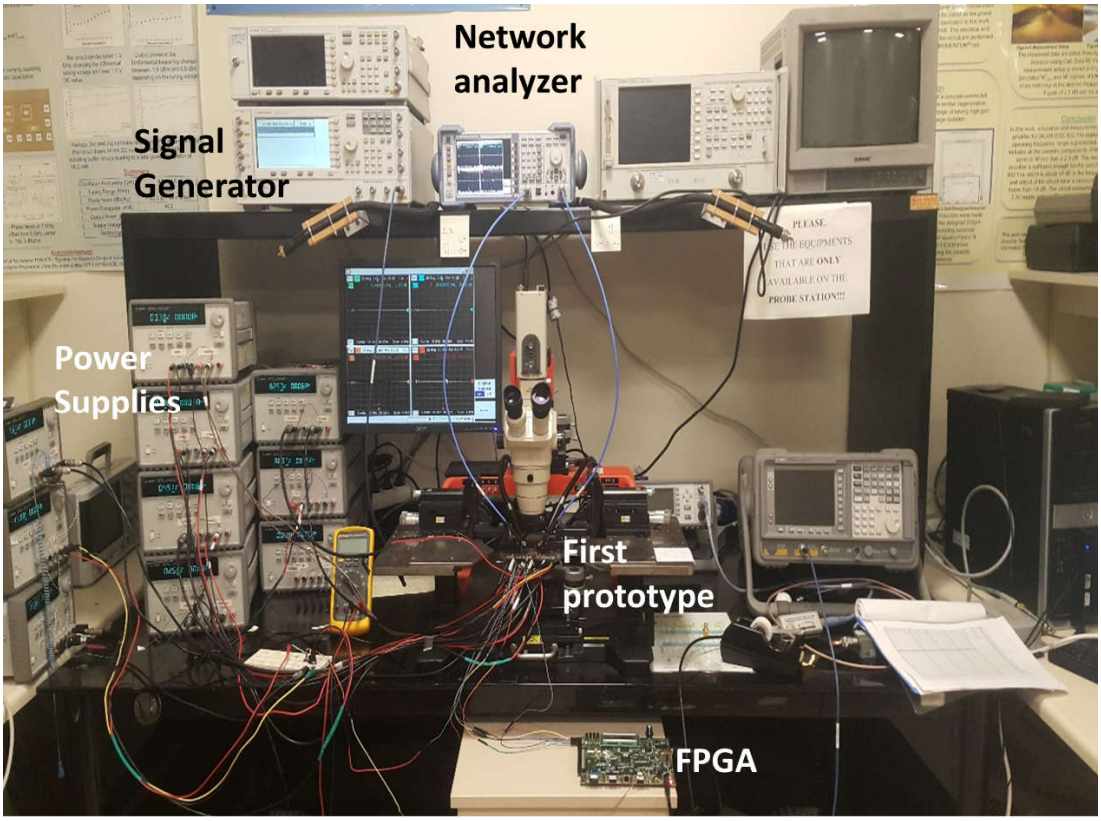


Fig. 53: Measurement Setup.

Relative insertion phase response of the PS without calibration, (with using *Static-LUT*) is presented in Fig. 54. As shown in this figure, most of the phases overlap and excessive number of phase states are not obtained. After calibration, (with using *Self-Generated - LUT*) relative insertion phase response is shown in Fig. 55. Most of the missing phase states are recovered as shown in this figure. However, because of the following reason, some of the missing states cannot be generated with this technique, that is why there are some empty places at Fig. 55, especially around 75°, 165°, and 320°. The algorithm of the proposed DPU is based on keeping one of the vector size at maximum, and sweeping the other vector. In other words, these missing states can be explained referring to the expression (48) in third chapter,

$$RF_{out} = G_1 I^+ + G_2 Q^+ + G_3 I^- + G_4 Q^- \tag{70}$$

For instance, during searching the correct vector pair for 75°, G_2 in (70) is kept maximum, and the algorithm searches the optimum G_1 value. However, these missing phase states, for instance the phase states around 75°, requires two vectors such that both of them are not at maximum amplitude.

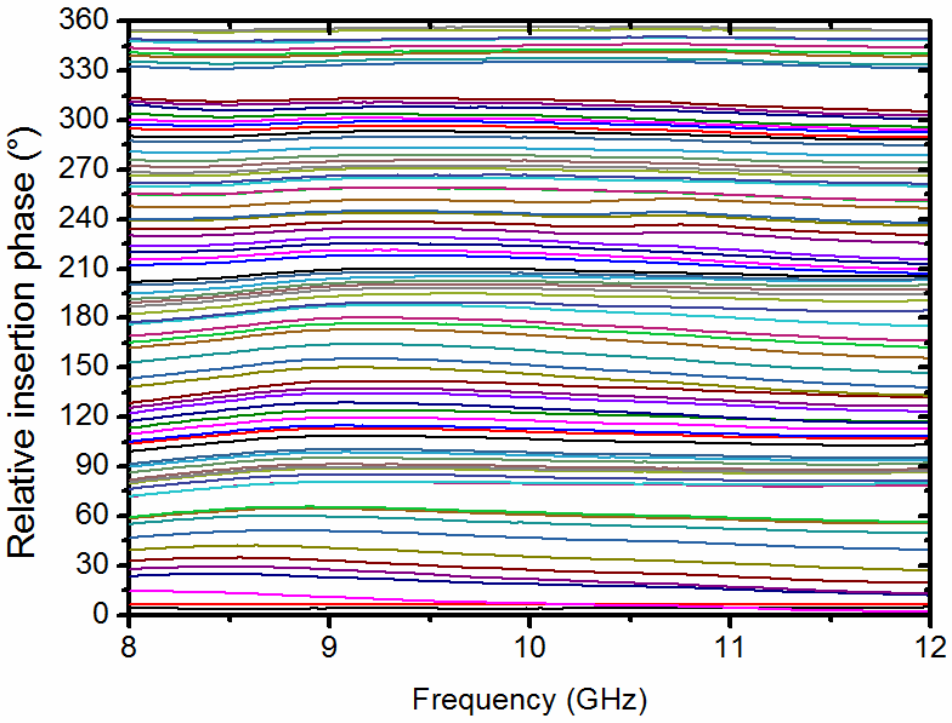


Fig. 54: Measured relative insertion phase response of PS with *Static LUT* which is based on post layout simulation results.

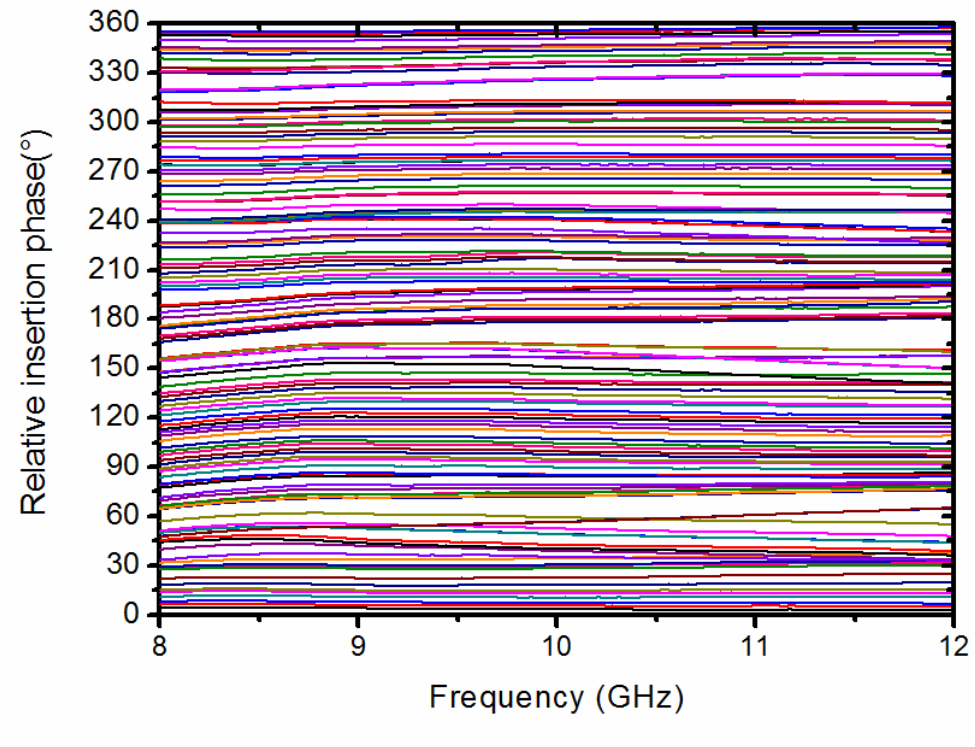


Fig. 55: Measured relative insertion phase response of PS after calibration.

Phase performance of a phase shifter is better represented with rms-phase error graphics, which is demonstrated in Fig. 56. As shown in this figure there is a significant difference between simulation results and measurement results of the phase shifter without calibration (*Static LUT*) because of the following reasons. First of all, the phase insertion effect of the VGA dominates the error in center frequency (10GHz). This behavior of VGA is dependent to junction capacitances, which are not perfectly modeled in CAD tools. In addition, these junction capacitances are strictly dependent to the process parameters. Model inaccuracies have also significant effect on this error.

Secondly, the amplitude and phase mismatch of active BALUN and I-Q generator, dominates the error in edge frequencies (8 and 12 GHz). This mismatch is minimum at center frequency, and maximum in the edge frequencies. Especially, simulation results show that CB-CE selection based BALUN has less than 2° of phase error in entire bandwidth; however, in measurements this error increases up to 22° in corner frequencies, because of the inaccurate modeling and process variations. As a consequence of these errors, rms- phase error is increased up to 5° at 8 GHz.

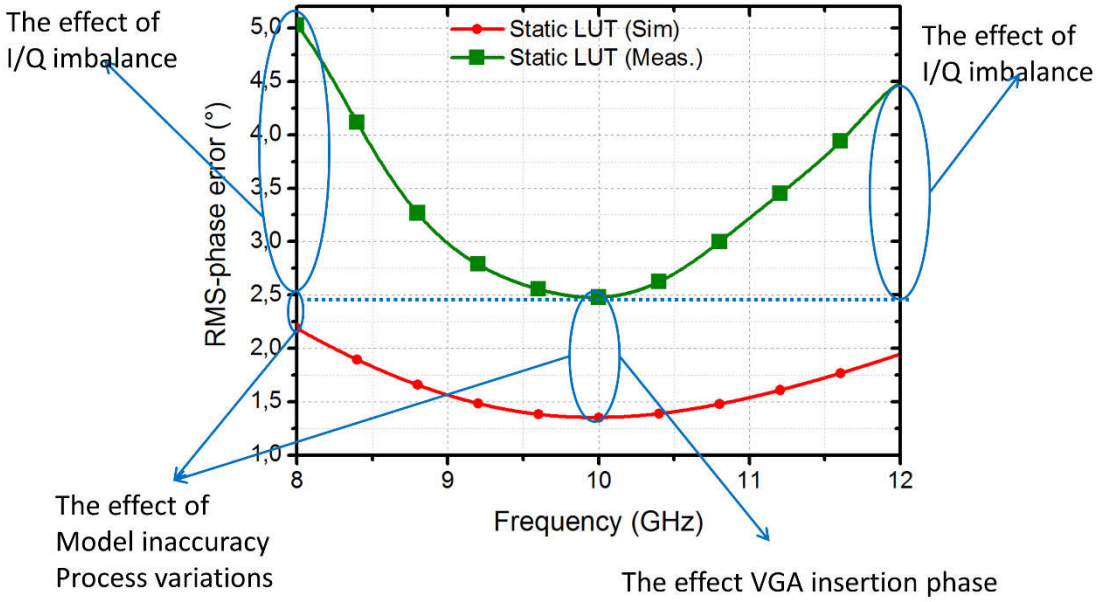


Fig. 56: Comparison of simulation and measurement results of phase shifter with *Static LUT* which is based on post layout simulation results.

In proposed technique (*Self-Generated* curves in Fig. 57), a smart way of vector pair selection is applied after fabrication, therefore these errors are necessarily compensated. As shown in Fig. 57, the effects of VGA insertion phase due to process variations and model inaccuracies are minimized. Rms phase error is decreased to 1.6° from 2.5° at center frequency. In addition, because of using proper vectors, phase error in corner frequencies are also reduced. Rms phase error at 8 GHz is reduced to 2.35° from 5°, and maximum phase error at 12 GHz is reduced to 2.95° from 4.95°.

Chip to chip variation of proposed technique is represented in Fig. 58. In this figure, the variation is minimum in center frequency and maximum in corner frequencies. In these measurements, during calibration, single tone signal at 10 GHz is applied; therefore, the calibration circuit is very successful in compensation of the error in center frequency. However, in corner frequencies, the process variation of BALUN and I-Q generator is dominant, that is why, in the second chip the rms phase error is increased to 3.4° in 8 GHz, and 3.8° in 12 GHz. In order to compensate effects of the process variation, amplitude and phase mismatch of BALUN at 8 GHz, (assuming RADAR is operating around 8GHz) user can recalibrate the phase shifter through applying the calibration signal at 8 GHz, and reduce phase error, as represented at Fig. 59.

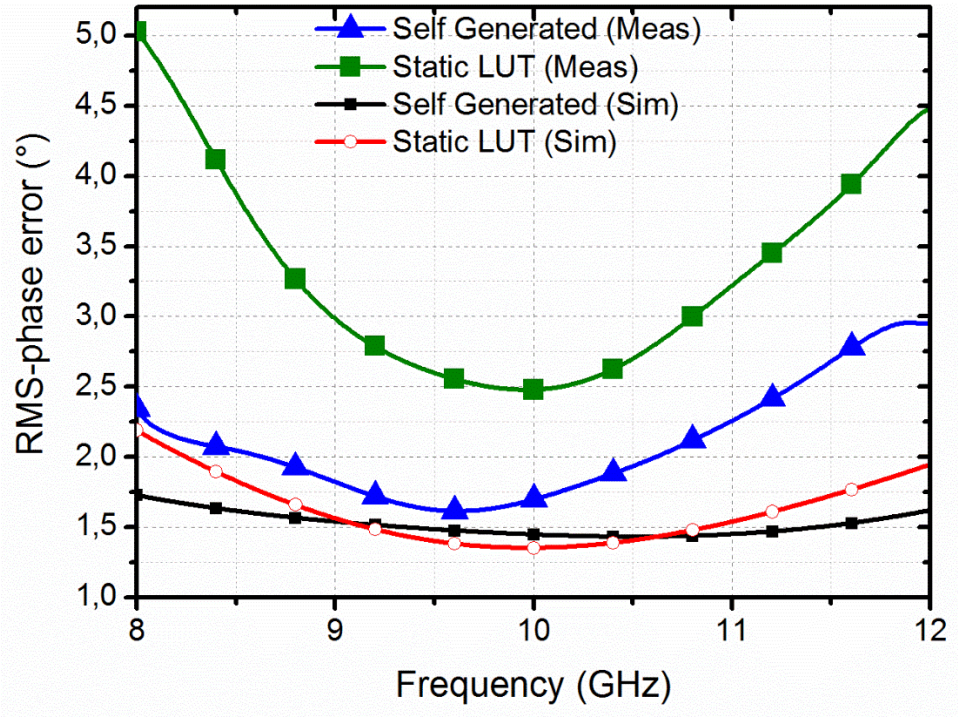


Fig. 57: Comparison of rms phase error simulations and measurement results of phase shifters. *Static LUT* curves represent the results of the phase shifter with a LUT which is based on post layout simulation results. *Self-Genereated* curves represent results of the proposed technique.

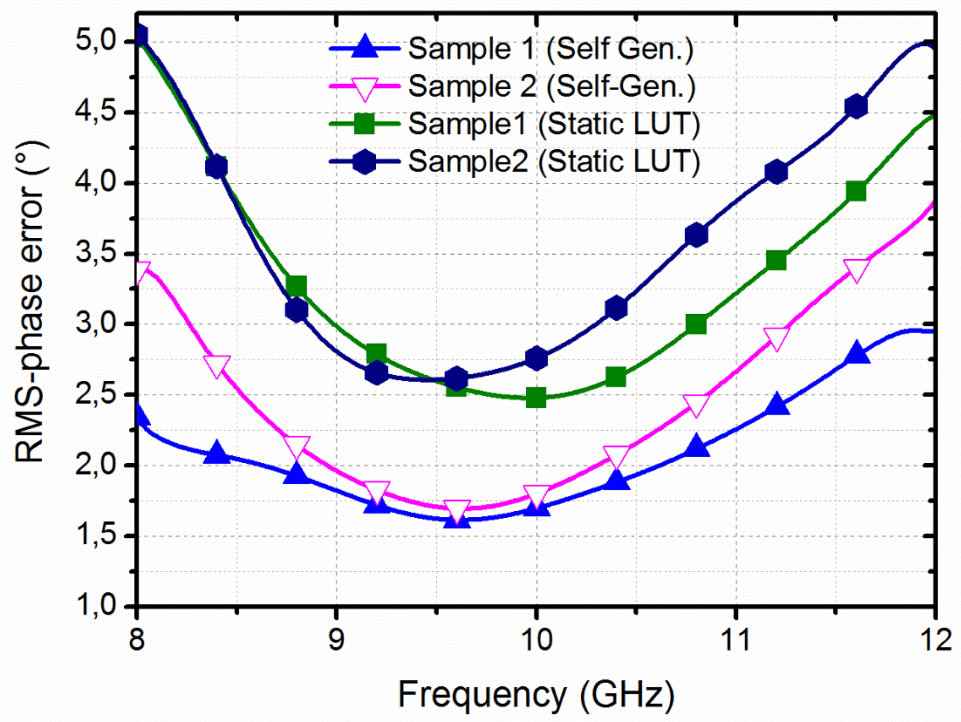


Fig. 58: rms phase error measurement results for different dies.

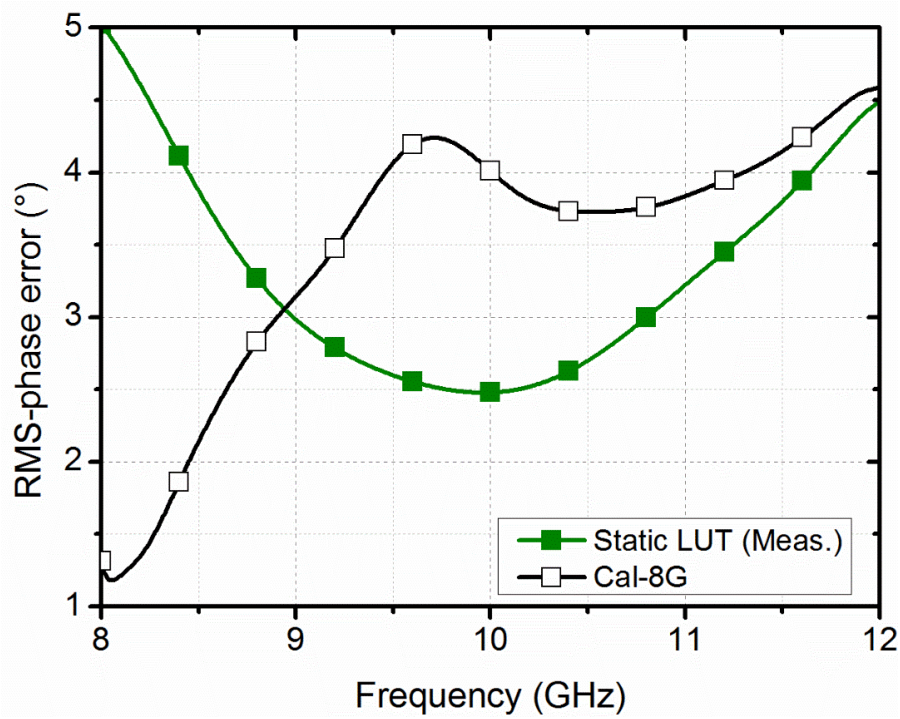


Fig. 59: The effect of I/Q phase-amplitude imbalance can be compensated through the recalibration at corner frequencies.

One of the most important functionality of this technique is the reconfigurable center frequency. User can reconfigure and regenerate LUT for different frequencies through applying the single tone calibration signal at the target frequency. As it is previously declared that, to the best of authors knowledge, this is a new competence to phase shifters. Particularly for transmitter applications this competence has more effect, because the user knows transmit frequency, and recalibrate the phase shifter for this frequency. In active RADAR applications, object is illuminated with the transmitter, and receives reflected signals. Assuming received signal frequency is very close to the frequency of transmitted signals, this competence has still important impacts in receiver applications.

Results of the recalibration at four center frequencies are illustrated at Fig. 60. If we apply the calibration signal at 8 GHz, rms-phase error reduces to 1.3° from 5°. It is not required to send the calibration signal exactly target frequency, for instance, if we apply the calibration signal at 11 GHz, rms-phase error at 12 GHz reduces to 2.2°. The operation bandwidth of the phase shifter can be extended with recalibration. Three recalibrations with three signals respectively at, 8GHz, 10GHz and 11 GHz extends the operation bandwidth to more than 4 GHz in which rms phase error is lower than 2°.

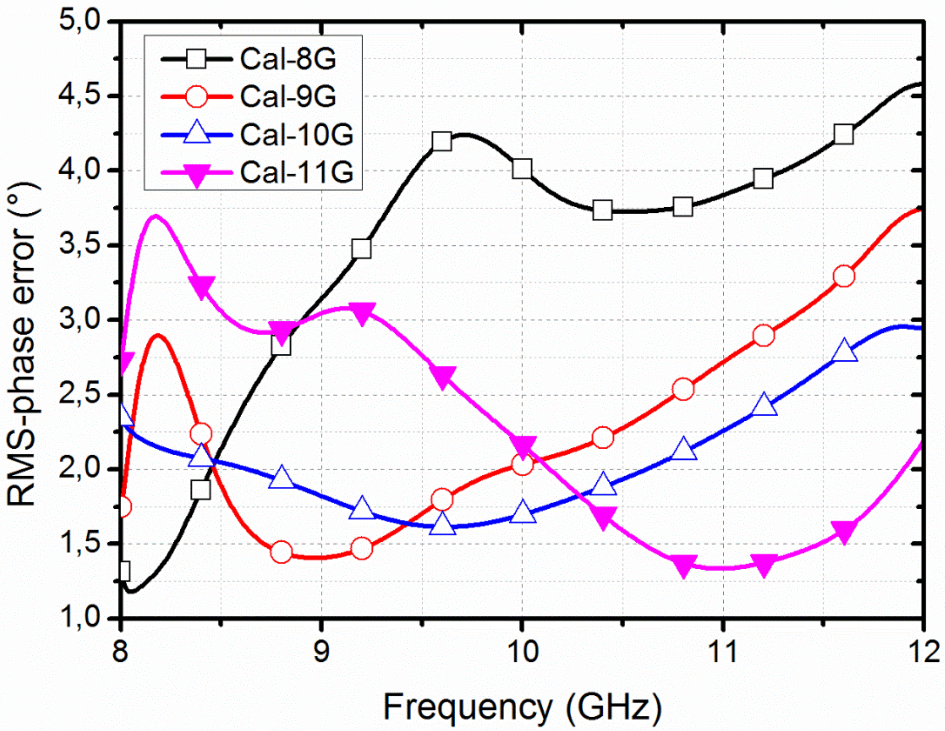


Fig. 60: Measurement results for the comparison of rms phase error of four calibrations. Proposed technique enables flexibility of tuning the center frequency.

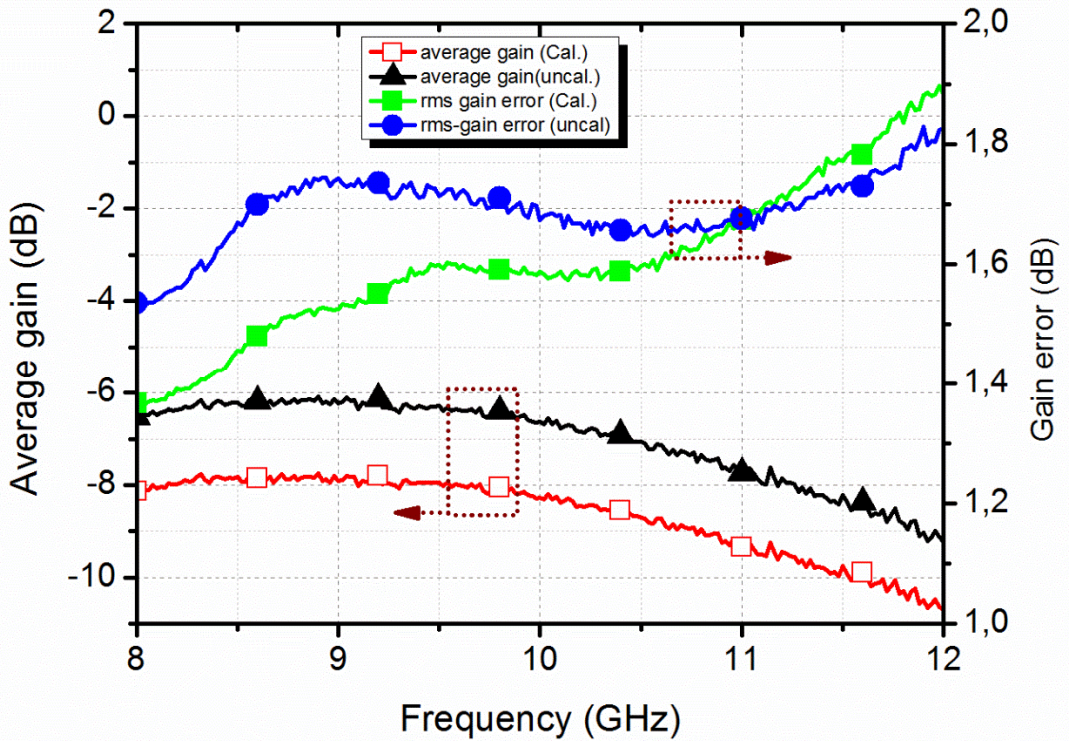


Fig. 61: Average gain and rms gain error measurements of phase shifter.

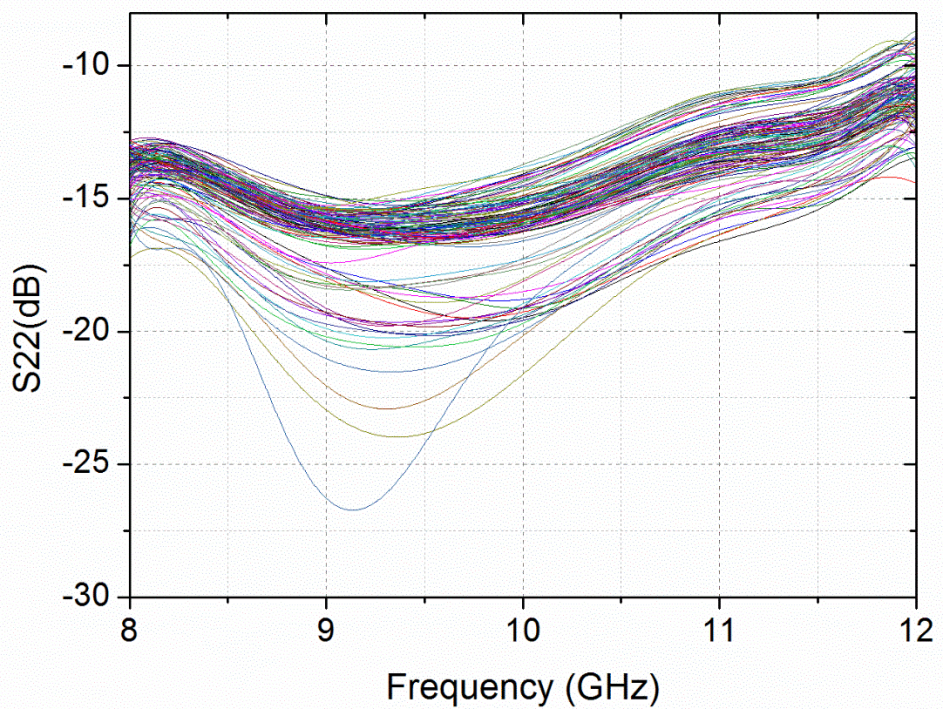


Fig. 62: Output return loss of proposed technique for 128 phase states.

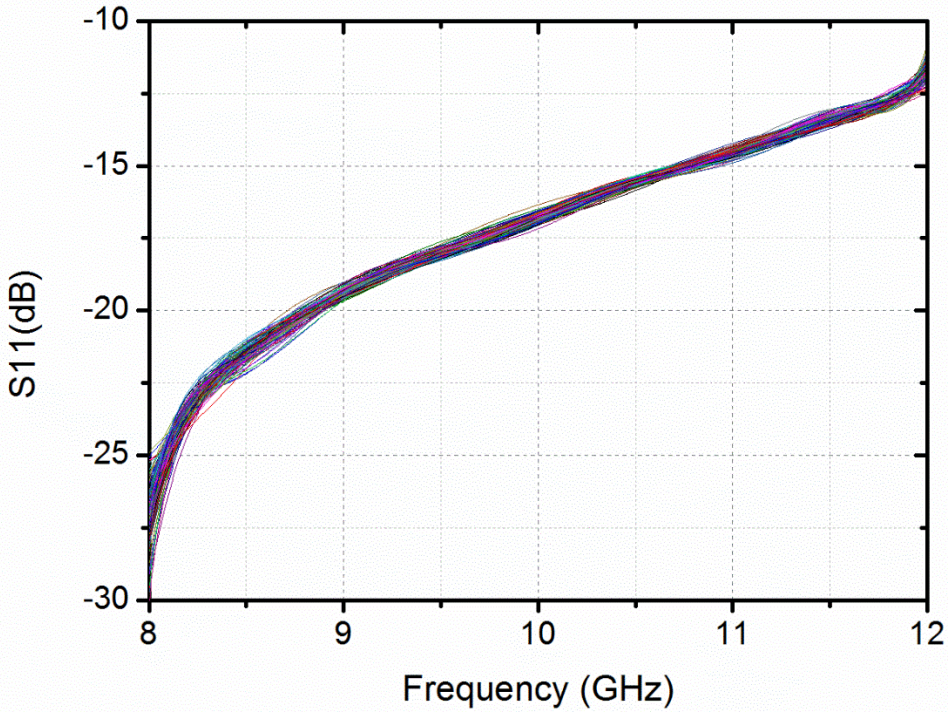


Fig. 63: Input return loss of the proposed technique for 128 phase states.

The drawback of the proposed technique is the increase of insertion loss. Fig. 61 shows measured average loss and rms loss error. Proposed calibration technique increases the insertion loss around 1.6 dB in average, due to utilization of the coupler. The average loss is around 8.6 dB, rms gain error is around 1.6 dB. Proposed calibration technique also enables to control the amplitude of phase shifter. User can minimize amplitude error with the cost of phase error. On the other hand, input and output return loss is higher than 10 dB, as shown in Fig. 62 and Fig. 63.

Benchmark of measurement results of this work with the state of the art PS is shown in Table 13. First of all, the resolution of proposed PS is 7-bit which is the highest resolution in literature, to the best of author's knowledge. Secondly, because of the adaptable center frequency competence, this phase shifter with proposed calibration technique, has the ability of operating in a wide bandwidth. Proposed phase shifter achieves target phase accuracy (RMS<2 °) at 8 GHz to 12 GHz bandwidth, which corresponds 0.25 of fractional bandwidth. To the best of author's knowledge, this is still the highest fractional bandwidth for a phase shifter with phase resolution of 6-bit or higher in literature. On the other hand,

Table 13: Benchmark of measurement results of this work with state of the art phase shifters

Ref	Process	Design technique	Freq. GHz	Frac. BW	Ph. Err. (°)	Gain Err. (dB)	Gain (dB)	Phase range	OP1dB (dBm)	Area mm^2	Pow. mW
[51]	180 nm SiGe	Vector sum	6-18	1.00	5.6	1	18±1.5 **	360° (5 Bit)	-20	0.18	62**
[52]	130 nm SOI	Vector sum	23-23.4	0.06	2.8	0.5	14*	360° (6 Bit)	-15.00	0.87	45*
[53]	65 nm CMOS	Vector sum	50-66	0.28	11	1.7	-6	360° (4 Bit)	-2.00	1.60	30
SU RFIC [54]	250 nm SiGe	Vector sum	9 - 12	0.30	5	2	-5.00	360° (6 Bit)	-11.00	1.65	110
This Work*[1] (First prot.)	250 nm SiGe	Vector sum with self-calibration	8-12	0.8	2.8	1.6	-8.6	360° (7 Bit)	-11.00	2.6	110*[1] 233*[2]

*1: After calibration *2: During the calibration

proposed technique does not have additional static power consumption; however, power consumption instantaneously increases during calibration. Proposed technique increases insertion loss, and area of the phase shifter which is not a difficulty for T/R modules.

6 CONCLUSION and RECOMMENDATION of FUTURE STUDIES

Over the last decade, a continuously growing effort has been shown on phased array RADAR. The primary concern is to increase phase resolution, which dictates the accuracy of antenna beam direction and side-lobe level. Particularly, in consideration of silencing unwanted signals, tracking operations require high antenna directivity and low side-lobe levels. For instance, when tracking an enemy aircraft, RADAR must be immune to jamming signals of another enemy aircraft coming from a different direction. For this immunity, highly directive phased arrays are required. Phase resolution and directivity are determined by Phase Shifters, which makes them essential items for phased arrays. On the other hand, RADAR must operate at different temperatures without performance degradation. Therefore, the PS must have high tolerance to temperature variations. Moreover, phased arrays consist of thousands of T/R modules; for this reason, chip to chip, performance variation of PS must be as small as possible.

During my PhD study, I have worked on design of a HP/LP switching based 4-bit passive phase shifter [50]. In addition, I have designed a 4-bit phase shifter with distributed active switches [47], [79], Vector Sum type active phase shifter with analog control [56], and Vector Sum type active phase shifter with 6-bit digital control [54]. From these designs and the literature review given in second chapter, I have come to the conclusion that, in the class of the PS design techniques, vector sum is the most preferable one which provides the lowest insertion loss and area and phase error; as well as the highest operation bandwidth. However, in vector sum type PS, it is not possible to create two signals with 90° out of phase without amplitude and phase errors in a wideband operation. In addition, variable gain amplifiers are utilized to control amplitude of the vectors, and they cause additional phase error. Moreover, both I/Q vector generation circuits and amplitude control circuits have less tolerance to process and temperature variations.

Starting from the basic signal processing principles, phase shift function of a vector sum type PS is derived. It is also shown that phase shift of this type of PS can be estimated through the measurement of amplitudes of reference vectors.

For the sake of dealing with challenges of vector sum type PS, as the primary novelty, self-measurement and recalibration of the phase shifter is proposed in this thesis. In order to estimate the phase shift, amplitudes of the I, Q and Sum vectors are measured with a power detector. As the second novelty in this thesis, a new design technique is proposed for power detector circuit design (cascode configuration with diode connected PMOS load). Starting from the basic instantaneous voltage current definitions for the transistor, output voltage of proposed power detector is derived for a given input signal amplitude. The impact of this circuit is shown in theoretical explanations, and verified with measurements. Proposed power detector achieves highest dynamic range in literature, with a competitive linearity performance.

Proposed self-measurement and recalibration technique consists of an ADC which converts the amplitude information to digital domain. As the third novelty in this thesis, phase shift is calculated through the cosine formula using an embedded DPU. After the calculations of phase shift for all possible vector pairs, optimum control signals of phase shifter are recorded in a LUT, which is a 24×128 register array.

By using this self-calibration technique, first of all, it is intended to decrease the I/Q amplitude and mismatch because of on-chip measurement. Secondly, during the on-chip phase estimation, VGA phase error is also taken into account, therefore its effect is also reduced. As the third impact of this self-calibration technique, it is aimed to increase the tolerance on process variations, through the generation of LUT after fabrication. As the fourth impact, an increase of the tolerance on temperature change is targeted because LUT is produced at operating temperature, and recalibration of the circuit is possible after the temperature change.

In order to test the feasibility of the idea, a matlab script is written. In this script, VGA phase error (after post layout simulations) is imported, and optimum vector pairs are

selected. Measurement sensitivity and quantization error are also taken into account. The results show that, maximum phase error is lower than 2.5° and rms phase error is lower than 1.1° which is sufficient for 7-bit phase shifter design.

The first prototype consisting of integrated PS, coupler, LNA and PD has been designed using Cadence® and Sonnet®. Modelsim® is used for design and simulation of PDU. Synopsys® is used to synthesize, and Encounter® is utilized for place and route of the digital circuits. Simulation results shows that, after calibration maximum rms phase error is reduced to 1.7° from 2.2° in 8-12 GHz. It is shown that circuit can be recalibrated for target frequency band. Using three calibration signals, operation bandwidth is extended to 6.8 GHz. Corner simulations are also applied, which demonstrate that, the tolerance on process variation increases through the proposed calibration. As a result of using this technique, phase shifter accuracy is increased and rms-phase error is compensated up to 0.64°. Simulations are applied at different temperatures such as -40 °C, 27 °C, and 85°C. The results of these simulations underline the impact of this calibration technique on temperature change such that precision of the phase shifter is enhanced and rms-phase error is reduced as far as 0.54°.

The proposed method has been proven with experimental results. The first prototype consisting of integrated PS, coupler, LNA and PD has been designed and fabricated. In order to obtain the functions of ADC and DPU, FPGA is connected to the first prototype at the board level. Measurement results prove that, proposed method reduces phase error and increases the accuracy of the PS because of the following reasons. First of all, proposed method compensates VGA phase error at target frequency. In consideration of testing this impact, using a single tone signal is applied at 10 GHz. In this frequency, amplitude and phase imbalance of BALUN and I-Q generators are minimum and VGA phase error dominates. After the calibration, rms-phase error is reduced to 1.6°, which was 2.5°.

Secondly, proposed method compensates the phase and amplitude imbalance of the vectors. In order to test this impact, the calibration signal is applied on 8 GHz. The phase shifter is designed to operate in 8-12 GHz band, and maximum phase and amplitude

imbalance occurs at corner frequencies, and phase error increases to 5°. After the calibration, the phase error at 8 GHz is reduced to 1.3°.

Moreover, proposed method compensates the process variations. In order to test this impact, two chips have been measured, and chip to chip variation of rms phase error at calibration signal frequency is negligible (0.1°). In addition, compensation of VGA phase error also shows that, proposed method reduces the effects of process variations. Because, VGA phase error is dependent to junction capacitances that are susceptible to the fabrication and process variations.

One of the most important functionality of this technique is the reconfigurable center frequency. User can reconfigure and regenerate LUT for different frequencies through applying the single tone calibration signal at the target frequency. Operation bandwidth of the phase shifter can be extended more than 4 GHz, in which rms phase error is lower than 2°, through three recalibration using three signals respectively at, 8GHz, 10 GHz and 11 GHz.

The research on this topic can continue on design of a smarter DPU. In the algorithm of the proposed DPU, size of one of the vector is kept at maximum, and the size of other vectors are swept. However, with this technique some of the phase states cannot be generated which requires both of the vector amplitudes are lower than maximum. In order to generate these phases, the algorithm of the DPU can be improved in searching the other vector amplitudes.

Second improvement on the digital circuit, can be the extension of LUT. In current version, only one tone of the calibration signal can be applied during calibration, and LUT for this target frequency is recorded in one LUT. If target frequency band changes, circuit has to be recalibrated. The algorithm can be improved such that, more than one calibration can be applied consecutively, with using different calibration signal frequencies, and more than one LUT can be generated in order to be used when the target frequency is changed. For instance, LUT for 8GHz, 10GHz and 11 GHz can be generated, and recorded. When target frequency is 8 GHz, LUT of 8 GHz can be utilized.

During the calibration, the signal power range to be applied, is very limited. Although the power detector in this paper has the highest dynamic range in the literature, further improvements in this area are required. For instance, the techniques in this thesis and at [74] can be combined.

The objective of this thesis was not to design a state of the art ADC. Straightforward design techniques are used in these circuits, however, overall performance of the system is reduced in second prototype. As part of the future works, differential topologies can be chosen for the ADC, and design of this circuit can be improved. Designing a state of the art DPU was also not the primary focus of this thesis. This circuit is designed only for research purposes, and further optimizations can be applied on this circuit especially in terms of speed and die area.

Measurement results also show that, using a CB-CE selection based BALUN does not provide accurate 180° of phase shift with a low amplitude error. In future works, design of the phase shifter can be updated by using different approaches for BALUN stage, such as completely differential circuit [51] or a passive transformer.

Heretofore, the proposed method is demonstrated in two approaches. In first approach, ADC and DPU is a completely integrated to the circuit. In second approach, an off-chip connected FPGA is used for the functions of ADC and DPU. The proposed calibration method can also be applied on computation level, and the concept can be restricted to the utilization of the front end circuits of the first prototype.

In addition to the future works, this idea can also be implemented at IHP 13S technology in which noise figure will be significantly lower, and the circuit area will be lower than 2.6 mm^2.

To conclude, through utilization of proposed calibration technique, the first 7-bit phase shifter in literature is designed in SiGe-BiCMOS process. In addition, proposed calibration technique enables the flexibility of tuning the center frequency, which is a new competence for phase shifters. As the first impact of this competence, to the best of author's knowledge, proposed PS has the highest fractional bandwidth for a PS with phase

resolution of 6-bit or higher in literature. Proposed technique also enables to control the amplitude of phase shifter, and reduce amplitude errors. However, the insertion loss is higher than its counterparts in literature, because of the coupler in signal path. Proposed technique does not have additional static power consumption; However, power consumption instantaneously increase during calibration. The area consumption is higher, due to the technology limitations on the area of digital circuit. The proposed technique is a strong candidate to be used in phase shifters for high accurate phased array RADAR systems.

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Appendix

```
clc
clear all;
close all;

all_angle_errors=zeros (100,16);

tic
for z=1:1:1
   A=1; %ilk vektör boyu
   amp=zeros([1,16]);%ideal boylar
   phs=zeros([1,16]);%ideal fazlar
   sum_ampl=zeros([1,16]);

   for i=1:1:16
      amp(i)=A*tan((45-(i-1)*2.8125)*2*pi/360); %saat yönünde 90 dereceden 45 dereceye dönmek için x eksenli vektörlerin boyları
   end

   % faz hatası olduğunda daha fazla ara vektör kullanılacak, 4 kat olsun

   ampl_non=zeros([1,64]);% boylar
   phs_non=zeros([1,64]);% fazlar
   difference=zeros([1,64]);
   index_array=zeros([1,16]);

   angle=xlsread('gainfaz2.xlsx', 'A:A');
   ampl_non= 10.^(xlsread('gainfaz2.xlsx', 'B:B')/20)/2.6351; %dB to normalize, normalize to first to 1 2.6351 ya da 3.1326 'a oranla
   phs_non= 2*pi/360*(xlsread('gainfaz2.xlsx', 'C:C')-90);%dereceden radyana dönüşüm, 90'dan çıkarılıyor


   % ***************************NON IDEAL VEKTÖRLERİN ÇİZİMİ*****************
   figure

   for i=1:1:64 %ikinci vektörlerin faz ile çizimi
      p0=[0,0];
      x=ampl_non(i)*cos(phs_non(i));
```

```
   y=ampl_non(i)*sin(phs_non(i));
   p1=[x,y];
   vectarrow(p0,p1)
   hold on;
end
%% ************************END NON IDEAL VEKTÖRLERİN ÇİZİMİ*****************

for j=1:1:64 %bütün ara vektörler için bak
      x=ampl_non(j)*cos(phs_non(j));
      y=ampl_non(j)*sin(phs_non(j));
      sum_ampl_non(j)=sqrt(x^2+(1+y)^2);% non_ideal_vektör boyu
      angle_non_ideal(j)=atan(x/(y+1))*360/2/pi;
end

%*******************************ERROR PART*******************************

ampl_non_dB=zeros([1,64]);
sum_ampl_non_dB=zeros([1,64]);
factor_error=0.01; %max kaç dB error factor/2 mean hata

%meas_err=factor_error*rand(1,64); %random error uniform distribution
meas_err=factor_error*randn(1,64); %random error gaussian distribution !!!!!
%sum_ampl_non_dB=20.*log10(sum_ampl_non)+ meas_err; %dB cinsi, ekle
sum_ampl_non=sum_ampl_non+meas_err; %decimale dön

meas_err2=factor_error*randn(64,1); %random error gaussian distribution    !!!!
%ampl_non_dB=20.*log10(ampl_non)+ meas_err2; %dB cinsi, ekle
ampl_non=ampl_non+meas_err2; %decimale dön
%*******************************END ERROR PART****************************
%********************QUANTIZATION PART************************************
factor=1/0.01; %1/factor dB cinsinden ölçüm hassasiyeti
ampl_non_rounded=round(ampl_non*factor)/factor;
sum_ampl_non_rounded=round(sum_ampl_non*factor)/factor;
%*********************END QUANTIZATION************************************

for k=1:1:16 % İDEAL OLMAYAN toplam vektörünün min error bulunması
   min=1000;%min vektör boyu 45 derece için ilk değer al
   cosine=cos((45-(k-1)*2.8125)*2*pi/360);
   for j=1:1:64 %bütün ara vektörler için bak
      %sum_ampl_non(j)=sqrt(x^2+(1+y)^2);% non_ideal_vektör boyu, ölçümden gelecek
```

```
        %difference (j) = abs(sum_ampl_non(j)^2 + 1^2 - ampl_non(j)^2 - 2*1*sum_ampl_non(j)*cosine);
        difference (j) = abs(sum_ampl_non_rounded(j)^2 + 1^2 - ampl_non_rounded(j)^2 -
2*1*sum_ampl_non_rounded(j)*cosine);
        if (difference(j)<=min) %min hatayla karşılaştır
           index=j; %min hata endeksini güncelle
           min=difference(j);%yeni min değer
        end
      end
      index_array(k)=index; % min error için endeksler
   end


   for i=1:1:16
   angle_error(i)=angle_non_ideal(index_array(i))-(45-(i-1)*2.8125); % açı hatası hesabı
   final_vector_ampl(i)=20*log10(sum_ampl_non(index_array(i)));

   end
%    figure;
%    plot (angle_error);
%    hold on;
   all_angle_errors(z,:)=angle_error;
   rms_angle_err(z)=sqrt(angle_error*angle_error'/16)

end

figure;
plot (max(abs(all_angle_errors)));
hold on;



figure;
plot (rms_angle_err);
hold on;
max(rms_angle_err)

toc
```